V536-H/V526 Professional Camera SoC Datasheet

Revision 1.6

Jan. 9, 2023

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Revision History

Revision	Date	Description
1.0	Apr.22,2019	Initial release version
1.1	May.21,2019	Add V526 information
1.2	Jul.16,2019	BT656/BT1120 resolution is added in section 8.1.1
1.3	Jun.07,2021	Refresh the specification for V526
1.4	Oct.08,2021	Modify V536 to V536-H.
1.5	Apr.20,2022	Add absolute maximum ratings in section 2.3
1.6	Jan. 9, 2023	Update RMII and RGMII timing figures and parameter tables in sections 2.5.6.1 and 2.5.6.2. Update the block diagram in section 6.2. Update the minimum value of **Setup time in Stop** under fast mode in **Table 2-54 TWI Timing Constants** in section 2.5.12

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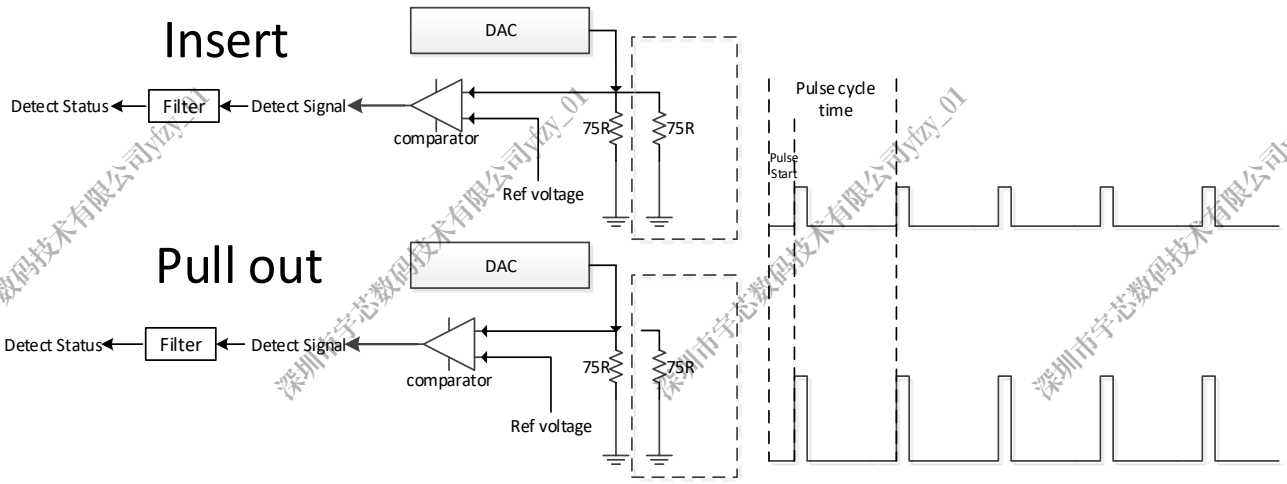

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About This Document

Purpose

This document describes the features,logical structures,functions,operating modes,and related registers of each module about V536-H/V526. The document also describes the interface timings and related parameters in diagrams.In addition,the document describes the pins,pin usages,performance parameters, and package dimension of V536-H/V526 in detail.

Related Versions

The following describes the product versions related to the document.

Product Name	Version
V536-H	/
V526	/

Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
CAUTION	A caution means that damage to equipment is possible.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear,clear the bit automatically when the operation of complete. Writing 0 has no effect.
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear. Writing 1 has no effect
R/W1C	Read/Write 1 to Clear. Writing 0 has no effect
R/W1S	Read/Write 1 to Set. Writing 0 has no effect
W	Write Only

Reset Value Conventions

In the register definition tables:

If other column value in a bit or multiple bits row is "/", that this bit or these multiple bits are unused.

If the default value of a bit or multiple bits is "UDF", that the default value is undefined.

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency,data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary(register description is excluded.)
X	00X,XX1	In data expression,X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

Acronyms and Abbreviations

The following table contains acronyms and abbreviations used in this document.

ADC	Analog-to-Digital Converter
AE	Automatic Exposure

AEC	Audio Echo Cancellation
AES	Advanced Encryption Standard
AF	Automatic Focus
AGC	Automatic Gain Control
AHB	AMBA High-Speed Bus
ALC	Automatic Level Control
ANR	Active Noise Reduction
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
AVS	Audio Video Standard
AWB	Automatic White Balance
BROM	Boot ROM
CIR	Consumer Infrared
CMOS	Complementary Metal-Oxide Semiconductor
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
CVBS	Composite Video Broadcast Signal
DDR	Double Data Rate
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DVFS	Dynamic Voltage and Frequency Scaling
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
FBGA	Fine Ball Grid Array
FEL	Fireware Exchange Launch
FIFO	First In First Out
GIC	Generic Interrupt Controller
GPIO	General Purpose Input Output
HD	High Definition
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HiSPI	High-Speed Serial Pixel Interface
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
ISP	Image Signal Processor
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
KEYADC	Analog to Digital Converter for Key

LCD	Liquid-Crystal Display
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MIC	Microphone
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MSB	Most Significant Bit
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
NVM	Non Volatile Storage Medium
OHCI	Open Host Controller Interface
OSD	On-Screen Display
OTP	One Time Programmable
OWA	One Wire Audio
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
R	Read only/non-Write
RGB	Read Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RSA	Rivest-Shamir-Adleman
RTC	Real Time Clock
SAR	Successive Approximation Register
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDRAM	Sychronous Dynamic Random Access Memory
SDXC	Secure Digital Extended Capacity
SLC	Single-Level Cell
SoC	System on Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TDES	Triple Data Encryption Standard
TFBGA	Thin Fine Ball Grid Array
TWI	Two Wire Interface
UART	Universal Asynchronous Receiver Transmitter

UDF	Undefined
USB OTG	Universal Serial Bus On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

Chapter 1 Product Description

1.1. Device Difference

V536-H/V526 is configured with different sets of features in different devices. The feature difference across different devices are shown in Table 1-1.

Table 1-1. Device Difference

Contents	V536-H	V526
SDRAM	32-bit width	16-bit width
Video encoder	Maximum resolution: 3840 x 2160	Maximum resolution: 2688 x 1600
Video decoder	Maximum resolution: 3840 x 2160	Maximum resolution: 2688 x 1600
ISP	Maximum resolution: 4224 x 3168	Maximum resolution: 2688 x 1600
HDMI	Maximum resolution: 3840 x 2160	Not support

1.2. V536-H/V526 Description

1.2.1. V536-H

The V536-H is a high performance and low-power 4K Ultra HD SoC for the video encoding industry that can be widely used in security monitor, SDV, driving recorder, Police BODY-WORN CAMERA, etc. The V536-H integrates dual-core ARM Cortex-A7 that supports frequency up to 1.2GHz. Integrated H.264/H.265 video encoding processor that supports encoding of multiple streams, the performance of video encoding/decoding up to 4K@30fps + VGA30fps. The V536-H integrates the latest generation of ISP image processor, which supports 3A/3DNR/multi-frame wide dynamic range and other image enhancement algorithms, supports EISE, Wide-angle distortion correction, fisheye and PTZ calibration and other image correction algorithms to achieve professional image effects. The V536-H supports multiple video input interface, such as HiSPi/Sub-LVDS/MIPI-CSI/Combophy, and also supports multiple video output interface, such as RGB/MIPI/HDMI/CVBS. The Allwinner SDK features high stability and ease of use, supports driving recoder and 4K action cameras for rapid mass production.

1.2.2. V526

The V526 is a high performance and low-power 2K Ultra HD SoC for the video encoding industry that can be widely used in security monitor, SDV, driving recorder, Police BODY-WORN CAMERA, etc. The V526 integrates dual-core ARM Cortex-A7 that supports frequency up to 1.2GHz. Integrated H.264/H.265 video encoding processor that supports encoding of multiple streams, the performance of video encoding/decoding up to 2K@30fps. The V526 integrates the latest generation of ISP image processor, which supports 3A/3DNR/multi-frame wide dynamic range and other image enhancement algorithms, supports EISE, Wide-angle distortion correction, fisheye and PTZ calibration and other image correction algorithms to achieve professional image effects. The V526 supports multiple video input interface, such as HiSPi/Sub-LVDS/MIPI-CSI/Combophy, and also supports multiple video output interface, such as RGB/MIPI/CVBS. The Allwinner SDK features high stability and ease of use, supports driving recoder and 2K action cameras for rapid mass production.

1.3. Application Scenarios

1.3.1. 4K/2K Camera Solution

The typical application scenario of the V536-H/V526 is shown in Figure 1-1.

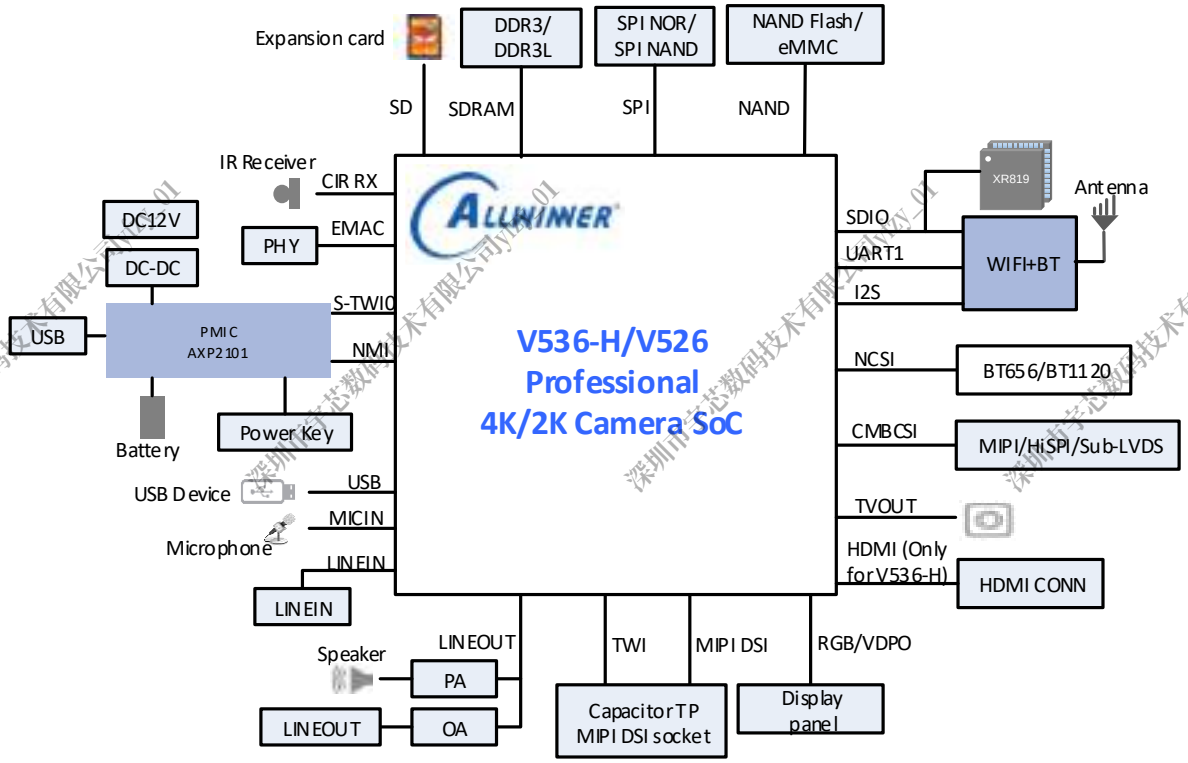


Figure 1-1. V536-H/V526 Application Diagram

1.4. Architecture

1.4.1. Overview

The logic block diagram of the V536-H is shown in Figure 1-2.

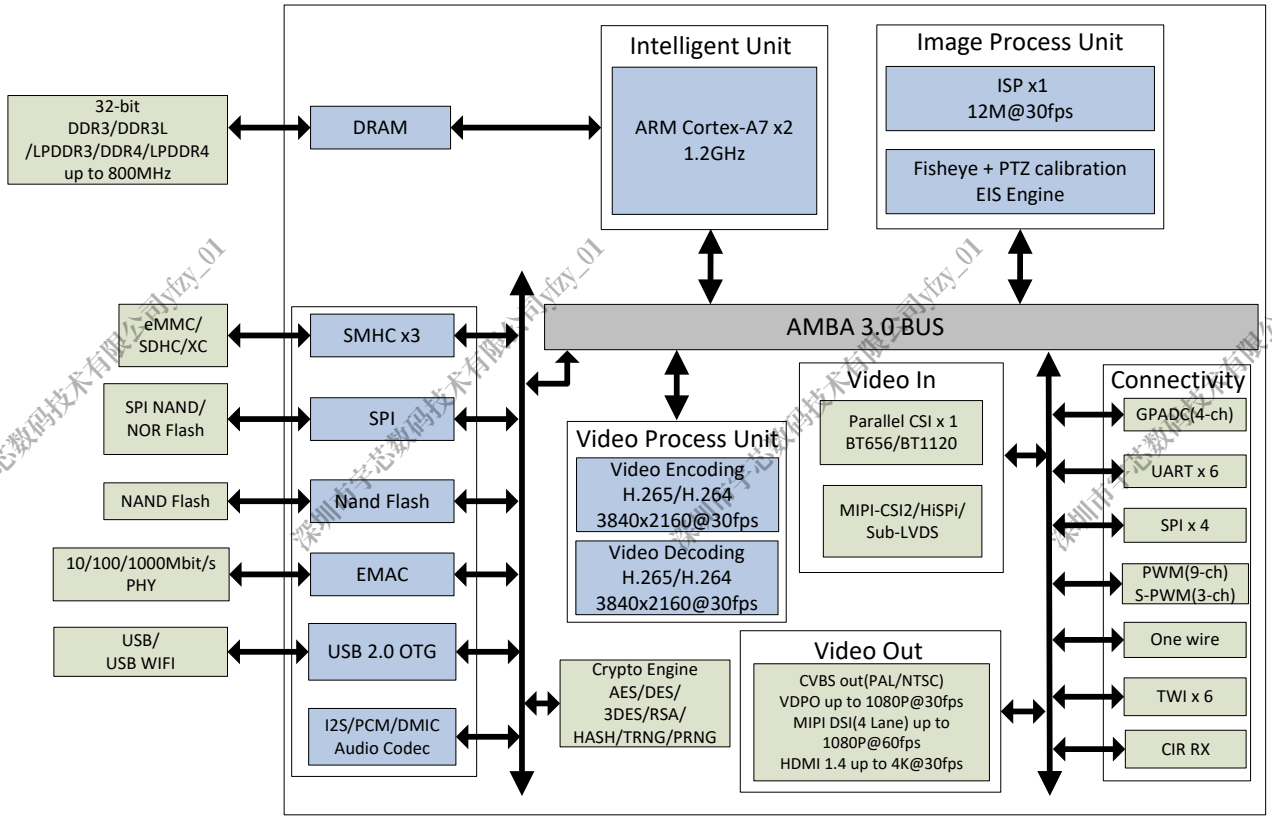


Figure 1-2. V536-H Logic Block Diagram

The logic block diagram of the V526 is shown in Figure 1-3.

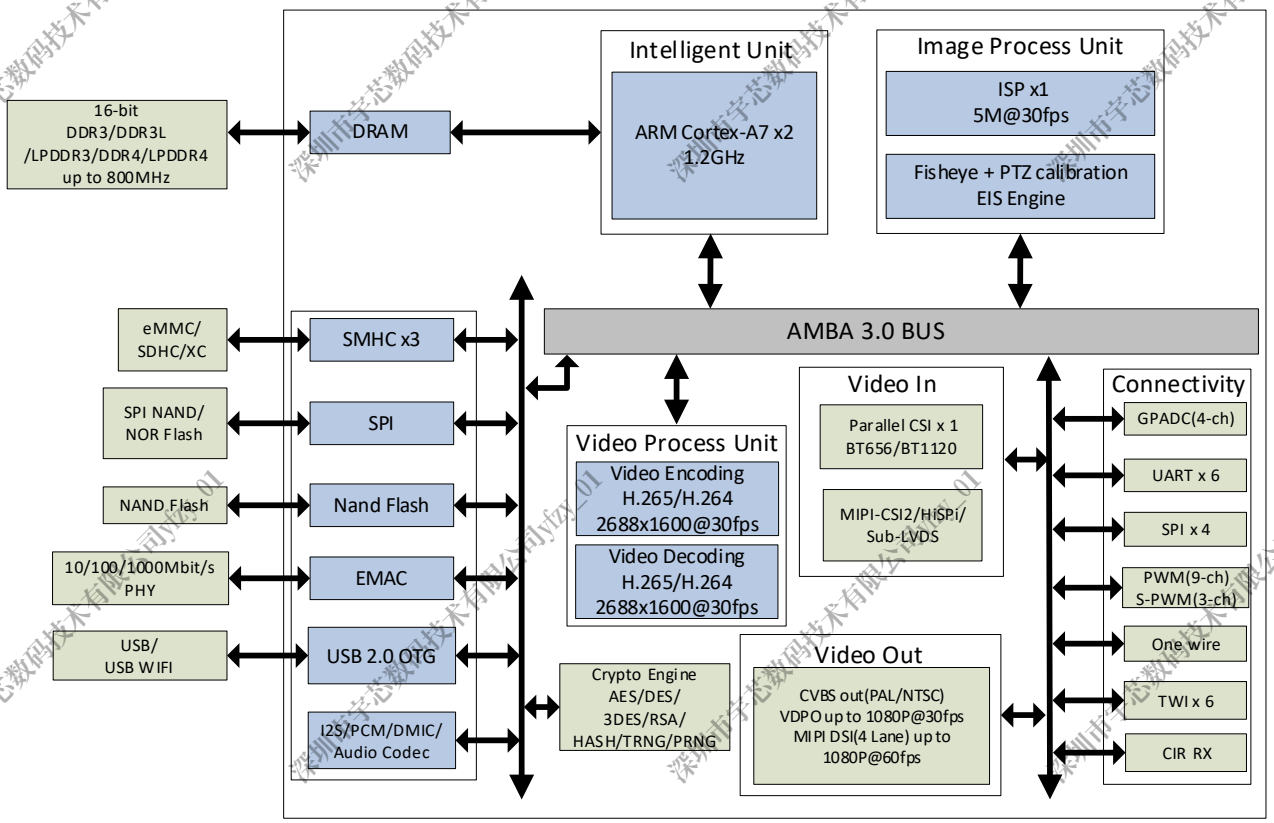


Figure 1-3. V526 Block Diagram

1.4.2. Processor Core

- Dual-core ARM Cortex™-A7@1.2GHz
- ARMv7 ISA standard ARM instruction set
- Thumb-2 Technology
- Jazeller RCT
- NEON Advanced SIMD
- VFPv4 floating point
- Large Physical Address Extensions (LPAE)
- Supports dynamic frequency scaling
- 32KB L1 Instruction cache and 32KB L1 Data cache per core
- 256KB L2 cache shared

1.4.3. Video Encoding Specifications

- H.264 BP/MP/HP
- H.265 MP
- H.264/H.265 supports I/P frame, dual-P frame
- MJPEG/JPEG baseline

1.4.4. Video Encoding Performance

- **V536-H**: maximum resolution of 3840 x 2160 for H.264/H.265 encoding
  V526: maximum resolution of 2688 x 1600 for H.264/H.265 encoding
- Real-time multiple streams H.264/H.265 encoding capability:
  V536-H: 3840 x 2160@30fps + VGA@30fps + 3840 x 2160@1fps snapshot
  V526: 2688 x 1600@30fps snapshot
- JPEG snapshot performance of 1080p@60fps independently
- Supports the constant bit rate (CBR)/variable bit rate (VBR) bit rate control mode, ranging from 2kbit/s to 100Mbit/s
- Encoding of eight regions of interest (ROIs)
- Encoding frame rate ranging from 1/16fps to 60fps

1.4.5. Video Decoding Specifications

- H.264 BP/MP/HP
- H.265 MP
- MJPEG/JPEG MP

1.4.6. Video Decoding Performance

- **V536-H**: H.264/H.265 decoding maximum resolution of 3840 x 2160
  V526: H.264/H.265 decoding maximum resolution of 2688 x 1600
- H.264/H.265 decoding maximum bit rate of 60Mbit/s
- **V536-H**: H.264/H.265 decoding performance of 3840 x 2160@30fps
  V526: H.264/H.265 decoding performance of 2688 x 1600@30fps
- JPEG decoding performance of 1080p@100fps independently

1.4.7. Video and Graphics Processing

- Lens distortion correction, fisheye (wall mounting/top mounting/bottom mounting) and PTZ calibration
- Real-time stitch for two-channel images (panoramic 360^0, wide angle 180^0)
- Picture rotation by 90^0, 180^0 or 270^0
- Supports Electronic Image Stabilization Engine (EISE)
- EISE: support frame rate up to 1080p@60fps
- Supports 2 Video channels,up to 4K@30fps
- Supports 2 UI channels, up to 1080p@60fps
- Blending of 2 Video channels and 2 UI channels
- Supports SmartColor for excellent display experience

1.4.8. ISP&VIPP

- One image signal processor (ISP)

- **V536-H**: maximum 4224 x 3168 resolution;
  V526: maximum 2688 x 1600 resolution
- Adjustable 3A functions, including automatic exposure (AE), automatic white balance (AWB) and automatic focus (AF)
- Highlight compensation, backlight compensation, gamma correction and color enhancement
- Defect pixel correction, 2D/3D denoising
- Sensor build-in WDR, 2F-line base WDR, local tone mapping
- 1/64 to 1x scaling output for 4 channels, among 2 channels supports frame buffer compress
- On-screen display (OSD) overlay pre-processing for 8 regions and cover for 8 regions
- Graphics mirror and flip
- ISP tuning tools for the PC
- Dual Video Input Post Processor(VIPP)
- Supports image interception
- The output scaling of width is 1/8 ~ 1x
- The ouput scaling of height is 1/8 ~ 1x

1.4.9. Security Engine

- Encryption and decryption algorithms implemented by using hardware, including AES, DES and 3DES
- Signature and verification algorithms implemented by using hardware, including RSA512/1024/2048/3072/4096 bits
- HASH tamper proofing algorithms implemented by using hardware, including MD5/SHA/HMAC
- Hardware true random number generator (TRNG) and hardware pseudo random number generator (PRNG)
- Integrated 2Kbits efuse storage space

1.4.10. Video Interfaces

1.4.10.1. **Input**

- One combo sensors input
- Main channel supports 4 lane mobile industry processor interface (MIPI), 12 lane sub low-voltage differential signaling (sub-LVDS), and 4 lane high-speed serial pixel interface (HiSPI)
- Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, Omni Vision and Panasonic
- BT.601, BT.656 and BT.1120 video input interfaces

1.4.10.2. **Output**

- One phase alternating line (PAL)/national television systems committee (NTSC) for automatic load detection
- One BT.1120/BT.656 video output interface
- One high definition multimedia interface (HDMI) output, up to 4K@30fps (Only for V536-H)
- One MIPI digital serial interface (DSI) output, up to 1920 x 1080@60fps
- One RGB output

1.4.11. Audio Interfaces

- Integrated audio codec, supporting 20-bit audio input and output
- Inter-IC sound (I2S)/time division multiplex (TDM) interface for connecting to an external audio codec
- Dual channel microphone differential input for reducing noise

1.4.12. Peripheral Interfaces

- One internal RTC
- Four channels general purpose analog-to-digital converter (GPADC)
- 6 UART interfaces
- 4 SPI interfaces
- 12-ch PWM Controller (CPUX:9, CPUS:3)
- Three SD3.0/SDIO3.0 interfaces,supporting secure digital extended capacity (SDXC)
- One USB2.0 OTG interface
- RGMII in 10/100/1000 Mbit/s full-duplex or half-duplex mode, RMII in 10/100 Mbit/s full-duplex or half-duplex mode
- Six TWI interfaces, one one-wire interface, one CIR RX interface, 126 GPIO interfaces

1.4.13. External Memory Interfaces

- DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 interface
  - Supports 32/16-bit DDR3/DDR3L, up to 800 MHz
  - Supports 32/16-bit LPDDR3, up to 800 MHz
  - Supports 32/16-bit DDR4, up to 800 MHz
  - Supports 32/16-bit LPDDR4, up to 800 MHz
- SPI Nor Flash interface
  - 1-, 2-, 4-wire mode
  - 3 bytes or 4 bytes address mode
- SPI Nand Flash interface
- eMMC 5.0 interface
- Nand Flash interface
  - 8-bit data width
  - 16-,24-,28-,32-,40-,44-,48-,52-,56-60-,64-,68-,72-,80-bit ECC
  - SLC/MLC/TLC flash and EF-NAND memory
- Booting from SPI NOR, SPI NAND, eMMC, SD, USB, UART or RAW NAND, one-key FEL
- Hardware boot pin select

NOTE

V526 only supports 16-bit DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 interface.

1.4.14. Physical Specifications

- Power consumption

  - TBD
  - Multi-level power-saving mode
- Operating voltages
  - 0.9V core voltage
  - 3.3V IO voltage
  - 1.5V, 1.35V, 1.2V, 1.2V or 1.1V for DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 interface
- Package
  - Restrictions on the use of certain hazardous substances (RoHS), thin&fine-pitch ball grid array (TFBGA)
  - Body size of 14 mm x 14 mm, 0.5 mm ball pitch

1.5. Boot Modes

The V536-H/V526 can boot from the following devices:

- SD/eMMC
- NAND FLASH
- SPI NOR
- SPI NAND
- USB
- UART

During power-on reset, the boot mode despends on the values of BOOT_SEL[5:0] and FEL, the details are shown in Table 1-2.

Table 1-2. Boot Select Setting and Boot Media

BOOT_SEL[5:0]	FEL	Boot Media
XXXXX0	0	Booting from UART
XXXXX1	0	Booting from USB
11111X	1	SMHC0 -> MLC NAND -> SLC NAND
11110X	1	SMHC0 -> SLC NAND ->MLC NAND
11101X	1	SMHC0 -> eMMC USER -> eMMC BOOT
11011X	1	SMHC0 -> eMMC BOOT ->eMMC USER
10111X	1	SMHC0 -> SPI_NOR
01111X	1	SMHC0 -> SPI NAND

NOTE

X indicates not concerned about the value.

Chapter 2 Hardware

2.1. Package and Pinout

2.1.1. Package

The V536-H/V526 uses the TFBGA package, it has 412 pins, its body size is 14 mm x 14 mm, and its ball pitch is 0.5 mm pitch. Figure 2-1 shows the top view of the 14 mm x 14 mm package, Figure 2-2 shows the bottom view of the 14 mm x 14 mm package , and Figure 2-3 shows the side view of the 14 mm x 14 mm package, Figure 2-4 shows the enlarged view of detail “A” in the side view. Figure 2-5 shows the dimensions of the 14 mm x 14 mm package .

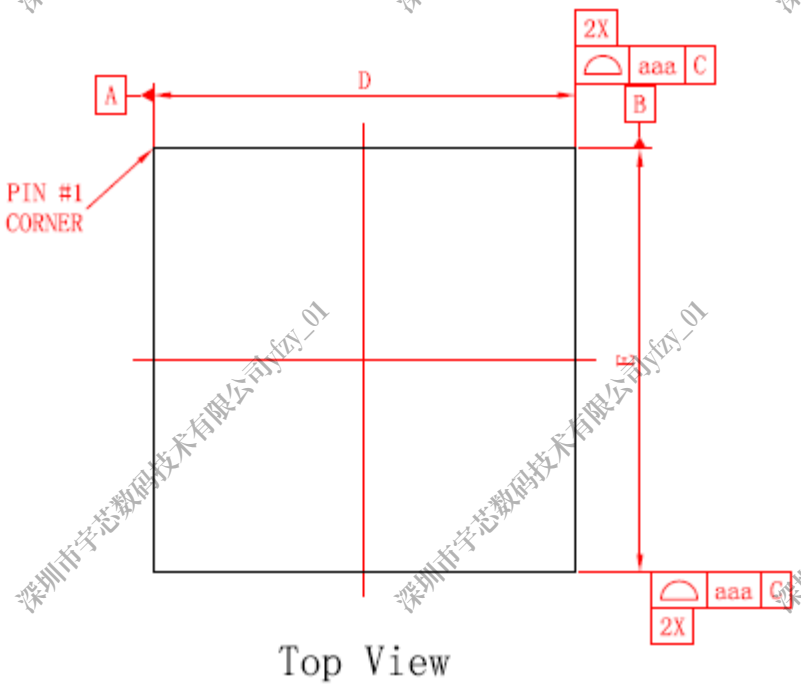


Figure 2-1. 14 mm x 14 mm Package Top View

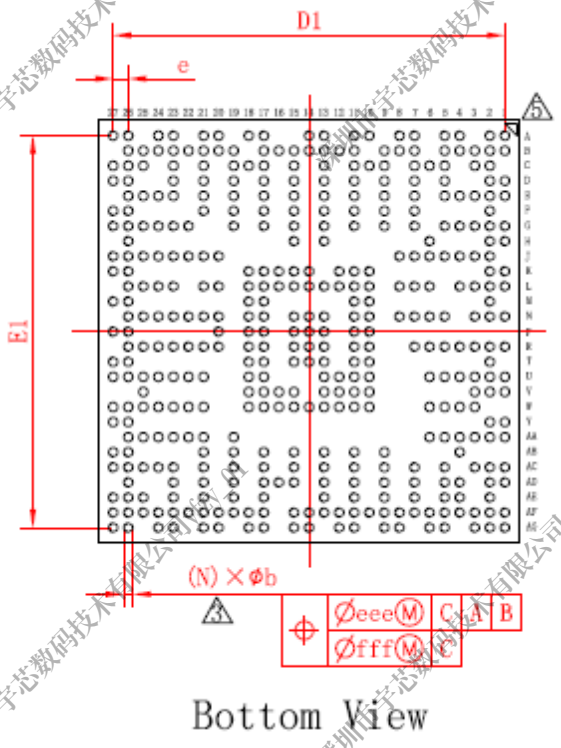


Figure 2-2. 14 mm x 14 mm Package Bottom View

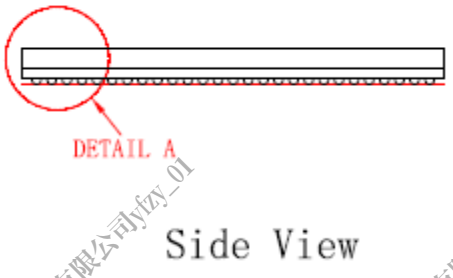


Figure 2-3. 14 mm x 14 mm Package Side View

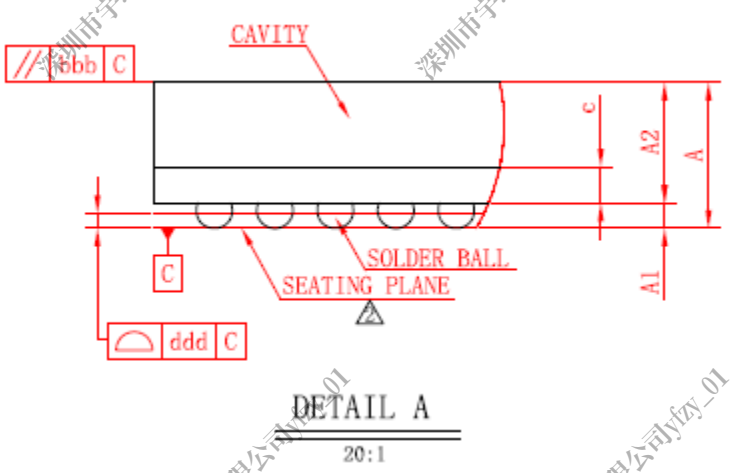


Figure 2-4. Enlarged View of Detail "A"

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.310	—	—	0.052
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.950	1.000	1.050	0.037	0.039	0.041
c	0.260	0.300	0.340	0.010	0.012	0.013
D	13.900	14.000	14.100	0.547	0.551	0.555
E	13.900	14.000	14.100	0.547	0.551	0.555
D1	—	13.000	—	—	0.512	—
E1	—	13.000	—	—	0.512	—
e	—	0.500	—	—	0.020	—
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.300			0.012		
N	412			412		
MD/ME	27/27			27/27		

Figure 2-5. 14 mm x 14 mm Package Dimensions

2.1.2. Pin Quantity

Table 2-1 lists the pin quantity of the V536-H/V526.

Table 2-1. Pin Quantity

Pin Type	Quantity
I/O	278
Power	31
GND	93
DDR Power	10
Total	412

2.2. Pin Description

For details about pin description,see the *V536-H_PINOUT_EN* and *V526_PINOUT_EN.*

2.3. Electrical Characteristics

2.3.1. Power Consumption Parameters

If you have questions about power consumption parameters, contact Allwinner FAE.

2.3.2. Thermal Resistance Parameters

Table 2-2 shows thermal resistance parameters. The following thermal resistance characteristics is based on JEDEC JESD51 standard, because the actual system design could be different with JEDEC JESD51, the simulating result data is a reference only, please prevail in the actual application condition test.

NOTE

Test condition: four-layer board(2s2p),natural convection, no air flow.

Table 2-2. Thermal Resistance Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Junction-to-Ambient Thermal Resistance	θ_{JA}	-	26.9	-	°C/W
Junction-to-Board Thermal Resistance	θ_{JB}	-	10.56	-	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	-	6.72	-	°C/W

2.3.3. Absolute Maximum Ratings

The device will be damaged if the stresses are beyond the absolute maximum ratings. The following table specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 2-4 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device in these or any other conditions beyond the values in the Section *Operating Conditions* is not implied. Exposure to the absolute maximum rated conditions for extended periods may affect the device reliability.

Table 2-3. Absolute Maximum Ratings

Symbol	Parameter	Min(1)	Max(1)	Unit
AVCC	Power Supply for Analog Part	-0.3	2.16	V
VCC-IO	Power Supply for 3.3 V Digital Part	-0.3	3.96	V
VCC-PC	Digital GPIO C Power	-0.3	3.96	V
VCC-PD	Digital GPIO D Power	-0.3	3.96	V
VCC-PE	Digital GPIO E Power	-0.3	3.96	V
VCC18-PF	1.8V Digital GPIO F Power	-0.3	2.16	V
VCC33-PF	3.3V Digital GPIO F Power	-0.3	3.96	V
VCC-PG	Digital GPIO G Power	-0.3	3.96	V
VCC-PI	Digital GPIO I Power	-0.3	3.96	V
VCC-PL	Digital GPIO L Power	-0.3	3.96	V
VCC18-PLL	Power Supply for System PLL	-0.3	2.16	V
VCC-RTC	Power Supply for RTC	-0.3	2.16	V

VCC33-USB	USB Analog Power		-0.3	3.96	V
VCC-TVOUT	Power Supply for TV		-0.3	2.16	V
VCC-EFUSE	Power Supply for EFUSE Program Mode		-0.3	2.16	V
VCC18-HDMI-DSI-CSI(Only for V536-H)	Power Supply for MIPI DSI Power Supply for Combo CSI0 Power Supply for HDMI		-0.3	2.16	V
VCC18-DSI-CSI(Only for V526)	Power Supply for MIPI DSI Power Supply for Combo CSI0		-0.3	2.16	V
VCC-DRAM	Power Supply for DDR4 IO Domain		-0.3	1.44	V
	Power Supply for DDR3 IO Domain		-0.3	1.8	V
	Power Supply for DDR3L IO Domain		-0.3	1.62	V
	Power Supply for LPDDR3 IO Domain		-0.3	1.44	V
	Power Supply for LPDDR4 IO Domain		-0.3	1.32	V
VDD-DRAM	Power Supply for Digital Part(include Controller and PHY)		-0.3	1.3	V
VDD18-DRAM	DRAM 1.8V Internal PAD Power		-0.3	2.16	V
VDD-CPUS	CPUS Power		-0.3	1.3	V
VDD-CPU	CPU Power		-0.3	1.3	V
VDD-SYS	Power Supply for System		-0.3	1.3	V
V_{ESD}	Electrostatic Discharge(2)	Human Body Model(HBM)(3)	-2000	2000	V
		Charged Device Model(CDM)(4)	-500	500	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(5)		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin(6)		Pass		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.

(5) Based on JESD78E; each device is tested with IO pin injection of ±200 mA at room temperature.

(6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

2.3.4. Operating Conditions

All V536-H/V526 modules are used under the operating conditions contained in Table 2-3.

Table 2-4. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	70	°C
Tj	Junction Temperature Range	-20	-	115	°C
AVCC	Power Supply for Analog Part	1.764	1.8	1.836	V
VCC-IO	Power Supply for 3.3V Digital Part	2.97	3.3	3.63	V
VCC-PC	Power Supply for Port C 1.8V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V

	3.3V voltage				
VCC-PD	Power Supply for Port D 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PE	Power Supply for Port E 1.8V voltage 2.5V voltage 2.8V voltage 3.3V voltage	1.62 2.25 2.52 2.97	1.8 2.5 2.8 3.3	1.98 2.75 3.08 3.63	V
VCC18-PF	Power Supply for Port F 1.8V voltage	1.62	1.8	1.98	V
VCC33-PF	Power Supply for Port F 3.3V voltage	2.97	3.3	3.63	V
VCC-PG	Power Supply for Port G 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PI	Power Supply for Port I 1.8V voltage 2.8V voltage 3.3V voltage	1.62 2.52 2.97	1.8 2.8 3.3	1.98 3.08 3.63	V
VCC-PL	Power Supply for Port L 3.3V voltage	2.97	3.3	3.63	V
VCC18-PLL	Power Supply for System PLL	1.62	1.8	1.98	V
VCC-RTC	Power Supply for RTC	1.62	1.8	1.98	V
VCC33-USB	Power Supply for USB	3.07	3.3	3.6	V
VCC-TVOUT	Power Supply for TV	1.74	1.8	1.86	V
VCC-EFUSE	Power Supply for EFUSE Program Mode	1.8	1.89	1.98	V
VCC18-HDMI-DSI-CSI (Only for V536-H)	Power Supply for MIPI DSI Power Supply for Combo CSI0 Power Supply for HDMI	1.62	1.8	1.98	V
VCC18-DSI-CSI (Only for V526)	Power Supply for MIPI DSI Power Supply for Combo CSI0	1.62	1.8	1.98	V
VCC-DRAM	Power Supply for DDR4 IO Domain	1.14	1.2	1.26	V
	Power Supply for DDR3 IO Domain	1.425	1.5	1.575	V
	Power Supply for DDR3L IO Domain	1.283	1.35	1.45	V
	Power Supply for LPDDR3 IO Domain	1.14	1.2	1.3	V
	Power Supply for LPDDR4 IO Domain	1.06	1.1	1.17	V
VDD-DRAM	Power Supply for Digital Part(include Controller and PHY)	0.87	0.9	0.93	V
VDD18-DRAM	Power Supply for SoC 1.8V Internal PAD	1.71	1.8	1.89	V
VDD-CPUS	Power Supply for CPUS	0.873	0.9	0.927	V
VDD-CPU	Power Supply for CPU	0.81	-	1.08	V
VDD-SYS	Power Supply for System	0.92	0.94	0.96	V

2.3.5. Power-On and Power-Off Sequences

Figure 2-6 shows an example of the power on sequence for V536-H/V526 device. The description of the power on sequence is as follows.

- The consequent steps in power on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage,unless stated otherwise.
- VCC-RTC should remain powered on continuously,to maintain internal real-time clock status.And it has to be powered on together with VDD-CPUS,or preceding VDD-CPUS.
- VDD-CPUS should be powered on together, or any time after VCC-RTC.
- 24M clock need to start oscillating and be stable.
- VDD-SYS,VCC-DRAM and VDD-CPUS, VDD-DRAM start to ramp simultaneously.
- Other power domains can ramp after VDD-SYS,VCC-DRAM and VDD-CPUS are stabilized.
- During the entire power on sequence, the RESET pin must be held on low until all power domains are stable.

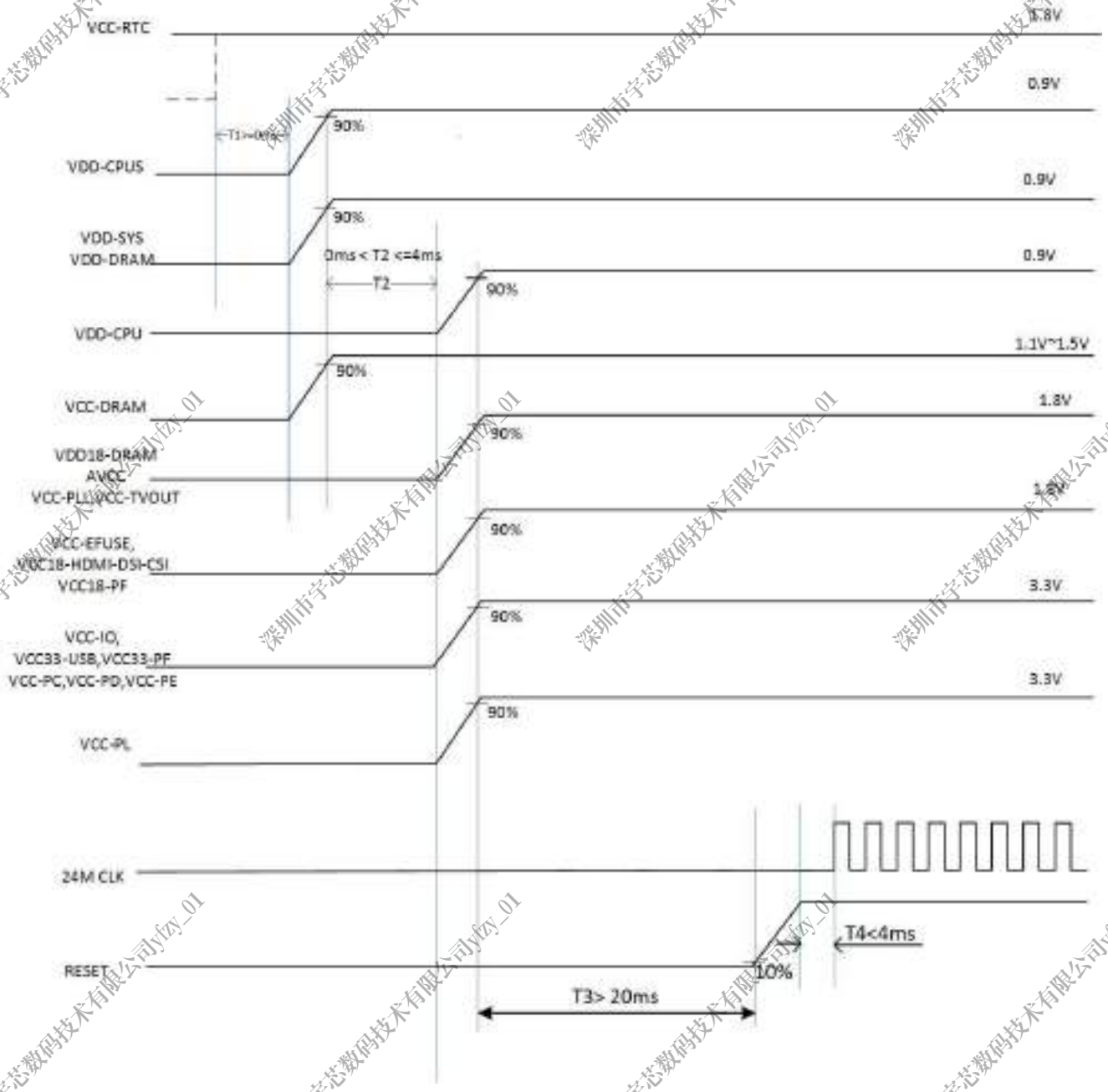


Figure 2-6. V536-H/V526 Power-On Sequence

Figure 2-7 shows an example of the power off sequence for V536-H/V526 device.

- Reset V536-H/V526 device.
- VCC-RTC holds high.
- After PMIC receives the power-down command, pull-down RESET#, and delay T4.
- Other powers start to ramp down simultaneously, and the ramp rate of each power rail is generated by the load on the power.

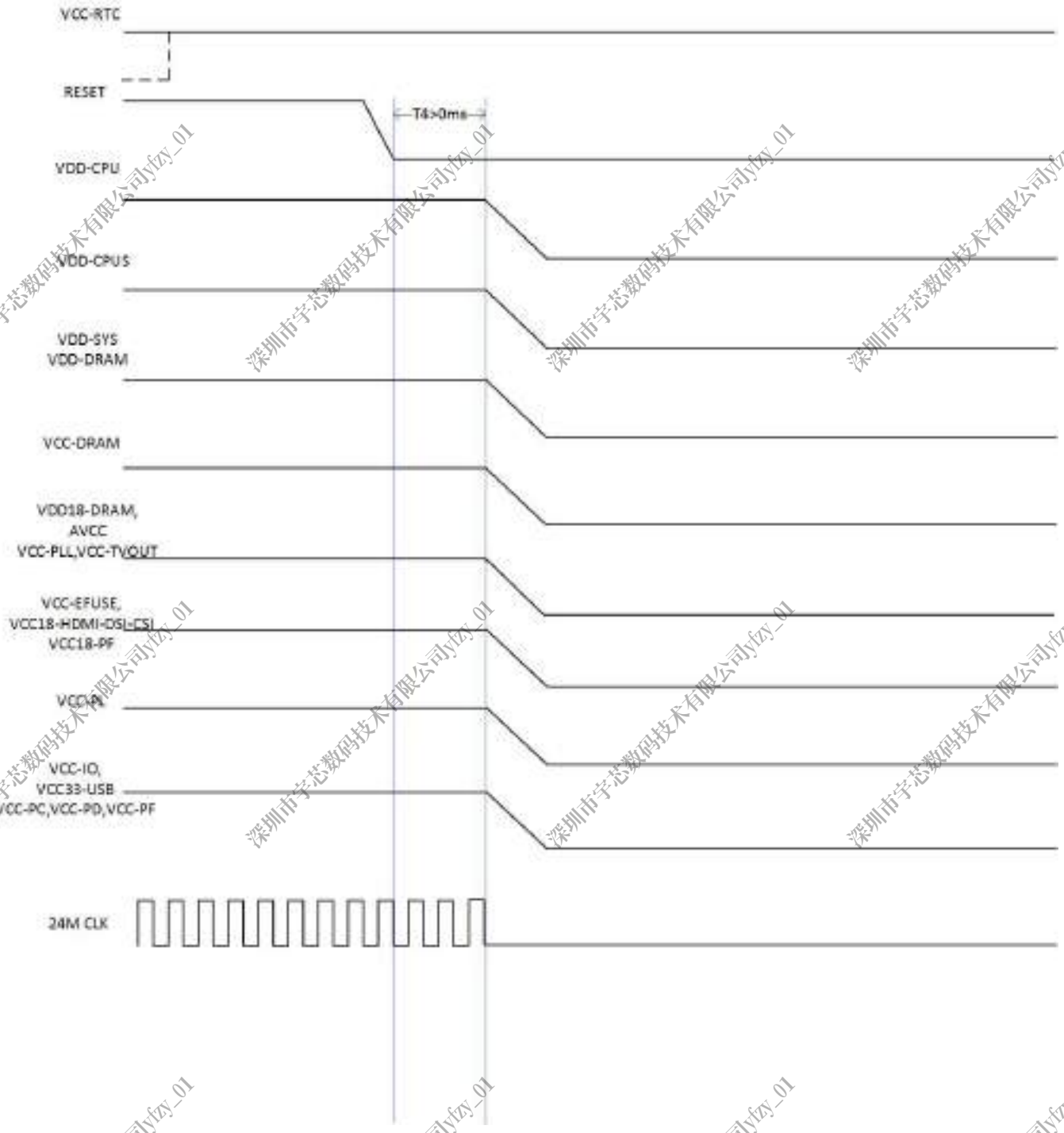


Figure 2-7. V536-H/V526 Power-Off Sequence

2.3.6. DC Electrical Parameters

Table 2-4 summarizes the DC electrical characteristics of the V536-H/V526.

Table 2-5. DC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	80	100	120	kΩ
R_{PD}	Input Pull-down Resistance	80	100	120	kΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO - 0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

2.3.7. SDRAM I/O DC Electrical Parameters

The DDR I/O pads supports DDR3/DDR3L, LPDDR3, DDR4 and LPDDR4 operational modes. The SDRAM Controller(DRAMC) is designed to be compatible with JEDEC-compliant SDRAMs. The DRAMC supports the following memory types:

- DDR3 SDRAM compliant to JESD79-3F DDR3 JEDEC standard release July,2012
- DDR3L SDRAM compliant to JESD79-3-1A DDR3L JEDEC standard release January,2013
- LPDDR3 SDRAM compliant to JESD209-3C LPDDR3 JEDEC standard release August,2015
- DDR4 SDRAM compliant to JESD79-4A DDR4 JEDEC standard release November,2013
- LPDDR4 SDRAM compliant to JESD209-4A LPDDR4 JEDEC standard release November,2015

Table 2-6. DC Input Logic Level

Characteristics	Symbol	Min	Max	Unit
DC input logic high	$V_{IH(DC)}$	V_{ref} +20	-	mV
DC input logic low	$V_{IL(DC)}$	-	V_{ref} –20	mV

Table 2-7. DDR3/DDR3L mode, DC Input Conditions

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Reference Voltage	V_{ref}	V_{DDQ}	30.1%	31.1%	32.1%	Please refer to Note 1 and 2
On-die termination(ODT) programmable resistances	R_{TT}	ohm	-	open, 120, 60	-	Please refer to Note 3

Table 2-8. LPDDR4 and DDR4 mode, DC Input Conditions

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Reference Voltage	V_{ref}	V	-	Variable	-	Please refer to Note 4.
On-die termination(ODT)	R_{TT}	ohm	-	open, 240,	-	Please refer to

programmable resistances				120, 80, 60, 48, 40		Note 5 and 6

Table 2-9. LPDDR4 mode, DC Input Conditions

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Reference Voltage	V_{ref}	V	-	Variable	-	Please refer to Note 4.
On-die termination(ODT) programmable resistances	R_{TT}	ohm	-	open, 240, 120, 80, 60, 48, 40	-	Please refer to Note 5 and 7.

NOTE

1. If the external V_{ref} to the receivers is enabled, V_{ref} is expected to be set to a nominal value of (VDDQ/2)*RxAtten(RxAttenuation for DDR3/DDR3L is 0.623)through a voltage divider in order to track VDDQ level. It can be adjusted in the system to margin the input DQ signals, although this margin does not necessarily represent the eye height since a change in V_{ref} also changes the input receiver common mode, altering receiver performance.

2. Externally supplied V_{ref} is not recommended. Internal V_{ref} generation through local V_{ref} generation at each receiver is preferred.

3. For DDR3, ODT is a Thevenin resistance to $V_{DDQ}/2$.

4. V_{ref} must be set according to the DRAMs loading and termination during reads. Because termination at the DRAMs is configurable, there is no fixed setting. The V_{ref} value is dependent on driver impedance R_{on} and System effective ODT impedence R_{TT}. The V_{ref} value for specific combination of R_{on} and R_{tt} can be calculated from the following equation:

$$V_{ref} = \frac{V_{DDQ}}{2}\left(\frac{2R_{on} + R_{tt}}{R_{on} + R_{tt}}\right)$$

5. ODT is configurable based on DRAM configuration.

6. For DDR4, ODT is a pull-up to V_{DDQ}.

7. For LPDDR4, ODT is a pull-down to V_{SS}.

2.3.8. MIPI/LVDS RX Electrical Parameters

Table 2-9 shows LVDS differential DC electrical parameters.

Table 2-10. LVDS Differential DC Electrical Parameters

Symbol	Parameter		Min	Typ	Max	Unit
V_{IDTH}(SL)	Differential input threshold voltage (V_P-V_M)/2(MIN)	Sub-LVDS	-	-	±25	mV
V_{IDTH}(HS)		HiSPi	-	-	±25	
V_{IDTH}(DP)		D-PHY HS	-	-	±70	
V_{CM}(SL)	Common mode voltage range (V_P+V_M)/2(MIN)	Sub-LVDS	0.5	0.9	1.3	V
V_{CM}(HS)		HiSPi	0.135	0.2	0.275	
V_{CM}(DP)		D-PHY HS	0.07	0.2	0.33	
V_{ISVR}(SL)	Single-ended input voltage	Sub-LVDS	0.4	-	1.4	V
V_{CM}(HS)		HiSPi	-0.165	-	0.575	

V_{CM}(DP)	range V_P,V_M	D-PHY HS	-0.04	-	0.46	
Z_{ID}(SL)	Internal termination resister value	Sub-LVDS	80	100	120	Ω
Z_{ID}(HS)		HiSPi	80	100	125	
Z_{ID}(LV)		LVDS	80	100	120	

Table 2-10 to Table 2-12 show MIPI electrical parameters.

Table 2-11. MIPI High-Speed(HS) DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	mV

Table 2-12. MIPI HS AC Parameters

Symbol	Parameter	Min	Typ	Max	Unit
ΔV_{CMRX} (HF)	Common-mode interface beyond 450MHz	-	-	100	mV
ΔV_{CMRX} (LF)	Common-mode interface 50MHz ~450MHz	-50	-	50	mV
C_{CM}	Common-mode termination	-	-	60	pF

Table 2-13. MIPI Low-Power(LP) DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit
V_{IHLP}	Logic 1 input voltage	880	-	-	mV
V_{ILLP}	Logic 0 input voltage	-	-	550	mV
V_{HYST}	Input hysteresis	25	-	-	mV

2.3.9. SDIO Electrical Parameters

The SDIO electrical parameters are related to different supply voltage.

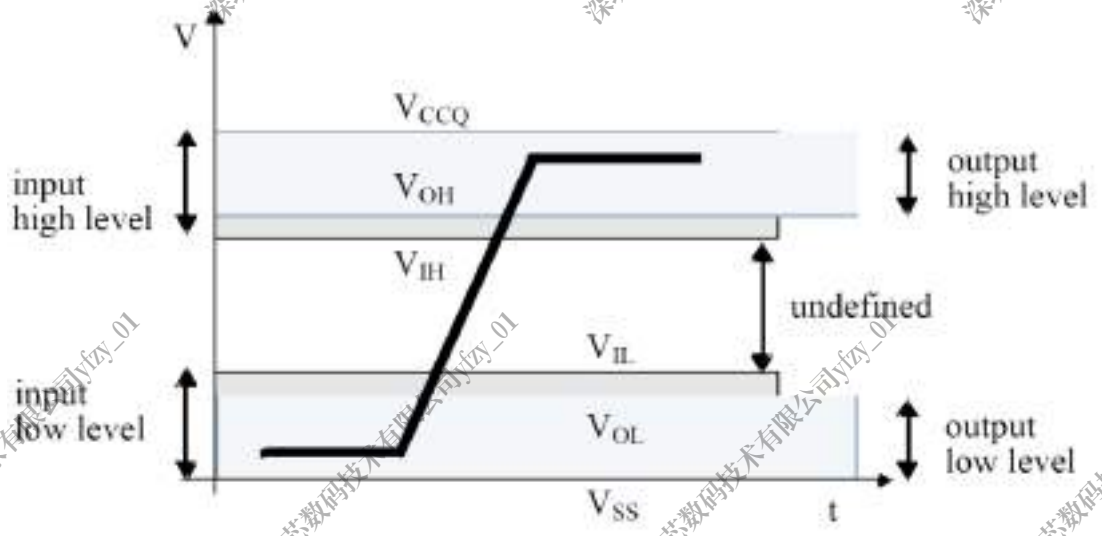


Figure 2-8. SDIO Voltage Waveform

Table 2-13 shows 3.3V SDIO electrical parameters.

Table 2-14. 3.3V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75* V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125* V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625* V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS}- 0.3	-	0.25* V_{CCQ}	V

Table 2-14 shows 1.8V SDIO electrical parameters.

Table 2-15. 1.8V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output HIGH voltage	V_{CCQ} -0.45	-	-	V
V_{OL}	Output LOW voltage	-	-	0.45	V
V_{IH}	Input HIGH voltage	0.625* V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input LOW voltage	V_{SS} - 0.3	-	0.35* V_{CCQ} (2)	V

NOTE

0.7 * VDD for MMC4.3 or lower. 0.3 * VDD for MMC4.3 or lower.

2.3.10. Audio Codec Electrical Parameters

Table 2-15 to Table 2-17 show audio codec electrical parameters.

Test Conditions:

VDD-SYS = 0.9V, AVCC=1.8V, TA=25℃, 1kHz sinusoid signal, fs = 48kHz, 16-bit audio data unless otherwise stated.

Table 2-16. Audio Codec Electrical Parameters

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DAC Path	DAC to LINEOUTL or LINEOUTR(R=10kΩ)					
	Fullscale	0dBFS 1kHz	-	0.55	-	Vrms
	SNR@A	0dB 1kHz	-	96	-	dB
	THD+N	0dB 1kHz	-	-85	-	dB
	Crosstalk	0dB 1kHz	-	-85	-	dB
ADC Path	MIC1 to ADC via ADC mixer					
	SNR@A	1.6Vpp 1kHz 0dB	-	96	-	dB
	THD+N	1.6Vpp 1kHz 0dB	-	-85	-	dB
	SNR@A	70mVpp 1kHz 27dB	-	76	-	dB
	THD+N	70mVpp 1kHz 27dB	-	-76	-	dB
	SNR@A	35mVpp 1kHz 33dB	-	70	-	dB

	THD+N	35mVpp 1kHz 33dB	-	-75	-	dB
	SNR@A	12.5mVpp 1kHz 42dB	-	60	-	dB
	THD+N	12.5mVpp 1kHz 42dB	-	-60	-	dB
	MIC2 to ADC via ADC mixer					
	SNR@A	1.6Vpp 1kHz 0dB	-	96	-	dB
	THD+N	1.6Vpp 1kHz 0dB	-	-85	-	dB
	SNR@A	70mVpp 1kHz 27dB	-	75	-	dB
	THD+N	70mVpp 1kHz 27dB	-	-75	-	dB
	SNR@A	35mVpp 1kHz 33dB	-	70	-	dB
	THD+N	35mVpp 1kHz 33dB	-	-75	-	dB
	SNR@A	12.5mVpp 1kHz 42dB	-	60	-	dB
	THD+N	12.5mVpp 1kHz 42dB	-	-60	-	dB
	LINEINL or LINEINR to ADC via ADC mixer					
	FullScale	1.6Vpp 1kHz 0dB	-	825	-	mFFs
	SNR@A	1.6Vpp 1kHz 0dB	-	96	-	dB
	THD+N	1.6Vpp 1kHz 0dB	-	-85	-	dB
AA path	LINEIN to LINEOUT via output mixer					
	Fullscale	1.6Vpp 1kHz 0dB	-	0.55	-	Vrms
	SNR@A	1.6Vpp 1kHz 0dB	-	100	-	dB
	THD+N	1.6Vpp 1kHz 0dB	-	-90	-	dB
Microphone Bias **NOTE** **2.2uF Capacitor on MBIAS**						
MBIAS	Type Voltage		-	2.2	-	V
	MBIAS current		-	-	2	mA

Table 2-17. Audio Codec Operation Mode

Operation Mode	Test Conditions	AVCC(1.8V)
Music Playback to Lineout	0dB wav 600Ω load	4.0mA
MIC1 Record	0Vpp input signal 42dB Gain	6.9mA
MIC2 Record	1Vpp input signal 42dB Gain	6.8mA
Stereo Linein Record	1Vpp input signal 0dB PGA Gain	5.3mA

Table 2-18. Power Specifications

Parameter	Min	Typ	Max	Unit	Note
AVCC	1.764	1.8	1.836	V	Relative to AGND
VRA1	-	AVCC/2	-	V	Relative to AGND
VAR2	-	AVCC/2	-	V	Relative to AGND
VDD33	3.0	3.3	3.6	V	Relative to GND,MBIAS input voltage

2.4. PCB Design Recommendations

For details about PCB design recommendations, see the *V536-H Hardware Design User Guide* and *V526 Hardware Design User Guide*.

2.5. Interface Timings

2.5.1. SDRAM Interface Timing

2.5.1.1. DDR3/DDR3L Parameters

Figure 2-9 shows the DDR3/DDR3L command and address timing diagram. The timing parameters for this diagram shows in Table 2-18.

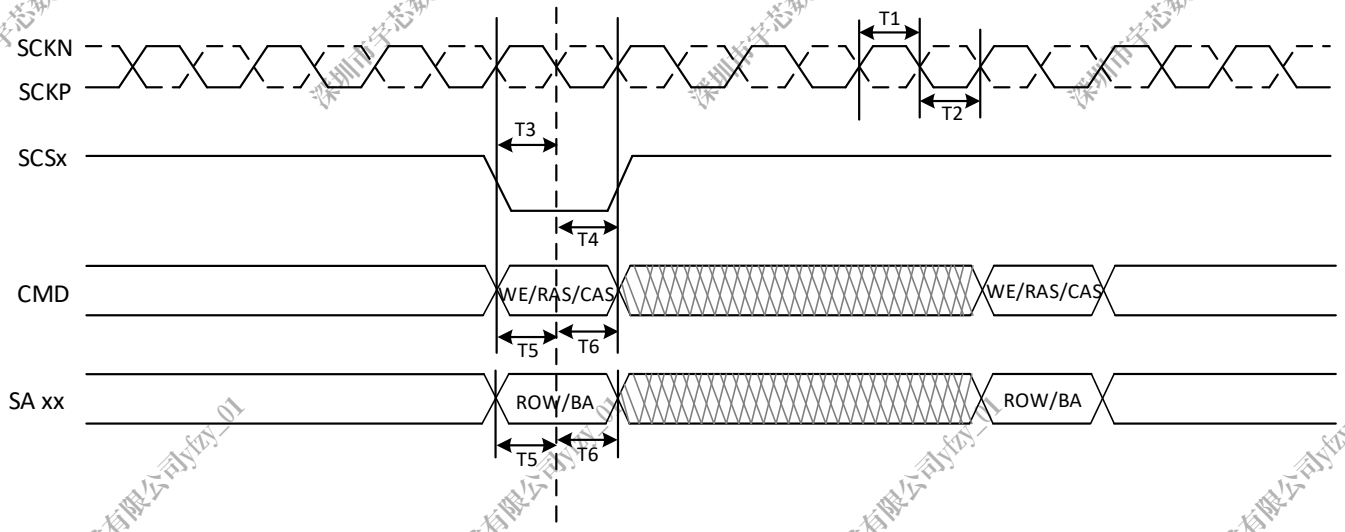


Figure 2-9. DDR3/DDR3L Command and Address Timing

Table 2-19. DDR3/DDR3L Timing Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T1	Clock high-level width	t_{CH}	0.47	-	0.53	tck
T2	Clock low-level width	t_{CL}	0.47	-	0.53	tck
T3	CS setup time	t_{IS}	170	295	-	ps
T4	CS hold time	t_{IH}	120	245	-	ps
T5	Command and Address setup time to Clock edge	t_{IS}	170	295	-	ps
T6	Command and Address hold time to Clock edge	t_{IH}	120	245	-	ps

T1 and T2 are in reference to V_{ref} level.

T3,T4,T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 2-10 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram shows in Table 2-19.

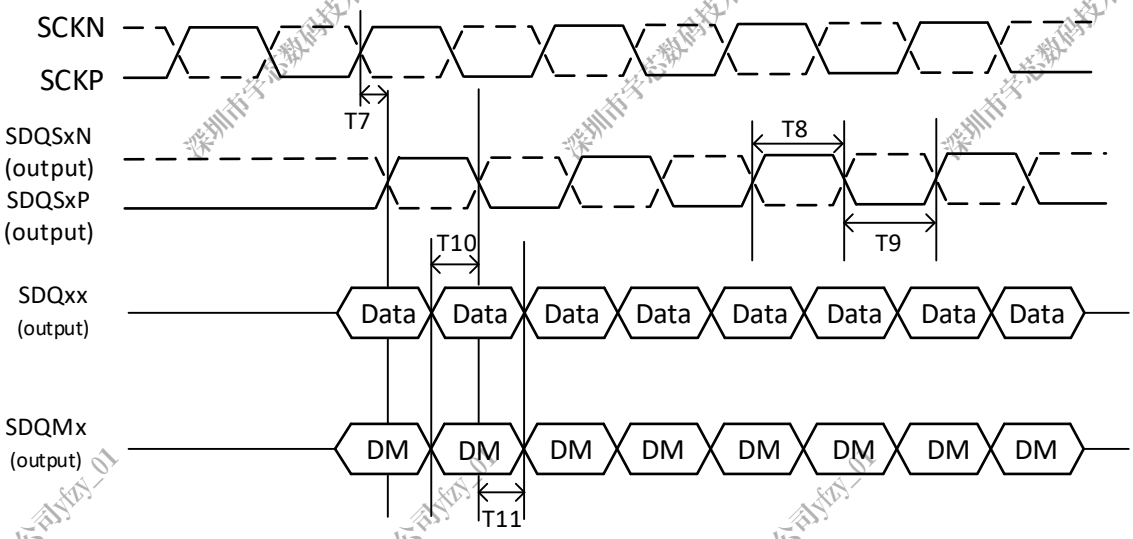


Figure 2-10. DDR3/DDR3L Write Cycle

Table 2-20. DDR3/DDR3L Write Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T7	SDQS rising edge to SCK rising edge	t_{DQSS}	-0.27	-	0.27	t_{CK}
T8	SDQS high level width	t_{DQSH}	0.45	-	0.55	t_{CK}
T9	SDQS low level width	t_{DQSL}	0.45	-	0.55	t_{CK}
T10	Data setup time to SDQS	t_{DS}	10	145	-	ps
T11	Data hold time to SDQS	t_{DH}	45	180	-	ps

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.

T7,T8, and T9 are in reference to V_{ref} level.

T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 2-11 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram shows in Table 2-20.

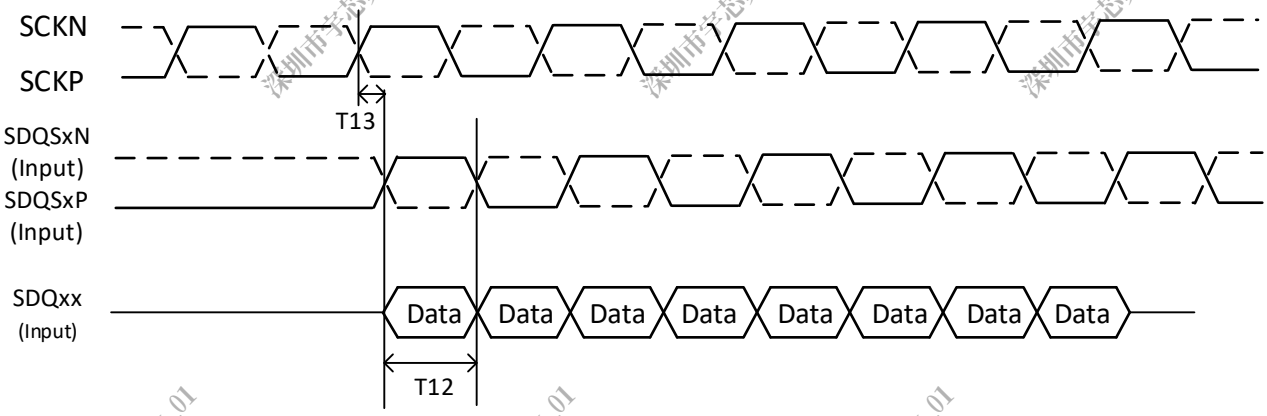


Figure 2-11. DDR3/DDR3L Read Cycle

Table 2-21. DDR3/DDR3L Read Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz		Unit
			Min	Max	

T12	Read Data valid width	t_{Data}	200	-	ps
T13	SDQS rising edge to SCK rising edge	t_{DQSCK}	-225	225	ps

T12 and T13 are in reference to V_{ref} level.

2.5.1.2. **LPDDR3 Parameters**

Figure 2-12 shows the LPDDR3 command and address timing diagram. The timing parameters for this diagram shows in Table 2-21.

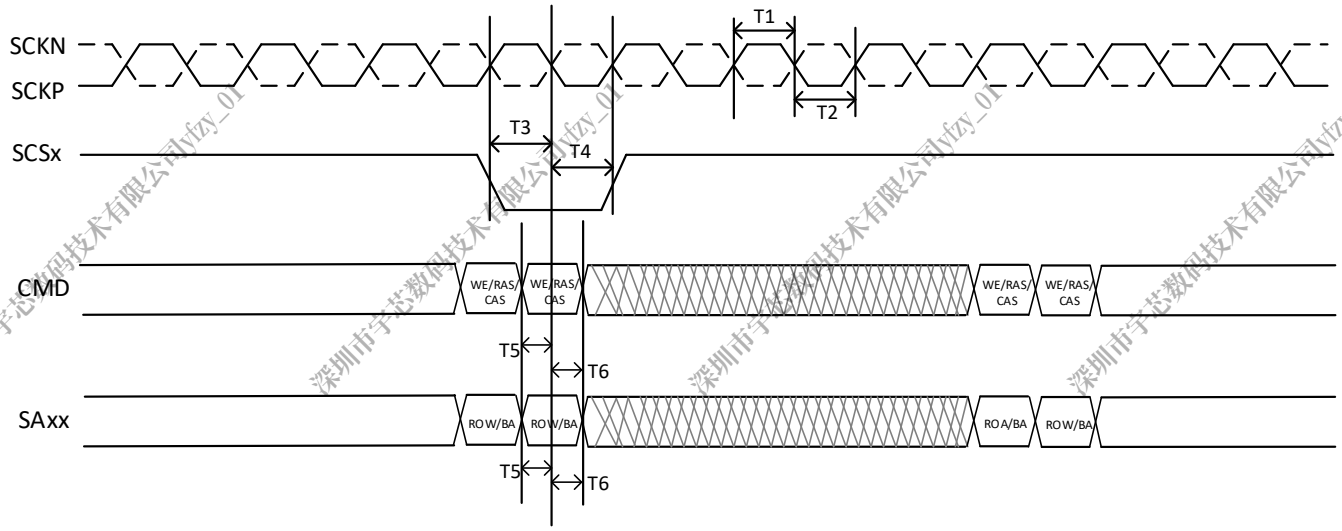


Figure 2-12. LPDDR3 Command and Address Timing Diagram

Table 2-22. LPDDR3 Command and Address Timing Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T1	Clock high pulse width	t_{CH}	0.45	-	0.55	t_{CK}
T2	Clock low pulse width	t_{CL}	0.45	-	0.55	t_{CK}
T3	SCSx input setup time	t_{ISCS}	195	347.5	-	ps
T4	SCSx input hold time	t_{IHCS}	220	372.5	-	ps
T5	Address and control input setup time	t_{IAS}	75	152.5	-	ps
T6	Address and control input hold time	t_{IAH}	100	177.5	-	ps

T1 and T2 are in reference to V_{ref} level.

T3,T4,T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 2-13 shows the LPDDR3 write timing diagram. The timing parameters for this diagram shows in Table 2-22.

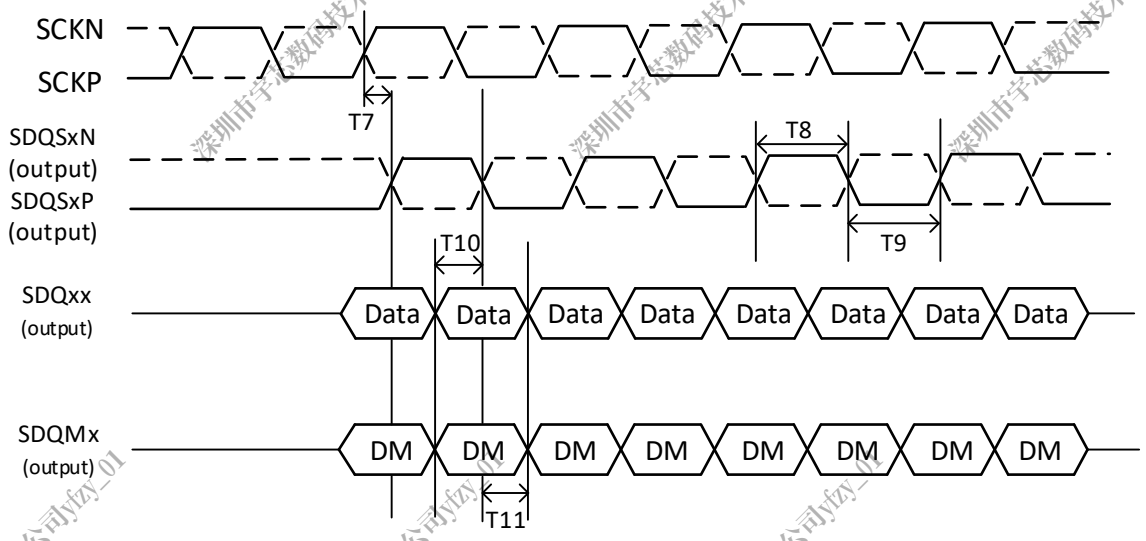


Figure 2-13. LPDDR3 Write Cycle

Table 2-23. LPDDR3 Write Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T7	SDQS rising edge to SCK rising edge	t_{DQSS}	0.75	-	1.25	t_{CK}
T8	SDQS input high-level width	t_{DQSH}	0.4	-	-	t_{CK}
T9	SDQS input low-level width	t_{DQSL}	0.4	-	-	t_{CK}
T10	SDQxx and SDQMx input setup time	t_{DS}	75	152.5	-	ps
T11	SDQxx and SDQMx input hold time	t_{DH}	100	177.5	-	ps

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.

T7,T8, and T9 are in reference to V_{ref} level.

T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 2-14 shows the LPDDR3 read timing diagram. The timing parameters for this diagram shows in Table 2-23.

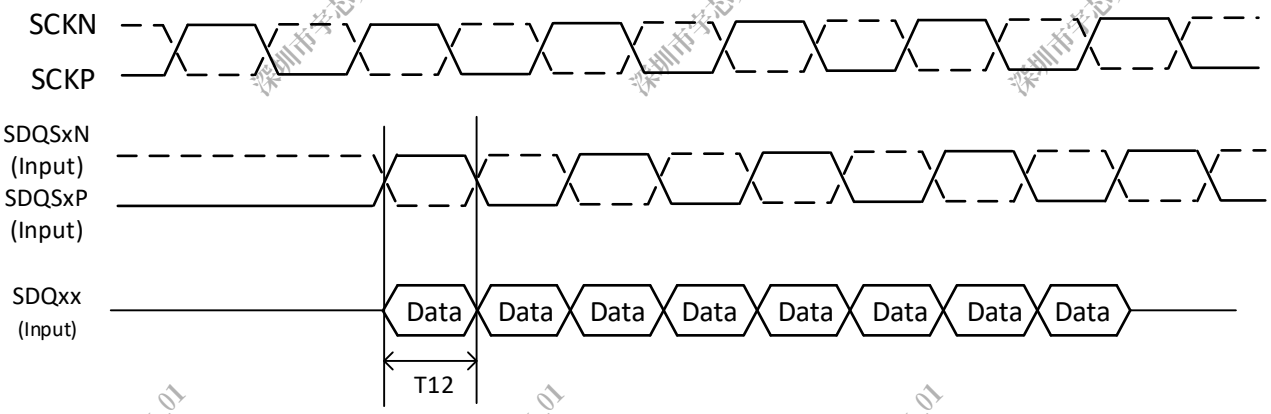


Figure 2-14. LPDDR3 Read Cycle

Table 2-24. LPDDR3 Read Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz		Unit
			Min	Max	

T12	Read Data valid width	t_{DATA}	200	-	ps

T12 is in reference to V_{ref} level.

2.5.1.3. **DDR4 Parameters**

Figure 2-15 shows the DDR4 command and address timing diagram. The timing parameters for this diagram shows in Table 2-24.

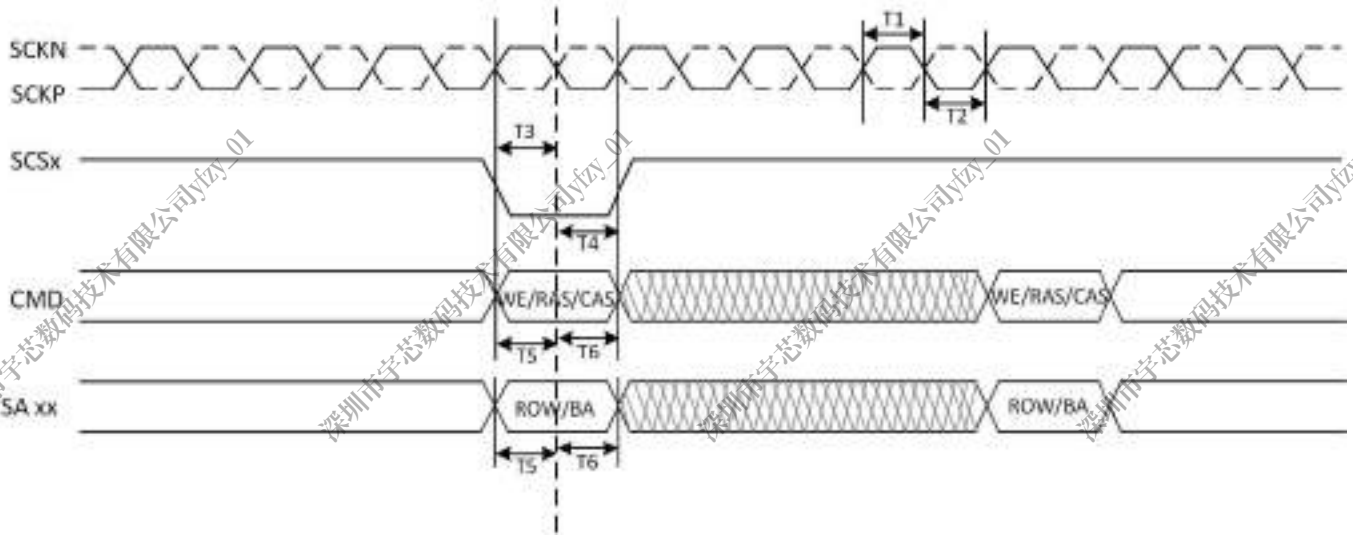


Figure 2-15. DDR4 Comman and Address Timing

Table 2-25. DDR4 Timing Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T1	Clock high-level width	t_{CH}	0.48	-	0.52	tck
T2	Clock low-level width	t_{CL}	0.48	-	0.52	tck
T3	CS setup time	t_{IS}	115	-	-	ps
T4	CS hold time	t_{IH}	140	-	-	ps
T5	Command and Address setup time to CK	t_{IS}	115	-	-	ps
T6	Command and Address hold time to CK	t_{IH}	140	-	-	ps

T1~T2 are in reference to Vref level.

T3/T5 are in reference to Vih(ac) / Vil(ac) levels.(AC100)

T4/T6 are in reference to Vih(ac) / Vil(ac) levels.(DC75)

Figure 2-16 shows the DDR4 write timing diagram. The timing parameter for this diagram shows in Table 2-25.

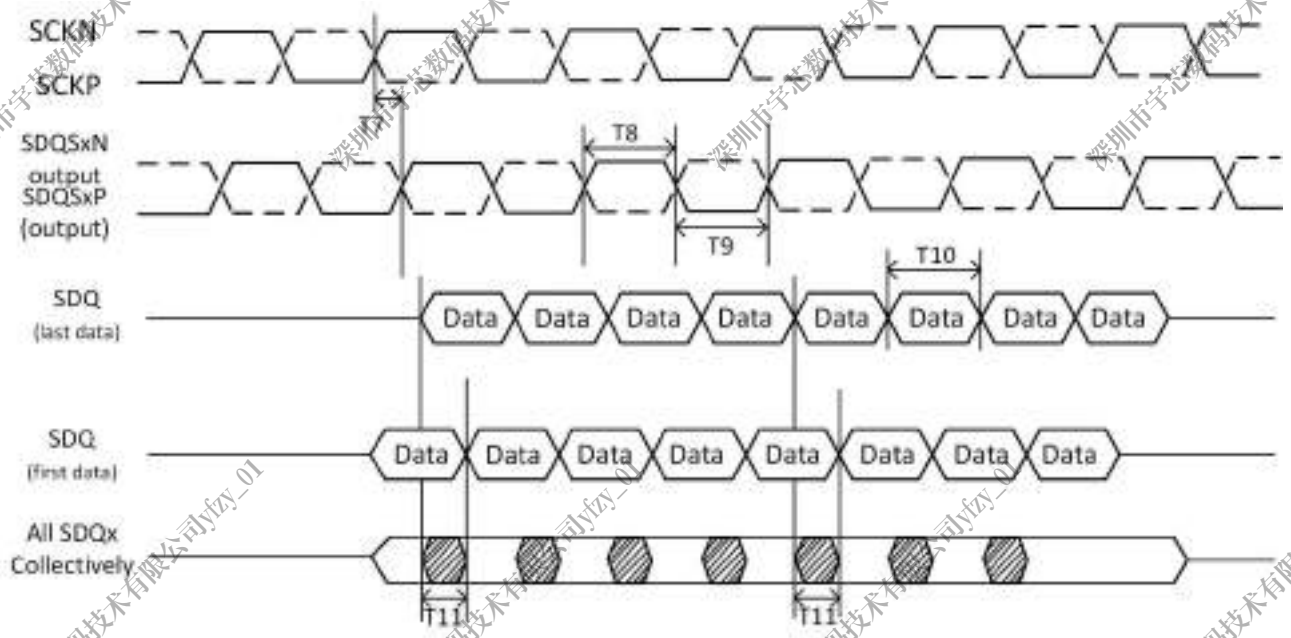


Figure 2-16. DDR4 Write Cycle

Table 2-26. DDR4 Write Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T7	SDQS rising edge to SCK rising edge	t_{DQSS}	-0.27	-	0.27	t_{CK}
T8	SDQS high level width	t_{DQSH}	0.46	-	0.54	t_{CK}
T9	SDQS low level width	t_{DQSL}	0.46	-	0.54	t_{CK}
T10	Data Valid Window per pin per UI	t_{DVWp}	0.66	-	-	t_{ui}
T11	Data Valid Window per device per UI	t_{DVWd}	0.63	-	-	t_{ui}

T7~T9 are in reference to Vref level.

T10 is Data Valid Window per pin per UI and is derived from (t_{QH} - t_{DQSQ}) of each UI on a pin of a given DRAM.

T11 is the Data Valid Window per device per UI and is derived from (t_{QH} - t_{DQSQ}) of each UI on a given DRAM

Figure 2-17 shows the DDR4 read timing diagram. The timing parameters for this diagram shows in Table 2-26.

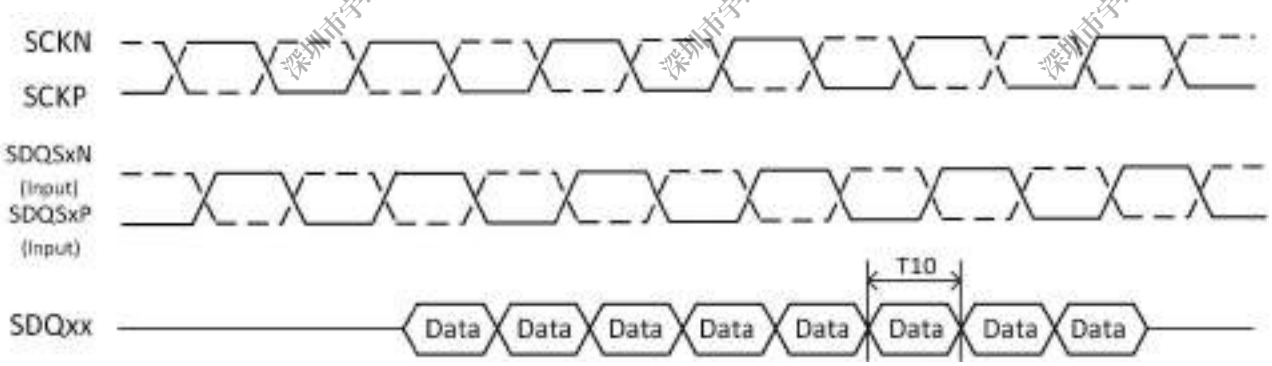


Figure 2-17. DDR4 Read Cycle

Table 2-27. DDR4 Read Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz		Unit
			Min	Max	
T10	Data Valid Window per pin per UI	t_{DVWp}	0.66	-	t_{ui}

T10 is in reference to Vref level.

2.5.1.4. LPDDR4 Parameters

Figure 2-18 shows the LPDDR4 command and address timing diagram. The timing parameters for this diagram shows in Table 2-27.

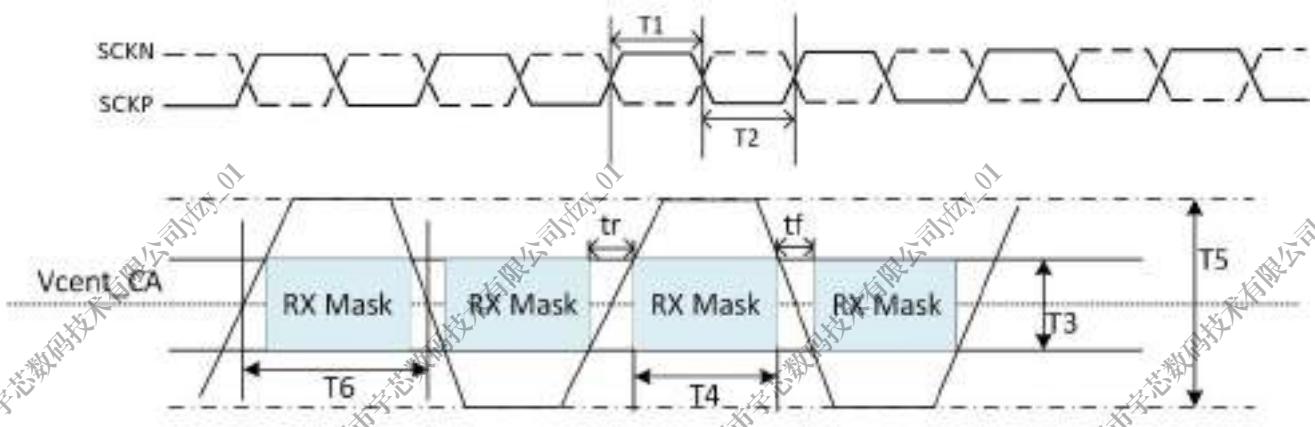


Figure 2-18. LPDDR4 Command and Address Timing Diagram

NOTE

T7 = T3/(tr or tf), signal must be monotonic within tr and tf range.

Table 2-28. LPDDR4 Command and Address Timing Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T1	Clock high pulse width	t_{CH}	0.46	-	0.54	t_{CK}
T2	Clock low pulse width	t_{CL}	0.46	-	0.54	t_{CK}
T3	Rx Mask voltage - p-p	V_{cIVW}	-	-	175	mV
T4	Rx timing window	T_{cIVW}	-	-	0.3	UI
T5	CA AC input pulse amplitude pk-pk	V_{IHL_AC}	210	-	-	mV
T6	CA input pulse width	T_{cIPW}	0.55	-	-	UI
T7	Input Slew Rate over VcIVW	SR_{IN_cIVW}	1	TBD	7	V/ns

Figure 2-19 shows the LPDDR4 write timing diagram. The timing parameters for this diagram shows in Table 2-28.

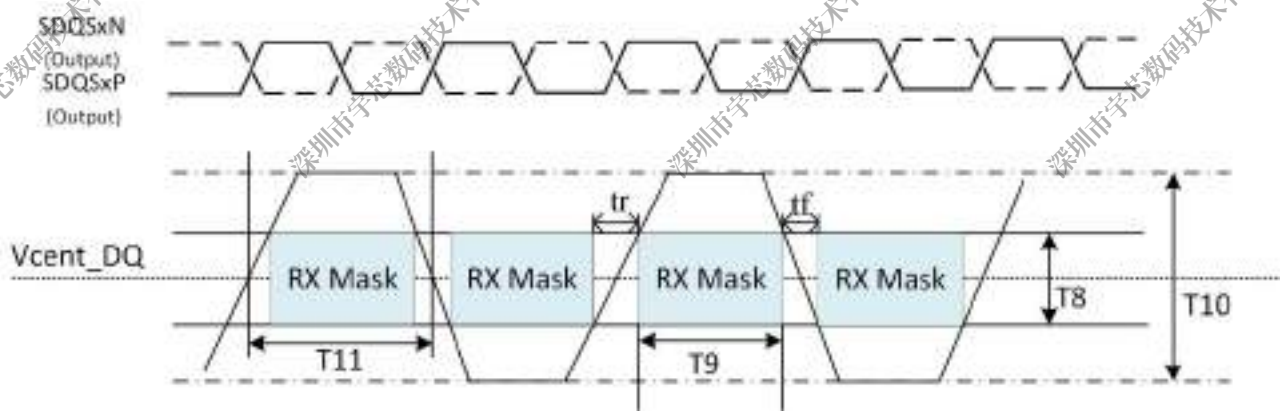


Figure 2-19. LPDDR4 Write Cycle

NOTE

T12 = T8/(tr or tf), signal must be monotonic within tr and tf range.

Table 2-29. LPDDR4 Write Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T8	Rx Mask voltage - p-p total	V_{dIVW_total}		-	140	mV
T9	Rx timing window total (At VdIVW voltage levels)	T_{dIVW_total}		-	0.22	UI
T10	DQ AC input pulse amplitude pk-pk	V_{IHL_AC}	180	-		mV
T11	Input pulse width (At Vcent_DQ)	$T_{dIPW\ DQ}$	0.45	-		UI
T12	Input Slew Rate over VdIVW_total	SR_{IN_dIVW}	1	TBD	7	V/ns

Figure 2-20 shows the LPDDR4 read timing diagram. The timing parameters for this diagram shows in Table 2-29.

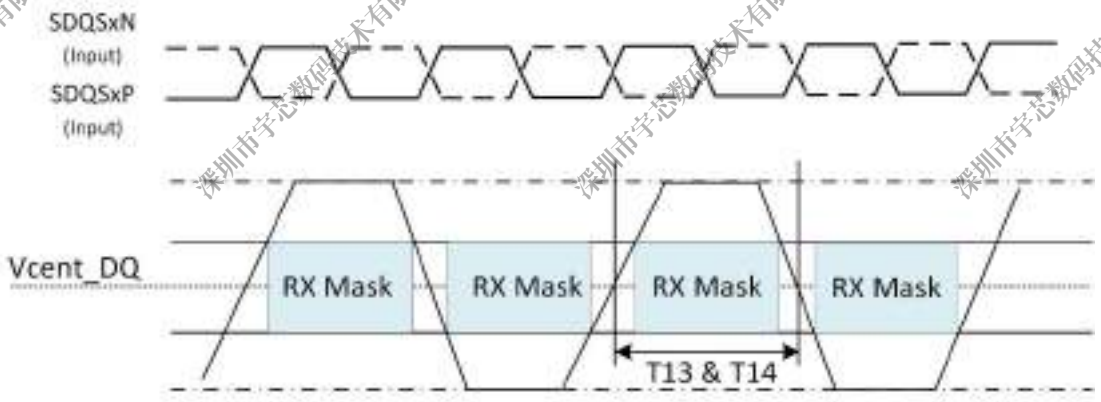


Figure 2-20. LPDDR4 Read Cycle

Table 2-30. LPDDR4 Read Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz		Unit
			Min	Max	
T13	DQ output window time total, per pin (DBI-Disabled)	t_{QW_total}	0.75	-	UI
T14	DQ output window time total, per pin (DBI-Enabled)	$t_{QW\_total\_DBI}$	0.75	-	UI

2.5.2. Nand Interface Timing

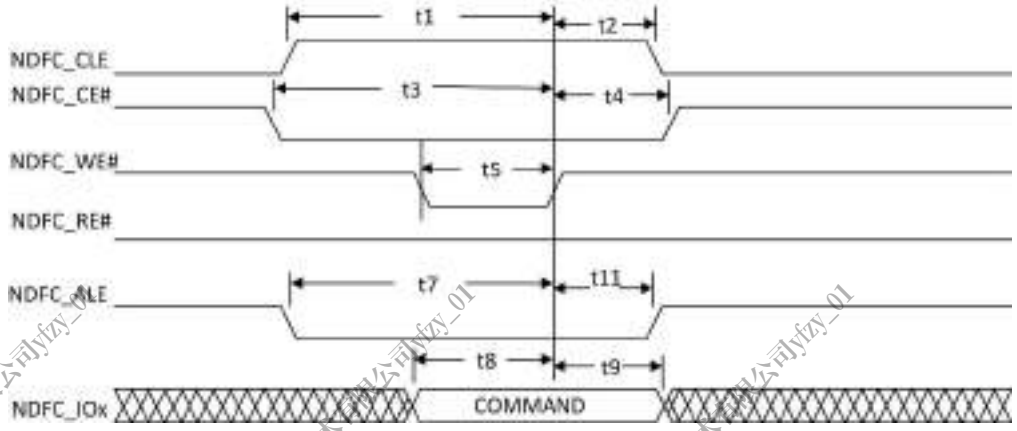


Figure 2-21. Command Cycle Timing

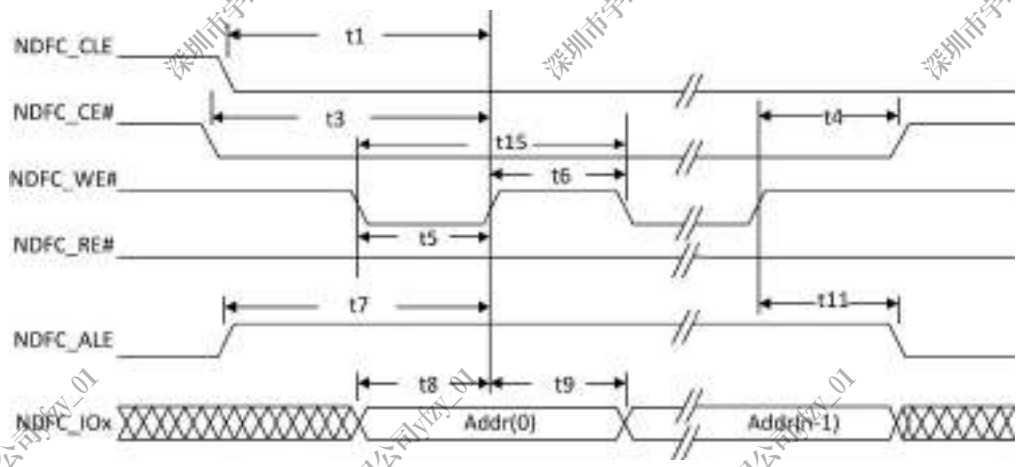


Figure 2-22. Address Cycle Timing

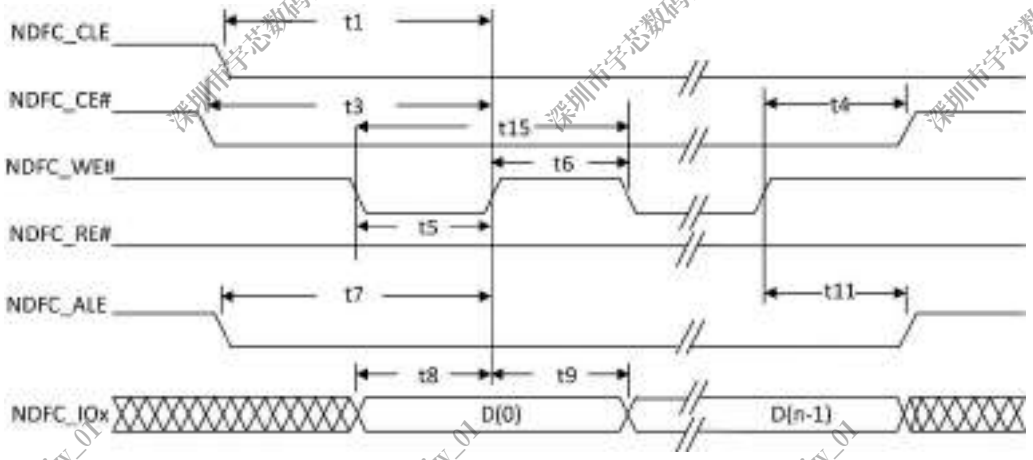


Figure 2-23. Write Data to Flash Cycle Timing

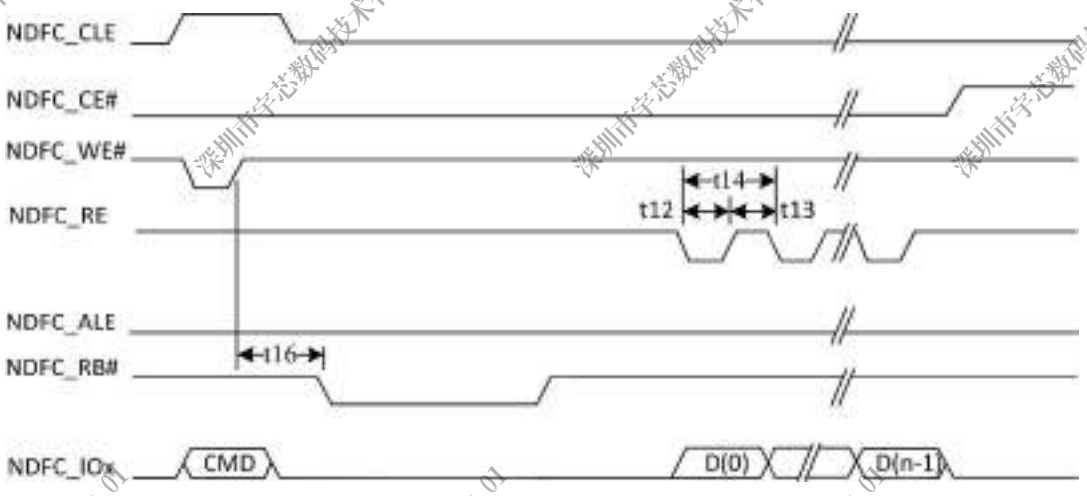


Figure 2-24. Waiting R/B# Ready Timing

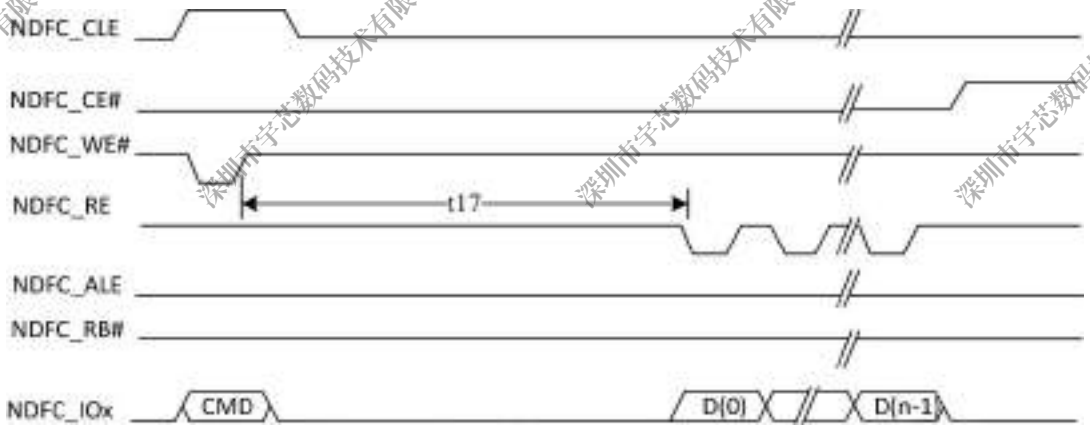


Figure 2-25. WE# High to RE# Low Timing

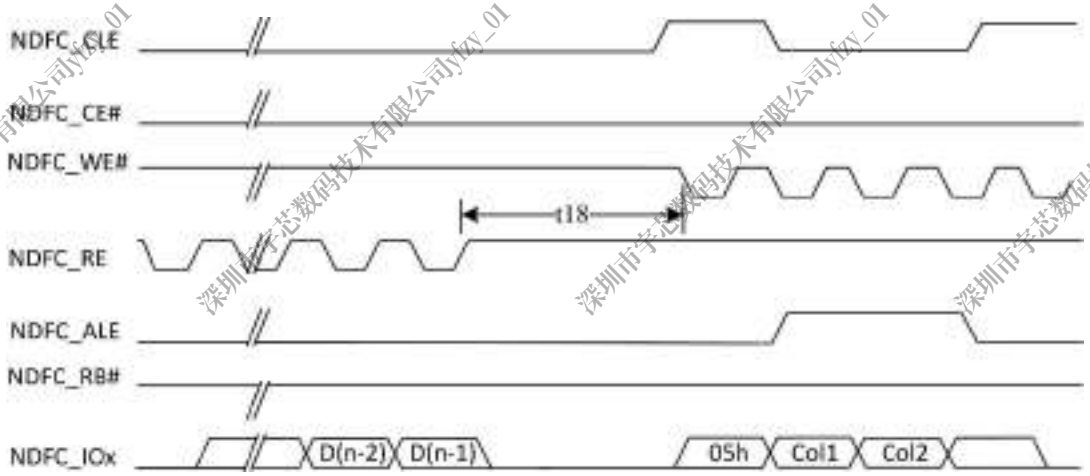


Figure 2-26. RE# High to WE# Low Timing

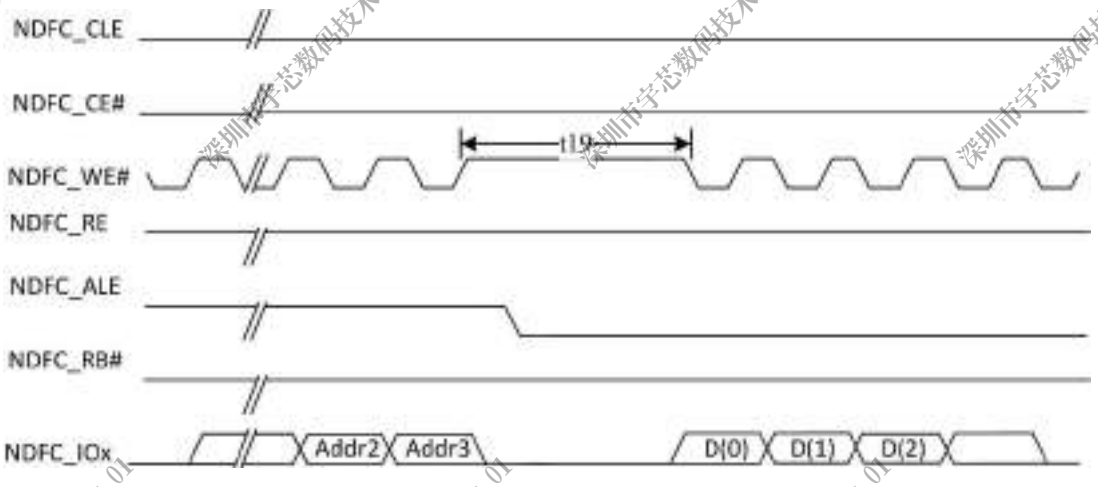


Figure 2-27. Address to Data Loading Timing

Table 2-31. Nand Timing Parameters

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T(1)	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns
NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB(2)	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR(3)	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW(4)	ns
Address to Data Loading time	t19	T_ADL(5)	ns
NOTE (1):T is the cycle of clock. **NOTE (2),(3),(4),(5):**This values is configurable in Nand Flash Controller. The value of T_WB could be 28T/44T/60T/76T, the value of T_WHR could be 0T/12T/28T/44T, the value of T_RHW could be 8T/24T/40T/56T, the value of T_ADL could be 0T/12T/28T/44T.			

2.5.3. SMHC Interface Timing

2.5.3.1. SMHC0/1 Interface Timing

2.5.3.1.1. SDR Mode(<100MHz)

The contents of this section can be applied to DS, HS, SDR12, SDR25, SDR50, SDR104（<100MHz） speed mode.

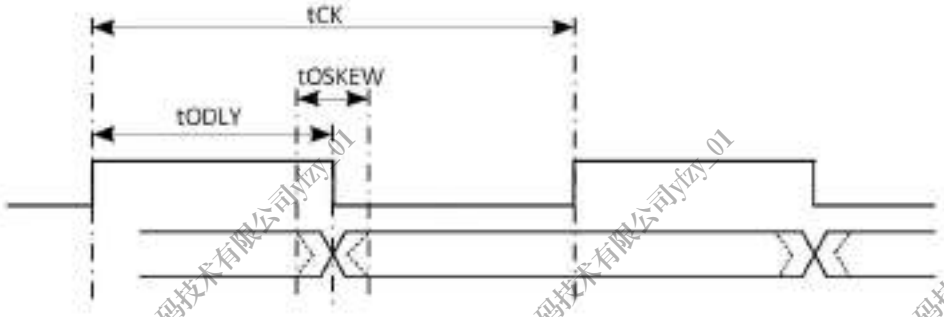


Figure 2-28. SMHC0/1 SDR Mode Output Timing Diagram

Table 2-32. SMHC0/1 SDR Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns
NOTE **Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. The GPIO's driver strength level is 2 for test.**					

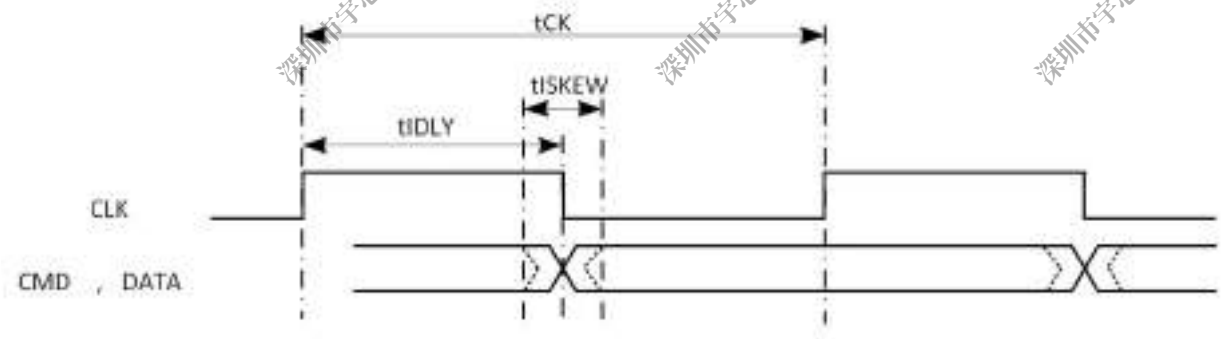


Figure 2-29. SMHC0/1 SDR Mode Input Timing Diagram

Table 2-33. SMHC0/1 SDR Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%

Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	1	ns
NOTE **The GPIO's driver strength level is 2 for test.**					

2.5.3.1.2. DDR50 Mode

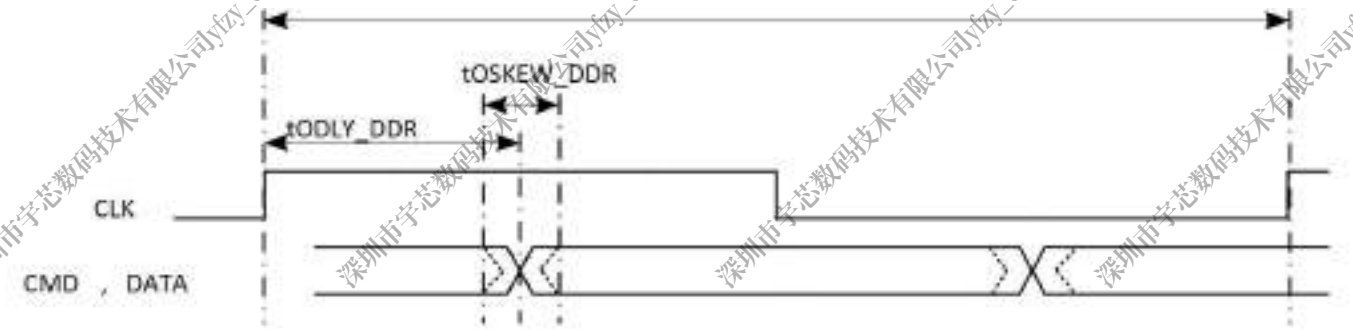


Figure 2-30. SMHC0/1 DDR50 Mode Output Timing Diagram

Table 2-34. SMHC0/1 DDR50 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY	-	0.25	0.25	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns
NOTE **Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. The GPIO's driver strength level is 2 for test.**					

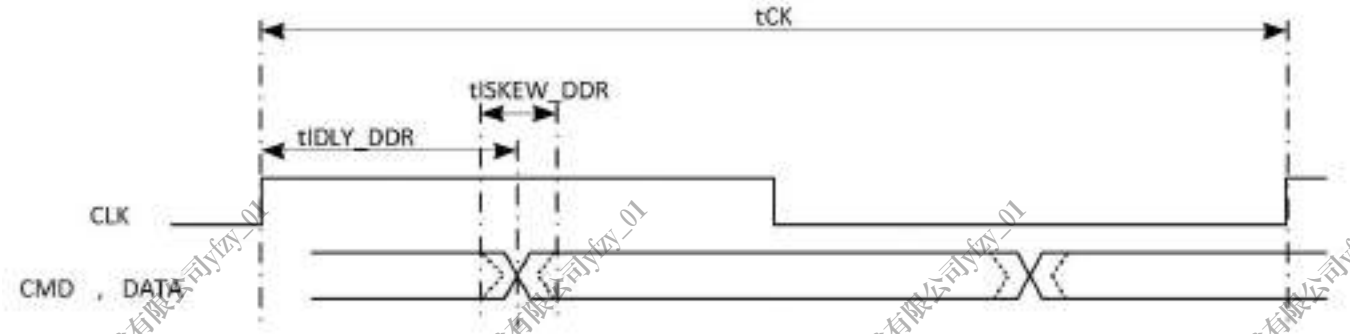


Figure 2-31. SMHC0/1 DDR50 Mode Input Timing Diagram

Table 2-35. SMHC0/1 DDR50 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	-	ns
Data input skew time in DDR mode	tISKEW_DDR	-	-	-	ns
NOTE **The GPIO's driver strength level is 2 for test.**					

2.5.3.1.3. SDR104 Mode(>100MHz)

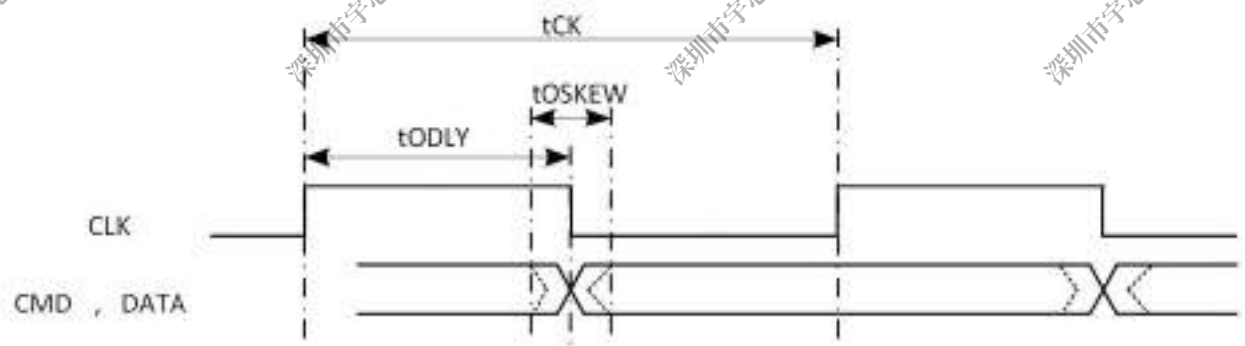


Figure 2-32. SMHC0/1 SDR104 Mode Output Timing Diagram

Table 2-36. SMHC0/1 SDR104 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	-	150	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns
NOTE **Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. The GPIO's driver strength level is 2 for test.**					

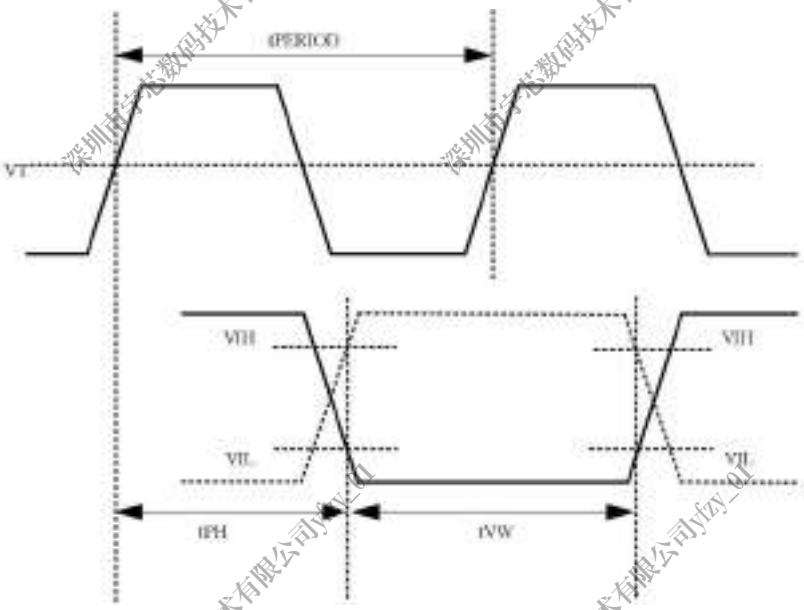


Figure 2-33. SMHC0/1 SDR-104 Mode Input Timing Diagram

Table 2-37. SMHC0/1 SDR-104 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	
NOTE(1): Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE(2)**: The GPIO's driver strength level is 3 for test. **NOTE(3)**: Temperature variation: -20°C **NOTE(4)**: Temperature variation: 90°C						

2.5.3.2. **SMHC2 Interface Timing**

2.5.3.2.1. HS-SDR/HS-DDR Mode

NOTE

IO volatage is 1.8V or 3.3V.

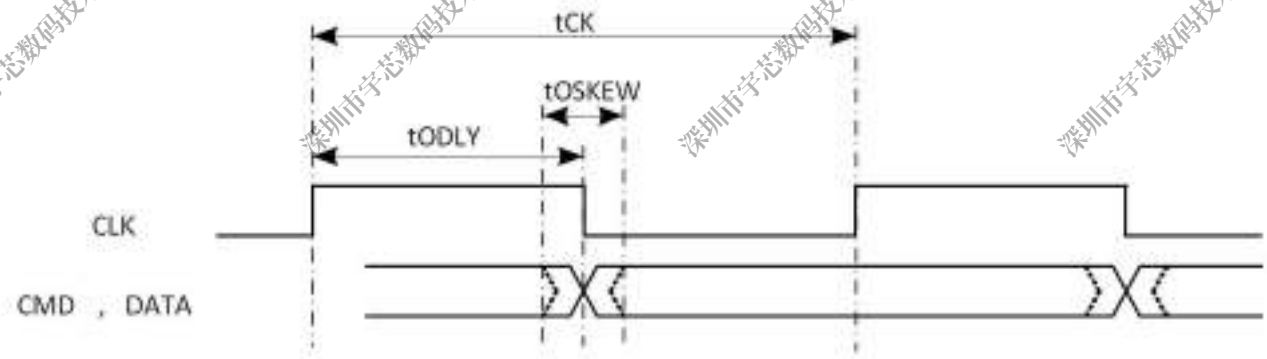


Figure 2-34. SMHC2 HS-SDR Mode Output Timing Diagram

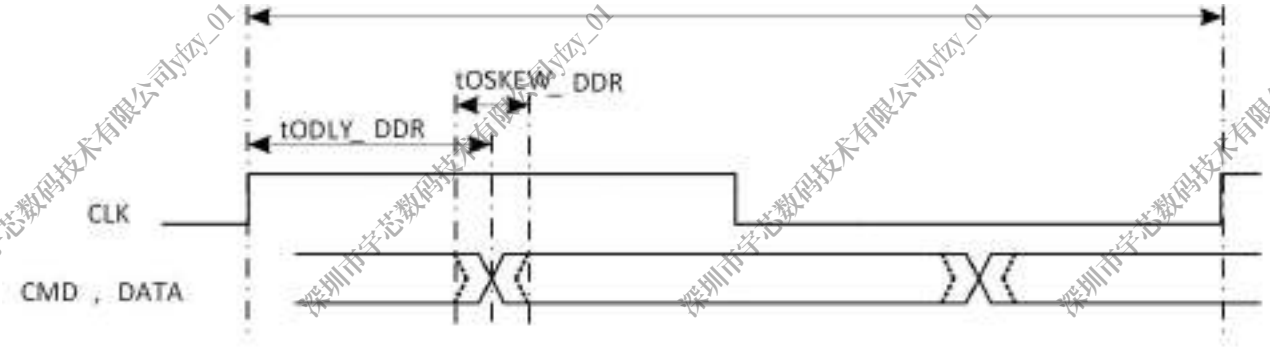


Figure 2-35. SMHC2 HS-DDR Mode Output Timing Diagram

Table 2-38. SMHC2 HS-SDR/HS-DDR Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI	
Data output delay skew time	tOSKEW	-	-		ns	

NOTE

Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50MHz.

The GPIO's driver strength level is 2 for test.

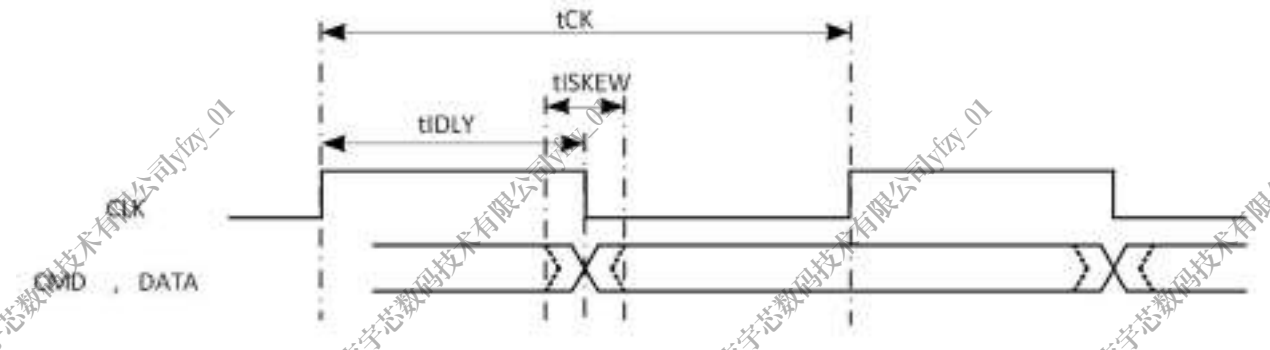


Figure 2-36. SMHC2 HS-SDR Mode Input Timing Diagram

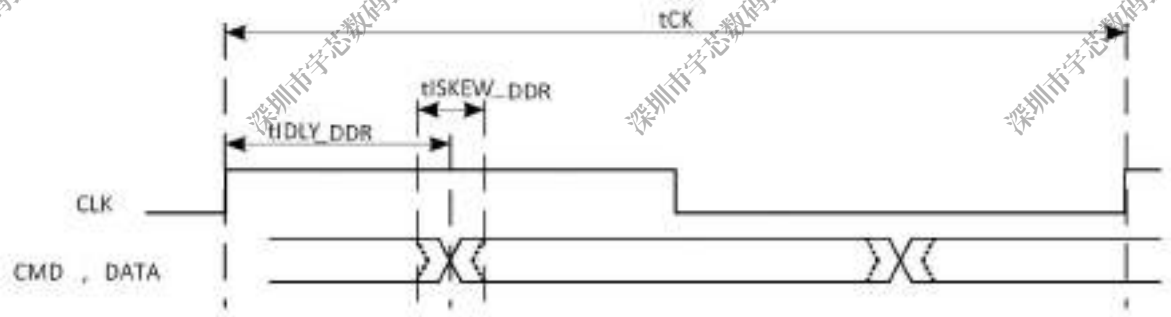


Figure 2-37. SMHC2 HS-DDR Mode Input Timing Diagram

Table 2-39. SMHC2 HS-SDR/HS-DDR Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-		ns	
Data input delay in DDR mode.It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-		ns	
Data input skew time in SDR mode	tISKEW	-	-		ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-		ns	
NOTE **The GPIO's driver strength level is 2 for test.**						

2.5.3.2.2. HS200 Mode

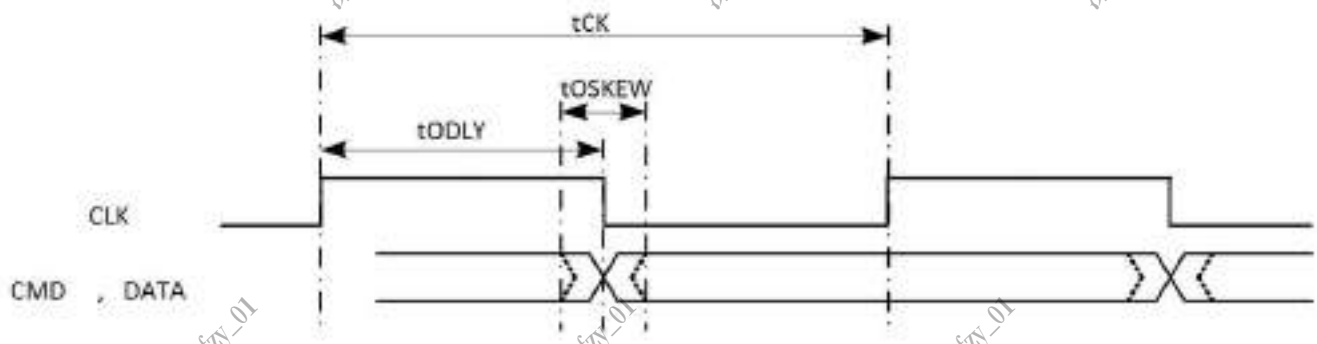


Figure 2-38. SMHC2 HS200 Mode Output Timing Diagram

Table 2-40. SMHC2 HS200 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						

Clock frequency	tCK	-	-	150	MHz	
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-		ns	

NOTE

Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.

The GPIO's driver strength level is 3 for test.

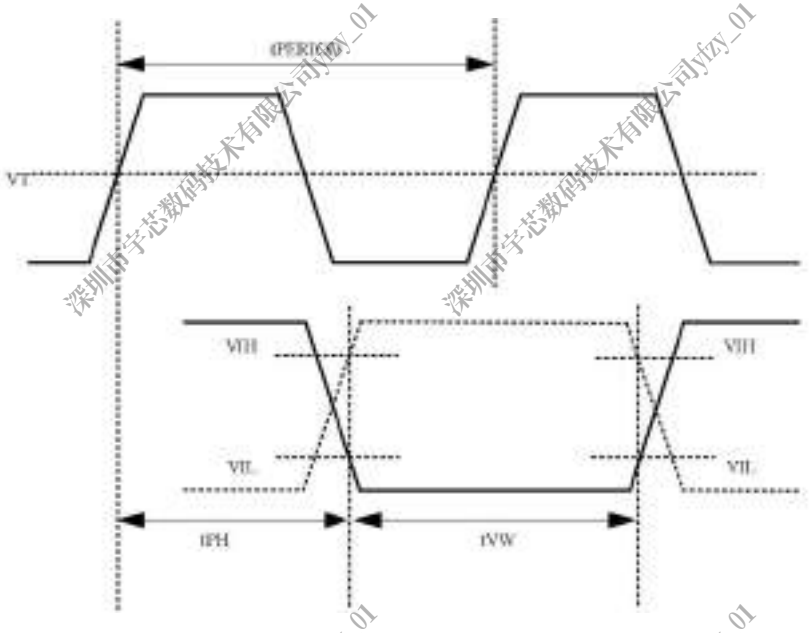


Figure 2-39. SMHC2 HS200 Mode Input Timing Diagram

Table 2-41. SMHC2 HS200 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	

NOTE (1): Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.

NOTE (2): The GPIO's driver strength level is 3 for test.

NOTE (3): Temperature variation: -20°C.

NOTE (4): Temperature variation: 90°C.

2.5.3.2.3. HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

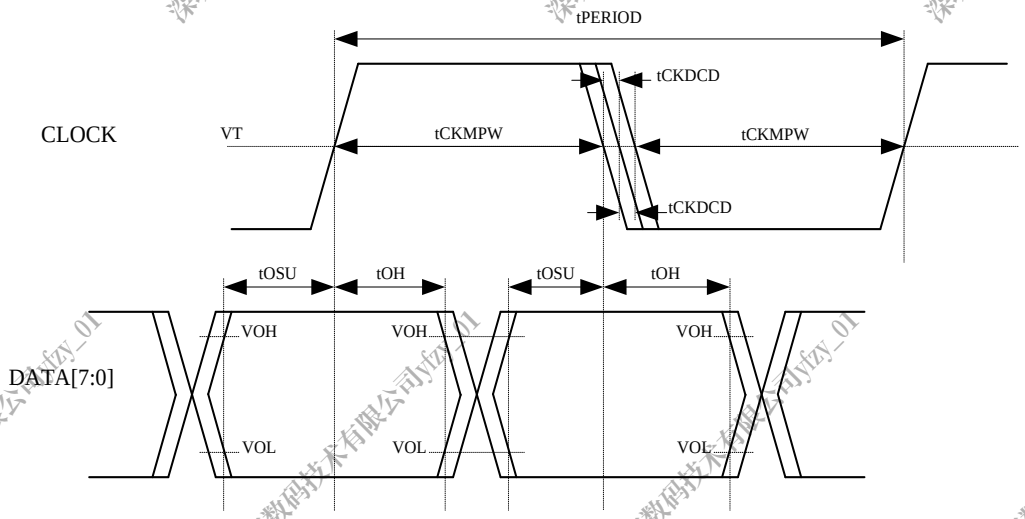


Figure 2-40. SMHC2 HS400 Mode Data Output Timing Diagram

Table 2-42. SMHC2 HS400 Mode Data Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	10	-	-	ns	Max:100MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA(referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	ns	

NOTE

Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.

The GPIO's driver strength level is 3 for test.

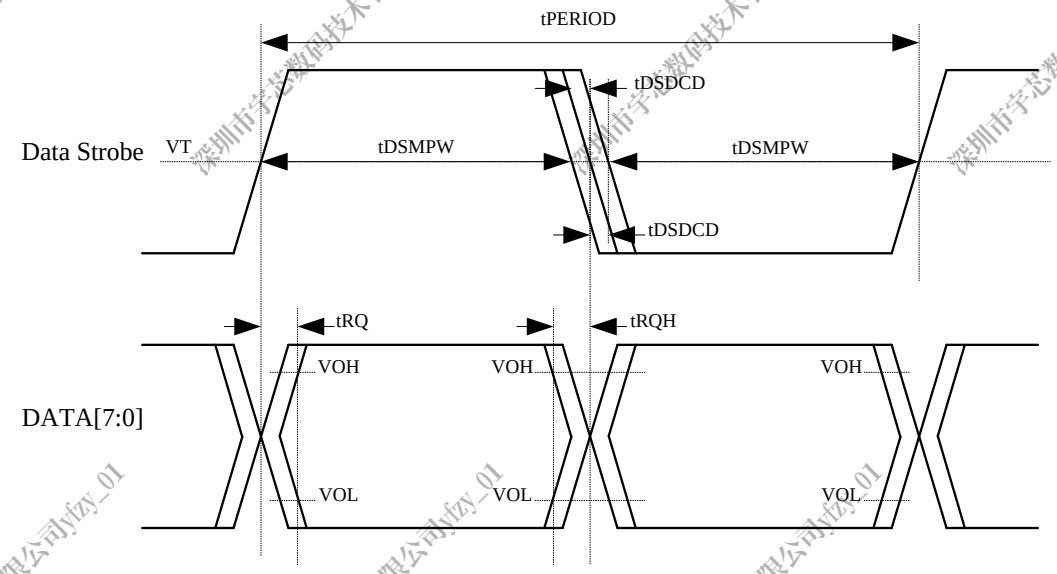


Figure 2-41. SMHC2 HS400 Mode Data Input Timing Diagram

Table 2-43. SMHC2 HS400 Mode Data Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS(Data Strobe)						
DS period	tPERIOD	10	-	-	ns	Max:100MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Output DATA(referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	

NOTE

Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.

The GPIO's driver strength level is 3 for test.

2.5.4. LCD Interface Timing

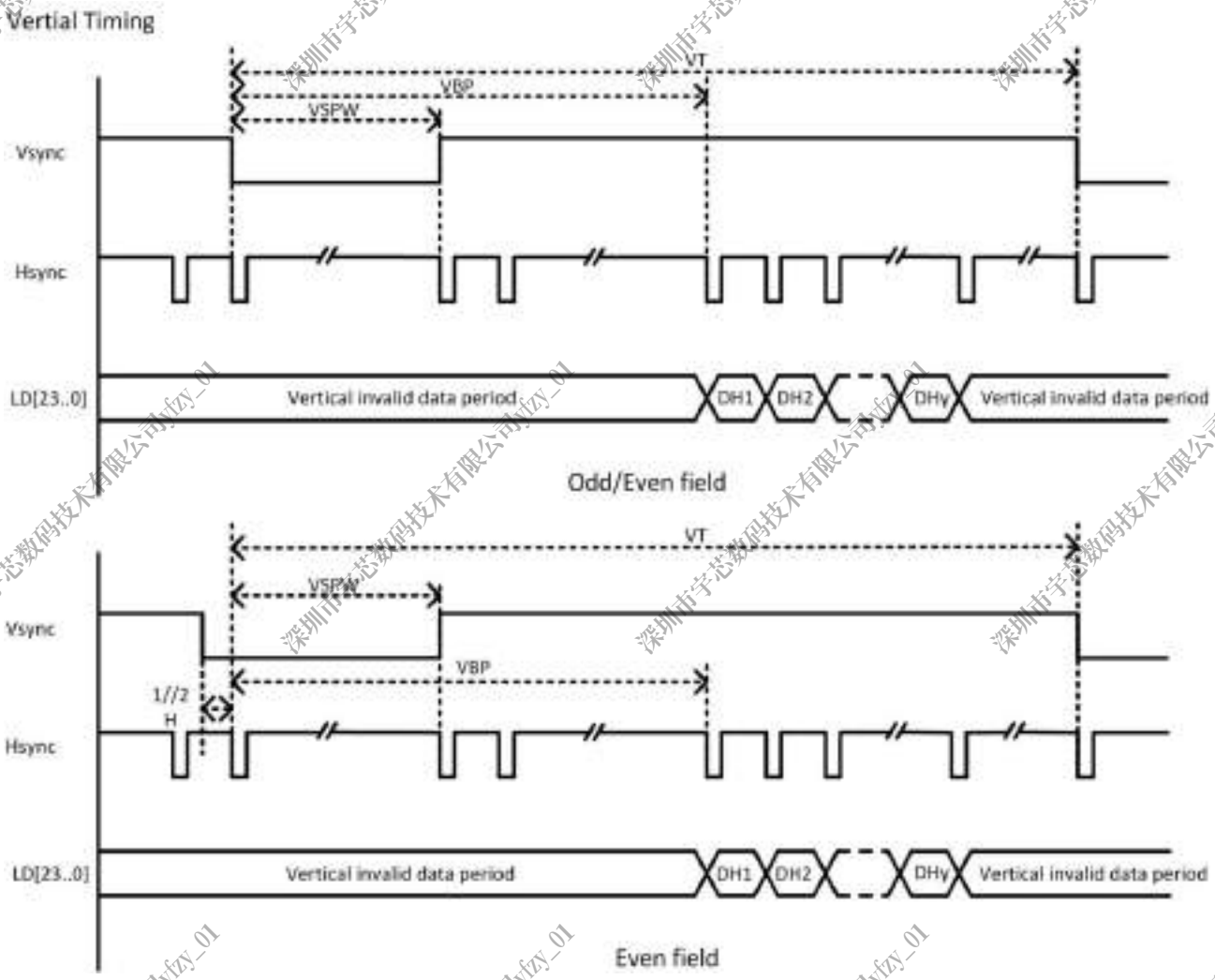


Figure 2-42. HV_IF Interface Vertical Timing

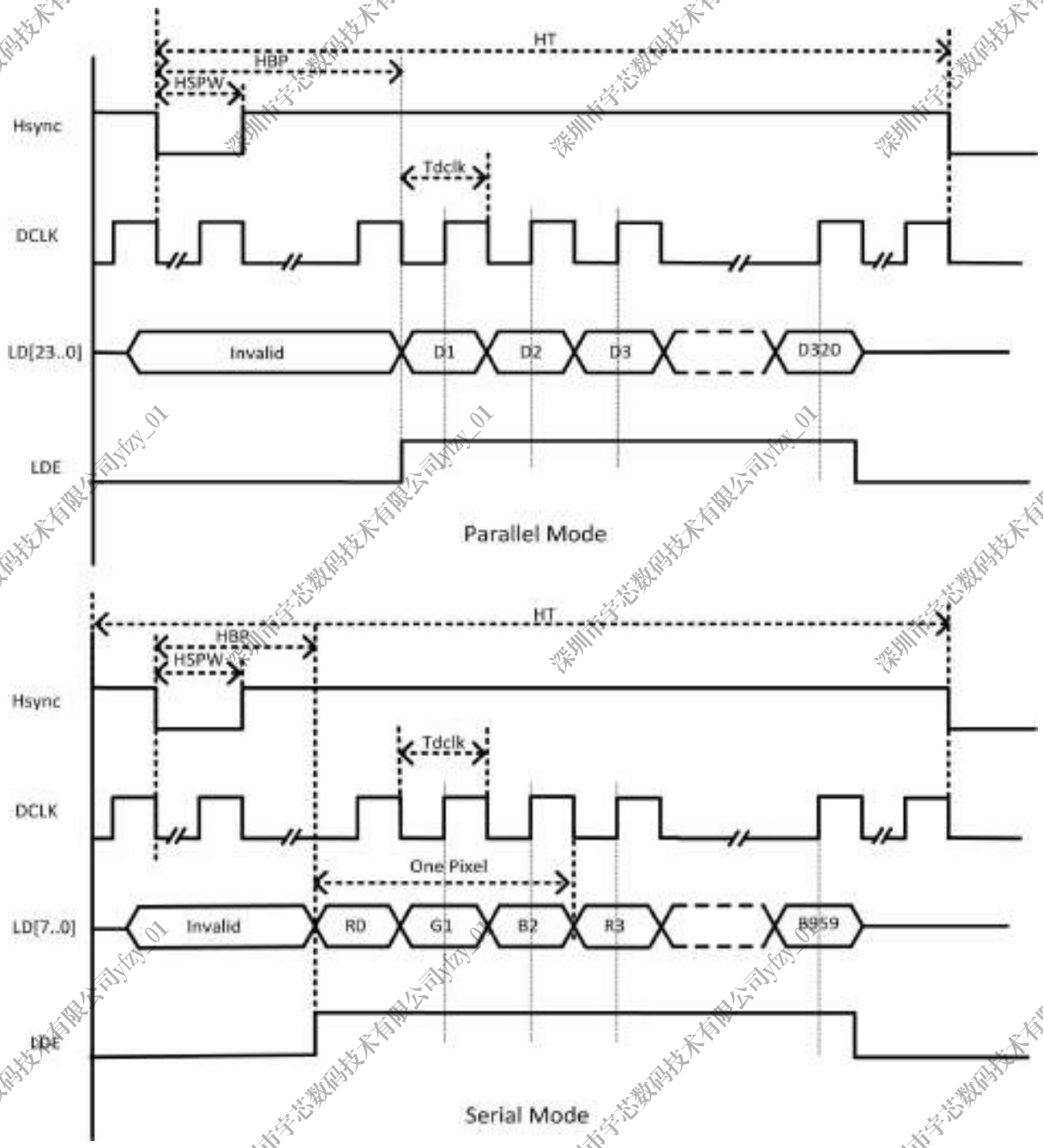


Figure 2-43. HV Interface Horizontal Timing

Table 2-44. HV Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK
HSYNC width	tHSPW	-	HSPW+1	-	tDCLK
HSYNC back porch	tHBP	-	HBP+1	-	tDCLK
VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT

NOTE

Vsync: Vertical sync, indicates one new frame

Hsync: Horizontal sync, indicates one new scan line
DCLK: Dot clock, pixel data are sync by this clock
LDE: LCD data enable
LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel

2.5.5. CSI Interface Timing

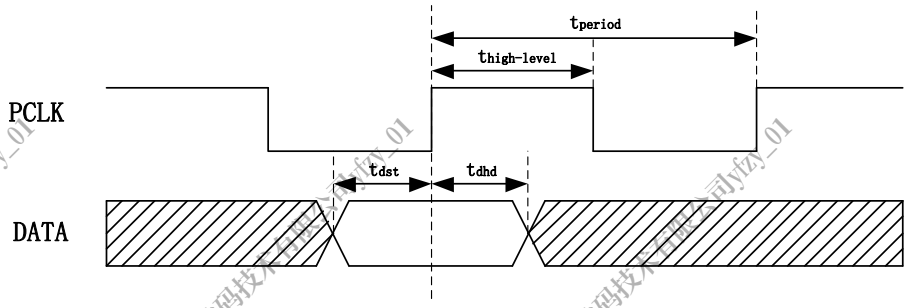


Figure 2-44. CSI Interface Timing

Table 2-45. CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.7	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk duty	$t_{high\text{-}level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

2.5.6. EMAC Interface Timing

2.5.6.1. RGMII

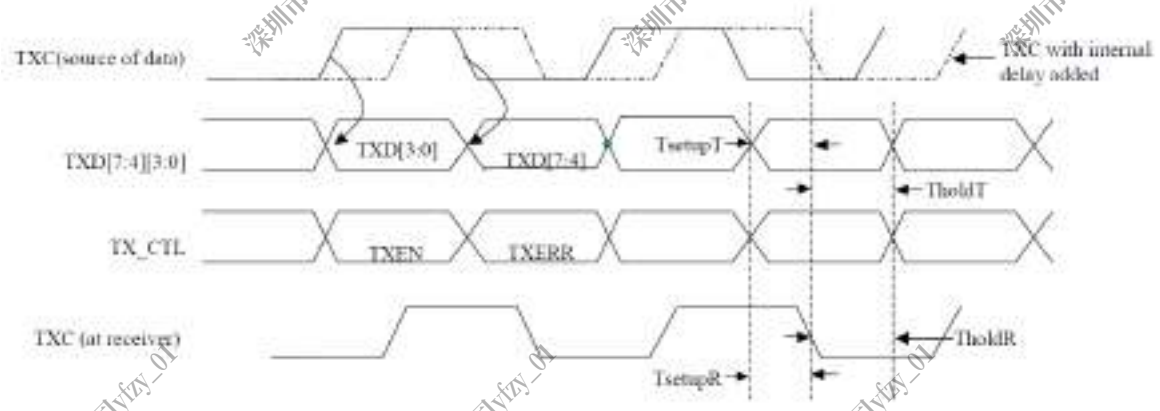


Figure 2-45. RGMII Transmit Timing

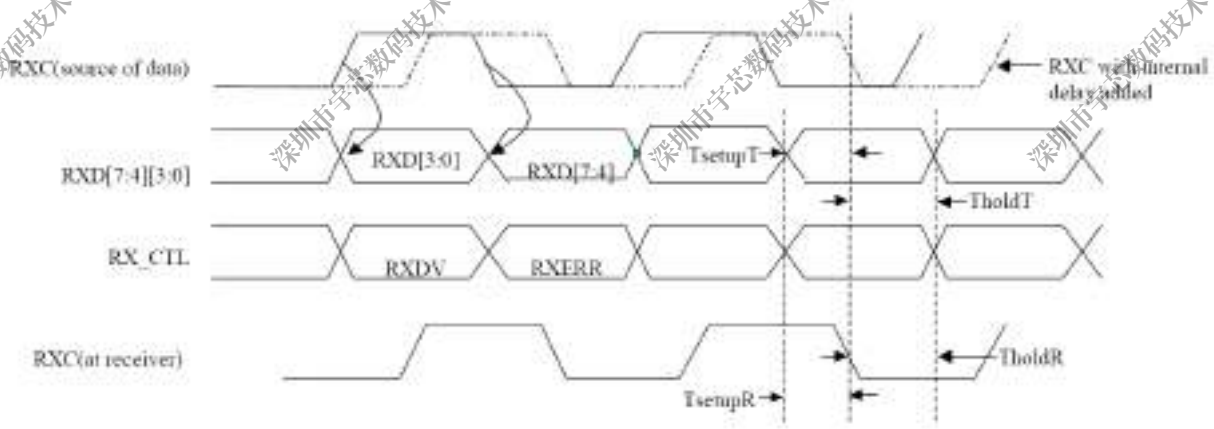


Figure 2-46. RGMII Receive Timing

Table 2-46. RGMII Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
Tcyc	Clock Cycle Duration *note1	7.2	8	8.8	ns
Duty_G	Duty Cycle Duration for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
TsetupT	Data to clock output setup(at Transmitter integrated delay)	1.2	2.0		ns
TholdT	Data to clock output hold(at Transmitter integrated delay)	1.2	2.0		ns
TsetupR	Data to clock input setup(at Receiver integrated delay)	1.0	2.0		ns
TholdR	Data to clock input hold(at Receiver integrated delay)	1.0	2.0		ns

NOTE

For 10Mbps and 100Mbps， Tcyc will scale 400ns±40ns and 40ns±4ns.

2.5.6.2. **RMII**

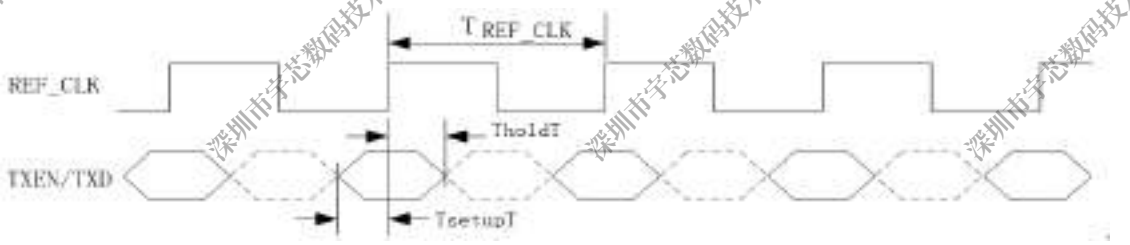


Figure 2-47. RMII Transmit Timing

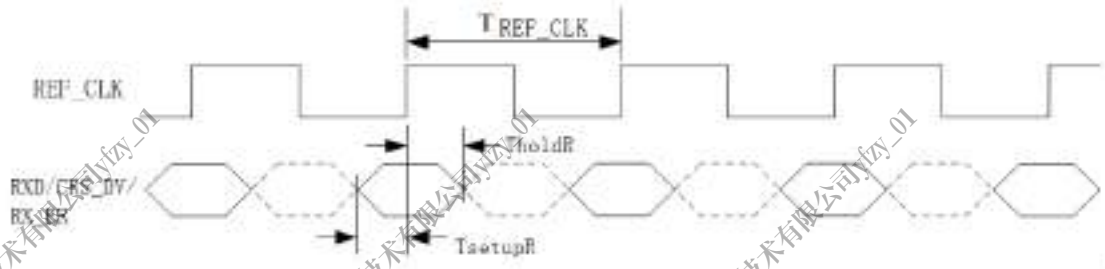


Figure 2-48. RMII Receive Timing

Table 2-47. RMII Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
T_{REF_CLK}	Reference Clock Period	-	20	-	ns
Tduty	REF_CLK duty cycle	35		65	%
TsetupT	TXD/TXEN to REF_CLK setup time	4			ns
TholdT	TXD/TXEN to REF_CLK hold time	2			ns
TsetupR	RXD/CRS_DV/RX_ER to REF_CLK setup time	4			ns
TholdR	RXD/CRS_DV/RX_ER to REF_CLK hold time	2			ns

2.5.7. I2S/PCM Interface Timing

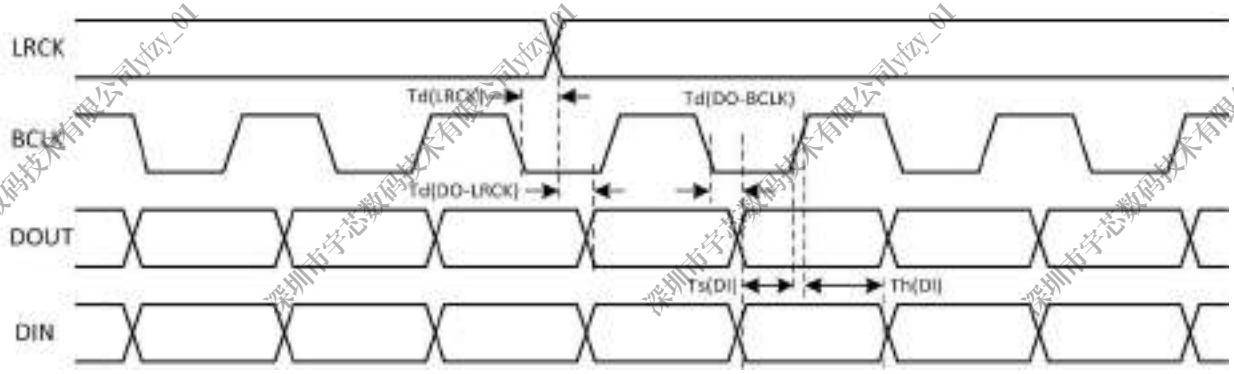


Figure 2-49. I2S/PCM in Master Mode Timing

Table 2-48. I2S/PCM in Master Mode Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT Delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT Delay	T_d(DO-BCLK)	-	-	10	ns
DIN Setup	T_s(DI)	4	-	-	ns
DIN Hold	T_h(DI)	4	-	-	ns
BCLK Rise Time	T_r	-	-	8	ns
BCLK Fall Time	T_f	-	-	8	ns

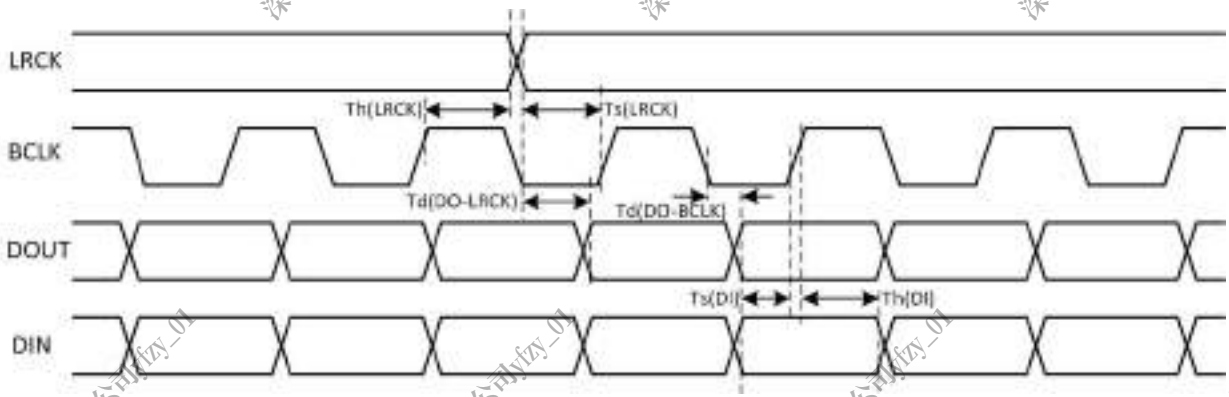


Figure 2-50. I2S/PCM in Slave Mode Timing

Table 2-49. I2S/PCM in Slave Mode Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit

LRCK Setup	T_s(LRCK)	4	-	-	ns
LRCK Hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT Delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT Delay	T_d(DO-BCLK)	-	-	10	ns
DIN Setup	T_s(DI)	4	-	-	ns
DIN Hold	T_h(DI)	4	-	-	ns
BCLK Rise Time	T_r	-	-	4	ns
BCLK Fall Time	T_f	-	-	4	ns

2.5.8. DMIC Interface Timing

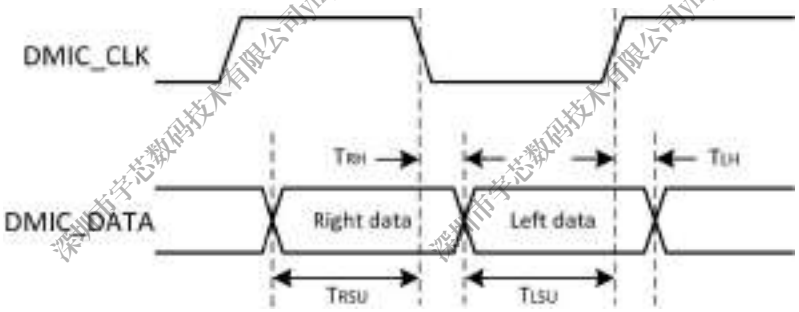


Figure 2-51. DMIC Interface Timing

Table 2-50. DMIC Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) setup time to falling edge of DMIC_CLK	T_{RSU}	15	-	-	ns
DMIC_DATA(Right) hold time from falling edge of DMIC_CLK	T_{RH}	0	-	-	ns
DMIC_DATA(Left) setup time to rising edge of DMIC_CLK	T_{LSU}	15	-	-	ns
DMIC_DATA(Left) hold time from rising edge of DMIC_CLK	T_{LH}	0	-	-	ns

2.5.9. MIPI-Rx Interface Timing

Table 2-51. MIPI Rx Interface Timing Constants

Symbol	Parameters	Min	Typ	Max	Unit
f_{MAXDF}	Maximum Data Speed	-	-	1.5G	bps
T_{CIP}	Differential Clock Period	2	(T)	-	ns
T_{DUDF}	CKxP/M Duty Cycle	0.45(T)	-	0.55(T)	ns
T_{SDF}	CKxP/M – D < 3:0 >xP/M Setup Time	0.15(T)	-	-	
T_{HDF}	CKxP/M – D < 3:0 >xP/M Hold Time	0.15(T)	-	-	
T_{RDF}	Differential Input Rise Time 20-80%	-	-	600	ps
T_{FDF}	Differential Input Fall Time 20-80%	-	-	600	
T_{SKDF}	DxP/M Channel to Channel Skew	-	-	150	

2.5.10. SPI Interface Timing

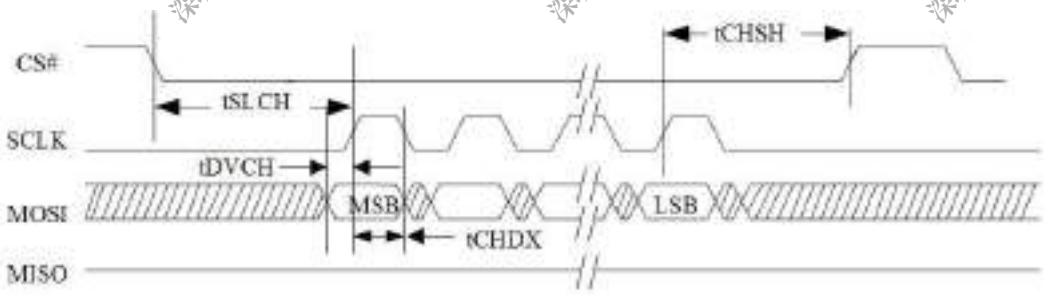


Figure 2-52. SPI MOSI Timing

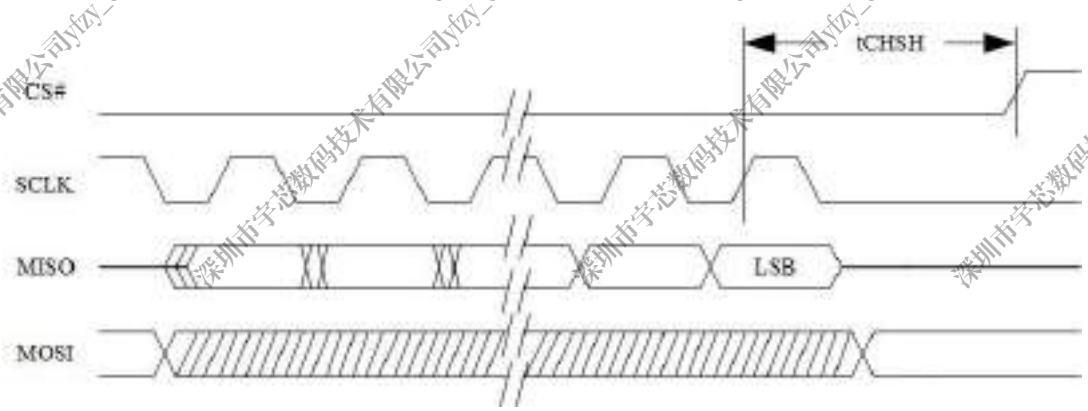


Figure 2-53. SPI MISO Timing

Table 2-52. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	tSLCH	-	2T	-	ns
CS# active hold time	tCHSH	-	2T	-	ns
Data in setup time	tDVCH	-	T/2-3	-	ns
Data in hold time	tCHDX	-	T/2-3	-	ns

NOTE

T is the cycle of clock.

2.5.11. UART Interface Timing

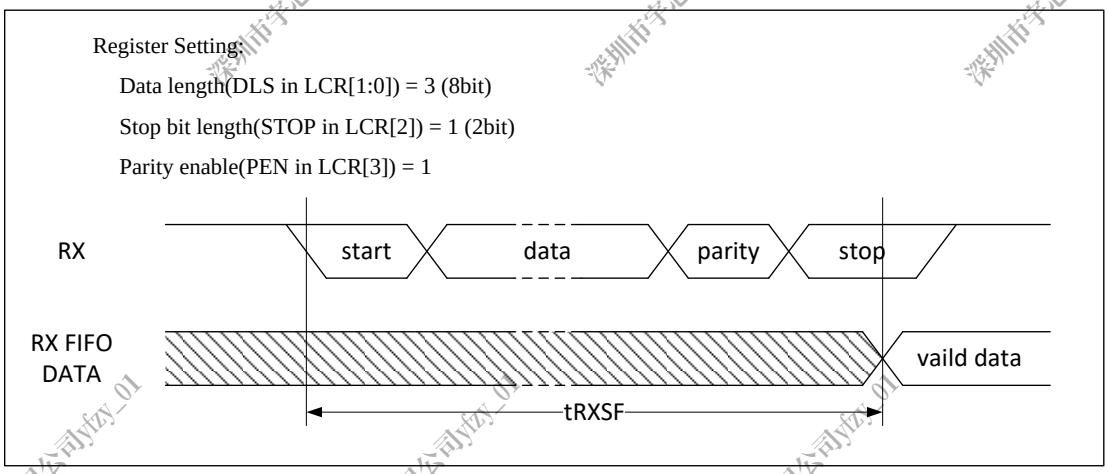


Figure 2-54. UART RX Timing

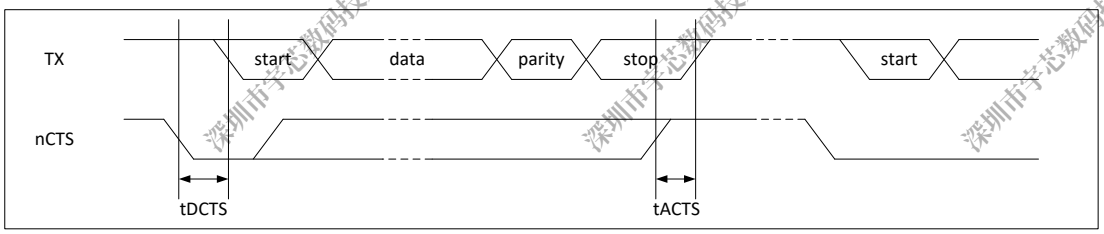


Figure 2-55. UART nCTS Timing

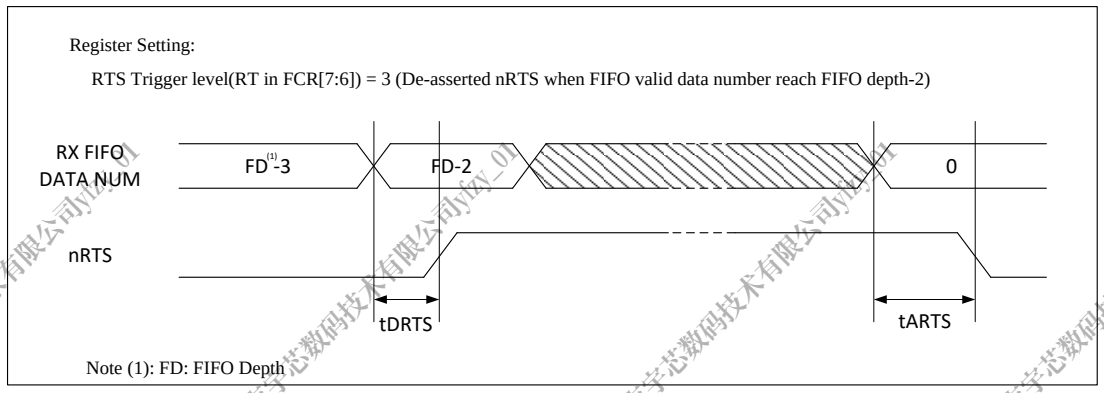


Figure 2-56. UART nRTS Timing

Table 2-53. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP	ns
Delay time of asserted nRTS	tARTS	-	-	BRP	ns

NOTE

BRP: Baud-Rate Period.

2.5.12. TWI Interface Timing

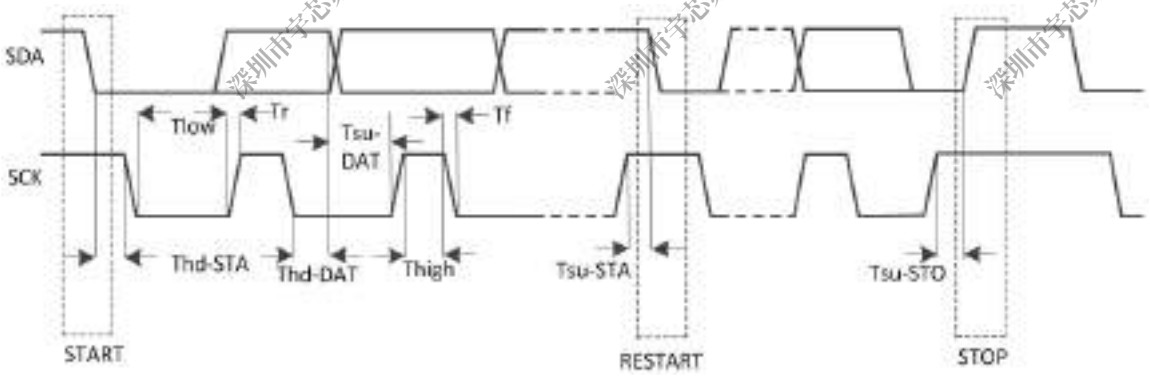


Figure 2-57. TWI Timing

Table 2-54. TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in start	Tsu-STA	4.7	-	0.6	-	us
Hold time in start	Thd-STA	4.0	-	0.6	-	us
Setup time in data	Tsu-DAT	250	-	100	-	ns
Hold time in data	Thd-DAT	5.0	-	-	-	ns
Setup time in stop	Tsu-STO	4.0	-	0.6	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	ns
SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

2.5.13. CIR Receiver Interface Timing

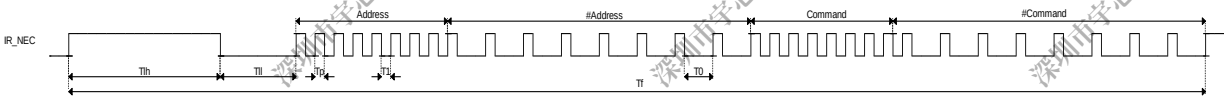


Figure 2-58. CIR Receiver Timing

Table 2-55. CIR Receiver Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Frame period	Tf	-	67.5	-	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	Tll	-	4.5	-	ms
Pulse time	Tp	-	560	-	us
Logical 1 low time	T1	-	1680	-	us
Logical 0 low time	T0	-	560	-	us

Chapter 3 System

3.1. Memory Mapping

Module	Address(It is for Cluster CPU)	Size(Bytes)
N-BROM	0x0000 0000---0x0000 FFFF	64K
SRAM A1	0x0002 0000---0x0003 7FFF	96K
SRAM C	0x0002 8000---0x0005 8FFF	132K
SRAM A2	0x0010 0000---0x0010 3FFF	16K
	0x0010 4000---0x0011 BFFF	96K
DE	0x0100 0000---0x013F FFFF	4M
G2D	0x0148 0000---0x014B FFFF	256K
CE_NS	0x0190 4000---0x0190 47FF	2K
CE_S	0x0190 4800---0x0190 4FFF	2K
VE SRAM	0x01A0 0000---0x01BF FFFF	2M
VE	0x01C0 E000---0x01C0 FFFF	8K
ISE	0x01C1 0000---0x01C1 0FFF	4K
ISE_SRAM	0x01C1 1000---0x01C9 0FFF	512K
ISP_SRAM	0x01D0 0000---0x020F FFFF	4M
ISP	0x0210 0000---0x0210 5FFF	24K
EISE	0x0230 0000---0x0230 0FFF	4K
EISE_SRAM	0x0230 1000---0x0238 0FFF	512K
SYS_CFG	0x0300 0000---0x0300 0FFF	4K
CCU	0x0300 1000---0x0300 1FFF	4K
DMAC	0x0300 2000---0x0300 2FFF	4K
MSGBOX	0x0300 3000---0x0300 3FFF	4K
SPINLOCK	0x0300 4000---0x0300 4FFF	4K
HSTIMER	0x0300 5000---0x0300 5FFF	4K
SID	0x0300 6000---0x0300 6FFF	4K
TIMER	0x0300 9000---0x0300 93FF	1K
PWM	0x0300 A000---0x0300 A3FF	1K
GPIO	0x0300 B000---0x0300 B3FF	1K
PSI	0x0300 C000---0x0300 C3FF	1K
DCU	0x0301 0000---0x0301 FFFF	64K
GIC	0x0302 0000---0x0302 FFFF	64K
DRAM_CTRL	0x047F B000---0x047F FFFF	20K
PHY_CTRL	0x0480 0000---0x04FF FFFF	8M
MSI_CTRL	0x047F A000---0x047F AFFF	4K
NDFC	0x0401 1000---0x0401 1FFF	4K

SMHC0	0x0402 0000---0x0402 0FFF	4K
SMHC1	0x0402 1000---0x0402 1FFF	4K
SMHC2	0x0402 2000---0x0402 2FFF	4K
UART0	0x0500 0000---0x0500 03FF	1K
UART1	0x0500 0400---0x0500 07FF	1K
UART2	0x0500 0800---0x0500 0BFF	1K
UART3	0x0500 0C00---0x0500 0FFF	1K
UART4	0x0500 1000---0x0500 13FF	1K
TWI0	0x0500 2000---0x0500 23FF	1K
TWI1	0x0500 2400---0x0500 27FF	1K
TWI2	0x0500 2800---0x0500 2BFF	1K
TWI3	0x0500 2C00---0x0500 2FFF	1K
SPI0	0x0501 0000---0x0501 0FFF	4K
SPI1	0x0501 1000---0x0501 1FFF	4K
SPI2	0x0501 2000---0x0501 2FFF	4K
SPI3	0x0501 3000---0x0501 3FFF	4K
EMAC	0x0502 0000---0x0502 FFFF	64K
GPADC	0x0507 0000---0x0507 03FF	1K
THS	0x0507 0400---0x0507 07FF	1K
I2S/PCM0	0x0509 0000---0x0509 0FFF	4K
I2S/PCM1	0x0509 1000---0x0509 1FFF	4K
I2S/PCM2	0x0509 2000---0x0509 2FFF	4K
DMIC	0x0509 5000---0x0509 53FF	1K
Audio Codec	0x0509 6000---0x0509 6FFF	4K
USB2.0_OTG	0x0510 0000---0x051F FFFF	1M
HDMI_TX0	0x0600 0000---0x060F FFFF	1M
MIPI_DSI	0x0650 4000---0x0650 5FFF	8K
DISP_IF_TOP	0x0651 0000---0x0651 0FFF	4K
TCON_LCD0	0x0651 1000---0x0651 1FFF	4K
TCON_TV0	0x0651 5000---0x0651 5FFF	4K
TVE_TOP	0x0652 0000---0x0652 3FFF	16K
TVE	0x0652 4000---0x0652 7FFF	16K
VDPO	0x0654 2000---0x0654 2FFF	4K
CSI	0x0660 0000---0x0661 FFFF	128K
CSI_SRAM	0x0662 0000---0x0669 FFFF	512K
RTC	0x0700 0000---0x0700 03FF	1K
R_CPUS_CFG	0x0700 0400---0x0700 0BFF	2K
R_PRCM	0x0701 0000---0x0701 03FF	1K
R_TIMER	0x0702 0000---0x0702 03FF	1K
R_WDOG	0x0702 0400---0x0702 07FF	1K
R_PWM	0x0702 0C00---0x0702 0FFF	1K
R_INTC	0x0702 1000---0x0702 13FF	1K
R_GPIO	0x0702 2000---0x0702 23FF	1K
R_CIR_RX	0x0704 0000---0x0704 03FF	1K
R_OWC	0x0704 0400---0x0704 07FF	1K

R_UART	0x0708 0000---0x0708 03FF	1K
R_TWI0	0x0708 1400---0x0708 17FF	1K
R_TWI1	0x0708 1800---0x0708 1BFF	1K
R_RSB	0x0708 3000---0x0708 33FF	1K
CPUS_BIST	0x0710 0000---0x07100FFF	4K
CPU_SYS_CFG	0x0810 0000---0x0810 03FF	1K
TIMESTAMP_STU	0x0811 0000---0x0811 0FFF	4K
TIMESTAMP_CTRL	0x0812 0000---0x0812 0FFF	4K
C0_CPUX_CFG	0x0901 0000---0x0901 03FF	1K
C0_CPUX_MBIST	0x0902 0000---0x0902 0FFF	4K
DRAM SPACE	0x4000 0000---0xFFFF FFFF	3G

3.2. CPUX Configuration

3.2.1. Overview

The CPUX Configuration(CPUX_CFG) module is used to configure CLUSTER control, including power on,reset, cache, debug, and check the status of CPU. It will be used when you want to disable/enable the CPU, cluster switch, CPU status check, and debug, etc.

The CPUX_CFG module includes C0_CPUX_CFG and CPU_SUBSYS_CTRL.

The C0_CPUX_CFG module is used for configuring CLUSTER0, such as reset, control, cache, debug, CPU status.

The CPU_SUBSYS_CTRL module is used for the system resource control of CPU sub-system, such as GIC-400,JTAG.

The CPUX configuration includes the following features:

- CPU reset system: CORE reset,debug circuit reset and other reset function
- CPU related control: interface control, CP15 control, power on and power down control
- CPU status check: idle status, SMP status, interrupt status and so on
- CPU debug related register for control and status

3.2.2. CPUX Block Diagram

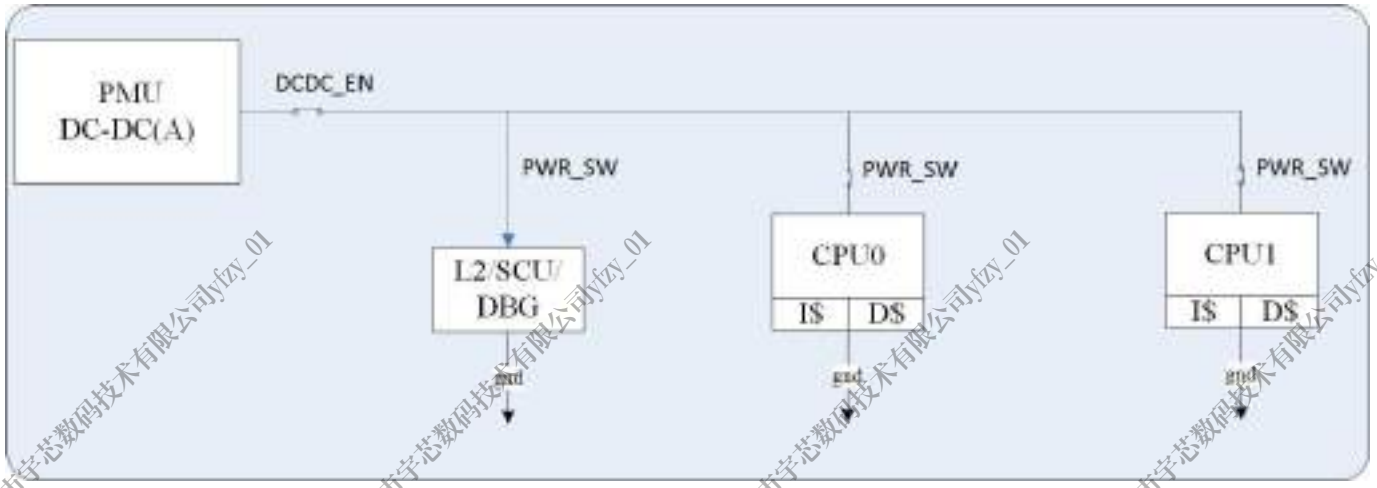


Figure 3-1. CPUX Power Domain Diagram

Figure 3-1 above lists the power domain of CLUSTER in default. All power switch of CPU core are default to power on.All CPU pwron_rst is de-asserted, core reset of CPU0 is de-asserted,core reset of CPU1 is asserted.

Since each CPU core and its appended circuits have the same power domain, the processor and related L1 cache, neon and vfp should be taken as a whole core.

3.2.3. Operations and Functional Descriptions

3.2.3.1. **Signal Description**

For the detail of CPUX signal, please refer to ***ARM Cortex-A7 TRM***.

3.2.3.2. L2 Idle Mode

When the L2 of Cluster needs to enter WFI mode, firstly make sure the CPU0/1 of Cluster enter WFI mode, which can be checked through the bit[17:16] of **Cluster CPU Status Register**, and then pull high the **ACINACTM** of Cluster by writing 1 to the bit0 of **Cluster Control Register1** , and then check whether L2 enters idle status by checking whether the **STANDBYWFIL2** is high. Remember to set the **ACINACTM** to low when exiting the L2 idle mode.

3.2.3.3. CPUX Reset System

The CPUX reset includes **core reset**, **power-on reset** and **H_Reset**. And their scopes rank: **core reset** < **power-on Reset** < **H_Reset**. The description of all reset signal in CPUX Reset System is as follows.

Table 3-1. Reset Signal Description

Reset signal	Description
CORE_RST	This is the primary reset signal which resets the corresponding core logic that includes NEON and VFP, Debug, ETM, breakpoint and watchpoint logic. This maps to a warm reset that covers reset of the processor logic.
PWRON_RST	This power-on reset signal resets all the processor logic, including the Debug, ETM trace unit, breakpoint, watchpoint logic, and performance monitors logic. This maps to a cold reset that covers reset of the processor logic and the integrated debug functionality. This does not reset debug logic in the debug power domain. Including CORE_RST/ETM_RST/DBG_RST.
AXI2MBUS_RST	Reset the AXI2MBUS interface logic circuit.
L2_RST	This single, cluster-wide signal resets the L2 memory system and the logic in the SCU.
ETM_RST	Reset ETM debug logic circuit.
DBG_RST	Reset only the debug, and breakpoint and watchpoint logic in the processor power domain. It also resets the debug logic for each processor in the debug power domain.
SOC_DBG_RST	Reset all the debug logic including DBG_RST.
MBIST_RST	Reset all resettable registers in the cluster, for entry into, and exit from, MBIST mode.
H_RST	Including PWRON_RST/L2_RST/MBIST_RST/SOC_DBG_RST/C0_CPUX_CFG.
CPU_SUBSYS_RST	Including C0_H_RST/GIC-400/CPU_SUBSYS_CTRL.

3.2.3.4. Operation Principle

The CPU-related operation needs proper configuration of CPUCFG related register, as well as related system control resource including BUS, clock ,reset and power control.

3.2.4. Programming Guidelines

For CPU core and cluster operation,please see *V536-H/V526_CPU_AP_Note.pdf*.

3.2.5. Cluster Configuration Register List

Module Name	Base Address
CPU_CFG	0x09010000

Register Name	Offset	Description
C0_RST_CTRL	0x0000	Cluster 0 Reset Control Register
C0_CTRL_REG0	0x0010	Cluster 0 Control Register0
C0_CTRL_REG1	0x0014	Cluster 0 Control Register1
C0_CTRL_REG2	0x0018	Cluster 0 Control Register2
CACHE_CFG_REG	0x0024	Cache Configuration Register
C0_CPU_STATUS	0x0080	Cluster 0 CPU Status Register
L2_STATUS_REG	0x0084	Cluster 0 L2 Status Register
DBG_REG0	0x00C0	Cluster 0 Debug Control Register0
DBG_REG1	0x00C4	Cluster 0 Debug Control Register1

3.2.6. Cluster Configuration Register Description

3.2.6.1. Cluster 0 Reset Control Register(Default Value: 0x13FF_0101)

Offset: 0x0000			Register Name: C0_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	DDR_RST AXI2MBUS Logic Circuit Reset 0: Assert 1: De-assert
27:26	/	/	/
25	R/W	0x1	MBIST_RST CPUBIST Reset The reset signal for test. 0: Assert 1: De-assert
24	R/W	0x1	SOC_DBG_RST Cluster SOC Debug Reset 0: Assert 1: De-assert
23:22	/	/	/
21:20	R/W	0x3	ETM_RST Cluster ETM Reset Assert. 0: assert 1: de-assert
19:18	/	/	/
17:16	R/W	0x3	DBG_RST Cluster Debug Reset Assert

			0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x1	L2_RST Cluster L2 Cache Reset 0: Assert 1: De-assert
7:2	/	/	/
1:0	R/W	0x1	CORE_RESET Cluster CPU[1:0] Reset Assert 0: Assert 1: De-assert

3.2.6.2. **Cluster 0 Control Register0(Default Value:0x8000_0000)**

Offset: 0x0010			**Register Name: C0_CTRL_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	SYSBAR_DISABLE Disable broadcasting of barriers onto system bus 0: Barriers are broadcast onto system bus,this requires an AMBA4 interconnect. 1: Barriers are not broadcast onto the system bus.This is compatible with an AXI3 interconnect.
30	R/W	0x0	BROADCAST_INNER Enable broadcasting of inner shareable transactions 0: Inner shareable transactions are not broadcasted externally. 1: Inner shareable transactions are broadcasted externally.
29	R/W	0x0	BROADCAST_OUTER Enable broadcasting of outer shareable transactions 0: Outer Shareable transactions are not broadcasted externally. 0: Outer Shareable transactions are broadcasted externally.
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches 0: Cache maintenance operations are not broadcasted to downstream caches. 1: Cache maintenance operations are broadcasted to downstream caches.
27:10	/	/	/
9:8	R/W	0x0	CP15S_DISABLE Disable write access to some secure CP15 register.
7:5	/	/	/
4	R/W	0x0	L2_RST_DISABLE Disable automatic L2 cache invalidate at reset. 0: L2 cache is reset by hardware. 1: L2 cache is not reset by hardware.

3:2	/	/	/
1:0	R/W	0x0	L1_RST_DISABLE Disable automatic Cluster CPU[1:0] L1 cache invalidate at reset. 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

3.2.6.3. **Cluster 0 Control Register1(Default Value:0x0000_0000)**

Offset: 0x0014			**Register Name: C0_CTRL_REG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ACINACTM Snoop interface is inactive and no longer accepting requests. 0: Snoop interface is active 1: Snoop interface is inactive

3.2.6.4. **Cluster 0 Control Register2(Default Value:0x0000_0010)**

Offset: 0x0018			**Register Name: C0_CTRL_REG2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	EVENTI Event input for processor wake-up from WFE state. This bit must remain HIGH for at least one clock cycle to be visible by the cores.
23:22	/	/	/
21:20	R/W	0x0	EXM_CLR[1:0] Clear the status of interface.
19:0	/	/	/

3.2.6.5. **Cache Configuration Register (Default Value: 0x0000_001A)**

Offset: 0x0024			**Register Name: CACHE_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:3	R/W	0x3	EMA[2:0] Cache SRAM EMA control port
2:1	R/W	0x1	EMAW[1:0] Cache SRAM EMAW control port
0	R/W	0x0	EMAS Cache SRAM EMAS control port

3.2.6.6. Cluster0 CPU Status Register(Default Value: 0x0001_0000)

Offset: 0x0080			Register Name: C0_CPU_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R	0x0	SMP_AMP CPU[1:0] is in symmetric multiprocessing mode or asymmetric multiprocessing mode. 0: AMP mode 1: SMP mode
23:18	/	/	/
17:16	R	0x1	STANDBYWFI Indicates if Cluster CPU[1:0] is in WFI standby mode. 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
15:10	/	/	/
9:8	R	0x0	STANDBYWFE Indicates if Cluster CPU[1:0] is in the WFE standby mode. 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
7:1	/	/	/
0	R	0x0	STANDBYWFIL2 Indicates if the Cluster L2 memory system is in WFI standby mode. 0: Cluster L2 not in WFI standby mode 1: Cluster L2 in WFI standby mode

3.2.6.7. L2 Status Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: L2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R	0x0	EVENTO Event output This bit is asserted HIGH for 3 clock cycles when any core in the cluster executes an SEV instruction.
8:0	/	/	/

3.2.6.8. Cluster 0 Debug Control Register0(Default Value:0x0000_0003)

Offset: 0x00C0			Register Name: DBG_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	DBGRESTART[1:0] External restart requests.

7:2	/	/	/
1:0	R/W	0x3	C_DBGPWRDUP Cluster Powered-up 0: Core is powered down 1: Core is powered up

3.2.6.9. **Cluster 0 Debug Control Register1 (Default Value: 0x0000_0000)**

Offset: 0x00C4			**Register Name: DBG_REG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	DBGRESTARTED[1:0] Handshake for DBGRESTART.
11:6	/	/	/
5:4	R	0x0	C_DBGNOPWRDWN No power-down request. Debugger has requested that processor is not powered down. Debug no power down[1:0].
3:2	/	/	/
3:0	R	0x0	C_DBGPWRUPREQ Power up request. Debug power up request[1:0] 0: Do not request that the core is powered up 1: Request that the core is powered up

3.2.7. CPU Subsystem Control Register List

Module Name	**Base Address**
CPU_SUBSYS_CTRL	0x08100000

Register Name	**Offset**	**Description**
GENER_CTRL_REG0	0x0000	General Control Register0
GIC_JTAG_RST_CTRL	0x000C	GIC and Jtag Reset Control Register
C0_INT_EN	0x0010	Cluster0 Interrupt Enable Control Register
IRQ_FIQ_STATUS	0x0014	GIC IRQ/FIQ Status Register
GENER_CTRL_REG2	0x0018	General Control Register2

3.2.8. CPU Subsystem Control Register Description

3.2.8.1. **General Control Register0(Default Value: 0x0000_0000)**

Offset: 0x0000			**Register Name: GENER_CTRL_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:1	/	/	/
0	R/W	0x0	GIC_CFGSDISABLE Disables write access to some secure GIC registers.

3.2.8.2. **GIC and Jtag Reset Control Register(Default Value: 0x0000_0F01)**

Offset: 0x000C			**Register Name: GIC_JTAG_RST_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x0	EXM_CLR[1:0] Clear the status of interface, for debug
15:12	/	/	/
11	R/W	0x1	CS_RST CoreSight reset 0: Assert 1: De-assert
10	/	/	/
9	R/W	0x1	PORTRST Jtag portrst 0: Assert 1: De-assert
8	R/W	0x1	TRST Jtag trst 0: Assert 1: De-assert
7:1	/	/	/
0	R/W	0x1	GIC_RESET Gic_reset_cpu_reg 0: Assert 1: De-assert

3.2.8.3. **Cluster 0 Interrupt Enable Register(Default Value: 0x0000_FFFF)**

Offset: 0x0010			**Register Name: C0_INT_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	C0_GIC_EN Interrupt enable control register. Mask irq_out/firq_out to system domain.

3.2.8.4. **GIC IRQ/FIQ Status Register(Default Value: 0x0000_0000)**

Offset: 0x0014			**Register Name: IRQ_FIQ_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	R/W	0x0000	FIQ_OUT[15:0]
15:0	R/W	0x0000	IRQ_OUT[15:0]

3.2.8.5. **General Control Register2(Default Value: 0x0000_0000)**

Offset: 0x0018			**Register Name: GENER_CTRL_REG2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CDBGRSTACK
15:1	/	/	/
0	R/W	0x0	C0_TSCLKCHANGE

3.3. CCU

3.3.1. Overview

The CCU controls the PLLs configuration and most of the clock generation, division, distribution, synchronization and gating. CCU input signals include the external clock for the reference frequency (24MHz). The outputs from CCU are mostly clocks to other blocks in the system.

The CCU includes the following features:

- 12 PLLs
- Bus Source and Divisions
- Clock Output Control
- PLL Bias Control
- PLL Tuning Control
- PLL Pattern Control
- Configuring Modules Clock
- Bus Clock Gating
- Bus Software Reset
- PLL Lock Control

3.3.2. Operations and Functional Descriptions

3.3.2.1. System Bus Tree

Figure 3-2 shows a block diagram of the System Bus Tree.

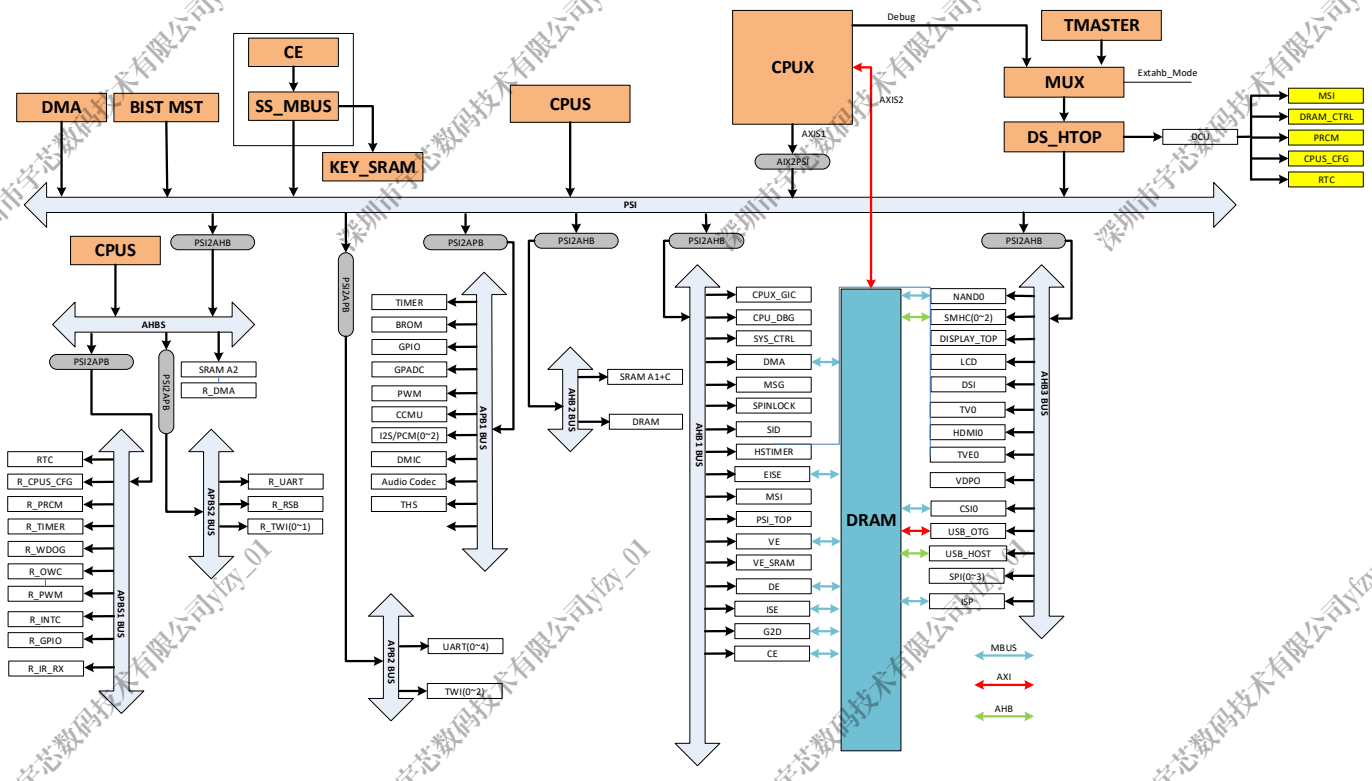
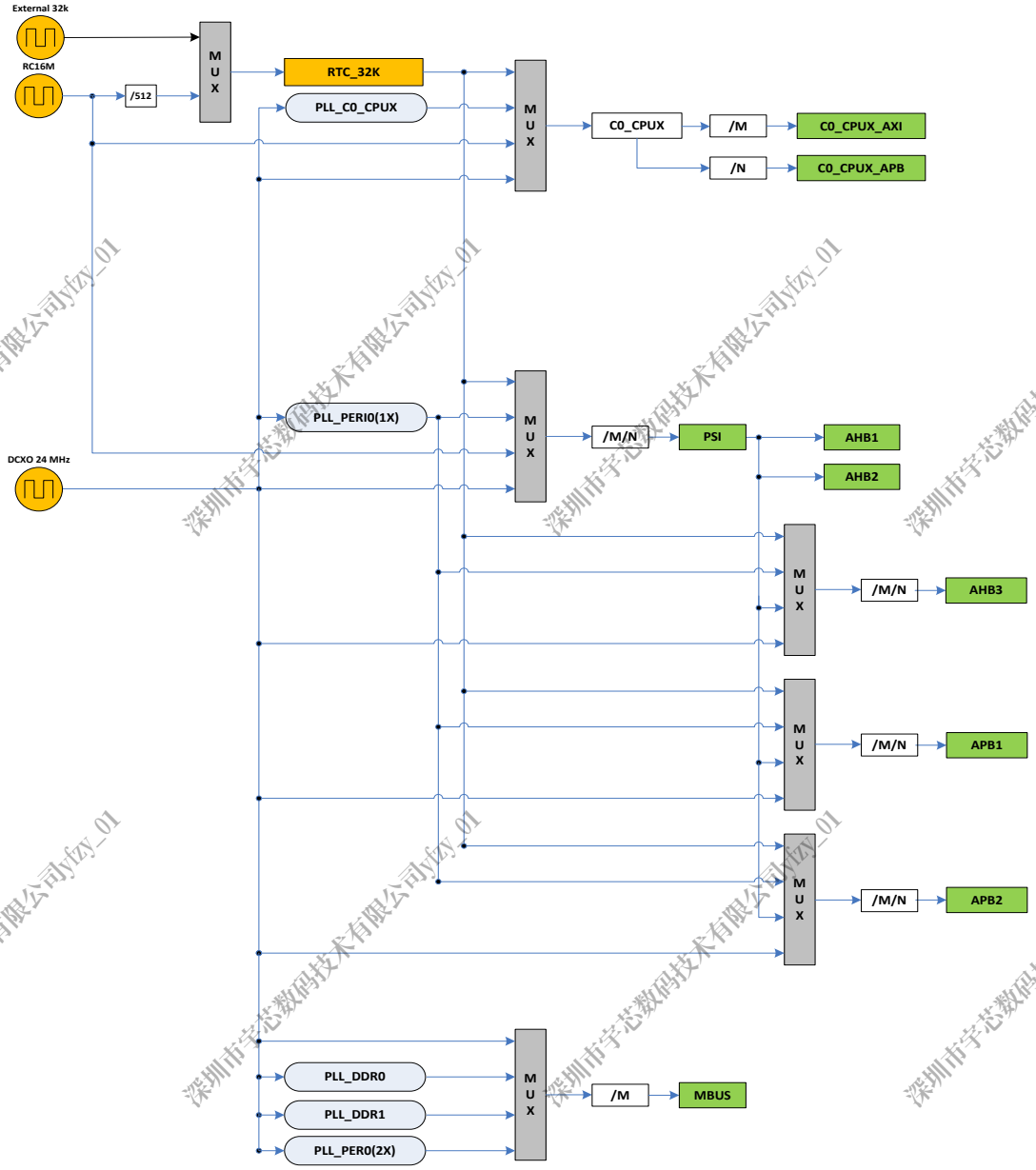


Figure 3-2. System Bus Tree

3.3.2.2. **Bus Clock Tree**

Figure 3-3 shows a block diagram of the Bus Clock Tree.



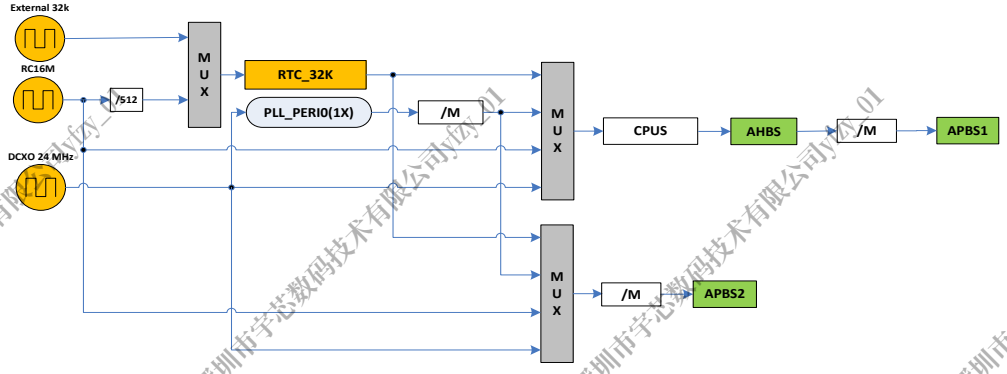


Figure 3-3. Bus Clock Tree

3.3.2.3. **Module Clock Tree**

Figure 3-4 shows the block diagram of the Module Clock Tree.

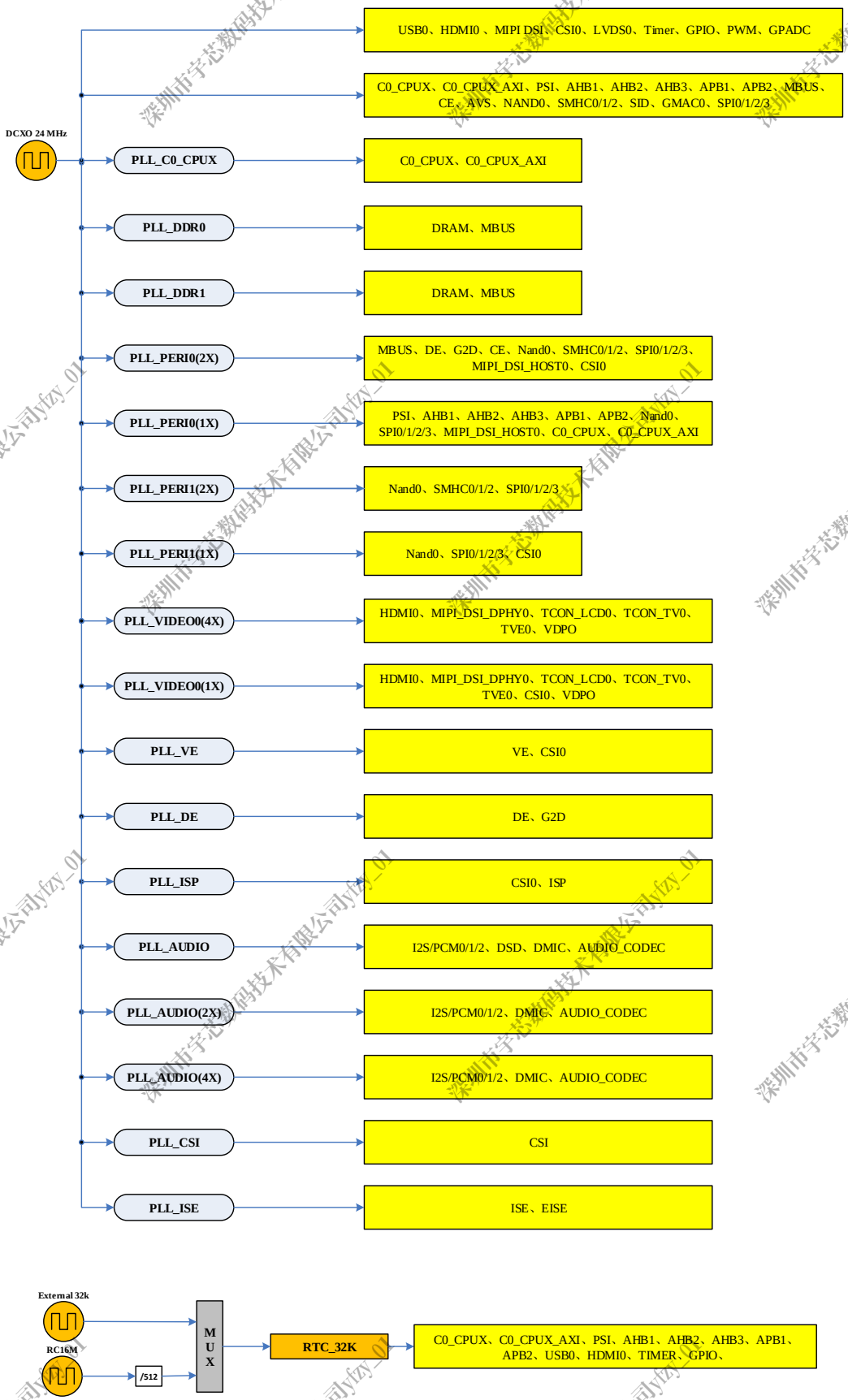


Figure 3-4. Module Clock Tree

3.3.2.4. Typical Applications

PLL applications: use the available clock sources to generate clock roots to various parts of the chip.

Table 3-2. PLL Typical Applications

PLLs	Typical Applications	Description
PLL_CPUX	CPUX	Support DVFS
PLL_DDR0	MBUS,DRAM	Support spread spectrum Not support linear frequency scaling
PLL_DDR1	MBUS,DRAM	Support spread spectrum Not support linear frequency scaling
PLL_PERI0(2X)	MBUS, DE,G2D,CE,NAND0,SMHC0/1/2, SPI0/1/2/3, MIPI_DSI_HOST	Not Support DVFS
PLL_PERI0(1X)	PSI,AHB1,AHB2,AHB3,APB1,APB2 ,NAND, SPI0/1/2/3 , MIPI_DSI_HOST, CSI, CPU, CPU_AXI	Not Support DVFS
PLL_PERI1(2X)	NAND,SMHC0/1/2,SPI0/1/2/3	Not Support DVFS
PLL_PERI1(1X)	NAND0,SPI0/1/2/3,CSI	Not Support DVFS
PLL_VIDEO0(4X)	HDMI,TCON_LCD,TCON_TV,MIPI_DSI_DPHY, TVE,VDPO	Not Support DVFS
PLL_VIDEO0(1X)	HDMI,TCON_LCD,TCON_TV,MIPI_DSI_DPHY, TVE,VDPO, CSI	Not Support DVFS
PLL_VE	VE,CSI_TOP	Not Support DVFS
PLL_DE	DE,G2D	Not Support DVFS
PLL_ISP	CSI, ISP	Not Support DVFS
PLL_AUDIO	I2S/PCM0,I2S/PCM1,I2S/PCM2, DMIC, AUDIO_CODEC	Not Support DVFS
PLL_AUDIO(2X)	I2S/PCM0,I2S/PCM1,I2S/PCM2, DMIC, AUDIO_CODEC	Not Support DVFS
PLL_AUDIO(4X)	I2S/PCM0,I2S/PCM1,I2S/PCM2, DMIC, AUDIO_CODEC	Not Support DVFS
PLL_ISE	ISE	Not Support DVFS
PLL_CSI	CSI	

DVFS: dynamic voltage and frequency scaling.

3.3.2.5. **PLL Features**

Table 3-3. PLL Features

PLL	Stable Operating Frequency	Actual Operating Frequency	Spread Spectrum	Linear FM	Rate Control	Pk-Pk	Lock Time
PLL_CPUX	288MHz~5.0GHz (24*N/div1)	288MHz~1.8GHz	No	No	No	<200ps	1.5ms
PLL_AUDIO	24.576MHz 22.5792MHz (24*N/div1/div2)	24.576MHz 22.5792MHz (24.576*8)MHz (22.5792*8)MHz	Yes(fractional frequency-dividing)	No	No	<200ps	500us
PLL_PERI0(2X)	180MHz~3.0GHz (24*N/div1/div2)	1.2GHz	Yes	No	No	<200ps	500us
PLL_PERI1(2X)	180MHz~3.0GHz (24*N/div1/div2)	1.2GHz	Yes	No	No	<200ps	500us
PLL_VIDEO0(4X)	252MHz~3.0GHz (24*N/Div)	192MHz~1200MHz	Yes	No	No	<200ps	500us
PLL_VE	180MHz~3.0GHz (24*N/div1/div2)	192MHz~600MHz	Yes	No	No	<200ps	500us
PLL_DDR0	180MHz~3.0GHz (24*N/div1/div2)	192MHz~2.0GHz	Yes	No	No	200MHz~800MHz(<200ps) 800MHz~1.3GHz(<140ps) 1.3GHz~2.0GHz(<100ps)	2ms
PLL_DDR1	180MHz~3.0GHz (24*N/div1/div2)	192MHz~2.0GHz	Yes	No	No	200MHz~800MHz(<200ps) 800MHz~1.3GHz(<140ps) 1.3GHz~2.0GHz(<100ps)	2ms
PLL_DE	180MHz~3GHz (24*N/div1/div2)	192MHz~600MHz	Yes	No	No	<200ps	500us
PLL_ISE	180MHz~3GHz (24*N/div1/div2)	300MHz~600MHz	Yes	No	No	<200ps	500us
PLL_ISP	180MHz~3GHz (24*N/div1/div2)	192MHz~600MHz	Yes	No	No	<200ps	500us
PLL_CSI	180MHz~3GHz (24*N/div1/div2)	192MHz~600MHz	Yes	No	No	<200ps	500us

3.3.3. Programming Guidelines

3.3.3.1. PLL

(1) In practical application, other PLLs do not support dynamic frequency scaling except for PLL_CPUX.

(2) The user guide of PLL Lock(using PLL_CPUX as an example)

(a).PLL_CPUX from close to open:

- Write 0 to the bit29 of **PLL_CPUX_CTRL_REG**.
- Configure the parameters **(N,M,P)** of **PLL_CPUX_CTRL_REG**.
- Write 1 to the **Enable** bit of **PLL_CPUX_CTRL_REG**.
- Write 1 to the bit29 of **PLL_CPUX_CTRL_REG**.
- Read the bit28 of **PLL_CPUX_CTRL_REG**, when it is 1, then CPUX PLL is locked.
- Delay 20us.

(b).PLL_CPUX frequency conversion:

- Write 0 to the bit29 of **PLL_CPUX_CTRL_REG**.
- Configure the parameters **(N,M,P)** of **PLL_CPUX_CTRL_REG**.
- Write 1 to the bit29 of **PLL_CPUX_CTRL_REG**.
- Read the bit28 of **PLL_CPUX_CTRL_REG**, when it is 1, then CPUX PLL is locked.
- Delay 20us.

(c).PLL_CPUX from open to close:

- Write 0 to the **Enable** bit of **PLL_CPUX_CTRL_REG**.
- Write 0 to the bit29 of **PLL_CPUX_CTRL_REG**.

3.3.3.2. BUS

(1) When setting the BUS clock , you should set the division factor firstly, and after the division factor becomes valid, switch the clock source. The clock source will be switched after at least three clock cycles.

(2) The BUS clock should not be dynamically changed in most applications.

3.3.3.3. Clock Switch

Make sure that the clock source output is valid before the clock source switch, and then set a proper divide ratio; after the division factor becomes valid, switch the clock source.

3.3.3.4. Gating and Reset

Make sure that the reset signal has been released before the release of module clock gating.

3.3.4. Register List

Module Name	Base Address
CCU	0x03001000

Register Name	Offset	Description
PLL_CPUX_CTRL_REG	0x0000	PLL_CPUX Control Register
PLL_DDR0_CTRL_REG	0x0010	PLL_DDR0 Control Register
PLL_DDR1_CTRL_REG	0x0018	PLL_DDR1 Control Register
PLL_PERI0_CTRL_REG	0x0020	PLL_PERI0 Control Register
PLL_PERI1_CTRL_REG	0x0028	PLL_PERI1 Control Register
PLL_VIDEO0_CTRL_REG	0x0040	PLL_VIDEO0 Control Register
PLL_VE_CTRL_REG	0x0058	PLL_VE Control Register
PLL_DE_CTRL_REG	0x0060	PLL_DE Control Register
PLL_ISP_CTRL_REG	0x0068	PLL_ISP Control Register
PLL_AUDIO_CTRL_REG	0x0078	PLL_AUDIO Control Register
PLL_ISE_CTRL_REG	0x00D0	PLL_ISE Control Register
PLL_CSI_CTRL_REG	0x00E0	PLL_CSI Control Register
PLL_DDR0_PAT_CTRL_REG	0x0110	PLL_DDR0 Pattern Control Register
PLL_DDR1_PAT_CTRL_REG	0x0118	PLL_DDR1 Pattern Control Register
PLL_PERI0_PAT0_CTRL_REG	0x0120	PLL_PERI0 Pattern0 Control Register
PLL_PERI0_PAT1_CTRL_REG	0x0124	PLL_PERI0 Pattern1 Control Register
PLL_PERI1_PAT0_CTRL_REG	0x0128	PLL_PERI1 Pattern0 Control Register
PLL_PERI1_PAT1_CTRL_REG	0x012C	PLL_PERI1 Pattern1 Control Register
PLL_VIDEO0_PAT0_CTRL_REG	0x0140	PLL_VIDEO0 Pattern0 Control Register
PLL_VIDEO0_PAT1_CTRL_REG	0x0144	PLL_VIDEO0 Pattern1 Control Register
PLL_VE_PAT0_CTRL_REG	0x0158	PLL_VE Pattern0 Control Register
PLL_VE_PAT1_CTRL_REG	0x015C	PLL_VE Pattern1 Control Register
PLL_DE_PAT0_CTRL_REG	0x0160	PLL_DE Pattern0 Control Register
PLL_DE_PAT1_CTRL_REG	0x0164	PLL_DE Pattern1 Control Register
PLL_ISP_PAT0_CTRL_REG	0x0168	PLL_ISP Pattern0 Control Register
PLL_ISP_PAT1_CTRL_REG	0x016C	PLL_ISP Pattern1 Control Register
PLL_AUDIO_PAT0_CTRL_REG	0x0178	PLL_AUDIO Pattern0 Control Register
PLL_AUDIO_PAT1_CTRL_REG	0x017C	PLL_AUDIO Pattern1 Control Register
PLL_ISE_PAT0_CTRL_REG	0x01D0	PLL_ISE Pattern0 Control Register
PLL_ISE_PAT1_CTRL_REG	0x01D4	PLL_ISE Pattern1 Control Register
PLL_CSI_PAT0_CTRL_REG	0x01E0	PLL_CSI Pattern0 Control Register
PLL_CSI_PAT1_CTRL_REG	0x01E4	PLL_CSI Pattern1 Control Register
PLL_C0_CPUX_BIAS_REG	0x0300	PLL_C0_CPUX Bias Register
PLL_DDR0_BIAS_REG	0x0310	PLL_DDR0 Bias Register
PLL_DDR1_BIAS_REG	0x0318	PLL_DDR1 Bias Register
PLL_PERI0_BIAS_REG	0x0320	PLL_PERI0 Bias Register
PLL_PERI1_BIAS_REG	0x0328	PLL_PERI1 Bias Register
PLL_VIDEO0_BIAS_REG	0x0340	PLL_VIDEO0 Bias Register
PLL_VE_BIAS_REG	0x0358	PLL_VE Bias Register

PLL_DE_BIAS_REG	0x0360	PLL_DE Bias Register
PLL_ISP_BIAS_REG	0x0368	PLL_ISP Bias Register
PLL_AUDIO_BIAS_REG	0x0378	PLL_AUDIO Bias Register
PLL_ISE_BIAS_REG	0x03D0	PLL_ISE Bias Register
PLL_CSI_BIAS_REG	0x03E0	PLL_CSI Bias Register
PLL_C0_CPUX_TUN_REG	0x0400	PLL_C0_CPUX Tuning Register
C0_CPUX_AXI_CFG_REG	0x0500	C0_CPUX_AXI Configuration Register
PSI_AHB1_AHB2_CFG_REG	0x0510	PSI_AHB1_AHB2 Configuration Register
AHB3_CFG_REG	0x051C	AHB3 Configuration Register
APB1_CFG_REG	0x0520	APB1 Configuration Register
APB2_CFG_REG	0x0524	APB2 Configuration Register
MBUS_CFG_REG	0x0540	MBUS Configuration Register
DE_CLK_REG	0x0600	DE Clock Register
DE_BGR_REG	0x060C	DE Bus Gating Reset Register
G2D_CLK_REG	0x0630	G2D Clock Register
G2D_BGR_REG	0x063C	G2D Bus Gating Reset Register
CE_CLK_REG	0x0680	CE Clock Register
CE_BGR_REG	0x068C	CE Bus Gating Reset Register
VE_CLK_REG	0x0690	VE Clock Register
VE_BGR_REG	0x069C	VE Bus Gating Reset Register
ISE_CLK_REG	0x06A0	ISE Clock Register
ISE_BGR_REG	0x06AC	ISE Bus Gating Reset Register
EISE_CLK_REG	0x06D0	EISE Clock Register
EISE_BGR_REG	0x06DC	EISE Bus Gating Reset Register
DMA_BGR_REG	0x070C	DMA Bus Gating Reset Register
MSGBOX_BGR_REG	0x071C	Message-Box Bus Gating Reset Register
SPINLOCK_BGR_REG	0x072C	Spin-Lock Bus Gating Reset Register
HSTIMER_BGR_REG	0x073C	HS-Timer Bus Gating Reset Register
AVS_CLK_REG	0x0740	AVS Clock Register
DBGSYS_BGR_REG	0x078C	DBGSYS Bus Gating Reset Register
PSI_BGR_REG	0x079C	PSI Bus Gating Reset Register
PWM_BGR_REG	0x07AC	PWM Bus Gating Reset Register
DRAM_CLK_REG	0x0800	DRAM Clock Register
MBUS_MST_CLK_GATING_REG	0x0804	MBUS Master Clock Gating Register
DRAM_BGR_REG	0x080C	DRAM Bus Gating Reset Register
NAND0_0_CLK_REG	0x0810	NAND0_0 Clock Register
NAND0_1_CLK_REG	0x0814	NAND0_1 Clock Register
NAND_BGR_REG	0x082C	NAND Bus Gating Reset Register
SMHC0_CLK_REG	0x0830	SMHC0 Clock Register
SMHC1_CLK_REG	0x0834	SMHC1 Clock Register
SMHC2_CLK_REG	0x0838	SMHC2 Clock Register
SMHC_BGR_REG	0x084C	SMHC Bus Gating Reset Register
UART_BGR_REG	0x090C	UART Bus Gating Reset Register
TWI_BGR_REG	0x091C	TWI Bus Gating Reset Register
SPI0_CLK_REG	0x0940	SPI0 Clock Register

SPI1_CLK_REG	0x0944	SPI1 Clock Register
SPI2_CLK_REG	0x0948	SPI2 Clock Register
SPI3_CLK_REG	0x094C	SPI3 Clock Register
SPI_BGR_REG	0x096C	SPI Bus Gating Reset Register
EPHY_25M_CLK_REG	0x0970	EPHY_25M Clock Register
EMAC_BGR_REG	0x097C	EMAC Bus Gating Reset Register
GPADC_BGR_REG	0x09EC	GPADC Bus Gating Reset Register
THS_BGR_REG	0x09FC	THS Bus Gating Reset Register
I2S/PCM0_CLK_REG	0x0A10	I2S/PCM0 Clock Register
I2S/PCM1_CLK_REG	0x0A14	I2S/PCM1 Clock Register
I2S/PCM2_CLK_REG	0x0A18	I2S/PCM2 Clock Register
I2S/PCM_BGR_REG	0x0A1C	I2S/PCM Bus Gating Reset Register
DMIC_CLK_REG	0x0A40	DMIC Clock Register
DMIC_BGR_REG	0x0A4C	DMIC Bus Gating Reset Register
AUDIO_CODEC_1X_CLK_REG	0x0A50	Audio Codec 1X Clock Register
AUDIO_CODEC_4X_CLK_REG	0x0A54	Audio Codec 4X Clock Register
AUDIO_CODEC_BGR_REG	0x0A5C	Audio Codec Bus Gating Reset Register
USB2.0_OTG_CLK_REG	0x0A70	USB2.0_OTG Clock Register
USB_CGR_REG	0x0A8C	USB Clock Gating Reset Register
HDMI_CLK_REG	0x0B00	HDMI Clock Register
HDMI_SLOW_CLK_REG	0x0B04	HDMI Slow Clock Register
HDMI_CEC_CLK_REG	0x0B10	HDMI CEC Clock Register
HDMI_BGR_REG	0x0B1C	HDMI Bus Gating Reset Register
MIPI_DSI_DPHY_HS_CLK_REG	0x0B20	MIPI DSI DPHY High Speed Clock Register
MIPI_DSI_HOST_CLK_REG	0x0B24	MIPI DSI HOST Clock Register
MIPI_DSI_BGR_REG	0x0B4C	MIPI DSI Bus Gating Reset Register
DISPLAY_IF_TOP_BGR_REG	0x0B5C	DISPLAY_IF_TOP Bus Gating Reset Register
TCON_LCD0_CLK_REG	0x0B60	TCON_LCD0 Clock Register
TCON_LCD_BGR_REG	0x0B7C	TCON_LCD Bus Gating Reset Register
TCON_TV0_CLK_REG	0x0B80	TCON_TV0 Clock Register
TCON_TV_BGR_REG	0x0B9C	TCON_TV Bus Gating Reset Register
TVE_CLK_REG	0x0BB0	TVE Clock Register
TVE_BGR_REG	0x0BBC	TVE Bus Gating Reset Register
CSI_MISC_CLK_REG	0x0C00	CSI MISC Clock Register
CSI_TOP_CLK_REG	0x0C04	CSI TOP Clock Register
CSI_MCLK0_REG	0x0C08	CSI Master Clock0 Register
CSI_MCLK1_REG	0x0C0C	CSI Master Clock1 Register
ISP_CLK_REG	0x0C20	ISP Clock Register
CSI_BGR_REG	0x0C2C	CSI Bus Gating Reset Register
VDPO_CLK_REG	0x0C50	VDPO Clock Register
VDPO_BGR_REG	0x0C5C	VDPO Bus Gating Reset Register
PLL_LOCK_DBG_CTRL_REG	0x0F04	PLL Lock Debug Control Register

3.3.5. Register Description

3.3.5.1. **PLL_CPUX Control Register (Default Value: 0x0A00_1000)**

Offset: 0x0000			Register Name: PLL_CPUX_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_CPUX= 24MHz*N/P Its default value is 408MHz, its output range is from 200MHz to 3GHz.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:24	R/W	0x2	PLL_LOCK_TIME. PLL Lock Time. This bit is a stepping range from a frequency to another frequency,it can adjust the speed of clock changing. Not recommended to modify the value.
23:18	/	/	/
17:16	R/W	0x0	PLL_OUT_EXT_DIVP. PLL Output External Divider P. 00: 1 01: 2 10: 4 When output clock is less than 288MHz,clock frequency is output by dividing P.
15:8	R/W	0x10	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M PLL Factor M M = PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3. The M factor is only for test.

3.3.5.2. PLL_DDR0 Control Register (Default Value: 0x0800_2301)

Offset: 0x0010			Register Name: PLL_DDR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_DDR0 = 24MHz*N/M0/M1. PLL_DDR0 is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.3. PLL_DDR1 Control Register (Default Value: 0x0800_2301)

Offset: 0x0018	Register Name: PLL_DDR1_CTRL_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_DDR1 = 24MHz*N/M0/M1. PLL_DDR1 is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.4. PLL_PERI0 Control Register (Default Value: 0x0800_3100)

Offset: 0x0020			Register Name: PLL_PERI0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_PERI0 = 24MHz*N/M0/M1.

			PLL_PERI0 is 1.2GHz by default.It is not suggested to change the value.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x31	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.5. PLL_PERI1 Control Register (Default Value: 0x0800_3100)

Offset: 0x0028			**Register Name: PLL_PERI1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_PERI1= 24MHz*N/M0/M1. PLL_PERI1 is 1.2GHz by default. It is not suggested to change the value.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable

			0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x31	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.6. **PLL_VIDEO0 Control Register (Default Value: 0x0800_6203)**

Offset: 0x0040			**Register Name: PLL_VIDEO0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable For application, PLL_VIDEO0(4X)= 24MHz*N/M. PLL_VIDEO0(1X)=24MHz*N/M/4. PLL_VIDEO0 is 1188MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK_STATUS

			0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV_M PLL Input Div M M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_D PLL Output Div D (This factor is used for testing.) M0=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. For test, PLL_VIDEO0(4X) =24MHz*N/M/D

3.3.5.7. **PLL_VE Control Register (Default Value: 0x0800_2301)**

Offset: 0x0058			**Register Name: PLL_VE_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_VE = 24MHz*N/M0/M1. PLL_VE is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK_STATUS 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable

			1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.8. **PLL_DE Control Register (Default Value: 0x0800_2301)**

Offset: 0x0060			**Register Name: PLL_DE_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable The PLL_DE = 24MHz*N/M0/M1. PLL_DE is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK_STATUS 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable

23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.9. **PLL_ISP Control Register (Default Value: 0x0800_2301)**

Offset: 0x0068			**Register Name: PLL_ISP_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_ISP = 24MHz*N/M0/M1. PLL_ISP is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK_STATUS 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254.

			In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.10. **PLL_AUDIO Control Register (Default Value: 0x0814_2A01)**

Offset: 0x0078			**Register Name: PLL_AUDIO_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable This PLL is for Audio. PLL_AUDIO = 24MHz*N/M0/M1/P. PLL_AUDIO(4X) = 24MHz*N/M1/2 PLL_AUDIO(2X) = 24MHz*N/M1/4 7.5≤N/M0/M1≤125 and 12≤N 24MHz*N/M0/M1: 180MHz~3.0GHz PLL_AUDIO is 24.5714 MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK_STATUS 0:Unlocked 1: Locked (It indicates that the PLL has been stable.) The bit28 is valid when only the bit29 is set to 1.
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:22	/	/	/
21:16	R/W	0x14	PLL_POST_DIV_P PLL Post-div P P= PLL_POST_DIV_P +1

			PLL_POST_DIV_P is from 0 to 63.
15:8	R/W	0x2A	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.11. **PLL_ISE Control Register (Default Value: 0x0800_2301)**

Offset: 0x00D0			**Register Name: PLL_ISE_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_ISE = 24MHz*N/M0/M1. PLL_ISE is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK_STATUS 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254.

			In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.12. **PLL_CSI Control Register (Default Value: 0x0000_2301)**

Offset: 0x00E0			**Register Name: PLL_CSI_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. The PLL_CSI = 24MHz*N/M0/M1. PLL_CSI default is 432MHz.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1

			PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.13. PLL_DDR0 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PLL_DDR0_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1,this register is set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.14. PLL_DDR1 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PLL_DDR1_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1

			10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1,this register is set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.15. **PLL_PERI0 Pattern0 Control Register (Default Value: 0x0000_0000)**

Offset: 0x0120			**Register Name: PLL_PERI0_PAT0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1,this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.5.16. **PLL_PERI0 Pattern1 Control Register (Default Value:0x0000_0000)**

Offset: 0x0124			Register Name: PLL_PERI0_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

3.3.5.17. **PLL_PERI1 Pattern0 Control Register (Default Value: 0x0000_0000)**

Offset: 0x0128			Register Name: PLL_PERI1_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1,this register is set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.18. **PLL_PERI1 Pattern1 Control Register (Default Value: 0x0000_0000)**

Offset: 0x012C	Register Name: PLL_PERI1_PAT1_CTRL_REG

Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.19. **PLL_VIDEO0 Pattern0 Control Register (Default Value: 0x0000_0000)**

Offset: 0x0140			Register Name: PLL_VIDEO0_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.20. **PLL_VIDEO0 Pattern1 Control Register (Default Value: 0x0000_0000)**

Offset: 0x0144			Register Name: PLL_VIDEO0_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN

19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.21. **PLL_VE Pattern0 Control Register (Default Value: 0x0000_0000)**

Offset: 0x0158			Register Name: PLL_VE_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.22. **PLL_VE Pattern1 Control Register (Default Value: 0x0000_0000)**

Offset: 0x015C			Register Name: PLL_VE_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.23. PLL_DE Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PLL_DE_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.24. PLL_DE Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: PLL_DE_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.25. PLL_ISP Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: PLL_ISP_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN

			Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.26. PLL_ISP Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: PLL_ISP_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.27. PLL_AUDIO Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PLL_AUDIO_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1

			10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.28. **PLL_AUDIO Pattern1 Control Register (Default Value: 0x0000_0000)**

Offset: 0x017C			**Register Name: PLL_AUDIO_PAT1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.29. **PLL_ISE Pattern0 Control Register (Default Value: 0x0000_0000)**

Offset: 0x01D0			**Register Name: PLL_ISE_PAT0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL

			SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.30. **PLL_ISE Pattern1 Control Register (Default Value: 0x0000_0000)**

Offset: 0x01D4			**Register Name: PLL_ISE_PAT1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.31. **PLL_CSI Pattern0 Control Register (Default Value: 0x0000_0000)**

Offset: 0x01E0			**Register Name: PLL_CSI_PAT0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ.

			Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.5.32. **PLL_CSI Pattern1 Control Register (Default Value: 0x0000_0000)**

Offset: 0x01E4			**Register Name: PLL_CSI_PAT1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

3.3.5.33. **PLL_CPUX Bias Register (Default Value: 0x8010_0000)**

Offset: 0x0300			**Register Name: PLL_CPUX_BIAS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	VCO_RST VCO reset in
30:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CURRENT PLL current bias control [4:0], CPU_CP.
15:0	/	/	/

3.3.5.34. **PLL_DDR0 Bias Register (Default Value: 0x0003_0000)**

Offset: 0x0310			**Register Name: PLL_DDR0_BIAS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.35. **PLL_DDR1 Bias Register (Default Value: 0x0003_0000)**

Offset: 0x0318	**Register Name: PLL_DDR1_BIAS_REG**

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.36. **PLL_PERI0 Bias Register (Default Value: 0x0003_0000)**

Offset: 0x0320			Register Name: PLL_PERI0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.37. **PLL_PERI1 Bias Register (Default Value: 0x0003_0000)**

Offset: 0x0328			Register Name: PLL_PERI1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.38. **PLL_VIDEO0 Bias Register (Default Value: 0x0003_0000)**

Offset: 0x0340			Register Name: PLL_VIDEO0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.39. **PLL_VE Bias Register (Default Value: 0x0003_0000)**

Offset: 0x0358			Register Name: PLL_VE_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.40. **PLL_DE Bias Register (Default Value: 0x0003_0000)**

Offset: 0x0360			Register Name: PLL_DE_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.41. **PLL_ISP Bias Register (Default Value: 0x0003_0000)**

Offset: 0x0368			Register Name: PLL_ISP_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.42. **PLL_AUDIO Bias Register (Default Value: 0x0003_0000)**

Offset: 0x0378			Register Name: PLL_AUDIO_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.43. **PLL_ISE Bias Register (Default Value: 0x0003_0000)**

Offset: 0x03D0			Register Name: PLL_ISE_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.44. **PLL_CSI Bias Register (Default Value: 0x0003_0000)**

Offset: 0x03E0			Register Name: PLL_CSI_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL.

			PLL bias control [4:0].
15:0	/	/	/

3.3.5.45. **PLL_CPUX Tuning Register (Default Value: 0x4440_4000)**

Offset: 0x0400			Register Name: PLL_CPUX_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x4	VCO_RNG_CTRL VCO range control [2:0]
27	/	/	/
26:24	R/W	0x4	KVCO_GAIN_CTRL KVCO gain control [2:0]
23	/	/	/
22:16	R/W	0x40	CNT_INIT_CTRL Counter initial control [6:0]
15	R/W	0x0	C_OD0 C-REG-OD0 for verify
14:8	R/W	0x40	C_B_IN C-B-IN [6:0] for verify
7	R/W	0x0	C_OD1 C-REG-OD1 for verify
6:0	R	0x0	C_B_OUT C-B-OUT [6:0] for verify

3.3.5.46. **CPUX_AXI Configuration Register (Default Value: 0x0000_0301)**

Offset: 0x0500			Register Name: CPUX_AXI_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: RTC_32K 10: RC16M 11: PLL_C0_CPUX C0_CPUX Clock = Clock Source C0_CPUX_AXI Clock = Clock Source/M C0_CPUX_APB Clock = Clock Source/N
23:10	/	/	/
9:8	R/W	0x3	CPUX _APB_FACTOR_N Factor N (N = FACTOR_N +1) The range of N is from 1 to 4.
7:2	/	/	/

1:0	R/W	0x1	FACTOR_M Factor M (M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.47. **PSI_AHB1_AHB2 Configuration Register (Default Value: 0x0000_0000)**

Offset: 0x0510			**Register Name: PSI_AHB1_AHB2_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: RTC_32K 10: RC16M 11: PLL_PERI0(1X) PSI_AHB1_AHB2 CLK = Clock Source/M/N
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.48. **AHB3 Configuration Register (Default Value: 0x0000_0000)**

Offset: 0x051C			**Register Name: AHB3_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: RTC_32K 10: PSI 11: PLL_PERI0(1X) AHB3 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1

			01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.49. **APB1 Configuration Register (Default Value: 0x0000_0000)**

Offset: 0x520			**Register Name: APB1_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: RTC_32K 10: PSI 11: PLL_PERI0(1X) APB1 CLK = Clock Source/M/N
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.50. **APB2 Configuration Register (Default Value: 0x0000_0000)**

Offset: 0x524			**Register Name: APB2_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: RTC_32K 10: PSI 11: PLL_PERI0(1X) APB2 CLK = Clock Source/M/N.

23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.51. **MBUS Configuration Register (Default Value: 0xC000_0000)**

Offset: 0x540			**Register Name: MBUS_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON MBUS CLK = Clock Source/M.
30	R/W	0x1	MBUS_RST MBUS Reset 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERI0(2X) 10: PLL_DDR0 11: PLL_DDR1
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 8.

3.3.5.52. **DE Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0600			**Register Name: DE_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF

			1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_DE 1: PLL_PERI0(2X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.53. **DE Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x060C			**Register Name: DE_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DE_RST DE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DE_GATING Gating Clock For DE 0: Mask 1: Pass

3.3.5.54. **G2D Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0630			**Register Name: G2D_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_DE 1: PLL_PERI0(2X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1)

			The range of M is from 1 to 16.

3.3.5.55. **G2D Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x063C			Register Name: G2D_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	G2D_RST G2D Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	G2D_GATING Gating Clock For G2D 0: Mask 1: Pass

3.3.5.56. **CE Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0680			Register Name: CE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: OSC24M 1: PLL_PERI0(2X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.57. **CE Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x068C			Register Name: CE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CE_RST CE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CE_GATING Gating Clock For CE 0: Mask 1: Pass

3.3.5.58. **VE Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0690			Register Name: VE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/Divider M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_VE 1: /
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 8.

3.3.5.59. **VE Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x069C			Register Name: VE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	VE_RST VE Reset 0: Assert 1: De-assert
15:1	/	/	/

0	R/W	0x0	VE_GATING Gating Clock For VE 0: Mask 1: Pass

3.3.5.60. ISE Clock Register (Default Value: 0x0000_0000)

Offset: 0x06A0			Register Name: ISE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_ISE Others: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.61. ISE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x06AC			Register Name: ISE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	ISE_RST ISE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	ISE_GATING Gating Clock For ISE 0: Mask 1: Pass

3.3.5.62. EISE Clock Register (Default Value: 0x0000_0000)

Offset: 0x06D0			Register Name: EISE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_ISE 01: / 10: / 11:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.63. **EISE Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x06DC			**Register Name: EISE_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EISE_RST. EISE Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EISE_GATING. Gating Clock For EISE 0: Mask 1: Pass

3.3.5.64. **DMA Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x070C			**Register Name: DMA_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMA_RST DMA Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMA_GATING Gating Clock For DMA

			0: Mask 1: Pass

3.3.5.65. **MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x071C			Register Name: MSGBOX_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MSGBOX_RST MSGBOX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MSGBOX_GATING Gating Clock For MSGBOX 0: Mask 1: Pass

3.3.5.66. **SPINLOCK Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	SPINLOCK_RST SPINLOCK Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPINLOCK_GATING Gating Clock For SPINLOCK 0: Mask 1: Pass

3.3.5.67. **HSTIMER Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x073C			Register Name: HSTIMER_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HSTIMER_RST HSTIMER Reset 0: Assert 1: De-assert
15:1	/	/	/

0	R/W	0x0	HSTIMER_GATING Gating Clock For HSTIMER 0: Mask 1: Pass

3.3.5.68. **AVS Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0740			Register Name: AVS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = OSC24M.
30:0	/	/	/

3.3.5.69. **DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST DBGSYS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DBGSYS_GATING Gating Clock For DBGSYS 0: Mask 1: Pass

3.3.5.70. **PSI Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x079C			Register Name: PSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PSI_RST PSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PSI_GATING Gating Clock For PSI

			0: Mask 1: Pass

3.3.5.71. **PWM Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x07AC			Register Name: PWM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PWM_RST PWM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PWM_GATING Gating Clock For PWM 0: Mask 1: Pass

3.3.5.72. **DRAM Clock Register (Default Value: 0x0100_0000)**

Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	MODULE_RST Module Reset 0: Assert 1: De-assert SCLK = Clock Source/M.
29:26	/	/	/
25:24	R/W	0x1	CLK_SRC_SEL Clock Source Select 00: PLL_DDR0 01: PLL_DDR1 Others: /
23:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.73. **MBUS Master Clock Gating Register (Default Value: 0x0000_0000)**

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:23	/	/	/
22	R/W	0x0	CVE_MCLK_GATING Gating MBUS Clock For CVE 0: Mask 1: Pass
21	/	/	/
20:14	/	/	/
13	R/W	0x0	ISE_MCLK_GATING Gating MBUS Clock For ISE 0: Mask 1: Pass
12	/	/	/
11	R/W	0x0	DI_MCLK_GATING Gating MBUS Clock For DI 0: Mask 1: Pass
10	R/W	0x0	G2D_MCLK_GATING Gating MBUS Clock For G2D 0: Mask 1: Pass
9	R/W	0x0	ISP0_MCLK_GATING Gating MBUS Clock For ISP0 0: Mask 1: Pass
8	R/W	0x0	CSI_MCLK_GATING Gating MBUS Clock For CSI 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	NAND0_MCLK_GATING Gating MBUS Clock For NAND0 0: Mask 1: Pass
4:3	/	/	/
2	R/W	0x0	CE_MCLK_GATING Gating MBUS Clock For CE 0: Mask 1: Pass
1	R/W	0x0	VE_MCLK_GATING Gating MBUS Clock For VE 0: Mask 1: Pass
0	R/W	0x0	DMA_MCLK_GATING Gating MBUS Clock For DMA 0: Mask 1: Pass

NOTE

DE MCLK puts in DE module.

3.3.5.74. **DRAM Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DRAM_RST DRAM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DRAM_GATING Gating Clock For DRAM 0: Mask 1: Pass

3.3.5.75. **NAND0_0 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0810			Register Name: NAND0_0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8

7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.76. **NAND0_1 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0814			**Register Name: NAND0_1_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.77. **NAND Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x082C			**Register Name: NAND_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	NAND0_RST NAND0 Reset 0: Assert 1: De-assert

15:1	/	/	/
0	R/W	0x0	NAND0_GATING Gating Clock For NAND0 0: Mask 1: Pass

3.3.5.78. **SMHC0 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0830			**Register Name: SMHC0_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.79. **SMHC1 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0834			**Register Name: SMHC1_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/

25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16

3.3.5.80. **SMHC2 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0838			**Register Name: SMHC2_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.81. **SMHC Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	SMHC2_RST SMHC2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SMHC1_RST SMHC1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SMHC0_RST SMHC0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SMHC2_GATING Gating Clock For SMHC2 0: Mask 1: Pass
1	R/W	0x0	SMHC1_GATING Gating Clock For SMHC1 0: Mask 1: Pass
0	R/W	0x0	SMHC0_GATING Gating Clock For SMHC0 0: Mask 1: Pass

3.3.5.82. **UART Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20	R/W	0x0	UART4_RST UART4 Reset 0: Assert 1: De-assert
19	R/W	0x0	UART3_RST UART3 Reset 0: Assert

			1: De-assert
18	R/W	0x0	UART2_RST UART2 Reset 0: Assert 1: De-assert
17	R/W	0x0	UART1_RST UART1 Reset 0: Assert 1: De-assert
16	R/W	0x0	UART0_RST UART0 Reset 0: Assert 1: De-assert
15:5	/	/	/
4	R/W	0x0	UART4_GATING Gating Clock For UART4 0: Mask 1: Pass
3	R/W	0x0	UART3_GATING Gating Clock For UART3 0: Mask 1: Pass
2	R/W	0x0	UART2_GATING Gating Clock For UART2 0: Mask 1: Pass
1	R/W	0x0	UART1_GATING Gating Clock For UART1 0: Mask 1: Pass
0	R/W	0x0	UART0_GATING Gating Clock For UART0 0: Mask 1: Pass

3.3.5.83. **TWI Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x091C			**Register Name: TWI_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TWI3_RST TWI3 Reset 0: Assert 1: De-assert
18	R/W	0x0	TWI2_RST

			TWI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	TWI1_RST TWI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	TWI0_RST TWI0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	TWI3_GATING Gating Clock For TWI3 0: Mask 1: Pass
2	R/W	0x0	TWI2_GATING Gating Clock For TWI2 0: Mask 1: Pass
1	R/W	0x0	TWI1_GATING Gating Clock For TWI1 0: Mask 1: Pass
0	R/W	0x0	TWI0_GATING Gating Clock For TWI0 0: Mask 1: Pass

3.3.5.84. **SPI0 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0940			**Register Name: SPI0_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X)

			100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.85. **SPI1 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0944			**Register Name: SPI1_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.86. **SPI2 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0948			Register Name: SPI2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.87. **SPI3 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x094C			Register Name: SPI3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X)

			011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.88. **SPI Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x096C			**Register Name: SPI_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	SPI3_RST SPI3 Reset 0: Assert 1: De-assert
18	R/W	0x0	SPI2_RST SPI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SPI1_RST SPI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SPI0_RST SPI0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	SPI3_GATING Gating Clock For SPI3 0: Mask 1: Pass
2	R/W	0x0	SPI2_GATING Gating Clock For SPI2 0: Mask 1: Pass

1	R/W	0x0	SPI1_GATING Gating Clock For SPI1 0: Mask 1: Pass
0	R/W	0x0	SPI0_GATING Gating Clock For SPI0 0: Mask 1: Pass

3.3.5.89. EPHY_25M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0970			Register Name: EPHY_25M_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = PLL_PERI0(1X)/24 = 25M.
30:0	/	/	/

3.3.5.90. EMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x097C			Register Name: EMAC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EMAC_RST EMAC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EMAC_GATING Gating Clock For EMAC 0: Mask 1: Pass

3.3.5.91. GPADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	GPADC_RST GPADC Reset 0: Assert

			1: De-assert
15:1	/	/	/
0	R/W	0x0	GPADC_GATING Gating Clock For GPADC 0: Mask 1: Pass

3.3.5.92. **THS Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x09FC			**Register Name: THS_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	THS_RST THS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	THS_GATING Gating Clock For THS 0: Mask 1: Pass

3.3.5.93. **I2S/PCM0 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0A10			**Register Name: I2S/PCM0_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4

			11: 8
7:0	/	/	/

3.3.5.94. **I2S/PCM1 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0A14			Register Name: I2S/PCM1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.95. **I2S/PCM2 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0A18			Register Name: I2S/PCM2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /

23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.96. **I2S/PCM Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0A1C			**Register Name: I2S/PCM_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	I2S/PCM2_RST I2S/PCM2 Reset 0: Assert 1: De-assert
17	R/W	0x0	I2S/PCM1_RST I2S/PCM1 Reset 0: Assert 1: De-assert
16	R/W	0x0	I2S/PCM0_RST I2S/PCM0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	I2S/PCM2_GATING Gating Clock For I2S/PCM2 0: Mask 1: Pass
1	R/W	0x0	I2S/PCM1_GATING Gating Clock For I2S/PCM1 0: Mask 1: Pass
0	R/W	0x0	I2S/PCM0_GATING Gating Clock For I2S/PCM0 0: Mask 1: Pass

3.3.5.97. **DMIC Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0A40			**Register Name: DMIC_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.98. DMIC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A4C			Register Name: DMIC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMIC_RST DMIC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMIC_GATING Gating Clock For DMIC 0: Mask 1: Pass

3.3.5.99. AUDIO CODEC 1X Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A50			Register Name: AUDIO_CODEC_1X_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON

			SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The factor of M is from 1 to 16.

3.3.5.100. **AUDIO CODEC 4X Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0A54			**Register Name: AUDIO_CODEC_4X_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The factor of M is from 1 to 16.

3.3.5.101. **AUDIO CODEC Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0A5C			**Register Name: AUDIO_CODEC_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	AUDIO_CODEC _RST AUDIO_CODEC Reset 0: Assert 1: De-assert
15:1	/	/	/

0	R/W	0x0	AUDIO_CODEC _GATING Gating Clock For AUDIO_CODEC 0: Mask 1: Pass

3.3.5.102. **USB2.0_OTG Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0A70			**Register Name: USB2.0_OTG_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING_USB2.0_OTG_OHCI Gating Special Clock For USB2.0_OTG_OHCI 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USB2.0_OTG_PHY_RST USB2.0_OTG PHY Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USB2.0_OTG_PHY Gating Special Clock For USB2.0_OTG PHY 0: Clock is OFF 1: Clock is ON SCLK is from OSC24M
28:26	/	/	/
25:24	R/W	0x0	USB2.0_OTG_OHCI_12M_SRC_SEL USB2.0_OTG_OHCI 12M Source Select 00: 12MHz divided from 48MHz 01: 12MHz divided from 24MHz 10: LOSC 11: /
23:0	/	/	/

3.3.5.103. **USB Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0A8C			**Register Name: USB_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	USB2.0_OTG_RST USB2.0_OTG Reset 0: Assert 1: De-assert
23:21	/	/	/
20	R/W	0x0	USB2.0_OTG_EHCI_RST USB2.0_OTG_EHCI Reset 0: Assert

			1: De-assert
19:17	/	/	/
16	R/W	0x0	USB2.0_OTG_OHCI_RST USB2.0_OTG_OHCI Reset 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x0	USB2.0_OTG_GATING Gating Clock For USB2.0_OTG 0: Mask 1: Pass
7:5	/	/	/
4	R/W	0x0	USB2.0_OTG_EHCI_GATING Gating Clock For USB2.0_OTG_EHCI 0: Mask 1: Pass
3:1	/	/	/
0	R/W	0x0	USB2.0_OTG_OHCI_GATING Gating Clock For USB2.0_OTG_OHCI 0: Mask 1: Pass

3.3.5.104. **HDMI Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0B00			**Register Name: HDMI_HS_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_VIDEO0(1X) 01: PLL_VIDEO0(4X) 10: / 11: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.105. **HDMI Slow Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0B04			Register Name: HDMI_SLOW_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = OSC24M.
30:0	/	/	/

3.3.5.106. **HDMI CEC Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0B10			Register Name: HDMI_CEC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: CCU_32K 01: PLL_PERI0(2X)/36621 = 32.768kHz 1X:/
23:0	/	/	/

3.3.5.107. **HDMI Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0B1C			Register Name: HDMI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	HDMI_SUB_RST HDMI_SUB Reset 0: Assert 1: De-assert
16	R/W	0x0	HDMI_MAIN_RST HDMI_MAIN Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HDMI_GATING Gating Clock For HDMI 0: Mask

			1: Pass

3.3.5.108. **MIPI DSI DPHY High Speed Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0B20			Register Name: MIPI_DSI_DPHY_HS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_VIDEO0(1X) 01: PLL_VIDEO0(4X) 10:/ 11:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.109. **MIPI DSI Host Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0B24			Register Name: MIPI_DSI_HOST_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_PERI0(1X) 01: PLL_PERI0(2X)

			10: OSC24M 11:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.110. **MIPI DSI Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0B4C			**Register Name: MIPI_DSI_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MIPI_DSI_RST MIPI_DSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MIPI_DSI_GATING Gating Clock For MIPI_DSI 0: Mask 1: Pass

3.3.5.111. **DISPLAY_IF_TOP Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0B5C			**Register Name: DISPLAY_IF_TOP_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DISPLAY_IF_TOP_RST DISPLAY_IF_TOP Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DISPLAY_IF_TOP_GATING Gating Clock For DISPLAY_IF_TOP 0: Mask 1: Pass

3.3.5.112. **TCON LCD0 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0B60			**Register Name: TCON_LCD0_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock

			0: Clock is OFF 1: Clock is ON SCLK = Clock Source
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(4X) Others:/
23:0	/	/	/

3.3.5.113. **TCON LCD Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0B7C			**Register Name: TCON_LCD_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TCON_LCD0_RST TCON_LCD0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TCON_LCD0_GATING Gating Clock For TCON_LCD0 0: Mask 1: Pass

3.3.5.114. **TCON TV0 Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0B80			**Register Name: TCON_TV0_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(4X) Others:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N

			00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The value of M is from 1 to 16.

3.3.5.115. **TCON TV Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0B9C			**Register Name: TCON_TV_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TCON_TV0_RST TCON_TV0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TCON_TV0_GATING Gating Clock For TCON_TV0 0: Mask 1: Pass

3.3.5.116. **TVE Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0BB0			**Register Name: TVE_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(4X) 010: / 011: / 100: / 101: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N

			Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The value of M is from 1 to 16.

3.3.5.117. **TVE Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0BBC			**Register Name: TVE_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	TVE_RST TVE Reset 0: Assert 1: De-assert
16	R/W	0x0	TVE_TOP_RST TVE_TOP Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	TVE_GATING Gating Clock For TVE 0: Mask 1: Pass
0	R/W	0x0	TVE_TOP_GATING Gating Clock For TVE_TOP 0: Mask 1: Pass

3.3.5.118. **CSI MISC Clock Register (Default: 0x0000_0000)**

Offset: 0x0C00			**Register Name: CSI_MISC_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
1	R/W	0x0	CSI_CCI1_CLK_GATING Gating CCI1 Special Clock,Clock source is OSC24M 0: Clock is OFF 1: Clock is ON
0	R/W	0x0	CSI_CCI0_CLK_GATING Gating CCI0 Special Clock,Clock source is OSC24M

			0: Clock is OFF 1: Clock is ON

3.3.5.119. **CSI TOP Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0C04			Register Name: CSI_TOP_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:PLL_VIDEO0(1X) 001:PLL_ISP 010:PLL_VE 011:PLL_PERI0(1X) 100: PLL_CSI Others:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.120. **CSI Master Clock0 Register (Default Value: 0x0000_0000)**

Offset: 0x0C08			Register Name: CSI_MST_CLK0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK0_GATING Gating CSI Master Clock0 This clock output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_VIDEO0(1X) 010: PLL_PERI0(2X) 011: PLL_PERI1(1X) 100: PLL_ISP

			101: PLL_CSI Others:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 32.

3.3.5.121. **CSI Master Clock1 Register (Default Value: 0x0000_0000)**

Offset: 0x0C0C			**Register Name: CSI_MST_CLK1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK1_GATING Gating CSI Master Clock1 This clock output to external device. 0: Clock is OFF 1: Clock is ON MCLK1 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_VIDEO0(1X) 010: PLL_PERI0(2X) 011: PLL_PERI1(1X) 100: PLL_ISP 101: PLL_CSI Others:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 32.

3.3.5.122. **ISP Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0C20			**Register Name: ISP_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select

			00: PLL_ISP 01: PLL_PERI(1X) 10: PLL_VIDEO0(1X) 11:
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.123. **CSI Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0C2C			Register Name: CSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CSI_RST CSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CSI_GATING Gating Clock For CSI 0: Mask 1: Pass

3.3.5.124. **VDPO Clock Register (Default Value: 0x0000_0000)**

Offset: 0x0C50			Register Name: VDPO_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(4X) 010: / 011: / 100: / 101: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N

			Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 0 to 15

3.3.5.125. **VDPO Bus Gating Reset Register (Default Value: 0x0000_0000)**

Offset: 0x0C5C			**Register Name: VDPO_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
16	R/W	0x0	VDPO_RST VDPO Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	VDPO_GATING Gating Clock For VDPO 0: Mask 1: Pass

3.3.5.126. **PLL Lock Debug Control Register (Default Value: 0x0000_0000)**

Offset: 0x0F04			**Register Name: PLL_LOCK_DBG_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DBG_EN Debug Enable 0: Disable 1: Enable
30:25	/	/	/
24:20	R/W	0x0	DBG_SEL Debug Select 00000: PLL_C0_CPUX 00001: / 00010: PLL_DDR0 00011:PLL_DDR1 00100: PLL_PERI0(2X) 00101: PLL_PERI1(2X) 00110:/ 00111:/

			01000: PLL_VIDEO0(4X) 01001: / 01010: / 01011: PLL_VE 01100: PLL_DE 01101: PLL_ISP 01110: / 01111: PLL_AUDIO 10000: / 10001: / 10010: / 10011: / 10100: / 10101: / 10110: / 10111: / 11000: / 11001: / 11010: PLL_ISE 11011: / Others: /
19	/	/	/
18:17	R/W	0x0	UNLOCK_LEVEL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
16	R/W	0x0	LOCK_LEVEL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
15:0	/	/	/

3.4. Boot System

3.4.1. Overview

The V536-H/V526 system has several ways to boot. It has an integrated on-chip Boot ROM (BROM) which could be considered the primary program-loader. On startup, the V536-H/V526 starts to fetch the first instruction from address 0x0, where is the BROM located at.
The Boot system is split up into two parts :FEL and Media Boot. The task of FEL is to write the external data to the local NVM,the task of the Media Boot is to load an effective and legitimate BOOT0 from NVM and run.

The Boot system includes the following features:

- CPU0 boot process and NON_CPU0 boot process
- Super standby wakeup process
- Hotplug process
- Mandatory upgrade process through SMHC0,USB and UART
- GPIO pin or eFuse is used to select the kind of boot media to boot
- Loads only certified firmware

3.4.2. Operations and Functional Descriptions

3.4.2.1. Boot Select Description

The BROM system supports the following boot media:

- SD/MMC
- NAND FLASH
- SPI NOR FLASH
- SPI NAND FLASH

There are two ways of boot select: GPIO pin select and eFuse select. The BROM will read the state of BOOT_MODE , according to the state of BOOT_MODE to decide whether GPIO pin or eFuse to select the kind of boot media to boot. The BOOT_MODE is actually a bit in the SID. Table 3-4 shows BOOT_MODE setting.

Table 3-4.BOOT_MODE Setting

BOOT_MODE[0]	Boot Select Type
0	GPIO pin select
1	eFuse select

If the state of the BOOT_MODE is 0,that is to choose the GPIO pin ,which has multi-pins to select boot media to boot.Table 3-5 shows boot select setting of GPIO pin.

Table 3-5. GPIO Pin Boot Select Setting

Pin_Boot_Select[14:10]	Boot media
01111	SMHC0->SPI_NAND
10111	SMHC0->SPI_NOR

11011	SMHC0->EMMC_BOOT->EMMC_USER
11101	SMHC0->EMMC_USER->EMMC_BOOT
11110	SMHC0->SLC_NAND->MLC_NAND
11111	SMHC0->MLC_NAND->SLC_NAND

If the state of the BOOT_MODE is 1,that is to choose the eFuse .eFuse select has 12 bits,so each of the 3 bits is divided into a group of the Boot Select ,so it has four groups of boot_select .Table 3-6 shows eFuse Boot Select Configure.

Table 3-6. eFuse Boot Select Configure

eFuse_Boot_Select_Cfg[11:0]	Description
eFuse_Boot_Select[2:0]	eFuse_Boot_Select_1
eFuse_Boot_Select[5:3]	eFuse_Boot_Select_2
eFuse_Boot_Select[8:6]	eFuse_Boot_Select_3
eFuse_Boot_Select[11:9]	eFuse_Boot_Select_4

Table 3-7 describes each group of the eFuse Boot select settings. The first group to the third group are the same settings,but the fourth group need to be careful.If eFuse_Boot_Select_4 is set to 111,that means the way of the *Try*.The way of *Try* is followed by SMHC0->SPI NOR->SMHC2->SPI NAND->NAND FLASH.

Table 3-7. eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot media
000	Try
001	SMHC0->SLC_NAND->MLC_NAND
010	SMHC0->EMMC_USER->EMMC_BOOT
011	SMHC0->SPI_NOR
100	SMHC0->SPI_NAND
101	SMHC0->MLC_NAND->SLC_NAND
110	SMHC0->EMMC_BOOT->EMMC_USER
111	The next a group of the eFuse_Boot_Select. But when the n is equal to 4,it will be a way of Try.

3.4.2.2. **BROM System Description**

3.4.2.2.1. BROM Process

In Normal boot mode,the system boot will start from CPU0 or NON_CPU0, BROM will read CPU ID number to distinguish CPU0 or NON_CPU0,then BROM will read the **Hotplug Flag Regsiter** and the **Supper Standby Flag Regsiter** ,according to the flag whether to go through the appropriate process.Finally,BROM will read the state of the FEL Pin,if the FEL Pin signal is detected to pull to high level, then the system will jump to the Try Media Boot process,or jump to the mandatory upgrade process. Figure 3-5 shows the Normal BROM Process.

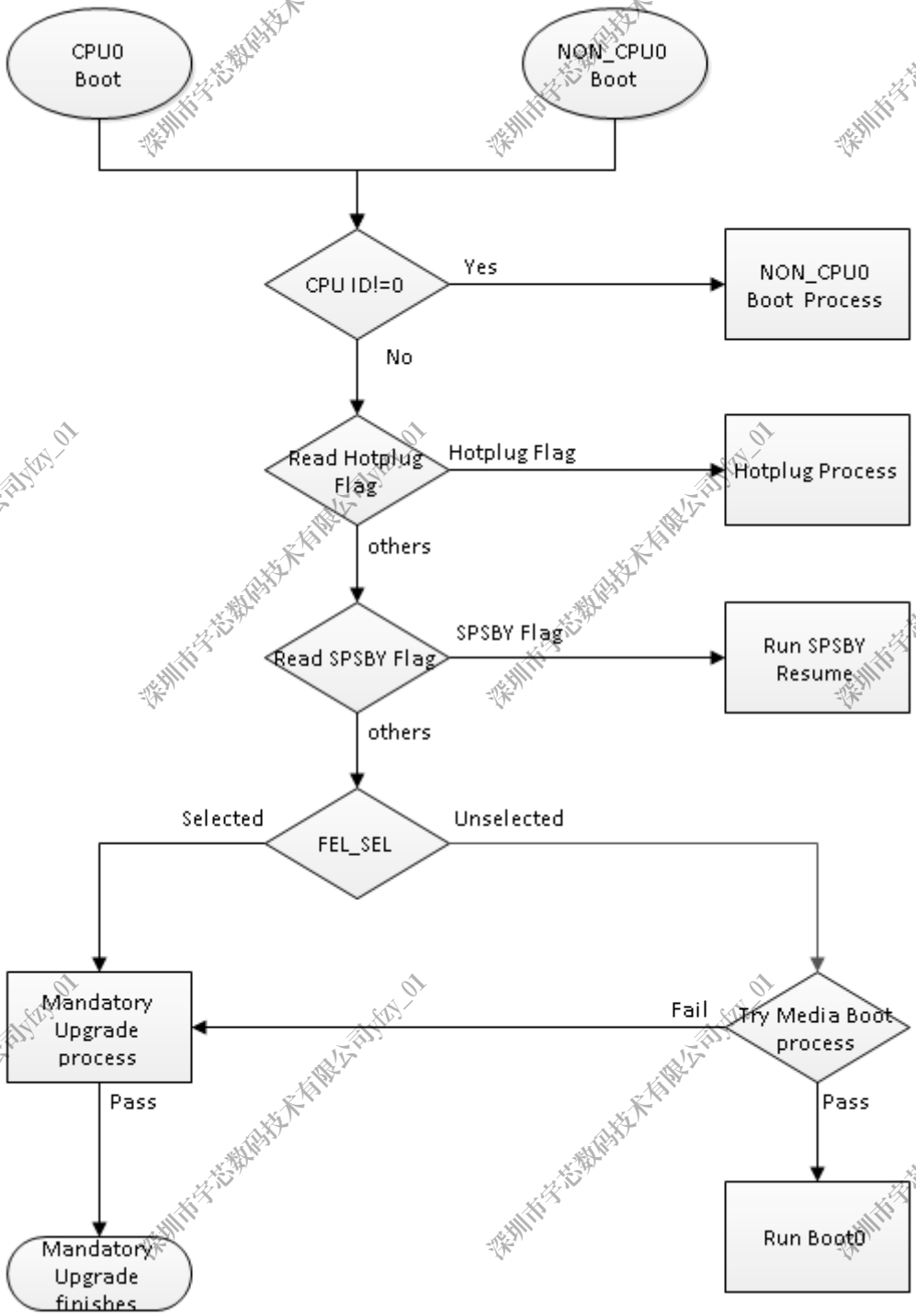


Figure 3-5. Normal Mode Boot Process

3.4.2.2.2. NON_CPU0 Boot Process

If CPU ID is greater than 0,the system boot from boot from NON_CPU0,BROM will read the Soft Entry Address Register,then jump the Soft Entry Address,and run NON_CPU0 boot code. Figure 3-6 shows the NON_CPU0 Boot Process.

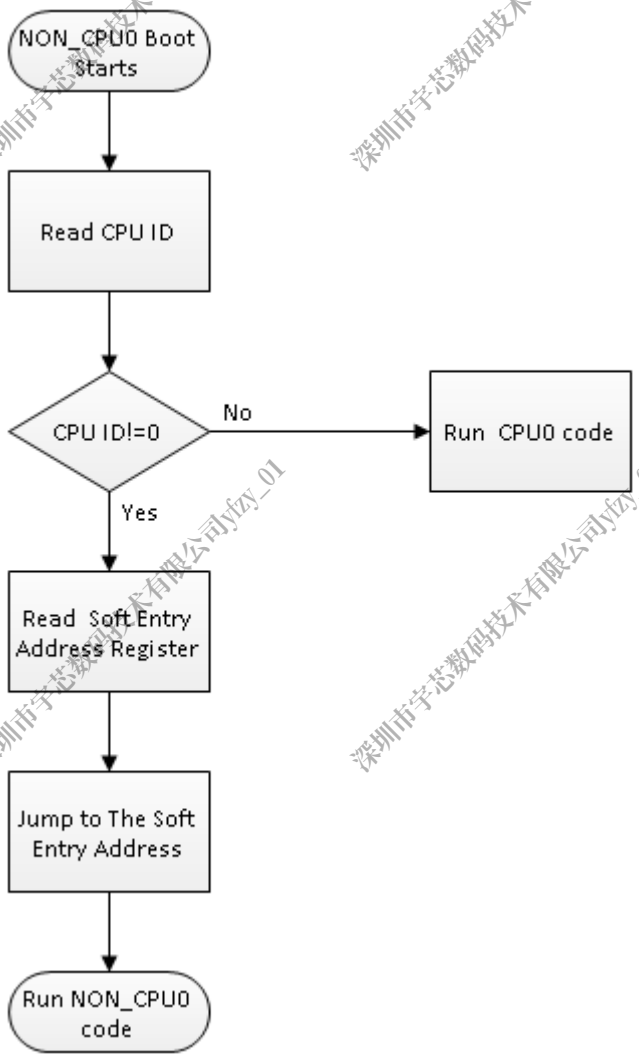


Figure 3-6. NON_CPU0 Boot Process

NOTE

The Soft Entry Address Register is 0x070005C8.

3.4.2.3. **CPU0 Hot Plug Process**

The Hot Plug flag determines whether the system will do hotplug boot. If CPU Hotplug Flag value is equal to 0×FA50392F, then read the Soft Entry Register and the system will jump to the Soft Entry Address. Figure 3-7 shows the CPU0 Hotplug Process.

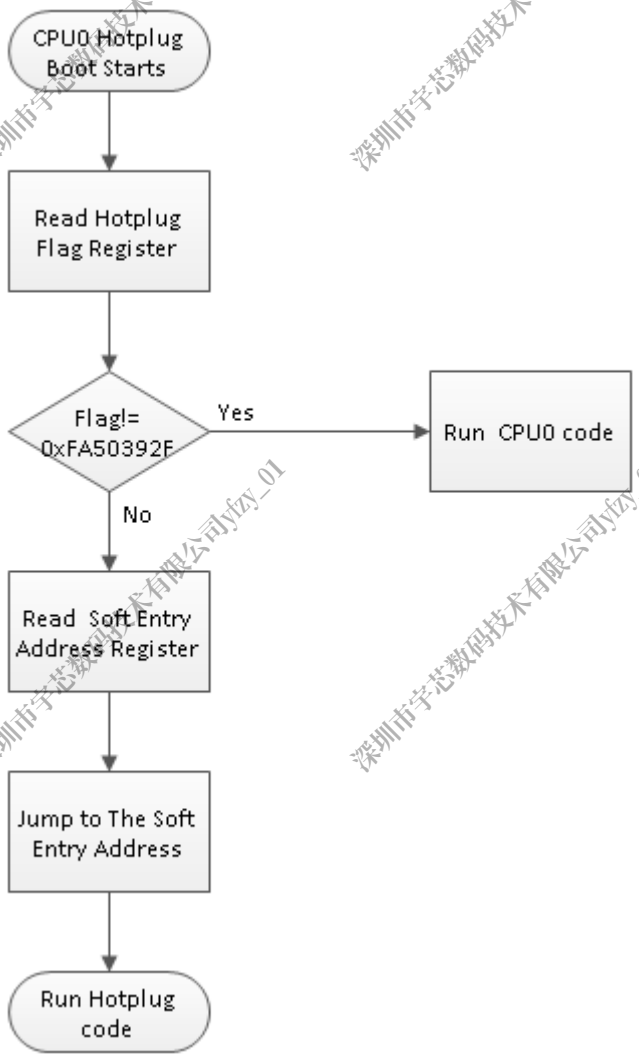


Figure 3-7. CPU0 Hot Plug Process

NOTE

The Hotplug Flag Register is 0x070005C0. The Soft Entry Address Register is 0x070005C4.

3.4.2.4. Super Standby Wakeup Process

Super Standby(SPSBY) wakeup will be started by CPUs, and will be carried on by CPU0 after the CPU0 released. If the SPSBY register value is checked to be the SPSBY flag, then the system will go to SPSBY wakeup process.Figure 3-8 shows the SPSBY Wakeup Process.

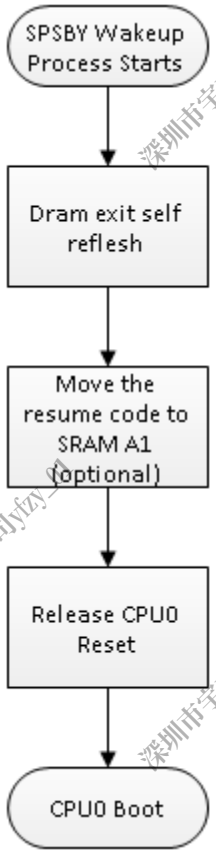


Figure 3-8. SPSBY Wakeup Process

During the SPSBY wakeup, the system will first check the SPSBY resume code pointed by SPSBY resume code pointer.If it is right, then the system will run SPSBY wakeup, otherwise the system will jump to the Try Media Boot process. Figure3-9 shows the SPSBY Resume Code Process.

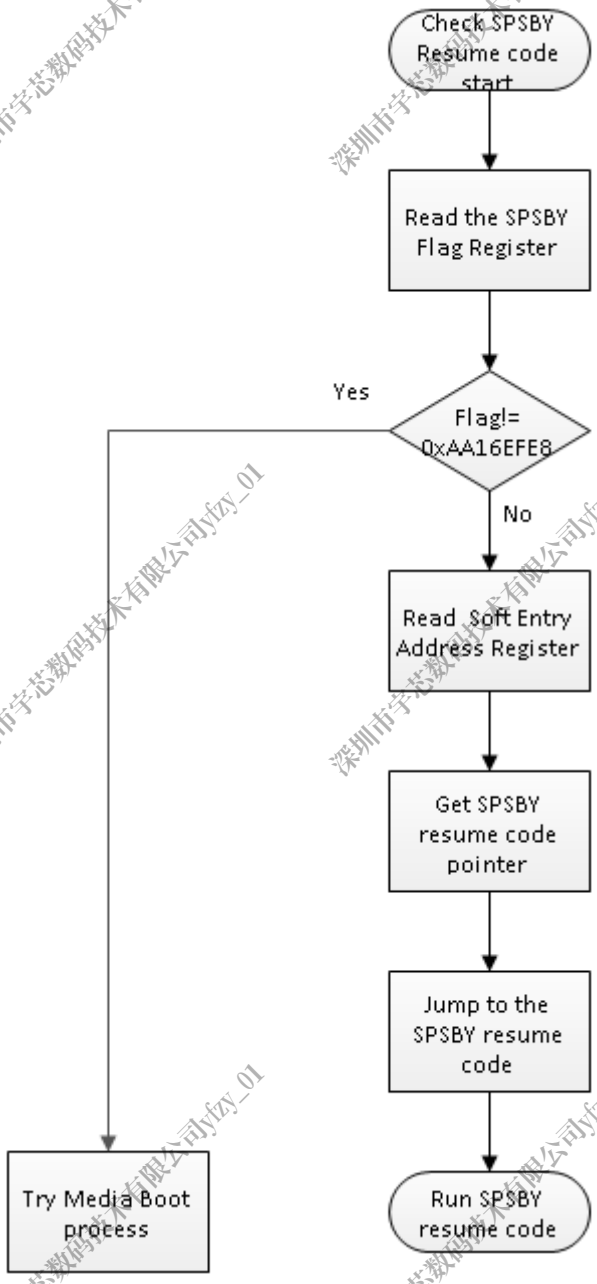


Figure 3-9. SPSBY Resume Code Check Process

3.4.2.5. **Mandatory Upgrade Process**

If the FEL Pin signal is detected to pull low, then the system will jump to mandatory upgrade process. And the process will read the boot_select2 pin, when the pin signal is detected to pull to high level, the system will enter the USB upgrade process,or enter the UART upgrade process. Figure 3-10 shows the mandatory upgrade process.

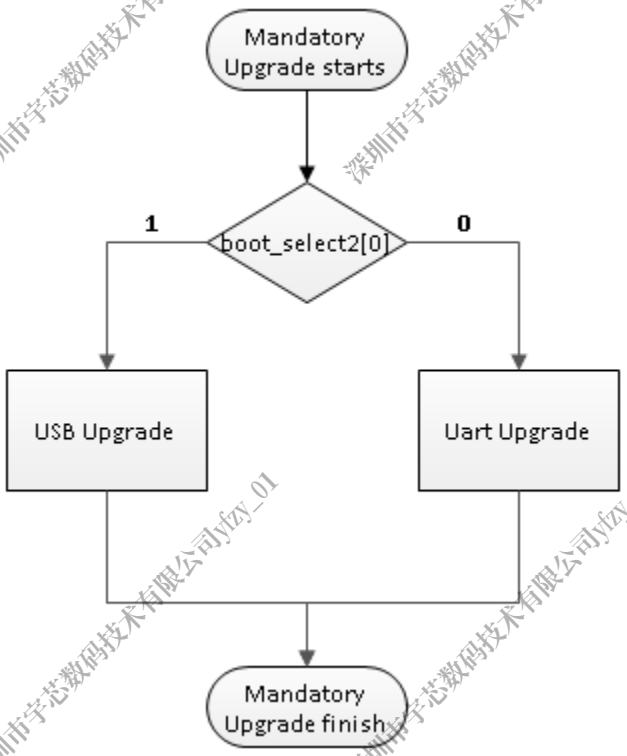


Figure 3-10. Mandatory Upgrade Process

NOTE

The FEL address of the BROM is 0x20.

3.4.2.6. **FEL Process**

When the system chooses to enter Mandatory Upgrade Process, if the boot_select2 pin signal is detected to pull to high level,then the system will jump to the FEL process.Figure 3-11 shows the FEL upgrade process.

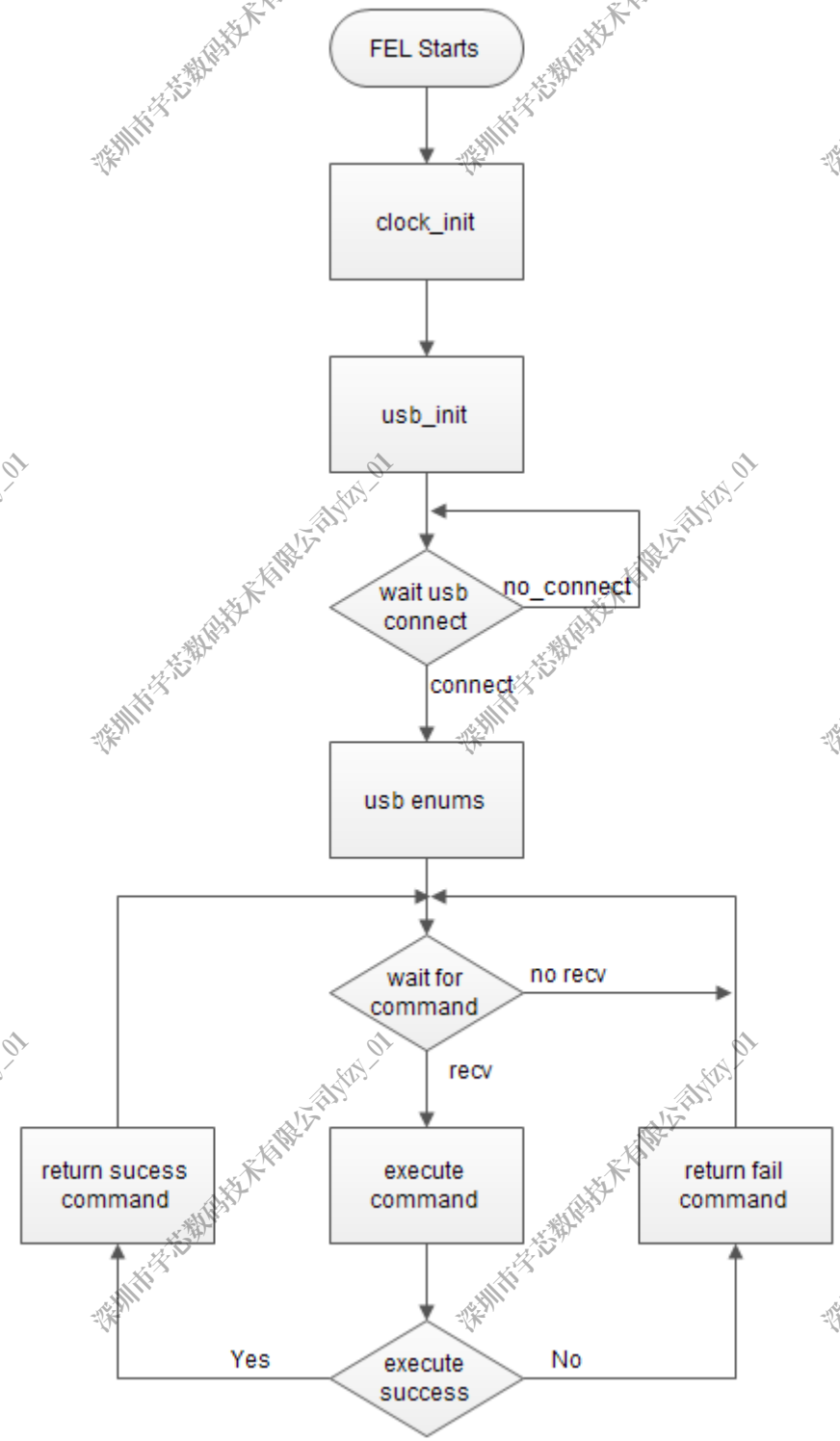


Figure 3-11. USB FEL Process

3.4.2.7. **UART Upgrade Process**

When the system chooses to enter Mandatory Upgrade Process, if the boot_select2 pin signal is detected to pull to low level,then the system will jump to the UART upgrade process.Figure 3-12 shows the UART upgrade process.

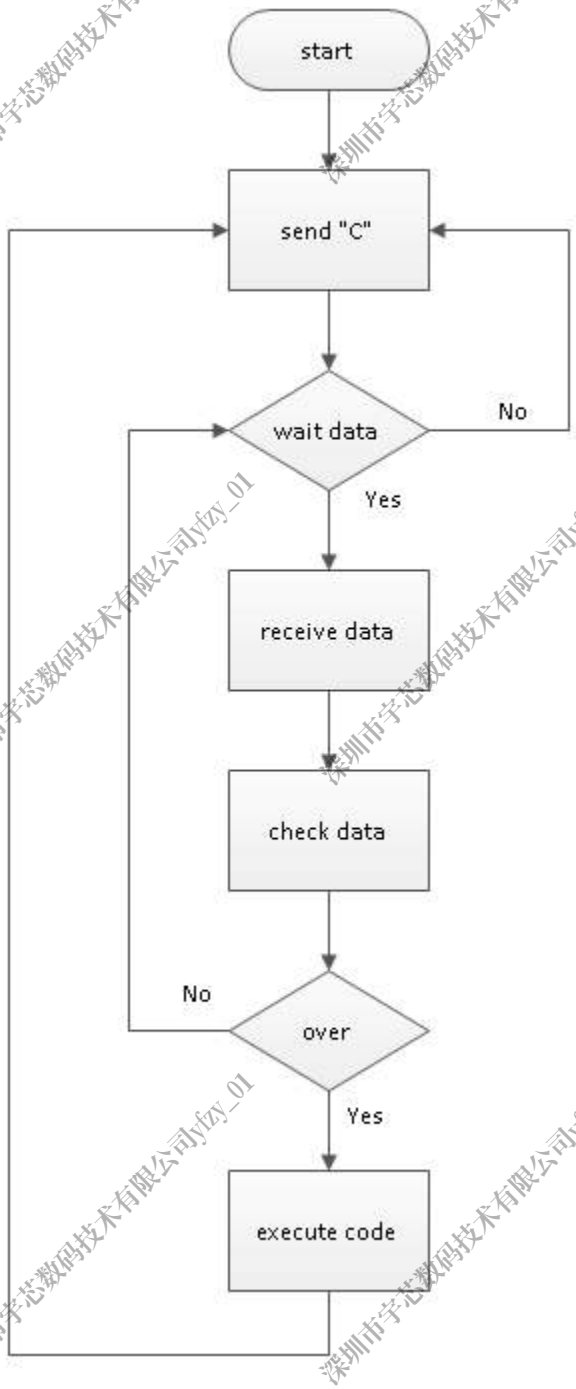


Figure 3-12. UART FEL Process

3.4.2.8. **Try Media Boot Process**

If the FEL Pin signal is detected to pull to high level, then the system will jump to the Try Media Boot process.

Try Media Boot Process will read the state of BOOT_MODE register,according to the state of BOOT_MODE, GPIO pin or efuse is descided to select boot media.Figure 3-13 shows BROM GPIO Pin Boot Select Process.

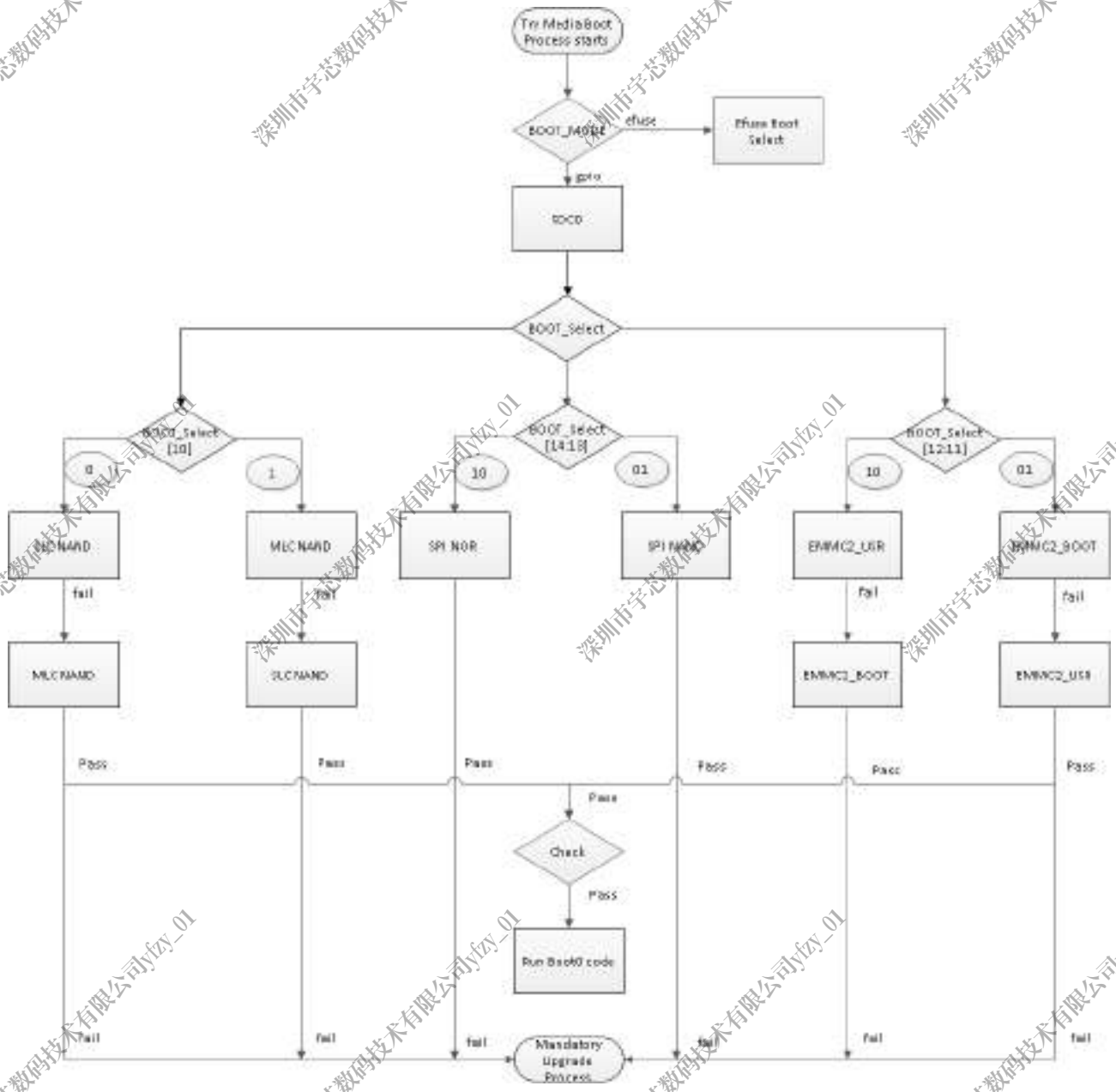


Figure 3-13. GPIO Pin Boot Select Process

NOTE

SMHC0 is external SD/TF card. SMHC2 is external eMMC.

Figure 3-14 shows Normal BROM eFuse Boot Select Process.

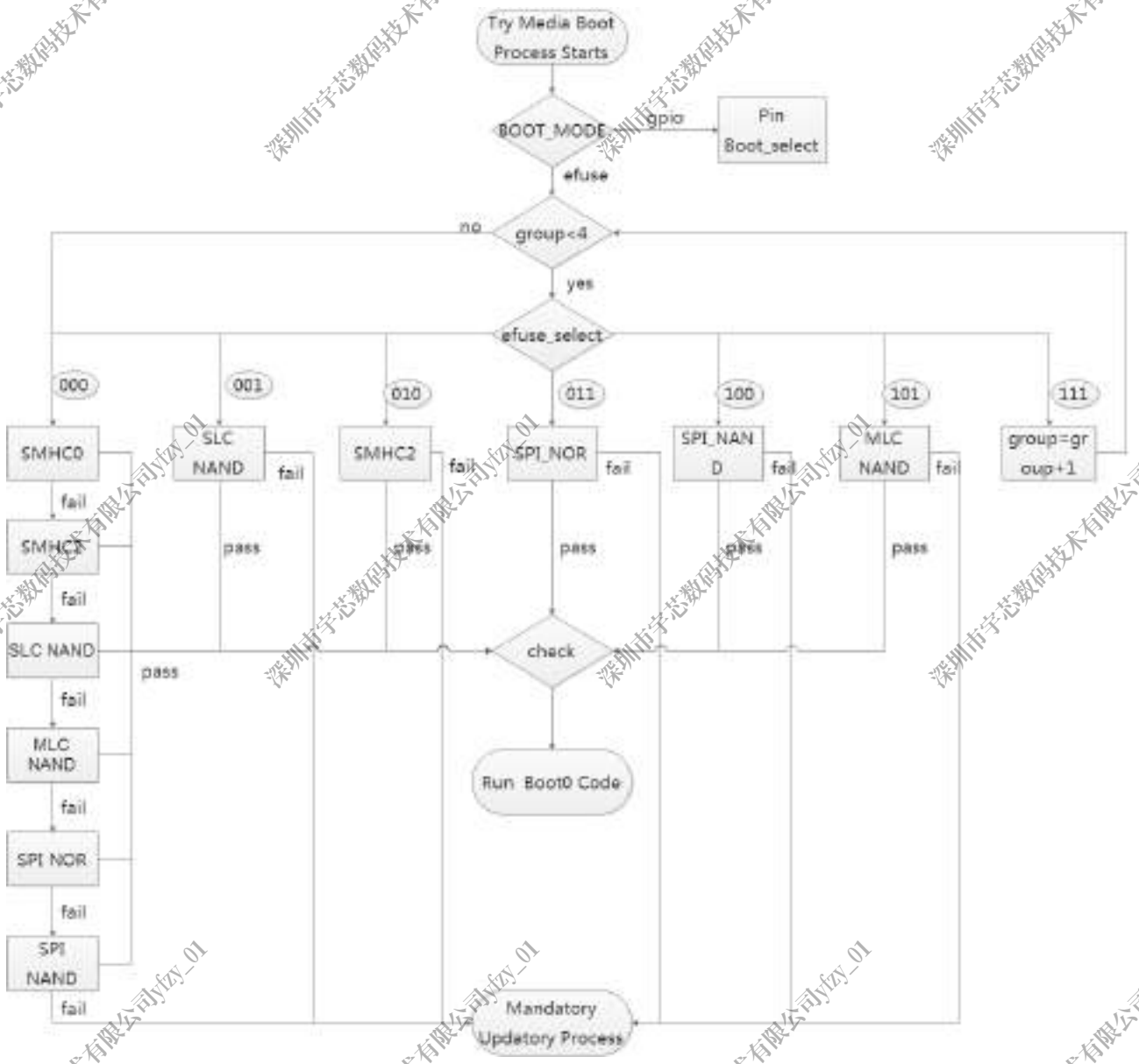


Figure 3-14. eFuse Boot Select Process

3.5. System Configuration

3.5.1. Overview

The system configuration module is used to configure parameter for system domain, such as SRAM, CPU, PLL, BROM, and so on.

The system configuration module has the following features:

- SRAM Bist function
- System parameter configuration
- PLL back door configuration
- BROM debug parameter configuration

The address range of SRAM is as follows.

Area	Address	Size(Bytes)
SRAM A1	0x0002 0000---0x0002 7FFF	32K
SRAM A2	0x0010 0000---0x0010 3FFF	16K
	0x0010 4000---0x0011 3FFF	64K
SRAM C	0x0002 8000---0x0004 7FFF	128K

3.5.2. Register List

Module Name	Base Address
SYS_CFG	0x03000000

Register Name	Offset	Description
VER_REG	0x0024	Version Register
EMAC_EPHY_CLKC_REG	0x0030	EMAC-EPHY Clock Register
BROM_OUTPUT_REG	0x00A4	BROM Output Register

3.5.3. Register Description

3.5.3.1. **Version Register**

<table>
<tr><td colspan="3">Offset:0x0024</td><td colspan="6">Register Name: VER_REG</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td colspan="6">Description</td></tr>
<tr><td>31:16</td><td>R</td><td>0x0</td><td colspan="6">Reserved</td></tr>
<tr><td>15</td><td>R/W</td><td>0x0</td><td colspan="6">Reserved</td></tr>
<tr><td>14:10</td><td>R</td><td>UDF</td><td colspan="6">BOOT_SEL_PAD_STA
<table>
<tr><td>Bit[10]</td><td>Bit[11]</td><td>Bit[12]</td><td>Bit[13]</td><td>Bit[14]</td><td>Media</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>MLC NAND</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>SLC NAND</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>eMMC USER</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>eMMC_BOOT</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>SPI_NOR</td></tr>
</table></td></tr>
</table>

			1 | 1 | 1 | 1 | 0 | SPI_NAND Bit[10] --> BOOT SLECT1 Bit[11] --> PC2 Bit[12] --> PC3 Bit[13] --> PC4 Bit[14] --> PC5
9	R	UDF	BOOT_SEL_0_PAD_STA(BOOT SELECT0) 0:UART Boot 1:USB Boot
8	R	UDF	FEL_SEL_PAD_STA Fel_Select_Pin_Status 0: Run_FEL 1:Try Media Boot
7:3	/	/	/
2:0	R	0x0	Reserved

3.5.3.2. **EMAC-EPHY Clock Register (Default Value: 0x0005_8000)**

Offset:0x0030			**Register Name: EMAC_EPHY_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	BPS_EFUSE
27	R/W	0x0	XMII_SEL 0: Internal SMI and MII 1: External SMI and MII
26:25	R/W	0x0	EPHY_MODE Operation Mode Selection 00: Normal Mode 01: Sim Mode 10: AFE Test Mode 11:/
24:20	R/W	0x0	PHY_ADDR PHY Address
19	R/W	0x0	BIST_CLK_EN 0: BIST clk disable 1: BIST clk enable
18	R/W	0x1	CLK_SEL 0:25MHz 1:24MHz
17	R/W	0x0	LED_POL 0:High active 1:Low active
16	R/W	0x1	SHUTDOWN 0:Power up 1:Shutdown
15	R/W	0x1	PHY_SELECT

			0:External PHY 1:Internal PHY
14	/	/	/
13	R/W	0x0	RMII_EN 0:Disable RMII module 1:Enable RMII module When the bit asserts, MII or RGMII interface is disabled.(It means bit13 is prior to bit2)
12:10	R/W	0x0	ETXDC Configure EMAC Transmit Clock Delay Chain
9:5	R/W	0x0	ERXDC Configure EMAC Receive Clock Delay Chain
4	R/W	0x0	ERXIE Enable EMAC Receive Clock Invertor 0:Disable 1:Enable
3	R/W	0x0	ETXIE Enable EMAC Transmit Clock Invertor 0:Disable 1:Enable
2	R/W	0x0	EPIT EMAC PHY Interface Type 0:MII 1:RGMII
1:0	R/W	0x0	ETCS EMAC Transmit Clock Source 00:Transmit clock source for MII 01:External transmit clock source for GMII and RGMII 10:Internal transmit clock source for GMII and RGMII 11:Reserved

3.5.3.3. **BROM Output Register (Default Value: 0x0000_0000)**

Offset:0x00A4			**Register Name: BROM_OUTPUT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	BROM_OUTPUT_VALUE 0: U-Boot pin output 0 1: U-Boot pin output 1
0	R/W	0x0	BROM_OUTPUT_ENALBE 0: Disable U-Boot pin output 1: Enable U-Boot pin output

3.6. Timer

3.6.1. Overview

The timer module implements the timing and counting functions.The timer module includes timer0 and timer1,watchdog, AVS.

The timer0 and timer1 are completely consistent.The timer0/1 has the following features:

- Configurable count clock: LOSC and OSC24M. LOSC is the internal low-frequency clock or the external low-frequency clock by setting LOSC_SRC_SEL. The external low-frequency has much accuracy.
- Configurable 8 prescale factor
- Programmable 32-bit down timer
- Two working modes: continue mode and single count mode
- Generates an interrupt when the count is decreased to 0

The watchdog is used to transimit a reset signal to reset the entire system after an exception occurs in the system.The watchdog has the following features:

- Single clock sourece: OSC24M/750
- 12 initial values to configure
- Generation of timeout interrupts
- Generation of reset signal
- Watchdog restart the timing

The AVS is used to the synchronization of audio and video. The AVS module includes AVS0 and AVS1, the AVS0 and AVS1 are completely consistent.The AVS has the following features:

- Single clock source: OSC24M
- Programmable 33-bit up timer
- Initial value can be updated anytime
- 12-bit frequency divider factor
- Pause/Start function

3.6.2. Block Diagram

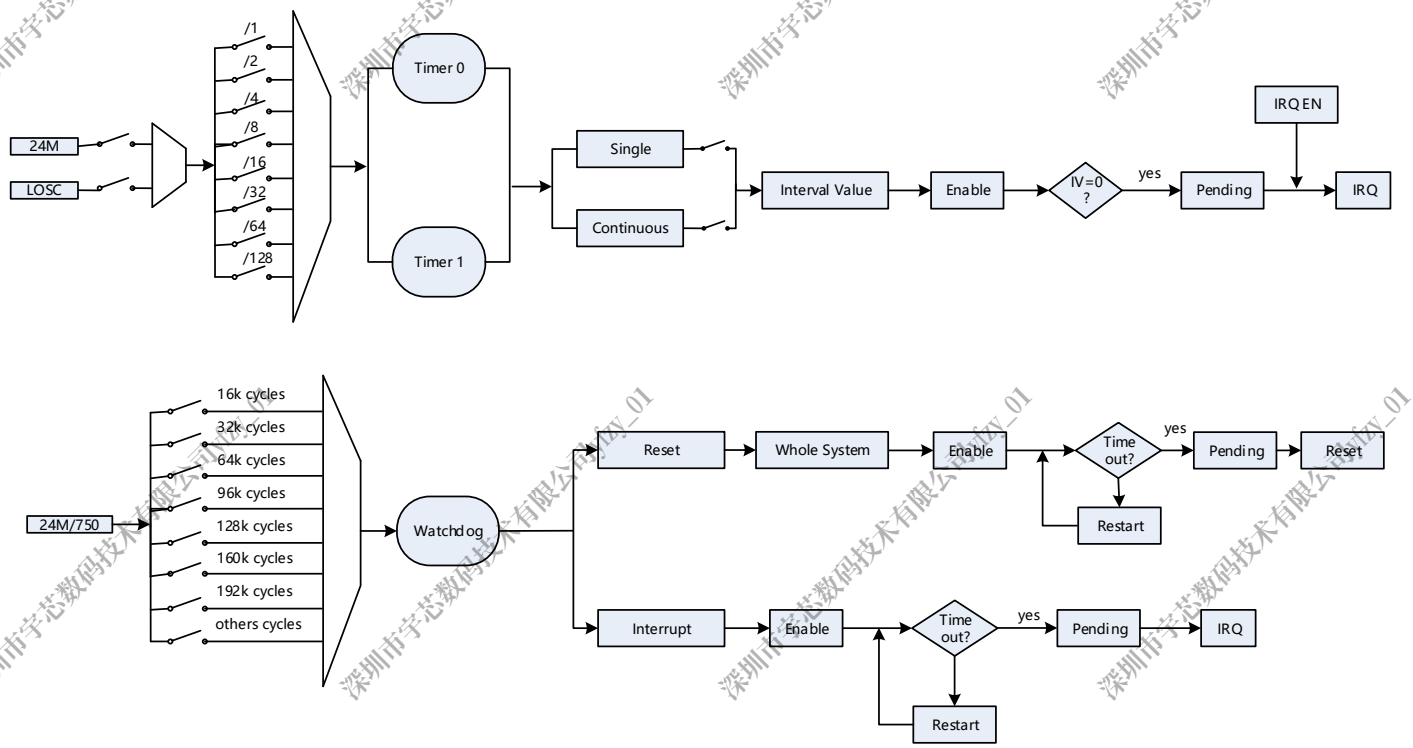


Figure 3-15. Timer Block Diagram

3.6.3. Operations and Functional Descriptions

3.6.3.1. **Timer Formula**

$$T_{timer0} = \frac{TMR0\_INTV\_VALUE\_REG - TMR0\_CUR\_VALUE\_REG}{TMR0\_CLK\_SRC} \times TMR0\_CLK\_PRES$$

TMR0_INTV_VALUE_REG: timer initial value;

TMR0_CUR_VALUE_REG: timer current counter;

TMR0_CLK_SRC: timer clock source;

TMR0_CLK_PRES: timer clock prescale ratio.

3.6.3.2. **Typical Application**

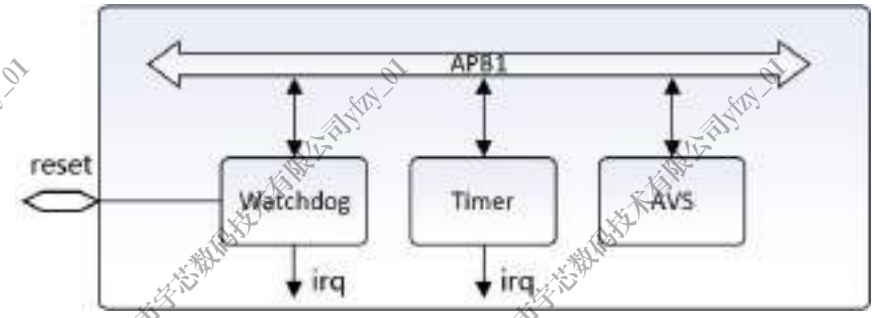


Figure 3-16. Timer Application Diagram

3.6.3.3. Function Implemention

3.6.3.3.1. Timer

The timer is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock. Each timer has independent interrupt.

The timer has two operating modes.

- Continuous mode

The bit7 of the TMRn_CTRL_REG is set to the continuous mode, when the count value is decreased to 0, the timer module reloads data from TMRn_INTV_VALUE_REG then continues to count.

- Single mode

The bit7 of the TMRn_CTRL_REG is set to the single mode, when the count value is decreased to 0, the timer stops counting. The timer starts to count again only when a new initial value is loaded.

Each timer has a prescaler that divides the working clock frequency of each timer by 1,2,4,8,16,32,64,128.

3.6.3.3.2. Watchdog

The watchdog is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

The watchdog has two operating modes.

- Interrupt mode

The WDOG0_CFG_REG is set to 0x02, when the counter value reaches 0 and the WDOG0_IRQ_EN_REG is enabled, the watchdog generates an interrupt.

- Reset mode

The WDOG0_CFG_REG is set to 0x01, when the counter value reaches 0, the watchdog generates a reset signal to reset the entire system.

The clock source of the watchdog is OSC24M/750.There are 12 configurable initial count values.

The watchdog can restart to count by setting the WDOG0_CTRL_REG: write 0xA57 to bit[12:1],then write 1 to bit[0].

3.6.3.3.3. AVS

The AVS is a 33-bit up counter.The counter value is increased by 1 on each rising edge of the count clock.

The AVS can be operated after its clock gating in CCU module is opened.

The AVS has an OSC24M clock source and a 12-bit division factor N. When the timer increases to N from 0, AVS counter adds 1; when the counter reaches 33-bit upper limit,the AVS will start to count from initial value again.

In counter working process, the division factor and initial counter of the AVS can be changed anytime.And the AVS can stop or start to operate counter anytime.

3.6.3.4. Operating Mode

3.6.3.4.1. Timer Initial

(1) Configure the timer parameters: clock source, prescale factor, working mode. The configuration of these parameters have no sequence,and implement by writing **TMRn_CTRL_REG**.
(2) Write the initial value: write **TMRn_INTV_VALUE_REG** to provide an initial value for the timer; write the bit[1] of **TMRn_CTRL_REG** to load the initial value to the timer, the bit[1] can not be written again before it is cleared automatically.
(3) Enable timer: write the bit[0] of **TMRn_CTRL_REG** to enable timer count; read **TMRn_CUR_VALUE_REG** to get the current count value.

3.6.3.4.2. Timer Interrupt

(1) Enable interrupt: write corresponding interrupt enable bit of **TMR_IRQ_EN_REG**, when timer counter time reaches, the corresponding interrupt generates.
(2) After enter interrupt process, write **TMR_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(3) Resume the interrupt and continue to execute the interrupted process.

3.6.3.4.3. Watchdog Initial

(1) Write **WDOG0_CFG_REG** to configure the generation of the interrupts and the output of reset signal.
(2) Write **WDOG0_MODE_REG** to configure the initial count value.
(3) Write **WDOG0_MODE_REG** to enable the watchdog.

3.6.3.4.4. Watchdog Interrupt

Watchdog interrupt is only used for the counter.
(1) Write **WDOG0_IRQ_EN_REG** to enable the interrupt.
(2) After enter the interrupt process, write **WDOG0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(3) Resume the interrupt and continue to execute the interrupted process.

3.6.3.4.5. AVS Start/Pause

(1) Write **AVS_CNT_DIV_REG** to configure the division factor.
(2) Write **AVS_CNT_REG** to configure the initial count value.
(3) Write **AVS_CNT_CTL_REG** to enable AVS counter. AVS counter can be paused at any time.

3.6.4. Programming Guidelines

3.6.4.1. Timer

Take making a 1ms delay for an example, 24M clock source, single mode and 2 pre-scale will be selected in the instance.

```
writel(0x2EE0,TMR_0_INTV);                    //Set interval value
writel(0x94, TMR_0_CTRL);                     //Select Single mode,24MHz clock source,2 pre-scale
writel(readl(TMR_0_CTRL)|(1<<1), TMR_0_CTRL); //Set Reload bit
while((readl(TMR_0_CTRL)>>1)&1);              //Waiting Reload bit turns to 0
writel(readl(TMR_0_CTRL)|(1<<0), TMR_0_CTRL); //Enable Timer0
```

3.6.4.2. Watchdog Reset

In the following instance making configurations for watchdog: configurate clock source as 24M/750, configurate interval value as 1s and configurate watchdog configuration as to whole system. This instance indicates that reset system after 1s.

```
writel(0x1, WDOG_CONFIG);                     //To whole system
writel(0x10, WDOG_MODE);                      //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);   //Enable Watchdog
```

3.6.4.3. Watchdog Restart

In the following instance making configurations for watchdog: configurate clock source as 24M/750, configurate interval value as 1s and configurate watchdog configuration as to whole system. In the following instance, if the time of other codes is larger than 1s, watchdog will reset the whole system. If the sentence of restart watchdog is implemented inside 1s, watchdog will be restarted.

```
writel(0x1, WDOG_CONFIG);                     //To whole system
writel(0x10, WDOG_MODE);                      //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);   //Enable Watchdog
----other codes---
writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0)，WDOG_CTRL); //Writel 0xA57 at Key Field and Restart Watchdog
```

3.6.5. Register List

Module Name	Base Address
Timer	0x03009000

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer Status Register
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register

TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
WDOG_IRQ_EN_REG	0x00A0	Watchdog IRQ Enable Register
WDOG_IRQ_STA_REG	0x00A4	Watchdog Status Register
WDOG_CTRL_REG	0x00B0	Watchdog Control Register
WDOG_CFG_REG	0x00B4	Watchdog Configuration Register
WDOG_MODE_REG	0x00B8	Watchdog Mode Register
AVS_CNT_CTL_REG	0x00C0	AVS Control Register
AVS_CNT0_REG	0x00C4	AVS Counter 0 Register
AVS_CNT1_REG	0x00C8	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x00CC	AVS Divisor Register

3.6.6. Register Description

3.6.6.1. **Timer IRQ Enable Register(Default Value: 0x0000_0000)**

Offset: 0x0000			**Register Name: TMR_IRQ_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1S	0x0	TMR1_IRQ_EN Timer 1 Interrupt Enable 0: Disable 1: Enable
0	R/W1S	0x0	TMR0_IRQ_EN Timer 0 Interrupt Enable 0: Disable 1: Enable

3.6.6.2. **Timer IRQ Status Register(Default Value: 0x0000_0000)**

Offset: 0x0004			**Register Name: TMR_IRQ_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	TMR1_IRQ_PEND Timer 1 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 1 interval value is reached
0	R/W1C	0x0	TMR0_IRQ_PEND Timer 0 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 0 interval value is reached

3.6.6.3. Timer 0 Control Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR0_MODE Timer 0 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR0_RELOAD Timer 0 Reload 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it is cleared automatically.
0	R/W	0x0	TMR0_EN Timer 0 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.6.6.4. Timer 0 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TMR0_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_INTV_VALUE Timer 0 Interval Value The value setting should consider the system clock and the timer clock source.

3.6.6.5. Timer 0 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_CUR_VALUE Timer 0 Current Value Timer 0 current value is a 32-bit down-counter (from interval value to 0).

3.6.6.6. Timer 1 Control Register(Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR1_MODE Timer 1 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES Select the pre-scale of timer 1 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR1_RELOAD Timer 1 Reload

			0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it is cleared automatically.
0	R/W	0x0	TMR1_EN Timer 1 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.6.6.7. Timer 1 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_INTV_VALUE. Timer 1 Interval Value. The value should consider the system clock and the timer clock source.

3.6.6.8. Timer 1 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name:TMR1_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_CUR_VALUE Timer 1 Current Value Timer 1 current value is a 32-bit down-counter (from interval value to 0).

3.6.6.9. Watchdog IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name:WDOG_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1S	0x0	WDOG_IRQ_EN Watchdog Interrupt Enable 0: No effect 1: Watchdog interrupt enable.

3.6.6.10. Watchdog Status Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name:WDOG_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	WDOG_IRQ _PEND Watchdog IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, Watchdog interval value is reached

3.6.6.11. Watchdog Control Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name:WDOG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:1	R/W	0x0	WDOG_KEY_FIELD Watchdog Key Field It should be written to 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	WDOG_RESTART Watchdog Restart 0: No effect 1: Restart the Watchdog

3.6.6.12. Watchdog Configuration Register (Default Value: 0x0000_0001)

Offset: 0x00B4			Register Name:WDOG_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	WDOG_CONFIG 00:/ 01: to whole system 10: only interrupt 11: /

3.6.6.13. Watchdog Mode Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name:WDOG_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	WDOG_INTV_VALUE Watchdog Interval Value

			Watchdog clock source is OSC24M / 750. If the clock source is turned off, Watchdog will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) Others:Reserved
3:1	/	/	/
0	R/W1S	0x0	WDOG_EN Watchdog Enable 0: No effect 1: Enable the Watchdog

3.6.6.14. AVS Counter Control Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: AVS_CNT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN Audio/Video Sync Counter 1 Enable/ Disable The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN Audio/Video Sync Counter 0 Enable/ Disable The counter source is OSC24M. 0: Disable 1: Enable

3.6.6.15. **AVS Counter 0 Register (Default Value: 0x0000_0000)**

Offset: 0x00C4			Register Name: AVS_CNT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT0 Counter 0 for Audio/Video Sync Application The high 32 bits of the internal 33-bit counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter will not increase.

3.6.6.16. **AVS Counter 1 Register(Default Value: 0x0000_0000)**

Offset: 0x00C8			Register Name:AVS_CNT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT1 Counter 1 for Audio/ Video Sync Application The high 32 bits of the internal 33-bit counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter will not increase.

3.6.6.17. **AVS Counter Divisor Register (Default Value: 0x05DB_05DB)**

Offset: 0x00CC			Register Name: AVS_CNT_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D Divisor N for AVS Counter 1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit [27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. It can be configured by software at any time.

15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D Divisor N for AVS Counter 0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit [11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. It can be configured by software at any time.

3.7. High Speed Timer

3.7.1. Overview

The high speed timer(HSTimer) module implements the timing and counting functions.

The HSTimer has the following features:

- Timing clock is AHB1 that can provides more accurate timing clock, the normal working frequency is 200MHz
- Configurable 5 prescale factor
- Configurable 56-bit down timer
- Supports 2 working modes: continuous mode and single mode
- Supports test mode
- Generates an interrupt when the count is decreased to 0

3.7.2. Block Diagram

Figure 3-17 shows a block diagram of the HSTimer.

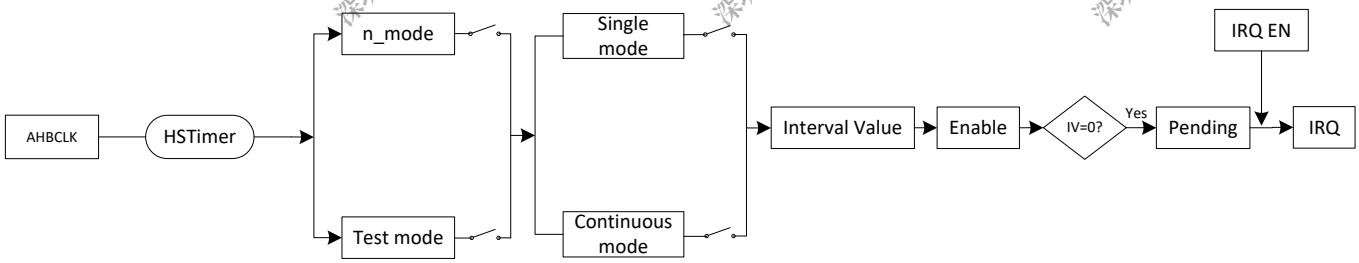


Figure 3-17. HSTimer Block Diagram

3.7.3. Operations and Functional Description

3.7.3.1. HSTimer Formula

$$\frac{(HS\_TMR\_INTV\_HI\_REG<<32 + HS\_TMR\_INTV\_LO\_REG) - (HS\_TMR\_CURNT\_HI\_REG<<32 + HS\_TMR\_CURNT\_LO\_REG)}{AHB1CLK} \times HS\_TMR\_CLK$$

HS_TMR_INTV_HI_REG: Initial of Counter Higher Bit

HS_TMR_INTV_LO_REG: Initial of Counter Lower Bit

HS_TMR_CURNT_HI_REG: Current Value of Counter Higher Bit

HS_TMR_CURNT_LO_REG: Current Vaule of Counter Lower Bit

AHB1CLK: AHB1 Clock Frequency

HS_TMR_CLK: Time Prescale Ratio of Counter

3.7.3.2. Typical Application

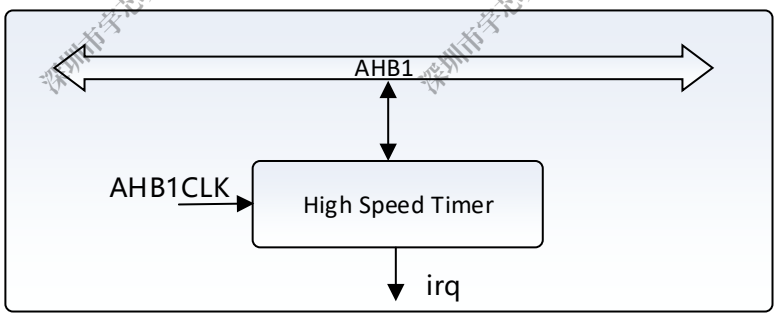


Figure 3-18. HSTimer Application Diagram

The high speed timer is on AHB1, and the high speed timer controls registers by AHB1.
The high speed timer has single clock source: AHB. The high speed timer can generate interrupt.

3.7.3.3. Function Implemention

The timer is a 56-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.
The high speed timer has two timing modes.

- Continuous mode : The bit7 of HS_TMR0_CTRL_REG is set to the continuous mode, when the count value is decreased to 0, the high speed timer module reloads data from HS_TMR_INTV_LO_REG and HS_TMR_INTV_HI_REG then continues to count.
- Single mode : The bit7 of HS_TMR0_CTRL_REG is set to the single mode, when the count value is decreased to 0, the high speed timer stops counting. The high speed timer starts to count again only when a new initial value is loaded.

The high speed timer has two operating modes.

- Normal mode: When the bit31 of HS_TMR0_CTRL_REG is set to the normal mode, the high speed timer is used as 56-bit down counter, which can continuous timing and single timing.
- Test mode: When the bit31 of HS_TMR0_CTRL_REG is set to the normal mode, then HS_TMR_INTV_LO_REG must be set to 0x1, the high speed timer is used as 24-bit down counter, and HS_TMR_INTV_HI_REG is the initial value of the high speed timer.

Each high speed timer has a prescaler that divides the working clock frequency of each working timer by 1,2,4,8, 16.

3.7.3.4. Operating Mode

3.7.3.4.1. HSTimer Initial

(1) AHB1 clock management: Open the clock gating of AHB1 and de-assert the soft reset of AHB1 in CCU.
(2) Configure the corresponding parameters of the high speed timer: clock source, prescaler factor, working mode, counting mode. These parameters that are written to **HS_TMR0_CTRL_REG** have no sequences.
(3) Write the initial value: Firstly write the low-bit register **HS_TMR_INTV_LO_REG**, then write the high-bit register **HS_TMR_INTV_HI_REG**. Write the bit1 of **HS_TMR0_CTRL_REG** to load the initial value. If in timing stop stage of high speed timer, write the bit1 and bit0 of **HS_TMR0_CTRL_REG** to reload the initial value.
(4) Enable high speed timer: Write the bit[0] of **HS_TMR0_CTRL_REG** to enable high speed timer to count.

3.7.3.4.2. HSTimer Interrupt

(1) Enable interrupt: Write the corresponding interrupt enable bit of **HS_TMR_IRQ_EN_REG**, when the counting time of high speed timer reaches , the corresponding interrupt generates.
(2) After enter the interrupt process, write **HS_TMR_IRQ_STAS_REG** to clear the interrupt pending.
(3) Resume the interrupt and continue to execute the interrupted process.

3.7.4. Programming Guidelines

Take making a 1us delay using HSTimer0 for an instance as follow, AHB1CLK will be configurated as 100MHz and n_mode,single mode and 2 pre-scale will be selected in this instance.

```
writel(0x0, HS_TMR0_INTV_HI);                    //Set interval value Hi 0x0
writel(0x32, HS_TMR0_INTV_LO);                   //Set interval value Lo 0x32
writel(0x90, HS_TMR0_CTRL);                      //Select n_mode,2 pre-scale,single mode
writel(readl(HS_TMR0_CTRL)|(1<<1), HS_TMR0_CTRL);  //Set Reload bit
writel(readl(HS_TMR0_CTRL)|(1<<0), HS_TMR0_CTRL);  //Enable HSTimer0
while(!(readl(HS_TMR_IRQ_STAT)&1));              //Wait for HSTimer0 to generate pending
writel(1,HS_TMR_IRQ_STAT);                       //Clear HSTimer0 pending
```

3.7.5. Register List

Module Name	Base Address
High Speed Timer	0x03005000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0000	HS Timer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x0004	HS Timer Status Register
HS_TMR0_CTRL_REG	0x0020	HS Timer 0 Control Register
HS_TMR0_INTV_LO_REG	0x0024	HS Timer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x0028	HS Timer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x002C	HS Timer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x0030	HS Timer 0 Current Value High Register
HS_TMR1_CTRL_REG	0x0040	HS Timer 1 Control Register
HS_TMR1_INTV_LO_REG	0x0044	HS Timer 1 Interval Value Low Register
HS_TMR1_INTV_HI_REG	0x0048	HS Timer 1 Interval Value High Register
HS_TMR1_CURNT_LO_REG	0x004C	HS Timer 1 Current Value Low Register
HS_TMR1_CURNT_HI_REG	0x0050	HS Timer 1 Current Value High Register

3.7.6. Register Description

3.7.6.1. HS Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1S	0x0	HS_TMR1_INT_EN High Speed Timer 1 Interrupt Enable 0: Disable 1: Enable
0	R/W1S	0x0	HS_TMR0_INT_EN High Speed Timer 0 Interrupt Enable 0: Disable 1: Enable

3.7.6.2. HS Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	HS_TMR1_IRQ_PEND High Speed Timer 1 IRQ Pending Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 1 interval value is reached.
0	R/W1C	0x0	HS_TMR0_IRQ_PEND High Speed Timer 0 IRQ Pending Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 0 interval value is reached.

3.7.6.3. HS Timer 0 Control Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: HS_TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR0_TEST High Speed Timer 0 Test Mode In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode
30:8	/	/	/
7	R/W	0x0	HS_TMR0_MODE

			High Speed Timer 0 Mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W1S	0x0	HS_TMR0_RELOAD High Speed Timer 0 Reload 0: No effect 1: Reload High Speed Timer 0 Interval Value
0	R/W	0x0	HS_TMR0_EN High Speed Timer 0 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.4. HS Timer 0 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: HS_TMR0_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_INTV_VALUE_LO High Speed Timer 0 Interval Value [31:0]

3.7.6.5. HS Timer 0 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0028	Register Name: HS_TMR0_INTV_HI_REG

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_INTV_VALUE_HI High Speed Timer 0 Interval Value [55:32]

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the High register should be written after the Lo register.

3.7.6.6. HS Timer 0 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_CUR_VALUE_LO High Speed Timer 0 Current Value [31:0]

3.7.6.7. HS Timer 0 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: HS_TMR0_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_CUR_VALUE_HI High Speed Timer 0 Current Value [55:32]

NOTE

HS timer current value is a 56-bit down-counter (from interval value to 0).

The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

3.7.6.8. HS Timer 1 Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: HS_TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR1_TEST High Speed Timer 1 Test Mode In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode
30:8	/	/	/
7	R/W	0x0	HS_TMR1_MODE High Speed Timer 1 Mode

			0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR1_CLK Select the pre-scale of the high speed timer 1 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W1S	0x0	HS_TMR1_RELOAD High Speed Timer 1 Reload 0: No effect 1: Reload High Speed Timer 1 Interval Value
0	R/W	0x0	HS_TMR1_EN High Speed Timer 1 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.9. **HS Timer 1 Interval Value Lo Register(Default Value: 0x0000_0000)**

Offset: 0x0044			**Register Name: HS_TMR1_INTV_LO_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_INTV_VALUE_LO High Speed Timer 1 Interval Value [31:0]

3.7.6.10. **HS Timer 1 Interval Value Hi Register(Default Value: 0x0000_0000)**

Offset: 0x0048			**Register Name: HS_TMR1_INTV_HI_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_INTV_VALUE_HI High Speed Timer 1 Interval Value [55:32]

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the High register should be written after the Lo register.

3.7.6.11. HS Timer 1 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: HS_TMR1_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_CUR_VALUE_LO High Speed Timer 1 Current Value [31:0]

3.7.6.12. HS Timer 1 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: HS_TMR1_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_CUR_VALUE_HI High Speed Timer 1 Current Value [55:32]

NOTE

HS timer current value is a 56-bit down-counter (from interval value to 0).

The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

3.8. GIC

3.8.1. Interrupt Source

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0	SGI 0	0x0000	SGI 0 interrupt
1	SGI 1	0x0004	SGI 1 interrupt
2	SGI 2	0x0008	SGI 2 interrupt
3	SGI 3	0x000C	SGI 3 interrupt
4	SGI 4	0x0010	SGI 4 interrupt
5	SGI 5	0x0014	SGI 5 interrupt
6	SGI 6	0x0018	SGI 6 interrupt
7	SGI 7	0x001C	SGI 7 interrupt
8	SGI 8	0x0020	SGI 8 interrupt
9	SGI 9	0x0024	SGI 9 interrupt
10	SGI 10	0x0028	SGI 10 interrupt
11	SGI 11	0x002C	SGI 11 interrupt
12	SGI 12	0x0030	SGI 12 interrupt
13	SGI 13	0x0034	SGI 13 interrupt
14	SGI 14	0x0038	SGI 14 interrupt
15	SGI 15	0x003C	SGI 15 interrupt
16	PPI 0	0x0040	PPI 0 interrupt
17	PPI 1	0x0044	PPI 1 interrupt
18	PPI 2	0x0048	PPI 2 interrupt
19	PPI 3	0x004C	PPI 3 interrupt
20	PPI 4	0x0050	PPI 4 interrupt
21	PPI 5	0x0054	PPI 5 interrupt
22	PPI 6	0x0058	PPI 6 interrupt
23	PPI 7	0x005C	PPI 7 interrupt
24	PPI 8	0x0060	PPI 8 interrupt
25	PPI 9	0x0064	PPI 9 interrupt
26	PPI 10	0x0068	PPI 10 interrupt
27	PPI 11	0x006C	PPI 11 interrupt
28	PPI 12	0x0070	PPI 12 interrupt
29	PPI 13	0x0074	PPI 13 interrupt
30	PPI 14	0x0078	PPI 14 interrupt
31	PPI 15	0x007C	PPI 15 interrupt
32	GPADC	0x0080	GPADC interrupt
33	THS	0x0084	THS interrupt
34	/	/	/
35	/	/	/
36	/	/	/
37	/	/	/
38	/	/	/

Interrupt Number	Interrupt Source	Interrupt Vector	Description
39	DMIC	0x009C	DMIC interrupt
40	DRAM_PHY	0x00A0	DRAM PHY interrupt
41	DRAM	0x00A4	DRAM interrupt
42	DMA	0x00A8	DMA interrupt
43	MBOX	0x00AC	MBOX interrupt
44	SPINLOCK	0x00B0	SPINLOCK interrupt
45	/	/	/
46	WDOG	0x00B8	WDOG interrupt
47	PWM	0x00BC	PWM interrupt
48	/	/	/
49	BUS_TIMEOUT	0x00C4	Bus Timeout interrupt
50	/	/	/
51	PSI	0x00CC	PSI interrupt
52	/	/	/
53	G2D	0x00D4	G2D interrupt
54	/	0x00D8	/
55	/	0x00DC	/
56	ISE	0x00E0	ISE interrupt
57	VE	0x00E4	VE interrupt
58	EISE	0x00E8	EISE interrupt
59	EMAC	0x00EC	EMAC interrupt
60	Audio Codec	0x00F0	Audio Codec interrupt
61	NAND0	0x00F4	NAND0 interrupt
62	TVE	0x00F8	TVE interrupt
63	DE	0x00FC	DE interrupt
64	DI	0x0100	DE-interlace interrupt
65	ISP0	0x0104	ISP0 interrupt
67	/	0x010C	/
68	CE_S	0x0110	CE_S interrupt
69	I2S/PCM0	0x0114	I2S/PCM0 interrupt
70	I2S/PCM1	0x0118	I2S/PCM1 interrupt
71	I2S/PCM2	0x011C	I2S/PCM2 interrupt
72	HDMI1.4_TX0	0x0120	HDMI1.4_TX0 interrupt
73	TWI0	0x0124	TWI0 interrupt
74	TWI1	0x0128	TWI1 interrupt
75	TWI2	0x012C	TWI2 interrupt
76	TWI3	0x0130	TWI3 interrupt
77	MIPI_DSI	0x0134	MIPI_DSI interrupt
78	SMHC0	0x0138	SMHC0 interrupt
79	SMHC1	0x013C	SMHC1 interrupt
80	SMHC2	0x0140	SMHC2 interrupt
81	UART0	0x0144	UART0 interrupt
82	UART1	0x0148	UART1 interrupt
83	UART2	0x014C	UART2 interrupt

Interrupt Number	Interrupt Source	Interrupt Vector	Description
84	UART3	0x0150	UART3 interrupt
85	UART4	0x0154	UART4 interrupt
86	SPI0	0x0158	SPI0 interrupt
87	SPI1	0x015C	SPI1 interrupt
88	SPI2	0x0160	SPI2 interrupt
89	SPI3	0x0164	SPI3 interrupt
90	HSTIMER0	0x0168	HSTIMER0 interrupt
91	HSTIMER1	0x016C	HSTIMER1 interrupt
92	TIMER0	0x0170	TIMER0 interrupt
93	TIMER1	0x0174	TIMER1 interrupt
94	TCON_LCD0	0x0178	TCON_LCD0 interrupt
95	TCON_TV0	0x017C	TCON_TV0 interrupt
96	USB2.0_OTG_DEVICE	0x0180	USB2.0_OTG_DEVICE interrupt
97	USB2.0_OTG_EHCI	0x0184	USB2.0_OTG_EHCI interrupt
98	USB2.0_OTG_OHCI	0x0188	USB2.0_OTG_OHCI interrupt
99	GPIOC	0x018C	GPIOC interrupt
100	GPIOD	0x0190	GPIOD interrupt
101	GPIOE	0x0194	GPIOE interrupt
102	GPIOF	0x0198	GPIOF interrupt
103	GPIOG	0x019C	GPIOH interrupt
104	GPIOH	0x01A0	GPIOH interrupt
105	GPIOI	0x01A4	GPIOI interrupt
106	CSI_DMA0	0x01A8	CSI_DMA0 interrupt
107	CSI_DMA1	0x01AC	CSI_DMA1 interrupt
108	CSI_DMA2	0x01B0	CSI_DMA2 interrupt
109	CSI_DMA3	0x01B4	CSI_DMA3 interrupt
110	CSI_PARSER0	0x01B8	CSI_PARSER0 interrupt
111	CSI_PARSER1	0x01BC	CSI_PARSER1 interrupt
112	CSI_CCI0	0x01C0	CSI_CCI0 interrupt
113	CSI_CCI1	0x01C4	CSI_CCI1 interrupt
114	CSI_COMBO0_RX	0x01C8	CSI_COMBO0 interrupt
115~123	/	/	/
124	CSI_TOP_PKT	0x01F0	CSI_TOP_PKT interrupt
125	/	/	/
126	VDPO	0x01F8	VDPO interrupt
127~135	/	/	/
136	External NMI	0x0220	External NMI interrupt
137	R_TIMER0	0x0224	R_TIMER0 interrupt
138	R_TIMER1	0x0228	R_TIMER1 interrupt
139	R_Alarm0	0x022C	R_Alarm0 interrupt
140	R_Alarm1	0x0230	R_Alarm1 interrupt
141	R_WDOG	0x0234	R_WDOG interrupt
142	R_GPIOL	0x0238	R_GPIOL interrupt
143	R_UART0	0x023C	R_UART0 interrupt

Interrupt Number	Interrupt Source	Interrupt Vector	Description
144	R_TWI0	0x0240	R_TWI0 interrupt
145	R_TWI1	0x0244	R_TWI1 interrupt
146	R_RSB	0x0248	R_RSB interrupt
147	R_CIR_RX	0x024C	R_CIR interrupt
148	R_CPU_IDLE	0x0250	R_CPU_IDLE interrupt
149	R_OWC	0x0254	R_OWC interrupt
150		0x0258	
151~159	/	/	/
160	C0_CTI0	0x0280	C0_CTI0 interrupt
161	C0_CTI1	0x0284	C0_CTI1 interrupt
162	C0_CTI2	0x0288	C0_CTI2 interrupt
163	C0_CTI3	0x028C	C0_CTI3 interrupt
164	C0_COMMTX0	0x0290	C0_COMMTX0 interrupt
165	C0_COMMTX1	0x0294	C0_COMMTX1 interrupt
166	C0_COMMTX2	0x0298	C0_COMMTX2 interrupt
167	C0_COMMTX3	0x029C	C0_COMMTX3 interrupt
168	C0_COMMRX0	0x02A0	C0_COMMRX0 interrupt
169	C0_COMMRX1	0x02A4	C0_COMMRX1 interrupt
170	C0_COMMRX2	0x02A8	C0_COMMRX2 interrupt
171	C0_COMMRX3	0x02AC	C0_COMMRX3 interrupt
172	C0_PMU0	0x02B0	C0_PMU0 interrupt
173	C0_PMU1	0x02B4	C0_PMU1 interrupt
174	C0_PMU2	0x02B8	C0_PMU2 interrupt
175	C0_PMU3	0x02BC	C0_PMU3 interrupt
176	C0_AXI_ERROR	0x02C0	C0_AXI_ERROR interrupt
177	/	/	/
178	C0_AXI_WR	0x02C8	C0_AXI_WR interrupt
179	C0_AXI_RD	0x02CC	C0_AXI_RD interrupt

For details about GIC, please refer to the GIC PL400 technical reference manual and ARM GIC Architecture Specification V2.0.

3.9. DMA

3.9.1. Overview

The direction memory access (DMA) is used to transfer data between a peripheral and a memory, between peripherals, or between memories. DMA is a high-speed data transfer operation that reduces the CPU resources.

The DMA has the following features:

- 16 channels DMA
- Provides 32 peripheral DMA requests for data read and 32 peripheral DMA requests for data write
- Transfer with linked list
- Programmable 8-,16-,32-,64-bit data width
- Programmable DMA burst length
- DRQ response includes wait mode and handshake mode
- Memory devices support non-aligned transform
- DMA channel supports pause function

3.9.2. Block Diagram

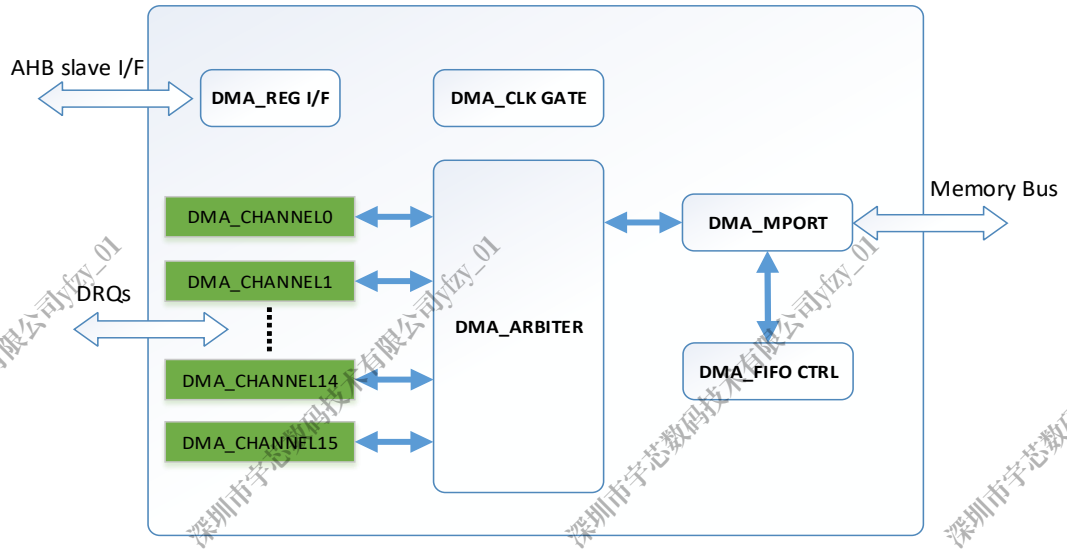


Figure 3-19. DMA Block Diagram

DMA_ARBITER: Arbitrate DMA read/write requirement of each channel, and convert to read/write requirement of each port.

DMA_CHANNEL: DMA transform engine.Each channel is independent. The priorities of DMA channels uses polling mechanism. When the DMA requests from two peripherals are valid simultaneously, if DMA_ARBITER is non-idle ,the next channel of the current channel has the higher priority; if DMA_ARBITER is idle, the channel0 has the highest priority, whereas the channel15 has the lowest priority.

DMA_MPORT: Receive read/write requirement of DMA_ARBITER ,and convert to the corresponding MBUS access.

DMA_FIFOCTL: Internal FIFO cell control module.

DMA_REGIF: Common register module, mainly used to resolve AHB1 demand.

DMA_CLKGATE: Hardware auto clock gating control module.

DMA integrates 16 independent DMA channels. When DMA channel starts, DMA gets DMA descriptor by

DMA_DESC_ADDR_REG to use for the configuration information of the current DMA package transfer ,and DMA can transfer data between the specified peripherals through the configuration information. When a package transfer finished, DMA judges if the current channel transfer finished through the linked information in descriptor.

3.9.3. Operations and Functional Description

3.9.3.1. Clock and Reset

DMA is on AHB1.The clock of AHB1 influences the transfer efficiency of DMA.

3.9.3.2. Typical Application

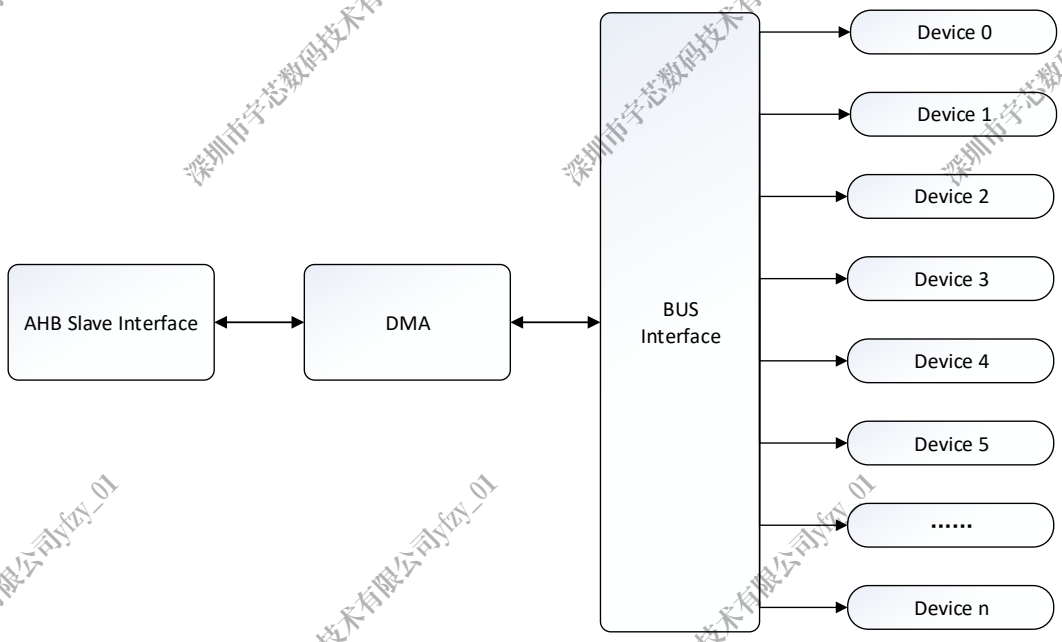


Figure 3-20. DMA Typical Application Diagram

3.9.3.3. DRQ Type

Table 3-8. DMA DRQ Table

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2		port2	
port3	I2S/PCM0-RX	port3	I2S/PCM0-TX
port4	I2S/PCM1-RX	port4	I2S/PCM1-TX
port5	I2S/PCM2-RX	port5	I2S/PCM2-TX
port6	Audio Codec	port6	Audio Codec
port7	DMIC	port7	

port8		port8	
port9		port9	
port10	NAND0	port10	NAND0
port11		port11	
port12	GPADC	port12	
port13		port13	
port14	UART0-RX	port14	UART0-TX
port15	UART1-RX	port15	UART1-TX
port16	UART2-RX	port16	UART2-TX
port17	UART3-RX	port17	UART3-TX
port18	UART4-RX	port18	UART4-TX
port19		port19	
port20		port20	
port21		port21	
port22	SPI0-RX	port22	SPI0-TX
port23	SPI1-RX	port23	SPI1-TX
port24	SPI2-RX	port24	SPI2-TX
port25	SPI3-RX	port25	SPI3-TX
port26		port26	
port27		port27	
port28		port28	
port29		port29	
Port30	USB2.0_OTG_EP1	Port30	USB2.0_OTG_EP1
Port31	USB2.0_OTG_EP2	Port31	USB2.0_OTG_EP2
Port32	USB2.0_OTG_EP3	Port32	USB2.0_OTG_EP3
Port33	USB2.0_OTG_EP4	Port33	USB2.0_OTG_EP4
Port34	USB2.0_OTG_EP5	Port34	USB2.0_OTG_EP5
Port35			
Port36			
Port37			
Port38			
Port39			
Port40			
Port41			
Port42			
Port43	TWI1	Port43	TWI1
Port44	TWI2	Port44	TWI2
Port45	TWI3	Port45	TWI3
Port46	TWI4	Port46	TWI4

3.9.3.4. DMA Descriptor

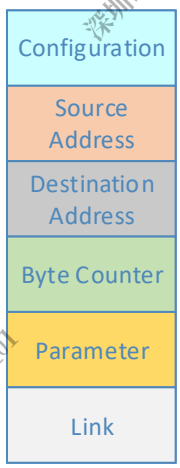


Figure 3-21. DMA Descriptor

DMA descriptor is the configuration information of DMA transfer that decides the DMA working mode. Each descriptor includes 6 words, in turn, configuration, source address, destination address, byte counter, parameter, link.

Configuration : Configure the following information by DMA_CFG_REG.

- DRQ type of source and destination.
- Transferred address count mode : IO mode indicates the address is fixed during transfer; linear mode indicates the address is increasing during transfer.
- Transferred block length : block length is the amount of DMA transferred data in one-shot valid DRQ. The block length supports 1-bit,4-bit,8-bit or 16-bit mode.
- Transferred data width: data width indicates the data width of every operation, and supports 8-bit,16-bit,32-bit or 64-bit mode.

Source Address: Configure the transferred source address.

Destination Address: Configure the transferred destination address.

DMA reads data from the source address , then writes data to the destination address.

Byte counter: Configure the amount of a package. The maximum package is not more than (2^25-1) bytes. If the amount of the package reaches the maximum value, even if DRQ is valid, DMA should stop the current transfer.

Parameter: Configure the interval between data block. The parameter is valid for non-memory peripherals. When DMA detects that DRQ is high level, DMA transfers block cycle. And during time, the changing of DRQ is ignored.After transferred, DMA waits the setting cycle(WAIT_CYC), then executes the next DRQ detection.

If the value of the link is 0xFFFFF800, the current package is at the end of the linked list. DMA will stop transfer after the package is transferred; if the value of the link is not 0xFFFFF800, the value of the link is considered the descriptor address of the next package.

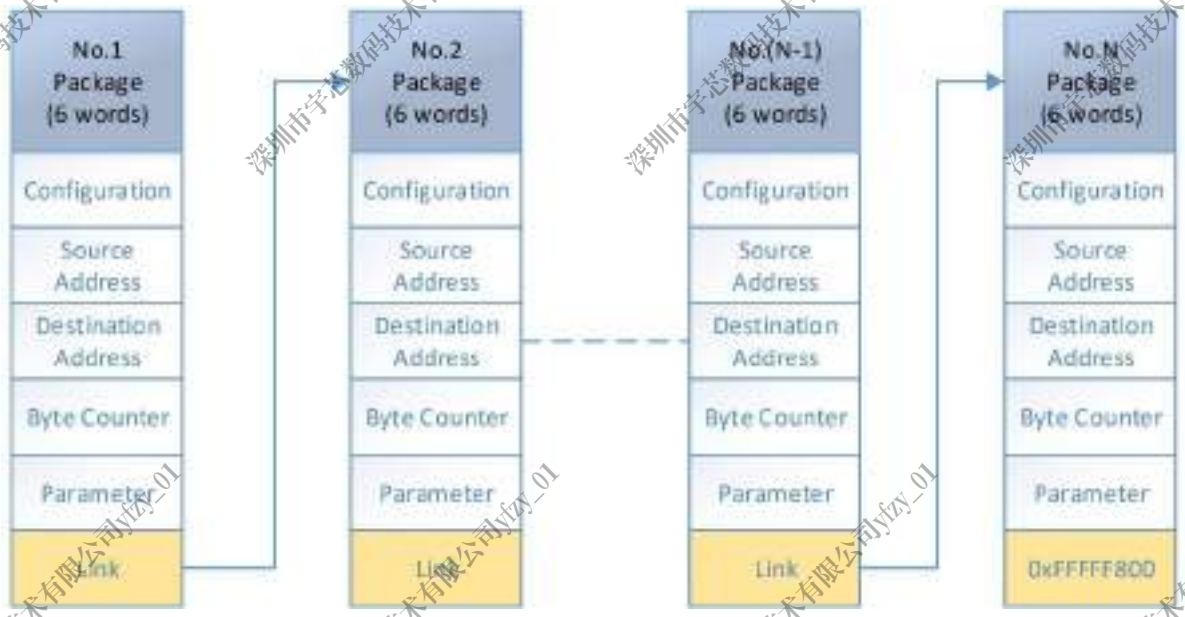


Figure 3-22. DMA Chain Transfer

3.9.3.5. **Interrupt**

The half package interrupt is enabled, DMA sends half package interrupt after the half package transfer completes. The total package interrupt is enabled, DMA sends package end interrupt after the total package transfer completes. The total queue interrupt is enabled, DMA sends queue end interrupt after the total queue completes. Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts generate very closely, the later interrupt may override the former one. So DMA has only a system interrupt source.

3.9.3.6. **Clock Gating**

DMA CLK GATE module is the clock module of auto-controlled by hardware. DMA CLK GATE module is mainly used to generate the clock of DMA sub-module and the local circuit in module, including clock gating of channel and clock gating of public part.

The clock gating of the channel indicates DMA clock can auto-open when the system accesses the current DMA channel register and DMA channel is enabled. When DMA transfer is completed, DMA channel clock can auto-close after 16 HCLK delay, meanwhile the clock of the corresponding channel control and FIFO control will be closed.

The clock gating of the common part indicates the clock of the common circuit can auto-close when all DMA channels are opened. The common circuit includes the common circuit of FIFO control module, MPORT module and memory bus clock.

DMA clock gating can support all the functions stated above or not by software.

3.9.3.7. **Transfer Mode**

DMA supports two data transfer modes: wait mode and handshake mode.

(1) Wait Mode

When device request signal enters DMA, the device request signal is transformed into the internal DRQ signal through

block and wait counter. The transformed principle is as follows.

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically.
- After the internal DRQ holds low automatically to the DMA cycle of wait counter times, DMA restarts to detect the external request, if the external request signal is valid, then the next transfer starts.

(2) Handshake Mode

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically; meanwhile within the last operation , DMA follows the operating demand to send DMA last signal simultaneously.
- The DMA last signal that is used as a part of DMA demand transmits at BUS, when the device receives the operating demand of DMA last at BUS, the device can judge DMA transfer block length finished, that is before transmit the request again ,DMA operation cannot appear, and a DMA active signal is generated to the DMA controller. Notice that each DRQ signal of device corresponds to an active signal, if the device has many DRQ signals, then DMA returns different active signal through different bus operation.
- When DMA receives the transmitted active signal of devices, DMA ACK signal is returned to devices.
- After the device receives DMA ACK signal, if all operations of devices are completed , FIFO status and DRQ status are refreshed, then active signal is set as invalid.
- When DMA detects the falling edge of active signal, then the corresponding ACK signal is set as invalid, and DMA restarts to detect the external request signal. If the request signal is valid, then the next transfer starts.

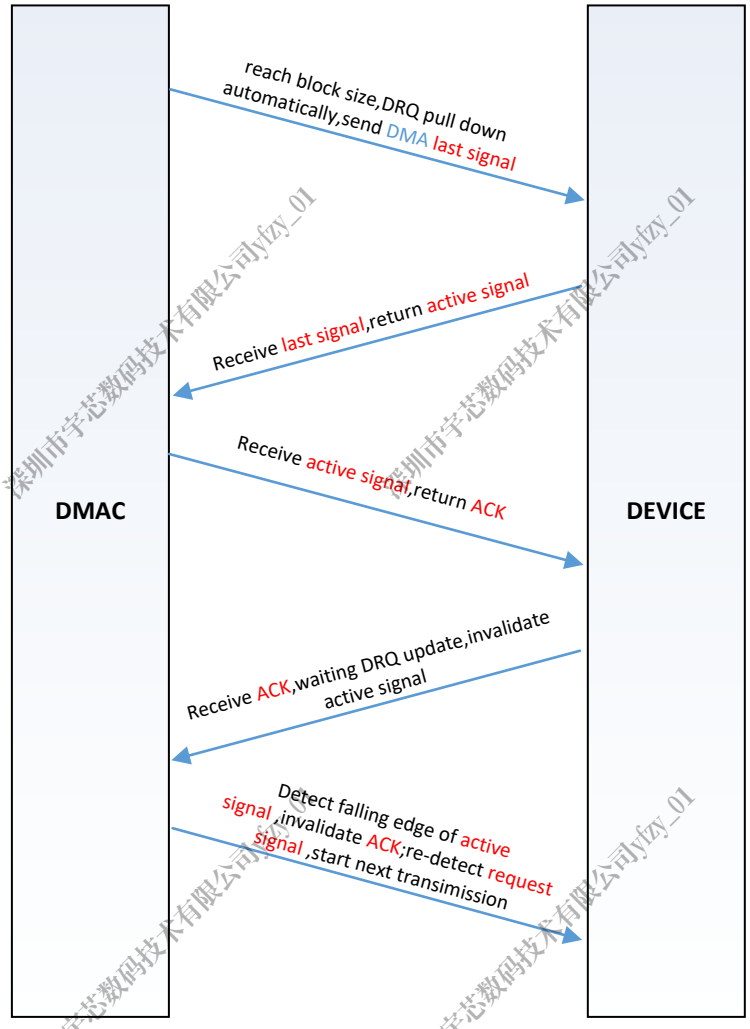


Figure 3-23. DMA Transfer Mode

3.9.3.8. Auto-alignment Function

The DMA supports address alignment of non-IO devices, that is when the start address of non-IO devices is non 32-byte aligned, DMA firstly aligns the burst transfer within 32-byte to 32-byte. If the device of a DMA channel is configured to non-IO type, and the start address is 0x86, then DMA firstly aligns 26-byte burst transfer to 0xA0, then DMA transfers by 64-byte burst(maximum transfer amount of MBUS allowed). The address alignment function helps to improve the DRAM access efficiency.

IO devices does not support address alignment, so the bit width of IO devices must match the address offset, or not DMA ignores the non-consistency and indirectly transmits data of the corresponding bit width to the address.

3.9.3.9. Operating Mode

3.9.3.9.1. Clock Control

- The DMA clock is synchronous with AHB1 clock. Make sure that open the DMA gating bit of AHB1 clock before access DMA register.
- The reset input signal of DMA is asynchronous with AHB1, and is low valid by default. Make sure that de-assert the reset signal of DMA before DMA register accesses.
- To avoid indefinite state within registers, firstly de-assert the reset signal, secondly open the gating bit of AHB1.
- DMA has the function of clock auto gating, DMA clock can be disabled in DMA idle state using software to reduce power consumption. DMA enables clock auto gating by default.

3.9.3.9.2. DMA Transfer Process

The DMA transfer process is as follows.

(1) Request DMA channel, and judge the idle state of the channel by the enable or disable of DMA channel.

(2) Write the descriptor with 6-word into memory, the descriptor must be word-aligned. Refer to 3.10.3.4 DMA descriptor in detail.

(3) Write the start address of storing descriptor to **DMA_DESC_ADDR_REG**.

(4) Enable DMA channel, and write the corresponding channel to **DMA_EN_REG**.

(5) DMA obtains the descriptor information.

(6) Start to transmit a package ,when half package is completed, DMA sends **Half Package Transfer Interrupt**; when total package is completed, DMA sends **Package End Transfer Interrupt**. These interrupt status can be read by **DMA_IRQ_PEND_REG**.

(7) Set **DMA_PAU_REG** to pause or resume the data transfer.

(8) After completed the total package transfer, DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; if the link is other value, the next package starts to transmit. When the transfer ends, DMA sends **Queue End Transfer Interrupt**.

(9) Disable the DMA channel.

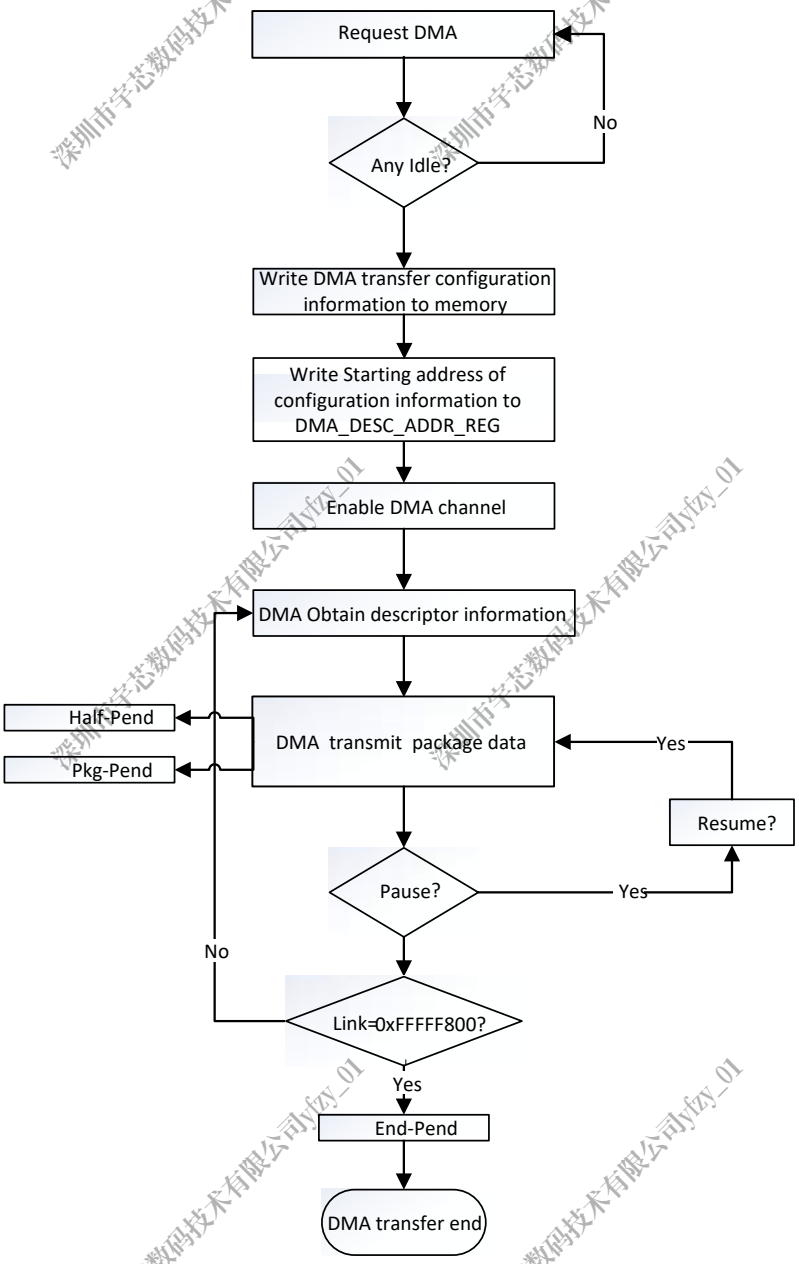


Figure 3-24. DMA Transfer Process

3.9.3.9.3. DMA Interrupt

(1) Enable interrupt: write the corresponding interrupt enable of DMA_IRQ_EN_REG, when the corresponding interrupt condition is satisfied,the corresponding interrupt generates.

(2) After enter the interrupt process, write DMA_IRQ_PEND_REG to clear the interrupt pending, and execute the process of waiting for the interrupt.

(3) Resume the interrupt and continue to execute the interrupted process.

3.9.4. Programming Guidelines

(1) The transfer width of IO type device is consistent with the offset of start address.

(2) MBUS protocol does not support read operation of non-integer word, so for non-integer word read operation, device must ignore redundant inconsistent data between data width and configuration, that is, the device of non-integer word must interpret DMA demand through its FIFO width instead of read demand width.

(3) When the DMA transfer is paused, this is equivalent to invalid DRQ. Because DMA transfer command has a certain time delay, DMA will not stop transfer immediately until the current command and the command in Arbiter finished, at most 32byte data.

DMA application example :

```
writel(0x00000000, mem_address + 0x00);   //Setting configuration, mem_address must be word-aligned
writel(0x00001000, mem_address + 0x04);    // Setting the start address for the source device
writel(0x20000000, mem_address + 0x08);   //Setting the start address for the destination device
writel(0x00000020, mem_address + 0x0C);   // Setting data package size
writel(0x00000000, mem_address + 0x10);   //Setting parameter
writel(0xFFFFF800, mem_address + 0x14);          //Setting the start address for the next descriptor
writel(mem_address, 0x01C02000+ 0x100 + 0x08); //Setting the start address for the DMA channel0 descriptor
do{
If(mem_address == readl(0x01C02000 + 0x100 + 0x08));
break;
}while(1);              //Make sure writing operation valid
writel(0x000000001, 0x01C02000 + 0x100 + 0x00);      // Enable DMA channel0 transfer
```

DMA supports increasing data package in transfer, there are a few points to note here.

- When the value of **DMA Channel Descriptor Address Register** is 0xFFFFF800, it indicates that DMA channel has got back the descriptor of the last package. When DMA channel completed the package data transfer, DMA channel will stop automatically data transfer.
- If needing increase data package,then at first it is essential to judge that whether DMA channel has got back the descriptor of the last package, if DMA channel has got back the descriptor of the last package, then this is impossible for increasing data package, DMA channel need start again. If DMA is not transmitting the last package,then the last descriptor address 0xFFFFF800 can be changed to the start address of the next descriptor.
- To ensure that the data changed valid, we can read again the value of **DMA Channel Descriptor Address Register** after changed the data. If there is not 0xFFFFF800,then it indicates that increasing data package is succeed, and fail otherwise. Because the process of increasing data package need some time, during this time,DMA channel may get back the descriptor of the last package.At the moment we can read again **DMA Channel Current Source Address Register** and **DMA Channel Current Destination Address Register**, if the increasing memory address accords with the information of the increasing data package, then the increasing data package is succeed, and fail otherwise.
- To ensure the higher success rate, it is suggested that increase data package before half package interrupt of penultimate data package.

3.9.5. Register List

Module Name	Base Address
DMA	0x03002000

Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0000	DMA IRQ Enable Register 0
DMA_IRQ_EN_REG1	0x0004	DMA IRQ Enable Register 1

DMA_IRQ_PEND_REG0	0x0010	DMA IRQ Pending Register 0
DMA_IRQ_PEND_REG1	0x0014	DMA IRQ Pending Register 1
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_EN_REG	0x0100+N*0x0040	DMA Channel Enable Register (N=0~15)
DMA_PAU_REG	0x0100+N*0x0040+0x0004	DMA Channel Pause Register(N=0~15)
DMA_DESC_ADDR_REG	0x0100+N*0x0040+0x0008	DMA Channel Start Address Register(N=0~15)
DMA_CFG_REG	0x0100+N*0x0040+0x000C	DMA Channel Configuration Register(N=0~15)
DMA_CUR_SRC_REG	0x0100+N*0x0040+0x0010	DMA Channel Current Source Register(N=0~15)
DMA_CUR_DEST_REG	0x0100+N*0x0040+0x0014	DMA Channel Current Destination Register(N=0~15)
DMA_BCNT_LEFT_REG	0x0100+N*0x0040+0x0018	DMA Channel Byte Counter Left Register(N=0~15)
DMA_PARA_REG	0x0100+N*0x0040+0x001C	DMA Channel Parameter Register(N=0~15)
DMA_MODE_REG	0x0100+N*0x0040+0x0028	DMA Mode Register(N=0~15)
DMA_FDESC_ADDR_REG	0x0100+N*0x0040+0x002C	DMA Former Descriptor Address Register(N=0~15)
DMA_PKG_NUM_REG	0x0100+N*0x0040+0x0030	DMA Package Number Register(N=0~15)

3.9.6. Register Description

3.9.6.1. DMA IRQ Enable Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN

			DMA 6 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable 0: Disable

			1: Enable
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable 0: Disable 1: Enable

3.9.6.2. **DMA IRQ Enable Register1 (Default Value: 0x0000_0000)**

Offset: 0x0004			**Register Name: DMA_IRQ_EN_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA15_QUEUE_IRQ_EN DMA 15 Queue End Transfer Interrupt Enable 0: Disable 1: Enable

29	R/W	0x0	DMA15_PKG_IRQ_EN DMA 15 Package End Transfer Interrupt Enable 0: Disable 1: Enable
28	R/W	0x0	DMA15_HLAF_IRQ_EN DMA 15 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA14_QUEUE_IRQ_EN DMA 14 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
25	R/W	0x0	DMA14_PKG_IRQ_EN DMA 14 Package End Transfer Interrupt Enable 0: Disable 1: Enable
24	R/W	0x0	DMA14_HLAF_IRQ_EN DMA 14 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA13_QUEUE_IRQ_EN DMA 13 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
21	R/W	0x0	DMA13_PKG_IRQ_EN DMA 13 Package End Transfer Interrupt Enable 0: Disable 1: Enable
20	R/W	0x0	DMA13_HLAF_IRQ_EN DMA 13 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA12_QUEUE_IRQ_EN DMA 12 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	DMA12_PKG_IRQ_EN DMA 12 Package End Transfer Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	DMA12_HLAF_IRQ_EN DMA 12 Half Package Transfer Interrupt Enable 0: Disable

			1: Enable
15	/	/	/
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11 Package End Transfer Interrupt Enable 0: Disable 1: Enable
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA 10 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA 10 Package End Transfer Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	DMA10_HLAF_IRQ_EN DMA 10 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA9_QUEUE_IRQ_EN DMA 9 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA 9 Package End Transfer Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA 9 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA 8 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	DMA8_PKG_IRQ_EN

			DMA 8 Package End Transfer Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	DMA8_HLAF_IRQ_EN DMA 8 Half Package Transfer Interrupt Enable 0: Disable 1: Enable

3.9.6.3. **DMA IRQ Pending Status Register 0 (Default Value: 0x0000_0000)**

Offset:0x0010			**Register Name: DMA_IRQ_PEND_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND DMA 7 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND DMA 7 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND DMA 6 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA6_PKG_IRQ_ PEND DMA 6 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND DMA 6 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/

22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND DMA 5 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA5_PKG_IRQ_ PEND DMA 5 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND DMA 5 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND DMA 4 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_ PEND DMA 4 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND DMA 4 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND DMA 3 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
13	R/W1C	0x0	DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND DMA 3 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect

			1: Pending
11	/	/	/
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND DMA 2 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND DMA 2 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND DMA 1 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND DMA 1 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND DMA 0 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_ PEND DMA 0 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND DMA 0 Half Package Transfer Interrupt Pending. Setting 1 to the bit will

			clear it. 0: No effect 1: Pending

3.9.6.4. **DMA IRQ Pending Status Register 1 (Default Value: 0x0000_0000)**

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA15_QUEUE_IRQ_PEND DMA 15 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA15_PKG_IRQ_PEND DMA 15 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA14_HLAF_IRQ_PEND DMA 14 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA14_QUEUE_IRQ_PEND DMA 14 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA14_PKG_IRQ_PEND DMA 14 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA14_HLAF_IRQ_PEND DMA 14 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA13_QUEUE_IRQ_PEND DMA 13 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect

			1: Pending
21	R/W1C	0x0	DMA13_PKG_IRQ_PEND DMA 13 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA13_HLAF_IRQ_PEND DMA 13 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA12_QUEUE_IRQ_PEND DMA 12 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA12_PKG_IRQ_PEND DMA 12 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA12_HLAF_IRQ_PEND DMA 12 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA11_QUEUE_IRQ_PEND DMA 11 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
13	R/W1C	0x0	DMA11_PKG_IRQ_PEND DMA 11 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA11_HLAF_IRQ_PEND DMA 11 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA10_QUEUE_IRQ_PEND DMA 10 Queue End Transfer Interrupt Pending. Setting 1 to the bit will

			clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA10_PKG_IRQ_PEND DMA 10 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA10_HLAF_IRQ_PEND DMA 10 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA9_QUEUE_IRQ_PEND DMA 9 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA9_PKG_IRQ_PEND DMA 9 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA9_HLAF_IRQ_PEND DMA 9 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA8_QUEUE_IRQ_PEND DMA 8 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA8_PKG_IRQ_PEND DMA 8 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA8_HLAF_IRQ_PEND DMA 8 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

3.9.6.5. DMA Auto Gating Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT DMA MCLK interface circuit auto gating bit 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT DMA common circuit auto gating bit 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT DMA channel circuit auto gating bit 0: Auto gating enable 1: Auto gating disable

NOTE

When initializing DMA Controller, the bit2 of DMA_AUTO_GATE_REG should be set up.

3.9.6.6. DMA Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R	0x0	MBUS FIFO Status 0: Empty 1: Not Empty
29:16	/	/	/
15	R	0x0	DMA15_STATUS DMA Channel 15 Status 0: Idle 1: Busy
14	R	0x0	DMA14_STATUS DMA Channel 14 Status 0: Idle 1: Busy
13	R	0x0	DMA13_STATUS DMA Channel 13 Status 0: Idle 1: Busy
12	R	0x0	DMA12_STATUS DMA Channel 12 Status 0: Idle

			1: Busy
11	R	0x0	DMA11_STATUS DMA Channel 11 Status 0: Idle 1: Busy
10	R	0x0	DMA10_STATUS DMA Channel 10 Status 0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status 0: Idle 1: Busy
7	R	0x0	DMA7_STATUS DMA Channel 7 Status 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS

			DMA Channel 0 Status 0: Idle 1: Busy

3.9.6.7. **DMA Channel Enable Register (Default Value: 0x0000_0000)**

Offset:0x0100+N*0x0040+0x0000(N=0~15)			Register Name: DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_EN DMA Channel Enable 0: Disable 1: Enable

3.9.6.8. **DMA Channel Pause Register (Default Value: 0x0000_0000)**

Offset:0x0100+N*0x0040+0x0004(N=0~15)			Register Name: DMA_PAU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE Pausing DMA Channel Transfer Data 0: Resume Transferring 1: Pause Transferring

3.9.6.9. **DMA Channel Descriptor Address Register (Default Value: 0x0000_0000)**

Offset:0x0100+N*0x0040+0x0008(N=0~15)			Register Name: DMA_DESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMA_DESC_ADDR DMA Channel Descriptor Address The Descriptor Address must be word-aligned.

3.9.6.10. **DMA Channel Configuration Register (Default Value: 0x0000_0000)**

Offset:0x0100+N*0x0040+0x000C(N=0~15)			Register Name: DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH DMA Destination Data Width 00: 8-bit 01: 16-bit 10: 32-bit

			11: 64-bit
24	R	0x0	DMA_ADDR_MODE DMA Destination Address Mode 0: Linear Mode 1: IO Mode
23:22	R	0x0	DMA_DEST_BLOCK_SIZE DMA Destination Block Size 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH DMA Source Data Width 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	R	0x0	DMA_SRC_ADDR_MODE DMA Source Address Mode 0: Linear Mode 1: IO Mode
7:6	R	0x0	DMA_SRC_BLOCK_SIZE DMA Source Block Size 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

3.9.6.11. **DMA Channel Current Source Address Register (Default Value: 0x0000_0000)**

Offset:0x0100+N*0x0040+0x0010(N=0~15)			**Register Name: DMA_CUR_SRC_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_SRC DMA Channel Current Source Address, read only.

3.9.6.12. DMA Chacnnel Current Destination Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0014(N=0~15)			Register Name: DMA_CUR_DEST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_DEST DMA Channel Current Destination Address, read only.

3.9.6.13. DMA Channel Byte Counter Left Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0018(N=0~15)			Register Name: DMA_BCNT_LEFT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT DMA Channel Byte Counter Left, read only.

3.9.6.14. DMA Channel Parameter Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x001C(N=0~15)			Register Name: DMA_PARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	WAIT_CYC Wait Clock Cycles

3.9.6.15. DMA Mode Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0028(N=0~15)			Register Name: DMA_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	DMA_DST_MODE 0: Wait mode 1: Handshake mode
2	R/W	0x0	DMA_SRC_MODE 0: Wait mode 1: Handshake mode
1:0	/	/	/

3.9.6.16. DMA Former Descriptor Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x002C(N=0~15)			Register Name: DMA_FDESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_FDESC_ADDR

			This register is used to store the former value of DMA Channel Descriptor Address Register.

3.9.6.17. **DMA Package Number Register (Default Value: 0x0000_0000)**

Offset:0x0100+N*0x0040+0x0030(N=0~15)			Register Name: DMA_PKG_NUM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_PKG_NUM This register will record the number of packages which has been completed in one transmission.

3.10. RTC

3.10.1. Overview

The RTC(Real Time Clock) is used to display the real time and periodically wakeup .The RTC can display the year, month, day, week, hour, minute, second in real time. The RTC has the independent power to continue to work in system power-off. The RTC has the following features:

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32768Hz low-frequency oscillator for count clock
- Configurable initial value by software anytime
- Periodically alarm to wakeup the external devices
- Stores power-off information in eight 32-bit general purpose register

3.10.2. Block Diagram

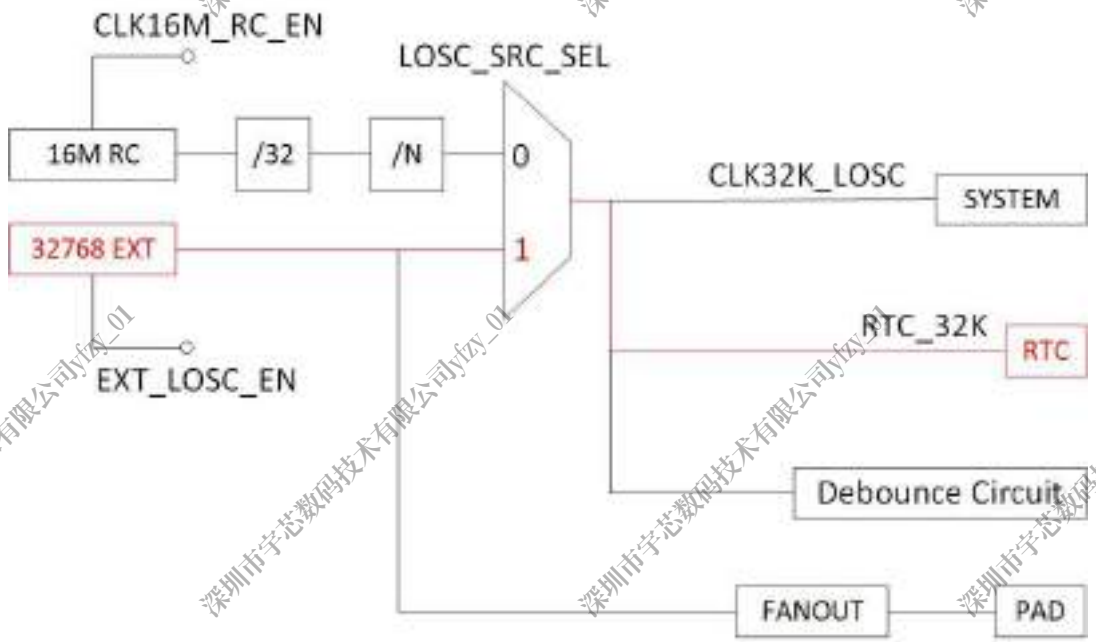


Figure 3-25. RTC Clock Tree

RTC Clock tree can be selected by corresponding switch, including RC16M and EXT32K.
Clock sources: 32768Hz low-frequency crystal oscillator, internal 16MHz RC.
Output clock: CLK32K_LOSC, RTC_32K.

3.10.3. Operations and Functional Descriptions

3.10.3.1. **External Signals**

Table 3-9. RTC External Signals

Signal	Description
X32KIN	32.768kHz oscillator input
X32KOUT	32.768kHz oscillator output
X32KFOUT	32.768kHz clock fanout, provides low frequency clock for external devices
NMI	Alarm wakeup generates low level into NMI
RTC-VIO	RTC low voltage,generated via internal LDO
VCC-RTC	RTC high voltage,generated via external power

3.10.3.2. Clock and Reset

The RTC module has the independent reset signal, the signal follows VCC-RTC. When VCC-RTC powers on, the reset signal resets the RTC module; after VCC-RTC reaches stable, the reset signal always holds high level.
The RTC module accesses its register by APB1.

3.10.3.3. Typical Application

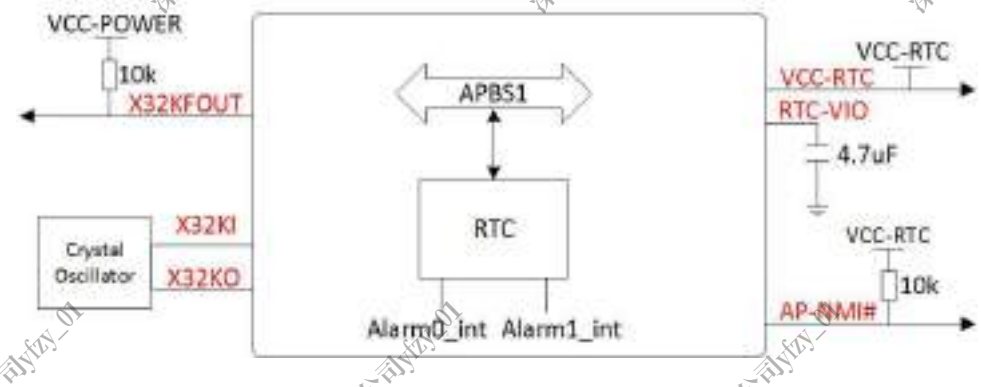


Figure 3-26. RTC Application Diagram

The system accesses RTC register by APB1 to generate the real time.
The external low-frequency oscillator must be 32.768kHz.
If the external devices need low-frequency oscillator, X32KFOUT can provide.
AP-NMI# and alarm0 in common generate low level signal.

3.10.3.4. Function Implementation

3.10.3.4.1. Clock Sources

The RTC has two clock sources: internal RC , external low frequency oscillator.
The internal RC can change RTC clock by changing division ratio ;the external clock can not change clock.
The RTC selects the internal RC by default, when the system starts, the RTC can select by software the external low frequency oscillator to provide much accuracy clock.
The clock accurate of the RTC is related to the accurate of the external low frequency oscillator. The external oscillator usually selects 32.768kHz oscillator with ±20ppm frequency tolerance.

3.10.3.4.2. Real Time Clock

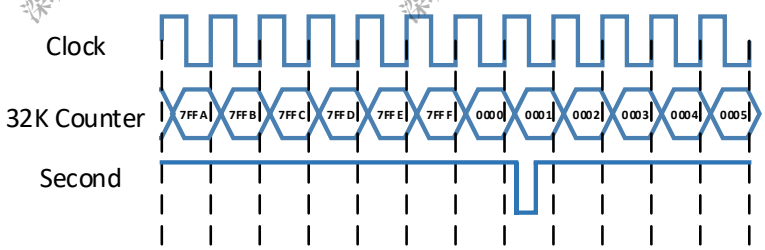


Figure 3-27. RTC Counter

The 32K counter adds 1 on each rising edge of the clock. When the clock number reaches 0x8000,32KHz counter starts to count again from 0, and the second counter adds 1. The 32KHz counter block diagram is as follows.

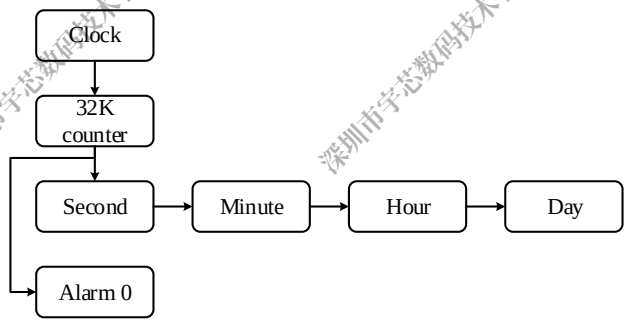


Figure 3-28. RTC 32768Hz Counter Block Diagram

According to above implementation, the changing range of each counter is as follows.

Table 3-10. RTC Counter Changing Range

Counter	Range
Second	If the counter value is not in the range from 0 to 59, then the counter value can change to 59 automatically.
Minute	If the counter value is not in the range from 0 to 59, then the counter value can change to 59 automatically.
Hour	If the counter value is not in the range from 0 to 23, then the counter value can change to 23 automatically.
Day	If the counter value is not in the range from 1 to 31, then the counter value can change to the maximum value of that month automatically.

3.10.3.4.3. Alarm 0

The principle of alarm0 is similar to the second counter, the difference is that alarm0 is a 32-bit down counter. When the counter decreases to 0 from the initial value, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.

3.10.3.4.4. Power-off Storage

The RTC provides eight 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, CPU can judge software process by the storing information.

3.10.3.4.5. RTC_VIO

The RTC module has a LDO ,the input source of the LDO is VCC-RTC,the output of the LDO is RTC-VIO,the value of RTC-VIO is adjustable,it is mainly used for internal digital logic.

3.10.3.5. **Operating Mode**

3.10.3.5.1. RTC Clock Control

(1) Select clock source: Select clock source by the bit0 of **LOSC_CTRL_REG**, the clock source is the internal RC oscillator by default, when the system starts, the clock source can be switched to the external 32K oscillator by software.
(2) Auto switch: After enabled the bit[14] of **LOSC_CTRL_REG**, the RTC automatically switches clock source to the internal oscillator when the external oscillator could not output waveform, the switch status can query by the bit[1] of **LOSC_AUTO_SWT_STA_REG**.
(3) After auto switch is valid, the clock source status bit cannot be changed, because the two functions are independent.

3.10.3.5.2. RTC Calendar

(1) Write time initial value: Write the current time to **RTC_DAY_REG** and **RTC_DAY_REG**.
(2) After update time, the RTC restarts to count again .The software can read the current time anytime.
(3) The leap year function can be set only by the software.

3.10.3.5.3. Alarm0

(1) Enable alram0 interrupt by writing **ALARM0_IRQ_EN**.
(2) Set the counter initial value, write the count-down second number to **ALARM0_COUNTER_REG**.
(3) Enable alarm0 function by writing **ALARM0_ENABLE_REG**, then the software can query alarm count value in real time.
(4) After enter the interrupt process, write **ALARM0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(5) Resume the interrupt and continue to execute the interrupted process.
(6) Power-off wakeup is generated via SoC hardware and PMIC, software only need set pending condition of alarm0, and set 1 to **ALARM0_CONFIG_REG**.

3.10.3.5.4. Fanout

The bit0 of **LOSC_OUT_GATING_REG** is set to 1, and external pull-up resistor and voltage is normal, then 32.768kHz square wave can be output.

3.10.3.5.5. Pad Hold

When the corresponding bit of **GPL_HOLD_OUTPUT_REG** is set to 1, the corresponding pin can hold in stable state(high level,low level or high impedance). The function is used to prevent output pin from changing when corresponding power changes.

3.10.3.5.6. RC Calibration Usage Scenario

Power-on: Select non-accurate 32kHz clock divided by internal RC.
Normal scenario: RTC can select 32kHz clock divided by 24MHz, or use calibration clock.If there has fanout requirement, then calibration clock is needed.
Standby or power-off scenario: Select accurate 32kHz generated by DCXO24M calibrates RC clock.

3.10.4. Programming Guidelines

3.10.4.1. RTC Clock Sources Setting

Configure **LOSC_CTRL_REG** to set RTC clock source.

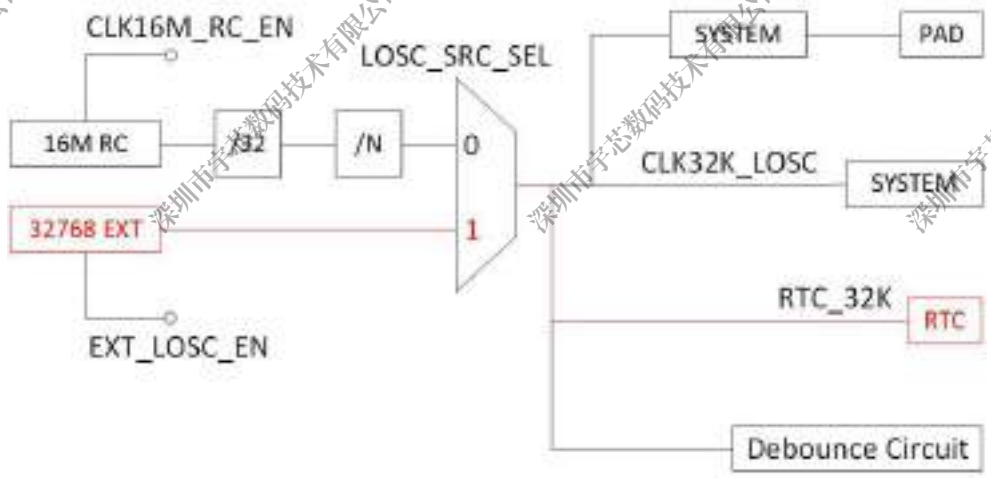


Figure 3-29. Selecting External Clock

For example: select external 32kHz clock source as RTC clock.

```
writel(0x16aa4000,LOSC_CTRL);      //writing key field
writel(0x16aa4001,LOSC_CTRL);      //select external 32K clock
```


3.10.4.2. **Real Time Clock**

```
RTC_DAY_REG = 0x00000015;
RTC_HH_MM_SS_REG = 0x00070809;//0000 0000 000|0 0000(Hour) 00|00 0000(Minute) 00|00 0000(Second)
Read (RTC_DAY_REG);
Read (RTC_HH_MM_SS_REG);
```

3.10.4.3. **Alarm 0**

```
irq_request(GIC_SRC_R_Alarm0,Alm0_handler);
irq_enable(GIC_SRC_R_Alarm0);
writel(1,ALM0_COUNTER);                    //set 1 seconds corresponding to normal mode.
writel(1,ALM0_EN);
writel(1,ALM_CONFIG); //NMI output
while(!readl(ALM0_IRQ_STA));
writel(1,ALM0_IRQ_EN);
while(readl(ALM0_IRQ_STA));
```

3.10.5. Register List

Module Name	Base Address
RTC	0x07000000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0000	Low Oscillator Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
RTC_DAY_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_COUNTER_REG	0x0020	Alarm 0 Counter Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM_CONFIG_REG	0x0050	Alarm Configuration Register
LOSC_OUT_GATING_REG	0x0060	LOSC Output Gating Register
GP_DATA_REG	0x0100 + N*0x04	General Purpose Register (N=0~7)
DCXO_CTRL_REG	0x0160	DCXO Control Register
GPL_HOLD_OUTPUT_REG	0x0180	GPL Hold Output Register
RTC_PWR_MODE_SEL_REG	0x0188	RTC POWER MODE SELECT Register
RTC_VIO_REG	0x0190	RTC_VIO Regulate Register
IC_CHARA_REG	0x1F0	IC Characteristic Register
CRY_CONFIG_REG	0x0210	Crypt Configuration Register
CRY_KEY_REG	0x0214	Crypt Key Register

CRY_EN_REG	0x0218	Crypt Enable Register

3.10.6. Register Description

3.10.6.1. LOSC Control Register (Default Value: 0x0000_4010)

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15	/	/	/
14	R/W	0x1	LOSC_AUTO_SWT_EN LOSC Auto Switch Enable 0: Disable 1: Enable
13:10	/	/	/
9	R/W	0x0	ALM_DDHHMMSS_ACCE ALARM DD-HH-MM-SS access After writing the Alarm Week HH-MM-SS Register, this bit is set and it will be cleared until the real writing operation is finished.
8	R/W	0x0	RTC_HHMMSS_ACCE RTC HH-MM-SS access After writing the RTC HH-MM-SS Register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS Register, the RTC HH-MM-SS Register will be refreshed for at most one seconds.
7	R/W	0x0	RTC_YYMMDD_ACCE RTC YY-MM-DD access After writing the RTC YY-MM-DD Register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD Register, the RTC YY-MM-DD Register will be refreshed for at most one seconds.
6:5	/	/	/
4	R/W	0x1	EXT_LOSC_EN External 32768Hz Crystal Enable 0: Disable 1: Enable
3:2	R/W	0x0	EXT_LOSC_GSM External 32768Hz Crystal GSM 00: Low 01: / 10: / 11 High

1	/	/	/
0	R/W	0x0	LOSC_SRC_SEL LOSC Clock source Select. 'N' is the value of Internal OSC Clock Prescalar Register. 0: Low Frequency Clock from 16M RC 1: External 32.768kHz OSC

NOTE

If the bit[9:7] of LOSC_CTRL_REG is set, the corresponding of Alarm 1 Week HH-MM-SS Register, RTC HH-MM-SS Register, RTC YY-MM-DD Register cannot be written.

3.10.6.2. **LOSC Auto Switch Status Register (Default Value: 0x0000_0000)**

Offset:0x0004			**Register Name: LOSC_AUTO_SWT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA 0: External 32.768kHz OSC work normally 1: External 32.768kHz OSC work abnormally
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND LOSC auto switch pending 0: No effect 1: Auto switches pending Setting 1 to this bit will clear it.
0	R	0x0	LOSC_SRC_SEL_STA Checking LOSC Clock Source Status. 'N' is the value of Internal OSC Clock Prescalar Register. 0: Low Frequency Clock from 16M RC 1: External 32.768kHz OSC

3.10.6.3. **Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)**

Offset:0x0008			**Register Name: INTOSC_CLK_PRESCAL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0xF	INTOSC_CLK_PRESCAL. Internal OSC Clock Prescalar value N. 00000: 1 00001: 2 00010: 3 ..... 11111: 32

3.10.6.4. **RTC YY-MM-DD Register**

Offset:0x0010			Register Name: RTC_DAY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	UDF	DAY Day Range from 1~65535.

3.10.6.5. **RTC HH-MM-SS Register**

Offset:0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR Range from 0~23
15:14	/	/	/
13:8	R/W	UDF	MINUTE Range from 0~59
7:6	/	/	/
5:0	R/W	UDF	SECOND Range from 0~59

NOTE

If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

3.10.6.6. **Alarm 0 Day setting Register (Default Value: 0x0000_0000)**

Offset:0x0020			Register Name: ALARM0_COUNTER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is Based on Day.

NOTE

If the day is set to 0, it will be 1 day in fact.

3.10.6.7. **Alarm 0 HH-MM-SS setting Register**

Offset:0x0024	Register Name: ALARM0_CUR_VLU_REG

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	x	HOUR. Range from 0~23
15:14	/	/	/
13:8	R/W	x	MINUTE. Range from 0~59
7:6	/	/	/
5:0	R/W	x	SECOND. Range from 0~59

3.10.6.8. **Alarm 0 Enable Register (Default Value: 0x0000_0000)**

Offset:0x0028			Register Name: ALARM0_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable If this bit is set to “1”, the valid bits of Alarm 0 Counter Register will down count to zero, and the alarm pending bit will be set to “1”. 0: Disable 1: Enable

3.10.6.9. **Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)**

Offset:0x002C			Register Name: ALARM0_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable 0: Disable 1: Enable

3.10.6.10. **Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)**

Offset:0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND

			Alarm 0 IRQ Pending bit 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.10.6.11. **Alarm Configuration Register (Default Value: 0x0000_0000)**

Offset:0x0050			**Register Name: ALARM_CONFIG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

3.10.6.12. **LOSC Output Gating Register (Default Value: 0x0000_0000)**

Offset:0x0060			**Register Name: LOSC_OUT_GATING_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	LOSC_OUT_GATING Configuration of LOSC output, and without LOSC output by default. 0: Disable LOSC output gating 1: Enable LOSC output gating

3.10.6.13. **General Purpose Register (Default Value: 0x0000_0000)**

Offset:0x0100+N*0x0004 (N=0~7)			**Register Name: GP_DATA_REGN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	GP_DATA Data [31:0]

NOTE

General purpose register 0~7 value can be stored if the RTC-VIO is larger than 1.0V.

3.10.6.14. **DCXO Control Register (Default Value: 0x083F_10F2)**

Offset:0x0160	**Register Name: DCXO_CTRL_REG**

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CLK_REQ_ENB. 0: enable DCXO wake up function 1: disable DCXO wake up function
30:28	/	/	/
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value
23	/	/	/
22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value Capacity cell is 55fF
15:13	/	/	/
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal, active high
6	R/W	0x1	XTAL_MODE Xtal mode enable signal, active high 0: For external clk input mode 1: For normal mode
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO rfclk enhance Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5pF, 0x1 for 10pF, 0x2 for 15pF, 0x3 for 20Pf.
3:2	/	/	/
1	R/W	0x1	DCXO_EN DCXO enable 1: Enable 0: Disable
0	R/W	0x1	CLK16M_RC_EN 1: enable 0: disable

3.10.6.15. **GPL Hold Output Register (Default Value: 0x0000_0000)**

Offset:0x0180			Register Name: GPL_HOLD_OUTPUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	GPL12_HOLD_OUTPUT Hold the output of GPIOL12 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable

			1: Hold enable
11	R/W	0x0	GPL11_HOLD_OUTPUT Hold the output of GPIOL11 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
10	R/W	0x0	GPL10_HOLD_OUTPUT Hold the output of GPIOL10 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
9	R/W	0x0	GPL9_HOLD_OUTPUT Hold the output of GPIOL9 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
8	R/W	0x0	GPL8_HOLD_OUTPUT Hold the output of GPIOL8 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
7	R/W	0x0	GPL7_HOLD_OUTPUT Hold the output of GPIOL7 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
6	R/W	0x0	GPL6_HOLD_OUTPUT Hold the output of GPIOL6 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
5	R/W	0x0	GPL5_HOLD_OUTPUT Hold the output of GPIOL5 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
4	R/W	0x0	GPL4_HOLD_OUTPUT Hold the output of GPIOL4 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other output may not hold

			on. 0: Hold disable 1: Hold enable
3	R/W	0x0	GPL3_HOLD_OUTPUT Hold the output of GPIOL3 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
2	R/W	0x0	GPL2_HOLD_OUTPUT Hold the output of GPIOL2 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
1	R/W	0x0	GPL1_HOLD_OUTPUT Hold the output of GPIOL1 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
0	R/W	0x0	GPL0_HOLD_OUTPUT Hold the output of GPIOL0 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable

3.10.6.16. RTC Power Mode Select Register (Default Value: 0x0000_0001)

Offset:0x0188			Register Name: RTC_PWR_MODE_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	RTC_POW_MOD_SELECT VCC-RTC POWER MODE SELECT 0: 3.3V 1:1.8V

3.10.6.17. RTC_VIO Regulation Register (Default Value: 0x0000_0004)

Offset:0x0190			Register Name:RTC_VIO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:5	/	/	/
4	R/W	0x0	V_SEL. 0: resistance divider 1: band gap
3	/	/	/
2:0	R/W	0x4	RTC_VIO_REGU These bits are useful for regulating the RTC_VIO from 0.6V to 1.3V , and the regulation step is 0.1V. 000: 1.0V 001: 0.6V 010: 0.7V 011: 0.8V 100: 0.9V 101: 1.1V 110: 1.2V 111: 1.3V

3.10.6.18. **IC Characteristic Register (Default Value: 0x0000_0000)**

Offset:0x1F0			Register Name: IC_CHARA_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	IC_CHARA. Key Field. Should be written at value 0x16AA. Writing any other value in this field aborts the write operation.
15:0	R/W	0x0	ID_DATA. Return 0x16aa only if the KEY_FIELD is set as 0x16aa when read those bits, otherwise return 0x0.

3.10.6.19. **Crypto Configuration Register (Default Value: 0x0000_0000)**

Offset:0x0210			**Register Name: CRY_CONFIG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	KEY_FIELD Key Field If you want to read or write Crypt Key Register/Crypt Enable Register , you should write 0x1689 in these bits.

3.10.6.20. **Crypto Key Register (Default Value: 0x0000_0000)**

Offset:0x0214			**Register Name: CRY_KEY_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R/W	0x0	CRY_KEY Crypto Key

3.10.6.21. **Crypto Enable Register (Default Value: 0x0000_0000)**

Offset:0x0218			Register Name: CRY_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CRY_EN Crypto Enable

3.11. Thermal Sensor Controller

3.11.1. Overview

Thermal sensors have became common elements in wide range of modern system on chip (SOC) platform. Thermal sensors are used to constantly monitor the temperature on the chip.

The Thermal Sensor Controller(THS) embeds 4 thermal sensors, sensor0 for CPU,sensor1 for VE, sensor2 for ISP and sensor3 for DDR. The Thermal sensors can generate interrupt to SW to lower temperature via DVFS, on reaching a certain thermal threshold.

The THS has the following features:

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -25℃ to +125℃
- Power supply voltage:1.8V
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

3.11.2. Block Diagram

Figure 3-30 shows a block diagram of the Thermal Sensor Controller.

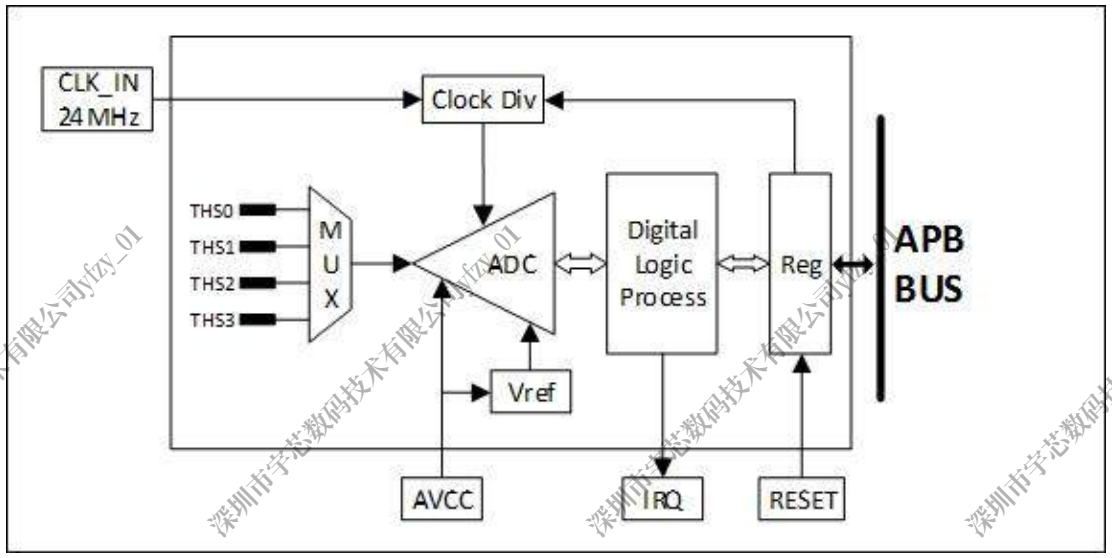


Figure 3-30. Thermal Sensor Controller Block Diagram

3.11.3. Operations and Functional Descriptions

3.11.3.1. **Clock Sources**

The THS gets one clock source. Table 3-11 describes the clock source for Thermal Sensor Controller. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 3-11. Thermal Sensor Controller Clock Sources

Clock Sources	Description
OSC24M	24MHz OSC

3.11.3.2. **Timing Requirements**

CLK_IN = 24MHz
CONV_TIME(Conversion Time) = 1/(24MHz/14Cycles) =0.583 (us)
TACQ> 1/(24MHz/24Cycles)
THERMAL_PER > ADC Sample Frequency > TACQ+CONV_TIME

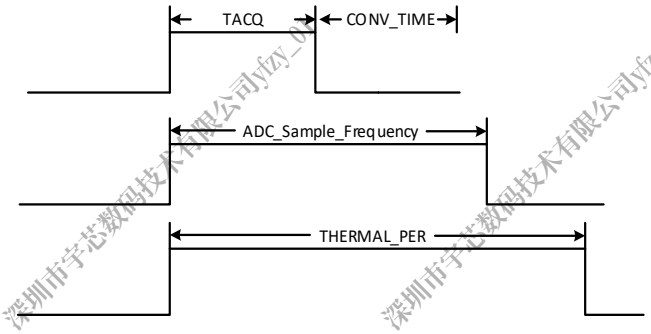


Figure 3-31. Thermal Sensor Time Requirement

3.11.3.3. **Interrupt**

The THS has four interrupt sources, such as DATA_IRQ , SHUTDOWN_IRQ,ALARM_IRQ and ALARM_OFF_IRQ. Figure 3-32 shows the thermal sensor interrupt sources.

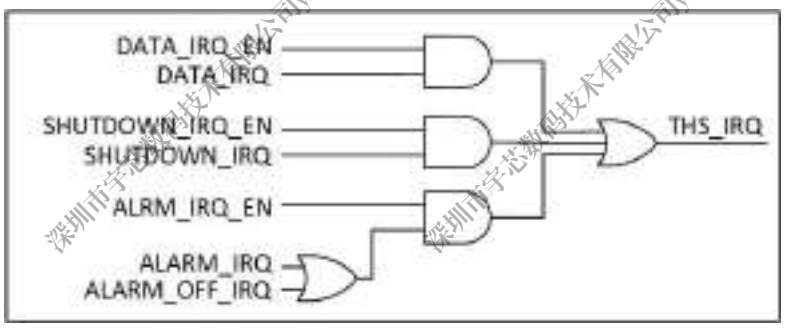


Figure 3-32. Thermal Sensor Controller Interrupt Source

When temperature is higher than Alarm_Threshold, ALARM_IRQ is generated. When temperature is lower than Alarm_Off_Thershold, ALARM_OFF_IRQ is generated. ALARM_OFF_IRQ is fall edge trigger.

3.11.4. Programming Guidelines

3.11.4.1. Initial Process

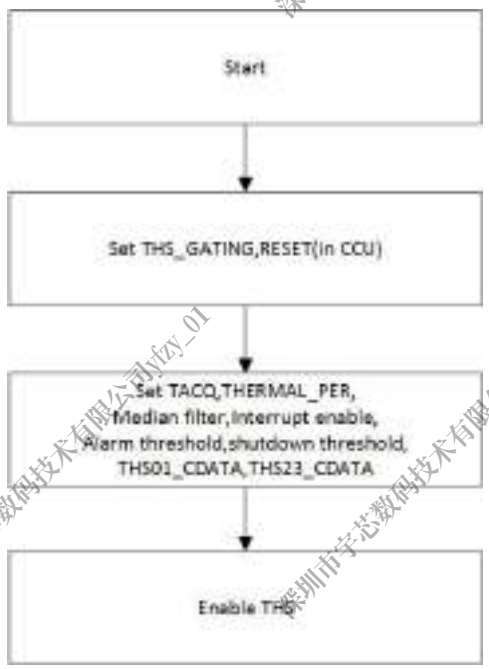


Figure 3-33. THS Initial Process

The formula of THS is y=-ax+b. In FT stage, THS is calibrated according to ambient temperature, the calibration value is written in EFUSE. Please refer to SID Spec about EFUSE information.
Before enabling THS, read EFUSE value and write the value to **THS01_CDATA, THS23_CDATA**.

3.11.4.2. Temperature Conversion Formula

T= (sensor_data - 2794)/(-14.882), the unit of T is Celsius.
sensor_data: read from sensor data register.

3.11.5. Register List

Module Name	Base Address
Thermal Sensor	0x05070400

Register Name	Offset	Description
THS_CTRL	0x0000	THS Control Register
THS_EN	0x0004	THS Enable Register
THS_PER	0x0008	THS Period Control Register
THS_DATA_INTC	0x0010	THS Data Interrupt Control Register
THS_SHUT_INTC	0x0014	THS Shut Interrupt Control Register
THS_ALARM_INTC	0x0018	THS Alarm Interrupt Control Register
THS_DATA_INTS	0x0020	THS Data Interrupt Status Register

THS_SHUT_INTS	0x0024	THS Shut Interrupt Status Register
THS_ALARMO_INTS	0x0028	THS Alarm Off Interrupt Status Register
THS_ALARM_INTS	0x002C	THS Alarm Interrupt Status Register
THS_FILTER	0x0030	THS Median Filter Control Register
THS0_ALARM_CTRL	0x0040	THS0 Alarm Threshold Control Register
THS1_ALARM_CTRL	0x0044	THS1 Alarm Threshold Control Register
THS2_ALARM_CTRL	0x0048	THS2 Alarm Threshold Control Register
THS3_ALARM_CTRL	0x004C	THS3 Alarm threshold Control Register
THS01_SHUTDOWN_CTRL	0x0080	THS0&1 Alarm Threshold Control Register
THS23_SHUTDOWN_CTRL	0x0084	THS2&3 Shutdown Threshold Control Register
THS01_CDATA	0x00A0	THS0&1 Calibration Data
THS23_CDATA	0x00A4	THS2&3 Calibration Data
THS0_DATA	0x00C0	THS0 Data Register
THS1_DATA	0x00C4	THS1 Data Register
THS2_DATA	0x00C8	THS2 Data Register
THS3_DATA	0x00CC	THS3 Data Register

3.11.6. Register Description

3.11.6.1. THS Control Register(Default Value : 0x01DF_002F)

Offset: 0x0000			Register Name: THS_CTRL
Bit	**Rear/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1DF (50kHz)	FS_DIV ADC Sample Frequency Divider CLK_IN/(N+1) (N > 0x17)
15:0	R/W	0x2F(2uS)	TACQ ADC Acquire Time CLK_IN/(n+1)

3.11.6.2. THS Enable Register(Default Value : 0x0000_0000)

Offset: 0x0004			Register Name: THS_EN
Bit	**Rear/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	THS3_EN Enable temperature measurement sensor3 0:Disable 1:Enable
2	R/W	0x0	THS2_EN Enable temperature measurement sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_EN

			Enable temperature measurement sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_EN Enable temperature measurement sensor0 0:Disable 1:Enable

3.11.6.3. **THS Period Control Register(Default Value: 0x0003_A000)**

Offset: 0x0008			**Register Name: THS_PER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x3A(10ms)	THERMAL_PER 4096*(n+1)/CLK_IN
11:0	/	/	/

3.11.6.4. **THS Data Interrupt Control Register(Default Value: 0x0000_0000)**

Offset: 0x0010			**Register Name: THS_DATA_INTC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	THS3_DATA_IRQ_EN Selects Temperature measurement data of sensor3 0:Disable 1:Enable
2	R/W	0x0	THS2_DATA_IRQ_EN Selects Temperature measurement data of sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_DATA_IRQ_EN Selects temperature measurement data of sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_DATA_IRQ_EN Selects temperature measurement data of sensor0 0:Disable 1:Enable

3.11.6.5. **THS Shut Interrupt Control Register(Default Value: 0x0000_0000)**

Offset: 0x0014			**Register Name: THS_SHUT_INTC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

3	R/W	0x0	SHUT_INT3_EN Selects shutdown interrupt for sensor3 0:Disable 1:Enable
2	R/W	0x0	SHUT_INT2_EN Selects shutdown interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	SHUT_INT1_EN Selects shutdown interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	SHUT_INT0_EN Selects shutdown interrupt for sensor0 0:Disable 1:Enable

3.11.6.6. **THS Alarm Interrupt Control Register(Default Value: 0x0000_0000)**

Offset: 0x0018			**Register Name: THS_ALARM_INTC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	ALARM_INT3_EN Selects Alarm interrupt for sensor3 0:Disable 1:Enable
2	R/W	0x0	ALARM_INT2_EN Selects Alarm interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	ALARM_INT1_EN Selects alarm interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	ALARM_INT0_EN Selects alarm interrupt for sensor0 0:Disable 1:Enable

3.11.6.7. **THS Data Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0020			**Register Name: THS_DATA_INTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

3	R/W1C	0x0	THS3_DATA_IRQ _STS Data interrupt status for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	THS2_DATA_IRQ_STS Data interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	THS1_DATA_IRQ_STS Data interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	THS0_DATA_IRQ_STS Data interrupt status for sensor0 Write '1' to clear this interrupt.

3.11.6.8. **THS Shut Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0024			**Register Name: THS_SHUT_INTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	SHUT_INT3_STS Shutdown interrupt status for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	SHUT_INT2_STS Shutdown interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	SHUT_INT1_STS Shutdown interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown interrupt status for sensor0 Write '1' to clear this interrupt .

3.11.6.9. **THS Alarm Off Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0028			**Register Name: THS_ALARMO_INTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	ALARM_ OFF3_STS Alarm interrupt off pending for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_OFF2_STS Alarm interrupt off pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_OFF1_STS Alarm interrupt off pending for sensor1

			Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_OFF0_STS Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt.

3.11.6.10. **THS Alarm Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x002C			Register Name: THS_ALARM_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	ALARM_INT3_STS Alarm interrupt pending for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_INT2_STS Alarm interrupt pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_INT1_STS Alarm interrupt pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_INT0_STS Alarm interrupt pending for sensor0 Write '1' to clear this interrupt.

3.11.6.11. **Median Filter Control Register(Default Value: 0x0000_0001)**

Offset: 0x0030			Register Name: THS_FILTER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE Average Filter Type 00: 2 01: 4 10: 8 11: 16

3.11.6.12. **THS0 Alarm Threshold Control Register(Default Value: 0x05A0_0684)**

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**

31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT Thermal Sensor0 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST Thermal Sensor0 alarm threshold for hysteresis temperature

3.11.6.13. **THS1 Alarm Threshold Control Register (Default Value: 0x05A0_0684)**

Offset: 0x0044			**Register Name: THS1_ALARM_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT Thermal Sensor1 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal Sensor1 alarm threshold for hysteresis temperature

3.11.6.14. **THS2 Alarm Threshold Control Register (Default Value: 0x05A0_0684)**

Offset: 0x0048			**Register Name: THS2_ALARM_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM2_T_HOT Thermal Sensor2 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM2_T_HYST Thermal Sensor2 alarm threshold for hysteresis temperature

3.11.6.15. **THS3 Alarm threshold Control Register (Default Value: 0x05A0_0684)**

Offset: 0x004C			**Register Name: THS3_ALARM_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM3_T_HOT Thermal sensor3 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM3_T_HYST Thermal sensor3 Alarm threshold for hysteresis temperature

3.11.6.16. **THS0&1 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)**

Offset: 0x0080			Register Name: THS01_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x4E9	SHUT1_T_HOT Thermal Sensor1 shutdown threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT Thermal Sensor0 shutdown threshold for hot temperature

3.11.6.17. **THS2&3 Shutdown Threshold Control Register (Default Value: 0x0000_04E9)**

Offset: 0x0084			Register Name: THS2_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x4E9	SHUT3_T_HOT Thermal sensor3 Shutdown Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT2_T_HOT Thermal Sensor2 shutdown threshold for hot temperature

3.11.6.18. **THS0&1 Calibration Data Register (Default Value: 0x0800_0800)**

Offset: 0x00A0			Register Name: THS01_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x800	THS1_CDATA Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA Thermal Sensor0 calibration data

3.11.6.19. **THS2&3 Calibration Data Register (Default Value: 0x0000_0800)**

Offset: 0x00A4			Register Name: THS2_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x800	THS3_CDATA Thermal Sensor3 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS2_CDATA Thermal Sensor2 calibration data

3.11.6.20. **THS0 Data Register(Default Value: 0x0000_0000)**

Offset: 0x00C0			Register Name: THS0_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS0_DATA Temperature measurement data of sensor0

3.11.6.21. **THS1 Data Register(Default Value: 0x0000_0000)**

Offset: 0x00C4			Register Name: THS1_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS1_DATA Temperature measurement data of sensor1

3.11.6.22. **THS2 Data Register(Default Value: 0x0000_0000)**

Offset: 0x00C8			Register Name: THS2_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS2_DATA Temperature measurement data of sensor2

3.11.6.23. **THS3 Data Register (Default Value: 0x0001_0000)**

Offset: 0x00CC			Register Name: THS3_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS3_DATA Temperature measurement data of sensor3

3.12. PSI

3.12.1. Overview

PSI（Peripheral System Interconnect）is a peripheral bus interconnect device based on AHB and APB protocol, which supports 16 AHB master and 16 slave bus. The type of slave bus can be AHB bus or APB bus. Each bus supports 64 slave devices.

3.12.2. Block Diagram

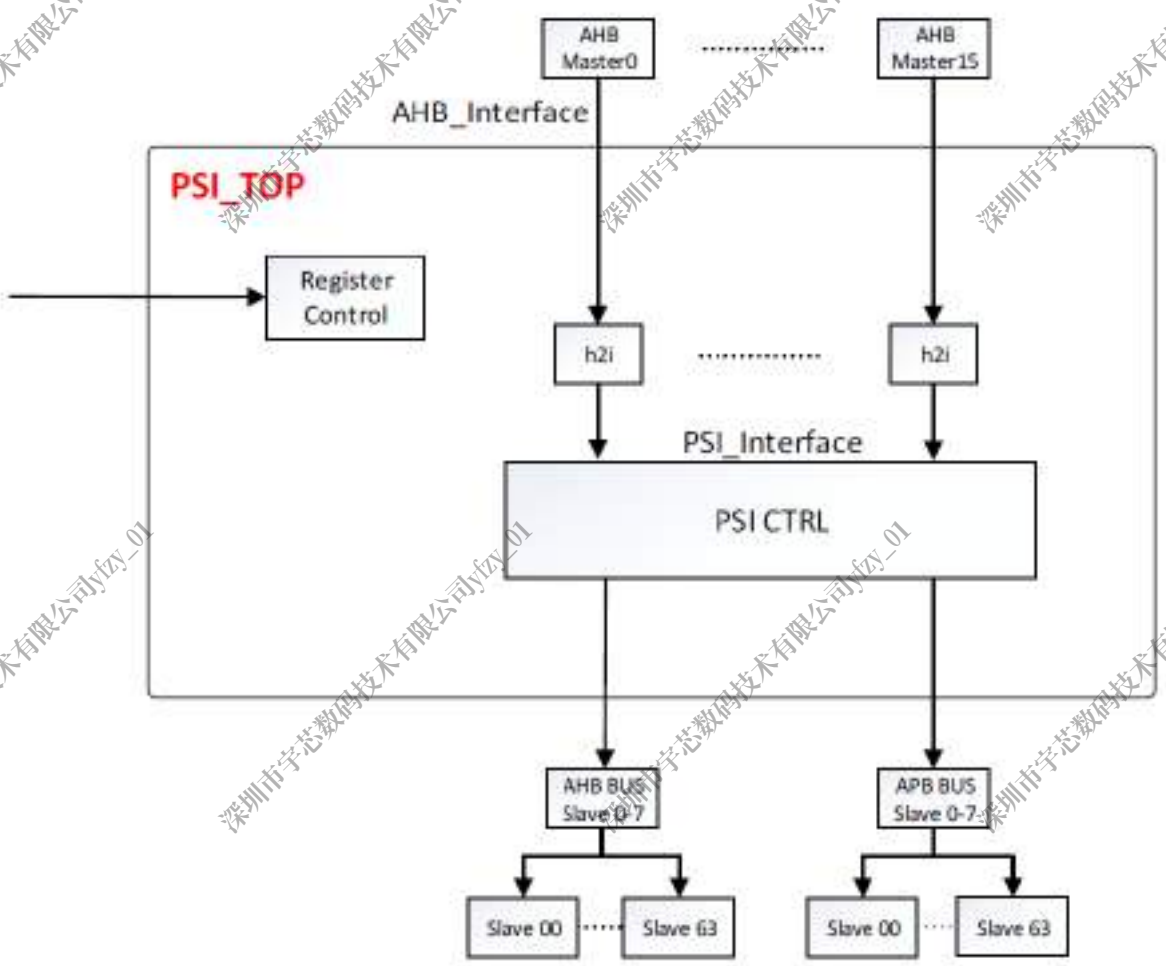


Figure 3-34. PSI Block Diagram

3.13. Message Box

3.13.1. Overview

The Message Box(MSGBOX) provides interrupt communication mechanism for on-chip processor.

The MSGBOX has the following features:

- The communication parties transmit information through channel
- FIFO depth is 4 x 32 bits
- The communication parties are CPUS and CPUX
- Interrupt alarm function

3.13.2. Block Diagram

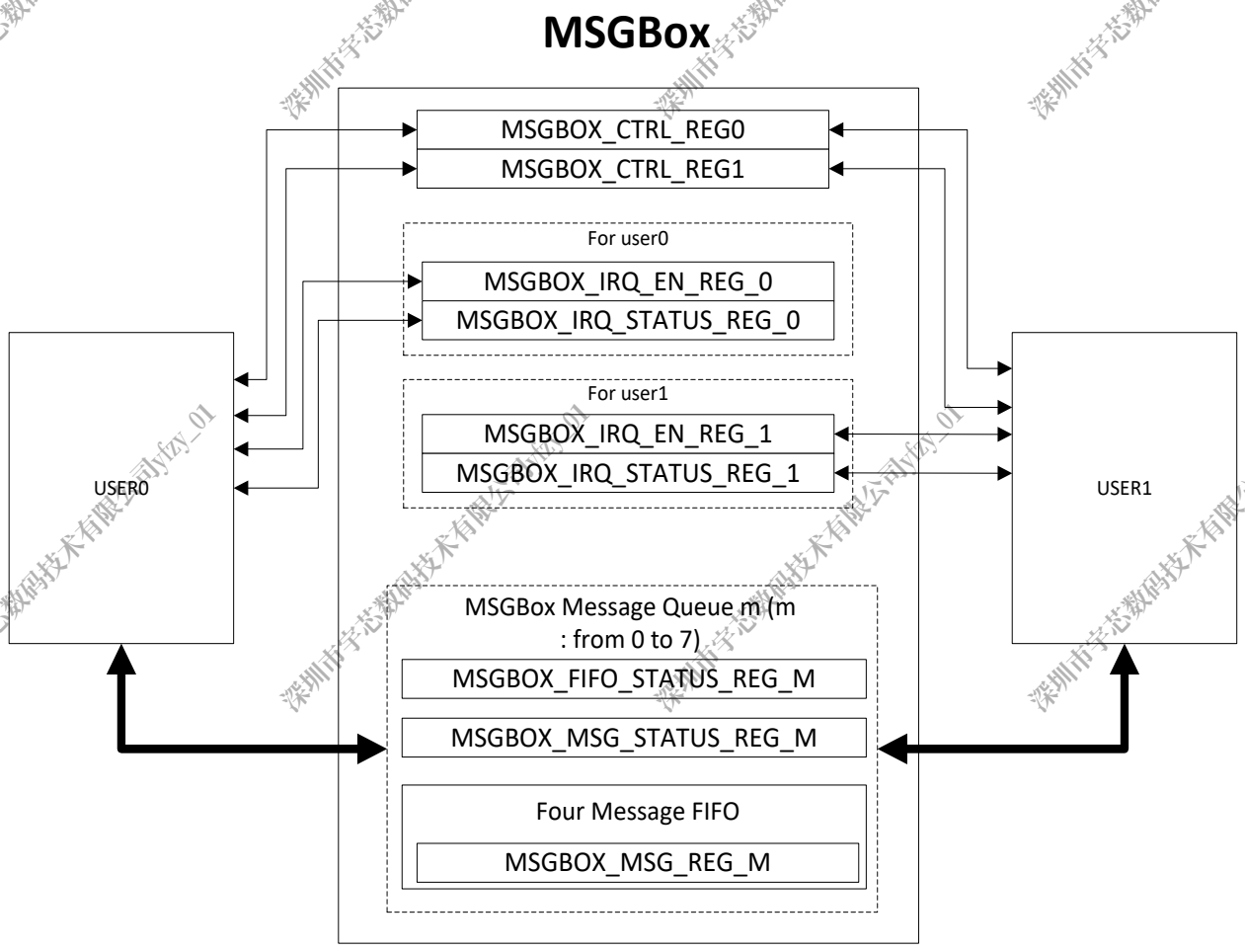


Figure 3-35. Message Box Block Diagram

3.13.3. Operations and Functional Descriptions

3.13.3.1. Clock and Reset

MSGBOX is on AHB1 bus. To access MSGBOX, perform the following steps about AHB1 bus:
Step1: De-assert MSGBOX reset signal.
Step2: Open MSGBOX gating signal.

3.13.3.2. Typical Application

Two different CPU can build communication by configuring MSGBOX. The communication parties have 8 bidirectional channels. If a party is receiver, then another is transmitter. During communication process, the current status can be judged through interrupt or FIFO status.

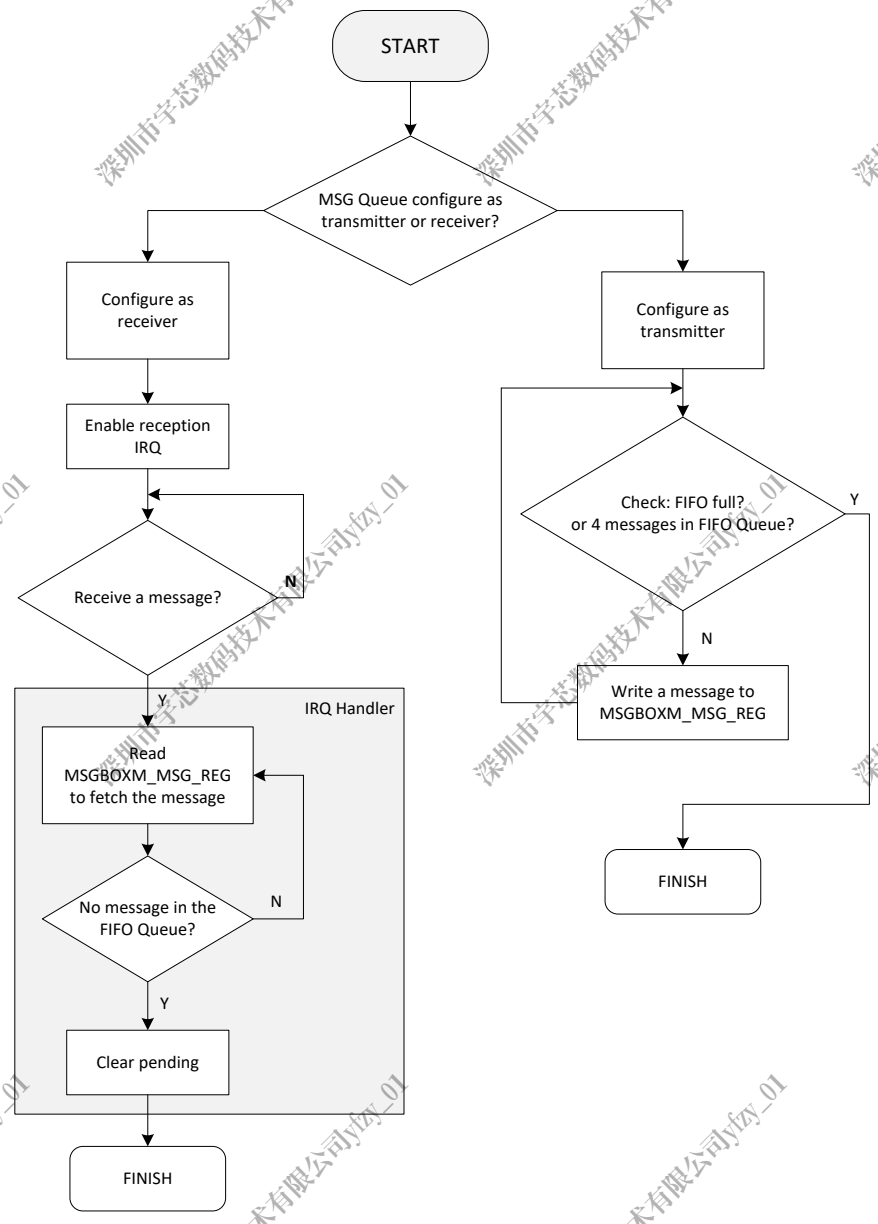


Figure 3-36. Message Box Typical Application Chart

3.13.3.3. Function Implemention

3.13.3.3.1. Transmitter and Receiver Mode

User0 and User1 can be configured as transmitter or receiver, but User0 and User1 cannot configure as same mode in the same channel, that is, User0 is transmitter, User1 must be receiver; User0 is receiver, User1 must be transmitter.

3.13.3.3.2. Interrupt

Interrupt has two types:

- As receiver, when received new information, the interrupt signal can generate.
- As transmitter, when channel FIFO is not full, the interrupt signal can generate.

Eight channels can configure the interrupt enable bit individually, but interrupt controller only has a MSGBOX interrupt number.

3.13.3.3.3. FIFO Status

- When channel FIFO is not full, the value of **FIFO_FULL_FLAG** is 0, at this time ,FIFO can execute write operation.
- When channel FIFO is full, the value of **FIFO_FULL_FLAG** is 1, at this time, if writing data again to FIFO, the first data in FIFO can be overrided.
- FIFO status can be read by **MSGBOXM_MSG_STATUS_REG**.

3.13.3.3.4. Debug Mode

- In debug mode, User0 can transmit data to User0, User1 can transmit data to User1.
- In debug mode, FIFO function will close.

3.13.3.4. Operating Mode

3.13.3.4.1. Transfer Mode Configuration

- Queue n (n=0~3)transmitter mode: Write 1 to the bit[8*n+4] of **MSGBOX_CTRL_REG0**.
- Queue m (m=4~7)transmitter mode : Write 1 to the bit[8*(m-4)+4] of **MSGBOX_CTRL_REG1**.
- Queue n (n=0~3) receiver mode: Write 1 to the bit[8*n] of **MSGBOX_CTRL_REG0**.
- Queue m (m=4~7) receiver mode : Write 1 to the bit[8*(m-4)] of **MSGBOX_CTRL_REG1**.

3.13.3.4.2. Interrupt Check Transfer Status

(1) Configure transmitter and receiver mode through **chapter 3.13.3.4.1. Transfer Mode Configuration**.
(2) Interrupt enable bit: Configure the interrupt enable bit of transmitter/receiver through **MSGBOX_IRQ_EN_REG**.
(3) When FIFO is not full, an interrupt pending generates to remind the transmitter to transmit data, at this time, to write data to FIFO in interrupt handler ,and clear the pending bit and the enable bit of *Transmitter IRQ*.
(4) When FIFO has new data, an interrupt pending generates to remind the receiver to receive data, at this time, to read data from FIFO in interrupt handler, and clear the pending bit and the enable bit of *Receiver IRQ*.

3.13.3.4.3. FIFO Check Transfer Status

(1) Configure transmitter and receiver mode through **chapter 3.13.3.4.1. Transfer Mode Configuration**.
(2) When FIFO is not full, the transmitter fills FIFO to 4*32 bits.
(3) When the receiver considers FIFO is full, then the receiver reads FIFO data, and reads **MSGBOXM_MSG_STATUS_REG** to require the current FIFO number.

3.13.3.4.4. Debug

To use MSGBOX in debug mode, performs the following steps:
(1) Write 1 to the bit0 of **MSGBOX_DEBUG_REG**.
(2) The control bit of the corresponding channel is set to 1.

3.13.4. Register List

Module Name	Base Address
MSGBOX	0x03003000

Register Name	Offset	Description
MSGBOX_CTRL_REG0	0x0000	Message Queue Attribute Control Register 0
MSGBOX_CTRL_REG1	0x0004	Message Queue Attribute Control Register 1
MSGBOXU_IRQ_EN_REG	0x0040+n*0x20	IRQ Enable for User n (n=0,1)
MSGBOXU_IRQ_STATUS_REG	0x0050+n*0x20	IRQ Status for User n (n=0,1)
MSGBOXM_FIFO_STATUS_REG	0x0100+N*0x04	FIFO Status for Message Queue N(N = 0~7)
MSGBOXM_MSG_STATUS_REG	0x0140+N*0x04	Message Status for Message Queue N(N=0~7)
MSGBOXM_MSG_REG	0x0180+N*0x04	Message Register for Message Queue N(N=0~7)
MSGBOX_DEBUG_REG	0x01C0	MSGBOX Debug Register

3.13.5. Register Description

3.13.5.1. MSGBox Control Register 0(Default Value: 0x1010_1010)

Offset: 0x0000			Register Name: MSGBOX_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	TRANSMIT_MQ3 Message Queue 3 is a transmitter of user u 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ3 Message Queue 3 is a receiver of user u 0: user0 1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ2 Message Queue 2 is a transmitter of user u 0: user0 1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ2 Message Queue 2 is a receiver of user u 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ1 Message Queue 1 is a transmitter of user u 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ1 Message Queue 1 is a receiver of user u 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ0 Message Queue 0 is a transmitter of user u 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ0 Message Queue 0 is a receiver of user u 0: user0 1: user1

3.13.5.2. **MSGBox Control Register 1(Default Value: 0x1010_1010)**

Offset: 0x0004			Register Name: MSGBOX_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	TRANSMIT_MQ7 Message Queue 7 is a transmitter of user u 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ7 Message Queue 7 is a receiver of user u 0: user0 1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ6 Message Queue 6 is a transmitter of user u 0: user0 1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ6 Message Queue 6 is a receiver of user u 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ5 Message Queue 5 is a transmitter of user u 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ5 Message Queue 5 is a receiver of user u 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ4 Message Queue 4 is a transmitter of user u 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ4 Message Queue 4 is a receiver of user u 0: user0 1: user1

3.13.5.3. **MSGBox IRQ Enable Register u(u=0,1)(Default Value: 0x0000_0000)**

Offset:0x0040+N*0x20(N=0,1)			Register Name: MSGBOX_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	TRANSMIT_MQ7_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 7 is not full.)
14	R/W	0x0	RECEPTION_MQ7_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 7 has received a new message.)
13	R/W	0x0	TRANSMIT_MQ6_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 is not full.)
12	R/W	0x0	RECEPTION_MQ6_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 has received a new message.)
11	R/W	0x0	TRANSMIT_MQ5_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 is not full.)
10	R/W	0x0	RECEPTION_MQ5_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 has received a new message.)
9	R/W	0x0	TRANSMIT_MQ4_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 is not full.)
8	R/W	0x0	RECEPTION_MQ4_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 has received a new message.)
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 3 is not full.)
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 3 has

			received a new message.)
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 2 is not full.)
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 2 has received a new message.)
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 is not full.)
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 has received a new message.)
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 is not full.)
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 has received a new message.)

3.13.5.4. **MSGBox IRQ Status Register u(Default Value: 0x0000_AAAA)**

Offset:0x0050+N*0x20(N=0,1)			**Register Name: MSGBOXU_IRQ_STATUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x1	TRANSMIT_MQ7_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 is not full. Setting one to this bit will clear it.
14	R/W	0x0	RECEPTION_MQ7_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 has received a new message. Setting one to this bit will clear it.
13	R/W	0x1	TRANSMIT_MQ6_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 6 is not full. Setting one to this bit will clear it.
12	R/W	0x0	RECEPTION_MQ6_IRQ_PEND 0: No effect

			1: Pending. This bit will be pending for user u when Message Queue 6 has received a new message. Setting one to this bit will clear it.
11	R/W	0x1	TRANSMIT_MQ5_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 is not full. Setting one to this bit will clear it.
10	R/W	0x0	RECEPTION_MQ5_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 has received a new message. Setting one to this bit will clear it.
9	R/W	0x1	TRANSMIT_MQ4_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 is not full. Set one to this bit will clear it.
8	R/W	0x0	RECEPTION_MQ4_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 has received a new message. Setting one to this bit will clear it.
7	R/W	0x1	TRANSMIT_MQ3_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 is not full. Setting one to this bit will clear it.
6	R/W	0x0	RECEPTION_MQ3_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 has received a new message. Setting one to this bit will clear it.
5	R/W	0x1	TRANSMIT_MQ2_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 is not full. Setting one to this bit will clear it.
4	R/W	0x0	RECEPTION_MQ2_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 has received a new message. Setting one to this bit will clear it.
3	R/W	0x1	TRANSMIT_MQ1_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 1 is not full. Setting one to this bit will clear it.
2	R/W	0x0	RECEPTION_MQ1_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 1 has received a new message. Setting one to this bit will clear it.
1	R/W	0x1	TRANSMIT_MQ0_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 is not full. Setting one to this bit will clear it.

0	R/W	0x0	RECEPTION_MQ0_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 has received a new message. Setting one to this bit will clear it.

3.13.5.5. **MSGBox FIFO Status Register m(Default Value: 0x0000_0000)**

Offset:0x0100+N*0x04 (N=0~7)			**Register Name: MSGBOXM_FIFO_STATUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	FIFO_FULL_FLAG 0: The Message FIFO queue is not full (space is available) 1: The Message FIFO queue is full. This FIFO status register has the status related to the message queue.

3.13.5.6. **MSGBox Message Status Register m(Default Value: 0x0000_0000)**

Offset:0x0140+N*0x04 (N=0~7)			**Register Name: MSGBOXM_MSG_STATUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	MSG_NUM Number of unread messages in the message queue. Here, limited to four messages per message queue. 000: There is no message in the message FIFO queue. 001: There is 1 message in the message FIFO queue. 010: There are 2 messages in the message FIFO queue. 011: There are 3 messages in the message FIFO queue. 100: There are 4 messages in the message FIFO queue. 101~111:/

3.13.5.7. **MSGBox Message Queue Register m(Default Value : 0x0000_0000)**

Offset:0x0180+N*0x04 (N=0~7)			**Register Name: MSGBOXM_MSG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

3.13.5.8. **MSGBox Debug Register(Default Value: 0x0000_0000)**

Offset: 0x01C0			**Register Name: MSGBOX_DEBUG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

15:8	R/W	0x0	FIFO_CTRL MQ[7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode. 1: Disable the corresponding FIFO (Clear FIFO).
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE In the Debug Mode, each user can transmit messages to itself through each Message Queue. 0: Normal Mode 1: Debug Mode.

3.14. Spinlock

3.14.1. Overview

In multi-core system,the Spinlock offers hardware synchronization mechanism, lock operation can prevent multi processors from handling data-sharing at the same time, and ensure coherence of data.

The Spinlock has the following features:

- Spinlock module includes 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable(less than 200 cycles)

3.14.2. Block Diagram

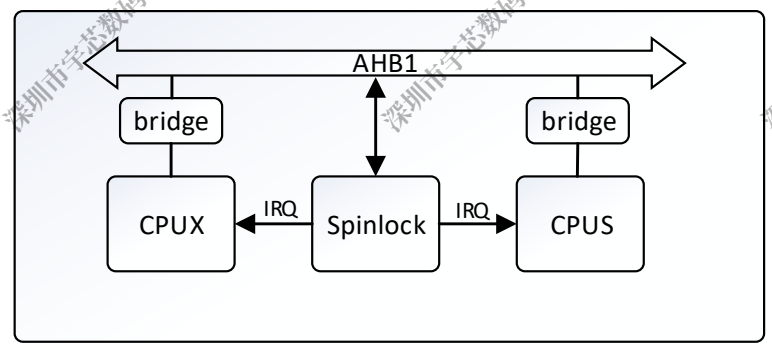


Figure 3-37. Spinlock Block Diagram

3.14.3. Operations and Functional Descriptions

3.14.3.1. Clock and Reset

The Spinlock is hung on AHB1. Before accessing Spinlock register, open the corresponding gating bit on AHB1 and de-assert reset signal. The correct operation order is to de-assert reset signal at first, and then open the corresponding gating signal.

3.14.3.2. Typical Application

A processor lock spinlock0, when the status is locked, the processor executes specific code, and then unlocks code. Other processors is released to start reading/writing operation.

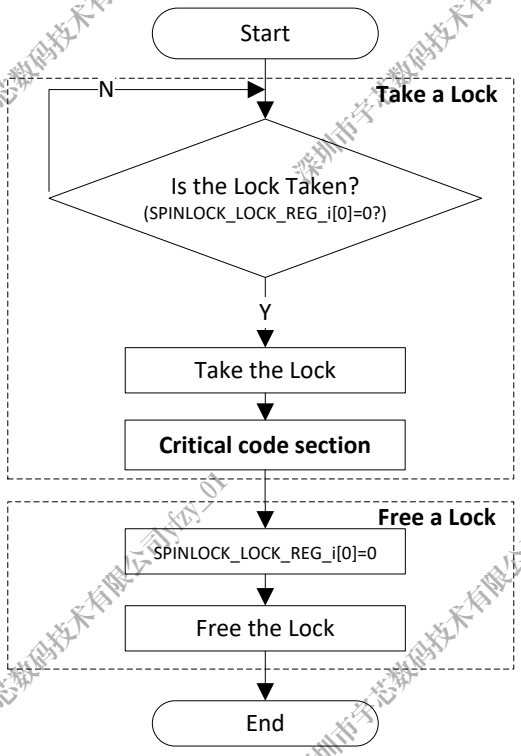


Figure 3-38. Spinlock Typical Application Diagram

3.14.3.3. Function Implemention

3.14.3.3.1. Spinlock State Machine

When a processor uses spinlock, it needs to acquire spinlock's status through **SPINLOCK_STATUS_REG**.
Reading Operation: when return value is 0, spinlock comes into locked status; when read this status bit again, return value is 1, spinlock comes into locked status.
Writing Operating: when the Spinlock is in locked status, the Spinlock can convert to unlocked status through writing 0. After reset, the Spinlock is in unlocked status by default.

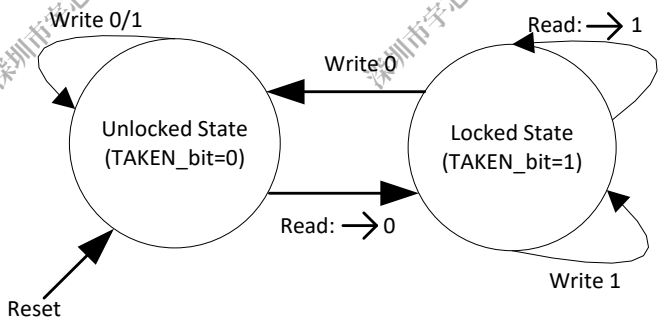


Figure 3-39. Spinlock State Machine

3.14.3.3.2. Interrupt

When **Free Lock** is released(lock status is changed from locked to unlocked), interrupt is generated.

3.14.3.4. **Operating Mode**

3.14.3.4.1. Switch Status

(1) When the read value from **SPINLOCKN_LOCK_REG** is 0, the Spinlock come into locked status.
(2) Execute application code, the status of **SPINLOCKN_STATUS_REG** is 1.
(3) Write 0 to **SPINLOCKN_LOCK_REG**, the Spinlock comes into unlocked status, the corresponding spinlock is released.

3.14.4. Programming Guidelines

Take CPU0's synchronization with CPUS with Spinlock0 for an example, CPU0 takes the spinlock0 firstly in the instance.

CPU0 of Cluster0:

```
Step 1: CPU0 initializes Spinlock
    put_wvalue(SPINLOCK_BGR_REG,0x00010000);
    put_wvalue(SPINLOCK_BGR_REG,0x00010001);
Step 2: CPU0 requests to take spinlock0
    rdata=readl(SPINLOCK_STATUS_REG0);                  //check lock register0 status, if it is taken, check till
    if(rdata != 0)    writel (0, SPINLOCK_LOCK_REG0);   //CPU0 frees spinlock0
    rdata=readl(SPINLOCK_LOCK_REG0);                    //request to take spinlock0, if fail, retry till
    if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0);  // lock register0 is taken
 ---------- CPU0 critical code section ----------
Step 3: CPU0 free spinlock0
    writel (0, SPINLOCK_LOCK_REG0);                     //CPU0 frees spinlock0
Step 4: CPU0 waits for CPUS' freeing spinlock0
    writel (readl(SPINLOCK_STATUS_REG0) == 1);          // CPU0 waits for CPUS' freeing spinlock0
```

CPUS:

```
Step 1: CPU0 has taken spinlock0, CPUS waits for CPU0' freeing spinlock0
    while(readl(SPINLOCK_STATUS_REG0) == 1);            // CPUS waits for CPU0' freeing spinlock0
 Step 2: CPUS takes spinlock0 and go on
    rdata=readl(SPINLOCK_LOCK_REG0);                    //request to take spinlock0, if fail, retry till
    if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0);  // lock register0 is taken
---------- CPUS critical code section ----------
Step 3: CPUS frees spinlock0
writel (0, SPINLOCK_LOCK_REG0);                         //CPUS frees spinlock0
```

3.14.5. Register List

Module Name	Base Address
Spinlock	0x03004000

Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	Spinlock System Status Register
SPINLOCK_STATUS_REG	0x0010	Spinlock Status Register
SPINLOCK_IRQ_EN_REG	0x0020	SpinLock Interrupt Enable Register

SPINLOCK_IRQ_STA_REG	0x0040	SpinLock Interrupt Status Register
SPINLOCK_LOCK_REGN	0x0100+N*0x04	Spinlock Register N (N=0~31)

3.14.6. Register Description

3.14.6.1. Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM Number of lock registers implemented 00: This instance has 256 lock registers. 01: This instance has 32 lock registers. 10: This instance has 64 lock registers. 11: This instance has 128 lock registers.
27:9	/	/	/
8	R	0x0	IU0 In-Use flag0, covering lock register0-31 0: All lock register 0-31 are in the NotTaken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

3.14.6.2. Spinlock Register Status(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R	0x0	LOCK_REG_STATUS SpinLock[i] status (i=0~31) 0: The Spinlock is free. 1: The Spinlock is taken.

3.14.6.3. Spinlock Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPINLOCK_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R/W	0x0	LOCK_IRQ_EN SpinLock[i] interrupt enable 0:Disable 1:Enable

3.14.6.4. Spinlock Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPINLOCK_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R/W1C	0x0	LOCK_IRQ_STATUS. SpinLock[i] interrupt status. 0:No effect 1:Pending Writing 1 will clear this bit.

3.14.6.5. Spinlock Register N (N=0 to 31)(Default Value: 0x0000_0000)

Offset:0x0100+N*0x04 (N=0~31)			Register Name: SPINLOCKN_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	TAKEN Lock State Read 0x0: The lock was previously Not Taken (free).The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.

Chapter 4 Video and Graphics

4.1. DE

The Display Engine(DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports four overlay windows to blend, and supports image post-processing in the video channel. The block diagram of DE is shown in Figure 4-1.

The DE has the following features:

- Output size up to 4096x4096
- Four alpha blending channels for main display
- Four overlay layers in each channel, and has a independent scaler
- Potter-duff compatible blending operation
- Input format semi-planar of YUV422/YUV420/YUV411 and planar of YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
  - Content adaptive backlight control
- Supports write back

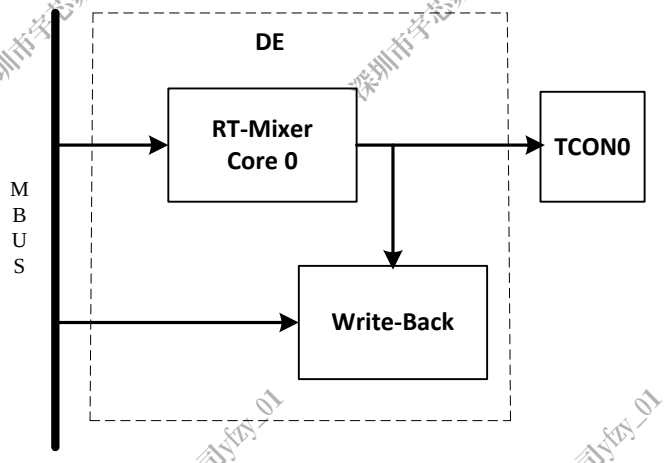


Figure 4-1. DE Block Diagram

4.2. G2D

The Graphic 2D(G2D) Engine is hardware accelerator for 2D graphic.

The G2D has the following features:

Mixer:

- Layer size up to 2048 x 2048 pixels
- Supports pre-multiply alpha image data
- Color key
- Two pipes porter-duff alpha blending
- Input/output format: YUV422(interleaved, semi-planar and planar format)/YUV420(semi-planar and planar format)/YUV411(semi-planar and planar format)/Y8/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Supports memory scan order option
- Any format convert function
- 1/16x to 32x resize ratio
- 32-phase 8-tap horizontal anti-alias filter, 32-phase 4-tape vertical anti-alias filter
- Window clip
- FillRectangle, BitBlit,StretchBlit and MaskBlit

Rotate:

- Horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

4.3. Video Encoding

The Video Encoding consists of the video encoding unit(VE) and JPEG encoder(JPGE). The VE supports H.264 and H.265 encoding,and JPGE supports JPEG/MJPEG encoding.

4.3.1. VE

4.3.1.1. Overview

The VE is a CODEC that supports H.264 and H.265 protocol based on ASIC. It is custom-made for the camera usage and features high compressing rate, low CPU usage, short delay and low power consumption.
The VE has the following features:

- Supports ITU-T H.265 main profile@level 6.0 main-tier encoding
  - Motion compensation with 1/2 and 1/4 pixel precision
  - Encoding of the multiple reference frame, long-term reference frame
  - Three prediction unit (PU) types of 32x32, 16x16 and 8x8 for inter-prediction
  - Four prediction unit types of 32x32, 16x16, 8x8 and 4x4 for intra-prediction
  - Skip mode and Merge mode with a maximum of two candidates processing to be merged
  - Four transform unit (TU) types of 32x32, 16x16, 8x8 and 4x4
  - CABAC entropy encoding
  - De-blocking filtering
  - Sample adaptive offset (SAO)
- Supports ITU-T H.264 high profile/main profile/baseline profile@level 5.2 encoding
  - Encoding of multiple slice
  - Motion compensation with 1/2 and 1/4 pixel precision
  - Encoding of the multiple reference frame, long-term reference frame
  - Two prediction unit (PU) types of 16x16 and 8x8 for inter-prediction
  - Three prediction unit types of Intra16x16, Intra8x8 and Intra4x4 for intra-prediction
  - Trans4x4 and trans8x8
  - CABAC and CAVLC entropy encoding
  - De-blocking filtering
- Supports QPMap mode for custom encoding
- Supports SSE/QP/MAD output based on 16x16
- Supports Smart, HVS and Alter FrameRate functions in particular
- Supports Classify, MB-RateControl, Fore-3D-Filter, Syclic-Intra-Refresh, Dynamic-ME, Inter-Only-in-P-Frame, Intra-4x4-Disable and HighPass-Filter Functions in general
- Supports the input picture format of semi-planar YCbCr4:2:0
- **V536-H** supports H.265/H.264 multi-stream encoding with the performance of 8-megapixel (3840x2160)@30fps + VGA@30fps
- Supports configurable picture resolutions
  - Minimum picture resolution: 192x96
  - Maximum picture resolution: 4096x4096
  - Step of the picture width or height: 2
- Supports region of interest (ROI) encoding
  - Maximum of 8 ROIs
  - Independent enable/disable control for the encoding function of each ROI

- Supports on-screen display (OSD) encoding protection that can be enabled or disabled
- Supports OSD front-end overlaying
  - OSD overlaying before encoding for a maximum of 64 regions
  - OSD overlaying with any size and at any position (within the size and position range of the picture)
  - 16-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports three bit rate control modes: constant bit rate (CBR), variable bit rate (VBR) and FIXQP
- Supports the output bit rate ranging from 2 kbit/s to 100 Mbit/s
- Supports Frame Buffer Compression

4.3.1.2. **Block Diagram**

The functional block diagram of the VE is as follows.

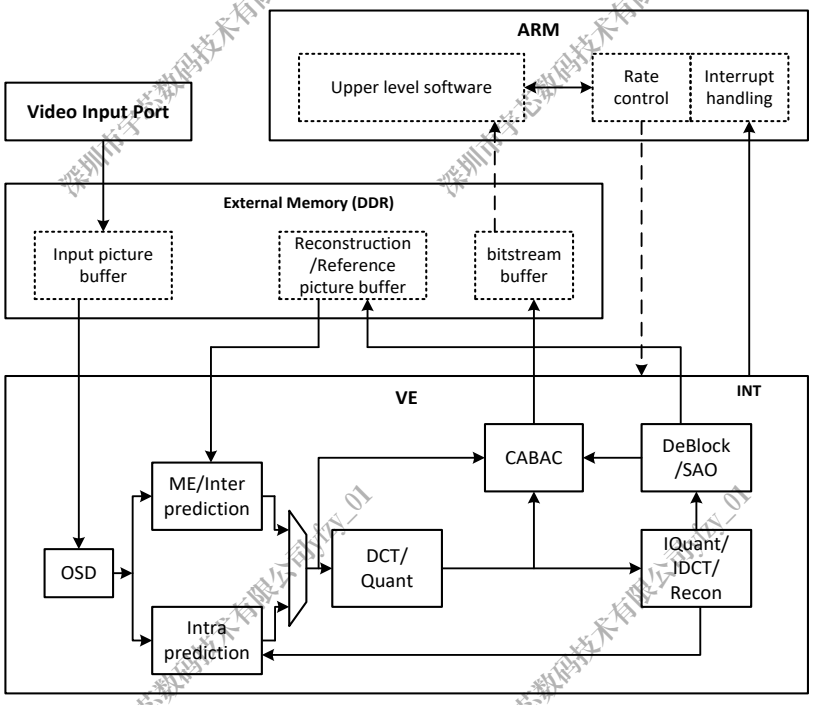


Figure 4-2. VE Block Diagram

Based on related protocols and algorithms, the VE supports motion estimation/inter-prediction, intra-prediction, transform/quantization, inverse transform/inverse quantization, CABAC encoding/stream generation and DeBlock/SAO. The ARM software controls the bitrate and handles interrupt.

Before the VE is enabled for video encoding, software allocates three types of buffers mainly in the external DDR SDRAM:

- **Input picture buffer**

  The VE reads the source pictures to be encoded form this buffer during encoding. This buffer is typically written by the Video Input Port module.

- **Reconstruction/Reference picture buffer**

  The VE writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames and B frames, reference pictures are read from this buffer.

- **Stream buffer**

  This buffer stores encoded streams. The VE writes streams to this buffer during encoding. This buffer is read by software.

4.3.2. JPGE

4.3.2.1. **Overview**

The JPGE is a high-performance encoder based on ASIC. It supports 64-megapixel snapshot or HD MJPEG encoding.

The JPGE has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
- Encodes the pictures in the chrominance sampling format of YCbCr4:2:0, YCbCr4:2:2 and YCbCr4:4:4
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
  - Semi-planar YCbCr4:4:4
- Supports JPEG encoding with the performance of 1080P@60fps
- Supports configurable picture resolutions
  - Minimum picture resolution: 192x96
  - Maximum picture resolution: 8192x8192
- Supports the picture width or height step of 8
- Supports configurable quantization tables for the Y component, Cb component and Cr component respectively
- Supports OSD front-end overlapping
  - OSD overlaying before encoding for a maximum of 64 regions
  - OSD overlaying with any size and at any position (within the size and position range of the picture)
  - 16-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports the color-to-gray function
- Supports the MJPEG output bit rate ranging from 2 kbit/s to 100 Mbit/s

4.3.2.2. **Block Diagram**

The functional block diagram of the JPGE is as follows.

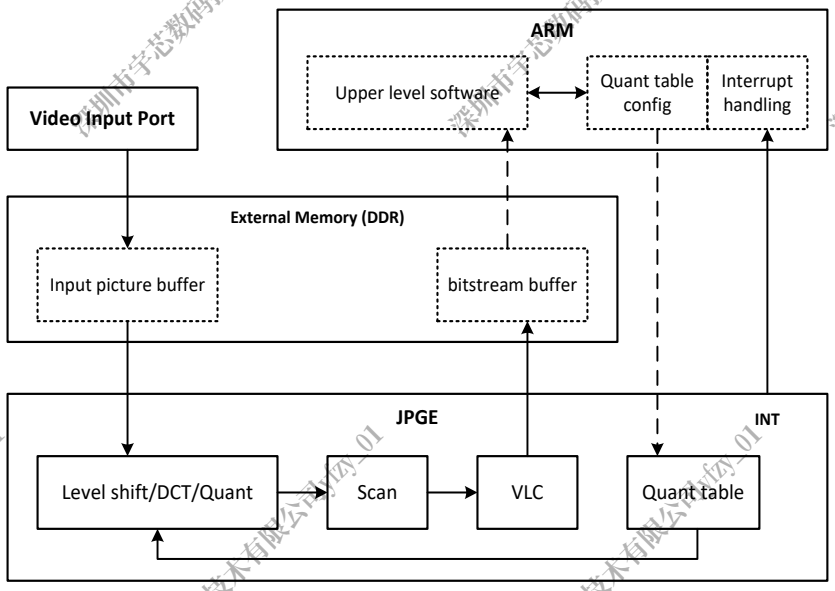


Figure 4-3. JPGE Block Diagram

Based on the protocols that require a large number of operands, the JPGE supports OSD, level shift, DCT, quantization, scanning, VLC encoding and stream generation. The ARM software configures quantization tables and handles interrupt.

Before the JPGE is enabled for video encoding, the software allocates two types of buffers mainly in the external DDR SDRAM:

- **Input picture buffer**

  The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the Video Input Port module.

- **Stream buffer**

  This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

4.4. ISE

The ISE(Image Stitch Engine) module implements Fisheye Correction, Lens Distortion Correction (LDC).

4.4.1. Fisheye Correction and LDC

4.4.1.1. Overview

The fisheye correction module corrects fisheye images to conform to user habit, and includes 360 panoramic mode, 180 panoramic mode, 360 split panoramic mode and normal mode. The LDC module removes the imaging distortion of wide angle lens.

4.4.1.2. Functional Descriptions

4.4.1.2.1. Input

- YUV420 Semi-planar Input
- Only uncompressed image is supported
- Minimum input resolution of 128 x 128
- For 360 mode, maximum input resolution: For 360 mode is 2048 x 2048. For 180mode and PTZ mode is 2816 x 2816. For LDC mode is 3840 x 2220.

4.4.1.2.2. Input Image Size

- The height should be a multiple of 8
- The width should be a multiple of 8

4.4.1.2.3. Output

- Supports YUV420 Semi-planar output, YUV420 Semi-planar output.
- Only uncompressed image is supported
- 180 mode: output height (/width) should be less than or equal to the input height (/width), while the minimum output height (/width) should be greater than 50% of the input height (/width)
- 360 mode: output width should be 2 times of input width, output height should be 1/2 of input height
- Normal mode: output height (/width) should be less than or equal to 1/2 of input height (/width). The minimum output size is 40x40
- 360 split mode: output resolution should be equal to input resolution
- LDC mode: output resolution should be equal to input resolution

4.4.1.2.4. Output Image Size

- The height should be a multiple of 8
- The width should be a multiple of 8

4.4.1.2.5. PTZ Parameters

- Wall mount: P[25,155], T[25,155], Z[1,4]
- Top mount and bottom mount: P[0,360], T[0,90], Z[1,4]

4.5. EISE

4.5.1. Overview

Electronic Image Stabilization Engine(EISE) is located between the ISE and the Encoder , It is a hardware accelerator for anti-shake processing of continuous video images acquired by Sensor. EISE includes two modes of image distortion correction and image stabilization.

The processing capability of the EISE module is as follows.

- Supports frame rate of 1080p@60fps

4.5.2. Functional Descriptions

4.5.2.1. Input

- Only NV12 is supported
- Only uncompressed image is supported
- Minimum input resolution of 32 x 32
- The height should be a multiple of 8
- The width should be a multiple of 8
- The stride should be a multiple of 32

4.5.2.2. Output

- Only NV12 and NV21 is supported
- Only uncompressed image is supported
- Minimum input resolution of 32 x 32
- The height should be a multiple of 8
- The width should be a multiple of 8
- The stride should be a multiple of 32
- Supports cropping

Chapter 5 Memory

5.1. SDRAM Controller(DRAMC)

5.1.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to the industy-standard DDR4/DDR3/DDR3L SDRAM and Low Power DDR3/4 SDRAM. It supports up to a 24G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register setting.

Features:

- 32/16-bit bus width
- Supports 2 chip selects
- Supports DDR4/DDR3/DDR3L/LPDDR3/LPDDR4 SDRAM
- Supports different memory device's power voltage of 1.2V,1.5V,1.35V,1.2V, 1.1V
- Supports clock frequency up to 800MHz(DDR4)
- Supports clock frequency up to 800MHz for DDR3/DDR3L
- Supports clock frequency up to 800MHz for LPDDR3
- Supports clock frequency up to 800MHz for LPDDR4
- Supports memory capacity up to 24G bits (3G bytes)
- Supports 18 address lines and 3 bank address lines
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Priority of transferring through multiple ports is programmable
- Random read or write operation is supported

NOTE

V526 only supports 16-bit DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 interface.

5.2. NAND Flash Controller(NDFC)

5.2.1. Overview

The NDFC is the NAND Flash Controller which supports all NAND flash memory available in the market. New type flash can be supported by software re-configuration.

The On-the-fly error correction code (ECC) is built-in NDFC for enhancing reliability. BCH is implemented and it can detect and correct up to 80 bits error per 1024 bytes data. The on chip ECC and parity checking circuit of NDFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NDFC provides automatic timing control for reading or writing external Flash. The NDFC maintains the proper relativity for CLE, CE# and ALE control signal lines.

There are three different kinds of modes for serial read access, mode0 is for conventional serial access , mode1 is for EDO type and the mode2 is for extension EDO type. NDFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NDFC has the following features:

- Supports all SLC/MLC/TLC flash and EF-NAND memory available in the market
- Software configure seed for randomize engine
- Software configure method for adaptability to a variety of system and memory types
- 2CE/2RB
- 8-bit data bus width
- 1024, 2048, 4096, 8192, 16384, 32768 bytes size per page
- Conventional and EDO serial access method for serial reading Flash
- On-the-fly BCH error correction code which correcting up to 80 bits per 1024 bytes
- Corrected Error bits number information report
- ECC automatic disable function for all 0xff data
- NDFC status information is reported by its registers and interrupt is supported
- One Command FIFO
- Internal DMA controller based on chain-structured descriptor list
- Two 256x32-bit RAM for Pipeline Procession
- SDR, ONFI DDR and Toggle DDR NAND
- Maximum IO Rate 50MHz in SDR mode, and 60MHz in both DDR1.0 and DDR2.0 mode
- Self-debug for NDFC debug

5.2.2. Block Diagram

The NDFC system block diagram is shown below.

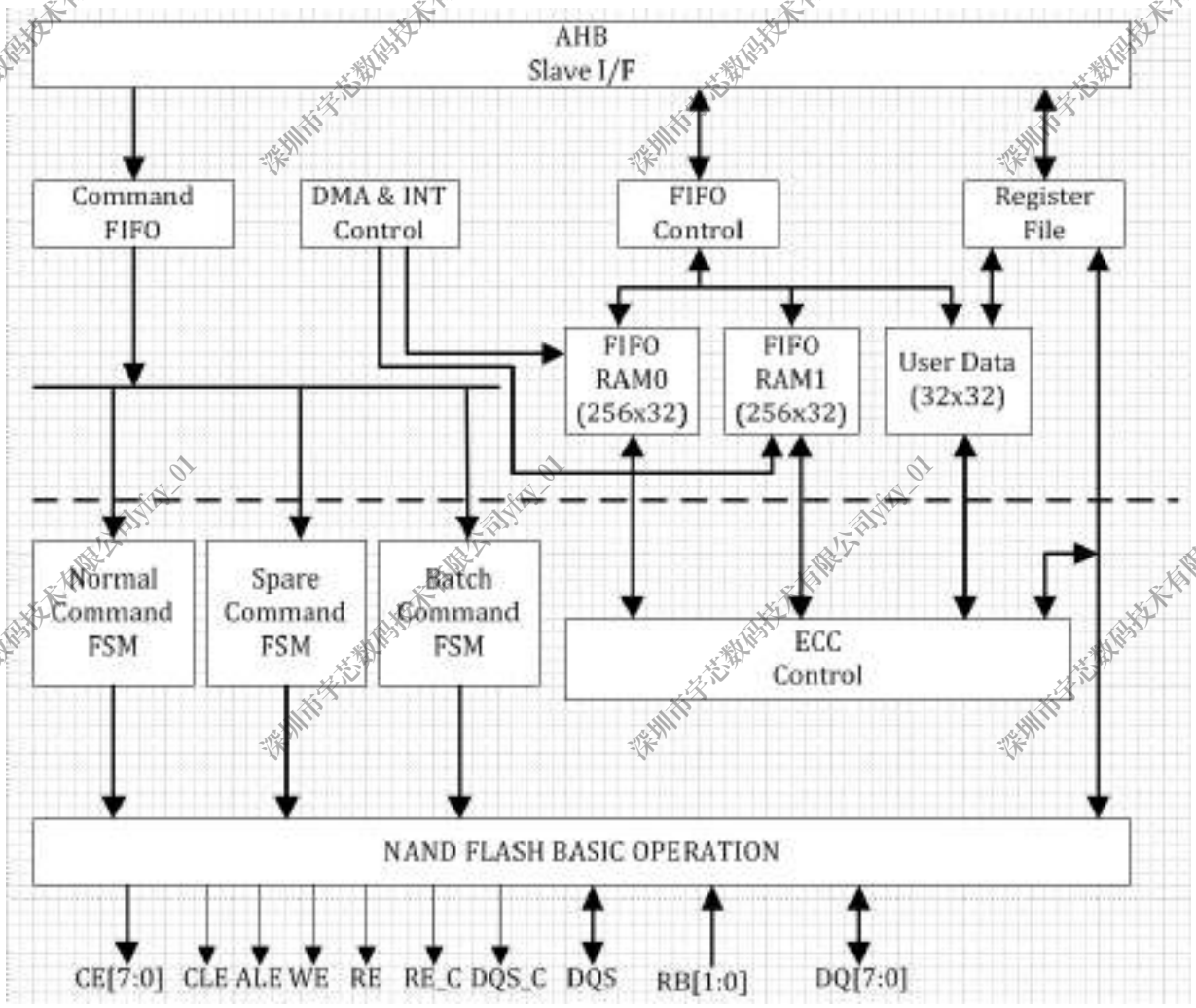


Figure 5-1. NDFC Block Diagram

5.2.3. Operations and Functional Descriptions

5.2.3.1. External Signals

Table 5-1 describes the external signals of NDFC. DQ0~DQ7 and DQS are bidirectional I/O.WE,ALE,CLE,CE,RE are output pin, RB is input pin. The RB pin in the NAND device is an open-drain driver, which must need a pull-up resistor.

Table 5-1. NDFC External Signals

Signal	Description	Type
NAND_WE	Write Enable	O
NAND_RE	Read Enable	O
NAND_ALE	Address Latch Enable, High is Active	O
NAND_CLE	Command Latch Enable, High is Active	O
NAND_CE0	Chip Enable, Low is Active	O
NAND_RB0	Ready/Busy, Low is Active	I
NAND_DQ0	Data Input / Output	I/O
NAND_DQ1	Data Input / Output	I/O
NAND_DQ2	Data Input / Output	I/O

NAND_DQ3	Data Input / Output	I/O
NAND_DQ4	Data Input / Output	I/O
NAND_DQ5	Data Input / Output	I/O
NAND_DQ6	Data Input / Output	I/O
NAND_DQ7	Data Input / Output	I/O
NAND_DQS	Data Strobe	I/O

5.2.3.2. **Clock Sources**

To ensure ECC efficiency,ECC engine and NDFC internal logic use different clock. The clock of NDFC internal logic is set by NAND0_0 Clock Register, the clock of ECC engine is set by NAND0_1 Clock Register .Note that NAND0_0 Clock Register set the internal logic clock of NDFC, but the frequency of external Nand Flash device is half of NDFC internal logic clock. That is, if external Nand Flash runs at 40MHz, then NDFC need set to 80MHz.

Both ECC engine and NDFC internal logic have five different clock sources. Users can select one of them to make ECC engine or internal logic clock source. Table 5-2 describles the clock sources of NDFC. Users can see CCU in chapter 3.3 for clock setting, configuration and gating information.

Table 5-2. NDFC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH0(2X)	Peripheral Clock, default value is 1.2GHz
PLL_PERIPH1(2X)	Peripheral Clock, default value is 1.2GHz

5.2.3.3. **Timing Diagram**

Typically, there are two kinds of serial access methods. One method is conventional method which fetching data at the rise edge of NDFC_RE# signal line. Another one is EDO type which fetching data at the next fall edge of NDFC_RE# signal line.

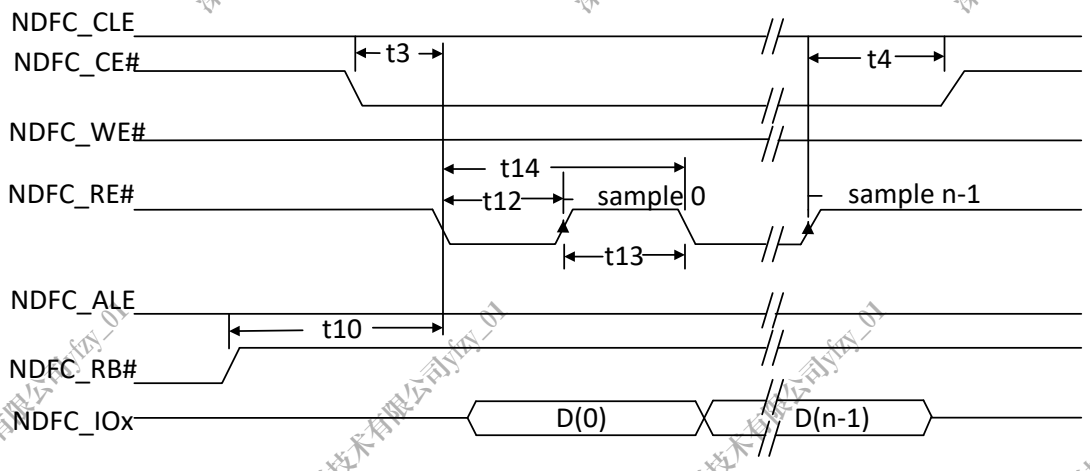


Figure 5-2. Conventional Serial Access Cycle Diagram (SAM0)

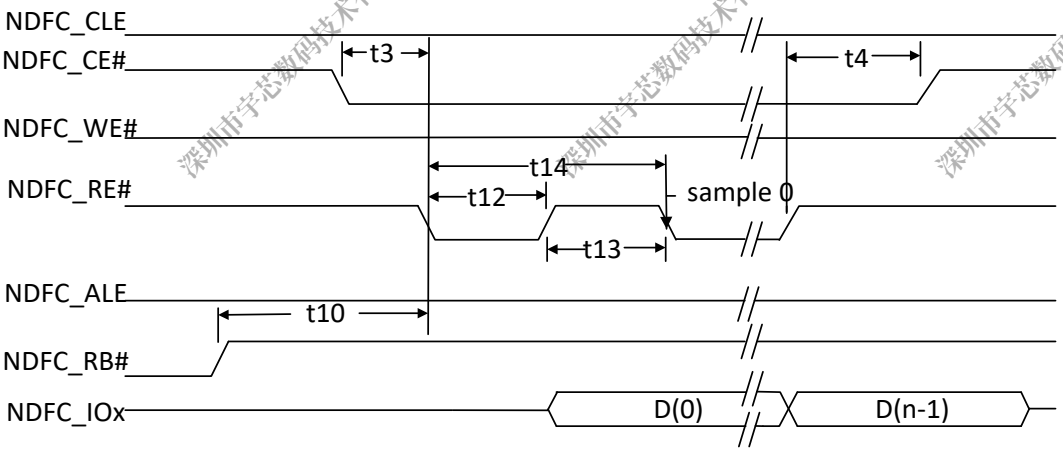


Figure 5-3. EDO Type Serial Access after Read Cycle (SAM1)

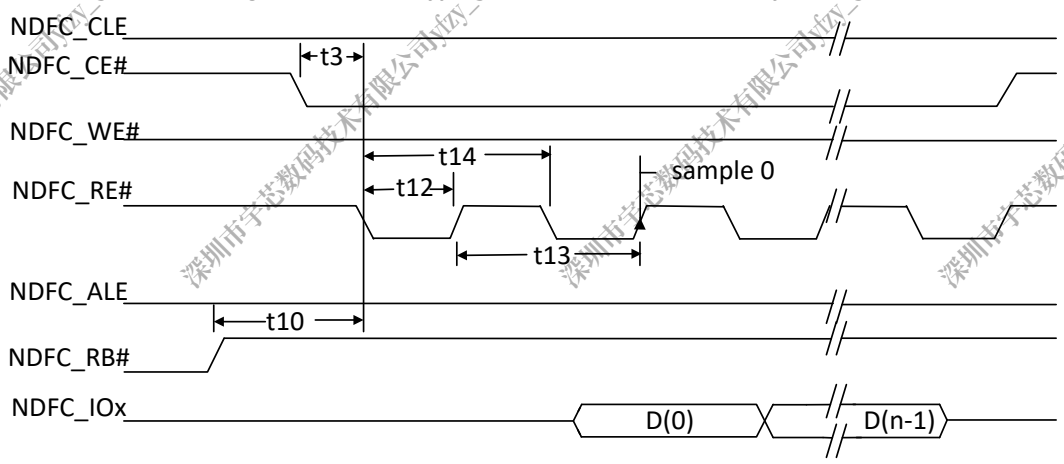


Figure 5-4. Extending EDO Type Serial Access Mode (SAM2)

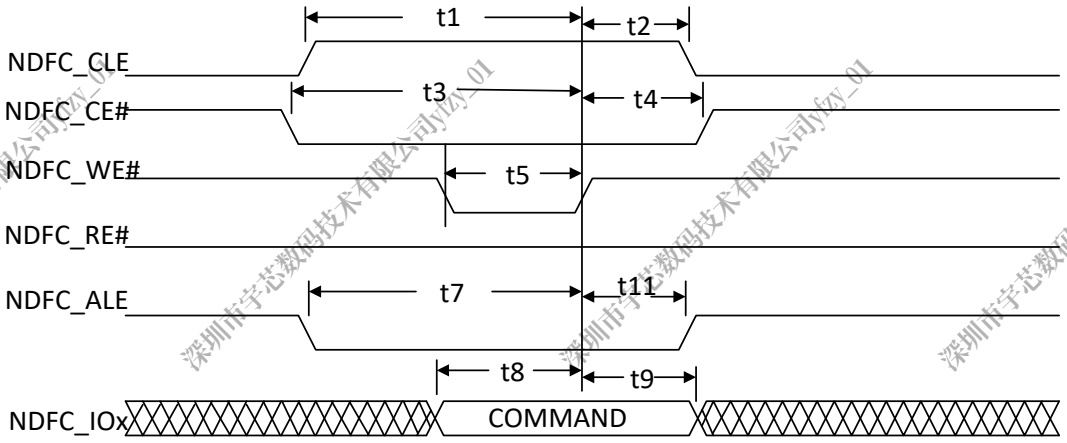


Figure 5-5. Command Latch Cycle

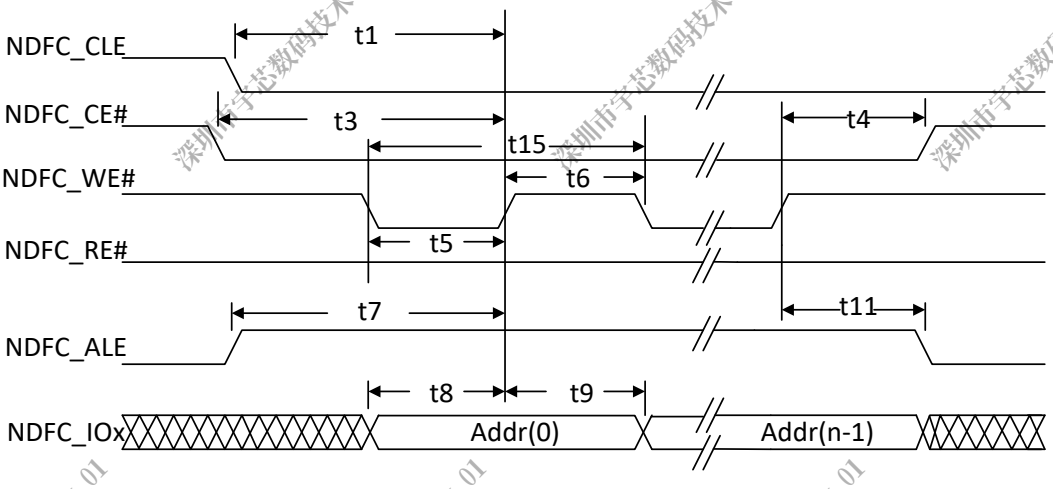


Figure 5-6. Address Latch Cycle

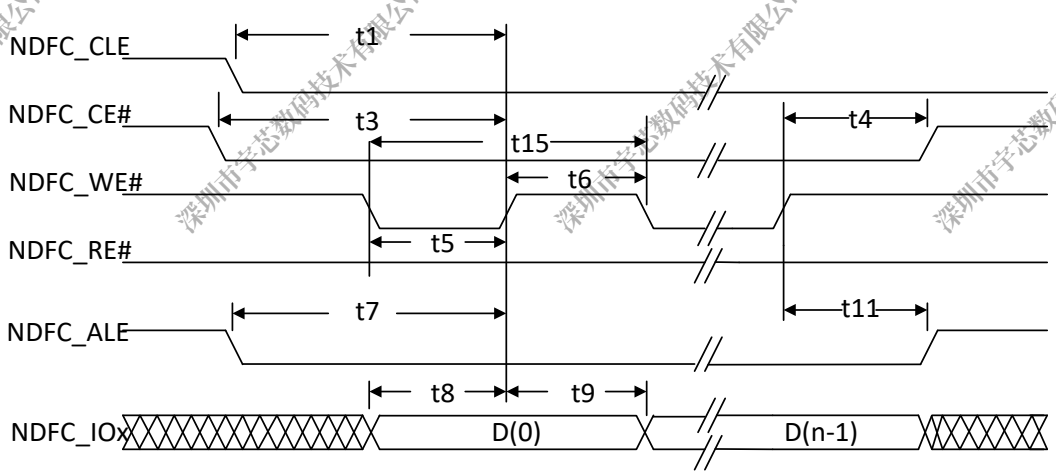


Figure 5-7. Write Data to Flash Cycle

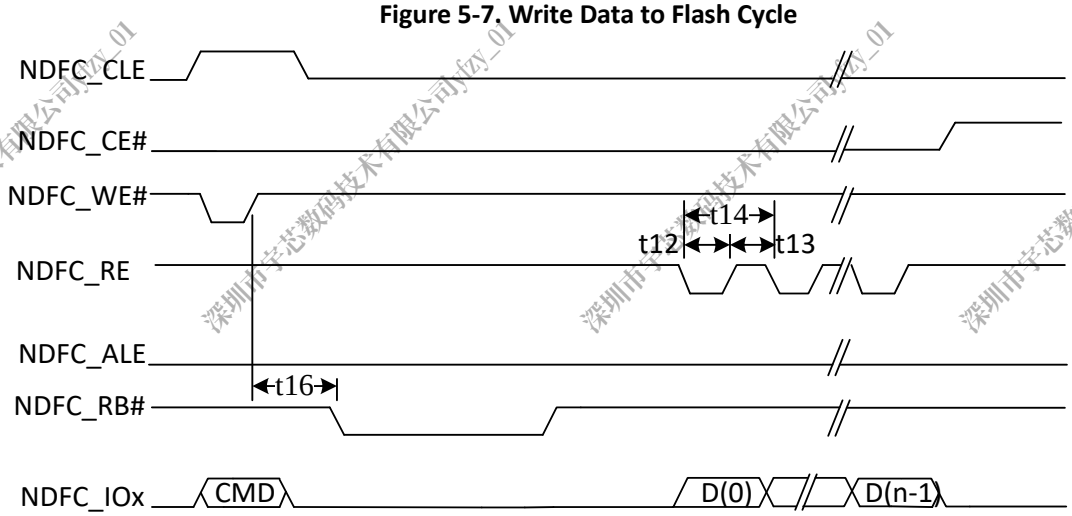


Figure 5-8. Waiting R/B# Ready Diagram

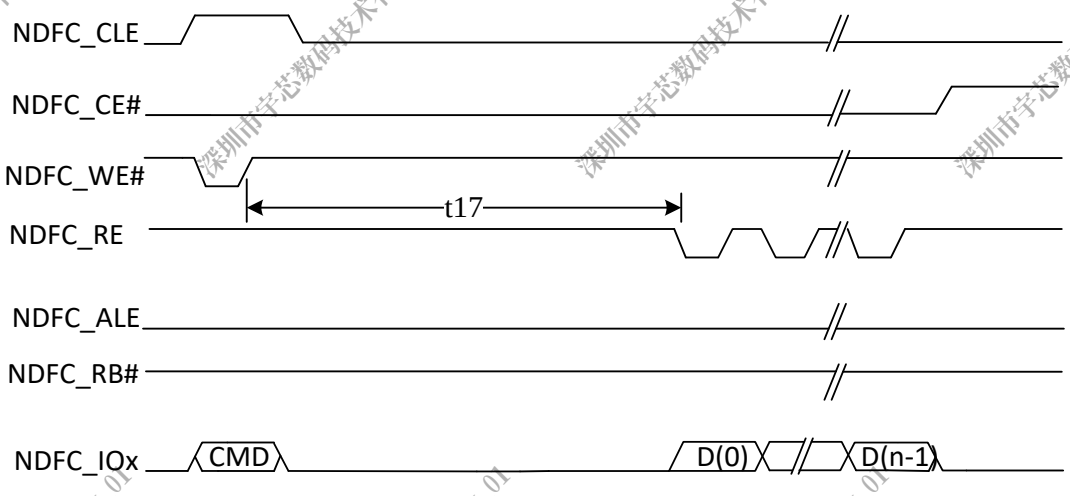


Figure 5-9. WE# High to RE# Low Timing Diagram

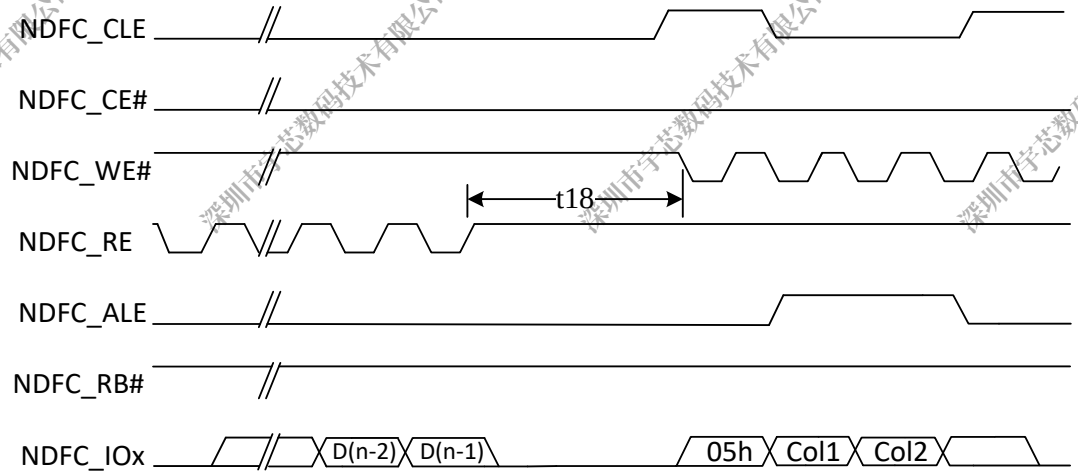


Figure 5-10. RE# High to WE# Low Timing Diagram

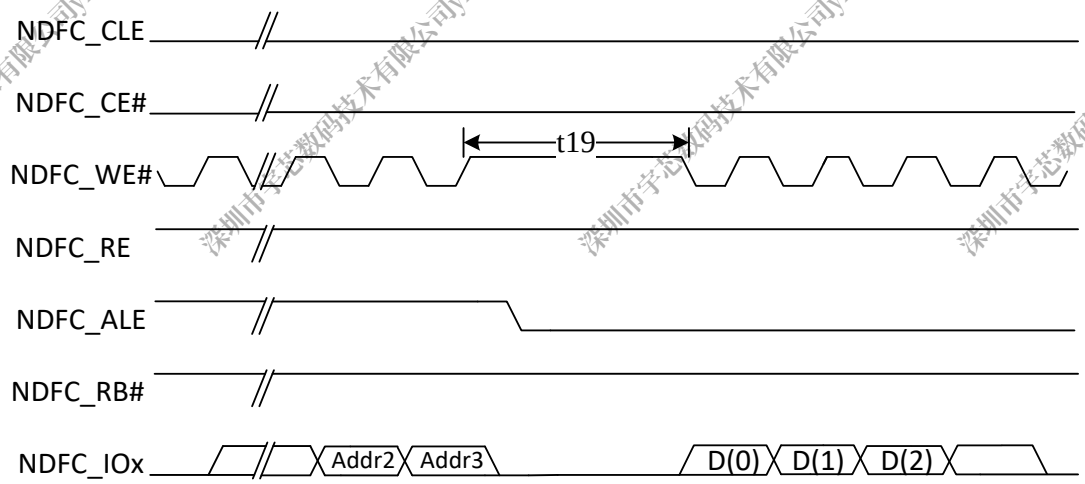


Figure 5-11. Address to Data Loading Timing Diagram

Timing cycle list:

ID	Parameter	Timing	Notes
t1	NDFC_CLE setup time	2T	
t2	NDFC_CLE hold time	2T	
t3	NDFC_CE setup time	2T	

t4	NDFC_CE hold time	2T	
t5	NDFC_WE# pulse width	T(1)	
t6	NDFC_WE# hold time	T	
t7	NDFC_ALE setup time	2T	
t8	Data setup time	T	
t9	Data hold time	T	
t10	Ready to NDFC_RE# low	3T	
t11	NDFC_ALE hold time	2T	
t12	NDFC_RE# pulse width	T	
t13	NDFC_RE# hold time	T	
t14	Read cycle time	2T	
t15	Write cycle time	2T	
t16	NDFC_WE# high to R/B# busy	T_WB(2)	Specified by timing configure register (NDFC_TIMING_CFG)
t17	NDFC_WE# high to NDFC_RE# low	T_WHR(3)	Specified by timing configure register (NDFC_TIMING_CFG)
t18	NDFC_RE# high to NDFC_WE# low	T_RHW(4)	Specified by timing configure register (NDFC_TIMING_CFG)
t19	Address to Data Loading time	T_ADL(5)	Specified by timing configure register (NDFC_TIMING_CFG)

Note(1): T is the cycle of the internal clock.

Note(2),(3),(4),(5): These values are configurable in nand flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 0*2T/6*2T/14*2T/22*2T, the value of T_RHW could be 4*2T/12*2T/20*2T/28*2T, the value of T_ADL could be 0*2T/6*2T/14*2T/22*2T.

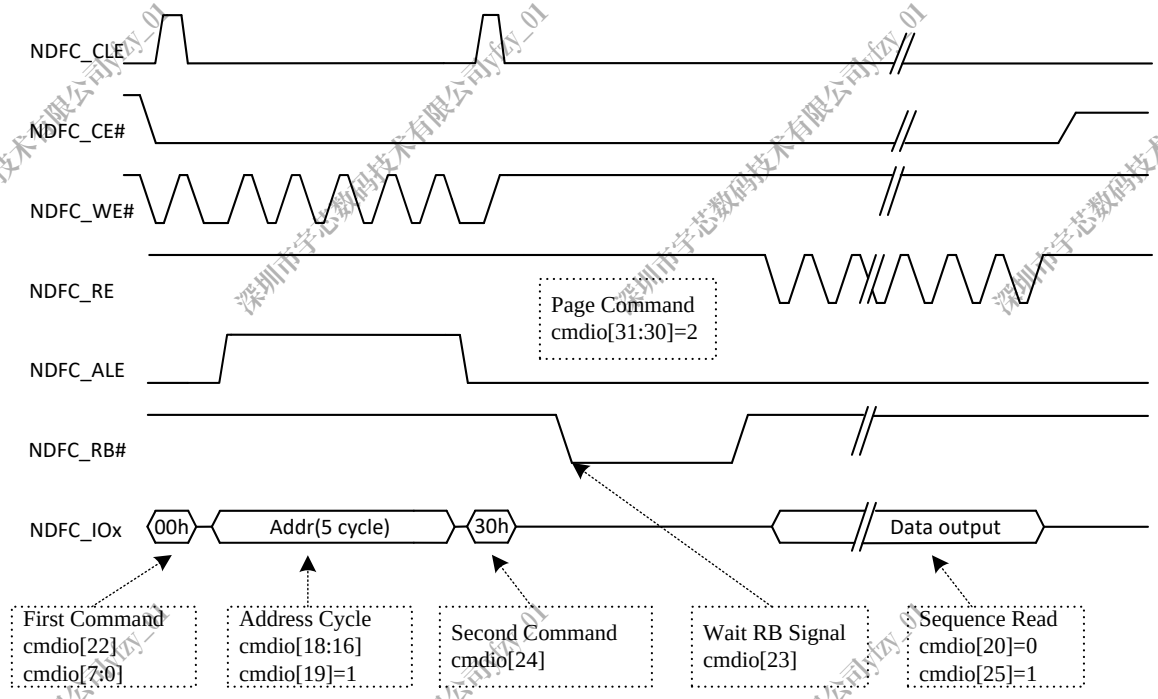


Figure 5-12. Page Read Command Diagram

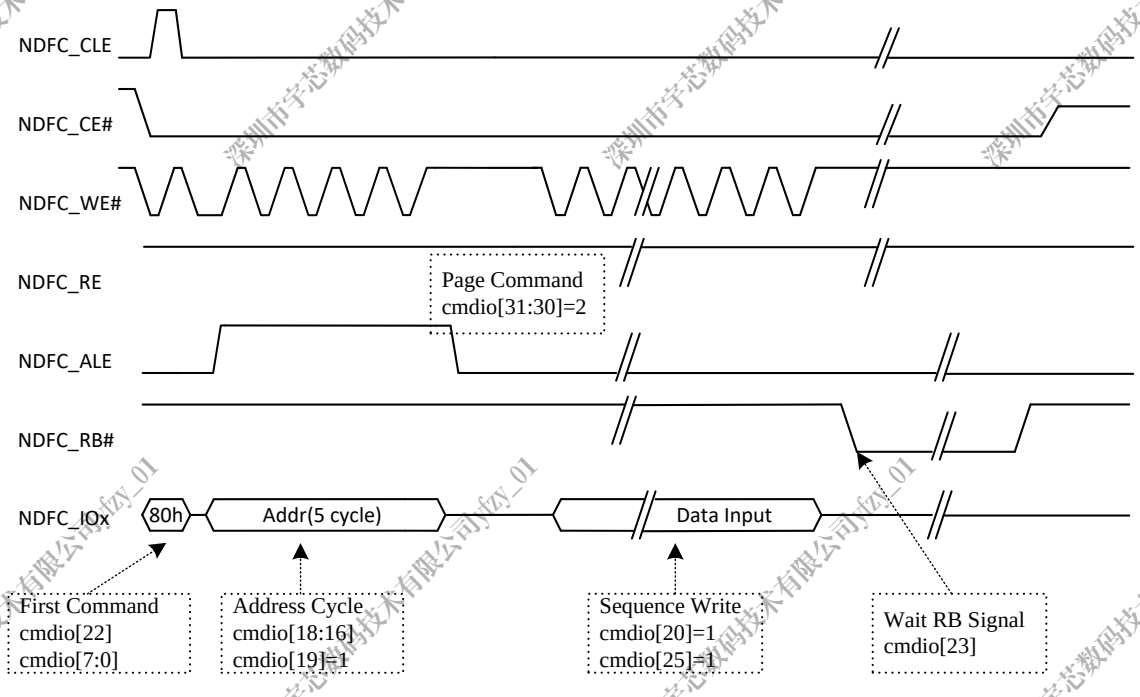


Figure 5-13. Page Program Diagram

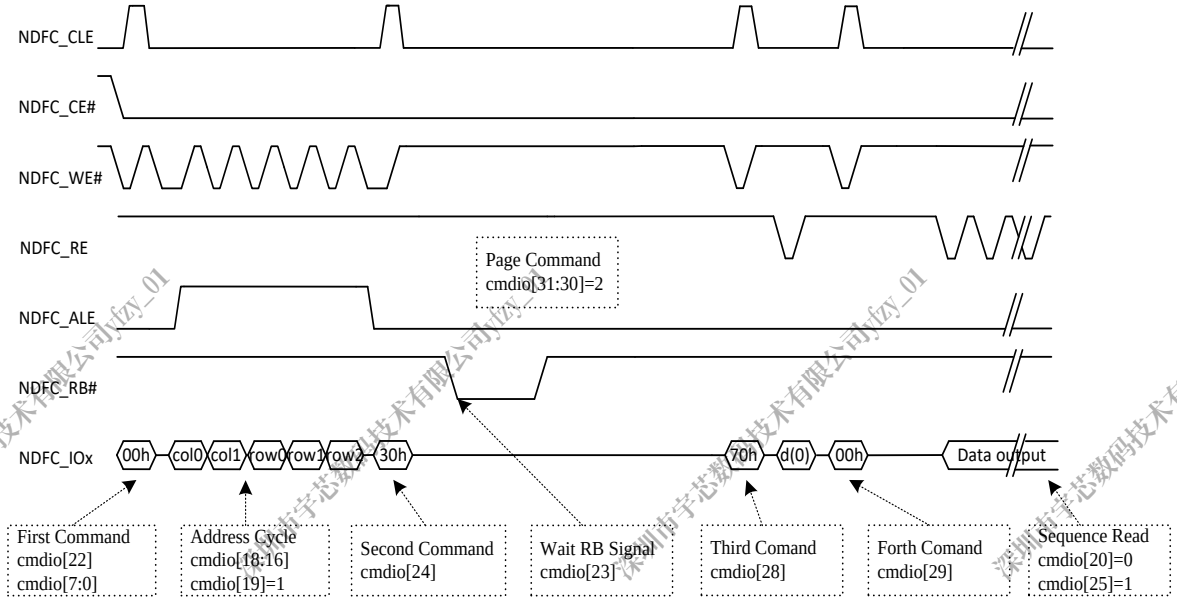


Figure 5-14. EF-NAND Page Read Diagram

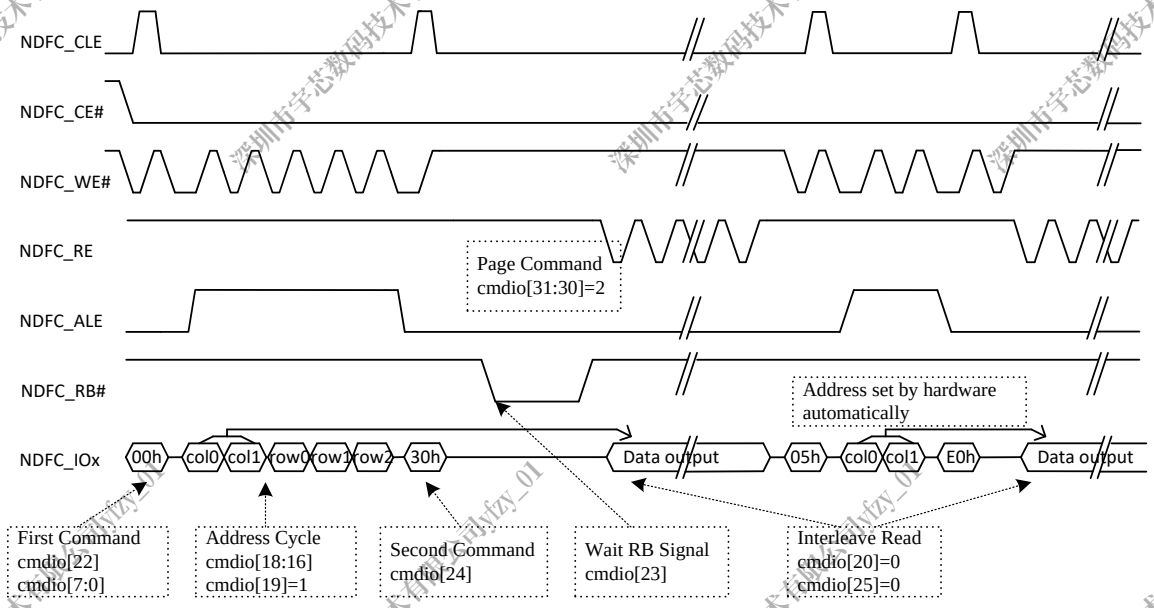


Figure 5-15. Interleave Page Read Diagram

5.2.3.4. Internal DMA Controller Descriptors

5.2.3.4.1. Descriptor Structure

NDFC internal DMA controller can transfer data between DMA FIFO in NDFC and DMA buffer in host memory using DMA descriptors. DMA descriptors reside in the host memory with chain structure is shown in Figure 5-16.

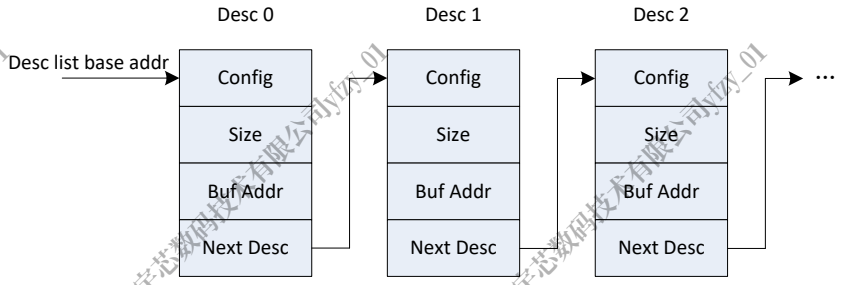


Figure 5-16. Internal DMA Descriptor Chain Structure

The start address of DMA descriptor list must be word (32-bit) aligned, and will be configured to NDFC DMA Descriptor List Base Address Register. Each DMA descriptor is consisted of four words(32-bit).

5.2.3.4.2. Descriptor Definition

Config	
Bit	**Description**
31:4	/
3	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first descriptor.

2	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1:0	/

Size	
Bit	**Description**
31:16	/
15:0	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 8 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

Buff Addr	
Bit	**Description**
31:0	BUFF_ADDR These bits indicate the physical address of DMA data buffer in host memory. The buffer address must be 4 bytes aligned.

Next Description	
Bit	**Description**
31:0	NEXT_DESC_ADDR These bits indicate the pointer to the physical host memory where the next descriptor is present.

5.2.4. Programming Guidelines

5.2.4.1. **NDFC Data Block Mask Register**

ECC_DATA_BLOCK is written or read through the value of NDFC Data Block Mask Register.But in real application scenario, capacity can not possibly waste, so writing operation does not use the function,only reading operation uses. In reading operation, we divides Sequence mode and Interleave mode through the store position of user_data.

Sequence mode: The user_data of every 1K main area data and ECC encoder data are next to main area data.

Interleave mode: All user_data and ECC encoder data are stored from page_size position.

When any ECC_DATA_BLOCK within page is read through batch command(NDFC_CMD_TYPE in 0x24 register is 0x10), the register is used differently for Sequence mode and Interleave mode.

Sequence mode can only support continue ECC_DATA_BLOCK,the register value can only be 0x1,0x3,0x7,etc.But Interleave mode has not limit.

Whether Sequence mode or Interleave mode, the first read ECC_DATA_BLOCK is used to calculate corresponding column address, and column address is written to 0x14 and 0x18 register.

5.2.4.2. **NDFC Enhanced Feature Register**

The bit[24] and bit[23:16] of the register are used to judge if free space need be padded random data except valid data when batch command function is used.

Take a SanDisk chip(SDTNQGAMA-008G) as an example:

Refer to the specification of the SanDisk chip, the page_size of the SanDisk chip is (16384+1280) bytes, but BCH level uses

40bit/1K, if user_data is 32 bytes, then the used space is 1152 bytes(14*40/8*16+32), the 128 bytes (1280-1152) space is not written. If there need be filled with 1 page, then the bit[24] of the register can be set to 1, and the bit[23:16] is written to 0x80, that the controller can automatically pad 128 bytes random data.

NOTE

Make sure that random function is enabled if there need be sent random data,that is, the NDFC_RANDOM_EN of 0x34 register is 0x1, or else the padding data is non-random, is all-0.

5.2.5. Register List

Module Name	Base Address
NDFC	0x04011000

Register Name	Offset	Description
NDFC_CTL	0x0000	NDFC Configure and Control Register
NDFC_ST	0x0004	NDFC Status Information Register
NDFC_INT	0x0008	NDFC Interrupt Control Register
NDFC_TIMING_CTL	0x000C	NDFC Timing Control Register
NDFC_TIMING_CFG	0x0010	NDFC Timing Configure Register
NDFC_ADDR_LOW	0x0014	NDFC Low Word Address Register
NDFC_ADDR_HIGH	0x0018	NDFC High Word Address Register
NDFC_DATA_BLOCK_MASK	0x001C	NDFC Data Block Mask Register
NDFC_CNT	0x0020	NDFC Data Counter Register
NDFC_CMD	0x0024	NDFC Commands IO Register
NDFC_RCMD_SET	0x0028	NDFC Read Command Set Register
NDFC_WCMD_SET	0x002C	NDFC Write Command Set Register
NDFC_ECC_CTL	0x0034	NDFC ECC Control Register
NDFC_ECC_ST	0x0038	NDFC ECC Status Register
NDFC_DATA_PAT_STA	0x003C	NDFC Data Pattern Status Register
NDFC_EFR	0x0040	NDFC Enhanced Feature Register
NDFC_RDATA_STA_CTL	0x0044	NDFC Read Data Status Control Register
NDFC_RDATA_STA_0	0x0048	NDFC Read Data Status Register 0
NDFC_RDATA_STA_1	0x004C	NDFC Read Data Status Register 1
NDFC_ERR_CNT_N	0x0050+0x04*N	NDFC Error Counter Register(N from 0 to 7)
NDFC_USER_DATA_LEN_N	0x0070+0x04*N	NDFC User Data Length Register(N from 0 to 3)
NDFC_USER_DATA_N	0x0080+0x04*N	NDFC User Data Field Register N (N from 0 to 31)
NDFC_EFNAND_STA	0x0110	NDFC EFNAND Status Register
NDFC_SPARE_AREA	0x0114	NDFC Spare Area Register
NDFC_PAT_ID	0x0118	NDFC Pattern ID Register
NDFC_DDR2_SPEC_CTL	0x011C	NDFC DDR2 Specific Control Register
NDFC_NDMA_MODE_CTL	0x0120	NDFC Normal DMA Mode Control Register
NDFC_MDMA_DLBA_REG	0x0200	NDFC MBUS DMA Descriptor List Base Address Register
NDFC_MDMA_STA	0x0204	NDFC MBUS DMA Interrupt Status Register
NDFC_DMA_INT_MASK	0x0208	NDFC MBUS DMA Interrupt Enable Register

NDFC_MDMA_CUR_DESC_ADDR	0x020C	NDFC MBUS DMA Current Descriptor Address Register
NDFC_MDMA_CUR_BUF_ADDR	0x0210	NDFC MBUS DMA Current Buffer Address Register
NDFC_DMA_CNT	0x0214	NDFC DMA Byte Counter Register
NDFC_IO_DATA	0x0300	NDFC Input/Output Data Register

5.2.6. Register Description

5.2.6.1. NDFC Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: NDFC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	NDFC_DDR_TYPE The type of DDR data interface. This bit is valid when NF_TYPE is 0x2 or 0x3. 0: DDR 1: DDR2
27:24	R/W	0x0	NDFC_CE_SEL Chip Select for NAND Flash Chips 0000: NDFC Select Chip 0 0001: NDFC Select Chip 1 0010: NDFC Select Chip 2 0011: NDFC Select Chip 3 0100: NDFC Select Chip 4 0101: NDFC Select Chip 5 0110: NDFC Select Chip 6 0111: NDFC Select Chip 7 1000: NDFC Select Chip 8 1001: NDFC Select Chip 9 1010: NDFC Select Chip 10 1011: NDFC Select Chip 11 1100: NDFC Select Chip 12 1101: NDFC Select Chip 13 1110: NDFC Select Chip 14 1111: NDFC Select Chip 15
23:22	/	/	/
21	R/W	0x0	NDFC_DDR_RM DDR Repeat Data Mode 0: Lower byte 1: Higher byte
20	R/W	0x0	NDFC_DDR_REN DDR Repeat Enable 0: Disable 1: Enable
19:18	R/W	0x0	NF_TYPE NAND Flash Type

			00: Normal SDR NAND 01: Reserved 10: ONFI DDR NAND 11: Toggle DDR NAND
17	R/W	0x0	NDFC_CLE_POL NDFC Command Latch Enable (CLE) Signal Polarity Select 0: High active 1: Low active
16	R/W	0x0	NDFC_ALE_POL NDFC Address Latch Enable (ALE) Signal Polarity Select 0: High active 1: Low active
15	R/W	0x0	NDFC_DMA_TYPE 0: Dedicated DMA 1: Normal DMA
14	R/W	0x0	NDFC_RAM_METHOD Access internal RAM method 0: Access internal RAM by AHB method 1: Access internal RAM by DMA method
13:12	/	/	/
11:8	R/W	0x0	NDFC_PAGE_SIZE 000: 1KB 001: 2KB 010: 4KB 011: 8KB 100: 16KB 101: 32KB The page size is for main field data.
7	/	/	/
6	R/W	0x0	NDFC_CE_ACT Chip Select Signal CE# Control during NAND operation 0: De-active Chip Select Signal NDFC_CE# during data loading, serial access and other no operation stage for power consumption. NDFC automatic control Chip Select Signals. 1: Chip select signal NDFC_CE# is always active after NDFC is enabled
5	/	/	/
4:3	R/W	0x0	NDFC_RB_SEL NDFC External R/B Signal Select The value 0-3 selects the external R/B signal. The same R/B signal can be used for multiple chip select flash.
2	R/W	0x0	NDFC_BUS_WIDTH 0: 8-bit bus 1: 16-bit bus
1	R/W1C	0x0	NDFC_RESET NDFC Reset Write 1 to reset NDFC and clear to 0 after reset

0	R/W	0x0	NDFC_EN NDFC Enable Control 0: Disable NDFC 1: Enable NDFC

5.2.6.2. **NDFC Status Register (Default Value: 0x0000_0F00)**

Offset: 0x0004			**Register Name: NDFC_ST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	NDFC_RDATA_STA_0 0: The number of bit 1 during current read operation is more than threshold value. 1: The number of bit 1 during current read operation is less than or equal to threshold value. This field only is valid when NDFC_RDATA_STA_EN is 1. The threshold value is configured in NDFC_RDATA_STA_TH.
12	R	0x0	NDFC_RDATA_STA_1 0: The number of bit 0 during current read operation is more than threshold value. 1: The number of bit 0 during current read operation is less than or equal to the threshold value. This field only is valid when NDFC_RDATA_STA_EN is 1. The threshold value is configured in NDFC_RDATA_STA_TH.
11	R	0x1	NDFC_RB_STATE3 NAND Flash R/B 3 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
10	R	0x1	NDFC_RB_STATE2 NAND Flash R/B 2 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
9	R	0x1	NDFC_RB_STATE1 NAND Flash R/B 1 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
8	R	0x1	NDFC_RB_STATE0 NAND Flash R/B 0 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
7:5	/	/	/
4	R	0x0	NDFC_STA 0: NDFC FSM in IDLE state 1: NDFC FSM in BUSY state When NDFC_STA is 0, NDFC can accept new command and process command.

3	R	0x0	NDFC_CMD_FIFO_STATUS 0: Command FIFO not full and can receive new command 1: Full and waiting NDFC to process commands in FIFO Since there is only one 32-bit FIFO for command. When NDFC latches one command, command FIFO is free and can accept another new command.
2	R/W1C	0x0	NDFC_DMA_INT_FLAG When it is 1, it means that a pending DMA is completed. It will be cleared after writing 1 to this bit or it will be automatically cleared before FSM processing an new command.
1	R/W1C	0x0	NDFC_CMD_INT_FLAG When it is 1, it means that NDFC has finished one Normal Command Mode or one Batch Command Work Mode. It will be cleared after writing 1 to this bit or it will be automatically cleared before FSM processing an new command.
0	R/W1C	0x0	NDFC_RB_B2R When it is 1, it means that NDFC_R/B# signal is transferred from BUSY state to READY state. It will be cleared after writing 1 to this bit.

5.2.6.3. **NDFC Interrupt and DMA Enable Register(Default Value: 0x0000_0000)**

Offset: 0x0008			**Register Name: NDFC_INT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	NDFC_DMA_INT_ENABLE Enable or disable interrupt when a pending DMA is completed.
1	R/W	0x0	NDFC_CMD_INT_ENABLE Enable or disable interrupt when NDFC has finished the procession of a single command in Normal Command Work Mode or one Batch Command Work Mode. 0: Disable 1: Enable
0	R/W	0x0	NDFC_B2R_INT_ENABLE Enable or disable interrupt when NDFC_RB# signal is transferring from BUSY state to READY state 0: Disable 1: Enable

5.2.6.4. **NDFC Timing Control Register(Default Value: 0x0000_0000)**

Offset: 0x000C			**Register Name: NDFC_TIMING_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	NDFC_READ_PIPE In SDR mode: 00: Normal

			01: EDO 10: E-EDO Others: Reserved In DDR mode: 1~15 is valid.(These bits configure the number of clock when data is valid after RE#'s falling edge)
7:6	/	/	/
5:0	R/W	0x0	NDFC_DC_CTL NDFC Delay Chain Control. (These bits are only valid in DDR data interface, and configure the relative phase between DQS and DQ[0…7])

5.2.6.5. **NDFC Timing Configure Register(Default Value: 0x0000_0095)**

Offset: 0x0010			**Register Name: NDFC_TIMING_CFG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	T_WC Write Cycle Time 00: 1*2T 01: 2*2T 10: 3*2T 11: 4*2T
17:16	R/W	0x0	T_CCS Change Column Setup Time 00: 12*2T 01: 20*2T 10: 28*2T 11: 60*2T
15:14	R/W	0x0	T_CLHZ CLE High to Output Hi-z 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
13:12	R/W	0x0	T_CS CE Setup Time 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
11	R/W	0x0	T_CDQSS DQS Setup Time for data input start 0: 4*2T 1: 20*2T

10:8	R/W	0x0	T_CAD Command, Address, Data Delay 000: 2*2T 001: 6*2T 010: 10*2T 011: 14*2T 100: 22*2T 101: 30*2T 110/111: 62*2T
7:6	R/W	0x2	T_RHW RE# high to WE# low cycle number 00: 4*2T 01: 12*2T 10: 20*2T 11: 28*2T
5:4	R/W	0x1	T_WHR WE# high to RE# low cycle number 00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
3:2	R/W	0x1	T_ADL Address to Data Loading cycle number 00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
1:0	R/W	0x1	T_WB WE# high to busy cycle number 00:14*2T 01: 22*2T 10: 30*2T 11: 38*2T

5.2.6.6. **NDFC Address Low Word Register(Default Value: 0x0000_0000)**

Offset: 0x0014			**Register Name: NDFC_ADDR_LOW**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA4 NAND Flash 4th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA3 NAND Flash 3rd Cycle Address Data
15:8	R/W	0x0	ADDR_DATA2 NAND Flash 2nd Cycle Address Data
7:0	R/W	0x0	ADDR_DATA1

			NAND Flash 1st Cycle Address Data

5.2.6.7. **NDFC Address High Word Register (Default Value: 0x0000_0000)**

Offset: 0x0018			**Register Name: NDFC_ADDR_HIGH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA8 NAND Flash 8th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA7 NAND Flash 7th Cycle Address Data
15:8	R/W	0x0	ADDR_DATA6 NAND Flash 6th Cycle Address Data
7:0	R/W	0x0	ADDR_DATA5 NAND Flash 5th Cycle Address Data

5.2.6.8. **NDFC Data Block Mask Register(Default Value: 0x0000_0000)**

Offset: 0x001C			**Register Name: NDFC_DATA_BLOCK_MASK**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 31 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
30	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 30 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
29	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 29 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
28	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 28 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
27	R/W	0x0	NDFC_DATA_BLOCK_MASK

			It is used to indicate the data block 27 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
26	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 26 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
25	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 25 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
24	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 24 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
23	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 23 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
22	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 22 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
21	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 21 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
20	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 20 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable

			1 data block = 1024 bytes main field data.
19	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 19 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
18	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 18 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
17	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 17 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
16	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 16 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
15	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 15 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
14	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 14 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
13	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 13 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
12	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 12 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**).

			0: Disable 1: Enable 1 data block = 1024 bytes main field data.
11	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 11 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
10	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 10 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
9	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 9 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
8	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 8 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
7	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 7 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
6	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 6 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
5	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 5 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
4	R/W	0x0	NDFC_DATA_BLOCK_MASK

			It is used to indicate the data block 4 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
3	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 3 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
2	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 2 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
1	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 1 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
0	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 0 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.

5.2.6.9. **NDFC Data Counter Register(Default Value: 0x0000_0000)**

Offset: 0x0020			**Register Name: NDFC_CNT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	NDFC_DATA_CNT Transfer Data Byte Counter The length can be set from 1 byte to 1024 bytes. However, 1024 bytes is set when it is zero.

5.2.6.10. **NDFC Command IO Register (Default Value: 0x0000_0000)**

Offset: 0x0024			**Register Name: NDFC_CMD**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:30	R/W	0x0	NDFC_CMD_TYPE 00: Common command for normal operation 01: Special command for Flash spare field operation 10: Page command for batch process operation 11: Reserved
29	R/W	0x0	NDFC_SEND_FOURTH_CMD 0: Donot send third set command 1: Send it on the external memory's bus It is used for EF-NAND page read.
28	R/W	0x0	NDFC_SEND_THIRD_CMD 0: Donot send third set command 1: Send it on the external memory's bus It is used for EF-NAND page read.
27	R/W	0x0	NDFC_SEND_RANDOM_CMD2_CTL 0: Donot send random cmd2 (NDFC_RANDOM_CMD2) 1: Send random cmd2 **NOTE** It is only valid in batch cmd operation and writing operation.
26	R/W	0x0	NDFC_DATA_METHOD Data swap method when the internal RAM and system memory It is only active for common command and special command. 0: No action 1: DMA transfer automatically It only is active when NDFC_RAM_METHOD is 1. If this bit is set to 1, NDFC should setup DRQ to fetching data before output to Flash or NDFC should setup DRQ to sending out to system memory after fetching data from Flash. If this bit is set to 0, NDFC output the data in internal RAM or do nothing after fetching data from Flash.
25	R/W	0x0	NDFC_SEQ User data & BCH check word position. It only is active for Page Command, donot care about this bit for other two commands. 0: Interleave Method (on page spare area) 1: Sequence Method (following data block)
24	R/W	0x0	NDFC_SEND_SECOND_CMD 0: Donot send second set command 1: Send it on the external memory's bus
23	R/W	0x0	NDFC_WAIT_FLAG 0: NDFC can transfer data regardless of the internal NDFC_RB wire 1: NDFC can transfer data when the internal NDFC_RB wire is READY; otherwise it cannot when the internal NDFC_RB wire is BUSY.
22	R/W	0x0	NDFC_SEND_FIRST_CMD 0: Donot send first set command 1: Send it on the external memory's bus
21	R/W	0x0	NDFC_DATA_TRANS

			0: No data transfer on external memory bus 1: Data transfer and direction is decided by the field NDFC_ACCESS_DIR
20	R/W	0x0	NDFC_ACCESS_DIR 0: Read NAND Flash 1: Write NAND Flash
19	R/W	0x0	NDFC_SEND_ADR 0: Donot send ADDRESS 1: Send N cycles ADDRESS, the number N is specified by NDFC_ADR_NUM field
18:16	R/W	0x0	NDFC_ADR_NUM Address Cycles' Number 000: 1 cycle address field 001: 2 cycles address field 010: 3 cycles address field 011: 4 cycles address field 100: 5 cycles address field 101: 6 cycles address field 110: 7 cycles address field 111: 8 cycles address field
15:10	/	/	/
9:8	R/W	0x0	NDFC_ADR_NUM_IN_PAGE_CMD The number of address cycles during page command. 00: 2 address cycles 11: 5 address cycles Others: reserved
7:0	R/W	0x0	NDFC_CMD_LOW_BYTE NDFC command low byte data This command will be sent to external Flash by NDFC.

5.2.6.11. **NDFC Command Set Register 0(Default Value: 0x00E0_0530)**

Offset: 0x0028			**Register Name: NDFC_CMD_SET0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x00	NDFC_RANDOM_CMD2 Used for Batch Operation
23:16	R/W	0xE0	NDFC_RANDOM_READ_CMD1 Used for Batch Read Operation
15:8	R/W	0x05	NDFC_RANDOM_READ_CMD0 Used for Batch Read Operation
7:0	R/W	0x30	NDFC_READ_CMD Used for Batch Read Operation

5.2.6.12. **NDFC Command Set Register 1(Default Value: 0x7000_8510)**

Offset: 0x002C	**Register Name: NDFC_CMD_SET1**

Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x70	NDFC_READ_CMD0 Used for EF-NAND Page Read Operation
23:16	R/W	0x00	NDFC_READ_CMD1 Used for EF-NAND Page Read Operation
15:8	R/W	0x85	NDFC_RANDOM_WRITE_CMD Used for Batch Write Operation
7:0	R/W	0x10	NDFC_PROGRAM_CMD Used for Batch Write Operation

5.2.6.13. **NDFC ECC Control Register(Default Value: 0x4A80_0008)**

Offset: 0x0034			Register Name: NDFC_ECC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R/W	0x4a80	NDFC_RANDOM_SEED The seed value for randomize engine. It is only active when NDFC_RANDOM_EN is set to '1'.
15:8	R/W	0x0	NDFC_ECC_MODE 00000000: BCH-16 00000001: BCH-24 00000010: BCH-28 00000011: BCH-32 00000100: BCH-40 00000101: BCH-44 00000110: BCH-48 00000111: BCH-52 00001000: BCH-56 00001001: BCH-60 00001010: BCH-64 00001011: BCH-68 00001100: BCH-72 00001101: BCH-76 00001110: BCH-80 Others : Reserved
7	R/W	0x0	NDFC_RANDOM_SIZE 0: ECC block size 1: Page size
6	R/W	0x0	NDFC_RANDOM_DIRECTION 0: LSB first 1: MSB first
5	R/W	0x0	NDFC_RANDOM_EN 0: Disable Data Randomize 1: Enable Data Randomize
4	R/W	0x0	NDFC_ECC_EXCEPTION

			0: Normal ECC 1: For ECC, there is an exception. If all data is 0xff or 0x00 for the block. When reading this page, ECC assumes that it is right. For this case, no error information is reported. It only is active when ECC is ON.
3	R/W	0x1	NDFC_ECC_PIPELINE Pipeline function enable or disable for batch command 0: Error Correction function no pipeline with next block operation 1: Error Correction pipeline
2:1	/	/	/
0	R/W	0x0	NDFC_ECC_EN 0: ECC is OFF 1: ECC is ON

5.2.6.14. **NDFC ECC Status Register(Default Value: 0x0000_0000)**

Offset: 0x0038			**Register Name: NDFC_ECC_ST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 31 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[31] of this register is corresponding the 31th ECC data block. 1 ECC Data Block = 1024 bytes.
30	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 30 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[30] of this register is corresponding the 30th ECC data block. 1 ECC Data Block = 1024 bytes.
29	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 29 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[29] of this register is corresponding the 29th ECC data block. 1 ECC Data Block = 1024 bytes.
28	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 28 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[28] of this register is corresponding the 28th ECC data block. 1 ECC Data

			Block = 1024 bytes.
27	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 27 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[27] of this register is corresponding the 27th ECC data block. 1 ECC Data Block = 1024 bytes.
26	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 26 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[26] of this register is corresponding the 26th ECC data block. 1 ECC Data Block = 1024 bytes.
25	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 25 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[25] of this register is corresponding the 25th ECC data block. 1 ECC Data Block = 1024 bytes.
24	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 24 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[24] of this register is corresponding the 24th ECC data block. 1 ECC Data Block = 1024 bytes.
23	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 23 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[23] of this register is corresponding the 23th ECC data block. 1 ECC Data Block = 1024 bytes.
22	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 22 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[22] of this register is corresponding the 22th ECC data block. 1 ECC Data Block = 1024 bytes.
21	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 21 0: ECC can correct these error bits or there is no error bit

			1: Error bits number beyond of ECC correction capability and cannot correct them The bit[21] of this register is corresponding the 21th ECC data block. 1 ECC Data Block = 1024 bytes.
20	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 20 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[20] of this register is corresponding the 20th ECC data block. 1 ECC Data Block = 1024 bytes.
19	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 19 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[19] of this register is corresponding the 19th ECC data block. 1 ECC Data Block = 1024 bytes.
18	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 18 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[18] of this register is corresponding the 18th ECC data block. 1 ECC Data Block = 1024 bytes.
17	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 17 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[17] of this register is corresponding the 17th ECC data block. 1 ECC Data Block = 1024 bytes.
16	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 16 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[16] of this register is corresponding the 16th ECC data block. 1 ECC Data Block = 1024 bytes.
15	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 15 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[15] of this register is corresponding the 15th ECC data block. 1 ECC Data Block = 1024 bytes.

14	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 14 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[14] of this register is corresponding the 14th ECC data block. 1 ECC Data Block = 1024 bytes.
13	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 13 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[13] of this register is corresponding the 13th ECC data block. 1 ECC Data Block = 1024 bytes.
12	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 12 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[12] of this register is corresponding the 12th ECC data block. 1 ECC Data Block = 1024 bytes.
11	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 11 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[11] of this register is corresponding the 11th ECC data block. 1 ECC Data Block = 1024 bytes.
10	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 10 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[10] of this register is corresponding the 10th ECC data block. 1 ECC Data Block = 1024 bytes.
9	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 9 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[9] of this register is corresponding the 9th ECC data block. 1 ECC Data Block = 1024 bytes.
8	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 8 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct

			them The bit[8] of this register is corresponding the 8th ECC data block. 1 ECC Data Block = 1024 bytes.
7	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 7 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[7] of this register is corresponding the 7th ECC data block. 1 ECC Data Block = 1024 bytes.
6	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 6 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[6] of this register is corresponding the 6th ECC data block. 1 ECC Data Block = 1024 bytes.
5	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 5 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[5] of this register is corresponding the 5th ECC data block. 1 ECC Data Block = 1024 bytes.
4	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 4 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[4] of this register is corresponding the 4th ECC data block. 1 ECC Data Block = 1024 bytes.
3	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 3 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[3] of this register is corresponding the 3rd ECC data block. 1 ECC Data Block = 1024 bytes.
2	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 2 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[2] of this register is corresponding the 2nd ECC data block. 1 ECC Data Block = 1024 bytes.
1	R	0x0	NDFC_ECC_ERR

			Error information bit of Data Block 1 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[1] of this register is corresponding the 1st ECC data block. 1 ECC Data Block = 1024 bytes.
0	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 0 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[0] of this register is corresponding the 0 ECC data block. 1 ECC Data Block = 1024 bytes.

5.2.6.15. **NDFC Data Pattern Status Register(Default Value: 0x0000_0000)**

Offset: 0x003C			**Register Name: NDFC_DATA_PAT_STA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 31 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
30	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 30 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
29	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 29 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
28	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 28 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
27	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 27 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
26	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 26 when read from external NAND flash.

			0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
25	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 25 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
24	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 24 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
23	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 23 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
22	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 22 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
21	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 21 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
20	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 20 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
19	R	0x0	Special pattern (all 0x00 or all 0xff) found Flag for Data Block 19 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
18	R	0x0	Special pattern (all 0x00 or all 0xff) Found flag for Data Block 18 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
17	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 17 when read from external NAND flash. 0: No found

			1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
16	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 16 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
15	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 15 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
14	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 14 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
13	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 13 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
12	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 12 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
11	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 11 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
10	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 10 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
9	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 9 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
8	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 8 when read from external NAND flash. 0: No found 1: Special pattern is found

			The register of NDFC_PAT_ID would indicate which kind of pattern is found.
7	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 7 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
6	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 6 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
5	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 5 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
4	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 4 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
3	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 3 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
2	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 2 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
1	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 1 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
0	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 0 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.

5.2.6.16. NDFC Enhanced Feature Register(Default Value: 0x0000_0000)

Offset: 0x0040	Register Name: NDFC_EFR

Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DB_CNT_EN Dummy_Byte_Count_EN 0:Disable fill Dummy Byte. 1:Enable fill Dummy Byte.
23:16	R/W	0x0	DB_CNT Dummy_Byte_Count After PAGE CMD operation finishing sending out the main data , user data and ECC code, controller would send dummy byte to fill the unused space in one page. **NOTE** It is only valid in PAGE CMD operation(**NDFC_CMD_TYPE**=0x3), and this function is disabled when **Dummy_Byte_Count_EN** is 0. If the **NDFC_RANDOM_EN** = 0x0, the value of the dummy byte is 0, so in order to improve the stability, when using this function , it is better to set the **NDFC_RANDOM_EN** to 0x1.
15:9	/	/	/
8	R/W	0x0	NDFC_WP_CTRL NAND Flash Write Protect Control Bit 0: Write Protect is active 1: Write Protect is not active When this bit is '0', WP signal line is low level and external NAND flash is on protected state.
7	/	/	/
6:0	R/W	0x0	NDFC_ECC_DEBUG For the purpose of debugging ECC engine, special error bits are inserted before writing external Flash Memory. 0: No error is inserted (ECC Normal Operation) n: N bits error are inserted

5.2.6.17. **NDFC Read Data Status Control Register(Default Value: 0x0100_0000)**

Offset: 0x0044			Register Name: NDFC_RDATA_STA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x1	NDFC_RDATA_STA_EN 0: Disable to count the number of bit 1 and bit 0 during current read operation 1: Enable to count the number of bit 1 and bit 0 during current read operation The number of bit 1 and bit 0 during current read operation can be used to check whether a page is blank or bad.
23:19	/	/	/
18:0	R/W	0x0	NDFC_RDATA_STA_TH The threshold value to generate data status

			If the number of bit 1 during current read operation is less than or equal to threshold value, the bit 13 of NDFC_ST register will be set. If the number of bit 0 during current read operation is less than or equal to threshold value, the bit 12 of NDFC_ST register will be set.

5.2.6.18. **NDFC Read Data Status Register 0(Default Value: 0x0000_0000)**

Offset: 0x0048			Register Name: NDFC_RDATA_STA_0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_1 The number of input bit 1 during current command. It will be cleared automatically when next command is executed.

5.2.6.19. **NDFC Read Data Status Register 1(Default Value: 0x0000_0000)**

Offset: 0x004C			Register Name: NDFC_RDATA_STA_1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_0 The number of input bit 0 during current command. It will be cleared automatically when next command is executed.

5.2.6.20. **NDFC Error Counter Register N(Default Value: 0x0000_0000)**

Offset: 0x0050+N*0x04(N=0~7)			Register Name: NDFC_ERR_CNT_N
Bit	**Read/Write**	**Default/Hex**	**Description**
[8M+7: 8M] (M=0~3)	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[N*0x04+M] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits ..... 01010000 : 80 corrected bits Others: Reserved 1 ECC Data Block =1024 bytes

5.2.6.21. **NDFC User Data Length Register N(Default Value: 0x0000_0000)**

Offset: 0x0070+N*0x04(N=0~3)			Register Name: NDFC_USER_DATA_LEN_N
Bit	**Read/Write**	**Default/Hex**	**Description**
[4M+3: 4M] (M=0~7)	R/W	0x0	It's used to indicate user data's length of ECC DATA BLOCK[0x08*N+M]. 0000 : no user data 0001 : 4 bytes user data

			0010 : 8 bytes user data 0011 : 12 bytes user data 0100 : 16 bytes user data 0101 : 20 bytes user data 0110 : 24 bytes user data 0111 : 28 bytes user data 1000 : 32 bytes user data Other : reserved

5.2.6.22. NDFC User Data Register N(Default Value: 0xFFFF_FFFF)

Offset: 0x0080 + N*0x04(N=0~31)			Register Name: NDFC_USER_DATA_N
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xffffffff	USER_DATA All of the user data in one page is stored in NDFC_USER_DATA_N. The start register address of each ECC DATA BLOCK's user data is determined by its length configured in NDFC_USER_DATA_LEN_N. For example: ECC DATA BLOCK[0] user data len = 8 Bytes, address = 0x80 ECC DATA BLOCK[1] user data len = 0 Bytes, ECC DATA BLOCK[2] user data len = 4 Bytes, address = 0x80+8 ECC DATA BLOCK[3] user data len = 4 Bytes, address = 0x80+8+4 ECC DATA BLOCK[4] user data len = 0 Bytes ECC DATA BLOCK[5] user data len = 16 Bytes, address = 0x80+8+4+4 ECC DATA BLOCK[6] user data len = 0 Bytes ECC DATA BLOCK[7] user data len = 0 Bytes

5.2.6.23. NDFC EFNAND Status Register(Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: NDFC_EFNAND_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	EF_NAND_STATUS The status value for EF-NAND page read operation

5.2.6.24. NDFC Spare Area Register(Default Value: 0x0000_0400)

Offset: 0x0114			Register Name: NDFC_SPARE_AREA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x400	NDFC_SPARE_ADR This value indicates the spare area first byte address for NDFC interleave page operation.

5.2.6.25. **NDFC Pattern ID Register(Default Value: 0x0000_0000)**

Offset: 0x0118			Register Name: NDFC_PAT_ID
Bit	**Read/Write**	**Default/Hex**	**Description**
n (n=0~31)	R	0x0	PAT_ID Special Pattern ID for ECC data block[n] 0: All 0x00 is found 1: All 0xFF is found

5.2.6.26. **NDFC DDR2 Specific Control Register(Default Value: 0x0000_0000)**

Offset: 0x011C			Register Name: NDFC_DDR2_SPEC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	DLEN_WR The number of latency DQS cycle for write 0000: No latency 0001: One latency DQS cycle 0010: Two latency DQS cycle 0011: Four latency DQS cycle
11:8	R/W	0x0	DLEN_RD The number of latency DQS cycle for read 0000: No latency 0001: One latency DQS cycle 0010: Two latency DQS cycle 0011: Four latency DQS cycle
7:3	/	/	/
2	R/W	0x0	EN_RE_C Enable the complementary RE# signal 0: Disable 1: Enable
1	R/W	0x0	EN_DQS_C Enable the complementary DQS signal 0: Disable 1: Enable
0	/	/	/

5.2.6.27. **NDFC Normal DMA Mode Control Register(Default Value: 0x0000_00E5)**

Offset: 0x0120			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

7:6	R/W	0x11	DMA_ACT_STA 00:dma_active is low 01:dma_active is high 10:dma_active is controlled by dma_request(DRQ) 11:dma_active is controlled by controller
5	R/W	0x1	DMA_ACK_EN 0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	DELAY_CYCLE The delay cycles The counts of hold cycles from DMA last signal high to dma_active high

5.2.6.28. **NDFC MBUS DMA Descriptor List Base Address Register(Default Value: 0x0000_0000)**

Offset: 0x0200			**Register Name: NDFC_MDMA_DLBA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_DESC_BASE_ADDR Start Address of Descriptor List Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the DMA internally. Hence these LSB bits are read-only.

5.2.6.29. **NDFC MBUS DMA Interrupt Status Register(Default Value: 0x0000_0000)**

Offset: 0x0204			**Register Name: NDFC_MDMA_STA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_TRANS_FINISH_INT Transfer Finish Interrupt Indicates that data transmission is finished for a descriptor. Writing a '1' clears this bit. Bit 0: Corresponding DMA descriptor 0 Bit 1: Corresponding DMA descriptor 1 … Bit 31: Corresponding DMA descriptor 31

5.2.6.30. **NDFC MBUS DMA Interrupt Enable Register(Default Value: 0x0000_0000)**

Offset: 0x0208			**Register Name: NDFC_DMA_INT_MASK**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_TRANS_INT_ENB Transfer Interrupt Enable When set, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled. Bit 0: Corresponding DMA descriptor 0

			Bit 1: Corresponding DMA descriptor 1 … Bit 31: Corresponding DMA descriptor 31

5.2.6.31. **NDFC MBUS DMA Current Descriptor Address Register(Default Value: 0x0000_0000)**

Offset: 0x020C			Register Name: NDFC_MDMA_CUR_DESC_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CUR_DESC_ADDR Current Descriptor Address Pointer Cleared on reset. Pointer updated by DMA during operation. This register points to the start address of the current descriptor read by the DMA.

5.2.6.32. **NDFC MBUS DMA Current Buffer Address Register(Default Value: 0x0000_0000)**

Offset: 0x0210			Register Name: NDFC_MDMA_CUR_BUF_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CUR_BUFF_ADDR Current Buffer Address Pointer Cleared on Reset. Pointer updated by DMA during operation. This register points to the current Data Buffer Address accessed by the DMA.

5.2.6.33. **NDFC DMA Byte Counter Register(Default Value: 0x0000_0000)**

Offset: 0x0214			Register Name: NDFC_DMA_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	DMA_CNT DMA data counter for DMA, only is valid for Normal DMA

5.2.6.34. **NDFC IO Data Register(Default Value: 0x0000_0000)**

Offset: 0x0300			Register Name: NDFC_IO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NDFC_IO_DATA Read/Write data into internal RAM Access unit is 32-bit.

5.3. SD/MMC Host Controller(SMHC)

5.3.1. Overview

The SD-MMC Host controller(SMHC) can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memory), UHS-I Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC.

The SMHC has the following features:

- Supports eMMC boot operation and alternative boot operation
- Supports Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- SMHC0 supports SD (Version1.0 to 3.0),4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@1.8V IO pad
- SMHC1 supports SDIO(Version1.1 to 3.0),4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@1.8V IO pad
- SMHC2 supports MMC(Version3.x to 4.2),eMMC(Version4.3-5.0,compatible with 5.1),8-bit bus width
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 100MHz@1.8V IO pad
  - DDR mode 50MHz@3.3V IO pad
- Hardware CRC generation and error detection
- Programmable baud rate
- Host pull-up control
- SDIO interrupts in 1-bit and 4-bit modes
- SDIO suspend and resume operation
- SDIO read wait
- Block size of 1 to 65535 bytes
- Descriptor-based internal DMA controller
- Internal 1KB FIFO for data transfer

5.3.2. Block Diagram

Figure 5-17 shows a block diagram of the SMHC.

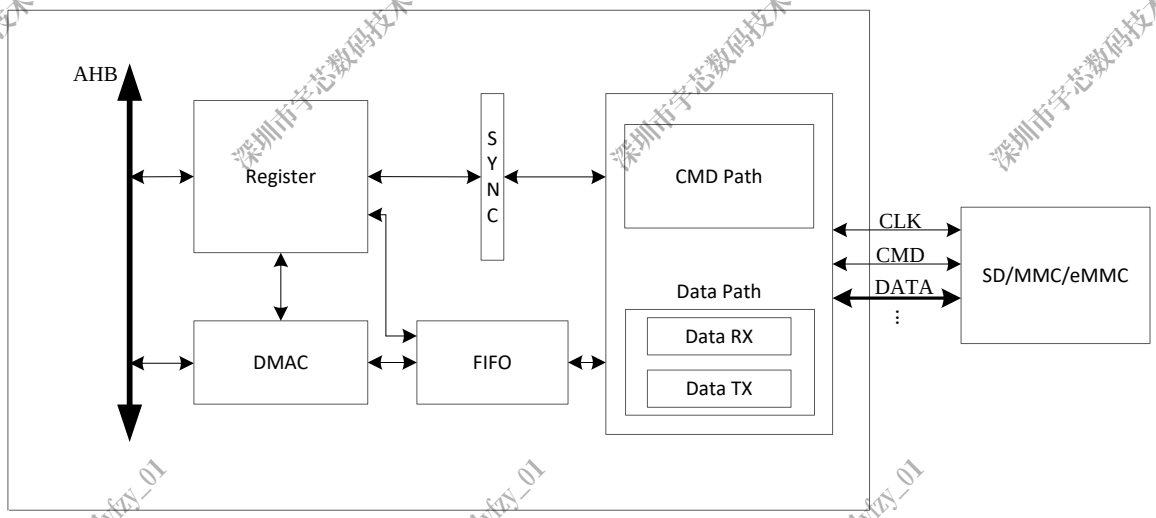


Figure 5-17. SMHC Block Diagram

5.3.3. Operations and Functional Descriptions

5.3.3.1. External Signals

Table 5-3 describes the external signals of SMHC.

Table 5-3. SMHC External Signals

Port Name	Width	Type	Description
SDC0_CLK	1	O	Clock output for SD/TF card
SDC0_CMD	1	I/O	CMD line for SD/TF card
SDC0_D[i] (i=0~3)	4	I/O	Data line for SD/TF card
SDC1_CLK	1	O	Clock output for SDIO Wi-Fi
SDC1_CMD	1	I/O	CMD line for SDIO Wi-Fi
SDC1_D[i] (i=0~3)	4	I/O	Data line for SDIO Wi-Fi
SDC2_CLK	1	O	Clock output for MMC
SDC2_CMD	1	I/O	CMD line for MMC
SDC2_D[i] (i=0~7)	8	I/O	Data line for MMC
SDC2_RST	1	O	Reset signal for MMC
SDC2_DS	1	I	Data Strobe for MMC

5.3.3.2. Clock Sources

Each SMHC gets three different clocks. User can select one of them to make SMHC clock source. Table 5-4 describes the clock sources of SMHC. Users can see CCU in chapter 3.3 for clock setting, configuration and gating information.

Table 5-4. SMHC Clock Sources

Clock Sources	Description

OSC24M	24MHz Crystal
PLL_PERIPH0(2X)	Peripheral Clock, the default value is 1.2GHz
PLL_PERIPH1(2X)	Peripheral Clock, the default value is 1.2GHz

5.3.3.3. **Timing Diagram**

Please refer to relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card(eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card(eMMC) Electrical Standard(4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard(5.0)

5.3.3.4. **Internal DMA Controller Description**

SMHC has an internal DMA controller (IDMAC) to transfer data between host memory and SMHC port. With a descriptor, IDMAC can efficiently move data from source to destination by automatically loading next DMA transfer arguments, which need less CPU intervention. Before transfer data in IDMAC, host driver should construct a descriptor list, configure arguments of every DMA transfer, then launch the descriptor and start the DMA. IDMAC has an interrupt controller, when enabled, it can interrupt the HOST CPU in situations such as data transmission completed or some errors happened.

5.3.3.4.1. IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

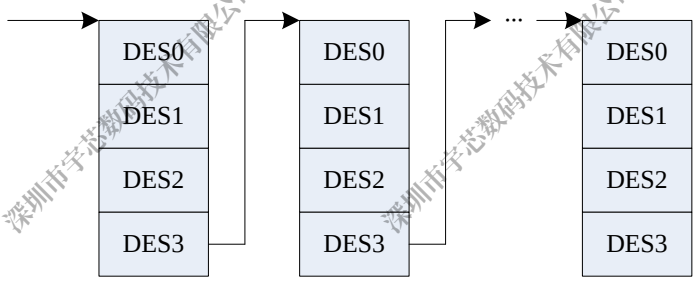


Figure 5-18. IDMAC Descriptor Structure Diagram

This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.
DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, and DES3 to denote [127:96] bits in a descriptor.

5.3.3.4.2. DES0 Definition

Bits	Name	Descriptor

31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:5	/	/
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor
0	/	/

5.3.3.4.3. DES1 Definition

For SMHC0/SMHC1

Bits	Name	Descriptor
31:16	/	/
15:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

For SMHC2

Bits	Name	Descriptor
31:13	/	/
12:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

5.3.3.4.4. DES2 Definition

Bits	Name	Descriptor

31:0	Buffer address pointer	BUFF_ADDR These bits indicate the physical address of data buffer. The IDMAC ignores DES2[1:0], corresponding to the bus width of 32.

5.3.3.4.5. DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present.

5.3.3.5. Calibrate Delay Chain

There are two delay chains in SMHC2. One is Data Strobe delay chain, which is used to generate delay to make proper timing between Data Strobe and data signals. Another is sample delay chain, which is used to generate delay to make proper timing between internal card clock signal and data signals. Each delay chain is made up with 64 delay cells.
There is only a sample delay chain in SMHC0/1.
The delay time of one delay cell can be estimated through delay chain calibration.The steps to calibrate delay chain are as follows:
Step1: Enable SMHC. In order to calibrate delay chain by operation registers in SMHC, SMHC must be enabled through **SMHC Bus Gating Reset Register** and **SMHC2 Clock Register**.

Step2: Configure a proper clock for SMHC. Calibration delay chain is based on the clock for SMHC from Clock Control Unit(CCU). Calibration delay chain is an internal function in SMHC and do not need device. So, it is unnecessary to open clock signal for device. The recommended clock frequency is 200MHz.

Step3: Set proper initial delay value. Writing 0xA0 to **delay control register** enables **Delay Software Enable** (bit[7]) and sets initial delay value 0x20 to **Delay chain**(bit[5:0]). Then write 0x0 to **delay control register** to clear the value.

Step4: Write 0x8000 to **delay control register** to start calibrate delay chain.

Step5: Wait until the flag(Bit14 in **delay control register**) of calibration done is set. The number of delay cells is shown at Bit8~Bit13 in **delay control register**. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This value is the result of calibration.
Step6: Calculate the delay time of one delay cell according to the cycle of SMHC's clock and the result of calibration.

NOTE

In the above descriptions,delay control register contains SMHC Sample Delay Control Register and SMHC Data Strobe Delay Control Register. Delay Software Enable contains Sample Delay Software Enable and Data Strobe Delay Software Enable. Delay chain contains Sample Delay Software and Data Strobe Delay Software.

5.3.4. Programming Guidelines

5.3.4.1. Initialization

Before data and command are exchanged between a card and the SMHC, the SMHC need to be initialized .The SMHC is initialized as follows.

Step1: Configure GPIO register as SMHC function by Port Controller module; reset clock by writing 1 to SMHC_BGR_REG[SMHCx_RST], open clock gating by writing 1 to SMHC_BGR_REG[SMHCx_GATING]; select clock sources and set division factor by configuring the SMHCx_CLK_REG(x=0,1,2) register.

Step2: Configure SMHC_CTRL to enable total interrupt; configure SMHC_INTMASK to 0xFFCE to enable normal interrupt and error abnormal interrupt, and register interrupt function.

Step3: Configure SMHC_CLKDIV to open clock for device; configure SMHC_CMD as change clock command(for example 0x80202000); send update clock command to deliver clock to device.

Step4: Configure SMHC_CMDARG, configure SMHC_CMD to set response type,etc, then command can send. According to initial process protocol, you can finish SMHC initializing by sending corresponding command one by one.

5.3.4.2. Writing a Single Data Block

To Write a single data block, perform the following steps:

Step1: Write 1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write 0x82 to SMHC_DMAC to enable DMAC interrupt, configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 1 data block to the first sector, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD24(Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD, send CMD24 command to write data to device.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD24 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle state. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD,go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle state,then the next command can be sent. If no, device is in busy state, then continue to send CMD13 to wait device idle until timeout exit.

5.3.4.3. Reading a Single Data Block

To read a single data block, perform the following steps:

Step1: Write 1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_DMAC to 0x82 to enable DMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive

interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 1 data block from the first sector, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD17(Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD , send CMD17 command to read data from device to DRAM/SRAM.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD17 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.3.4.4. **Writing Open-ended Multiple Data Blocks(CMD25+Auto CMD12)**

To write open-ended multiple data blocks, perform the following steps:

Step1: Write 1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_DMAC to 0x82 to enable DMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 3 data blocks to the zero sector, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25(Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD, send CMD25 command to write data to device, when data transfer is complete, CMD12 will be sent automatically .

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle state. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD,go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle state,then the next command can be sent. If no, device is in busy state, then continue to send CMD13 to wait device idle until timeout exit.

5.3.4.5. **Reading Open-ended Multiple Data Blocks(CMD18+Auto CMD12)**

To read open-ended multiple data blocks, perform the following steps:

Step1: Write 1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_DMAC to 0x82 to enable DMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive

interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks from the zero sector, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18(Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD , send CMD18 command to read data to device, when data transfer is complete, CMD12 will be sent automatically.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD18 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.3.4.6. **Writing Pre-defined Multiple Data Blocks(CMD23+CMD25)**

To write pre-defined multiple data blocks, perform the following steps:

Step1: Write 1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_DMAC to 0x82 to enable DMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 3 data blocks, then set SMHC_CMDARG to 0x3 to ensure the block number to be operated, send CMD23 command by writing 0x80000157 to SMHC_CMD .Check whether SMHC_RINTSTS[CC] is 1.If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25(Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD, send CMD25 command to write data to device.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step8: Send CMD13 command to query whether device writing operation is complete and whether return to idle state. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD,go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle state,then the next command can be sent. If no, device is in busy state, then continue to send CMD13 to wait device idle until timeout exit.

5.3.4.7. Reading Pre-defined Multiple Data Blocks(CMD23+CMD18)

To read pre-defined multiple data blocks, perform the following steps:

Step1: Write 1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_DMAC to 0x82 to enable DMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks, then set SMHC_CMDARG to 0x3 to ensure the block number to be operated, send CMD23 command by writing 0x80000157 to SMHC_CMD .Check whether SMHC_RINTSTS[CC] is 1.If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18(Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD, send CMD18 command to read data from device to DRAM/SRAM.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD18 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.3.5. Register List

Module Name	Base Address
SMHC0	0x04020000
SMHC1	0x04021000
SMHC2	0x04022000

Register Name	Offset	Description
SMHC_CTRL	0x0000	Control Register
SMHC_CLKDIV	0x0004	Clock Control Register
SMHC_TMOUT	0x0008	Time Out Register
SMHC_CTYPE	0x000C	Bus Width Register
SMHC_BLKSIZ	0x0010	Block Size Register
SMHC_BYTCNT	0x0014	Byte Count Register
SMHC_CMD	0x0018	Command Register
SMHC_CMDARG	0x001C	Command Argument Register
SMHC_RESP0	0x0020	Response 0 Register
SMHC_RESP1	0x0024	Response 1 Register
SMHC_RESP2	0x0028	Response 2 Register
SMHC_RESP3	0x002C	Response 3 Register
SMHC_INTMASK	0x0030	Interrupt Mask Register
SMHC_MINTSTS	0x0034	Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	Raw Interrupt Status Register

SMHC_STATUS	0x003C	Status Register
SMHC_FIFOTH	0x0040	FIFO Water Level Register
SMHC_FUNS	0x0044	FIFO Function Select Register
SMHC_TCBCNT	0x0048	Transferred Byte Count between Controller and Card
SMHC_TBBCNT	0x004C	Transferred Byte Count between Host Memory and Internal FIFO
SMHC_CSDC	0x0054	CRC Status Detect Control Register
SMHC_A12A	0x0058	Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SD New Timing Set Register
SMHC_HWRST	0x0078	Hardware Reset Register
SMHC_DMAC	0x0080	DMA Control Register
SMHC_DLBA	0x0084	Descriptor List Base Address Register
SMHC_IDST	0x0088	DMAC Status Register
SMHC_IDIE	0x008C	DMAC Interrupt Enable Register
SMHC_THLD	0x0100	Card Threshold Control Register
SMHC_EDSD	0x010C	eMMC4.5 DDR Start Bit Detection Control Register
SMHC_RES_CRC	0x0110	Response CRC from Device
SMHC_D7_CRC	0x0114	CRC in Data7 from Device
SMHC_D6_CRC	0x0118	CRC in Data6 from Device
SMHC_D5_CRC	0x011C	CRC in Data5 from Device
SMHC_D4_CRC	0x0120	CRC in Data4 from Device
SMHC_D3_CRC	0x0124	CRC in Data3 from Device
SMHC_D2_CRC	0x0128	CRC in Data2 from Device
SMHC_D1_CRC	0x012C	CRC in Data1 from Device
SMHC_D0_CRC	0x0130	CRC in Data0 from Device
SMHC_CRC_STA	0x0134	CRC Status from Device in Write Operation
SMHC_DRV_DL	0x0140	Drive Delay Control Register
SMHC_SMAP_DL	0x0144	Sample Delay Control Register
SMHC_DS_DL	0x0148	Data Strobe Delay Control Register
SMHC_FIFO	0x0200	Read/ Write FIFO

5.3.6. Register Description

5.3.6.1. SMHC Global Control Register(Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 1: AHB bus 0: DMA bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line

			Time unit is used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit is used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although eMMC's HS400 speed mode is 8-bit DDR, this filed should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

5.3.6.2. **SMHC Clock Control Register(Default Value: 0x0000_0000)**

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MASK_DATA0 0: Do not mask data0 when updating clock 1: Mask data0 when updating clock
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1: Turn off card clock when FSM is in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card Clock Divider n: Source clock is divided by 2*n.(n=0~255) when HS400_MD_EN is set, this field must be cleared.

5.3.6.3. **SMHC Timeout Register(Default Value:0xFFFF_FF40)**

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit This field can set time of the Host wait for the data from the Device. Ensure to communicate with the Device,this field must be set to maximum that greater than the time  . About the N_{AC}, the explanation is as follows: When Host read data, data transmission from the Device starts after the access time delay  beginning from the end bit of the read command(ACMD51,CMD8,CMD17,CMD18). When Host read multiple block(CMD18),the next block's data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host write data, this value is no effect.
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

5.3.6.4. **SMHC Bus Width Register(Default Value:0x0000_0000)**

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card Width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

5.3.6.5. **SMHC Block Size Register(Default Value:0x0000_0200)**

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block Size

5.3.6.6. **SMHC Byte Count Register(Default Value:0x0000_0200)**

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred; should be integer multiple of Block Size for block transfers.

5.3.6.7. **SMHC Command Register(Default Value:0x0000_0000)**

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMD_LOAD Start Command This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit (CMD_OVER) will be set in interrupt register. You should not write any other command before this bit is cleared, or a command busy interrupt bit (CMD_BUSY) will be set in interrupt register.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: normal command

			1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; when this bit is set, controller will change clock domain and clock output. No command will be sent.
20:16	/	/	/
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: Send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing “I/O Abort” in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the **SMHC_RESP1** will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction

			0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: Without data transfer 1: With data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0:Short Response (48 bits) 1:Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without response 1: Command with response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

5.3.6.8. SMHC Command Argument Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CMD_ARG Command argument

5.3.6.9. SMHC Response 0 Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

5.3.6.10. SMHC Response 1 Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP1 Response 1

			Bit[63:31] of response

5.3.6.11. **SMHC Response 2 Register(Default Value: 0x0000_0000)**

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

5.3.6.12. **SMHC Response 3 Register(Default Value: 0x0000_0000)**

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

5.3.6.13. **SMHC Interrupt Mask Register(Default Value: 0x0000_0000)**

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable

8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

5.3.6.14. **SMHC Masked Interrupt Status Register(Default Value: 0x0000_0000)**

Offset: 0x0034			**Register Name: SMHC_MINTSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	M_CARD_REMOVAL_INT Card Removed
30	R/W	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R/W	0x0	M_SDIO_INT SDIO Interrupt
15	R/W	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken or received CRC status taken is negative.
14	R/W	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R/W	0x0	M_DSE_BC_INT Data Start Error When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared.
12	R/W	0x0	M_CB_IW_INT Command Busy and Illegal Write

11	R/W	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R/W	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R/W	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R/W	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R/W	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative.
6	R/W	0x0	M_RCE_INT Response CRC Error
5	R/W	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R/W	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R/W	0x0	M_DTC_INT Data Transfer Complete
2	R/W	0x0	M_CC_INT Command Complete
1	R/W	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

5.3.6.15. **SMHC Raw Interrupt Status Register(Default Value: 0x0000_0000)**

Offset: 0x0038			**Register Name: SMHC_RINTSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:17	/	/	/

16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken. This is write-1-to-clear bits.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error When set during receiving data, it means that host controller found a error start bit. It is valid at 4-bit or 8-bit bus mode. When it set, host found start bit at data0, but did not find start bit at some or all of the other data lines. When set during transmitting data, it means that busy signal is cleared. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start This is write-1-to-clear bits. When set during receiving data, it means host did not find start bit on data0.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative. This is write-1-to-clear bits.

6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete This is write-1-to-clear bits.
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs. This is write-1-to-clear bits.
0	/	/	/

5.3.6.16. **SMHC Status Register(Default Value: 0x0000_0006)**

Offset: 0x003C			**Register Name: SMHC_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy

9	R	0x0	CARD_BUSY Card Data Busy Inverted version of DATA[0] 0: card data not busy 1: card data busy
8	R	0x0	CARD_PRESENT Data[3] Status level of DATA[3], checks whether card is present 0: card not present 1: card present
7:4	R	0x0	FSM_STA Command FSM States 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO Full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level Flag 0: FIFO didn’t reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level Flag 0: FIFO didn’t reach receive trigger level 1: FIFO reached receive trigger level

5.3.6.17. SMHC FIFO Water Level Register(Default Value: 0x000F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst Size of Multiple Transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved It should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD. A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) FIFO_DEPTH = 256, FIFO_SIZE = 256 * 32 = 1K Recommended: MSize = 16, TX_TL = 240, RX_TL = 15 (for SMHC2) MSize = 8, TX_TL = 248, RX_TL = 7 (for SMHC0,SMHC1)
27:24	/	/	/
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0~0xFE: RX Trigger Level is 0~254 0xFF: Reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 15 (means greater than 15, for SMHC2) 7 (means greater than 7, for SMHC0,SMHC1)
15:8	/	/	/
7:0	R/W	0x0	TX_TL TX Trigger Level 0x1~0xFF: TX Trigger Level is 1~255 0x0: No trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual.

			Recommended: 240(means less than or equal to 240, for SMHC2) 248(means less than or equal to 248, for SMHC0,SMHC1)

5.3.6.18. **SMHC Function Select Register(Default Value: 0x0000_0000)**

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

5.3.6.19. **SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)**

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

5.3.6.20. SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

5.3.6.21. SMHC CRC Status Detect Control Register(Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA 110: HS400 speed mode 011: Other speed mode

NOTE

The register is only for SMHC2.

5.3.6.22. SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xffff	SD_A12A. SD_A12A set the argument of command 12 automatically send by controller.

5.3.6.23. SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MODE_SELEC 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing
30:28	/	/	/
27	R/W	0x0	DAT0_BYPASS(for SMHC0,SMHC1) Select data0 input asyn or bypass sample logic, it is used to check card busy or not.

			0: Enable data0 bypass 1: Disable data0 bypass
26:25	/	/	/
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR Clear the input phase of command line and data lines during updating clock operation. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Clearthe input phase of data lines before receive CRC status. 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Clear the input phase of data lines before transfer data. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Clear the input phase of data lines before receive data. 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Clear command rx phase before send command. 0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAMPLE_TIMING_PHASE(Only for SMHC2) 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore
7:6	/	/	/
5:4	R/W	0x0	CMD_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore
3:0	/	/	/

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.24. **SMHC Hardware Reset Register (Default Value: 0x0000_0001)**

Offset: 0x78			Register Name: SMHC_HWRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	HW_RST 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

NOTE

The register is only valid for SMHC2.

5.3.6.25. **SMHC DMAC Control Register (Default Value: 0x0000_0000)**

Offset: 0x0080			Register Name: SMHC_DMAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	W	0x0	DES_LOAD_CTRL When DMAC fetches a descriptor, if the valid bit of a descriptor is not set, DMAC FSM will go to the suspend state. Setting this bit will make DMAC refetch descriptor again and do the transfer normally.
30:11	/	/	/
10:8	R	0x0	Reserved
7	R/W	0x0	IDMAC_ENB IDMAC Enable When set, the IDMAC is enabled. DE is read/write.
6:2	R/W	0x0	Reserved
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

5.3.6.26. **SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)**

Offset: 0x0084			Register Name: SMHC_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DES_BASE_ADDR

			Start of Descriptor List Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

5.3.6.27. **SMHC DMAC Status Register (Default Value: 0x0000_0000)**

Offset: 0x0088			**Register Name: SMHC_IDST_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:13	R	0x0	Reserved
12:10	R	0x0	DMAC_ERR_STA Error Bits Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved EB is read-only.
9	R/W1C	0x0	ABN_INT_SUM Abnormal Interrupt Summary Logical OR of the following: IDSTS[2]: Fatal Bus Interrupt IDSTS[4]: Descriptor Unavailable bit Interrupt IDSTS[5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NOR_INT_SUM Normal Interrupt Summary Logical OR of the following: IDSTS[0]: Transmit Interrupt IDSTS[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot ACK Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout

			DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt Indicates that data transmission is finished for a descriptor. Writing a '1' clears this bit.

5.3.6.28. SMHC DMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	Reserved
7:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.

0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

5.3.6.29. **SMHC Card Threshold Control Register (Default Value: 0x0000_0000)**

Offset: 0x0100			Register Name: SMHC_THLD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	CARD_RD_THLD Card Read Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB (only for SMHC2) Card Write Threshold Enable(HS400) 0: Card write threshold disabled 1: Card write threshold enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO
1	R/W	0x0	BCIG (only for SMHC2) Busy Clear Interrupt Generation 0: Busy clear interrupt disabled 1: Busy clear interrupt enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card read threshold disabled 1: Card read threshold enabled Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO.

5.3.6.30. **SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)**

Offset: 0x010C			Register Name: SMHC_EDSD
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS400_MD_EN(for SMHC2 only) HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT

			Control for start bit detection mechanism inside mstorage based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

5.3.6.31. SMHC Response CRC Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: SMHC_ RESP_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	RESP_CRC Response CRC Response CRC from device.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.32. SMHC Data7 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: SMHC_DAT7_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT7_CRC Data[7] CRC CRC in data[7] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode,it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.33. SMHC Data6 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: SMHC_DAT6_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT6_CRC Data[6] CRC CRC in data[6] from device.

			In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode,it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.34. SMHC Data5 CRC Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: SMHC_DAT5_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT5_CRC Data[5] CRC CRC in data[5] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode,it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.35. SMHC Data4 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: SMHC_DAT4_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT4_CRC Data[4] CRC CRC in data[4] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.36. SMHC Data3 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: SMHC_DAT3_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R	0x0	DAT3_CRC Data[3] CRC CRC in data[3] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.37. **SMHC Data2 CRC Register (Default Value: 0x0000_0000)**

Offset: 0x0128			Register Name: SMHC_DAT2_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT2_CRC Data[2] CRC CRC in data[2] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.38. **SMHC Data1 CRC Register (Default Value: 0x0000_0000)**

Offset: 0x012C			Register Name: SMHC_DAT1_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT1_CRC Data[1] CRC CRC in data[1] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.39. SMHC Data0 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: SMHC_DAT0_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT0_CRC Data[0] CRC CRC in data[0] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.40. SMHC CRC Status Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: SMHC_CRC_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	CRC_STA CRC Status CRC status from device in write operation Positive CRC status token: 3’b010 Negative CRC status token: 3’b101

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

5.3.6.41. SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is 90^0 at SDR mode, 45^0 at DDR mode, 90^0 at DDR4/HS400 mode. 1: Data drive phase offset is 180^0 at SDR mode, 90^0 at DDR mode, 0^0 at DDR4/HS400 mode.
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select

			0: Command drive phase offset is 90^0 at SDR mode, 45^0 at DDR mode, 90^0 at DDR4/HS400 mode. 1: Command drive phase offset is 180^0 at SDR mode, 90^0 at DDR mode, 0^0 at DDR4/HS400 mode.
15:0	/	/	/

5.3.6.42. **SMHC Sample Delay Control Register (Default Value: 0x0000_2000)**

Offset: 0x0144			**Register Name: SMHC_SAMP_DL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

5.3.6.43. **SMHC Data Strobe Delay Control Register(Default Value: 0x0000_2000)**

Offset: 0x0148			**Register Name: SMHC_DS_DL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.

14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

NOTE

This register is for SMHC2 only.

5.3.6.44. SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

Chapter 6 EMAC

6.1. Overview

The Ethernet Medium Access Controller (EMAC) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10/100/1000 Mbit/s external PHY with RMII/RGMII interface in both full and half duplex mode. The Internal DMA is designed for packet-oriented data transfers based on a linked list of descriptors. 4 KBytes TXFIFO and 16 KBytes RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are also supported in this module.

The EMAC has the following features:

- Supports 10/100/1000 Mbit/s data transfer rates
- Supports RMII/RGMII PHY interface
- Supports MDIO
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KBytes
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KBytes of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4 KBytes TXFIFO for transmission packets and 16 KBytes RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

6.2. Block Diagram

The EMAC block diagram is shown below.

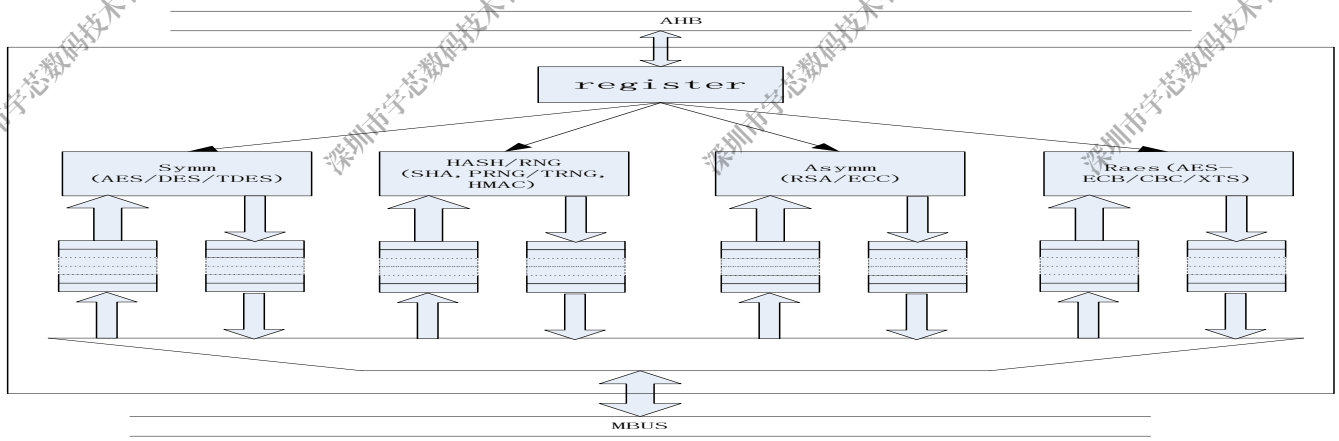


Figure 6-1. EMAC Block Diagram

6.3. Operations and Functional Descriptions

6.3.1. External Signals

Table 6-1 describes the pin mapping of EMAC.

Table 6-1. EMAC Pin Mapping

Pin Name	RGMII	RMII
RGMII_RXD3	RXD3	
RGMII_RXD2	RXD2	
RGMII_RXD1/RMII_RXD1	RXD1	RXD1
RGMII_RXD0/RMII_RXD0	RXD0	RXD0
RGMII_RXCK	RXCK	
RGMII_RXCTL/RMII_CRS_DV	RXCTL	CRS_DV
RGMII_TXD3	TXD3	
RGMII_TXD2	TXD2	
RGMII_TXD1/RMII_TXD1	TXD1	TXD1
RGMII_TXD0/RMII_TXD0	TXD0	TXD0
RGMII_TXCK/RMII_TXCK	TXCK	TXCK
RGMII_TXCTL/RMII_TXEN	TXCTL	TXEN
RGMII_CLKIN/ RMII_RXER	CLKIN	RXER
MDC	MDC	MDC
MDIO	MDIO	MDIO
EPHY_25M	EPHY_25M	EPHY_25M

Table 6-2 describes the pin list of RGMII.

Table 6-2. EMAC RGMII Pin List

Pin Name	Description	Type

RGMII_TXD[3:0]	EMAC RGMII Transmit Data	O
RGMII_TXCTL	EMAC RGMII Transmit Control	O
RGMII_TXCK	EMAC RGMII Transmit Clock	O
RGMII_RXD[3:0]	EMAC RGMII Receive Data	I
RGMII_RXCTL	EMAC RGMII Receive Control	I
RGMII_RXCK	EMAC RGMII Receive Clock	I
RGMII_CKIN	EMAC RGMII 125M Reference Clock Input	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O
EPHY_25M	25MHz Output for EMAC PHY	O

Table 6-3 describes the pin list of RMII.

Table 6-3. EMAC RMII Pin List

Pin Name	Description	Type
RMII_TXD[1:0]	EMAC RMII Transmit Data	O
RMII_TXEN	EMAC RMII Transmit Enable	O
RMII_TXCK	EMAC RMII Reference Clock	I
RMII_RXD[1:0]	EMAC RMII Receive Data	I
RMII_CRS_DV	EMAC RMII Receive Data Valid	I
RMII_RXER	EMAC RMII Receive Error	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O
EPHY_25M	25MHz Output for EMAC PHY	O

6.3.2. Clock Sources

Table 6-4 describes the clock of EMAC.

Table 6-4. EMAC Clock Characteristics

Clock Name	Description	Type
RGMII_TXCK/ RMII_TXCK	In RGMII mode, output 2.5MHz/25MHz/125MHz. In RMII mode, input 50MHz.	O/I
RGMII_RXCK	In RGMII mode, input 2.5MHz/25MHz/125MHz.	I
RGMII_CLKIN	In RGMII mode, input 125MHz Reference Clock	I

6.3.3. Typical Application

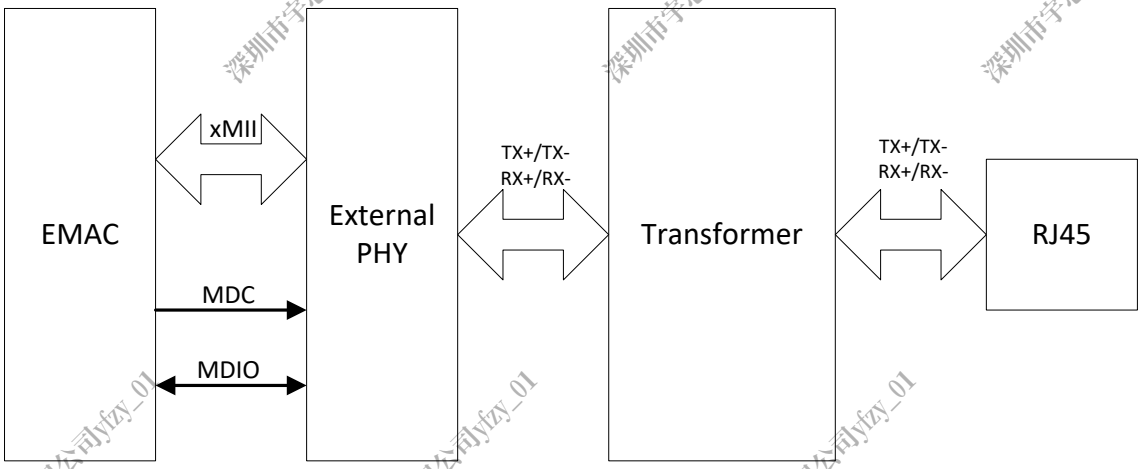


Figure 6-2. EMAC Typical Application

6.3.4. EMAC RX/TX Descriptor

The internal DMA of EMAC transfers data between host memory and internal RX/TX FIFO with a linked list of descriptors. Each descriptor is consisted of four words, and contains some necessary information to transfer TX and RX frames. The descriptor list structure is shown in Figure 6-3. The address of each descriptor must be 32-bit aligned.

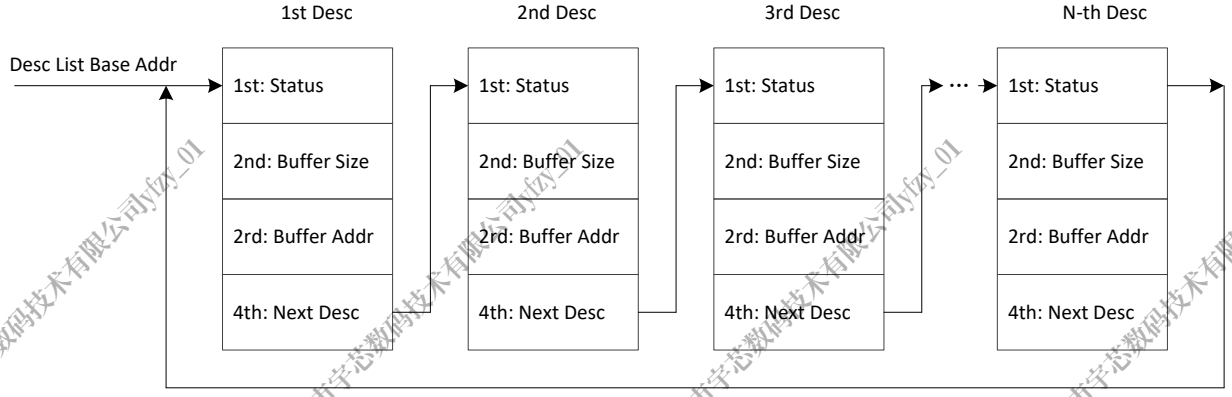


Figure 6-3. EMAC RX/TX Descriptor List

6.3.5. Transmit Descriptor

6.3.5.1. **1st Word of Transmit Descriptor**

Bits	Description
31	TX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in current descriptor's buffer are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of transmitted frame's header is wrong.

15	Reserved
14	TX_LENGHT_ERR When set, the length of transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of transmitted frame's payload is wrong.
11	Reserved
10	TX_CRS_ERR When set, carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of collision after contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR When set, the frame is aborted because of too much deferral.
1	TX_UNDERFLOW_ERR When set, the frame is aborted because of TX FIFO underflow error.
0	TX_DEFER When set in Half-Duplex mode, the EMAC defers the frame transmission.

6.3.5.2. **2nd Word of Transmit Descriptor**

Bits	**Description**
31	TX_INT_CTL When set and the current frame have been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When set, current descriptor is the last one for current frame.
29	FIR_DESC When set, current descriptor is the first one for current frame.
28:27	CHECKSUM_CTL These bits control to insert checksums in transmit frame.
26	CRC_CTL When set, CRC field is not transmitted.
25:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

6.3.5.3. **3rd Word of Transmit Descriptor**

Bits	**Description**
31:0	BUF_ADDR

	The address of buffer specified by current descriptor.

6.3.5.4. **4th Word of Transmit Descriptor**

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. It must be 32-bit aligned.

6.3.6. Receive Descriptor

6.3.6.1. **1st Word of Receive Descriptor**

Bits	Description
31	RX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when complete frame is received or current descriptor's buffer is full.
30	RX_DAF_FAIL When set, current frame donot pass DA filter.
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of receive frame.
15	Reserved
14	RX_NO_ENOUGH_BUF_ERR When set, current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When set, current fame donot pass SA filter.
12	Reserved.
11	RX_OVERFLOW_ERR When set, a buffer overflow error occurred and current frame is wrong.
10	Reserved
9	FIR_DESC When set, current descriptor is the first descriptor for current frame.
8	LAST_DESC When set, current descriptor is the last descriptor for current frame.
7	RX_HEADER_ERR When set, the checksum of frame's header is wrong.
6	RX_COL_ERR When set, there is a late collision during reception in half-duplex mode.
5	Reserved.
4	RX_LENGTH_ERR When set, the length of current frame is wrong.
3	RX_PHY_ERR When set, the receive error signal from PHY is asserted during reception.

2	Reserved.
1	RX_CRC_ERR When set, the CRC filed of received frame is wrong.
0	RX_PAYLOAD_ERR When set, the checksum or length of received frame's payload is wrong.

6.3.6.2. **2nd Word of Receive Descriptor**

Bits	Description
31	RX_INT_CTL When set and a frame have been received, the RX_INT will not be set.
30:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

6.3.6.3. **3rd Word of Receive Descriptor**

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

6.3.6.4. **4th Word of Receive Descriptor**

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. This field must be 32-bit aligned.

6.4. Register List

Module Name	Base Address
EMAC	0x05020000

Register Name	Offset	Description
EMAC_BASIC_CTL0	0x0000	EMAC Basic Control Register0
EMAC_BASIC_CTL1	0x0004	EMAC Basic Control Register1
EMAC_INT_STA	0x0008	EMAC Interrupt Status Register
EMAC_INT_EN	0x000C	EMAC Interrupt Enable Register
EMAC_TX_CTL0	0x0010	EMAC Transmit Control Register0
EMAC_TX_CTL1	0x0014	EMAC Transmit Control Register1
EMAC_TX_FLOW_CTL	0x001C	EMAC Transmit Flow Control Register
EMAC_TX_DMA_DESC_LIST	0x0020	EMAC Transmit Descriptor List Address Register

EMAC_RX_CTL0	0x0024	EMAC Receive Control Register0
EMAC_RX_CTL1	0x0028	EMAC Receive Control Register1
EMAC_RX_DMA_DESC_LIST	0x0034	EMAC Receive Descriptor List Address Register
EMAC_RX_FRM_FLT	0x0038	EMAC Receive Frame Filter Register
EMAC_RX_HASH0	0x0040	EMAC Hash Table Register0
EMAC_RX_HASH1	0x0044	EMAC Hash Table Register1
EMAC_MII_CMD	0x0048	EMAC Management Interface Command Register
EMAC_MII_DATA	0x004C	EMAC Management Interface Data Register
EMAC_ADDR_HIGH0	0x0050	EMAC MAC Address High Register0
EMAC_ADDR_LOW0	0x0054	EMAC MAC Address Low Register0
EMAC_ADDR_HIGHx	0x0050+0x08*N(N=1~7)	EMAC MAC Address High RegisterN(N:1~7)
EMAC_ADDR_LOWx	0x0054+0x08*N(N=1~7)	EMAC MAC Address Low RegisterN(N:1~7)
EMAC_TX_DMA_STA	0x00B0	EMAC Transmit DMA Status Register
EMAC_TX_CUR_DESC	0x00B4	EMAC Current Transmit Descriptor Register
EMAC_TX_CUR_BUF	0x00B8	EMAC Current Transmit Buffer Address Register
EMAC_RX_DMA_STA	0x00C0	EMAC Receive DMA Status Register
EMAC_RX_CUR_DESC	0x00C4	EMAC Current Receive Descriptor Register
EMAC_RX_CUR_BUF	0x00C8	EMAC Current Receive Buffer Address Register
EMAC_RGMII_STA	0x00D0	EMAC RGMII Status Register

6.5. Register Description

6.5.1. EMAC Basic Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: EMAC_BASIC_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	R/W	0x0	SPEED 00: 1000 Mbit/s 01: Reserved 10: 10 Mbit/s 11: 100 Mbit/s
1	R/W	0x0	LOOPBACK 0: Disable 1: Enable
0	R/W	0x0	DUPLEX 0: Half-duplex 1: Full-duplex

6.5.2. EMAC Basic Control Register1 (Default Value: 0x0800_0000)

Offset: 0x0004	Register Name: EMAC_BASIC_CTL1

Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI RX TX DMA priority 0: Same priority 1: RX priority over TX
0	R/W	0x0	SOFT_RST Soft Reset all Registers and Logic 0: No valid 1: Reset **NOTE** **All clock inputs must be valid before soft rest. This bit is cleared internally when the reset operation is completed fully. Before write any register, this bit should read a 0.**

6.5.3. EMAC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: EMAC_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W1C	0x0	RGMII_LINK_STA_P RMII Link Status Changed Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear
15:14	/	/	/
13	R/W1C	0x0	RX_EARLY_P RX DMA Filled First data Buffer of the Receive Frame Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear
12	R/W1C	0x0	RX_OVERFLOW_P RX FIFO Overflow Error Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear
11	R/W1C	0x0	RX_TIMEOUT_P RX Timeout Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear .When this bit asserts, the length of receive frame is greater

			than 2048 bytes(10240 when JUMBO_FRM_EN is set)
10	R/W1C	0x0	RX_DMA_STOPPED_P When this bit asserts, the RX DMA FSM is stopped.
9	R/W1C	0x0	RX_BUF_UA _P RX Buffer UA Interrupt Pending 0: No Pending 1: Pending Write '1' to clear .When this asserts, the RX DMA cannot acquire next RX descriptor and RX DMA FSM is suspended. The ownership of next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when writing to DMA_RX_START bit or next receive frame is coming.
8	R/W1C	0x0	RX_P Frame RX Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear. When this bit asserts, a frame reception is completed. The RX DMA FSM remains in the running state.
7:6	/	/	/
5	R/W1C	0x0	TX_EARLY_P Frame Transmitted to FIFO totally Interrupt Pending 0: No Pending 1: Pending Write '1' to clear.
4	R/W1C	0x0	TX_UNDERFLOW_P TX FIFO Underflow Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
3	R/W1C	0x0	TX_TIMEOUT_P Transmitter Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
2	R/W1C	0x0	TX_BUF_UA_P TX Buffer UA Interrupt Pending 0: No Pending 1: Pending When this bit asserts, the TX DMA can not acquire next TX descriptor and TX DMA FSM is suspended. The ownership of next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when writing to DMA_TX_START bit.
1	R/W1C	0x0	TX_DMA_STOPPED_P Transmission DMA Stopped Interrupt Pending 0: No Pending 1: Pending Write '1' to clear

0	R/W1C	0x0	TX_P Frame Transmission Interrupt Pending 0: No Pending 1: Pending Write '1' to clear

6.5.4. EMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: EMAC_INT_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN Early Receive Interrupt 0: Disable 1: Enable
12	R/W	0x0	RX_OVERFLOW_INT_EN Receive Overflow Interrupt 0: Disable 1: Enable
11	R/W	0x0	RX_TIMEOUT_INT_EN Receive Timeout Interrupt 0: Disable 1: Enable
10	R/W	0x0	RX_DMA_STOPPED_INT_EN Receive DMA FSM Stopped Interrupt 0: Disable 1: Enable
9	R/W	0x0	RX_BUF_UA_INT_EN Receive Buffer Unavailable Interrupt 0: Disable 1: Enable
8	R/W	0x0	RX_INT_EN Receive Interrupt 0: Disable 1: Enable
7:6	/	/	/
5	R/W	0x0	TX_EARLY_INT_EN Early Transmit Interrupt 0: Disable 1: Enable
4	R/W	0x0	TX_UNDERFLOW_INT_EN Transmit Underflow Interrupt 0: Disable 1: Enable
3	R/W	0x0	TX_TIMEOUT_INT_EN

			Transmit Timeout Interrupt 0: Disable 1: Enable
2	R/W	0x0	TX_BUF_UA_INT_EN Transmit Buffer Available Interrupt 0: Disable 1: Enable
1	R/W	0x0	TX_DMA_STOPPED_INT_EN Transmit DMA FSM Stopped Interrupt 0: Disable 1: Enable
0	R/W	0x0	TX_INT_EN Transmit Interrupt 0: Disable 1: Enable

6.5.5. EMAC Transmit Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: EMAC_TX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_EN Enable Transmitter 0: Disable 1: Enable When disable, transmit will continue until current transmit finish.
30	R/W	0x0	TX_FRM_LEN_CTL Frame Transmit Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off.
29:0	/	/	/

6.5.6. EMAC Transmit Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: EMAC_TX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_DMA_START Transmit DMA FSM Start 0: No valid 1: Start It is cleared internally and always read a 0
30	R/W	0x0	TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission.

			1: Start and run TX DMA.
29:11	/	/	/
10:8	R/W	0x0	TX_TH The threshold value of TX DMA FIFO. When TX_MD is 0, transmission starts when the size of frame in TX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD Transmission Mode 0: TX start after TX DMA FIFO bytes is greater than TX_TH 1: TX start after TX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_TX_FIFO Flush the data in the TX FIFO 0: Enable 1: Disable

6.5.7. EMAC Transmit Flow Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: EMAC_TX_FLOW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After completion of transmission, this bit will be cleared automatically. Before write register TX_FLOW_CTRL, this bit must be read as 0.
30:22	/	/	/
21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic retransmission of pause frame. The threshold values should be always less than the PAUSE_TIME
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN 0: Disable 1: Enable When set, enable the functionality to generate Zero-Quanta Pause control frame.

0	R/W	0x0	TX_FLOW_CTL_EN TX Flow Control Enable 0: Disable 1: Enable When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode.

6.5.8. EMAC Transmit DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: EMAC_TX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_DESC_LIST The base address of transmit descriptor list. It must be 32-bit aligned.

6.5.9. EMAC Receive Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: EMAC_RX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_EN Enable Receiver 0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL Frame Receive Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off
29	R/W	0x0	JUMBO_FRM_EN Jumbo Frame Enable 0: Disable 1: Enable Jumbo frames of 9,018 bytes without reporting a giant
28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length's field value is less than or equal to 1,500 bytes.
27	R/W	0x0	CHECK_CRC Check CRC Enable 0: Disable 1: Calculate CRC and check the IPv4 Header Checksum.
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with address specified in MAC

			Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decode the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

6.5.10. EMAC Receive Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: EMAC_RX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_DMA_START When set, the RX DMA will not work. It is cleared internally and always read a 0.
30	R/W	0x0	RX_DMA_EN Receive DMA Enable 0: Stop RX DMA after finish receiving current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL Receive FIFO Flow Control Enable 0: Disable 1: Enable,base on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT
23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT Threshold for Deactivating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT Threshold for Activating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
19:6	/	/	/
5:4	R/W	0x0	RX_TH Threshold for RX DMA FIFO Start 00: 64 01: 32 10: 96 11: 128 Only valid when RX_MD == 0, full frames with a length less than the threshold are transferred automatically.

3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When set, forward undersized frames with no error and length less than 64bytes
1	R/W	0x0	RX_MD Receive Mode 0: RX start read after RX DMA FIFO bytes is greater than RX_TH 1: RX start read after RX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_RX_FRM Flush Receive Frames 0: Enable when receive descriptors/buffers is unavailable 1: Disable

6.5.11. EMAC Receive DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: EMAC_RX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_DESC_LIST The base address of receive descriptor list. It must be 32-bit aligned.

6.5.12. EMAC Receive Frame Filter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: EMAC_RX_FRM_FLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DIS_ADDR_FILTER Disable Address Filter 0: Enable 1: Disable
30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST Disable Receive Broadcast Frames 0: Receive 1: Drop
16	R/W	0x0	RX_ALL_MULTICAST Receive All Multicast Frames Filter 0: Filter according to HASH_MULTICAST 1: Receive All
15:14	/	/	/
13:12	R/W	0x0	CTL_FRM_FILTER Receive Control Frames Filter 00: Drop all control frames 01: Drop all control frames

			10: Receive all control frames 11: Receive all control frames when pass the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST Filter Multicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
8	R/W	0x0	HASH_UNICAST Filter Unicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
7	/	/	/
6	R/W	0x0	SA_FILTER_EN Receive SA Filter Enable 0: Receive frames and update the result of SA filter 1: Update the result of SA filter. In addition, if the SA field of received frame does not match the values in SA MAC address registers, drop this frame.
5	R/W	0x0	SA_INV_FILTER Receive SA Invert Filter Set 0: Pass Frames whose SA field matches SA MAC address registers 1: Pass Frames whose SA field not matches SA MAC address registers
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it pass the address register filter or the hash filter(set by HASH_MULTICAST or HASH_UNICAST)
0	R/W	0x0	RX_ALL Receive All Frame Enable 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter(pass or fail) in the receive status word

6.5.13. EMAC Receive Hash Table Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: EMAC_RX_HASH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB0 The upper 32 bits of Hash table for receive frame filter.

6.5.14. EMAC Receive Hash Table Register1 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: EMAC_RX_HASH1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB1 The lower 32 bits of Hash table for receive frame filter.

6.5.15. EMAC MII Command Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: EMAC_MII_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC Clock Divide Ratio 000: 16 001: 32 010: 64 011: 128 Others: Reserved MDC Clock is divided from AHB clock
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR PHY Address
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR PHY Register Address
3:2	/	/	/
1	R/W	0x0	MII_WR MII Write and Read 0: Read 1: Write
0	R/W	0x0	MII_BUSY 0: Write no valid, read 0 indicate finish in read or write operation 1: Write start read or write operation, read 1 indicate busy.

6.5.16. EMAC MII Data Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: EMAC_MII_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	MII_DATA Write to or read from the register in the selected PHY.

6.5.17. EMAC MAC Address High Register0 (Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: EMAC_ADDR_HIGH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH0 The upper 16 bits of the 1st MAC address.

6.5.18. EMAC MAC Address Low Register0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: EMAC_ADDR_LOW0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	MAC_ADDR_LOW0 The lower 32 bits of 1st MAC address.

6.5.19. EMAC MAC Address High RegisterN (Default Value: 0x0000_0000)

Offset: 0x0050+0x8*N (N=1~7)			Register Name: EMAC_ADDR_HIGHN
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MAC_ADDR_CTL MAC Address Valid 0: Not valid 1: Valid
30	R/W	0x0	MAC_ADDR_TYPE MAC Address Type 0: used to compare with the destination address of the received frame 1: used to compare with the source address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC Address Byte Control Mask The lower bit of mask controls the lower byte of in MAC address. When the bit of mask is 1, do not compare the corresponding byte.
23:16	/	/	/
15:0	R/W	0x0	MAC_ADDR_HIGH The upper 16bits of the MAC address.

6.5.20. EMAC MAC Address Low Register N (Default Value: 0x0000_0000)

Offset: 0x0054+0x8*N (N=1~7)			Register Name: EMAC_ADDR_LOWN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MAC_ADDR_LOWN The lower 32bits of MAC address N (N: 1~7).

6.5.21. EMAC Transmit DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: EMAC_TX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	TX_DMA_STA The State of Transmit DMA FSM 000: STOP, When reset or disable TX DMA 001: RUN_FETCH_DESC, Fetching TX DMA descriptor 010: RUN_WAIT_STA, Waiting for the status of TX frame 011: RUN_TRANS_DATA, Passing frame from host memory to TX DMA FIFO 100: Reserved 101: Reserved 111: RUN_CLOSE_DESC, Closing TX descriptor 110: SUSPEND, TX descriptor unavailable or TX DMA FIFO underflow

6.5.22. EMAC Transmit DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: EMAC_TX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit descriptor.

6.5.23. EMAC Transmit DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: EMAC_TX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit DMA buffer.

6.5.24. EMAC Receive DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: EMAC_RX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	RX_DMA_STA The State of RX DMA FSM 000: STOP, When reset or disable RX DMA 001: RUN_FETCH_DESC, Fetching RX DMA descriptor 010: Reserved 011: RUN_WAIT_FRM, Waiting for frame. 100: SUSPEND, RX descriptor unavailable; 101: RUN_CLOSE_DESC, Closing RX descriptor. 110: Reserved 111: RUN_TRANS_DATA, Passing frame from host memory to RX DMA FIFO;

6.5.25. EMAC Receive DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: EMAC_RX_DMA_CUR_DESC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current receive descriptor

6.5.26. EMAC Receive DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: EMAC_RX_DMA_CUR_BUF
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current receive DMA buffer

6.5.27. EMAC RGMII Status Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: EMAC_RGMII_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R	0x0	RGMII_LINK The link status of RGMII interface 0: down 1: up
2:1	R	0x0	RGMII_LINK_SPD The link speed of RGMII interface 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: Reserved
0	R	0x0	RGMII_LINK_MD The link mode of RGMII interface 0: Half-Duplex 1: Full-Duplex

Chapter 7 Video Output Interfaces

7.1. HDMI (Only for V536-H)

7.1.1. Overview

The HDMI includes the following features:

- HDCP1.4/2.2
- Supports DDC and SCDC
- Integrated CEC hardware engine
- Video supported
  - 2D Video : 4K/1080P/1080I/720P/576P/576I/480P/480I, up to 4K@30fps(only for **V536-H**)
  - 2D Video : 1080P/1080I/720P/576P/576I/480P/480I, up to 1080p@60fps(only for **V526**)
  - Supports RGB/YUV444/YUV422/YUV420 output
  - Color depth: 8/10-bit
- Audio supported
  - Uncompressed audio formats: IEC60958 L-PCM, up to 8 channel 192 kHz audio sampling rate
  - Compressed audio formats: IEC61937, up to 24.576 Mbit/s audio stream bit rate

7.1.2. Block Diagram

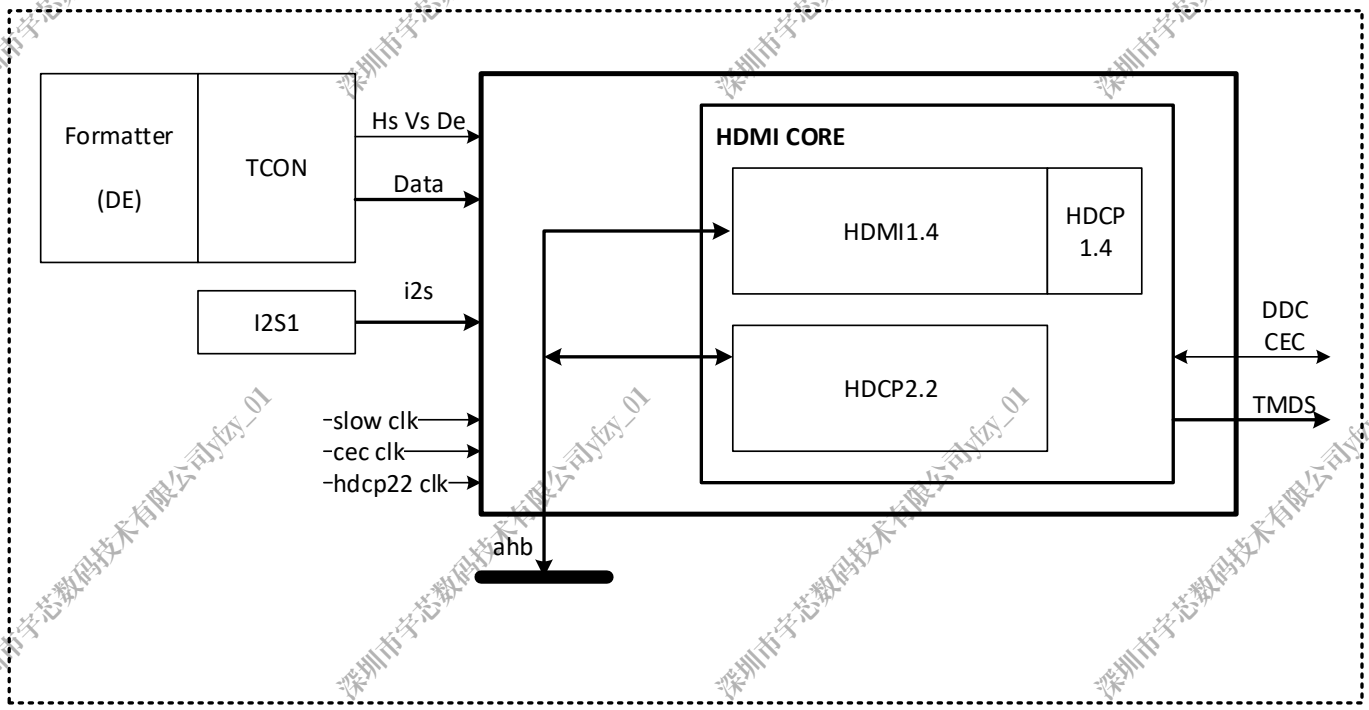


Figure 7-1. HDMI Block Diagram

7.2. TCON_LCD

7.2.1. Overview

The TCON_LCD(Timing Controller_LCD) is a module that processes video signals received from system using a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

- RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Serial RGB/dummy RGB interface, up to 800 x 480@60fps
- i8080 interface, up to 800 x 480@60fps
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence

7.2.2. Block Diagram

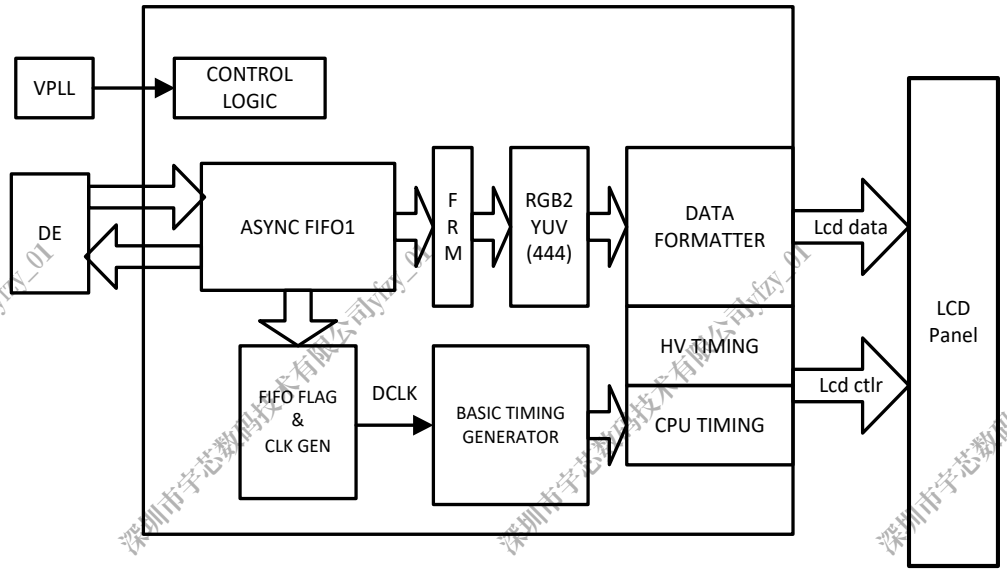


Figure 7-2. TCON_LCD Block Diagram

7.2.3. Operations and Functional Descriptions

7.2.3.1. External Signals

The LCD external signals are used to connect to panel interface.The panel interface has various types.

7.2.3.1.1. Control Signal and Data Port Mapping

	SYNC RGB					CPU cmd	CPU 18bit	CPU 16bit								CPU 8bit					CPU 9bit	
I/O	Para RGB	Serial RGB			CCIR 656		256K	256K							65K	256K			65K		256K	
		1st	2nd	3rd				1st	2nd	3rd	1st	2nd	1st	2nd		1st	2nd	3rd	1st	2nd	1st	2nd
IO0	VSYNC					CS																
IO1	HSYNC					RD																
IO2	DCLK					WR																
IO3	DE					RS																
D23	R7					D23	R5	R5	B5	G5	R5		R5	B5	R4							
D22	R6					D22	R4	R4	B4	G4	R4		R4	B4	R3							
D21	R5					D21	R3	R3	B3	G3	R3		R3	B3	R2							
D20	R4					D20	R2	R2	B2	G2	R2		R2	B2	R1							
D19	R3					D19	R1	R1	B1	G1	R1		R1	B1	R0							
D18	R2					D18	R0	R0	B0	G0	R0		R0	B0	G5							
D17	R1					D17																
D16	R0					D16																
D15	G7					D15	G5								G4							
D14	G6					D14	G4								G3							
D13	G5					D13	G3															
D12	G4	D17	D27	D37	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5	R4	G2	R5	G2
D11	G3	D16	D26	D36	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4	R3	G1	R4	G1
D10	G2	D15	D25	D35	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3	R2	G0	R3	G0
D9	G1					D9																
D8	G0					D8																
D7	B7	D14	D24	D34	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2	R1	B4	R2	B5
D6	B6	D13	D23	D33	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1	R0	B3	R1	B4
D5	B5	D12	D22	D32	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0	G5	B2	R0	B3
D4	B4	D11	D21	D31	D1	D4	B2								B1				G4	B1	G5	B2
D3	B3	D10	D20	D30	D0	D3	B1								B0				G3	B0	G4	B1
D2	B2					D2	B0														G3	B0
D1	B1					D1																
D0	B0					D0																

NOTE

In the above table, D1_N indicates the Nth bit of the first cycle, and D2_N, D3_N have the similar meanings(Where, N = 0, 1, 2, 3, 4, 5, 6, 7).

7.2.3.1.2. HV Interface (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 application.

Table 7-1. HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicate one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
LDE	LCD data enable	O
LD[23..0]	24Bit RGB output from input FIFO for panel	O

The timing diagram of HV interface is as follows.

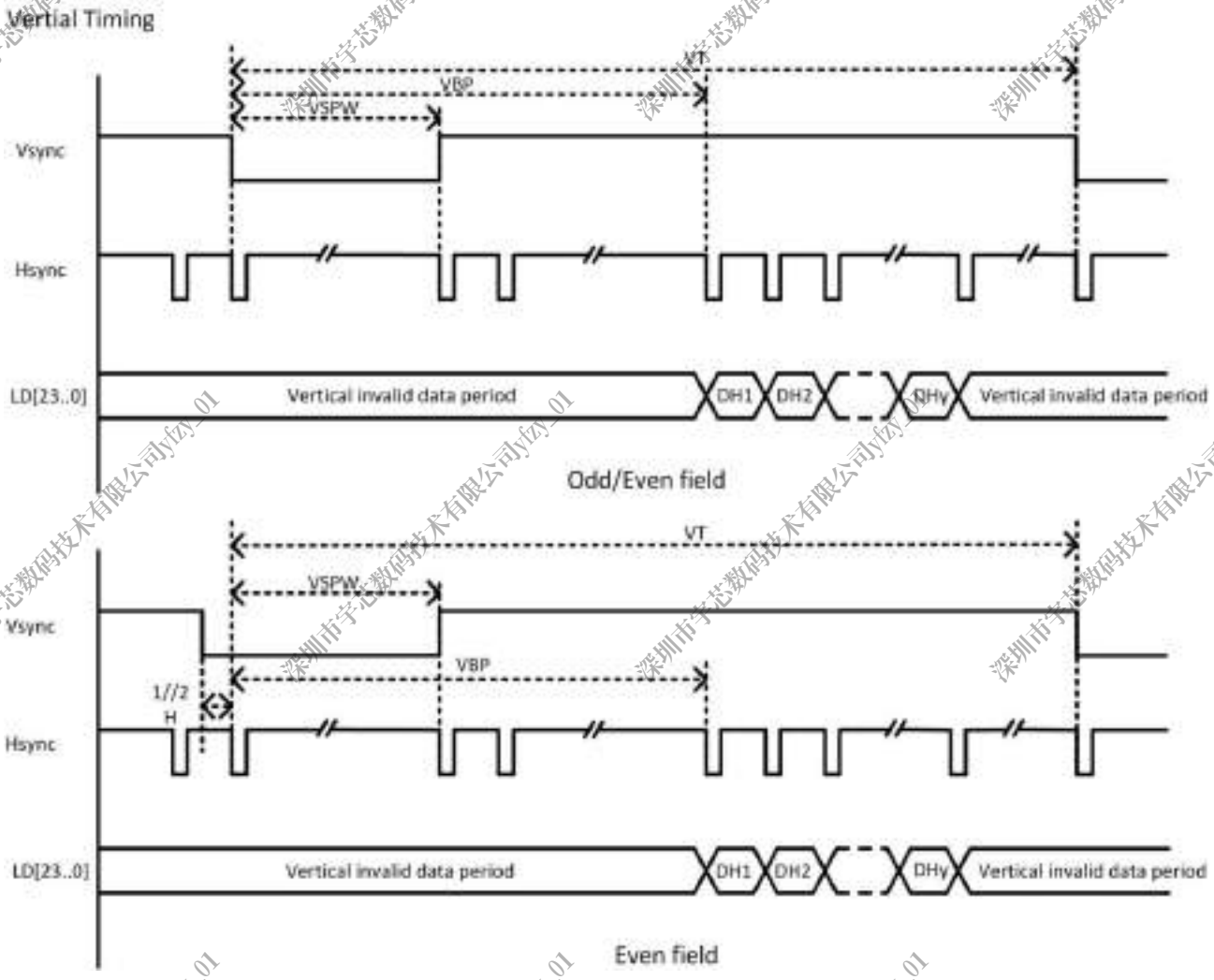


Figure 7-3. HV Interface Vertical Timing

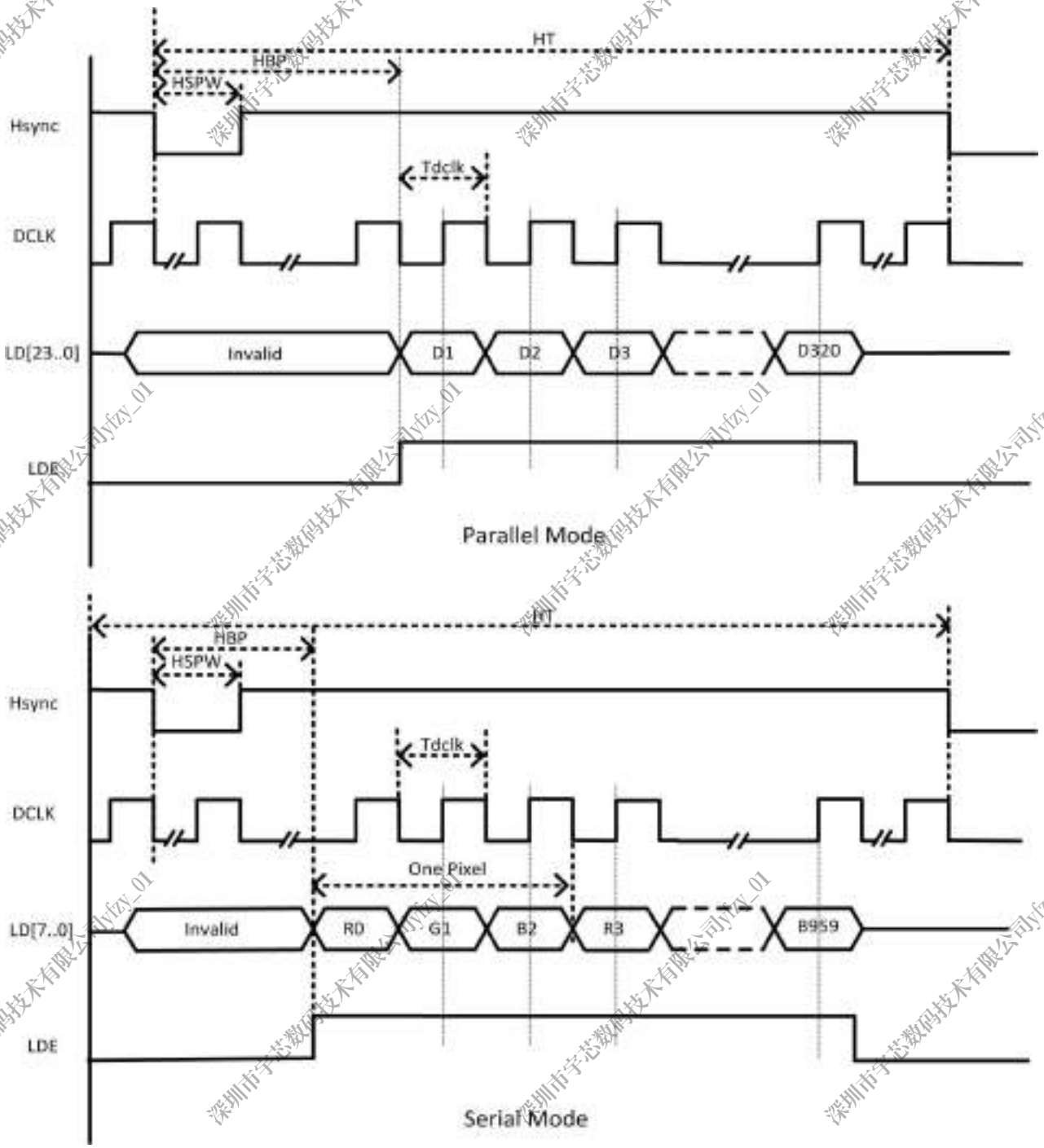


Figure 7-4. HV Interface Horizontal Timing

7.2.3.1.3. BT656 Interface

In HV serial YUV output mode, its timing is BT656 compatible. SAV adds right before active area every line; EAV adds right after active area every line.

Table 7-2. BT656 Panel Signals

Signal	Description	Type
DCLK	Clock Signal	O
DATA[7:0]	Data Signal	O

Its logic is:

F = “0” for Field 1 F = “1” for Field 2

V = “1” during vertical blanking

H = “0” at SAV H = “1” at EAV

P3-P0 = protection bits

P3 = V ⊕ H

P2 = F ⊕ H

P1 = F ⊕ V

P0 = F ⊕ V ⊕ H

Where ⊕ represents the exclusive-OR function

The 4 byte SAV/EAV sequence is as follows.

Table 7-3. EAV and SAV Sequence

	8-bit Data								10-bit Data	
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

7.2.3.1.4. i8080 Interface

i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels.CPU control signals are active low.

Table 7-4. CPU Panel Signals

Signal	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure relationship between basic timing and CPU timing. WR is 180° delay of DCLK; CS is active when pixel data are valid; RD is always set to 1; A1 are set by “LCD_CPUI/F”.

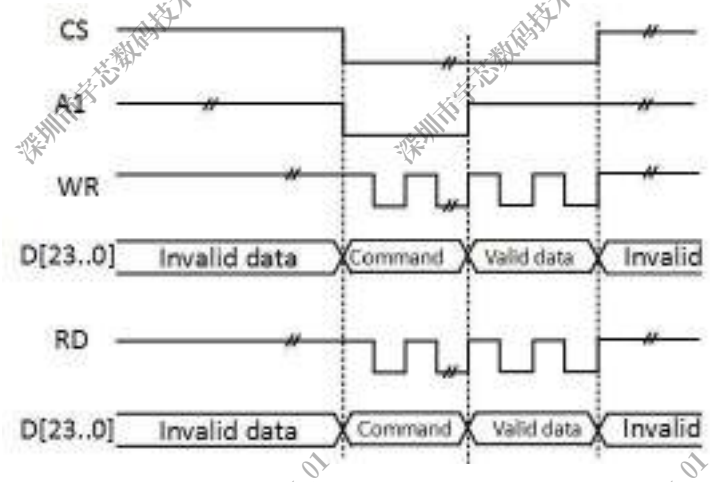


Figure 7-5. i8080 Interface Timing

When CPU I/F is in IDLE state, it can generate WR/RD timing by setting "**Lcd_CPUI/F**". CS strobe is one DCLK width, WR/RD strobe is half DCLK width.

7.2.3.2. Clock Sources

The following table describes the clock sources of TCON_LCD.Table 7-6 describes the clock sources of TCON_LCD.

Table 7-5. TCON_LCD Clock Sources

Clock Sources	Description
PLL_VIDEO0(1X)	Video PLL Clock,default value is 297MHz
PLL_VIDEO0(4X)	Video PLL Clock,default value is 1188MHz

7.2.3.3. RGB Gamma Correction

Function: This module correct the RGB input data of DE.
A 256*8*3 Byte register file is used to store the gamma table. The following is the layout.

Table 7-6. RGB Gamma Correction Table

Offset	Value
0x400, 0x401, 0x402	{ B0[7:0], G0[7:0], R0[7:0] }
0x404	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....
0x7FC	{ B255[7:0], G255[7:0], R255[7:0] }

7.2.3.4. CEU Module

This module enhances color data from DE .

R' = ((Rr*R + Rg*G + Rb*B +16)/16+ Rc+16)/16
G' = ((Gr*R + Gg*G + Gb*B +16)/16+Gc+16)/16

B’ = ((Br*R + Bg*G + Bb*B +16)/16+ Bc+16)/16

NOTE

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb s13 (-16,16)
Rc, Gc, Bc s19 (-16384, 16384)
R, G, B u8 [0-255]
R’ have the range of [Rmin ,Rmax]
G’ have the range of [Rmin ,Rmax]
B’ have the range of [Rmin ,Rmax]

7.2.3.5. CMAP Module

Function: This module map color data from DE.
Every 4 input pixels as an unit. An unit is divided into 12 bytes. Output byte can select one of those 12 bytes.Note that even line and odd line can be different, and output can be 12 bytes(4 pixels) or reduce to 6 bytes(2 pixels).

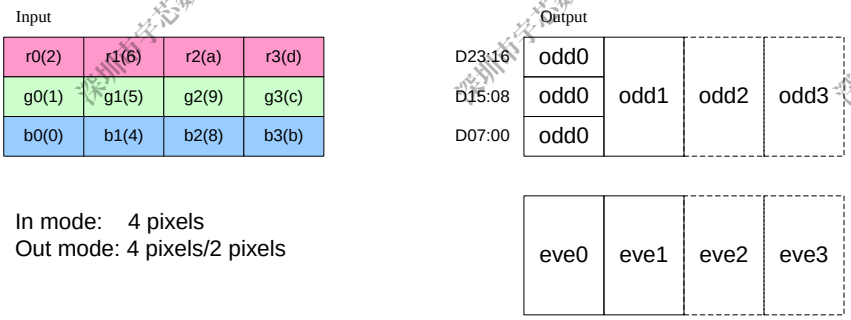


Figure 7-6. CMAP Module

7.2.4. Programming Guidelines

7.2.4.1. HV Mode Configuration Process

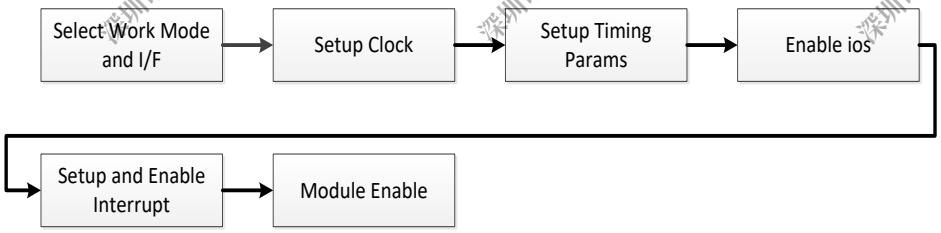


Figure 7-7. HV Mode Initial Process

Step1: Select HV interface type: parallel RGB or serial RGB.
Step2: Set clock, if phase changing function need be used, then the bit[31:28] of LCD_DCLK_REG should be set to 0xf.
Step3: Set timing parameter x, ht,hbp,hspw,y,vt,vbp,vspw. Note that hbp includes hspw,vbp includes vspw, and vt need be set to twice as actual value.
Step4: Open io output.
Step5: Set and open interrupt function.Note that when using line interrupt, the LCD_LINE_INT_NUM of LCD_GINT1_REG need be set first,then LCD_LINE_INT_EN of LCD_GINT0_REG is set to 1.
Step6: Open module enable.

7.2.4.2. i8080 Configuration Process

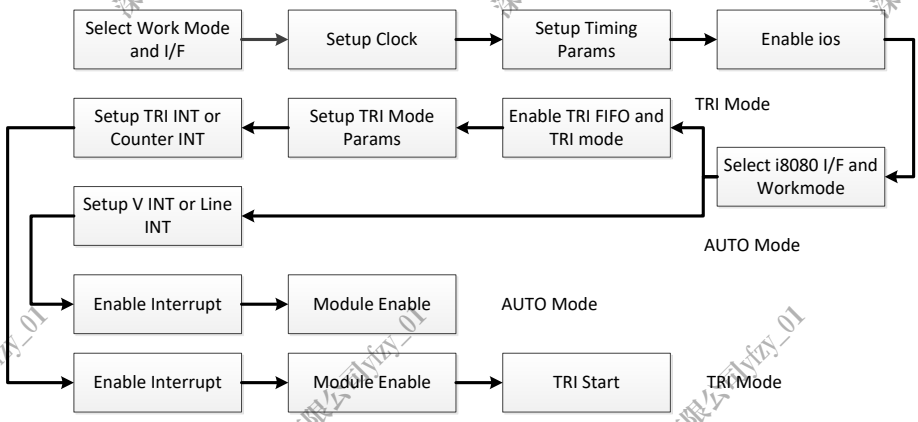


Figure 7-8. i8080 Mode Initial Process

Step1: Select i8080 interface type.

Step2: The step is the same as HV mode,but pulse adjustment function is invalid.

Step3: The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode , or a handful of functions such as CMAP will not be able to apply.

Step4: The step is the same as HV mode.

Step5: Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

----------TRI mode----------

Step6: Open TRI FIFO switch, and TRI mode function.

Step7: Set parameters of TRI mode, including block size,block space and block number.

NOTE

When output interface is parallel mode,then the setting value of block space parameter is not less than 20.
When output interface is 2 cycle serial mode,then the setting value of block space parameter is not less than 40.
When output interface is 3 cycle serial mode,then the setting value of block space parameter is not less than 60.
When output interface is 4 cycle serial mode,then the setting value of block space parameter is not less than 80.

Step8: Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24bit for offset 8c register is set to "1", to open up input of pad.

Step9: Open interrupt total switch.

Step10: Open interrupt total enable.

Step11: Operate tri start operation(the bit1 of LCD_CPU_IF_REG is set to"1")

----------Auto mode----------

Step6: Set and open V interrupt or Line interrupt, the step is the same as HV mode.

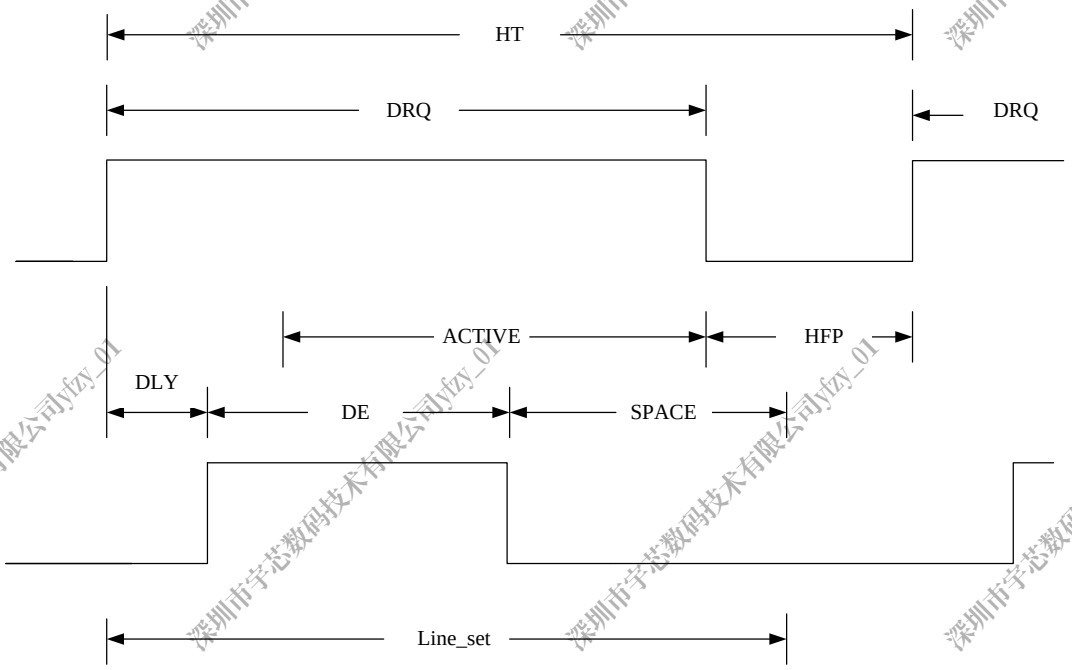
Step7 : Open module total enable.

7.2.4.3. Notes of MIPI DSI Mode

Notes of using MIPI DSI mode :

(1) Using DSI display, data clk of TCON_LCD should start first.

(2) When using TCON_LCD in conjunction with DSI video mode,the block space parameter should satisfy the following relationship:



DRQ < Line_set < HT

Figure 7-9. DSI Video Mode Data Request Timing

7.2.5. Register List

Module Name	Base Address
TCON_LCD0	0x06511000

Register Name	Offset	Description
LCD_GCTL_REG	0x0000	LCD Global Control Register
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x0014+N*0x04	LCD FRM Seed Register(N=0,1,2,3,4,5)
LCD_FRM_TAB_REG	0x002C+N*0x04	LCD FRM Table Register(N=0,1,2,3)
LCD_3D_FIFO_REG	0x003C	LCD 3D FIFO Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD CPU Panel Interface Register

LCD_CPU_WR_REG	0x0064	LCD CPU Panel Write Data Register
LCD_CPU_RD0_REG	0x0068	LCD CPU Panel Read Data Register0
LCD_CPU_RD1_REG	0x006C	LCD CPU Panel Read Data Register1
LCD_IO_POL_REG	0x0088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x008C	LCD IO Control Register
LCD_DEBUG_REG	0x00FC	LCD Debug Register
LCD_CEU_CTL_REG	0x0100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG	0x0110+N*0x04	LCD CEU Coefficient Register0(N=0,1,2,4,5,6,8,9,10)
LCD_CEU_COEF_ADD_REG	0x011C+N*0x10	LCD CEU Coefficient Register1(N=0,1,2)
LCD_CEU_COEF_RANG_REG	0x0140+N*0x04	LCD CEU Coefficient Register2(N=0,1,2)
LCD_CPU_TRI0_REG	0x0160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x0164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x0168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x016C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x0170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x0174	LCD CPU Panel Trigger Register5
LCD_CMAP_CTL_REG	0x0180	LCD Color Map Control Register
LCD_CMAP_ODD0_REG	0x0190	LCD Color Map Odd Line Register0
LCD_CMAP_ODD1_REG	0x0194	LCD Color Map Odd Line Register1
LCD_CMAP_EVEN0_REG	0x0198	LCD Color Map Even Line Register0
LCD_CMAP_EVEN1_REG	0x019C	LCD Color Map Even Line Register1
LCD_SAFE_PERIOD_REG	0x01F0	LCD Safe Period Register
LCD_FSYNC_GEN_CTRL_REG	0x23C	Module Enable and Output Value Register
LCD_FSYNC_GEN_DLY_REG	0x240	Fsync Active Time Register
LCD_GAMMA_TABLE_REG	0x400-0x7FF	LCD Gamma Table Registers

7.2.6. Register Description

7.2.6.1. LCD Global Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LCD_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: Disable 1: Enable When it is disabled, the module will be reset to idle state.
30	R/W	0x0	LCD_GAMMA_EN 0: Disable 1: Enable Enable the Gamma correction function.
29:0	/	/	/

7.2.6.2. **LCD Global Interrupt Register0(Default Value: 0x0000_0000)**

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_VB_INT_EN 0: Disable 1: Enable Enable the Vb interrupt.
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN 0: Disable 1: Enable Enable the line interrupt.
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN 0: Disable 1: Enable Enable the trigger finish interrupt.
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN 0: Disable 1: Enable Enable the trigger counter interrupt.
25	R/W	0x0	FSYNC_INT_EN 0: Disable 1: Enable Enable the fsync interrupt.
24	R/W	0x0	DE_INT_EN 0: Disable 1: Enable Enable the data enable interrupt.
23:16	/	/	/
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
14	/	/	/
13	R/W0C	0x0	LCD_LINE_INT_FLAG Trigger when SY0 matched the current LCD scan line. Write 0 to clear it.
12	/	/	/
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when cpu trigger mode finished. Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reached this value. Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG

			Only used in DSI video mode, tri when sync by DSI but not finish Write 0 to clear it.
8:3	/	/	/
2	R/W	0x0	FSYNC_INT_INV Enable the fsync interrupt set signal inverse polarity. When FSYNC is positive, this bit must be 1. And vice versa.
1	R/W0C	0x0	DE_INT_FLAG Asserted at the first valid line in every frame. Write 0 to clear it.
0	R/W0C	0x0	FSYNC_INT_FLAG Asserted at the fsync signal in every frame. Write 0 to clear it.

7.2.6.3. **LCD Global Interrupt Register1(Default Value: 0x0000_0000)**

Offset: 0x0008			**Register Name: LCD_GINT1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger(including inactive lines) Setting it for the specified line for trigger0. SY0 is writable only when LINE_TRG0 is disabled.
15:0	/	/	/

7.2.6.4. **LCD FRM Control Register(Default Value: 0x0000_0000)**

Offset: 0x0010			**Register Name: LCD_FRM_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_FRM_EN 0:Disable 1:Enable Enable the dither function.
30:7	/	/	/
6	R/W	0x0	LCD_FRM_MODE_R 0: 6-bit frm output 1: 5-bit frm output The R component output bits are in dither function.
5	R/W	0x0	LCD_FRM_MODE_G 0: 6-bit frm output 1: 5-bit frm output The G component output bits are in dither function.
4	R/W	0x0	LCD_FRM_MODE_B 0: 6-bit frm output

			1: 5-bit frm output The B component output bits are in dither function.
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST 00: FRM 01: half 5-/6-bit, half FRM 10: half 8-bit, half FRM 11: half 8-bit, half 5-/6-bit Set the test mode of dither function.

7.2.6.5. **LCD FRM Seed Register(Default Value: 0x0000_0000)**

Offset: 0x0014+N*0x04 (N=0,1,2,3,4,5)			**Register Name: LCD_FRM_SEED_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Avoid setting it to 0 Set the seed used in dither function.

7.2.6.6. **LCD FRM Table Register(Default Value: 0x0000_0000)**

Offset: 0x002C+N*0x04(N=0,1,2,3)			**Register Name: LCD_FRM_TAB_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRM_TABLE_VALUE Set the data used in dither function. Usually set as follow: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7f7f7777

7.2.6.7. **LCD 3D FIFO Register(Default Value: 0x0000_0000)**

Offset: 0x003C			**Register Name: LCD_3D_FIFO_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	3D_FIFO_BIST_EN

			0: Disable 1: Enable
30:14	/	/	/
13:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line=3D_FIFO_HALF_LINE_SIZE+1 Only valid when 3D_FIFO_SETTING is set as 2.
3:2	/	/	/
1:0	R/W	0x0	3D_FIFO_SETTING 00: by pass 01: used as normal FIFO 10: used as 3D interlace FIFO 11: reserved

7.2.6.8. **LCD Control Register(Default Value: 0x0000_0000)**

Offset: 0x0040			**Register Name: LCD_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: Disable 1: Enable It executes at the beginning of the first blank line of LCD timing.
30:26	/	/	/
25:24	R/W	0x0	LCD_IF 00: HV(Sync+DE) 01: 8080 I/F 1x:reservd Set the interface type of LCD controller.
23	R/W	0x0	LCD_RB_SWAP 0: Default 1: Swap RED and BLUE data at FIFO1
22	/	/	/
21	R/W	0x0	LCD_FIFO1_RST Writing 1 and then 0 to this bit will reset FIFO 1 1 holding time must more than 1 DCLK
20	R/W	0x0	LCD_INTERLACE_EN 0:Disable 1:Enable This flag is valid only when LCD_EN == 1
19:9	/	/	/
8:4	R/W	0x0	LCD_START_DELAY The unit of delay is T_{line}. Valid only when LCD_EN == 1
3	/	/	/
2:0	R/W	0x0	LCD_SRC_SEL 000: DE

			001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reserved 111: Gridding Check

7.2.6.9. **LCD Data Clock Register(Default Value: 0x0000_0000)**

Offset: 0x0044			**Register Name: LCD_DCLK REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LCD_DCLK_EN 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0001: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; Others:Reversed LCD clock enable.
27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV Tdclk = Tsclk * DCLKDIV **NOTE** **If dclk1&dclk2 used, DCLKDIV >=6. If dclk only, DCLKDIV >=1**

7.2.6.10. **LCD Basic Timing Register0(Default Value: 0x0000_0000)**

Offset: 0x0048			**Register Name: LCD_BASIC0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	Y Panel height is Y+1

7.2.6.11. **LCD Basic Timing Register1(Default Value: 0x0000_0000)**

Offset: 0x004C			**Register Name: LCD_BASIC1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation: 1) parallel:HT = X + BLANK Limitation: 1) parallel:HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

7.2.6.12. **LCD Basic Timing Register2(Default Value: 0x0000_0000)**

Offset: 0x0050			**Register Name: LCD_BASIC2_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

7.2.6.13. **LCD Basic Timing Register3(Default Value: 0x0000_0000)**

Offset: 0x0054			**Register Name: LCD_BASIC3_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync VT/2 > (VSPW+1)

7.2.6.14. **LCD HV Panel Interface Register(Default Value: 0x0000_0000)**

Offset: 0x0058			**Register Name: LCD_HV_IF_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:28	R/W	0x0	HV_MODE 0000: 24-bit/1cycle parallel mode 1000: 8-bit/3cycle RGB serial mode(RGB888) 1010: 8-bit/4cycle Dummy RGB(DRGB) 1011: 8-bit/4cycle RGB Dummy(RGBD) 1100: 8-bit/2cycle YUV serial mode(CCIR656) Set the HV mode of LCD controller.
27:26	R/W	0x0	RGB888_ODD_ORDER 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B Serial RGB888 mode output sequence at odd lines of the panel (line 1, 3, 5, 7…)
25:24	R/W	0x0	RGB888_EVEN_ORDER 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B Serial RGB888 mode output sequence at even lines of the panel (line 2, 4, 6, 8…)
23:22	R/W	0x0	YUV_SM 00: YUYV 01: YVYU 10: UYVY 11: VYUY Serial YUV mode output sequence 2-pixel-pair of every scan line
21:20	R/W	0x0	YUV EAV/SAV F LINE DELAY 00:F toggle right after active video line 01:delay 2 line(CCIR PAL) 10:delay 3 line(CCIR NTSC) 11:reserved Set the delay line mode.
19	R/W	0x0	CCIR_CSC_DIS 0: Enable 1: Disable Only valid when HV mode is “1100”. Select ‘0’ LCD convert source from RGB to YUV
18:0	/	/	/

7.2.6.15. **LCD CPU Panel Interface Register(Default Value: 0x0000_0000)**

Offset: 0x0060			**Register Name: LCD_CPU_IF_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	CPU_MODE

			0000: 18bit/256K mode 0010: 16bit mode0 0100: 16bit mode1 0110: 16bit mode2 1000: 16bit mode3 1010: 9bit mode 1100: 8bit 256K mode 1110: 8bit 65K mode xxx1: 24bit for DSI Set the i8080 interface work mode.
27	/	/	/
26	R/W	0x0	DA Pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA Pin A1 value in 8080 mode WR/RD execute
24	/	/	/
23	R	0x0	WR_FLAG 0:write operation is finishing 1:write operation is pending The status of write operation.
22	R	0x0	RD_FLAG 0:read operation is finishing 1:read operation is pending The status of read operation.
21:18	/	/	/
17	R/W	0x0	AUTO Auto Transfer Mode If it is 1, all the valid data during this frame are write to panel. This bit is sampled by Vsync
16	R/W	0x0	FLUSH Direct Transfer Mode If it is enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate is controlled by DCLK.
15:4	/	/	/
3	R/W	0x0	TRIGGER_FIFO_BIST_EN 0: Disable 1: Enable Entry addr is 0xFF8
2	R/W	0x0	TRIGGER_FIFO_EN 0:Disable 1:Enable Enable the trigger FIFO.
1	R/W1S	0x0	TRIGGER_START write ‘1’ to start a frame flush, writing ’0’ has no effect. This flag indicated frame flush is running.

			Sofeware must make sure write '1' only when this flag is '0'.
0	R/W	0x0	TRIGGER_EN 0: Trigger mode disable 1: Trigger mode enable Enable trigger mode.

7.2.6.16. **LCD CPU Panel Write Data Register(Default Value: 0x0000_0000)**

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	W	0x0	DATA_WR Data write on 8080 bus, launch a write operation on 8080 bus

7.2.6.17. **LCD CPU Panel Read Data Register0(Default Value: 0x0000_0000)**

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus

7.2.6.18. **LCD CPU Panel Read Data Register1(Default Value: 0x0000_0000)**

Offset: 0x006C			Register Name: LCD_CPU_RD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus

7.2.6.19. **LCD IO Polarity Register(Default Value: 0x0000_0000)**

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	IO_OUTPUT_SEL 0: Normal output 1: Register output When set as '1', d[23:0], io0, io1,io3 sync to dclk.
30:28	R/W	0x0	DCLK_SEL 000: Used DCLK0(normal phase offset) 001: Used DCLK1(1/3 phase offset) 010: Used DCLK2(2/3 phase offset)

			101: DCLK0/2 phase 0 100: DCLK0/2 phase 90 Others: Reserved Set the phase offset of clock and data in hv mode.
27	R/W	0x0	IO3_INV 0: Not invert 1: Invert Enable invert function of IO3.
26	R/W	0x0	IO2_ INV 0: Not invert 1: Invert Enable invert function of IO2.
25	R/W	0x0	IO1_INV 0: Not invert 1: Invert Enable invert function of IO1.
24	R/W	0x0	IO0_INV 0: Not invert 1: Invert Enable invert function of IO0.
23:0	R/W	0x0	Data_INV 0: Normal polarity 1: Invert the specify output LCD output port D[23:0] polarity control, with independent bit control.

7.2.6.20. **LCD IO Control Register(Default Value: 0x0FFF_FFFF)**

Offset: 0x008C			**Register Name: LCD_IO_TRI_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN 0: Normal 1: Bits_invert Set the endian of data bits.
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO3.
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO2.
25	R/W	0x1	IO1_OUTPUR_TRI_EN 1: Disable 0: Enable

			Enable the output of IO1.
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO0.
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN 1: Disable 0: Enable LCD output port D[23:0] output enable, with independent bit control.

7.2.6.21. **LCD Debug Register(Default Value: 0x2000_0000)**

Offset: 0x00FC			**Register Name: LCD_DEBUG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	LCD_FIFO_UNDERFLOW 0: Not underflow 1: Underflow The flag shows whether the fifos in underflow status.
30	/	/	/
29	R	0x1	LCD_FIELD_POL 0: Second field 1: First field The flag indicates the current field polarity.
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line.
15:0	/	/	/

7.2.6.22. **LCD CEU Control Register(Default Value: 0x0000_0000)**

Offset: 0x0100			**Register Name: LCD_CEU_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN 0: Bypass 1: Enable Enable CEU function.
30:0	/	/	/

7.2.6.23. **LCD CEU Coefficient Register0(Default Value: 0x0000_0000)**

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			**Register Name: LCD_CEU_COEF_MUL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb Signed 13bit value, range of (-16,16)

7.2.6.24. **LCD CEU Coefficient Register1(Default Value: 0x0000_0000)**

Offset: 0x011C+N*0x10(N=0,1,2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE N=0: Rc N=1: Gc N=2: Bc Signed 19bit value, range of (-16384, 16384)

7.2.6.25. **LCD CEU Coefficient Register2(Default Value: 0x0000_0000)**

Offset: 0x0140+N*0x04(N=0,1,2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8bit value, range of [0,255]

7.2.6.26. **LCD CPU Panel Trigger Register0(Default Value: 0x0000_0000)**

Offset: 0x0160			Register Name: LCD_CPU_TRI0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE The spaces between data blocks. It should be set >20*pixel.

15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE The size of data block.It is usually set as X.

7.2.6.27. **LCD CPU Panel Trigger Register1(Default Value: 0x0000_0000)**

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks.It is usually set as Y.

7.2.6.28. **LCD CPU Panel Trigger Register2(Default Value: 0x0000_0000)**

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x20	START_DELAY Tdly = (Start_Delay +1) * be_clk*8
15	R/W	0x0	TRANS_START_MODE 0: ecc_fifo+tri_fifo 1: tri_fifo Select the FIFOs used in CPU mode.
14:13	R/W	0x0	SYNC_MODE 0x: auto 10: 0 11: 1 Set the sync mode in CPU interface.
12:0	R/W	0x0	TRANS_START_SET Usual set as the length of a line.

7.2.6.29. **LCD CPU Panel Trigger Register3(Default Value: 0x0000_0000)**

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE 00: Disable 01: Counter mode 10: Te rising mode 11: Te falling mode When set as 01, Tri_Counter_Int occur in cycle of (Count_N+1)×(Count_M+1)×4 dclk.

			When set as 10 or 11, io0 is map as TE input.
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N The value of counter factor.
7:0	R/W	0x0	COUNTER_M The value of counter factor.

7.2.6.30. **LCD CPU Panel Trigger Register4(Default Value: 0x0000_0000)**

Offset: 0x0170			**Register Name: LCD_CPU_TRI4_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	PLUG_MODE_EN 0: Disable 1: Enable Enable the plug mode used in dsi command mode.
27:25	/	/	/
24	R/W	0x0	A1 Valid in first Block.
23:0	R/W	0x0	D23-D0 Valid in first Block.

7.2.6.31. **LCD CPU Panel Trigger Register5(Default Value: 0x0000_0000)**

Offset: 0x0174			**Register Name: LCD_CPU_TRI5_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	A1 Valid in Block except first
23:0	R/W	0x0	D23-D0 Valid in Block except first

7.2.6.32. **LCD Color Map Control Register(Default Value: 0x0000_0000)**

Offset: 0x0180			**Register Name: LCD_CMAP_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	COLOR_MAP_EN 0: Bypass 1: Enable Enable the color map function. This module only work when X is divided by 4.
30:1	/	/	/
0	R/W	0x0	OUT_FORMAT

			0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1 Set the pixel output format in color map function.

7.2.6.33. **LCD Color Map Odd Line Register0(Default Value: 0x0000_0000)**

Offset: 0x0190			**Register Name: LCD_CMAP_ODD0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD1 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_ODD0 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2

			1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.2.6.34. **LCD Color Map Odd Line Register1(Default Value: 0x0000_0000)**

Offset: 0x0194			**Register Name: LCD_CMAP_ODD1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD3 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_ODD2 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1

			0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.2.6.35. **LCD Color Map Even Line Register0(Default Value: 0x0000_0000)**

Offset: 0x0198			**Register Name: LCD_CMAP_EVEN0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN1 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_EVEN0 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0

			0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.2.6.36. **LCD Color Map Even Line Register1(Default Value: 0x0000_0000)**

Offset: 0x019C			**Register Name: LCD_CMAP_ EVEN1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN3 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_EVEN2 bit15-12: Reserved bit11-08: Out_Odd0[23:16]

			bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.2.6.37. **LCD Safe Period Register(Default Value: 0x0000_0000)**

Offset: 0x01F0			**Register Name: LCD_SAFE_PERIOD_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time,LCD controller allow dram controller to change frequency.The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM 011: safe at 2 and safe at sync active 100: safe at line Select the safe mode.

7.2.6.38. **LCD_FSYNC_GEN_CTRL_REG(Default Value: 0x0000_0000)**

Offset: 0x23C	**Register Name: FSYNC_GEN_CTRL_REG**

Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:8	R/W	0x0	sensor_dis_time Delay 0~2047 Hsync Period
7	/	/	/
6	R/W	0x0	sensor_act1_value 0: Fsync active_1 period output 0 1: Fsync active_1 period output 1
5	R/W	0x0	sensor_act0_value 0: Fsync active_0 period output 0 1: Fsync active_0 period output 1
4	R/W	0x0	sensor_dis_value 0: Fsync disable period output 0 1: Fsync disable period output 1
3	/	/	/
2	R/W	0x0	hsync_pol_sel 0: normal 1: opposite hsync to hysnc counter
1	R/W	0x0	sel_vsync_en 0: select vsync falling edge to start state machine 1: select vsync rising edge to start state machine
0	R/W	0x0	fsync_gen_en 0: disable 1: enable

7.2.6.39. **LCD_FSYNC_GEN_DLY_REG(Default Value: 0x0000_0000)**

Offset: 0x240			Register Name: FSYNC_GEN_DLY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	sensor_act0_time Delay 0~4095 Pixel clk Period
15:12	/	/	/
11:0	R/W	0x0	sensor_act1_time Delay 0~4095 Pixel clk Period

7.2.6.40. **LCD_GAMMA_TABLE_REG(Default Value: 0x0000_0000)**

Offset: 0x400~0x7FF			Register Name: LCD_GAMMA_TABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x00	Red Component
15:8	R/W	0x00	Green Component
7:0	R/W	0x00	Blue Component

7.3. TCON_TV

7.3.1. Overview

The TCON_TV(Timing Controller_TV) is a module that processes video signals received from systems using a complicated arithmetic and then generates control signals and transmits them to the HDMI or TVE.

The TCON_TV includes the following features:

- Supports Gamma correction with R/G/B channel independence
- **V536-H**: Supports RGB interface with DE/SYNC mode,up to 4K@30fps
  V526: Supports RGB interface with DE/SYNC mode,up to 1080p@60fps

7.3.2. Block Diagram

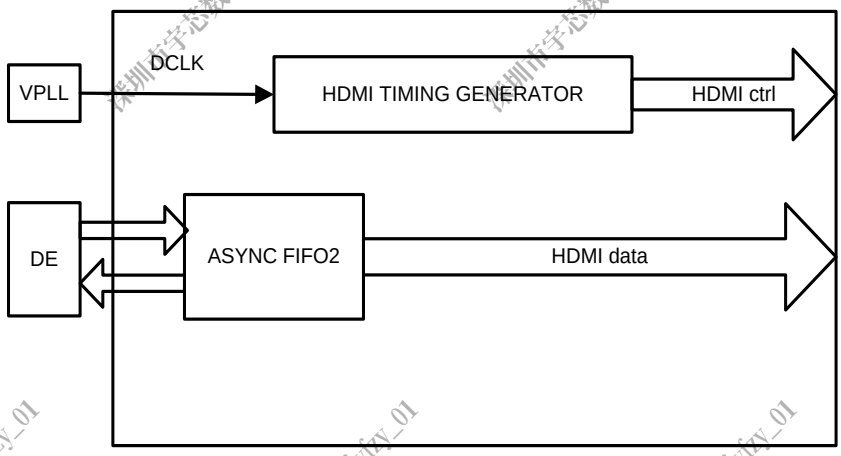


Figure 7-10. TCON_TV for HDMI Block Diagram

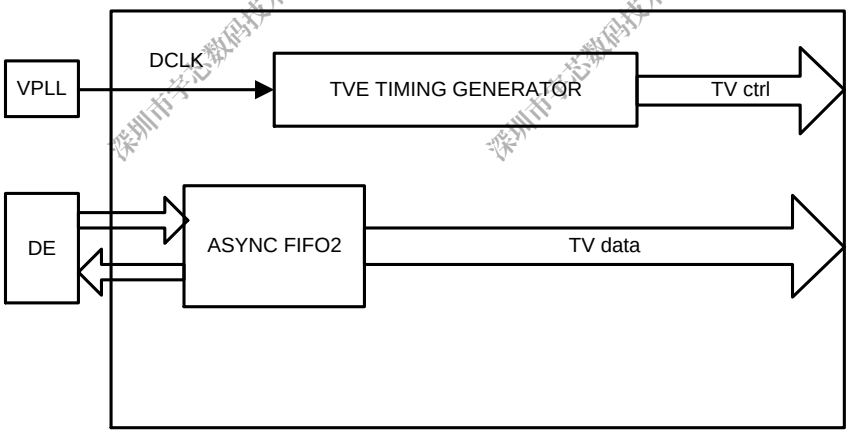


Figure 7-11. TCON_TV for TV Block Diagram

7.3.3. Operations and Functional Descriptions

7.3.3.1. Panel Interface

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.Its signals are defined as:

Table 7-7. HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicate one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
LDE	LCD data enable	O
LD[23..0]	24Bit RGB/YUV output from input FIFO for panel	O

HV control signals are active low.

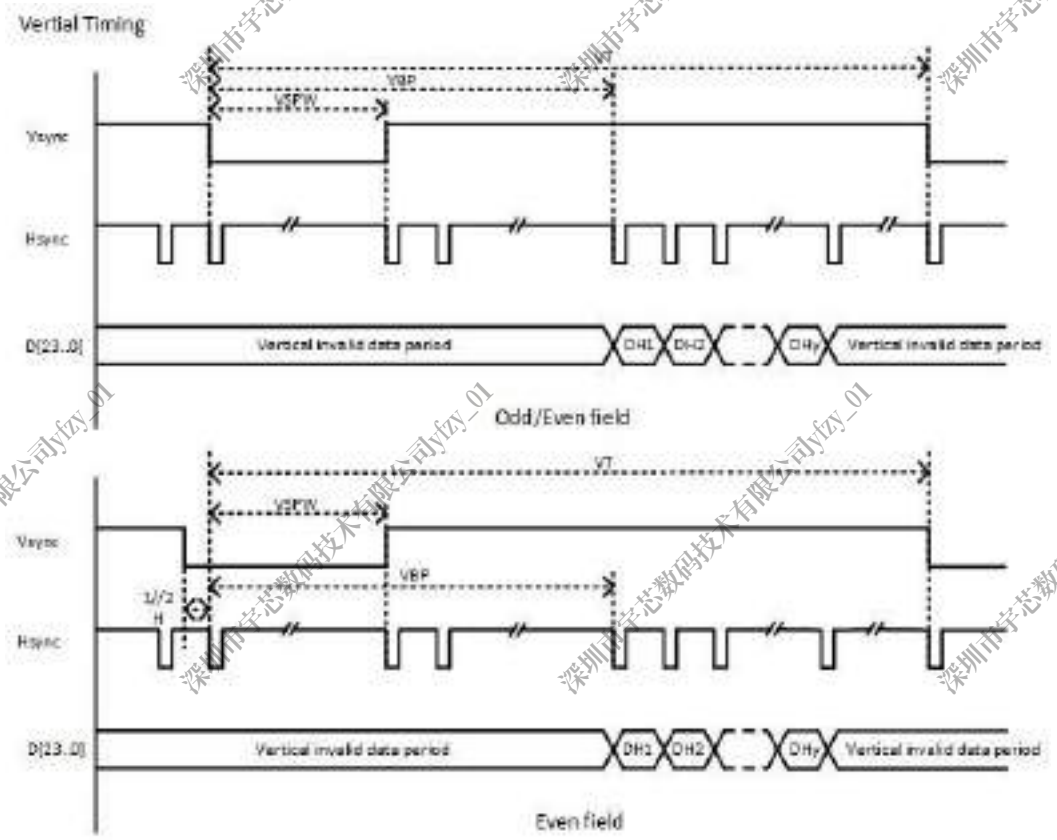


Figure 7-12. HV Interface Vertical Timing

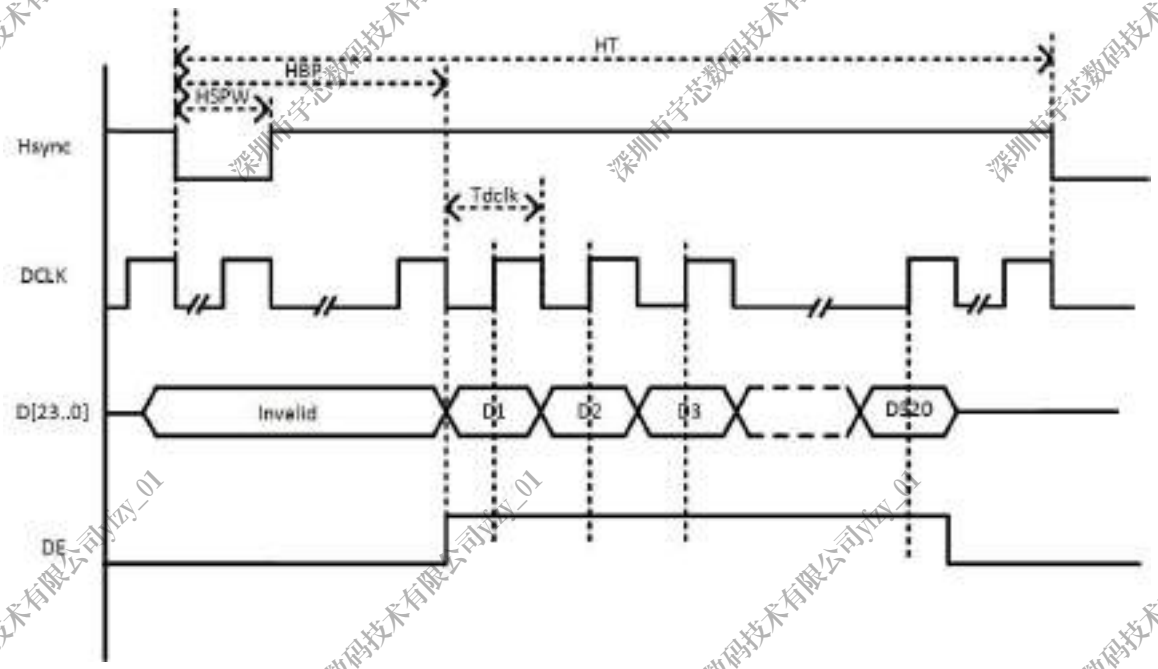


Figure 7-13. HV Interface Horizontal Timing

7.3.3.2. **Clock Sources**

The following table describes the clock sources of TCON_TV. Table 7-8 describes the clock sources of TCON_TV.

Table 7-8. TCON_TV Clock Sources

Clock Sources	Description
PLL_VIDEO0(1X)	Video PLL Clock,default value is 297MHz
PLL_VIDEO0(4X)	Video PLL Clock,default value is 1188MHz

7.3.3.3. **RGB Gamma Correction**

This module corrects the RGB input data of DE .
A 256*8*3 Byte register file is used to store the gamma table. The following is the layout.

Table 7-9. RGB Gamma Correction Table

Offset	Value
0x400, 0x401, 0x402	{ B0[7:0], G0[7:0], R0[7:0] }
0x404	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....
0x7FC	{ B255[7:0], G255[7:0], R255[7:0] }

7.3.3.4. **CEU Module**

This module enhance color data from DE .

R’ = Rr*R + Rg*G + Rb*B

G’ = Gr*R + Gg*G + Gb*B

B’ = Br*R + Bg*G + Bb*B

NOTE

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb bool 0,1

R, G, B u10 [0-1023]

R’ have the range of [Rmin ,Rmax]

G’ have the range of [Rmin ,Rmax]

B’ have the range of [Rmin ,Rmax]

7.3.4. Programming Guidelines

7.3.4.1. TCON_TV Configuration Process

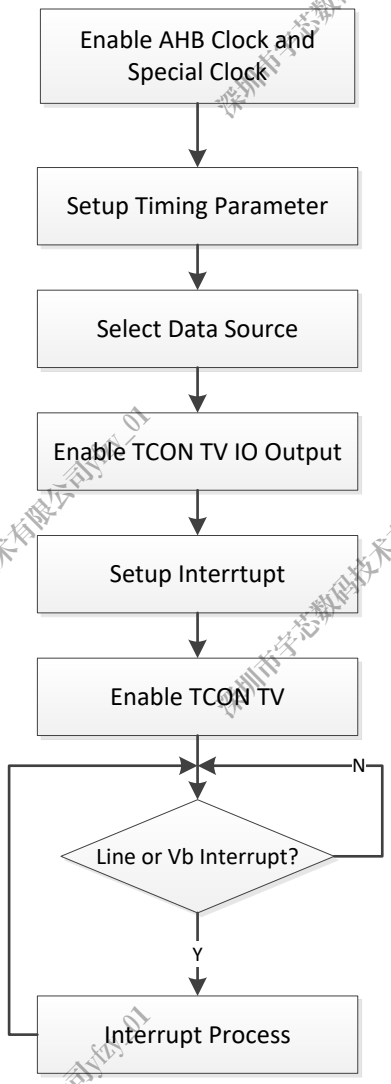


Figure 7-14. TCON TV Initial Process

Step1: Set special clock of CCU ,and dessert TCON TV related AHB clock gating and AHB reset .

Step2: Set timing parameter register of TCON TV, set corresponding resolution and standards followed, such as EIA or VESA.There are 8 parameters, including X ,HT ,HBP ,HSPW , Y , VT, VBP, VSPW. Note that for the controller,HBP includes HSPW width, VBP includes VSPW width, this is different with standard HBP and VBP.Note that for conversion.

Step3: Select TCON TV data sources. For the selecting of TCON TV data sources, it is decided by two setting. The first setting is the bit1(TV_SRC_SEL_GOBAL) of TV_CTL_REG, if setting to 1,then blue data is output; if setting to 0, then data source is decided by TV0_SRC_CTL_REG. According to needs, set up TV_SRC_SEL, select the required data sources.

Step4: The register offset of **TCON TV IO Output Function Setting** is 0x8C, writing 0 to the register to open output function.

Step5: Set and open interrupt. When using line interrupt, firstly TV_LINE_INT_NUM of TV_GINT1 need be set, secondly line interrupt is enabled, that is , the bit 28(TV_LINE_INT_EN) of TV_GINT0 is set to 1.

Step6: Start TCON TV.

7.3.4.2. **3D Mode Notes**

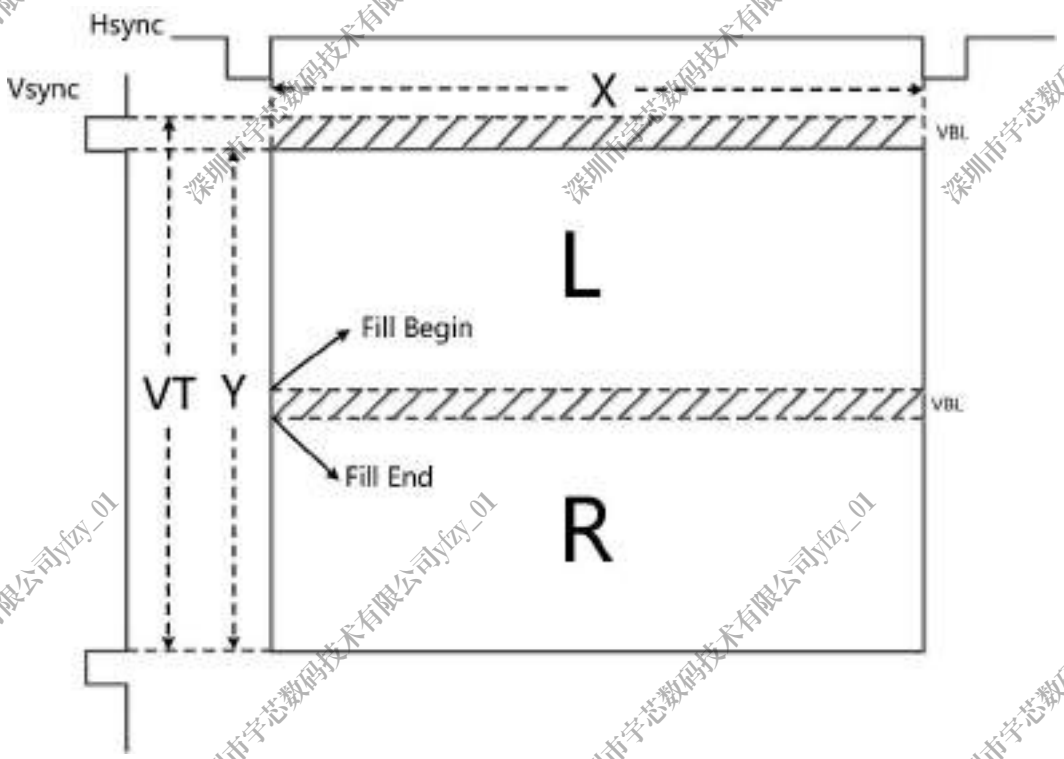


Figure 7-15. TCON TV 3D Mode Diagram

As shown in the above figure, VT= $VBL_L + Y_L + VBL_R + Y_R$, Y = $Y_L + VBL_R + Y_R$. But note that VT in this picture is the actual VT, is the half of VT in register.

In 3D mode, the 2 frames is synthesized into 1 frame to send data, so the effective data area will contain a blank area, this blank need be filled, and generally filled 0. The rest is to confirm the beginning and the end line of padding, the formula is as follows:

L_{begin} = VT/2 + 1, L_{end}=VT/2+(VT-Y)/2

Lastly, L_{begin} is filled to the bit[23:12] of TV_FILL_BEGIN_REG0(0x304), L_{end} is filled to the bit[23:12] of TV_FILL_END_RGB0(0x308), 0 is filled to TV_FILL_DATA_REG0(0x30C).

7.3.5. Register List

Module Name	Base Address
TCON_TV0	0x06515000

Register Name	Offset	Description
TV_GCTL_REG	0x0000	TV Global Control Register
TV_GINT0_REG	0x0004	TV Global Interrupt Register0
TV_GINT1_REG	0x0008	TV Global Interrupt Register1
TV_SRC_CTL_REG	0x0040	TV Source Control Register
TV_IO_POL_REG	0x0088	TV IO Polarity Register
TV_IO_TRI_REG	0x008C	TV IO Control Register
TV_CTL_REG	0x0090	TV Control Register
TV_BASIC0_REG	0x0094	TV Basic Timing Register0
TV_BASIC1_REG	0x0098	TV Basic Timing Register1
TV_BASIC2_REG	0x009C	TV Basic Timing Register2
TV_BASIC3_REG	0x00A0	TV Basic Timing Register3
TV_BASIC4_REG	0x00A4	TV Basic Timing Register4
TV_BASIC5_REG	0x00A8	TV Basic Timing Register5
TV_ECC_FIFO_REG	0x00F8	TV ECC FIFO Register
TV_DEBUG_REG	0x00FC	TV Debug Register
TV_CEU_CTL_REG	0x0100	TV CEU Control Register
TV_CEU_COEF_MUL_REG	0x0110+N*0x04	TV CEU Coefficient Register0(N=0,1,2,4,5,6,8,9,10)
TV_CEU_COEF_ADD_REG	0x011C+N*0x10	TV CEU coefficient register1(N=0,1,2)
TV_CEU_COEF_RANG_REG	0x0140+N*0x04	TV CEU Coefficient Register2(N=0,1,2)
TV_SAFE_PERIOD_REG	0x01F0	TV Safe Period Register
TV_FILL_CTL_REG	0x0300	TV Fill Data Control Register
TV_FILL_BEGIN_REG0	0x0304	TV Fill Data Begin Register0
TV_FILL_END_REG0	0x0308	TV Fill Data End Register0
TV_FILL_DATA_REG0	0x030C	TV Fill Data Value Register0
TV_FILL_BEGIN_REG1	0x0310	TV Fill Data Begin Register1
TV_FILL_END_REG1	0x0314	TV Fill Data End Register1
TV_FILL_DATA_REG1	0x0318	TV Fill Data Value Register1
TV_FILL_BEGIN_REG2	0x031C	TV Fill Data Begin Register2
TV_FILL_END_REG2	0x0320	TV Fill Data End Register2
TV_FILL_DATA_REG2	0x0324	TV Fill Data Value Register2

7.3.6. Registers Description

7.3.6.1. **TV Global Control Register(Default Value: 0x0000_0000)**

Offset: 0x0000			Register Name: TV_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_EN

			0: Disable 1: Enable When it is disabled, the module will be reset to idle state.
30	R/W	0x0	TV_GAMMA_EN 0: Disable 1: Enable Enable the Gamma correction function.
29:2	/	/	/
1	R/W	0x0	HDMI0_PAD_SEL 0:cec\ddc pad from gpio 1:cec\ddc pad from analog pad
0	/	/	/

7.3.6.2. **TV Global Interrupt Register0(Default Value: 0x0000_0000)**

Offset: 0x0004			**Register Name: TV_GINT0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TV_VB_INT_EN 0: Disable 1: Enable Enable the Vb interrupt.
29	/	/	/
28	R/W	0x0	TV_LINE_INT_EN 0: Disable 1: Enable Enable the line interrupt.
27:15	/	/	/
14	R/W	0x0	TV_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12	R/W	0x0	TV_LINT_INT_FLAG Trigger when SY1 match the current TV scan line Write 0 to clear it.
11:0	/	/	/

7.3.6.3. **TV Global Interrupt Register1(Default Value: 0x0000_0000)**

Offset: 0x0008			**Register Name: TV_GINT1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	TV_LINE_INT_NUM Scan line for TV line trigger(including inactive lines)

			Setting it for the specified line for trigger 1. SY1 is writable only when LINE_TRG1 disable.

7.3.6.4. **TV Source Control Register(Default Value: 0x0000_0000)**

Offset: 0x0040			Register Name: TV_SRC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	TV_SRC_SEL 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Reserved 101: Reserved 111: Gridding Check

7.3.6.5. **TV IO Polarity Register(Default Value: 0x0000_0000)**

Offset: 0x0088			Register Name: TV_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	IO3_INV 0: Not invert 1: Invert Enable invert function of IO3.
26	R/W	0x0	IO2_ INV 0: Not invert 1: Invert Enable invert function of IO2.
25	R/W	0x0	IO1_INV 0: Not invert 1: Invert Enable invert function of IO1.
24	R/W	0x0	IO0_INV 0: Not invert 1: Invert Enable invert function of IO0.
23:0	R/W	0x0	Data_INV 0: Normal polarity 1: Invert the specify output LCD output port D[23:0] polarity control, with independent bit control.

7.3.6.6. **TV IO Control Register(Default Value: 0x0FFF_FFFF)**

Offset: 0x008C			Register Name: TV_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO3.
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO2.
25	R/W	0x1	IO1_OUTPUR_TRI_EN 1: Disable 0: Enable Enable the output of IO1.
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO0.
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN 1: Disable 0: Enable TV output port D[23:0] output enable, with independent bit control.

7.3.6.7. **TV Control Register(Default Value: 0x0000_0000)**

Offset: 0x0090			Register Name: TV_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_EN 0: Disable 1: Enable
30:9	/	/	/
8:4	R/W	0x0	START_DELAY This is for DE.
3:2	/	/	/
1	R/W	0x0	TV_SRC_SEL 0: reserved 1: BLUE data(FIFO2 disable, RGB=0000FF) **NOTE** **The priority of this bit is higher than TV_SRC_SEL(bit[2:0]) in TV_SRC_CTL_REG.**
0	/	/	/

7.3.6.8. **TV Basic Timing Register0(Default Value: 0x0000_0000)**

Offset: 0x0094			Register Name: TV_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	XI source width is X+1
15:12	/	/	/
11:0	R/W	0x0	YI source height is Y+1

7.3.6.9. **TV Basic Timing Register1(Default Value: 0x0000_0000)**

Offset: 0x0098			Register Name: TV_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LS_XO Width is LS_XO+1
15:12	/	/	/
11:0	R/W	0x0	LS_YO Width is LS_YO+1 **NOTE** **LS_YO = TV_YI**

7.3.6.10. **TV Basic Timing Register2(Default Value: 0x0000_0000)**

Offset: 0x009C			Register Name: TV_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TV_XO Width is TV_XO+1
15:12	/	/	/
11:0	R/W	0x0	TV_YO Height is TV_YO+1

7.3.6.11. **TV Basic Timing Register3(Default Value: 0x0000_0000)**

Offset: 0x00A0			Register Name: TV_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/

28:16	R/W	0x0	HT Horizontal total time T_{hcycle} = (HT+1) * T_{hdclk}
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch T_{hbp} = (HBP +1) * T_{hdclk}

7.3.6.12. **TV Basic Timing Register4(Default Value: 0x0000_0000)**

Offset: 0x00A4			**Register Name: TV_BASIC4_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT Vertical total time (in HD line) T_{vt} = VT/2 * T_h
15:12	/	/	/
11:0	R/W	0x0	VBP Vertical back porch (in HD line) T_{vbp} = (VBP +1) * T_h

7.3.6.13. **TV Basic Timing Register5(Default Value: 0x0000_0000)**

Offset: 0x00A8			**Register Name: TV_BASIC5_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Horizontal Sync Pulse Width (in dclk) T_{hspw} = (HSPW+1) * T_{dclk} HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Vertical Sync Pulse Width (in lines) T_{vspw} = (VSPW+1) * T_h VT/2 > (VSPW+1)

7.3.6.14. **TV ECC FIFO Register(Default Value: 0x0000_0000)**

Offset: 0x00F8			**Register Name: TV_ECC_FIFO_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ECC_FIFO_BIST_EN 0: Disable 1: Enable

			Enable ECC FIFO BIST test function.
30	R	0x0	ECC_FIFO_ERR_FLAG Indicates the error information in ECC FIFO.
29:24	/	/	/
23:16	R	0x0	ECC_FIFO_ERR_BITS Indicates the error information in ECC FIFO.
15:9	/	/	/
8	R/W	0x0	ECC_FIFO_BLANK_EN 0: Disable ECC function in blanking 1: Enable ECC function in blanking ECC function is tent to triggered in blanking area at HV mode, set '0' when in HV mode.
7:4	/	/	/
3	R/W	0x0	ECC_FIFO_SETTING 0:Enable 1:Disable Enable ECC FIFO function.
2:0	/	/	/

7.3.6.15. **TV Debug Register(Default Value: 0x0000_0000)**

Offset: 0x00FC			**Register Name: TV_DEBUG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TV_FIFO_UNDERFLOW 0: Not underflow 1: Underflow The flag shows whether the FIFOs in underflow status.
29	/	/	/
28	R	0x0	TV_FIELD_POL 0: Second field 1: First field The flag indicates the current field polarity.
27:12	/	/	/
13	R/W	0x0	ECC_FIFO_BYPASS 0: Used 1: Bypass Setup that whether to bypass ECC FIFO.
12	/	/	/
11:0	R	0x0	TV_CURRENT_LINE The current scan line.

7.3.6.16. **TV CEU Control Register(Default Value: 0x0000_0000)**

Offset: 0x0100			Register Name: TV_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN 0: Bypass 1: Enable Enable CEU function.
30:0	/	/	/

7.3.6.17. **TV CEU Coefficient Register0(Default Value: 0x0000_0000)**

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: TV_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb Signed 13bit value, range of (-16,16).

7.3.6.18. **TV CEU Coefficient Register1(Default Value: 0x0000_0000)**

Offset: 0x011C+N*0x10(N=0,1,2)			Register Name: TV_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE N=0: Rc N=1: Gc N=2: Bc Signed 19bit value, range of (-16384, 16384).

7.3.6.19. **TV CEU Coefficient Register2(Default Value: 0x0000_0000)**

Offset: 0x0140+N*0x04 (N=0,1,2)	Register Name: TV_CEU_COEF_RANG_REG

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8bit value, range of [0,255]

7.3.6.20. **TV Safe Period Register(Default Value: 0x0000_0020)**

Offset: 0x01F0			Register Name: TV_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM,LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x2	SAFE_PERIOD_LINE Set a fixed line and during the line time,LCD controller allow dram controller to change frequency.The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM 011: safe at 2 and safe at sync active 100: safe at line Select the save mode.

7.3.6.21. **TV Fill Data Control Register(Default Value: 0x0000_0000)**

Offset: 0x0300			Register Name: TV_FILL_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_FILL_EN 0: Bypass 1: Enable Enable the fill data function in blanking area.This is only used in HDMI 3D mode.
30:0	/	/	/

7.3.6.22. **TV Fill Data Begin Register0(Default Value: 0x0000_0000)**

Offset: 0x0304	Register Name: TV_FILL_BEGIN_REG0

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	FILL_BEGIN Set the begin point of the fill data area.

7.3.6.23. **TV Fill Data End Register0(Default Value: 0x0000_0000)**

Offset: 0x0308			Register Name: TV_FILL_END_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END Set the end point of the fill data area.

7.3.6.24. **TV Fill Data Value Register0(Default Value: 0x0000_0000)**

Offset: 0x030C			Register Name: TV_FILL_DATA_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:0	R/W	0x0	FILL_VALUE Set the data value which is used to fill into the blanking area between two frames in HDMI 3D mode.

7.3.6.25. **TV Fill Data Begin Register1(Default Value: 0x0000_0000)**

Offset: 0x0310			Register Name: TV_FILL_BEGIN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_BEGIN Set the begin point of the fill data area.

7.3.6.26. **TV Fill Data End Register1(Default Value: 0x0000_0000)**

Offset: 0x314			Register Name: TV_FILL_END_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END Set the end point of the fill data area.

7.3.6.27. **TV Fill Data Value Register1(Default Value: 0x0000_0000)**

Offset: 0x0318	Register Name: TV_FILL_DATA_REG1

Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	0x0	FILL_VALUE Set the data value which is used to fill into the blanking area between two frames in HDMI 3D mode.

7.3.6.28. **TV Fill Data Begin Register2(Default Value: 0x0000_0000)**

Offset: 0x031C			Register Name: TV_FILL_BEGIN_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_BEGIN Set the begin point of the fill data area.

7.3.6.29. **TV Fill Data End Register2(Default Value: 0x0000_0000)**

Offset: 0x0320			Register Name: TV_FILL_END_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END Set the end point of the fill data area.

7.3.6.30. **TV Fill Data Value Register2(Default Value: 0x0000_0000)**

Offset: 0x0324			Register Name: TV_FILL_DATA_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:0	R/W	0x0	FILL_VALUE Set the data value which is used to fill into the blanking area between two frames in HDMI 3D mode.

7.4. MIPI DSI

7.4.1. Overview

The MIPI Display Serial Interface(DSI) is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces. This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.01 and a D-PHY module which is compliance with MIPI DPHY specification V1.00.

The MIPI DSI includes the following features:

- Compliance with MIPI DSI v1.01 , MIPI D-PHY v1.00 and MIPI DCS v1.02
- 1/2/3/4 data lanes configuration and up to 1Gbps per lane
- Supports ECC,CRC generation and EOT package
- Up to 1920 x 1080@60fps with 4 data lanes
- Pixel format: RGB888, RGB666, RGB666 packed, and RGB565
- Supports video mode
  - Non-burst mode with sync pulses
  - Non-burst mode with sync event
  - Burst mode
- Supports command mode up to 20MHz pixel clk

7.4.2. Block Diagram

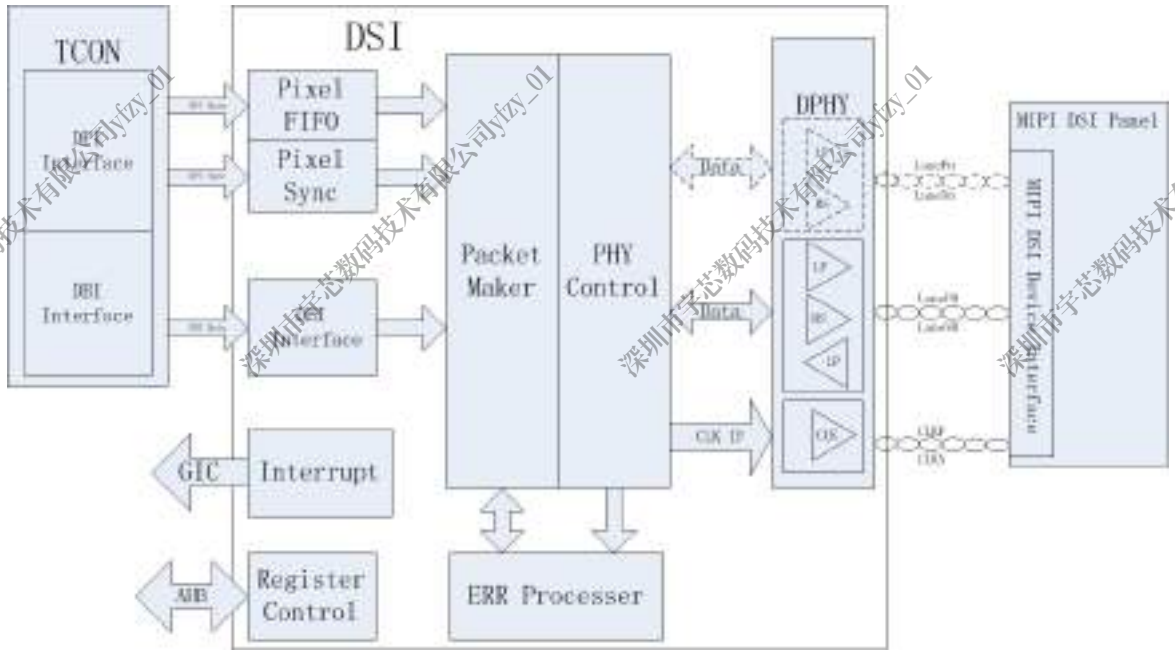


Figure 7-16. MIPI DSI Block Diagram

7.5. TV Encoder

7.5.1. Overview

The TV Encoder(TVE) module is a highly programmable digital video encoder supporting worldwide video standards Composite Video Broadcast Signal (CVBS).

The TVE includes the following features:

- 1 channel CVBS, PAL-D and NTSC-M supported
- Plug status auto detecting
- 10 bits DAC output

7.5.2. Block Diagram

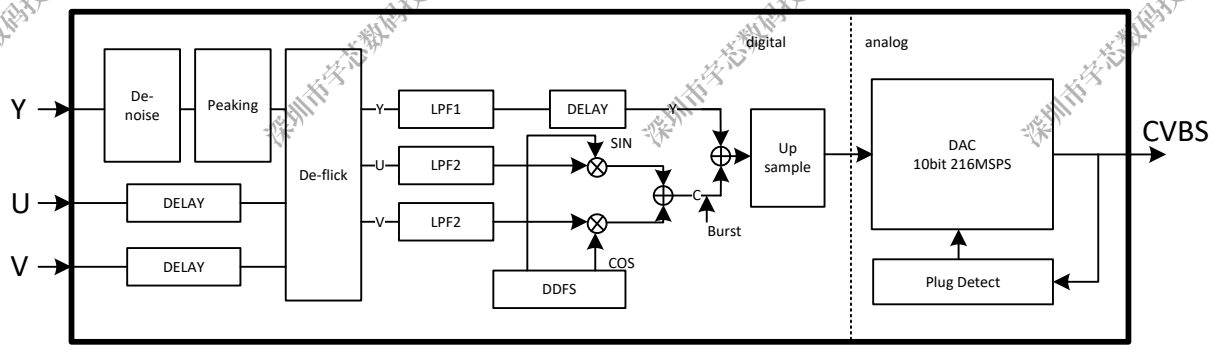


Figure 7-17. TVE Block Diagram

7.5.3. Operations and Functional Descriptions

7.5.3.1. External Signals

Table 7-10 describes the external signals of TVE.

Table 7-10. TVE External Signals

Pin Name	Function Description	Type
TV-VCC	TV DAC power, 1.8V±0.06V	P
TV-OUT	TV CVBS output	AO

7.5.3.2. Clock Sources

The TVE module requires one clock with 50% duty. Digital circuit and Analog circuit work by this clock. Mode and Clock frequency is shown below.

Table 7-11. TVE Clock Sources

Mode	TVE Clock Frequency
NTSC	216MHz
PAL	216MHz

7.5.4. Programming Guidelines

(1) Operate TVE module by below step, the process is shown in Figure 7-18.

Step 1: Set CCU clock source for TVE, and release AHB bus, and module reset.

Step2: Initial DAC amplitude value from efuse calibration value which has burned.

Step3: Enable plug-in detect function, and detect plug-in status every 200ms.

Step4: When plug-in has detected, configure TVE module to output mode setting by application.

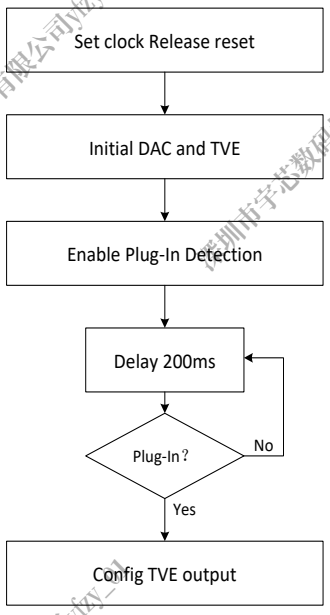


Figure 7-18. Operate TVE Process

(2) Auto Detect Function

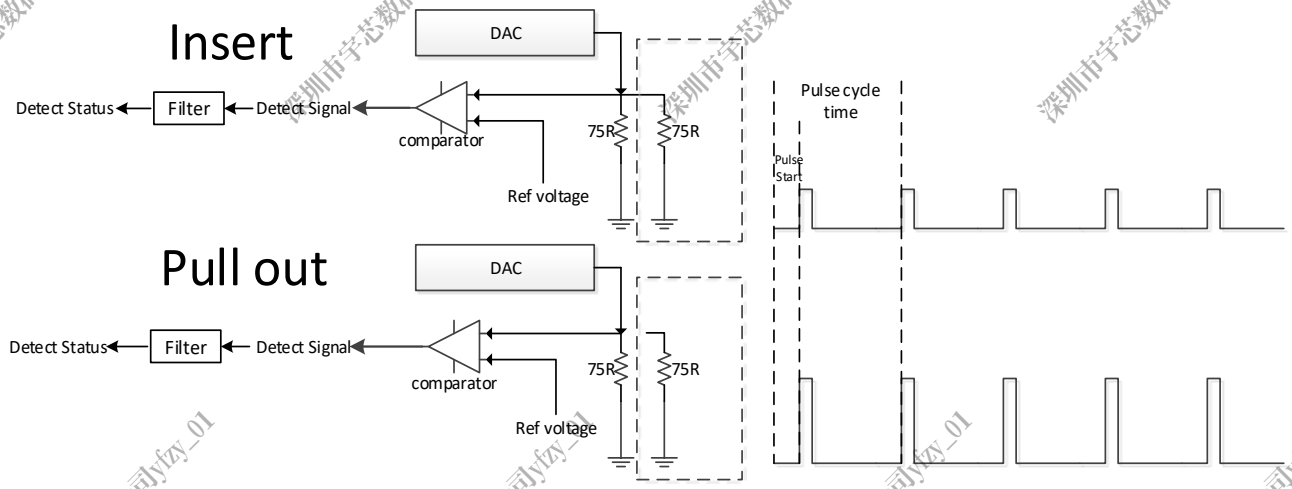


Figure 7-19. Auto Detect Function

DAC outputs constant current, when insert, external load is 37.5Ω; when pull out, external load is 75Ω. The method that

comparator judges pin level can detect plug action.

Because plug action may exist jitter, then there need be a filter to filter jitter, the debounce time of filter is set through the bit[3:0] of TV Encoder Auto Detection de-bounce Setting Register.

The pulse cycle time can be set through the bit[30:16] of TV Encoder Auto Detect Configuration Register1, the pulse start time can be set through the bit[14:0] of TV Encoder Auto Detect Configuration Register1.The clock sources of the two time are 32768Hz clock.

Pulse width is cycle time of 4 clock sources.

Pulse amplitude can be set through the bit[9:0] of TV Encoder Auto Detect Configuration Register0.

(3) DAC Calibration

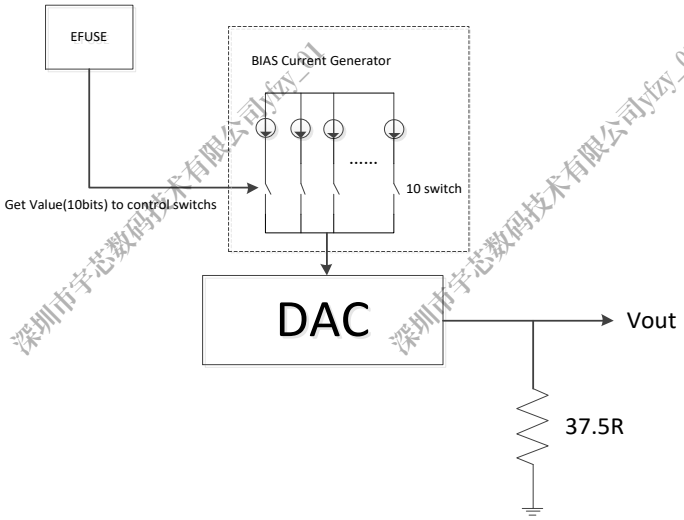


Figure 7-20. DAC Calibration

After FT, 10-bit calibration value is burned to efuse. Every time software can read the 10-bit calibration value from efuse, to control BIAS current and BIAS current switch, then a specific BIAS current is generated to calibrate maximum output voltage of DAC.

7.5.5. Register List

Module Name	Base Address
TVE_TOP	0x06520000
TVE	0x06524000

Register Name	Offset	Description
TVE_TOP		
TVE_DAC_MAP	0x0020	TV Encoder DAC MAP Register
TVE_DAC_STATUS	0x0024	TV Encoder DAC STAUTS Register
TVE_DAC_CFG0	0x0028	TV Encoder DAC CFG0 Register
TVE_DAC_CFG1	0x002C	TV Encoder DAC CFG1 Register
TVE_DAC_CFG2	0x0030	TV Encoder DAC CFG2 Register
TVE_DAC_CFG3	0x0034	TV Encoder DAC CFG2 Register
TVE_DAC_TEST	0x00F0	TV Encoder DAC TEST Register
TVE		
TVE_000_REG	0x0000	TV Encoder Clock Gating Register

Register Name	Offset	Description
TVE_004_REG	0x0004	TV Encoder Configuration Register
TVE_008_REG	0x0008	TV Encoder DAC Register1
TVE_00C_REG	0x000C	TV Encoder Notch and DAC Delay Register
TVE_010_REG	0x0010	TV Encoder Chroma Frequency Register
TVE_014_REG	0x0014	TV Encoder Front/Back Porch Register
TVE_018_REG	0x0018	TV Encoder HD Mode VSYNC Register
TVE_01C_REG	0x001C	TV Encoder Line Number Register
TVE_020_REG	0x0020	TV Encoder Level Register
TVE_024_REG	0x0024	TV Encoder DAC Register2
TVE_030_REG	0x0030	TV Encoder Auto Detection Enable Register
TVE_034_REG	0x0034	TV Encoder Auto Detection Interrupt Status Register
TVE_038_REG	0x0038	TV Encoder Auto Detection Status Register
TVE_03C_REG	0x003C	TV Encoder Auto Detection de-bounce Setting Register
TVE_0F8_REG	0x00F8	TV Encoder Auto Detect Configuration Register0
TVE_0FC_REG	0x00FC	TV Encoder Auto Detect Configuration Register1
TVE_100_REG	0x0100	TV Encoder Color Burst Phase Reset Configuration Register
TVE_104_REG	0x0104	TV Encoder VSYNC Number Register
TVE_108_REG	0x0108	TV Encoder Notch Filter Frequency Register
TVE_10C_REG	0x010C	TV Encoder Cb/Cr Level/Gain Register
TVE_110_REG	0x0110	TV Encoder Tint and Color Burst Phase Register
TVE_114_REG	0x0114	TV Encoder Burst Width Register
TVE_118_REG	0x0118	TV Encoder Cb/Cr Gain Register
TVE_11C_REG	0x011C	TV Encoder Sync and VBI Level Register
TVE_120_REG	0x0120	TV Encoder White Level Register
TVE_124_REG	0x0124	TV Encoder Video Active Line Register
TVE_128_REG	0x0128	TV Encoder Video Chroma BW and CompGain Register
TVE_12C_REG	0x012C	TV Encoder Register
TVE_130_REG	0x0130	TV Encoder Re-sync Parameters Register
TVE_134_REG	0x0134	TV Encoder Slave Parameter Register
TVE_138_REG	0x0138	TV Encoder Configuration Register0
TVE_13C_REG	0x013C	TV Encoder Configuration Register1
TVE_380_REG	0x0380	TV Encoder Low Pass Control Register
TVE_384_REG	0x0384	TV Encoder Low Pass Filter Control Register
TVE_388_REG	0x0388	TV Encoder Low Pass Gain Register
TVE_38C_REG	0x038C	TV Encoder Low Pass Gain Control Register
TVE_390_REG	0x0390	TV Encoder Low Pass Shoot Control Register
TVE_394_REG	0x0394	TV Encoder Low Pass Coring Register
TVE_3A0_REG	0x03A0	TV Encoder Noise Reduction Register

7.5.6. Register Description

7.5.6.1. TV Encoder DAC MAP Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: TVE_DAC_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DAC_MAP 000: OUT0 Others: Reserved
3:2	/	/	/
1:0	R/W	0x0	DAC_SEL 00: Reserved 01: TVE0 10: Reserved 11: Reserved

7.5.6.2. TV Encoder DAC Status Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TVE_DAC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R	0x0	DAC_STATUS 00: Unconnected 01: Connected 11: Short to ground 10: Reserved

7.5.6.3. TV Encoder DAC Configuration0 Register(Default Value: 0x8000_4200)

Offset: 0x0028			Register Name: TVE_DAC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	DAC_CLOCK_INVERT 0: Not invert 1: Invert
30:26	/	/	/
25:16	R/W	0x0	CALI_IN
15:12	R/W	0x4	Reserved
11:10	/	/	/
9	R/W	0x1	Reserved
8	R/W	0x0	Reserved
7:5	/	/	/
4	R/W	0x0	Reserved
3:1	/	/	/

Offset: 0x0028			Register Name: TVE_DAC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	DAC_EN 0: Disable 1: Enable

7.5.6.4. TV Encoder DAC Configuration1 Register(Default Value: 0x0000_023A)

Offset: 0x002C			Register Name: TVE_DAC_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	Reserved
8	R/W	0x0	Reserved
7:6	/	/	/
5:4	R/W	0x3	REF2_SEL 00: 0.25V 01: 0.30V 10: 0.35V 11: 0.40V (a_refslct2<1:0>)
3:0	R/W	0xA	REF1_SEL 0000: 0.50V 0001: 0.55V 0010: 0.60V 0011: 0.65V 0100: 0.70V 0101: 0.75V 0110: 0.80V 0111: 0.85V 1000: 0.90V 1001: 0.95V 1010: 1.00V 1011: 1.05V 1100: 1.10V 1101: 1.15V 1110: 1.20V 1111: 1.25V (a_refslct1<3:0>) The reference voltage is used for hot plug detect function.

7.5.6.5. **TV Encoder DAC Configuration2 Register(Default Value: 0x0000_0010)**

Offset: 0x0030			Register Name: TVE_DAC_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:6	R/W	0x0	Reserved
5:0	R/W	0x10	Reserved

7.5.6.6. **TV Encoder DAC Configuration3 Register(Default Value: 0x0000_0000)**

Offset: 0x0034			Register Name: TVE_DAC_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	FORCE_DATA_SET Force DAC input data
15:1	/	/	/
0	R/W	0x0	FORCE_DATA_EN 0:DAC input data from TVE 1: DAC input data from FORCE_DATA_SET

7.5.6.7. **TV Encoder DAC Test Register(Default Value: 0x0000_0000)**

Offset: 0x00F0			Register Name: TVE_DAC_TEST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	DAC_TEST_LENGTH DAC TEST DATA LENGTH
15:6	/	/	/
5:4	R/W	0x0	DAC_TEST_SEL 00: DAC0 Others: Reserved
3:1	/	/	/
0	R/W	0x0	DAC_TEST_ENABLE 0: Reserved 1: Repeat DAC data from DAC sram

7.5.6.8. **TV Encoder Clock Gating Register(Default Value: 0x0000_0000)**

Offset: 0x0000			Register Name: TVE_000_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLOCK_GATE_DIS 0: Enable 1: Disable

Offset: 0x0000			Register Name: TVE_000_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
30:29	/	/	/
28	R/W	0x0	BIST_EN 0: Normal mode 1: Bist mode
27:23	/	/	/
22	R/W	0x0	upsample for YPbPr 0:1x 1:2x
21:20	R/W	0x0	upsample for CVBS Out up sample 00: 27MHz 01: 54MHz 10: 108MHz 11: 216MHz
19:4	/	/	/
3:1	/	/	/
0	R/W	0x0	TVE_EN 0: Disable 1: Enable Video Encoder enable, default disable, write 1 to take it out of the reset state

7.5.6.9. **TV Encoder Configuration Register(Default Value: 0x0001_0000)**

Offset: 0x0004			Register Name: TVE_004_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	BYPASS_TV 0: Disable 1: Enable
28:27	R/W	0x0	DAC_SRC_SEL 00: TV Encoder 01: LCD controller, override all other TV encoder setting, the DAC clock can from LCD controller. 10: DAC test mode,DAC using DAC clock 11: DAC test mode, DAC using AHB clock
26	R/W	0x0	DAC_CONTROL_LOGIC_CLOCK_SEL 0: Using 27MHz clock or 74.25MHz clock depend on CCU setting 1: Using 54MHz clock or 148.5MHz clock depend on CCU setting
25	R/W	0x0	CORE_DATAPATH_LOGIC_CLOCK_SEL 0: Using 27MHz clock or 74.25MHz clock depend on CCU setting 1: Using 54MHz clock or 148.5MHz clock depend on CCU setting
24	R/W	0x0	CORE_CONTROL_LOGIC_CLOCK_SEL 0: Using 27MHz clock or 74.25MHz clock depend on CCU setting

Offset: 0x0004			Register Name: TVE_004_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Using 54MHz clock or 148.5MHz clock depend on CCU setting
23:21	/	/	/
20	R/W	0x0	CB_CR_SEQ_FOR_422_MODE 0: Cb first 1: Cr first
19	R/W	0x0	INPUT_CHROMA_DATA_SAMPLING_RATE_SEL 0: 4:4:4 1: 4:2:2
18	R/W	0x0	YUV_RGB_OUTPUT_EN 0: CVBS 1: Reserved
17	R/W	0x0	YC_EN 0: Y/C is disable 1: Reserved S-port Video enables selection. This bit selects whether the S-port(Y/C) video output is enabled or disabled.
16	R/W	0x1	CVBS_EN 0: Composite video is disabled, Only Y/C is enabled 1: Composite video is enabled, CVBS and Y/C are enabled Composite video enables selection. This bit selects whether the composite video output (CVBS) is enabled or disabled.
15:10	/	/	/
9	R/W	0x0	COLOR_BAR_TYPE 0: 75/7.5/75/7.5 (NTSC), 100/0/75/0(PAL) 1: 100/7.5/100/7.5(NTSC), 100/0/100/0(PAL)
8	R/W	0x0	COLOR_BAR_MODE 0: The Video Encoder input is coming from the Display Engineer 1: The Video Encoder input is coming from an internal standard color bar generator. **NOTE** **Standard Color bar input selection.** **This bit selects whether the Video Encoder video data input is replaced by an internal standard color bar generator or not.**
7:5	/	/	/
4	R/W	0x0	MODE_1080I_1250LINE_SEL 0: 1125 Line mode 1: 1250 Line mode
3:0	R/W	0x0	TVMODE_SELECT 0000: NTSC 0001: PAL 0010: Reserved 0011: Reserved

Offset: 0x0004			Register Name: TVE_004_REG
Bit	Read/Write	Default/Hex	Description
			01xx: Reserved 100x: Reserved 101x: Reserved 110x: Reserved 111x: Reserved Changing this register value will cause some relative register setting to relative value.

7.5.6.10. **TV Encoder DAC Register1(Default Value: 0x0000_0000)**

Offset: 0x0008			Register Name: TVE_008_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DAC0_SRC_SEL 000: Composite Others: Reserved
3:0	/	/	/

7.5.6.11. **TV Encoder Notch and DAC Delay Register(Default Value: 0x0201_4924)**

Offset: 0x000C			Register Name: TVE_00C_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CHROMA_FILTER_ACTIVE_VALID 0: Disable 1: Enable
30	R/W	0x0	LUMA_FILTER_LTI_ENABLE 0: Disable Luma filter lti 1: Enable Luma filter lti
27:25	R/W	0x1	Y_DELAY_BEFORE_DITHER
24	R/W	0x0	HD_MODE_CB_FILTER_BYPASS 0: Bypass Enable 1: Bypass Disable
23	R/W	0x0	HD_MODE_CR_FILTER_BYPASS 0: Bypass Enable 1: Bypass Disable
22	R/W	0x0	CHROMA_FILTER_1_444_EN 0: Chroma Filter 1 444 Disable 1: Chroma Filter 1 444 Enable
21	R/W	0x0	CHROMA_HD_MODE_FILTER_EN 0: Chroma HD Filter Disable 1: Chroma HD Filter Enable
20	R/W	0x0	CHROMA_FILTER_STAGE_1_BYPASS

Offset: 0x000C			Register Name: TVE_00C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Chroma Filter Stage 1 Enable 1: Chroma Filter Stage 1 bypass
19	R/W	0x0	CHROMA_FILTER_STAGE_2_BYPASS 0: Chroma Filter Stage 2 Enable 1: Chroma Filter Stage 2 bypass
18	R/W	0x0	CHROMA_FILTER_STAGE_3_BYPASS 0: Chroma Filter Stage 3 Enable 1: Chroma Filter Stage 3 bypass
17	R/W	0x0	LUMA_FILTER_BYPASS 0: Luma Filter Enable 1: Luma Filter bypass
16	R/W	0x1	NOTCH_EN 0: The luma notch filter is bypassed 1: The luma notch filter is operating Luma notch filter on/off selection **NOTE** **This bit selects if the luma notch filter is operating or bypassed.**
15:12	R/W	0x4	C_DELAY_BEFORE_DITHER
11:0	R/W	0x924	Reserved

7.5.6.12. TV Encoder Chroma Frequency Register(Default Value: 0x21F0_7C1F)

Offset: 0x0010			Register Name: TVE_010_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x21f07c1f	CHROMA_FREQ Specify the ratio between the color burst frequency. 32 bits unsigned fraction. Default value is h21f07c1f, which is compatible with NTSC specs. 3.5795455 MHz (X'21F07C1F'): NTSC-M, NTSC-J 4.43361875 MHz(X'2A098ACB'): PAL-B, D, G, H,I, N 3.582056 MHz (X'21F69446'): PAL-N(Argentina) 3.579611 MHz (X'21E6EFE3'): PAL-M

7.5.6.13. TV Encoder Front/Back Porch Register(Default Value: 0x0076_0020)

Offset: 0x0014			Register Name: TVE_014_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x76	BACK_PORCH Specify the width of the back porch in encoder clock cycles. Min value is (*burst_width+breeze_way*+17). 8 bits unsigned integer. Default value is 118. 720p mode, is 260

Offset: 0x0014			Register Name: TVE_014_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1080i/p mode, is 192
15:12	/	/	/
11:0	R/W	0x20	FRONT_PORCH Must be even. Specify the width of the front porch in encoder clock cycles. 6 bits unsigned even integer. Allowed range is 10 to 62. Default value is 32 in 1080i mode is 44.

7.5.6.14. **TV Encoder HD Mode VSYNC Register(Default Value: 0x0000_0016)**

Offset: 0x0018			Register Name: TVE_018_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BROAD_PLUS_CYCLE_NUMBER_IN_HD_MODE_VSYNC
15:12	/	/	/
11:0	R/W	0x16	FRONT_PORCH_LIKE_IN_HD_MODE_VSYNC

7.5.6.15. **TV Encoder Line Number Register(Default Value: 0x0016_020D)**

Offset: 0x001C			Register Name: TVE_01C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x16	FIRST_VIDEO_LINE Specify the index of the first line in a field/frame to have active video. 8 bits unsigned integer. For interlaced video: When VSync5=B'0', FirstVideoLine is restricted to be greater than 7. When VSync5=B'1', FirstVideoLine is restricted to be greater than 9. Default value is 21.
15:11	/	/	/
10:0	R/W	0x20D	NUM_LINES Specify the total number of lines in a video frame. 11 bits unsigned integer. Allowed range is 0 to 2048. Default value is 525. For interlaced video: When NTSC, and FirstVideoLine is greater than 20, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When NTSC, and FirstVideoLine is not greater than 20, then NumLines is restricted to be greater than 77. When PAL, and FirstVideoLine is greater than 22, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When PAL, and FirstVideoLine is not greater than 22, then NumLines is restricted to be greater than 81. If NumLines is even, then it is restricted to be divisible by 4. If NumLines is odd, then it is restricted to be divisible by 4 with a remainder of 1.

7.5.6.16. **TV Encoder Level Register(Default Value: 0x00F0_011A)**

Offset: 0x0020			Register Name: TVE_020_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0xf0	BLANK_LEVEL Specify the blank level setting for active lines. 10 bits unsigned integer. Allowed range 0 to 1023. Default value is 0xF0(dec240).
15:10	/	/	/
9:0	R/W	0x11a	BLACK_LEVEL Specify the black level setting. 10 bits unsigned integer. Allowed range is 240 to 1023. Default value is 282.

7.5.6.17. **TV Encoder Auto Detection Enable Register(Default Value: 0x0000_0000)**

Offset: 0x0030			Register Name: TVE_030_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DAC0_AUTO_DETECT_INTERRUPT_EN
15:1	/	/	/
0	R/W1C	0x0	DAC0_AUTO_DETECT_ENABLE

7.5.6.18. **TV Encoder Auto Detection Interrupt Status Register(Default Value: 0x0000_0000)**

Offset: 0x0034			Register Name: TVE_034_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DAC0_AUTO_DETECT_INTERRUPT_ACTIVE_FLAG Write 1 to inactive DAC0 auto detection interrupt

7.5.6.19. **TV Encoder Auto Detection Status Register(Default Value: 0x0000_0000)**

Offset: 0x0038			Register Name: TVE_038_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R	0x0	DAC0_STATUS 00: Unconnected 01: Connected 11: Short to ground 10: Reserved

7.5.6.20. **TV Encoder Auto Detection Debounce Setting Register(Default Value: 0x0000_0000)**

Offset: 0x003C			Register Name: TVE_03C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	DAC_TEST_REGISTER DAC test register.
15:4	/	/	/
3:0	R/W	0x0	DAC0_De_Bounce_Times The de_bounce time for hot plug detect function.

7.5.6.21. **TV Encoder Auto Detection Configuration Register0(Default Value: 0x0000_0000)**

Offset: 0x00F8			Register Name: TVE_0F8_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	DETECT_PULSE_VALUE Use for DAC data input at auto detect pluse. Set the pulse amplitude.

7.5.6.22. **TV Encoder Auto Detection Configuration Register1(Default Value: 0x0000_0000)**

Offset: 0x00FC			Register Name: TVE_0FC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R/W	0x0	DETECT_PULSE_PERIODS Use 32K clock
15	/	/	/
14:0	R/W	0x0	DETECT_PULSE_START Detect signal start time

7.5.6.23. **TV Encoder Color Burst Phase Reset Configuration Register (Default Value: 0x0000_0001)**

Offset: 0x0100			Register Name: TVE_100_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	COLOR_PHASE_RESET Color burst phase period selection These bits select the number of fields or lines after which the color burst phase is reset to its initial value as specified by the ChromaPhase parameter, This parameter is application only for interlaced video. 00: 8 field 01: 4 field 10: 2 lines

Offset: 0x0100			Register Name: TVE_100_REG
Bit	Read/Write	Default/Hex	Description
			11: only once

7.5.6.24. **TV Encoder VSYNC Number Register (Default Value: 0x0000_0000)**

Offset: 0x0104			Register Name: TVE_104_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	VSync5 Number of equalization pulse selection This bit selects whether the number of equalization pulses is 5 or 6. This parameter is applicable only for interlaced video. 0: 5 equalization pulse(default) 1: 6 equalization pulses

7.5.6.25. **TV Encoder Notch Filter Frequency Register (Default Value: 0x0000_0002)**

Offset: 0x0108			Register Name: TVE_108_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x2	NOTCH_FREQ Luma notch filter center frequency selection These bits select the luma notch filter (which is a band-reject filter) center frequency. In two of the selections, the filter width affects also the selection of the center frequency. 000: 1.1875 001: 1.1406 010: 1.0938 when notch_wide value is B‘1’ (this selection is proper for CCIR-NTSC), or 1.0000 when notch_wide value is B‘0’ 011: 0.9922. This selection is proper for NTSC with square pixels 100: 0.9531. This selection is proper for PAL with square pixel 101: 0.8359 when notch_wide value is B‘1’ (this selection is proper for CCIR-PAL), or 0.7734 when notch_wide value is B‘0’ 110: 0.7813 111: 0.7188

7.5.6.26. **TV Encoder Cb/Cr Level/Gain Register (Default Value: 0x0000_004F)**

Offset: 0x010C			Register Name: TVE_10C_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	Cr_Burst_Level

Offset: 0x010C			Register Name: TVE_10C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Specify the amplitude of the Cr burst. 8 bit 2's complement integer. Allowed range is (-127) to 127. Default value is 0.
7:0	R/W	0x4f	Cb_Burst_Level Specify the amplitude of the Cb burst. 8 bit 2's complement integer. Allowed range is (-127) to 127. Default value is 60.

7.5.6.27. **TV Encoder Tint and Color Burst Phase Register (Default Value: 0x0000_0000)**

Offset: 0x0110			Register Name: TVE_110_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	TINT Specify the tint adjustment of the chroma signal for CVBS and Y/C outputs. The adjustment is effected by setting the sub-carrier phase to the value of this parameter. 8.8 bit unsigned fraction. Units are cycles of the color burst frequency. Default value is 0.
15:8	/	/	/
7:0	R/W	0x0	CHROMA_PHASE Specify the color burst initial phase (*ChromaPhase)*. 8.8 bit unsigned fraction. Units are cycles of the color burst frequency. Default value is X'00'. The color burst is set to this phase at the first *HSYNC* and then reset to the same value at further *HSYNC*s as specified by the *CPhaseRset* bits of the *EncConfig5* parameter (see above)

7.5.6.28. **TV Encoder Burst Width Register (Default Value: 0x0016_447E)**

Offset: 0x0114			Register Name: TVE_114_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	BACK_PORCH Breezeway like in HD mode VSync 720p mode, is 220 2080i/p mode is 88(default)
23	/	/	/
22:16	R/W	0x16	BREEZEWAY Must be even. Specify the width of the breezeway in encoder clock cycles. 5 bit unsigned integer. Allowed range is 0 to 31. Default value is 22. In 1080i mode, is 44 In 1080p mode, is 44 In 720p mode,is 40
15	/	/	/
14:8	R/W	0x44	BURST_WIDTH

Offset: 0x0114			Register Name: TVE_114_REG
Bit	Read/Write	Default/Hex	Description
			Specify the width of the color frequency burst in encoder clock cycles. 7 bit unsigned integer. Allowed range is 0 to 127. Default value is 68. In hd mode, ignored
7:0	R/W	0x7e	HSYNC_WIDTH Specify the width of the horizontal sync pulse in encoder clock cycles. Min value is 16. Max value is (*FrontPorch + ActiveLine - BackPorch*). Default value is 126. The sum of *HSyncSize* and *BackPorch* is restricted to be divisible by 4. In 720p mode, is 40 In 1080i/p mode, is 44

7.5.6.29. TV Encoder Cb/Cr Gain Register (Default Value: 0x0000_A0A0)

Offset: 0x0118			Register Name: TVE_118_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0xa0	CR_GAIN Specify the Cr color gain. 8 bit unsigned fraction. Default value is 139.
7:0	R/W	0xa0	CB_GAIN Specify the Cb color gain. 8 bit unsigned fraction. Default value is 139.

7.5.6.30. TV Encoder Sync and VBI Level Register (Default Value: 0x0010_00F0)

Offset: 0x011C			Register Name: TVE_11C_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x10	SYNC_LEVEL Specify the sync pulse level setting. 8 bit unsigned integer. Allowed range is 0 to *ABlankLevel*-1 or *VBlankLevel*-1 (whichever is smaller).
15:10	/	/	/
9:0	R/W	0xf0	VBLANK_LEVEL Specify the blank level setting for non active lines. 10 bit unsigned integer. Allow range 0 to 1023.

7.5.6.31. TV Encoder White Level Register (Default Value: 0x01E8_0320)

Offset: 0x0120			Register Name: TVE_120_REG
Bit	Read/Write	Default/Hex	Description
31::26	/	/	/
25:16	R/W	0x1e8	HD_SYNC_BREEZEWAY_LEVEL Specify the breezeway level setting. 10 bit unsigned integer. Allowed range is 0 to 1023. Default value is 488.

Offset: 0x0120			Register Name: TVE_120_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:10	/	/	/
9:0	R/W	0x320	WHITE_LEVEL Specify the white level setting. 10 bit unsigned integer. Allowed range is black_level+1 or vbi_blank_level +1 (whichever is greater) to 1023. Default value is 800.

7.5.6.32. **TV Encoder Video Active Line Register (Default Value: 0x0000_05A0)**

Offset: 0x0124			Register Name: TVE_124_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x5A0	ACTIVE_LINE Specify the width of the video line in encoder clock cycles. 12 bit unsigned multiple of 4 integer. Allowed range is 0 to 4092 Default value is 1440.

7.5.6.33. **TV Encoder Video Chroma BW and CompGain Register (Default Value: 0x0000_0000)**

Offset: 0x0128			Register Name: TVE_128_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x0	CHROMA_BW Chroma filter bandwidth selection This bit specifies whether the bandwidth of the chroma filter is: 00: Narrow width 0.6MHz 01: Wide width 1.2MHz. 10: Extra width 1.8MHz 11: Ultra width 2.5MHz Default is 0.6MHz(value 0)
15:2	/	/	/
1:0	R/W	0x0	COMP_CH_GAIN Chroma gain selection for the composite video signal. These bits specify the gain of the chroma signal for composing with the luma signal to generate the composite video signal: 00: 100% 01: 25% 10: 50% 11: 75%

7.5.6.34. TV Encoder Register (Default Value: 0x0000_0101)

Offset: 0x012C			Register Name: TVE_12C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x1	NOTCH_WIDTH Luma notch filter width selection This bit selects the luma notch filter (which is a band-reject filter) width. 0: Narrow 1: Wide
7:1	/	/	/
0	R/W	0x1	COMP_YUV_EN This bit selects if the components video output are the RGB components or the YUV components. 0: The three component outputs are the RGB components. 1: The three component outputs are the YUV components, (i.e. the color conversion unit is by-passed)

7.5.6.35. TV Encoder Re-sync Parameters Register (Default Value: 0x0010_0001)

Offset: 0x0130			Register Name: TVE_130_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RE_SYNC_FIELD Re-sync field
30	R/W	0x0	RE_SYNC_DIS 0: Re-Sync Enable 1: Re-Sync Disable
29:27	/	/	/
26:16	R/W	0x10	RE_SYNC_LINE_NUM Re-sync line number from TCON
15:11	/	/	/
10:0	R/W	0x1	RE_SYNC_PIXEL_NUM Re-sync line pixel from TCON

7.5.6.36. TV Encoder Slave Parameter Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: TVE_134_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	SLAVE_THRESH Horizontal line adjustment threshold selection This bit selects whether the number of lines after which the Video Encoder starts the horizontal line length adjustment is slave mode is 0 or 30. 0: Number of lines is 0

Offset: 0x0134			Register Name: TVE_134_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Number of lines is 30
7:1	/	/	/
0	R/W	0x0	SLAVE_MODE Slave mode selection This bit selects whether the Video Encoder is sync slave, partial slave or sync master. It should be set to B‘0’. 0: The Video Encoder is not a full sync slave (i.e. it is a partial sync slave or a sync master) 1: Reserved

7.5.6.37. **TV Encoder Configuration Register (Default Value: 0x0000_0000)**

Offset: 0x0138			Register Name: TVE_138_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	INVERT_TOP Field parity input signal (top_field) polarity selection. This bit selects whether the top field is indicated by a high level of the field parity signal or by the low level. The bit is applicable both when the Video Encoder is the sync master and when the Video Encoder is the sync slave. 0: Top field is indicated by low level 1: Top field is indicated by high level
7:1	/	/	/
0	R/W	0x0	UV_ORDER This bit selects if the sample order at the chroma input to the Video Encoder is Cb first (i.e. Cb 0 Cr 0 Cb 1 Cr 1) or Cr first (i.e. Cr 0 Cb 0 Cr 1 Cb 1). 0: The chroma sample input order is Cb first 1: The chroma sample input order is Cr first

7.5.6.38. **TV Encoder Configuration Register (Default Value: 0x0000_0001)**

Offset: 0x013C			Register Name: TVE_13C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	RGB_SYNC R, G and B signals sync embedding selection. These bits specify whether the sync signal is added to each of the R, G and B components (B‘1’) or not (B‘0’). Bit [26] specify if the R signal have embedded syncs, bit [25] specify if the G signal have embedded syncs and bit [24] specify if the B signal have embedded syncs. When comp_yuv is equal to B‘1’, these bits are N.A. and should be set to B‘000’. When the value is different from B‘000’, **RGB_SETUP** should be set to B‘1’.

Offset: 0x013C			Register Name: TVE_13C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
23:17	/	/	/
16	R/W	0x0	RGB_SETUP “Set-up” enable for RGB outputs. This bit specifies if the “set-up” implied value (black_level – blank_level) specified for the CVBS signal is used also for the RGB signals. 0: The “set-up” is not used, or N.A. i.e. comp_yuv is equal to B‘1’. 1: The implied “set-up” is used for the RGB signals
15:1	/	/	/
0	R/W	0x1	BYPASS_YCLAMP Y input clamping selection This bit selects whether the Video Encoder Y input is clamped to 64 to 940 or not. When not clamped the expected range is 0 to 1023. The U and V inputs are always clamped to the range 64 to 960. 0: The Video Encoder Y input is clamped 1: The Video Encoder Y input is not clamped

7.5.6.39. **TV Encoder Low Pass Control Register(Default Value: 0x0000_0000)**

Offset: 0x0380			Register Name: TVE_380_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:10	R/W	0x0	USER_DEFLICKER_COEF up : coef/32 Center :1-coef/16 Down :coef/32
9	R/W	0x0	FIX_COEF_DEFLICKER 0: Auto deflicker 1: User deflicker
8	R/W	0x0	ENABLE_DEFLICKER 0: Disable deflicker 1: Enable deflicker
7:1	/	/	/
0	R/W	0x0	EN LP function enable 0: Disable 1: Enable

7.5.6.40. **TV Encoder Low Pass Filter Control Register(Default Value: 0x0000_0000)**

Offset: 0x0384			Register Name: TVE_384_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/

Offset: 0x0384			Register Name: TVE_384_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
21:16	R/W	0x0	HP_RATIO Default high-pass filter ratio In two complement,the range is from -31 to 31.
15:14	/	/	/
13:8	R/W	0x0	BP0_RATIO Default band-pass filter0 ratio In two complement,the range is from -31 to 31.
7:6	/	/	/
5:0	R/W	0x0	BP1_RATIO Default band-pass filter1 ratio In two complement,the range is from -31 to 31.

7.5.6.41. **TV Encoder Low Pass Gain Register(Default Value: 0x0000_0000)**

Offset: 0x0388			Register Name: TVE_388_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	GAIN Peaking gain setting.

7.5.6.42. **TV Encoder Low Pass Gain Control Register(Default Value: 0x0000_0000)**

Offset: 0x038C			Register Name: TVE_38C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	DIF_UP Gain control: limitation threshold.
15:8	/	/	/
4:0	R/W	0x0	BETA Gain control: large gain limitation.

7.5.6.43. **TV Encoder Low Pass Shoot Control Register(Default Value: 0x0000_0000)**

Offset: 0x0390			Register Name: TVE_390_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R/W	0x0	NEG_GAIN Undershoot gain control.

7.5.6.44. **TV Encoder Low Pass Coring Register(Default Value: 0x0000_0000)**

Offset: 0x0394			Register Name: TVE_394_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CORTHR Coring threshold.

7.5.6.45. **TV Encoder Noise Reduction Register(Default Value: 0x0000_0000)**

Offset: 0x03A0			Register Name: TVE_3A0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	T_Value
15:1	/	/	/
0	R/W	0x0	EN

7.6. VDPO

7.6.1. Overview

The video data parallel output(VDPO) is a parallel digital video output interface that compatible with ITU-R BT.656/1120 protocol. It transfers video data in YUV422 up to full-HD format.It works in two mode, 16-bit data output with one Y-channel and one C-channel or 8-bit data output with one multiplexed channel.

The VDPO includes the following features:

- Supports 16-bit parallel video data output up to full-HD
- Supports 8-bit parallel video data output up to HD, like BT.656 or BT.1120
- Supports embedded H.V.F sync or separate H.V.F sync
- YCbCr4:4:4 to YCbCr4:2:2 horizontal chrominance down-sampling with FIR
- 3V or 1.8V selectable IO power supply

7.6.2. Block Diagram

Figure 7-21 shows the block diagram of the VDPO.

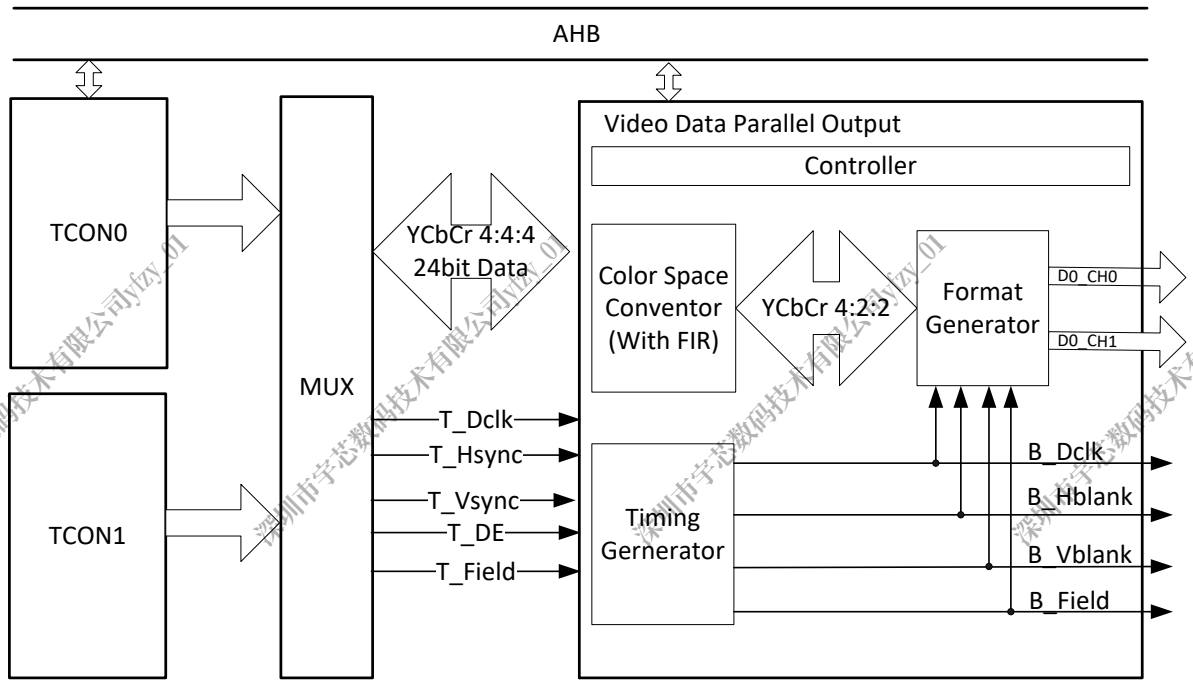


Figure 7-21. VDPO Block Diagram

7.6.3. Operations and Functional Descriptions

7.6.3.1. External Signals

Table 7-12 describes the external signals of VDPO.

Table 7-12. VDPO External Signals

Pin Name	Function Description	Type
VO_D0	Output Data0	O
VO_D1	Output Data1	O
VO_D2	Output Data2	O
VO_D3	Output Data3	O
VO_D4	Output Data4	O
VO_D5	Output Data5	O
VO_D6	Output Data6	O
VO_D7	Output Data7	O
VO_D8	Output Data8	O
VO_D9	Output Data9	O
VO_D10	Output Data10	O
VO_D11	Output Data11	O
VO_D12	Output Data12	O
VO_D13	Output Data13	O
VO_D14	Output Data14	O
VO_D15	Output Data15	O
VO_CLK	Output Clock	O
VO_HSYNC	Output Horizontal Blanking	O
VO_VSYNC	Output Vertical Blanking	O
VO_FIELD	Output Field Signal	O

7.6.3.2. Clock Sources

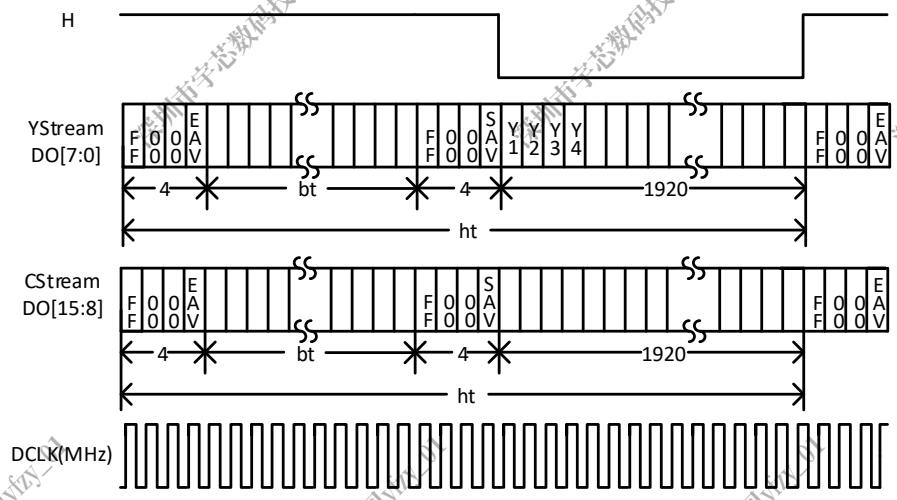
Table 7-13. VDPO Clock Sources

Clock Sources	Description
TCON SCLK	Source CLK from TCON

7.6.3.3. Typical Output Data Timing Format

7.6.3.3.1. 1080P @60/50/30/24 Hz

Horizontal timing(16-bit mode):



Frame Freq	ht(DCLK)	DCLK(MHz)
60P	2200	148.5
50P	2640	148.5
30P	2200	74.25
24P	2750	74.25

Figure 7-22. BT.1120 60/50/30/24P Horizontal Timing Diagram

Vertical timing:

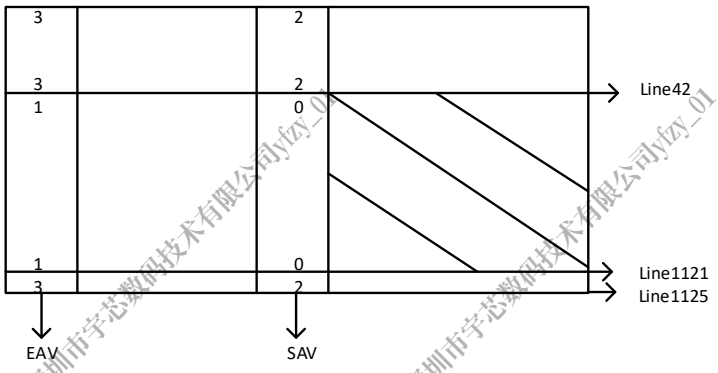
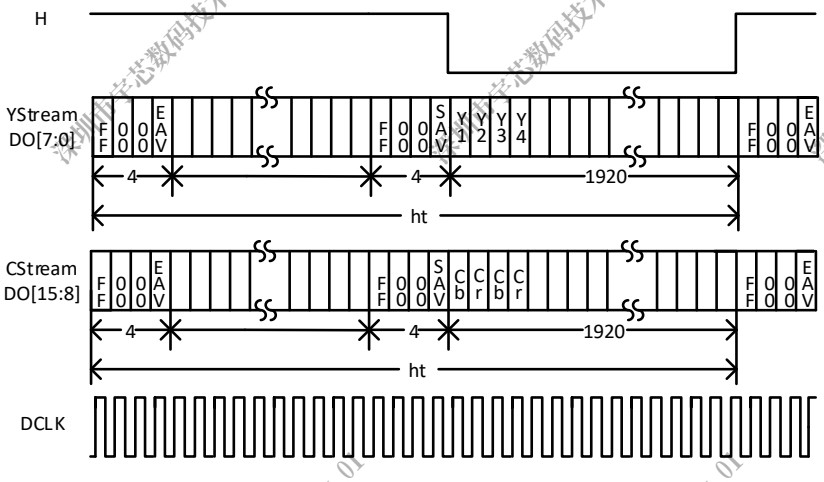


Figure 7-23. BT.1120 1080P Vertical Timing Diagram

7.6.3.3.2. 1080I @60/50 Hz

Horizontal timing(16-bit mode):



Frame Freq	ht(DCLK)	DCLK(MHz)
60I	2200	74.25
50I	2640	74.25

Figure 7-24. BT.1120 60/50I Horizontal Timing Diagram

Vertical timing:

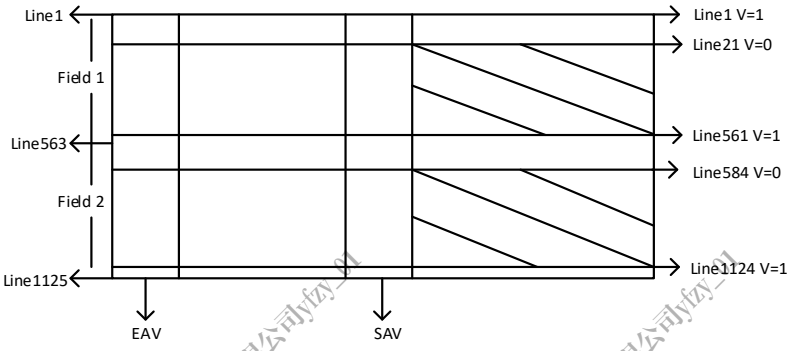
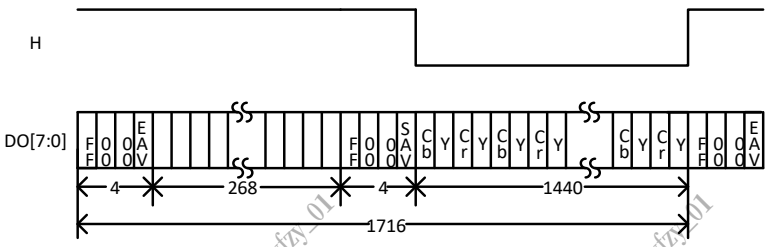


Figure 7-25. BT.1120 60/50I Vertical Timing Diagram

7.6.3.3.3. 525line @59.94Hz(BT.656)

Horizontal timing(8-bit mode):



Frame Freq	DCLK(MHz)
60I	27

Figure 7-26. BT.656 525line Horizontal Timing Diagram

Vertical timing:

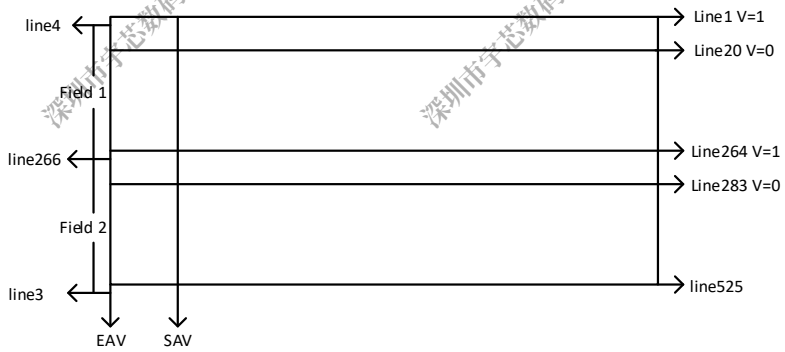
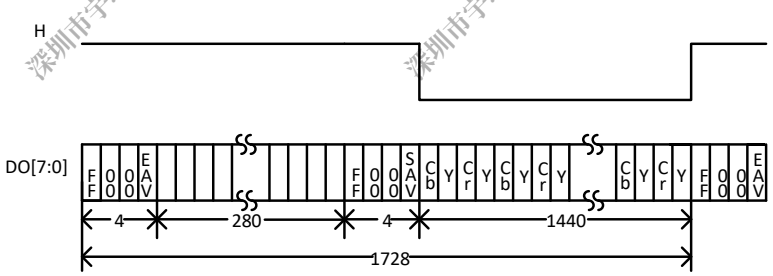


Figure 7-27. BT.656 525line Vertical Timing Diagram

7.6.3.3.4. 625line @50Hz(BT.656)

Horizontal timing(8-bit mode):



Frame Freq	DCLK(MHz)
50I	27

Figure 7-28. BT.656 625line Horizontal Timing Diagram

Vertical timing:

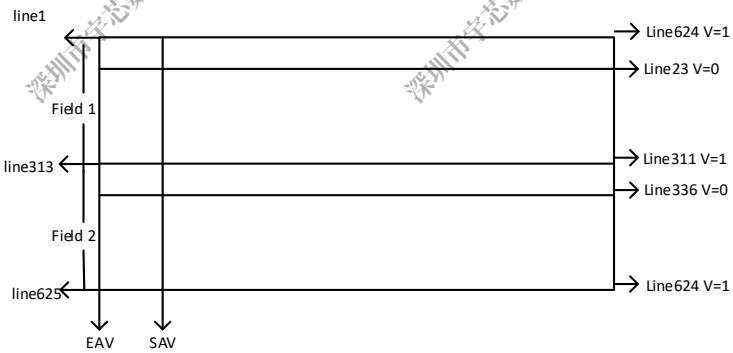
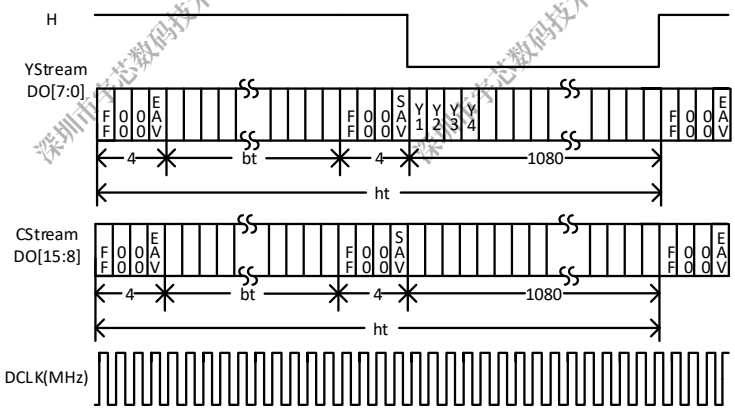


Figure 7-29. BT.656 625line Vertical Timing Diagram

7.6.3.3.5. 720P @60/50/30/24Hz

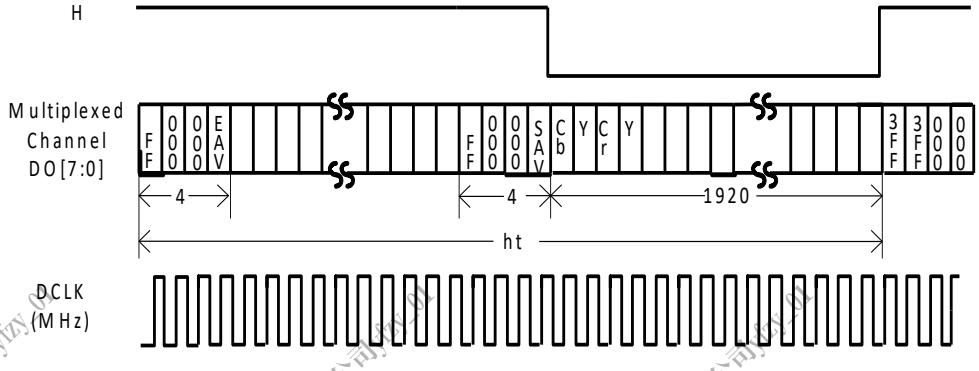
Horizontal timing(16-bit mode):



Frame Freq	ht(DCLK)	DCLK(MHz)
60P		37.125
50P		37.125

Figure 7-30. 720P YC Channel Mode(16-bit) Horizontal Timing Diagram

Horizontal timing(8-bit mode):



Frame Freq	ht(DCLK)	DCLK(MHz)
60P		74.25
50P		74.25

Figure 7-31. 720P YC Channel Mode(8-bit) Horizontal Timing Diagram

Vertical timing:

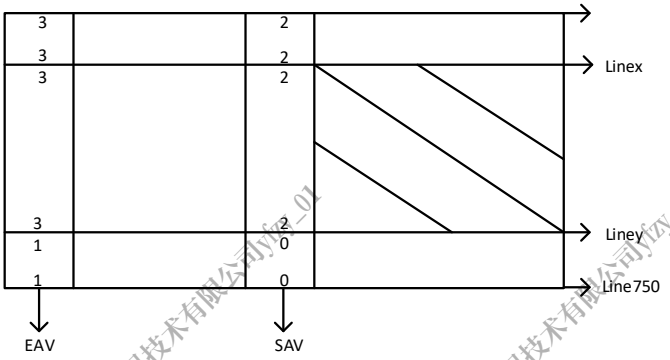


Figure 7-32. 720P Vertical Timing Diagram

7.6.3.4. BT.656 or BT.1120 SYNC Signal

In BT.656 or BT.1120, in every line, the active video data start right after a 4-byte sync signal(SAV) and finish with a 4-byte sync signal after the active video data (EAV), the definition of 4-byte sync signal data is shown below.

MSB	SAV/EAV bit status			Protection bit				Discarded in 8 bit mode	
Bit9	Bit 8(F)	Bit 7(V)	Bit 6(H)	Bit 5(P3)	Bit 4(P3)	Bit 3(P3)	Bit 2(P3)	Bit 1	Bit 0
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	0	0
1	0	1	0	1	0	1	1	0	0
1	0	1	1	0	1	1	0	0	0
1	1	0	0	0	1	1	1	0	0
1	1	0	1	1	0	1	0	0	0
1	1	1	0	1	1	0	0	0	0
1	1	1	1	0	0	0	1	0	0

NOTE

F: Field signal

V: Vertical blanking signal

H: Horizontal blanking signal

P3: P3= V⊕H

P2: P3= F⊕H

P1: P3= F⊕V

P0: P3= F⊕V⊕H

7.6.3.5. Horizontal Chrominance Down-Sampling and Video Data Clamp

7.6.3.5.1. YCbCr4:4:4 to YCbCr4:2:2 Horizontal Chrominance Down-Sampling

In this conversion, horizontal resolution of Cb and Cr component will be down-sampled by 2.

A 8-taps FIR filter will be applied to the input data:

For each line, Cb and Cr are filtered and down-sampled by 2 in horizontal direction like this:

```
yuv422_width = width >> 1;
for (i = 0;i < yuv422_width; i++) {
    j = i << 1;
    filtered(i) = (in(j-3)*HCOEF[0] + in(j-2)*HCOEF[1] + in(j-1)*HCOEF[2] + in(j)*HCOEF[3] +
    in(j+1)*HCOEF[4] + in(j+2)*HCOEF[5] + in(j+3)*HCOEF[6] + in(j+4)*HCOEF[7] + 0x20) >> 6;
```

NOTE

If (j-n)<0, in(j-n)=in(0), n can be 3/2/1.

If (j+n)> (width-1), in(j+n)=in(width-1), n can be 3/2/1.

Cb and Cr can be selected different COEF_SEL type.

Table 7-14. HCOEF according to Pixel Format Type

COEF_SEL TYPE	HCOEF							
	[0]	[1]	[2]	[3]	[4]	[5]	[6]	[7]
0	-2	0	18	32	18	0	-2	0
1	0	-2	0	18	32	18	0	-2
2	0	-2	7	27	27	7	-2	0
3	0	0	-2	7	27	27	7	-2
4	0	0	0	64	0	0	0	0
5	0	0	0	0	64	0	0	0
6	0	0	0	32	32	0	0	0
7	0	0	0	0	32	32	0	0

7.6.3.5.2. Video Data Clamp

Video data Clamp module is behind horizontal chrominance down-sampling module, the YCbCr422 video data can be clamp like below:

```
if(video_val<lowlimit)
        return lowlimit;
else if(video_val >uplimit)
        return uplimit;
else
    return val;
```

Y, Cb, Cr can be selected different lowlimit and uplimit.

7.6.3.6. Blanking Data

The data words occurring during digital blanking intervals that are not used for the timing reference codes (SAV and EAV), line number data, the error detection codes or ancillary data (ANC) are filled with words corresponding to the following blanking levels, appropriately placed in the multiplexed data:

- 16(8) for Y signals
- 128(8) for CB ,CR

7.6.4. Register List

Module Name	Base Address
VDPO	0x06542000

Register Name	Offset	Description
MODULE_CTRL_REG	0x0000	Module Control Register
FMT_CTRL_REG	0x0004	Output Data Format Control Register
SYNC_CTRL_REG	0x0008	Sync Signal Control Register
INT_CTRL_REG	0x000C	Interrupt Control Register
LINE_INT_NUM_REG	0x0010	Line Match Interrupt Register
DEUBG_STATUS_REG	0x0014	Debug Status Register
HOR_CHROMA_SPL _REG	0x0018	Horizontal Chrominance Dowm-sampling Control Register
CLAMP_CTRL_REG0	0x001C	Clamp Control Register0
CLAMP_CTRL_REG1	0x0020	Clamp Control Register1
CLAMP_CTRL_REG2	0x0024	Clamp Control Register2
H_TIMING_REG0	0x0028	Horizontal Timing Control Register0
VTIMING_REG0	0x002C	Vertical Timing Control Register0
VTIMING_REG1	0x0030	Vertical Timing Control Register1

7.6.5. Register Description

7.6.5.1. Module Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: MODULE_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	SEPARATE_SYNC_EN 0: Disable 1: Enable
0	R/W	0x0	VDPO_MODULE_EN 0: Disable 1: Enable

7.6.5.2. Output Data Format Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: FMT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	DATA_SEQ_SEL 00: Cb->Y->Cr->Y 01: Cr->Y->Cb->Y 10: Y->Cb->Y->Cr 11: Y->Cr->Y->Cb In dual data channel mode(Output_Data_Width=1), If output sequence is A->B->C->D, then D15-D8: A->C D7-D0: B->D In one data channel mode(Output_Data_Width=0),

			If output sequence is A->B->C->D, then D7-D0: A->B->C->D
7:5	/	/	/
4	R/W	0x0	EMBEDDED_SYNC_FMT 0: BT.1120 like 1: BT.656 like When the bit is 0,if data output width is 16-bit, the format is: C channel: FF,000,000,EAV,XXX……XX, XFF,000,000,SAV Y channel: FF,000,000,EAV,XXX……XX,XFF,000,000,SAV When the bit is 0,if data output width is 8-bit, the format is: FF FF 000 000 EAV EAV XXX……XX XF FFF 000 000 SAV SAV When the bit is 1,if data output width is 16-bit, the format is: C channel: FF 000 XXX……XX XFF 000 Y channel: 00 EAV XXX……XX 000 SAV When the bit is 1,if data output width is 8-bit, the format is: Multiplexed channel: FF 000 000 EAV XXX……XX XFF 000 000 SAV
3:2	/	/	/
1	R/W	0x0	PROG_INTL_MODE 0: Progress 1: Interlace
0	R/W	0x0	OUTPUT_DATA_WIDTH 0: 8-bit data output(one Y channel) 1: 16-bit data output(one Y channel +one C channel)

7.6.5.3. **Sync Signal Control Register(Default Value: 0x0000_0003)**

Offset: 0x0008			**Register Name: SYNC_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	DCLK_DLY_EN 0: Disable 1: Enable
9:4	R/W	0x0	DCLK_DLY_NUM Number= bit[9:4]+1
3	R/W	0x0	DCLK_INVERT 0: Disable dclk invert 1: Enable dclk invert
2	R/W	0x0	FIELD_POL 0: 0 respects field 1, 1 respects field 2. 1: 0 respects field 2, 1 respects field 1.
1	R/W	0x1	V_BLANK_POL 0: 0 respects blanking, 1 respects active. 1: 1 respects blanking, 0 respects active.
0	R/W	0x1	H_BLANK_POL

			0: 0 respects blanking, 1 respects active. 1: 1 respects blanking, 0 respects active.

7.6.5.4. **Interrupt Control Register(Default Value: 0x0000_0000)**

Offset: 0x000C			Register Name: INT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/WOC	0x0	VB_INT_FLAG Trigger when vertical blanking signal assert Write 0 to clear it.
16	R/WOC	0x0	LINE_MATCH_INT_FLAG Trigger when current scan line number match the line number in INT_LINE_NUM_REG. Write 0 to clear it.
15:2	/	/	/
1	R/W	0x0	VB_INT_EN 0: Disable 1: Enable
0	R/W	0x0	LINE_MATCH_INT_EN 0: Disable 1: Enable

7.6.5.5. **Line Match Interrupt Register(Default Value: 0x0000_0FFF)**

Offset: 0x0010			Register Name: LINE_INT_NUM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0xFFF	INT_LINE_NUM(including inactive line) Can be written only scan line match interrupt disable

7.6.5.6. **Debug Status Register(Default Value: 0x0001_0000)**

Offset: 0x0014			Register Name: DEUBG_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	0x1	FIELD_POL_STA 0: Even field in interlace mode 1: Odd field in interlace mode This bit always is 0 in progress mode.
15:13	/	/	/
12:0	R	0x0	CURRENT _LINE

7.6.5.7. **Horizontal Chrominance Dowm-sampling Control Register(Default Value: 0x0000_0000)**

Offset: 0x0018			Register Name: HOR_CHROMA_SPL _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	CR_HOR_SPL_TYPE
3	/	/	/
2:0	R/W	0x0	CB_HOR_SPL_TYPE

7.6.5.8. **Clamp Control Register0(Default Value: 0x00FF_0000)**

Offset: 0x001C			Register Name: CLAMP_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0xFF	Y_VAL_RANGE_MAX
15:8	/	/	/
7:0	R/W	0x0	Y_VAL_RANGE_MIN

7.6.5.9. **Clamp Control Register1(Default Value: 0x00FF_0000)**

Offset: 0x0020			Register Name: CLAMP_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0xFF	CB_VAL_RANGE_MAX
15:8	/	/	/
7:0	R/W	0x0	CB_VAL_RANGE_MIN

7.6.5.10. **Clamp Control Register2(Default Value: 0x00FF_0000)**

Offset: 0x0024			Register Name: CLAMP_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0xFF	CR_VAL_RANGE_MAX
15:8	/	/	/
7:0	R/W	0x0	CR_VAL_RANGE_MIN

7.6.5.11. **Horizontal Timing Control Register0(Default Value: 0x0000_0000)**

Offset: 0x0028			Register Name: H_TIMING_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

27:16	R/W	0x0	H_ACTIVE
15:12	/	/	/
11:0	R/W	0x0	H_BP

7.6.5.12. **Vertical Timing Control Register0(Default Value: 0x0000_0000)**

Offset: 0x002C			**Register Name: V_TIMING_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	V_ACTIVE
15:12	/	/	/
11:0	R/W	0x0	V_BP

7.6.5.13. **Vertical Timing Control Register1(Default Value: 0x0000_0000)**

Offset: 0x0030			**Register Name: V_TIMING_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	INTERLACE_MODE_OPTION Only valid in interlace mode , If V_Total is odd number: 1: Field 1 has more 1 line then field 0, the line adds to field 0 vbp. BT656 like 0: Field 0 has more 1 line then field 1, the line adds to field 0 vfp. BT1120 like
15:13	/	/	/
12:0	R/W	0x0	V_TOTAL Same as TCON parameter “vt”.

Chapter 8 Video Input Interfaces

8.1. CSIC

8.1.1. Overview

The CMOS Sensor Interface Controller(CSIC) is an image or video input control module which can receive image or video data via digital camera(DC) interface, BT656 interface, BT601 interface, BT1120 interface, high speed serial interface like MIPI, sub-LVDS and HiSPI. The controller can transfer valid data to embedded ISP or store the data in memory directly. There are also two built-in Camera Control Interface(CCI) modules can be used for external device control.

The CSIC includes the following features:

- Supports 8/10/12/16 DC interface
- Supports BT656,BT601,BT1120 interface
- Supports ITU-R BT.656/BT1120 time-multiplexed format
- Supports MIPI, sub-LVDS, HiSPI interface timings
- Supports DDR sample mode
- Supports image crop function
- Maximum 1080p@30fps resolution for DVP/BT656 interface
- Maximum 1080p@60fps/4K@15fps resolution for BT1120 interface(Only for V536-H)
- Maximum pixel clock for parallel to 148.5MHz

CCI:

- Compatible with i2c transmission in 7 bit slave ID + 1 bit R/W
- Automatic transmission
- 0/8/16/32 bit register address supported
- 8/16/32 bit data supported
- 64bytes-FIFO input CCI data supported
- Synchronized with CSI signal and delay trigger supported
- Repeated transmission with sync signal supported

8.1.2. Block Diagram

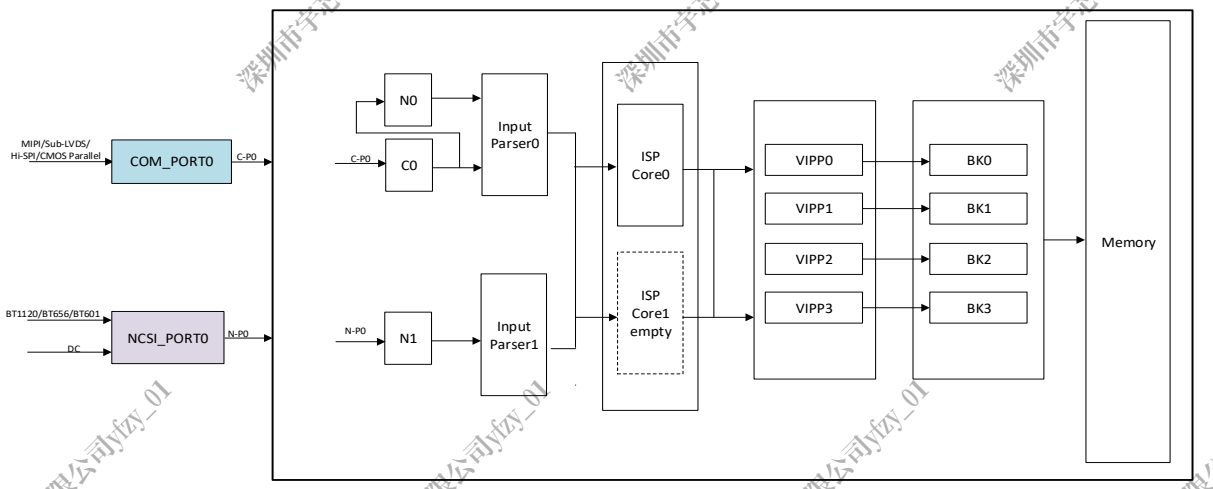


Figure 8-1. CSIC Block Diagram

The CSIC IP is consists of Input Parser, ISP, Video Input Post Process(VIPP) and DMA Control. In addition,the controller has 2 Input Parser, 1 ISP, 4 VIPP and 4 DMA.

Figure 8-2 shows block diagram of the CCI.

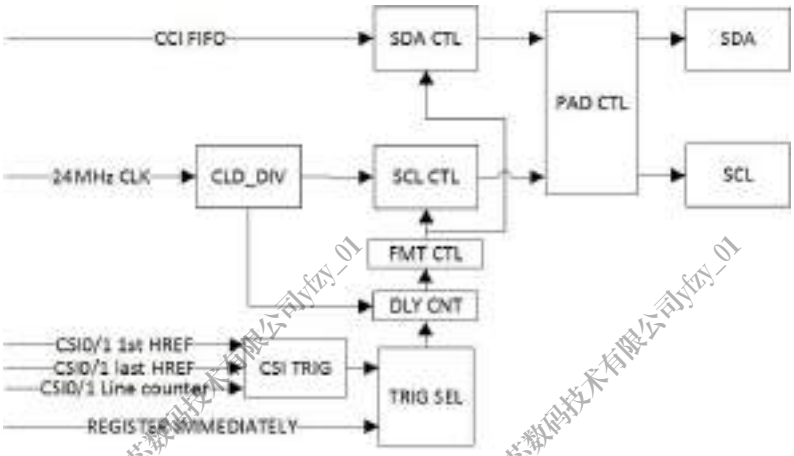


Figure 8-2. CCI Block Diagram

8.1.3. Operations and Functional Descriptions

8.1.3.1. External Signals

Table 8-1. CSIC External Signals

Pin Name	Function Description
Parallel CSI	
CSI_MASTERCLK1	Parallel CSI0 master clock
NCSI0_PCLK	Parallel CSI0 pixel clock
NCSI0_HSYNC	Parallel CSI0 horizontal Sync
NCSI0_VSYNC	Parallel CSI0 vertical Sync
CSI_CCI1_SCK	Parallel CSI0 CCI control clock

CSI_CCI1_SDA	Parallel CSI0 CCI control data
NCSI0_D0	Parallel CSI0 video input data0
NCSI0_D1	Parallel CSI0 video input data1
NCSI0_D2	Parallel CSI0 video input data2
NCSI0_D3	Parallel CSI0 video input data3
NCSI0_D4	Parallel CSI0 video input data4
NCSI0_D5	Parallel CSI0 video input data5
NCSI0_D6	Parallel CSI0 video input data6
NCSI0_D7	Parallel CSI0 video input data7
NCSI0_D8	Parallel CSI0 video input data8
NCSI0_D9	Parallel CSI0 video input data9
NCSI0_D10	Parallel CSI0 video input data10
NCSI0_D11	Parallel CSI0 video input data11
NCSI0_D12	Parallel CSI0 video input data12
NCSI0_D13	Parallel CSI0 video input data13
NCSI0_D14	Parallel CSI0 video input data14
NCSI0_D15	Parallel CSI0 video input data15
Combo CSI	
CSI_SM_VS	Combo slave mode vertical SYNC
CSI_SM_HS	Combo slave mode horizontal SYNC
CSI_MASTERCLK0	Combo master clock0
CSI_CCI0_SCK	Combo CCI control clock
CSI_CCI0_SDA	Combo CCI control data
CMBCSI0_A_CKP/CMB_CMOS0_PCLK	Combo CSI0 controller A clock positive/parallel CSI 0 pixel clock
CMBCSI0_A_CKN/CMB_CMOS0_FIELD	Combo CSI0 controller A clock negative/parallel CSI 0 field
CMBCSI0_A_D0P/CMB_CMOS0_HSYNC	Combo CSI0 controller A data channel 0 positive/parallel CSI0 horizontal sync
CMBCSI0_A_D0N/CMB_CMOS0_VSYNC	Combo CSI0 controller A data channel 0 negative/parallel CSI0 vertical sync
CMBCSI0_A_D1P/CMB_CMOS0_D0	Combo CSI0 controller A data channel 1 positive/parallel CSI0 data 0
CMBCSI0_A_D1N/CMB_CMOS0_D1	Combo CSI0 controller A data channel 1 negative/parallel CSI0 data 1
CMBCSI0_A_D2P/CMB_CMOS0_D2	Combo CSI0 controller A data channel 2 positive/parallel CSI0 data 2
CMBCSI0_A_D2N/CMB_CMOS0_D3	Combo CSI0 controller A data channel 2 negative/parallel CSI0 data 3
CMBCSI0_A_D3P/CMB_CMOS0_D4	Combo CSI0 controller A data channel 3 positive/parallel CSI0 data 4
CMBCSI0_A_D3N/CMB_CMOS0_D5	Combo CSI0 controller A data channel 3 negative/parallel CSI0 data 5
CMBCSI0_B_CKP/CMB_CMOS0_D6	Combo CSI0 controller B clock positive/parallel CSI0 data 6
CMBCSI0_B_CKN/CMB_CMOS0_D7	Combo CSI0 controller B clock negative/parallel CSI0 data 7
CMBCSI0_B_D0P/CMB_CMOS0_D8	Combo CSI0 controller B data channel 0 positive/parallel CSI0 data 8
CMBCSI0_B_D0N/CMB_CMOS0_D9	Combo CSI0 controller B data channel 0 negative/parallel CSI0 data 9
CMBCSI0_B_D1P/CMB_CMOS0_D10	Combo CSI0 controller B data channel 1 positive/parallel CSI0 data 10
CMBCSI0_B_D1N/CMB_CMOS0_D11	Combo CSI0 controller B data channel 1 negative/parallel CSI0 data 11
CMBCSI0_B_D2P/CMB_CMOS0_D12	Combo CSI0 controller B data channel 2 positive/parallel CSI0 data 12
CMBCSI0_B_D2N/CMB_CMOS0_D13	Combo CSI0 controller B data channel 2 negative/parallel CSI0 data 13
CMBCSI0_B_D3P/CMB_CMOS0_D14	Combo CSI0 controller B data channel 3 positive/parallel CSI0 data 14
CMBCSI0_B_D3N/CMB_CMOS0_D15	Combo CSI0 controller B data channel 3 negative/parallel CSI0 data 15

CMBCSI0_C_D0P	Combo CSI0 controller C data channel 0 positive
CMBCSI0_C_D0N	Combo CSI0 controller C data channel 0 negative
CMBCSI0_C_D1P	Combo CSI0 controller C data channel 1 positive
CMBCSI0_C_D1N	Combo CSI0 controller C data channel 1 negative

8.1.3.2. **Parallel CSI Mapping**

Table 8-2. Parallel CSI Mapping

Parallel CSI External Signals	8-bit DC Interface	10-bit DC Interface	12-bit DC Interface	16-bit DC Interface
NCSI0_D0	D0	D0	D0	Y0
NCSI0_D1	D1	D1	D1	Y1
NCSI0_D2	D2	D2	D2	Y2
NCSI0_D3	D3	D3	D3	Y3
NCSI0_D4	D4	D4	D4	Y4
NCSI0_D5	D5	D5	D5	Y5
NCSI0_D6	D6	D6	D6	Y6
NCSI0_D7	D7	D7	D7	Y7
NCSI0_D8	-	D8	D8	C0
NCSI0_D9	-	D9	D9	C1
NCSI0_D10	-	-	D10	C2
NCSI0_D11	-	-	D11	C3
NCSI0_D12	-	-	-	C4
NCSI0_D13	-	-	-	C5
NCSI0_D14	-	-	-	C6
NCSI0_D15	-	-	-	C7

8.1.3.3. **Typical Application**

The CSIC module has 2 input ports and 4 DMA, which means it can support 2 ports input and 4 video streams output to memory simultaneously at most. This make the applications very flexible.

The CSIC module supports following input case:

- 1 high speed serial inputs
- 1 parallel DC inputs
- 1 serial input + 1 parallel DC input
- 1 BT656/BT1120 input interleaved 4-channel
- 1 BT656 input interleaved 2-channel + 1 BT656 input interleaved 2-channel
- 1 BT1120 input interleaved 2-channel + 1 BT1120 input interleaved 2-channel

8.1.3.4. **CSIC FIFO Distribution**

Table 8-3. CSIC FIFO Distribution

Interface	YUYV422 Interleaved/Raw			MIPI Interface		
Input format	YUV422		Raw	YUV422		Raw
Output format	Planar	UV combined	Raw/RGB/PRGB	Planar	UV combined	Raw/RGB/PRGB
CH0_FIFO0	Y	Y	All pixels data	Y	Y	All pixels data
CH0_FIFO1	Cb (U)	CbCr (UV)	-	Cb (U)	CbCr (UV)	-
CH0_FIFO2	Cr (V)	-	-	Cr (V)	-	-

Table 8-4. CSIC FIFO Distribution(Continued)

Interface	BT656 Interface		BT1120 Interface	
Input format	YUV422		YUV422	
Output format	Planar	UV combined	Planar	UV combined
CH0_FIFO0	Y	Y	Y	Y
CH0_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH0_FIFO2	Cr (V)	-	Cr (V)	-
CH1_FIFO0	Y	Y	Y	Y
CH1_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH1_FIFO2	Cr (V)	-	Cr (V)	-
CH2_FIFO0	Y	Y	Y	Y
CH2_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH2_FIFO2	Cr (V)	-	Cr (V)	-
CH3_FIFO0	Y	Y	Y	Y
CH3_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH3_FIFO2	Cr (V)	-	Cr (V)	-

8.1.3.5. **Pixel Format Arrangement**

RAW-10:

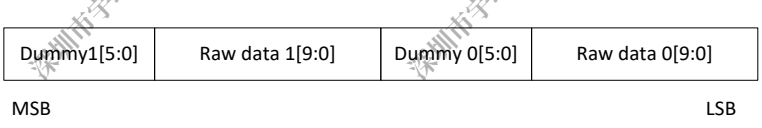


Figure 8-3. RAW-10 Format

RAW-12:

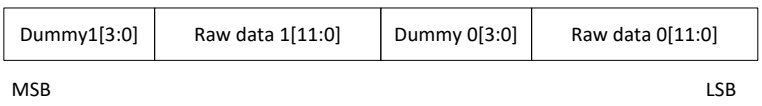


Figure 8-4. RAW-12 Format

YUV-10:

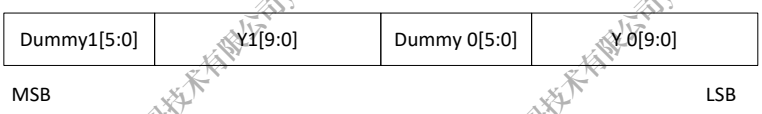


Figure 8-5. Y of YUV-10 Format

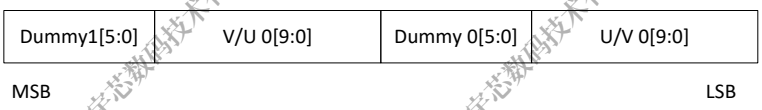


Figure 8-6. UV Combined of YUV-10 Format

RGB888:

B1[7:0]	R0[7:0]	G0[7:0]	B0[7:0]
G2[7:0]	B2[7:0]	R1[7:0]	G1[7:0]
R3[7:0]	G3[7:0]	B3[7:0]	R2[7:0]

MSB

Figure 8-7. RGB888 Format

PRGB888:

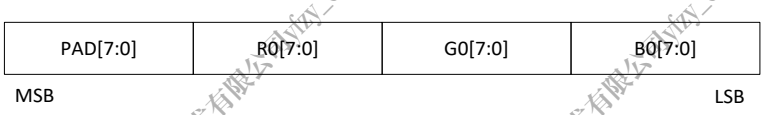


Figure 8-8. PRGB888 Format

RGB565:

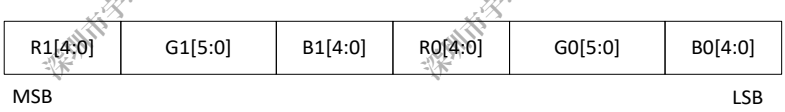


Figure 8-9. RGB565 Format

8.1.3.6. **Parallel CSI Timing**

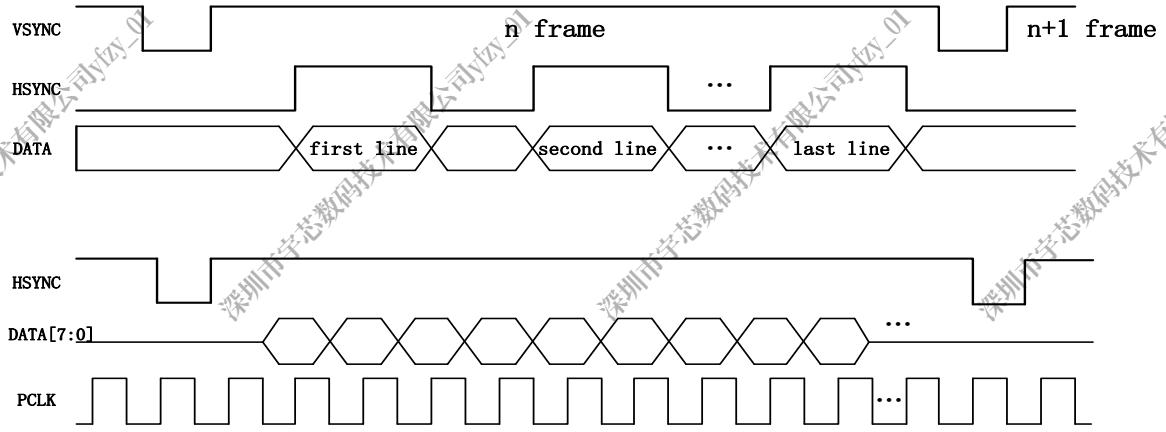


Figure 8-10. 8-bit CMOS Sensor Interface Timing

(clock rising edge sample.vsync valid = positive,hsycn valid = positive)

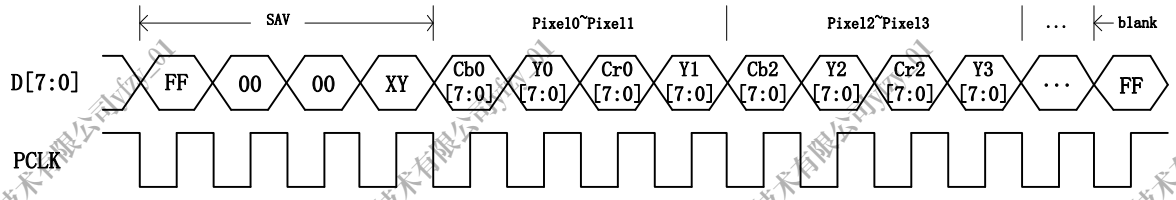


Figure 8-11. 8-bit YCbCr4:2:2 with Embedded Syncs(BT656) Timing

8.1.3.7. CCIR656 Head Code

Table 8-5 shows the header code of CCIR656.

Table 8-5. CCIR656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[7]	1	0	0	1
CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

Table 8-6 shows the Header Data Bit Definition of CCIR656.

Table 8-6. CCIR656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

8.1.3.8. Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.
For YUV422 format, pixel unit is a YU/YV combination.
For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
For Bayer and RAW format, pixel unit is a R/G/B single component.
For RGB565, pixel unit is 2 bytes of RGB565 package.
For RGB888, pixel unit is 3 bytes of RGB combination.

8.1.3.9. Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.
If horizontal flip is enabled, one or more pixels will be took as a unit:
For YUV format, a unit of $Y_0U_0Y_1V_1$ will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole.

So, a sequence of $Y_1U_0Y_0V_1$ will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

8.1.3.10. **Camera Communication Interface**

The CCI module supports master mode i2c-compatible single read and write access to camera and related devices.

It reads a series of packet from FIFO (accessed by registers) and transmit with the format defined in specific register(or packet data).

In compact mode, format register define the slave ID, R/W flag, register address width(0/8/16/32…bit), data width(8/16/32…bit) and access counter.

In complete mode, all data and format will be loaded from memory packet.

The access counter should be set to N(N> 0), and it will read N packets from FIFO. The total bytes should not exceed 64 for FIFO input mode.

Figure 8-12. R/W Sequence in Compact/Complete Mode

A packet is several bytes filled with register address and data(if in complete mode, slave id and width should be filled too) as the i2c access sequence defined. That is, the low address byte will be transmitted/received first. Bytes will be sent in write access, while some address will be written back with the data received in read access.

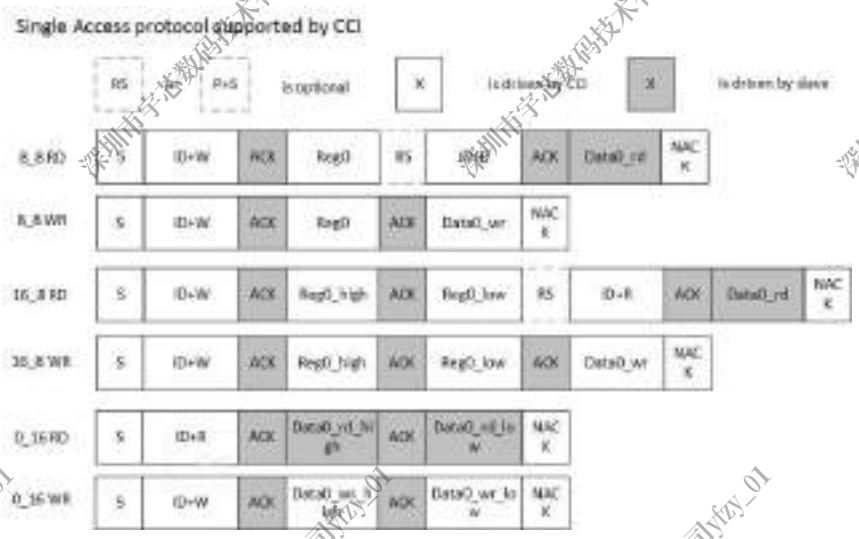


Figure 8-13. Single R/W Process of the CCI Protocol

After set the execution bit, the module will do the transmission automatically and return the result of success or fail. If any access fails, the whole transmission will be stopped and returned the number when it fails in the access counter.

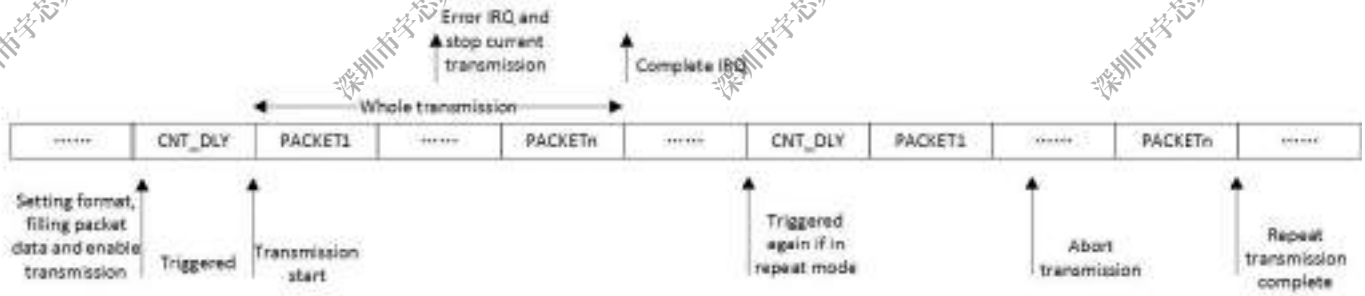


Figure 8-14. CCI Transmission Control

8.1.4. Register list

Module Name	Base Address
CSIC_BASE	0x06600000
CSIC_CCU	0x06600000
CSIC_TOP	0x06600800
CSIC_PARSER0	0x06601000
CSIC_PARSER1	0x06602000
CSIC_DMA0	0x06609000
CSIC_DMA1	0x06609200
CSIC_DMA2	0x06609400
CSIC_DMA3	0x06609600
CSIC_COMBO0	0x0660C000
CSIC_CCI0	0x06614000
CSIC_CCI1	0x06614400

CCU register list:

Register Name	Offset	Register name
CCU_CLK_MODE_REG	0x0000	CCU Clock Mode Register

CCU_PARSER_CLK_EN_REG	0x0004	CCU Parser Clock Enable Register
CCU_ISP_CLK_EN_REG	0x0008	CCU ISP Clock Enable Register
CCU_POST0_CLK_EN_REG	0x000C	CCU Post0 Clock Enable Register
CCU_POST1_CLK_EN_REG	0x0010	CCU Post1 Clock Enable Register

CSIC TOP register list:

Register Name	Offset	Register name
CSIC_TOP_EN_REG	0x0000	CSIC TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSIC Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSIC Pattern Control Register
/	0x000C~0x001C	Reserved
CSIC_PTN_LEN_REG	0x0020	CSIC Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSIC Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSIC Pattern ISP Size Register
CSIC_CONNECT_ENABLE_REG	0x002C	CSIC Connect enable Register
CSIC_ISP0_INPUT0_SEL_REG	0x0030	CSIC ISP0 Input0 Select Register
CSIC_ISP0_INPUT1_SEL_REG	0x0034	CSIC ISP0 Input1 Select Register
CSIC_ISP0_INPUT2_SEL_REG	0x0038	CSIC ISP0 Input2 Select Register
CSIC_ISP0_INPUT3_SEL_REG	0x003C	CSIC ISP0 Input3 Select Register
CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG	0x0070	CSIC ISP Bridge Buffer Maxuse Counter Clear Register
CSIC_ISP0_BRG_BUF_MAXUSE_CNT_REG	0x0074	CSIC ISP0 Bridge Buffer Maxuse Counter Register
/	0x0078~0x0080	Reserved
CSIC_ISP0_BRG_INT_EN_REG	0x0084	CSIC ISP0 Bridge Interrupt Enable Register
/	0x0088	Reserved
CSIC_ISP0_BRG_INT_PD_REG	0x008C	CSIC ISP0 Bridge Interrupt Pending Register
/	0x0090~0x009C	Reserved
CSIC_VIPP0_INPUT_SEL_REG	0x00A0	CSIC VIPP0 Input Select Register
CSIC_VIPP1_INPUT_SEL_REG	0x00A4	CSIC VIPP1 Input Select Register
CSIC_VIPP2_INPUT_SEL_REG	0x00A8	CSIC VIPP2 Input Select Register
CSIC_VIPP3_INPUT_SEL_REG	0x00A8	CSIC VIPP3 Input Select Register
CSIC_FEATURE_LIST_REG	0x00F0	CSIC Feature lis Register

PARSER 0/1 register list:

Register Name	Offset	Register name
PRS_EN_REG	0x0000	Parser Enable Register
PRS_NCSIC_IF_CFG_REG	0x0004	Parser NCSIC Interface Configuration Register
PRS_MCSIC_IF_CFG_REG	0x0008	Parser MCSIC Interface Configuration Register
PRS_CAP_REG	0x000C	Parser Capture Register
/	0x0018~0x0020	Reserved
PRS_C0_INFMT_REG	0x0024	Parser Channel_0 Input Format Register
PRS_C0_OUTPUT_HSIZE_REG	0x0028	Parser Channel_0 Output Horizontal Size Register

PRS_C0_OUTPUT_VSIZE_REG	0x002C	Parser Channel_0 Output Vertical Size Register
PRS_C0_INPUT_PARA0_REG	0x0030	Parser Channel_0 Input Parameter0 Register
PRS_C0_INPUT_PARA1_REG	0x0034	Parser Channel_0 Input Parameter1 Register
PRS_C0_INPUT_PARA2_REG	0x0038	Parser Channel_0 Input Parameter2 Register
PRS_C0_INPUT_PARA3_REG	0x003C	Parser Channel_0 Input Parameter3 Register
PRS_C0_INT_EN_REG	0x0040	Parser Channel_0 Interrupt Enable Register
PRS_C0_INT_STA_REG	0x0044	Parser Channel_0 Interrupt Status Register
PRS_CH0_LINE_TIME_REG	0x0048	Parser Channel_0 Line Time Register
/	0x004C~0x0120	Reserved
PRS_C1_INFMT_REG	0x0124	Parser Channel_1 Input Format Register
PRS_C1_OUTPUT_HSIZE_REG	0x0128	Parser Channel_1 Output Horizontal Size Register
PRS_C1_OUTPUT_VSIZE_REG	0x012C	Parser Channel_1 Output Vertical Size Register
PRS_C1_INPUT_PARA0_REG	0x0130	Parser Channel_1 Input Parameter0 Register
PRS_C1_INPUT_PARA1_REG	0x0134	Parser Channel_1 Input Parameter1 Register
PRS_C1_INPUT_PARA2_REG	0x0138	Parser Channel_1 Input Parameter2 Register
PRS_C1_INPUT_PARA3_REG	0x013C	Parser Channel_1 Input Parameter3 Register
PRS_C1_INT_EN_REG	0x0140	Parser Channel_1 Interrupt Enable Register
PRS_C1_INT_STA_REG	0x0144	Parser Channel_1 Interrupt Status Register
PRS_CH1_LINE_TIME_REG	0x0148	Parser Channel_1 Line Time Register
/	0x014C~0x0220	Reserved
PRS_C2_INFMT_REG	0x0224	Parser Channel_2 Input Format Register
PRS_C2_OUTPUT_HSIZE_REG	0x0228	Parser Channel_2 Output Horizontal Size Register
PRS_C2_OUTPUT_VSIZE_REG	0x022C	Parser Channel_2 Output Vertical Size Register
PRS_C2_INPUT_PARA0_REG	0x0230	Parser Channel_2 Input Parameter0 Register
PRS_C2_INPUT_PARA1_REG	0x0234	Parser Channel_2 Input Parameter1 Register
PRS_C2_INPUT_PARA2_REG	0x0238	Parser Channel_2 Input Parameter2 Register
PRS_C2_INPUT_PARA3_REG	0x023C	Parser Channel_2 Input Parameter3 Register
PRS_C2_INT_EN_REG	0x0240	Parser Channel_2 Interrupt Enable Register
PRS_C2_INT_STA_REG	0x0244	Parser Channel_2 Interrupt Status Register
PRS_CH2_LINE_TIME_REG	0x0248	Parser Channel_2 Line Time Register
/	0x024C~0x0320	Reserved
PRS_C3_INFMT_REG	0x0324	Parser Channel_3 Input Format Register
PRS_C3_OUTPUT_HSIZE_REG	0x0328	Parser Channel_3 Output Horizontal Size Register
PRS_C3_OUTPUT_VSIZE_REG	0x032C	Parser Channel_3 Output Vertical Size Register
PRS_C3_INPUT_PARA0_REG	0x0330	Parser Channel_3 Input Parameter0 Register
PRS_C3_INPUT_PARA1_REG	0x0334	Parser Channel_3 Input Parameter1 Register
PRS_C3_INPUT_PARA2_REG	0x0338	Parser Channel_3 Input Parameter2 Register
PRS_C3_INPUT_PARA3_REG	0x033C	Parser Channel_3 Input Parameter3 Register
PRS_C3_INT_EN_REG	0x0340	Parser Channel_3 Interrupt Enable Register
PRS_C3_INT_STA_REG	0x0344	Parser Channel_3 Interrupt Status Register
PRS_CH3_LINE_TIME_REG	0x0348	Parser Channel_3 Line Time Register
/	0x0348~0x04FC	Reserved
PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG	0x0500	Parser NCSIC RX Signal0 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL1_DLY_ADJ_REG	0x0504	Parser NCSIC RX Signal1 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL2_DLY_ADJ_REG	0x0508	Parser NCSIC RX Signal2 Delay Adjust Register

PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG	0x050C	Parser NCSIC RX Signal3 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG	0x0510	Parser NCSIC RX Signal4 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG	0x0514	Parser NCSIC RX Signal5 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG	0x0518	Parser NCSIC RX Signal6 Delay Adjust Register
PRS_SYNC_EN_REG	0x0520	Parser SYNC Enable Register
PRS_SYNC_CFG_REG	0x0524	Parser SYNC CFG Register
PRS_SYNC_WAIT_N_REG	0x0528	Parser SYNC WAIT N Register
PRS_SYNC_WAIT_M_REG	0x052C	Parser SYNC WAIT M Register
	0x0530~0x053C	
PRS_XSYNC_ENABLE_REG	0x0540	Parser XSYNC Enable Register
PRS_XVS_PERIOD_REG	0x0544	Parser XVS Period Register
PRS_XHS_PERIOD_REG	0x0548	Parser XHS Period Register
PRS_XVS_LENGHT_REG	0x054C	Parser XVS Lenght Register
PRS_XHS_LENGHT_REG	0x0550	Parser XHS Lenght Register

DMA0/1/2/3 register list:

CSIC_DMA_EN_REG	0x0000	CSIC DMA Enable Register
CSIC_DMA_CFG_REG	0x0004	CSIC DMA Configuration Register
CSIC_DMA_HSIZE_REG	0x0010	CSIC DMA Horizontal Size Register
CSIC_DMA_VSIZE_REG	0x0014	CSIC DMA Vertical Size Register
CSIC_DMA_F0_BUFA_REGc	0x0020	CSIC DMA FIFO 0 Output Buffer-A Address Register
CSIC_DMA_F0_BUFA_RESULT_REG	0x0024	CSIC DMA FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_F1_BUFA_REG	0x0028	CSIC DMA FIFO 1 Output Buffer-A Address Register
CSIC_DMA_F1_BUFA_RESULT_REG	0x002C	CSIC DMA FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_F2_BUFA_REG	0x0030	CSIC DMA FIFO 2 Output Buffer-A Address Register
CSIC_DMA_F1_BUFA_RESULT_REG	0x0034	CSIC DMA FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_BUF_LEN_REG	0x0038	CSIC DMA Buffer Length Register
CSIC_DMA_FLIP_SIZE_REG	0x003C	CSIC DMA Flip Size Register
CSIC_DMA_VI_TO_TH0_REG	0x0040	CSIC DMA Video Input Timeout Threshold0 Register
CSIC_DMA_VI_TO_TH1_REG	0x0044	CSIC DMA Video Input Timeout Threshold1 Register
CSIC_DMA_VI_TO_CNT_VAL_REG	0x0048	CSIC DMA Video Input Timeout Counter Value Register
CSIC_DMA_CAP_STA_REG	0x004C	CSIC DMA Capture Status Register
CSIC_DMA_INT_EN_REG	0x0050	CSIC DMA Interrupt Enable Register
CSIC_DMA_INT_STA_REG	0x0054	CSIC DMA Interrupt Status Register
CSIC_DMA_LINE_CNT_REG	0x0058	CSIC DMA LINE COUNTER Register
CSIC_DMA_FRM_CNT_REG	0x005C	CSIC DMA Frame Counter Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0060	CSIC DMA Frame Clock Counter Register
CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0064	CSIC DMA Accumulated And Internal Clock Counter Register
CSIC_DMA_FIFO_STAT_REG	0x0068	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x006C	CSIC DMA FIFO Threshold Register
CSIC_DMA_PCLK_STAT_REG	0x0070	CSIC DMA PCLK Statistic Register
CSIC_DMA_BUF_ADDR_FIFO0_ENTRY_REG	0x0080	CSIC DMA BUF Address FIFO0 Entry Register
CSIC_DMA_BUF_ADDR_FIFO1_ENTRY_REG	0x0084	CSIC DMA BUF Address FIFO1 Entry Register
CSIC_DMA_BUF_ADDR_FIFO2_ENTRY_REG	0x0088	CSIC DMA BUF Address FIFO2 Entry Register

CSIC_DMA_BUF_TH_REG	0x008C	CSIC DMA BUF Threshold Register
CSIC_DMA_BUF_ADDR_FIFO_CON_REG	0x0090	CSIC DMA BUF Address FIFO Content Register
CSIC_DMA_STORED_FRM_CNT_REG	0x0094	CSIC DMA Stored Frame Counter Register
CSIC_LBC_CONFIG_REG	0x0100	CSIC LBC Configure Register
CSIC_LBC_LINE_TAR_BIT0_REG	0x0104	CSIC LBC Line Target Bit0 Register
CSIC_LBC_LINE_TAR_BIT1_REG	0x0108	CSIC LBC Line Target Bit1 Register
CSIC_LBC_RC_ADV_REG	0x010C	CSIC LBC RC ADV Register
CSIC_LBC_MB_MIN_REG	0x0110	CSIC LBC MB MIN Register
CSIC_FEATURE_REG	0x01F4	CSIC DMA Feature List Register

CCI0/1 register list:

CCI_CTRL	0x0000	CCI Control Register
CCI_CFG	0x0004	CCI Transmission Configuration Register
CCI_FMT	0x0008	CCI Packet Format Register
CCI_BUS_CTRL	0x000C	CCI Bus Control Register
CCI_INT_CTRL	0x0014	CCI Interrupt Control Register
CCI_LC_TRIG	0x0018	CCI Line Counter Trigger Register
CCI_FIFO_ACC	0x0100~0x013C	CCI FIFO Access Register
CCI_RSV_REG	0x0200~0x0220	CCI Reserved Register

8.1.5. CCU Register Description

8.1.5.1. **CCU Clock Mode Register(Default Value:0x8000_0000)**

Offset: 0x0000			**Register Name: CCU_CLK_MODE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	CCU_CLK_GATING_DISABLE 0:CCU Clock Gating Registers(0x0004~0x0010) effect 1:CCU Clock Gating Registers(0x0004~0x0010) not effect
30:4	/	/	/
3:1	/	/	/
0	R/W	0x0	MCSI_CLK_MODE 0: CSI Core works in isp_clk2x clock 1: CSI Core works in csi clock

8.1.5.2. **CCU Parser Clock Enable Register(Default Value:0x0000_0000)**

Offset: 0x0004			**Register Name: CCU_PARSER_CLK_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCSI_COMBO0_CLK_ENABLE 0: Combo0 clock disable 1: Combo0 clock enable

7:2	/	/	/
1	R/W	0x0	MCSI_PARSER1_CLK_ENABLE 0: CSI Parser1 clock disable 1: CSI Parser1 clock enable
0	R/W	0x0	MCSI_PARSER0_CLK_ENABLE 0: CSI Parser0 clock disable 1: CSI Parser0 clock enable

8.1.5.3. **CCU ISP Clock Enable Register(Default Value:0x0000_0000)**

Offset: 0x0008			**Register Name: CCU_ISP_CLK_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	MISP0_BRIDGE_CLK_ENABLE 0: ISP0 bridge clock disable 1: ISP0 bridge clock enable
3:1	/	/	/
0	R/W	0x0	MISP0_CLK_ENABLE 0: ISP0 clock disable 1: ISP0 clock enable

8.1.5.4. **CCU Post0 Clock Enable Register(Default Value:0x0000_0000)**

Offset: 0x000C			**Register Name: CCU_POST0_CLK_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MCSI_POST0_CLK_ENABLE 0: POST0 clock disable 1: POST0 clock enable
15:12	/	/	/
11	R/W	0x0	MCSI_VIPP3_CLK_ENABLE 0: VIPP3 clock disable 1: VIPP3 clock enable,when MCSI_POST0_CLK_ENABLE is 1
10	R/W	0x0	MCSI_VIPP2_CLK_ENABLE 0: VIPP2 clock disable 1: VIPP2 clock enable,when MCSI_POST0_CLK_ENABLE is 1
9	R/W	0x0	MCSI_VIPP1_CLK_ENABLE 0:VIPP1 clock disable 1: VIPP1 clock enable,when MCSI_POST0_CLK_ENABLE is 1
8	R/W	0x0	MCSI_VIPP0_CLK_ENABLE 0: VIPP0 clock disable 1: VIPP0 clock enable,when MCSI_POST0_CLK_ENABLE is 1
7:4	/	/	/
3	R/W	0x0	MCSI_BK3_CLK_ENABLE

			0: BK3 clock disable 1: BK3 clock enable,when MCSI_POST0_CLK_ENABLE is 1
2	R/W	0x0	MCSI_BK2_CLK_ENABLE 0: BK2 clock disable 1: BK2 clock enable,when MCSI_POST0_CLK_ENABLE is 1
1	R/W	0x0	MCSI_BK1_CLK_ENABLE 0: BK1 clock disable 1: BK1 clock enable,when MCSI_POST0_CLK_ENABLE is 1
0	R/W	0x0	MCSI_BK0_CLK_ENABLE 0: BK0 clock disable 1: BK0 clock enable,when MCSI_POST0_CLK_ENABLE is 1

8.1.6. CSIC TOP Register Description

8.1.6.1. CSIC TOP Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CSIC_TOP_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_EN CSIC Version Register Read Enable: 0: Disable 1: Enable
30:4	/	/	/
3	R/W	0x0	ISP_BRIDGE_EN Enable Async Bridge from parser to isp and isp to post, when isp uses different clock source from csi_top_clk 0: disable 1: enable
2	R/W	0x0	BIST_MODE_EN 0: Closed 1: EN BIST TEST
1	/	/	/
0	R/W	0x0	CSIC_TOP_EN 0: Reset and disable the CSIC module 1: Enable the CSIC module

8.1.6.2. CSIC Pattern Generation Enable Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_PTN_GEN_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.

15:5	/	/	/
4	R/WAC	0x0	PTN_START CSIC Pattern Generating Start 0: Finish other: Start Software write this bit to “1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to “0” automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern Generation Enable

8.1.6.3. **CSIC Pattern Control Register(Default Value:0x0000_000F)**

Offset: 0x0008			**Register Name: CSIC_PTN_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	PTN_PORT_SEL Pattern Generator output port selection 000:MCSIC0 001:/ 010:NCSIC0 011:NCSIC1 100:/ 101:/
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH 00:8bit 01:10bit 10:12bit 11:reserved
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000~0011:reserved 0100:NCSIC YUV 8 bits width 0101:NCSIC YUV 16 bits width 0110:reserved 0111:reserved 1000:BT656 8 bits width 1001:BT656 16 bits width 1010:reserved 1011:reserved 1100:BAYER 12 bits for ISPFE 1101:UYVY422 12 bits for ISPFE 1110:UYVY420 12 bits for ISPFE

			1111:reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

8.1.6.4. **CSIC Pattern Generation Length Register(Default Value:0x0000_0000)**

Offset: 0x0020			**Register Name: CSIC_PTN_LEN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

8.1.6.5. **CSIC Pattern Generation Address Register(Default Value:0x0000_0000)**

Offset: 0x0024			**Register Name: CSIC_PTN_ADDR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

8.1.6.6. **CSIC Pattern ISP Size Register(Default Value:0x0000_0000)**

Offset: 0x0028			**Register Name: CSIC_PTN_ISP_SIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size,only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size,only valid for ISP mode pattern generation.

8.1.6.7. **CSIC Connect Enable Register(Default Value:0x0000_0000)**

Offset :0x002C			**Register Name: CSIC_CONNECT__SEL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
23:20	R/W	0x0	SYNC_CTR_PAR_EN Bit20: Enable Control Parser0 Bit17: Enable Control Parser1 Bit18: / Bit19: /

19:16	R	0x0	SYNC_SIGNAL_STATUS Bit16: Received SYNC_IN0 flag Bit17: Received SYNC_IN1 flag Bit18: Received SYNC_IN2 flag Bit19: Sent SYNC_OUT flag
15:10	/	/	/
9:8	R/W	0x0	SYNC_WIDTH 0: 8*TOP_CLK 1: 16*TOP_CLK 2: 24*TOP_CLK
7	/	/	/
6:4	R/W	0x0	SLAVE_INPUT_SEL Bit4: Enable SYNC_IN0 Bit5: Enable SYNC_IN1 Bit6: Enable SYNC_IN2
3	/	/	/
2	R/W	0x0	CONNECT_MODE_SEL 0: Slave 1: Master
1	R/W	0x0	SYNC_OUTPUT_EN 0: Disable 1: Enable
0	R/W	0x0	CONNECT_MODE_EN 0: Disable 1: Enable

8.1.6.8. **CSIC ISP0 Input0 Select Register(Default Value:0x0000_0000)**

Offset :0x0030			**Register Name: CSIC_ISP0_INPUT0_SEL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input0 Select 000: input from Parser0 CH0 001: input from Parser1 CH0 010: / 011: / 100: input from Parser0 CH1 101: input from Parser1 CH1 110: / 111: / others: reserved

8.1.6.9. **CSIC ISP0 Input1 Select Register(Default Value:0x0000_0000)**

Offset :0x0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input1 select 000: input from Parser0 CH1 001: input from Parser1 CH1 others: reserved

8.1.6.10. **CSIC ISP0 Input2 Select Register(Default Value:0x0000_0000)**

Offset :0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input2 Select 000: input from Parser0 CH2 001: input from Parser1 CH2 others: reserved

8.1.6.11. **CSIC ISP0 Input3 Select Register(Default Value:0x0000_0000)**

Offset :0x003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input3 Select 000: input from Parser0 CH3 001: input from Parser1 CH3 others: reserved

8.1.6.12. **CSIC ISP Bridge Buffer Maxuse Counter Clear Register(Default Value:0x0000_0000)**

Offset :0x0070			Register Name: CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	/	/	/
1	R/W	0x0	ISP0_BRG1_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
0	R/W	0x0	ISP0_BRG0_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear

8.1.6.13. **CSIC ISP0 Bridge Buffer Maxuse Counter Register(Default Value:0x0000_0000)**

Offset :0x0074			Register Name: CSIC_ISP0_BRG_BUF_MAXUSE_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	ISP0_BRG1_BUF_MAXUSE_CNT
15:0	RO	0x0	ISP0_BRG0_BUF_MAXUSE_CNT

8.1.6.14. **CSIC ISP0 Bridge Interrupt Enable Register(Default Value:0x0000_0000)**

Offset :0x0084			Register Name: CSIC_ISP0_BRG_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25	R/W	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side
24	R/W	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:18	/	/	/
17	R/W	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side
16	R/W	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:10	/	/	/
9	R/W	0x0	ISP0_BRG1_BUF_OV_INT_EN ISP0 Bridge1 Buffer overflow interrupt enable
8	R/W	0x0	ISP0_BRG0_BUF_OV_INT_EN ISP0 Bridge0 Buffer overflow interrupt enable
7:2	/	/	/
1	R/W	0x0	ISP0_BRG1_RS_INT_EN ISP0 Bridge0 Read clock too slow interrupt enable
0	R/W	0x0	ISP0_BRG0_RS_INT_EN ISP0 Bridge0 Read clock too slow interrupt enable

8.1.6.15. **CSIC ISP0 Bridge Interrupt Pending Register(Default Value:0x0000_0000)**

Offset :0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25	R/W1C	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side
24	R/W1C	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:18	/	/	/
17	R/W1C	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side

16	R/W1C	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:10	/	/	/
9	R/W1C	0x0	ISP0_BRG1_BUF_OV_INT_PD ISP0 Bridge1 Buffer overflow interrupt pending
8	R/W1C	0x0	ISP0_BRG0_BUF_OV_INT_PD ISP0 Bridge0 Buffer overflow interrupt pending
7:2	/	/	/
1	R/W1C	0x0	ISP0_BRG1_RS_INT_PD ISP0 Bridge0 Read clock too slow interrupt pending
0	R/W1C	0x0	ISP0_BRG0_RS_INT_PD ISP0 Bridge0 Read clock too slow interrupt pending

8.1.6.16. **CSIC VIPP0 Input Select Register(Default Value:0x0000_0000)**

Offset :0x00A0			**Register Name: CSIC_VIPP0_INPUT_SEL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP0 Input Select 000: input from ISP0 CH0 001: input from ISP1 CH0 others: reserved

8.1.6.17. **CSIC VIPP1 Input Select Register(Default Value:0x0000_0000)**

Offset :0x00A4			**Register Name: CSIC_VIPP1_INPUT_SEL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP1 Input Select 000: input from ISP0 CH0 001: input from ISP1 CH0 010: input from ISP0 CH1 011: input from ISP1 CH1 others: reserved

8.1.6.18. **CSIC VIPP2 Input Select Register(Default Value:0x0000_0000)**

Offset :0x00A8			**Register Name: CSIC_VIPP2_INPUT_SEL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP2 Input select 000: input from ISP0 CH0 001: input from ISP1 CH0

			010: input from ISP0 CH2 011: input from ISP1 CH2 others: reserved

8.1.6.19. **CSIC VIPP3 Input Select Register(Default Value:0x0000_0000)**

Offset :0x00AC			Register Name: CSIC_VIPP3_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP3 Input Select 000: input from ISP0 CH0 001: input from ISP1 CH0 010: input from ISP0 CH3 011: input from ISP1 CH3 100: input from ISP1 CH1 others: reserved

8.1.6.20. **CSIC Feature List Register(Default Value:0x2121_4400)**

Offset: 0x00F0			Register Name: CSIC_FEATURE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R	0x2	VER_SMALL_PARSER_NUM Only can be read when version register read enable is on.
27:24	R	0x1	VER_SMALL_MCSI_NUM Only can be read when version register read enable is on.
23:20	R	0x2	Reserved
19:16	R	0x1	VER_SMALL_ISP_NUM Only can be read when version register read enable is on.
15:12	R	0x4	VER_SMALL_VIPP_NUM Only can be read when version register read enable is on.
11:8	R	0x4	VER_SMALL_DMA_NUM Only can be read when version register read enable is on.
7:0	/	/	/

8.1.7. CSIC Parser Register Description

8.1.7.1. **Parser Enable Register(Default Value:0x0000_0000)**

Offset: 0x0000			Register Name: PRS_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCSIC_EN 0: Reset and disable the MCSIC module 1: Enable the MCSIC module

30:17	/	/	/
16	R/W	0x0	NCSIC_EN 0: Reset and disable the NCSIC module 1: Enable the NCSIC module
16	R/W	0x0	PCLK_EN 0:Gate pclk input 1:Enable pclk input
14:3	/	/	/
2	R/W	0x0	PRS_CH_MODE 0: Parser output channel 0~3 corresponding from input channel 0~3 1: Parser output channel 0~3 all from input channel 0(MIPI SEHDR)
1	R/W	0x0	PRS_MODE 0: Reserved 1: MCSI
0	R/W	0x0	PRS_EN 0: Reset and disable the parser module 1: Enable the parser module

8.1.7.2. **Parser NCSIC Interface Configuration Register(Default Value:0x0105_0080)**

Offset: 0x0004			**Register Name: PRS_NCSIC_IF_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30:28	/	/	/
27:24	R/W	0x1	FIELD_DT_PCLK_SHIFT Only for vsync detected field mode,the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT
23:22	/	/	/
21	R/W	0x0	SRC_TYPE Source type 0: Progressed 1: Interlaced
20	R/W	0x0	NCSI_DATA_ALIGN 0: NCSI data input bus in low bit alignment 1: NCSI data input bus in high bit alignment(16-bit)
19	R/W	0x0	FIELD For YUV HV timing, Field polarity 0: negative(field=0 indicate odd, field=1 indicate even) 1: positive(field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	0x1	VREF_POL

			Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
17	R/W	0x0	HERF_POL Href polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
16	R/W	0x1	CLK_POL Data clock type 0: active in rising edge 1: active in falling edge
15:14	R/W	0x0	Field_DT_MODE（only valid when CSI_IF is YUV and source type is interlaced） 00:by both field and vsync 01:by field 10:by vsync 11:reserved
13	R/W	0x0	DDR_SAMPLE_ MODE_EN 0:disable 1:enable
12:11	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2’b0 at the actual CSI data bus according to these sequences: 00: 6’bx+D[9:8], D[7:0] 01: D[9:2], 6’bx+D[1:0] 10: D[7:0], D[9:8]+6’bx 11: D[7:0], 6’bx+D[9:8]
10:8	R/W	0x0	IF_DATA_WIDTH 000: 8 bit data bus 001: 10 bit data bus 010: 12 bit data bus 011: 8+2bit data bus 100: 2x8bit data bus Others: reserved
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel:

			x0: UV x1: VU
5	R/W	0x0	OUTPUT_MODE 0:field mode 1:frame mode
4:0	R/W	0x0	CSI_IF YUV(separate syncs): 00000: YUYV422 Interleaved or RAW (All data in one data bus) 00001: 16 bit YUYV422 Interleaved 00010: Reserved 00011: Reserved CCIR656(embedded syncs): 00100: BT656 1 channel 00101: 16bit BT656(BT1120 like) 1 channel 00110: Reserved 00111: Reserved 01100: BT656 2 channels (All data interleaved in one data bus) 01101: 16bit BT656(BT1120 like) 2 channels(All data interleaved in one data bus) 01110: BT656 4 channels (All data interleaved in one data bus) 01111:16bit BT656(BT1120 like) 4 channels(All data interleaved in one data bus) Others: Reserved

8.1.7.3. **Parser MCSIC Interface Configuration Register(Default Value:0x0000_0080)**

Offset: 0x0008			**Register Name: PRS_MCSIC_IF_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30:8	/	/	/
7:6	R/W	0X2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU

5	R/W	0x0	OUTPUT_MODE 0:field mode 1:frame mode
4:0	/	/	/

8.1.7.4. **Parser Capture Register(Default Value:0x0000_0000)**

Offset: 0x000C			Register Name: PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:26	R/W	0x0	CH3_CAP_MASK Vsync number masked before capture.
25	R/W	0x0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	RC/W	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
13:12	/	/	/
21:18	R/W	0x0	CH2_CAP_MASK Vsync number masked before capture.
17	R/W	0x0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	RC/W	0x0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.

15:14	/	/	/
13:10	R/W	0x0	CH1_CAP_MASK Vsync number masked before capture.
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
8	RC/W	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
7:6	/	/	/
5:2	R/W	0x0	CH0_CAP_MASK Vsync number masked before capture.
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	RC/W	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.

8.1.7.5. **Parser Signal Status Register(Default Value:0x0000_0000)**

Offset: 0x0010			**Register Name: PRS_SIGNAL_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	PCLK_STA Indicates the pclk status 0:low

			1:high
23:0	R	0x0	DATA_STA Indicates the Dn status(n=0~23),MSB for D23,LSB for D0 0:low 1:high

8.1.7.6. **Parser NCSIC BT656 Header Configuration Register (Default Value:0x0302_0100)**

Offset: 0x0014			**Register Name: PRS_NCSIC_BT656_HEAD_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	CH3_ID The low 4bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode
23:20	/	/	/
19:16	R/W	0x2	CH2_ID The low 4bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode
15:12	/	/	/
11:8	R/W	0x1	CH1_ID The low 4bit of BT656 header for channel 1 Only valid in BT656 multi-channel mode
7:4	/	/	/
3:0	R/W	0x0	CH0_ID The low 4bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode

8.1.7.7. **Parser Channel_0 Input Format Register(Default Value:0x0000_0003)**

Offset: 0x0024			**Register Name: PRS_CH0_INFMT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.8. **Parser Channel_0 Output Horizontal Size Register(Default Value:0x0500_0000)**

Offset: 0x0028			Register Name: PRS_CH0_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.9. **Parser Channel_0 Output Vertical Size Register(Default Value:0x02D0_0000)**

Offset: 0x002C			Register Name: PRS_CH0_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.7.10. **Parser Channel_0 Input Parameter0 Register(Default Value:0x0000_0000)**

Offset: 0x0030			Register Name: PRS_CH0_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.11. **Parser Channel_0 Input Parameter1 Register(Default Value:0x0000_0000)**

Offset: 0x0034			Register Name: PRS_CH0_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.12. **Parser Channel_0 Input Parameter2 Register(Default Value:0x0000_0000)**

Offset: 0x0038			Register Name: PRS_CH0_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.13. **Parser Channel_0 Input Parameter3 Register(Default Value:0x0000_0000)**

Offset: 0x003C			Register Name: PRS_CH0_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.14. **Parser Channel_0 Interrupt Enable Register(Default Value:0x0000_0000)**

Offset: 0x0040			Register Name: PRS_CH0_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.15. **Parser Channel_0 Interrupt Status Register(Default Value:0x0000_0000)**

Offset: 0x0044			Register Name: PRS_CH0_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.

0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

8.1.7.16. **Parser Channel_0 Line Time Register(Default Value:0x0000_0000)**

Offset: 0x0048			**Register Name: PRS_CH0_LINE_TIME_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH0_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH0_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.17. **Parser Channel_1 Input Format Register(Default Value:0x0000_0003)**

Offset: 0x0124			**Register Name: PRS_CH1_INFMT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.18. **Parser Channel_1 Output Horizontal Size Register(Default Value:0x0500_0000)**

Offset: 0x0128			**Register Name: PRS_CH1_OUTPUT_HSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.19. **Parser Channel_1 Output Vertical Size Register(Default Value:0x02d0_0000)**

Offset: 0x012C			**Register Name: PRS_CH1_OUTPUT_VSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.7.20. **Parser Channel_1 Input Parameter0 Register(Default Value:0x0000_0000)**

Offset: 0x0130			**Register Name: PRS_CH1_INPUT_PARA0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.21. **Parser Channel_1 Input Parameter1 Register(Default Value:0x0000_0000)**

Offset: 0x0134			**Register Name: PRS_CH1_INPUT_PARA1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.22. **Parser Channel_1 Input Parameter2 Register(Default Value:0x0000_0000)**

Offset: 0x0138			**Register Name: PRS_CH1_INPUT_PARA2_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.23. **Parser Channel_1 Input Parameter3 Register(Default Value:0x0000_0000)**

Offset: 0x013C			**Register Name: PRS_CH1_INPUT_PARA3_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y

15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.24. **Parser Channel_1 Interrupt Enable Register(Default Value:0x0000_0000)**

Offset: 0x0140			Register Name: PRS_CH1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.25. **Parser Channel_1 Interrupt Status Register(Default Value:0x0000_0000)**

Offset: 0x0144			Register Name: PRS_CH1_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

8.1.7.26. **Parser Channel_1 Line Time Register(Default Value:0x0000_0000)**

Offset: 0x0148			Register Name: PRS_CH1_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH1_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH1_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.27. **Parser Channel_2 Input Format Register(Default Value:0x0000_0003)**

Offset: 0x0224			Register Name: PRS_CH2_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.28. **Parser Channel_2 Output Horizontal Size Register(Default Value:0x0500_0000)**

Offset: 0x0228			Register Name: PRS_CH2_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.29. **Parser Channel_2 Output Vertical Size Register(Default Value:0x02D0_0000)**

Offset: 0x022C			Register Name: PRS_CH2_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.7.30. **Parser Channel_2 Input Parameter0 Register(Default Value:0x0000_0000)**

Offset: 0x0230			Register Name: PRS_CH2_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress

			1:Interlace

8.1.7.31. **Parser Channel_2 Input Parameter1 Register(Default Value:0x0000_0000)**

Offset: 0x0234			Register Name: PRS_CH2_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.32. **Parser Channel_2 Input Parameter2 Register(Default Value:0x0000_0000)**

Offset: 0x0238			Register Name: PRS_CH2_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.33. **Parser Channel_2 Input Parameter3 Register(Default Value:0x0000_0000)**

Offset: 0x023C			Register Name: PRS_CH2_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.34. **Parser Channel_2 Interrupt Enable Register(Default Value:0x0000_0000)**

Offset: 0x0240			Register Name: PRS_CH2_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable

0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.35. **Parser Channel_2 Interrupt Status Register(Default Value:0x0000_0000)**

Offset: 0x0244			Register Name: PRS_CH2_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

8.1.7.36. **Parser Channel_2 Line Time Register(Default Value:0x0000_0000)**

Offset: 0x0248			Register Name: PRS_CH2_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH2_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH2_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.37. **Parser Channel_3 Input Format Register(Default Value:0x0000_0003)**

Offset: 0x0324			Register Name: PRS_CH3_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.38. **Parser Channel_3 Output Horizontal Size Register(Default Value:0x0500_0000)**

Offset: 0x0328			Register Name: PRS_CH3_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.39. **Parser Channel_3 Output Vertical Size Register(Default Value:0x02D0_0000)**

Offset: 0x032C			Register Name: PRS_CH3_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.7.40. **Parser Channel_3 Input Parameter0 Register(Default Value:0x0000_0000)**

Offset: 0x0330			Register Name: PRS_CH3_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.41. **Parser Channel_3 Input Parameter1 Register(Default Value:0x0000_0000)**

Offset: 0x0334			Register Name: PRS_CH3_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.42. **Parser Channel_3 Input Parameter2 Register(Default Value:0x0000_0000)**

Offset: 0x0338			Register Name: PRS_CH3_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.43. **Parser Channel_3 Input Parameter3 Register(Default Value:0x0000_0000)**

Offset: 0x033C			Register Name: PRS_CH3_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.44. **Parser Channel_3 Interrupt Enable Register(Default Value:0x0000_0000)**

Offset: 0x0340			Register Name: PRS_CH3_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.45. **Parser Channel_3 Interrupt Status Register(Default Value:0x0000_0000)**

Offset: 0x0344			Register Name: PRS_CH3_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.

0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

8.1.7.46. **Parser Channel_3 Line Time Register(Default Value:0x0000_0000)**

Offset: 0x0348			Register Name: PRS_CH3_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH3_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH3_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.47. **Parser NCSIC RX Signal0 Delay Adjust Register(Default Value:0x0000_0000)**

Offset :0x0500			Register Name: PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	Filed_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	Vsync_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	Hsync_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	Pclk_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.48. **Parser NCSIC RX Signal1 Delay Adjust Register(Default Value:0x0000_0000)**

Offset :0x0504			Register Name: PRS_NCSIC_RX_SIGNAL1_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D23_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D22_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D21_dly

			32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D20_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.49. **Parser NCSIC RX Signal2 Delay Adjust Register(Default Value:0x0000_0000)**

Offset :0x0508			Register Name: PRS_NCSIC_RX_SIGNAL2_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D19_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D18_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D17_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D16_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.50. **Parser NCSIC RX Signal3 Delay Adjust Register(Default Value:0x0000_0000)**

Offset :0x050C			Register Name: PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D15_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D14_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D13_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D12_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.51. **Parser NCSIC RX Signal4 Delay Adjust Register(Default Value:0x0000_0000)**

Offset :0x0510			Register Name: PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:29	/	/	/
28:24	R/W	0x0	D11_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D10_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D9_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D8_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.52. **Parser NCSIC RX Signal5 Delay Adjust Register(Default Value:0x0000_0000)**

Offset :0x0514			**Register Name: PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D7_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D6_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D5_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D4_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.53. **Parser NCSIC RX Signal6 Delay Adjust Register(Default Value:0x0000_0000)**

Offset :0x0518			**Register Name: PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D3_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D2_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D1_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/

4:0	R/W	0x0	D0_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.54. **Parser CSIC SYNC EN Register(Default Value:0x0000_0000)**

Offset :0x0520			Register Name: CSIC_SYNC_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
19:16	R/W	0x0	Input vsync singal Source select 0: Vsync signals all from 1 parser 1: Vsync signals from 2 parser 2: Vsync signals from 4 parser others:reserved
15:12	/	/	/
11:8	R/W	0x0	Generate sync singal Benchmark select Bit8: USE VSYNC_Input0 Bit9: USE VSYNC_Input1 Bit10: USE VSYNC_Input2 Bit11: USE VSYNC_Input3 Set 1,Use input
7:4	R/W	0x0	Parser input vsync singal enable in sync mode Bit4: VSYNC_Input0 Bit5: VSYNC_Input1 Bit6: VSYNC_Input2 Bit7: VSYNC_Input3 Set 1,enable input
3	/	/	/
2	R/W	0x0	Parser sent sync singal via by 0: FSYNC0 1: FSYNC1
1	R/W	0x0	Parser sync singal source select 0: From outside 1: Generate by self
0	R/W	0x0	Enable Parser sent sync singal 0: Disable 1: Enable

8.1.7.55. **Parser CSIC SYNC CFG Register(Default Value:0x0000_0000)**

Offset :0x0524			Register Name: CSIC_PULSE_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PUL_WID Sync singal pulse width $N*T_{24M}$,

			N*T_{24M}≥4*Tpclk
15:0	R/W	0x0	SYNC_DISTANCE The interval of two sync signal

8.1.7.56. **Parser CSIC VS WAIT N Register(Default Value:0x0000_0000)**

Offset :0x0528			Register Name: CSIC_SYNC_WAIT_N_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VS_WAIT_N When multi-channel vsync all come,the max wait time.

8.1.7.57. **Parser CSIC VS WAIT M Register(Default Value:0x0000_0000)**

Offset :0x052C			Register Name: CSIC_SYNC_WAIT_M_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VS_WAIT_M When in multi-channel mode,vsync comes at the different time,these bits indicate the max wait time.

8.1.7.58. **CSIC XSYNC ENABLE Register(Default Value:0x0000_0000)**

Offset:0x0540			Register Name: CSIC_XSYNC_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0x0	XVS_TO_XHS_T The period of XHS delay to XVS
7:5	/	/	/
4	R/W	0x0	XVS_XHS_OUT_SEL When sensor works in slave mode ,this bit select XVS and XHS to output. 0: XHS0,XVS0 1: XHS1,XVS1
3	R/W	0x0	XVS_POL When sensor works in slave mode ,this bit set polarity of XVS. 0: Negative 1: Positive
2	R/W	0x0	XHS_POL When sensor works in slave mode ,this bit set polarity of XHS. 0: Negative 1: Positive
1	R/W	0x0	XVS_OUT_EN When sensor works in slave mode ,this bit enable output XVS to sensor 0: Disable 1: Enable
0	R/W	0x0	XHS_OUT_EN

			When sensor works in slave mode ,this bit enable output XHS to sensor 0: Disable 1: Enable

8.1.7.59. **CSIC XVS Period Register(Default Value:0x0000_0000)**

Offset:0x0544			Register Name: CSIC_XVS_Period_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	XVS_T The period of XVS signal

8.1.7.60. **CSIC XHS Period Register(Default Value:0x0000_0000)**

Offset:0x0548			Register Name: CSIC_XHS_Period_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	XHS_T The period of XHS signal

8.1.7.61. **CSIC XVS Length Register(Default Value:0x0000_0000)**

Offset:0x054C			Register Name: CSIC_XVS_LENGTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	XVS_LEN The valid length of XVS signal in one XVS cycle.

8.1.7.62. **CSIC XHS Length Register(Default Value:0x0000_0000)**

Offset:0x0550			Register Name: CSIC_XHS_LENGTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	XHS_LEN The valid length of XHS signal in one XHS cycle.

8.1.7.63. **CSIC SYNC DELAY Register(Default Value:0x0000_0000)**

Offset:0x0554			Register Name: CSIC_SYNC_DLY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	SYNC_DLY The XHS/XVS will sent after SYNC_DLY time.

8.1.8. CSIC DMA Register Description

8.1.8.1. CSIC DMA Enable Register(Default Value:0x7000_0000)

Offset:0x0000			Register Name: CSIC_DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_EN
30	R/W	0x1	VFLIP_BUF_ADDR_CFG_MODE Vflip buffer address set by software or calculated by hardware 0: hardware 1: software
29	R/W	0x1	BUF_LENGTH_CFG_MODE buffer length set by software or calculated by hardware 0: hardware 1: software
28	R/W	0x1	FLIP_SIZE_CFG_MODE FLIP SIZE set by software or calculated by hardware 0: hardware 1: software
27:9	/	/	/
8	R/W	0x0	LBC_EN 0: disable 1: enable
7	R/W	0x0	BUF_ADDR_MODE 0: Buffer Address Register Mode 1: Buffer Address FIFO Mode
6	R/W	0x0	VI_TO_CNT_EN Enable Video Input Timeout counter, add 1 when there is no effective video input in a 12M clock, clear to 0 when detecting effective video input. 0: disable 1: enable
5	R/W	0x0	FRAME_CNT_EN When BK_TOP_EN enable, setting 1 to this bit indicates the Frame counter start to add. 0: Disable 1: Enable
4	R/W	0x0	DMA_EN When BK_TOP_EN enable, setting 1 to this bit indicates module works in DMA mode. 0: Disable 1: Enable
3	R/W	0x0	FBC_EN When BK_TOP_EN enable, setting 1 to this bit indicates module works in FBC mode. 0: Disable 1: Enable

2	R/W	0x0	CLK_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
1	R/W	0x0	CLK_CNT_EN clk count per frame enable
0	R/W	0x0	BK_TOP_EN 0: Disable 1: Enable

8.1.8.2. **CSIC DMA Configuration Register(Default Value:0x0000_0000)**

Offset: 0x0004			**Register Name: CSIC_DMA_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV 10bit store configure 0: YUV 10bit stored in low 10bit of a 16bit-word 1: YUV 10bit stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: reserved 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: reserved When the input format is set YUV422

			0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: field planar YCbCr 422 10bit UV combined(UV sequence) 1101: field planar YCbCr 420 10bit UV combined(UV sequence) 1110: field planar YCbCr 422 10bit UV combined(VU sequence) 1111: field planar YCbCr 420 10bit UV combined(VU sequence) When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011~1100: reserved 1101: field planar YCbCr 420 10bit UV combined(UV sequence) 1110: reserved 1111: field planar YCbCr 420 10bit UV combined(VU sequence) Others: reserved
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection.

			00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
5:2	/	/	/
1:0	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 0: 256 bytes (if hflip is enable, always select 256 bytes) 1: 512 bytes 2: 1k bytes 3: 2k bytes

8.1.8.3. CSIC DMA Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0010			Register Name: CSIC_DMA_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable,FBC_EN enable,DMA_EN disable,these bits indicate input width in FBC mode. When BK_TOP_EN enable,FBC_EN disable,DMA_EN enable, LBC disable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode. When BK_TOP_EN enable,FBC_EN disable,DMA_EN enable, LBC enable, these bits indicate input width in LBC mode.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.8.4. CSIC DMA Vertical Size Register(Default Value:0x02d0_0000)

Offset: 0x0014			Register Name: CSIC_DMA_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN

			When BK_TOP_EN enable,FBC_EN enable,DMA_EN disable,these bits indicate input height in FBC mode. When BK_TOP_EN enable,FBC_EN disable,DMA_EN enable, LBC disable, these bits indicate Valid line number of a frame in DMA mode. When BK_TOP_EN enable,FBC_EN disable,DMA_EN enable, LBC enable, these bits indicate input height in LBC mode.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.8.5. **CSIC DMA FIFO 0 Output Buffer-A Address Register(Default Value:0x0000_0000)**

Offset: 0x0020			**Register Name: CSIC_DMA_F0_BUFA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F0_BUFA When BK_TOP_EN enable,FBC_EN enable,DMA_EN disable,these bits indicate output address of overhead data in FBC mode. When BK_TOP_EN enable,FBC_EN disable,DMA_EN enable, LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When BK_TOP_EN enable,FBC_EN disable,DMA_EN enable, LBC_EN enable, these bits indicate the output buffer address in LBC mode.

8.1.8.6. **CSIC DMA FIFO 0 Output Buffer-A Address Result Register(Default Value:0x0000_0000)**

Offset: 0x0024			**Register Name: CSIC_DMA_F0_BUFA_RESULT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

8.1.8.7. **CSIC DMA FIFO 1 Output Buffer-A Address Register(Default Value:0x0000_0000)**

Offset: 0x0028			**Register Name: CSIC_DMA_F1_BUFA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F1_BUFA When BK_TOP_EN enable,FBC_EN enable,DMA_EN disable,these bits indicate output address of compressed data in FBC mode. When BK_TOP_EN enable,FBC_EN disable,DMA_EN enable,these bits indicate FIFO 1 output buffer-A address in DMA mode.

8.1.8.8. **CSIC DMA FIFO 1 Output Buffer-A Address Result Register(Default Value:0x0000_0000)**

Offset: 0x002C			Register Name: CSIC_DMA_F1_BUFA_RESULT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

8.1.8.9. **CSIC DMA FIFO 2 Output Buffer-A Address Register(Default Value:0x0000_0000)**

Offset: 0x0030			Register Name: CSIC_DMA_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

8.1.8.10. **CSIC DMA FIFO 2 Output Buffer-A Address Result Register(Default Value:0x0000_0000)**

Offset: 0x0034			Register Name: CSIC_DMA_F2_BUFA_RESULT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

8.1.8.11. **CSIC DMA Buffer Length Register(Default Value:0x0280_0500)**

Offset: 0x0038			Register Name: CSIC_DMA_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x280	BUF_LEN_C DMA_MODE:Buffer length of chroma C in a line. Unit is byte. LBC_MODE:Buffer length Stride of luminance Y in ONLY Y line. Unit is byte. Only Readable when BUF_LENGTH_CFG_MODE set 0
15:14	/	/	/
13:0	R/W	0x500	BUF_LEN DMA_MODE:Buffer length of luminance Y in a line. Unit is byte. LBC_MODE:Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte. Only Readable when BUF_LENGTH_CFG_MODE set 0

8.1.8.12. **CSIC DMA Flip Size Register(Default Value:0x02D0_0500)**

Offset: 0x003C			Register Name: CSIC_DMA_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:14	/	/	/
13:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

8.1.8.13. **CSIC DMA Video Input Timeout Threshold0 Register(Default Value:0x0000_0000)**

Offset: 0x0040			Register Name: CSIC_DMA_VI_TO_TH0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Video Input Timeout Threshold0 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH0 after VI_TO_CNT_EN is set , Time Unit is a 12M clock period.

8.1.8.14. **CSIC DMA Video Input Timeout Threshold1 Register(Default Value:0x0000_0000)**

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Video Input Timeout Threshold1 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH1 after getting the first frame has been input, Time Unit is a 12M clock period.

8.1.8.15. **CSIC DMA Video Input Timeout Counter Value Register(Default Value:0x0000_0000)**

Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Video Input Timeout Counter Value Indicate the current value of Video Input Timeout Counter

8.1.8.16. **CSIC DMA Capture Status Register(Default Value:0x0000_0000)**

Offset: 0x004C			Register Name: CSIC_DMA_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	FIELD_STA

			The status of the received field 0: Field 0 1: Field 1
1	R	0x0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
0	R	0x0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

8.1.8.17. **CSIC DMA Interrupt Enable Register(Default Value:0x0000_0000)**

Offset: 0x0050			**Register Name: CSIC_DMA_INT_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT when frame starts with empty Buffer Address FIFO , only use in BUF Address FIFO MODE
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12	R/W	0x0	VIDEO_INPUT_TO_INT_EN Set an INT when no video input exceeds the setting threshold time
11	R/W	0x0	CLR_FRAME_CNT_INT_EN Set a INT When Clear Frame cnt.
10	R/W	0x0	SENT_SYNC_INT_EN Set a INT When sent a SYNC signal.
9	R/W	0x0	FBC_DATA_WRDDR_FULL_EN Error flag of FBC_DATA_WRDDR_FULL.
8	R/W	0x0	FBC_OVHD_WRDDR_FULL_EN Error flag of FBC_OVHD_WRDDR_FULL.

7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

8.1.8.18. **CSIC DMA Interrupt Status Register(Default Value:0x0000_0000)**

Offset: 0x0054			**Register Name: CSIC_DMA_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD

			Set an INT when frame starts with empty Buffer Address FIFO, only use in BUF Address FIFO MODE
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12	R/W1C	0x0	VIDEO_INPUT_TO_INT_PD Set an INT Pending when no video input exceeds the setting threshold time
11	R/W1C	0x0	CLR_FRAME_CNT_INT Set a INT When Clear Frame cnt.
10	R/W1C	0x0	SENT_SYNC_INT Set a INT When sent a SYNC signal.
9	R/W1C	0x0	FBC_DATA_WRDDR_FULL_PD Error flag of FBC_DATA_WRDDR_FULL.
8	R/W1C	0x0	FBC_OVHD_WRDDR_FULL_PD Error flag of FBC_OVHD_WRDDR_FULL.
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	HB_OF_PD Hblank FIFO overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R/W1C	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R/W1C	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

8.1.8.19. **CSIC DMA Line Counter Register(Default Value:0x0000_0000)**

Offset: 0x0058			**Register Name: CSIC_DMA_LINE_CNT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

8.1.8.20. **CSIC DMA Frame Counter Register(Default Value:0x0001_0000)**

Offset: 0x005C			Register Name: CSIC_DMA_FRM_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	FRM_CNT_CLR When the bit set to 1,Frame cnt clear to 0
30:16	R/W	0x1	PCLK_DMA_CLR_DISTANCE Frame cnt clear cycle $N*T_{SYNC}$
15:0	R	0x0	FRM_CNT Counter value of frame. When frame done comes, the internal counter value add 1, and when the reg full ,it is cleared to 0 . When parser sent a sync signal,it is cleared to 0.

8.1.8.21. **CSIC DMA Frame Clock Counter Register(Default Value:0x0000_0000)**

Offset: 0x0060			Register Name: CSIC_DMA_FRM_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

8.1.8.22. **CSIC DMA Accumulated and Internal Clock Counter Register(Default Value:0x0000_0000)**

Offset: 0x0064			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/WC	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter.

			When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

8.1.8.23. **CSIC DMA FIFO Statistic Register(Default Value:0x0000_0000)**

Offset: 0x0068			Register Name: CSIC_DMA_FIFO_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	Line Index Indicates the line index in current vsync.
15:13	/	/	/
12:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone.

8.1.8.24. **CSIC DMA FIFO Threshold Register(Default Value:0x0000_0400)**

Offset: 0x006C			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x400	FIFO_THRS When FIFO occupied memory exceed the threshold, dram frequency can not change.

8.1.8.25. **CSIC DMA PCLK Statistic Register(Default Value:0x0000_7FFF)**

Offset: 0x0070			Register Name: CSIC_DMA_PCLK_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x7FFF	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

8.1.8.26. **CSIC DMA BUF Address FIFO0 Entry Register(Default Value:0x0000_0000)**

Offset: 0x0080			Register Name: CSIC_DMA_BUF_ADDR_FIFO0_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO0_ENTRY FIFO Entry of Buffer Address FIFO0 for input frames to be stored, only used in Buffer Addr FIFO Mode

8.1.8.27. **CSIC DMA BUF Address FIFO1 Entry Register(Default Value:0x0000_0000)**

Offset: 0x0084			Register Name: CSIC_DMA_BUF_ADDR_FIFO1_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO1_ENTRY FIFO Entry of Buffer Address FIFO1 for input frames to be stored, only used in Buffer Addr FIFO Mode

8.1.8.28. **CSIC DMA BUF Address FIFO2 Entry Register(Default Value:0x0000_0000)**

Offset: 0x0088			Register Name: CSIC_DMA_BUF_ADDR_FIFO2_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO2_ENTRY FIFO Entry of Buffer Address FIFO2 for input frames to be stored, only used in Buffer Addr FIFO Mode

8.1.8.29. **CSIC DMA BUF Threshold Register(Default Value:0x0020_0000)**

Offset: 0x008C			Register Name: CSIC_DMA_BUF_TH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
21:16	R/W	0x20	CSIC_DMA_STORED_FRM_THRESHOLD when stored frame counter value reaches the threshold , counter is cleared to 0 , only used in Buffer Addr FIFO Mode
15:6	/	/	/
5:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD when content in Buffer Address FIFO less than the threshold, an interrupt is set, only used in Buffer Addr FIFO Mode

8.1.8.30. **CSIC DMA BUF Address FIFO Content Register(Default Value:0x0000_0000)**

Offset: 0x0090			Register Name: CSIC_DMA_BUF_ADDR_FIFO_CON_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:16	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO2_CONTENT FIFO Content of address buffered in Buffer Address FIFO2, only used in Buffer Addr FIFO Mode
15:14	/	/	/
13:8	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO1_CONTENT

			FIFO Content of address buffered in Buffer Address FIFO1, only used in Buffer Addr FIFO Mode
7:6	/	/	/
5:0	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO0_CONTENT FIFO Content of address buffered in Buffer Address FIFO0, only used in Buffer Addr FIFO Mode

8.1.8.31. **CSIC DMA Stored Frame Counter Register(Default Value:0x0000_0000)**

Offset: 0x0094			**Register Name: CSIC_DMA_STORED_FRM_CNT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	RO	0x0	CSIC_DMA_STORED_FRM_CNT Indicates value of stored frames counter, when counter value reaches CSIC_DMA_STORED_FRM_THRESHOLD, counter is cleared to 0, only used in Buffer Addr FIFO Mode

8.1.8.32. **CSIC LBC Configure Register(Default Value:0x8F30_0008)**

Offset: 0x0100			**Register Name: CSIC_LBC_CONFIG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

8.1.8.33. **CSIC LBC Line Target Bit0 Register(Default Value:0x0000_2400)**

Offset: 0x0104			**Register Name: CSIC_LBC_LINE_TAR_BIT0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

8.1.8.34. **CSIC LBC Line Target Bit1 Register(Default Value:0x0000_3600)**

Offset: 0x0108			Register Name: CSIC_LBC_LINE_TAR_BIT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

8.1.8.35. **CSIC LBC RC ADV Register(Default Value:0x1010_1010)**

Offset: 0x010C			Register Name: CSIC_LBC_RC_ADV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x10	Rate control advanture 3
23:16	R/W	0x10	Rate control advanture 2
15:8	R/W	0x10	Rate control advanture 1
7:0	R/W	0x10	Rate control advanture 0

8.1.8.36. **CSIC LBC MB MIN Register(Default Value:0x006E_0037)**

Offset: 0x0110			Register Name: CSIC_LBC_MB_MIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

8.1.8.37. **CSIC DMA Feature List Register(Default Value:0x0000_0003)**

Offset: 0x01F4			Register Name: CSIC_FEATURE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R	0x1	DMA0_EMBEDDED_LBC 0: No Embedded LBC 1: Embedded LBC
0	R	0x1	DMA0_EMBEDDED_FBC 0: No Embedded DMA 1: Embedded FBC

8.1.9. CCI Register Description

8.1.9.1. **CCI Control Register(Default Value:0x00F8_0000)**

Offset: 0x0000	Register Name: CCI_CTRL

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SINGLE_TRAN 0: Transmission idle 1: Start single transmission Automatically cleared to '0' when finished. Abort current transmission immediately if changing from '1' to '0'. If slave not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. PACKET_CNT will return the sequence number when transmission fail. All format setting and data will be loaded from registers and FIFO when transmission start.
30	R/W	0x0	REPEAT_TRAN 0: transmission idle 1: repeated transmission When this bit is set to 1, transmission repeats when trigger signal (such as VSYNC/ VCAP done) repeats. If changing this bit from '1' to '0' during transmission, the current transmission will be guaranteed then stop.
29	R/W	0x0	/
28	R/W	0x0	RESTART_MODE 0: RESTART 1: STOP+START Define the CCI action after sending register address.
27:24	R	0x0	READ_TRAN_MODE 0: send slave_id+W 1: do not send slave_id+W Setting this bit to 1 if reading from a slave which register width is equal to 0.
23:16	R	0xf8	CCI_STA 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9th SCL clk Other: Reserved
15:2	/	/	/
1	R/W	0x0	SOFT_RESET 0: normal 1: reset
0	R/W	0x0	CCI_EN

			0: Module disable 1: Module enable

8.1.9.2. **CCI Transmission Configuration Register(Default Value:0x1000_0000)**

Offset: 0x0004			**Register Name: CCI_CFG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x10	TIMEOUT_N When sending the 9th clock, assert fail signal when slave device did not response after **N*F_{SCL}** cycles. And software must do a reset to CCI module and send a stop condition to slave.
23:16	R/W	0x0	INTERVAL Define the interval between each packet in 40*F_{SCL} cycles. 0~255
15	R/W	0x0	PACKET_MODE Select where to load slave id / data width 0: Compact mode 1: Complete mode In compact mode, slave id/register width / data width will be loaded from CCI_FMT register, only address and data read from memory. In complete mode, they will be loaded from packet memory.
14:7	/	/	/
6:4	R/W	0x0	TRIG_MODE Transmit mode: 000: Immediately, no trigger 001: Reserved 010: CSI0 int trigger 011: CSI1 int trigger
3:0	R/W	0x0	CSI_TRIG CSI Int trig signal select: 0000: First HREF start 0001: Last HREF done 0010: Line counter trigger other: Reserved

8.1.9.3. **CCI Packet Format Register(Default Value:0x0011_0001)**

Offset: 0x0008			**Register Name: CCI_FMT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	R/W	0x0	SLV_ID 7bit address
24	R/W	0x0	CMD 0: write 1: read
23:20	R/W	0x1	ADDR_BYTE

			How many bytes be sent as address 0~15
19:16	R/W	0x1	DATA_BYTE How many bytes be sent/received as data 1~15 Normally use ADDR_DATA with 0_2, 1_1, 1_2, 2_1, 2_2 access mode. If DATA bytes is 0, transmission will not start. In complete mode, the ADDR_BYTE and DATA_BYTE is defined in a byte's high/low 4bit.
15:0	R/W	0x1	PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format. Total bytes not exceed 32bytes.

8.1.9.4. **CCI Bus Control Register(Default Value:0x0000_25C0)**

Offset: 0x000C			**Register Name: CCI_BUS_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	/
15	R/W	0x0	DLY_CYC 0~65535 F_{SCL} cycles between each transmission
14:12	R/W	0x2	DLY_TRIG 0: disable 1: execute transmission after internal counter delay when triggered
11:8	R/W	0x5	CLK_M CCI output SCL frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status
5	R/W	0x0	SCL_PEN SCL PAD enable
4	R/W	0x0	SDA_PEN SDA PAD enable
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output en
0	R/W	0x0	SDA_MOE SDA manual output en

8.1.9.5. **CCI Interrupt Control Register(Default Value:0x0000_0000)**

Offset: 0x0014	**Register Name: CCI_INT_CTRL**

Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	S_TRAN_ERR_INT_EN
16	R/W	0x0	S_TRAN_COM_INT_EN
15:2	/	/	/
1	R/W1C	0x0	S_TRAN_ERR_PD
0	R/W1C	0x0	S_TRAN_COM_PD

8.1.9.6. CCI Line Counter Trigger Control Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: CCI_LC_TRIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LN_CNT 0~8191: line counter send trigger when 1st~8192th line is received.

8.1.9.7. CCI FIFO Access Register(Default Value:0x0000_0000)

Offset: 0x0100~0x013F			Register Name: CCI_FIFO_ACC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DATA_FIFO From 0x100 to 0x13f, CCI data fifo is 64bytes, used in fifo input mode. CCI transmission read/write data from/to fifo in byte.

8.1.9.8. CCI Reserved Register(Default Value:0x0000_0000)

Offset: 0x0200~0x0220			Register Name: CCI_RSV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	/	From 0x200 to 0x220 address, normal TWI registers are copied here. All transmission will be act like hardware controlling these registers. And don't change them in transmission.

Chapter 9 Combo Rx

9.1. Combo Rx

9.1.1. Overview

The Combo RX Interface Specification defines protocols between a host processor and peripheral devices that adhere to MIPI interfaces,Sub-LVDS interface, HiSPI interface and CMOS interface. The IP is Multi PHY. The Combo RX defines in the document is consists of Combo-PHY and Combo-Controller.

Feature:

MIPI Interface:

- Supports MIPI DPHY V1.1,MIPI CSI2 V1.1
- Supports MIPI 4 lane,up to 1.0Gbps/Lane
- Supports RAW8/10/12 YUV422,yuv420 data formats
- Supports Pixel to byte packing
- Supports Low Level Protocol,short packet,long packet,ECC and Check Sum
- Supports Virtual Channel Identifier
- Supports WDR/HDR(line by line),Supports VC,DOL WDR mode

Sub-LVDS Interface:

- Supports 1 clock 12 lane,up to 650Mbps/lane
- Supports 1 clock 4 lane,up to 1.0Gbps/lane
- Supports Pixel to byte packing
- Supports Generic Sync Format
- Supports WDR/HDR(line by line),Supports three modes as follow:
  - Mode 1:SOF-EOF, short and long exposure separate by synchronization code
  - Mode2:SAV-EAV,4 fields DOL mode
  - Mode3:SAV-EAV,5 fields DOL mode

HiSPi Interface:

- Supports 1 clock 4 lane,up to 1Gbps/lane
- Supports Pixel to byte packing
- Supports Generic Sync Format
- Supports SLVS-400,HiVCM Electrical characteristics
- Supports WDR/HDR(line by line)

9.1.2. Combo Rx Register List

Module Name	Base Address
CSIC_COMBO0	0x0660C000

Register Name	Offset	Description
CMB_MODE_SEL_REG	0x000	Combo Mode Select
CMB_APP_PIXEL_OUT_REG	0x004	Combo Application Pixel Out Select
CMB_MIPI_DPHY_CTR_REG	0x008	Combo MIPI DPHY Controller
CMB_MIPI_DPHY_LANE_MAPPING_REG	0x00C	Combo MIPI DPHY Lane Mapping
CMB_CSI2_STATUS_REG	0x100	Combo MIPI CSI2 Status
CMB_MIPI_CSI2_DATA_ID_REG	0x104	Combo MIPI CSI2 DATA ID
CMB_MIPI_CSI2_WORD_CNT_REG	0x108	Combo MIPI CSI2 Word Counter
CMB_MIPI_CSI2_ECC_VAL_REG	0x10C	Combo MIPI CSI2 ECC Value
CMB_MIPI_CSI2_LINE_LENTGH_REG	0x110	Combo MIPI CSI2 Line LENTGH
CMB_MIPI_CSI2_RCV_CNT_REG	0x114	Combo MIPI CSI2 Receive Counter
CMB_MIPI_CSI2_ECC_ERR_CNT_REG	0x118	Combo MIPI CSI2 ECC Error Counter
CMB_MIPI_CSI2_CHECK_SUM_ERR_REG	0x11C	Combo MIPI CSI2 Check Sum Error
CMB_LVDS_CTR_REG	0x200	Combo LVDS Controller
CMB_LVDS_LANE_MAPPING0_REG	0x204	Combo LVDS Lane Mapping
CMB_LVDS_LANE_MAPPING1_REG	0x208	Combo LVDS Lane Mapping
CMB_LVDS_LANE_MAPPING2_REG	0x20C	Combo LVDS Lane Mapping
CMB_LVDS_LANE0_SOF_SET0_REG	0x210	Combo LVDS Configure Sync Code
CMB_LVDS_LANE0_SOF_SET1_REG	0x214	Combo LVDS Configure Sync Code
CMB_LVDS_LANE0_SOL_SET0_REG	0x218	Combo LVDS Configure Sync Code
CMB_LVDS_LANE0_SOL_SET1_REG	0x21C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE0_EOL_SET0_REG	0x220	Combo LVDS Configure Sync Code
CMB_LVDS_LANE0_EOL_SET1_REG	0x224	Combo LVDS Configure Sync Code
CMB_LVDS_LANE0_EOF_SET0_REG	0x228	Combo LVDS Configure Sync Code
CMB_LVDS_LANE0_EOF_SET1_REG	0x22C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE1_SOF_SET0_REG	0x230	Combo LVDS Configure Sync Code
CMB_LVDS_LANE1_SOF_SET1_REG	0x234	Combo LVDS Configure Sync Code
CMB_LVDS_LANE1_SOL_SET0_REG	0x238	Combo LVDS Configure Sync Code
CMB_LVDS_LANE1_SOL_SET1_REG	0x23C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE1_EOL_SET0_REG	0x240	Combo LVDS Configure Sync Code
CMB_LVDS_LANE1_EOL_SET1_REG	0x244	Combo LVDS Configure Sync Code
CMB_LVDS_LANE1_EOF_SET0_REG	0x248	Combo LVDS Configure Sync Code
CMB_LVDS_LANE1_EOF_SET1_REG	0x24C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE2_SOF_SET0_REG	0x250	Combo LVDS Configure Sync Code
CMB_LVDS_LANE2_SOF_SET1_REG	0x254	Combo LVDS Configure Sync Code
CMB_LVDS_LANE2_SOL_SET0_REG	0x258	Combo LVDS Configure Sync Code
CMB_LVDS_LANE2_SOL_SET1_REG	0x25C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE2_EOL_SET0_REG	0x260	Combo LVDS Configure Sync Code
CMB_LVDS_LANE2_EOL_SET1_REG	0x264	Combo LVDS Configure Sync Code
CMB_LVDS_LANE2_EOF_SET0_REG	0x268	Combo LVDS Configure Sync Code

CMB_LVDS_LANE2_EOF_SET1_REG	0x26C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE3_SOF_SET0_REG	0x270	Combo LVDS Configure Sync Code
CMB_LVDS_LANE3_SOF_SET1_REG	0x274	Combo LVDS Configure Sync Code
CMB_LVDS_LANE3_SOL_SET0_REG	0x278	Combo LVDS Configure Sync Code
CMB_LVDS_LANE3_SOL_SET1_REG	0x27C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE3_EOL_SET0_REG	0x280	Combo LVDS Configure Sync Code
CMB_LVDS_LANE3_EOL_SET1_REG	0x284	Combo LVDS Configure Sync Code
CMB_LVDS_LANE3_EOF_SET0_REG	0x288	Combo LVDS Configure Sync Code
CMB_LVDS_LANE3_EOF_SET1_REG	0x28C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE4_SOF_SET0_REG	0x290	Combo LVDS Configure Sync Code
CMB_LVDS_LANE4_SOF_SET1_REG	0x294	Combo LVDS Configure Sync Code
CMB_LVDS_LANE4_SOL_SET0_REG	0x298	Combo LVDS Configure Sync Code
CMB_LVDS_LANE4_SOL_SET1_REG	0x29C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE4_EOL_SET0_REG	0x2A0	Combo LVDS Configure Sync Code
CMB_LVDS_LANE4_EOL_SET1_REG	0x2A4	Combo LVDS Configure Sync Code
CMB_LVDS_LANE4_EOF_SET0_REG	0x2A8	Combo LVDS Configure Sync Code
CMB_LVDS_LANE4_EOF_SET1_REG	0x2AC	Combo LVDS Configure Sync Code
CMB_LVDS_LANE5_SOF_SET0_REG	0x2B0	Combo LVDS Configure Sync Code
CMB_LVDS_LANE5_SOF_SET1_REG	0x2B4	Combo LVDS Configure Sync Code
CMB_LVDS_LANE5_SOL_SET0_REG	0x2B8	Combo LVDS Configure Sync Code
CMB_LVDS_LANE5_SOL_SET1_REG	0x2BC	Combo LVDS Configure Sync Code
CMB_LVDS_LANE5_EOL_SET0_REG	0x2C0	Combo LVDS Configure Sync Code
CMB_LVDS_LANE5_EOL_SET1_REG	0x2C4	Combo LVDS Configure Sync Code
CMB_LVDS_LANE5_EOF_SET0_REG	0x2C8	Combo LVDS Configure Sync Code
CMB_LVDS_LANE5_EOF_SET1_REG	0x2CC	Combo LVDS Configure Sync Code
CMB_LVDS_LANE6_SOF_SET0_REG	0x2D0	Combo LVDS Configure Sync Code
CMB_LVDS_LANE6_SOF_SET1_REG	0x2D4	Combo LVDS Configure Sync Code
CMB_LVDS_LANE6_SOL_SET0_REG	0x2D8	Combo LVDS Configure Sync Code
CMB_LVDS_LANE6_SOL_SET1_REG	0x2DC	Combo LVDS Configure Sync Code
CMB_LVDS_LANE6_EOL_SET0_REG	0x2E0	Combo LVDS Configure Sync Code
CMB_LVDS_LANE6_EOL_SET1_REG	0x2E4	Combo LVDS Configure Sync Code
CMB_LVDS_LANE6_EOF_SET0_REG	0x2E8	Combo LVDS Configure Sync Code
CMB_LVDS_LANE6_EOF_SET1_REG	0x2EC	Combo LVDS Configure Sync Code
CMB_LVDS_LANE7_SOF_SET0_REG	0x2F0	Combo LVDS Configure Sync Code
CMB_LVDS_LANE7_SOF_SET1_REG	0x2F4	Combo LVDS Configure Sync Code
CMB_LVDS_LANE7_SOL_SET0_REG	0x2F8	Combo LVDS Configure Sync Code
CMB_LVDS_LANE7_SOL_SET1_REG	0x2FC	Combo LVDS Configure Sync Code
CMB_LVDS_LANE7_EOL_SET0_REG	0x300	Combo LVDS Configure Sync Code
CMB_LVDS_LANE7_EOL_SET1_REG	0x304	Combo LVDS Configure Sync Code
CMB_LVDS_LANE7_EOF_SET0_REG	0x308	Combo LVDS Configure Sync Code
CMB_LVDS_LANE7_EOF_SET1_REG	0x30C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE8_SOF_SET0_REG	0x310	Combo LVDS Configure Sync Code
CMB_LVDS_LANE8_SOF_SET1_REG	0x314	Combo LVDS Configure Sync Code
CMB_LVDS_LANE8_SOL_SET0_REG	0x318	Combo LVDS Configure Sync Code
CMB_LVDS_LANE8_SOL_SET1_REG	0x31C	Combo LVDS Configure Sync Code

CMB_LVDS_LANE8_EOL_SET0_REG	0x320	Combo LVDS Configure Sync Code
CMB_LVDS_LANE8_EOL_SET1_REG	0x324	Combo LVDS Configure Sync Code
CMB_LVDS_LANE8_EOF_SET0_REG	0x328	Combo LVDS Configure Sync Code
CMB_LVDS_LANE8_EOF_SET1_REG	0x32C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE9_SOF_SET0_REG	0x330	Combo LVDS Configure Sync Code
CMB_LVDS_LANE9_SOF_SET1_REG	0x334	Combo LVDS Configure Sync Code
CMB_LVDS_LANE9_SOL_SET0_REG	0x338	Combo LVDS Configure Sync Code
CMB_LVDS_LANE9_SOL_SET1_REG	0x33C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE9_EOL_SET0_REG	0x340	Combo LVDS Configure Sync Code
CMB_LVDS_LANE9_EOL_SET1_REG	0x344	Combo LVDS Configure Sync Code
CMB_LVDS_LANE9_EOF_SET0_REG	0x348	Combo LVDS Configure Sync Code
CMB_LVDS_LANE9_EOF_SET1_REG	0x34C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE10_SOF_SET0_REG	0x350	Combo LVDS Configure Sync Code
CMB_LVDS_LANE10_SOF_SET1_REG	0x354	Combo LVDS Configure Sync Code
CMB_LVDS_LANE10_SOL_SET0_REG	0x358	Combo LVDS Configure Sync Code
CMB_LVDS_LANE10_SOL_SET1_REG	0x35C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE10_EOL_SET0_REG	0x360	Combo LVDS Configure Sync Code
CMB_LVDS_LANE10_EOL_SET1_REG	0x364	Combo LVDS Configure Sync Code
CMB_LVDS_LANE10_EOF_SET0_REG	0x368	Combo LVDS Configure Sync Code
CMB_LVDS_LANE10_EOF_SET1_REG	0x36C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE11_SOF_SET0_REG	0x370	Combo LVDS Configure Sync Code
CMB_LVDS_LANE11_SOF_SET1_REG	0x374	Combo LVDS Configure Sync Code
CMB_LVDS_LANE11_SOL_SET0_REG	0x378	Combo LVDS Configure Sync Code
CMB_LVDS_LANE11_SOL_SET1_REG	0x37C	Combo LVDS Configure Sync Code
CMB_LVDS_LANE11_EOL_SET0_REG	0x380	Combo LVDS Configure Sync Code
CMB_LVDS_LANE11_EOL_SET1_REG	0x384	Combo LVDS Configure Sync Code
CMB_LVDS_LANE11_EOF_SET0_REG	0x388	Combo LVDS Configure Sync Code
CMB_LVDS_LANE11_EOF_SET1_REG	0x38C	Combo LVDS Configure Sync Code
CMB_HISPI_CTR_REG	0x390	Combo HISPI Control
CMB_HISPI_SYNC_CODE_REG	0x394	Combo HISPI Sync code set
CMB_HISPI_CODE_MASK_REG	0x398	Combo HISPI Sync code mask
CMB_PHYA_LANE_EN_REG	0xE00	Combo PHYA LANE Enable
CMB_PHYA_CTR_REG	0xE04	Combo PHYA Control
CMB_PHYA_DLY_CTR0_REG	0xE08	Combo PHYA LANE Delay
CMB_PHYA_DLY_CTR1_REG	0xE0C	Combo PHYA LANE Delay
CMB_PHYA_DLY_CTR2_REG	0xE10	Combo PHYA LANE Delay
CMB_PHYA_CFG_REG	0xE14	Combo PHYA Configure Mode

9.1.3. Combo Rx Register Description

9.1.3.1. **CMB_MODE_SEL_REG (Default Value:0x0000_0000)**

Offset:0x000			**Register Name: CMB_MODE_SEL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:28	R/W	0x0	WDR_FIDMAP_SEL_3 Word 4th bit Number for FIDMAP[3]
27:24	R/W	0x0	WDR_FIDMAP_SEL_2 Word 4th bit Number for FIDMAP[2]
23:20	R/W	0x0	WDR_FIDMAP_SEL_1 Word 4th bit Number for FIDMAP[1]
19:16	R/W	0x0	WDR_FIDMAP_SEL_0 Word 4th bit Number for FIDMAP[0]
15:12	R/W	0x0	WDR_FIDMAP_SEL_EN FID output Mapping from Word 4th Enable Bit[12]:FID_OUT0 0: OFF default:MIPI-CSI2 VC[0] 1: ON :MODE_LBL_FIDMAP_SEL_0 Bit[13]:FID_OUT1 0: OFF default:MIPI-CSI2 VC[0] 1: ON :MODE_LBL_FIDMAP_SEL_1 Bit[14]:FID_OUT2 0: OFF default:MIPI-CSI2 VC[0] 1: ON :MODE_LBL_FIDMAP_SEL_2 Bit[15]:FID_OUT3 0: OFF default:MIPI-CSI2 VC[0] 1: ON :MODE_LBL_FIDMAP_SEL_3
11	R/W	0x0	FID_MODE_SEL When in WDR mode ,sometime use single bit indicate long/short frame ID(Such as SONY),sometime use two bits indicate long/short Frame ID.(such as MNXXXX,SONY) 0: single bit indicate Frame ID 1: two bits indicate Frame ID
10	/	/	/
9:8	R/W	0x0	WDR_MODE_SEL (LBL) Operation WDR Mode Control 0: Normal Operation 1: HDR/WDR Index on SYNC CODE 2: HDR/WDR Index on Pixel Data Others:reserved
7	R/W	0x0	EMBD_DAT_OUT_EN Output the embedded data enable (DT ID = 0x12) 0: Not receiving the embedded data 1: Receiving the embedded data
6:1	/	/	/
0	R/W	0x0	MODULE_EN 0: disable 1: enable When it's disabled, the module will be reset to idle state.

9.1.3.2. **CMB_APP_PIXEL_OUT_REG(Default Value: 0x0000_0000)**

Offset:0x004			Register Name: CMB_APP_PIXEL_OUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	APP_PIXEL_OUT_SEL Application layer output pixel data parallel out setting 0: 1 Pixel Out 1: 2 Pixel Out 2: 4 Pixel Out 3: 8 Pixel Out

9.1.3.3. **CMB_MIPI_DPHY_CTR_REG(Default Value: 0x0000_0400)**

Offset:0x008			Register Name: CMB_MIPI_DPHY_CTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	DPHY_P0_TIME_RES_ON When HS_DLY_OFF set 0,add (DPHY_P0_TIME_RES_ON + 1) cycles delay time for turning on RES.
23:16	R/W	0x0	DPHY_P0_TIME_HS_ON When HS_DLY_OFF set 0,add (DPHY_P0_TIME_RES_ON+ DPHY_P0_TIME_HS_ON +1) cycles delay time for turning on HS Comparator.
15:11	R/W	0x0	DPHY_P0_TIME_DT_ON When HS_DLY_OFF set 0,add (DPHY_P0_TIME_RES_ON+ DPHY_P0_TIME_HS_ON + DPHY_P0_TIME_DT_ON + 1) cycles delay time for receiving HS Data.
10	R/W	0x1	HS_DLY_OFF When set 1,disable HS mode delay time.
9	R/W	0x0	DPHY_LP_MODE_CTR 0: LP Operation ON 1: LP Operation OFF
8	R/W	0x0	DPHY_MSB_FIRST_SEL 0: Parallel Data LSB first in from PHY Analog Layer 1: Parallel Data MSB first in from PHY Analog Layer
7:6	/	/	/
5:4	R/W	0x0	DPHY_LANE_NUM 0: 1 lane mode 1: 2 lane mode 2: 3 lane mode 3: 4 lane mode
3:2	/	/	/
1:0	R/W	0x0	DPHY_CLK_SEL 0: use clock0 from PHYA Analog layer 1: use clock1 from PHYA Analog layer 2: use clock2 from PHYA Analog layer

			3: use clock3 from PHYA Analog layer

9.1.3.4. CMB_MIPI_DPHY_LANE_MAPPING_REG(Default Value: 0x0000_0000)

Offset:0x00C			Register Name: CMB_MIPI_DPHY_LANE_MAPPING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	DPHY_INTERNAL_LANE3 0: use PAD Lane0 to internal lane 3 1: use PAD Lane1 to internal lane 3 2: use PAD Lane2 to internal lane 3 3: use PAD Lane3 to internal lane 3
11:10	/	/	/
9:8	R/W	0x0	DPHY_INTERNAL_LANE2 0: use PAD Lane0 to internal lane 2 1: use PAD Lane1 to internal lane 2 2: use PAD Lane2 to internal lane 2 3: use PAD Lane3 to internal lane 2
7:6	/	/	/
5:4	R/W	0x0	DPHY_INTERNAL_LANE1 0: use PAD Lane0 to internal lane 1 1: use PAD Lane1 to internal lane 1 2: use PAD Lane2 to internal lane 1 3: use PAD Lane3 to internal lane 1
3:2	/	/	/
1:0	R/W	0x0	DPHY_INTERNAL_LANE0 0: use PAD Lane0 to internal lane 0 1: use PAD Lane1 to internal lane 0 2: use PAD Lane2 to internal lane 0 3: use PAD Lane3 to internal lane 0

9.1.3.5. CMB_MIPI_VMODE_REG(Default Value: 0x0000_0000)

Offset:0x010			Register Name: CMB_MIPI_VMODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	MIPI_VMODE When works in one channel,this bit set 0; Set 1 when works in multi-channel. 0: one channel mode 1: multi-channel

9.1.3.6. **CMB_MIPI_VC0_HIGHT_REG(Default Value: 0x0000_0000)**

Offset:0x014			Register Name: CMB_MIPI_VC0_HEIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	MIPI_VC0_HIGHT When the MIPI_VMODE bit set '1',these bits must be set ver len in channel 0.

9.1.3.7. **CMB_MIPI_VC1_HIGHT_REG(Default Value: 0x0000_0000)**

Offset:0x018			Register Name: CMB_MIPI_VC1_HEIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	MIPI_VC1_HIGHT When the MIPI_VMODE bit set '1',these bits must be set ver len in channel 1.

9.1.3.8. **CMB_MIPI_VC2_HIGHT_REG(Default Value: 0x0000_0000)**

Offset:0x01C			Register Name: CMB_MIPI_VC2_HEIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	MIPI_VC2_HIGHT When the MIPI_VMODE bit set '1',these bits must be set ver len in channel 2.

9.1.3.9. **CMB_MIPI_VC3_HIGHT_REG(Default Value: 0x0000_0000)**

Offset:0x020			Register Name: CMB_MIPI_VC3_HEIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	MIPI_VC3_HIGHT When the MIPI_VMODE bit set '1',these bits must be set ver len in channel 3.

9.1.3.10. **CMB_MIPI_CSI2_STATUS_REG(Default Value: 0x0000_0000)**

Offset:0x100			Register Name: CMB_CSI2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	MIPI_CSI2_PAYLOAD_STATUS

			0: HS code detect wait 1: Packet Header Analysis 2: Calculation Line Length 3: Burst Transmit 4: Packet Done Others:reserved

9.1.3.11. **CMB_MIPI_CSI2_DATA_ID_REG(Default Value: 0x0000_0000)**

Offset:0x104			**Register Name: CMB_MIPI_CSI2_DATA_ID_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	MIPI_CSI2_DATA_ID

9.1.3.12. **CMB_MIPI_CSI2_WORD_CNT_REG(Default Value: 0x0000_0000)**

Offset:0x108			**Register Name: CMB_MIPI_CSI2_WORD_CNT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	MIPI_CSI2_WORD_CNT

9.1.3.13. **CMB_MIPI_CSI2_ECC_VAL_REG(Default Value: 0x0000_0000)**

Offset:0x10C			**Register Name: CMB_MIPI_CSI2_ECC_VAL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	MIPI_CSI2_ECC_VAL

9.1.3.14. **CMB_MIPI_CSI2_LINE_LENTGH_REG(Default Value: 0x0000_0000)**

Offset:0x110			**Register Name: CMB_MIPI_CSI2_LINE_LENTGH_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	MIPI_CSI2_LINE_LENTGH

9.1.3.15. **CMB_MIPI_CSI2_RCV_CNT_REG(Default Value: 0x0000_0000)**

Offset:0x114			**Register Name: CMB_MIPI_CSI2_RCV_CNT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	MIPI_CSI2_RCV_CNT

9.1.3.16. **CMB_MIPI_CSI2_ECC_ERR_CNT_REG(Default Value: 0x0000_0000)**

Offset:0x118			Register Name: CMB_MIPI_CSI2_ECC_ERR_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	MIPI_CSI2_ECC_ERR_CNT_CNT

9.1.3.17. **CMB_MIPI_CSI2_CHECK_SUM_ERR_CNT_REG(Default Value: 0x0000_0000)**

Offset:0x11C			Register Name: CMB_MIPI_CSI2_CHECK_SUM_ERR_REG
Bit	**Read/Write**	**Bit**	**Read/Write**
31:16	/	31:16	/
15:0	R	15:0	R

9.1.3.18. **CMB_LVDS_CTR_REG(Default Value: 0x0000_0000)**

Offset:0x200			Register Name: CMB_LVDS_CTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LVDS_SYNC_CODE_WD4_SEL Sub-LVDS SYNC CODE 4th Output Mode Select lane Number
27	/	/	/
26:24	R/W	0x0	LVDS_SYNC_CODE_LINE_CNT Frame Valid of SOF Count Number Only use in Sub-lvds WDR mode of SONY Sensors. When the first Long frame finished,the internal Frame valid signal will go down.To receive the whole short frame,the internal Frame valid signal must not go down,so set LVDS_SYNC_CODE_LINE_CNT≥2 can extent the Frame valid signal.
23:22	/	/	/
21	R/W	0x0	LVDS_PIX_LSB Sub-LVDS Convert Pixel Component 0: OFF : MSB (Default) 1: ON : LSB
20	R/W	0x0	LVDS_SYNC_LINE_CODE_MODE_SEL(linea) 0: Normal SOF/SOL/EOL/EOF 1: Valid(SOL/EOL) or Invalid(SOF/EOF) For SONY
19	/	/	/
18:16	R/W	0x0	LVDS_BIT_WIDTH_SEL 0: RAW8 1: RAW10 2: RAW12 3: RAW14

			4: RAW16 Others:reserved
15:13	/	/	/
12	R/W	0x0	LVDS_MODE_SEL 0: Serial Mode 1: Parallel Mode
11:8	R/W	0x0	LVDS_LANE_NUM 2: 2 data lane 4: 4 data lane 8: 8 data lane 10: 10 data lane 12: 12 data lane others:reserved In WDR(4 or 5 code) mode,'8 data lane' indicate cut 8 pixel data with the ID information,others(2/4/6/10/12) just cut 4 pixel data.
7:6	/	/	/
5	R/W	0x0	LVDS_MSB_FIRST_SEL 0: Parallel Data LSB first in from PHY Analog Layer 1: Parallel Data MSB first in from PHY Analog Layer
4	R/W	0x0	LVDS_REC_DIRECT 0: use Normal Parallel Pass 1: use Receiver Direct(only TEG chip and FPGA combination)
3:0	R/W	0x0	LVDS_CLK_SEL 0: use clock0 from PHYA(Analog layer) 1: use clock1 from PHYA Analog layer 2: use clock2 from PHYA Analog layer 3: use clock3 from PHYA Analog layer 4: use clock4 from PHYA Analog layer 5: use clock5 from PHYA Analog layer 6: use clock6 from PHYA Analog layer 7: use clock7 from PHYA Analog layer 8: use clock8 from PHYA Analog layer 9: use clock9 from PHYA Analog layer 10: use clock10 from PHYA Analog layer 11: use clock11 from PHYA Analog layer

9.1.3.19. **CMB_LVDS_LANE_MAPPING0_REG(Default Value: 0x0000_0000)**

Offset:0x204			**Register Name: CMB_LVDS_LANE_MAPPING0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	LVDS_LANE3_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane3 2: use PAD Lane 1 to Internal Lane3

			3: use PAD Lane 2 to Internal Lane3 4: use PAD Lane 3 to Internal Lane3 5: use PAD Lane 4 to Internal Lane3 6: use PAD Lane 5 to Internal Lane3 7: use PAD Lane 6 to Internal Lane3 8: use PAD Lane 7 to Internal Lane3 9: use PAD Lane 8 to Internal Lane3 10: use PAD Lane 9 to Internal Lane3 11: use PAD Lane 10 to Internal Lane3 12: use PAD Lane 11 to Internal Lane3
23:20	/	/	/
19:16	R/W	0x0	LVDS_LANE2_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane2 2: use PAD Lane 1 to Internal Lane2 3: use PAD Lane 2 to Internal Lane2 4: use PAD Lane 3 to Internal Lane2 5: use PAD Lane 4 to Internal Lane2 6: use PAD Lane 5 to Internal Lane2 7: use PAD Lane 6 to Internal Lane2 8: use PAD Lane 7 to Internal Lane2 9: use PAD Lane 8 to Internal Lane2 10: use PAD Lane 9 to Internal Lane2 11: use PAD Lane 10 to Internal Lane2 12: use PAD Lane 11 to Internal Lane2
15:12	/	/	/
11:8	R/W	0x0	LVDS_LANE1_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane1 2: use PAD Lane 1 to Internal Lane1 3: use PAD Lane 2 to Internal Lane1 4: use PAD Lane 3 to Internal Lane1 5: use PAD Lane 4 to Internal Lane1 6: use PAD Lane 5 to Internal Lane1 7: use PAD Lane 6 to Internal Lane1 8: use PAD Lane 7 to Internal Lane1 9: use PAD Lane 8 to Internal Lane1 10: use PAD Lane 9 to Internal Lane1 11: use PAD Lane 10 to Internal Lane1 12: use PAD Lane 11 to Internal Lane1
7:4	/	/	/
3:0	R/W	0x0	LVDS_LANE0_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane0 2: use PAD Lane 1 to Internal Lane0 3: use PAD Lane 2 to Internal Lane0

			4: use PAD Lane 3 to Internal Lane0 5: use PAD Lane 4 to Internal Lane0 6: use PAD Lane 5 to Internal Lane0 7: use PAD Lane 6 to Internal Lane0 8: use PAD Lane 7 to Internal Lane0 9: use PAD Lane 8 to Internal Lane0 10: use PAD Lane 9 to Internal Lane0 11: use PAD Lane 10 to Internal Lane0 12: use PAD Lane 11 to Internal Lane0

9.1.3.20. **CMB_LVDS_LANE_MAPPING1_REG(Default Value: 0x0000_0000)**

Offset:0x208			**Register Name: CMB_LVDS_LANE_MAPPING1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	LVDS_LANE7_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane7 2: use PAD Lane 1 to Internal Lane7 3: use PAD Lane 2 to Internal Lane7 4: use PAD Lane 3 to Internal Lane7 5: use PAD Lane 4 to Internal Lane7 6: use PAD Lane 5 to Internal Lane7 7: use PAD Lane 6 to Internal Lane7 8: use PAD Lane 7 to Internal Lane7 9: use PAD Lane 8 to Internal Lane7 10: use PAD Lane 9 to Internal Lane7 11: use PAD Lane 10 to Internal Lane7 12: use PAD Lane 11 to Internal Lane7
23:20	/	/	/
19:16	R/W	0x0	LVDS_LANE6_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane6 2: use PAD Lane 1 to Internal Lane6 3: use PAD Lane 2 to Internal Lane6 4: use PAD Lane 3 to Internal Lane6 5: use PAD Lane 4 to Internal Lane6 6: use PAD Lane 5 to Internal Lane6 7: use PAD Lane 6 to Internal Lane6 8: use PAD Lane 7 to Internal Lane6 9: use PAD Lane 8 to Internal Lane6 10: use PAD Lane 9 to Internal Lane6 11: use PAD Lane 10 to Internal Lane6 12: use PAD Lane 11 to Internal Lane6
15:12	/	/	/

11:8	R/W	0x0	LVDS_LANE5_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane5 2: use PAD Lane 1 to Internal Lane5 3: use PAD Lane 2 to Internal Lane5 4: use PAD Lane 3 to Internal Lane5 5: use PAD Lane 4 to Internal Lane5 6: use PAD Lane 5 to Internal Lane5 7: use PAD Lane 6 to Internal Lane5 8: use PAD Lane 7 to Internal Lane5 9: use PAD Lane 8 to Internal Lane5 10: use PAD Lane 9 to Internal Lane5 11: use PAD Lane 10 to Internal Lane5 12: use PAD Lane 11 to Internal Lane5
7:4	/	/	/
3:0	R/W	0x0	LVDS_LANE4_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane4 2: use PAD Lane 1 to Internal Lane4 3: use PAD Lane 2 to Internal Lane4 4: use PAD Lane 3 to Internal Lane4 5: use PAD Lane 4 to Internal Lane4 6: use PAD Lane 5 to Internal Lane4 7: use PAD Lane 6 to Internal Lane4 8: use PAD Lane 7 to Internal Lane4 9: use PAD Lane 8 to Internal Lane4 10: use PAD Lane 9 to Internal Lane4 11: use PAD Lane 10 to Internal Lane4 12: use PAD Lane 11 to Internal Lane4

9.1.3.21. **CMB_LVDS_LANE_MAPPING2_REG(Default Value: 0x0000_0000)**

Offset:0x20C			**Register Name: CMB_LVDS_LANE_MAPPING2_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	LVDS_LANE11_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane11 2: use PAD Lane 1 to Internal Lane11 3: use PAD Lane 2 to Internal Lane11 4: use PAD Lane 3 to Internal Lane11 5: use PAD Lane 4 to Internal Lane11 6: use PAD Lane 5 to Internal Lane11 7: use PAD Lane 6 to Internal Lane11 8: use PAD Lane 7 to Internal Lane11

			9: use PAD Lane 8 to Internal Lane11 10: use PAD Lane 9 to Internal Lane11 11: use PAD Lane 10 to Internal Lane11 12: use PAD Lane 11 to Internal Lane11
23:20	/	/	/
19:16	R/W	0x0	LVDS_LANE10_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane10 2: use PAD Lane 1 to Internal Lane10 3: use PAD Lane 2 to Internal Lane10 4: use PAD Lane 3 to Internal Lane10 5: use PAD Lane 4 to Internal Lane10 6: use PAD Lane 5 to Internal Lane10 7: use PAD Lane 6 to Internal Lane10 8: use PAD Lane 7 to Internal Lane10 9: use PAD Lane 8 to Internal Lane10 10: use PAD Lane 9 to Internal Lane10 11: use PAD Lane 10 to Internal Lane10 12: use PAD Lane 11 to Internal Lane10
15:12	/	/	/
11:8	R/W	0x0	LVDS_LANE9_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane9 2: use PAD Lane 1 to Internal Lane9 3: use PAD Lane 2 to Internal Lane9 4: use PAD Lane 3 to Internal Lane9 5: use PAD Lane 4 to Internal Lane9 6: use PAD Lane 5 to Internal Lane9 7: use PAD Lane 6 to Internal Lane9 8: use PAD Lane 7 to Internal Lane9 9: use PAD Lane 8 to Internal Lane9 10: use PAD Lane 9 to Internal Lane9 11: use PAD Lane 10 to Internal Lane9 12: use PAD Lane 11 to Internal Lane9
7:4	/	/	/
3:0	R/W	0x0	LVDS_LANE8_MAPPING 0: Don't use Lane 1: use PAD Lane 0 to Internal Lane8 2: use PAD Lane 1 to Internal Lane8 3: use PAD Lane 2 to Internal Lane8 4: use PAD Lane 3 to Internal Lane8 5: use PAD Lane 4 to Internal Lane8 6: use PAD Lane 5 to Internal Lane8 7: use PAD Lane 6 to Internal Lane8 8: use PAD Lane 7 to Internal Lane8 9: use PAD Lane 8 to Internal Lane8

			10: use PAD Lane 9 to Internal Lane8 11: use PAD Lane 10 to Internal Lane8 12: use PAD Lane 11 to Internal Lane8

9.1.3.22. **CMB_LVDS_LANE0_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x210			Register Name: CMB_LVDS_LANE0_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE0_SOF_SET0 LVDS SOF Code Setting LANE0. This is low 32bit.

9.1.3.23. **CMB_LVDS_LANE0_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x214			Register Name: CMB_LVDS_LANE0_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE0_SOF_SET1 LVDS SOF Code Setting LANE0. This is high 32bit.

9.1.3.24. **CMB_LVDS_LANE0_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x218			Register Name: CMB_LVDS_LANE0_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE0_SOL_SET0 LVDS SOL Code Setting LANE0. This is low 32bit.

9.1.3.25. **CMB_LVDS_LANE0_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x21C			Register Name: CMB_LVDS_LANE0_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE0_SOL_SET1 LVDS SOL Code Setting LANE0. This is high 32bit.

9.1.3.26. **CMB_LVDS_LANE0_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x220			Register Name: CMB_LVDS_LANE0_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE0_EOL_SET0

			LVDS EOL Code Setting LANE0. This is low 32bit.

9.1.3.27. **CMB_LVDS_LANE0_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x224			Register Name: CMB_LVDS_LANE0_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE0_EOL_SET1 LVDS EOL Code Setting LANE0. This is high 32bit.

9.1.3.28. **CMB_LVDS_LANE0_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x228			Register Name: CMB_LVDS_LANE0_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE0_EOF_SET0 LVDS EOF Code Setting LANE0. This is low 32bit.

9.1.3.29. **CMB_LVDS_LANE0_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x22C			Register Name: CMB_LVDS_LANE0_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE0_EOF_SET1 LVDS EOF Code Setting LANE0. This is high 32bit.

9.1.3.30. **CMB_LVDS_LANE1_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x230			Register Name: CMB_LVDS_LANE1_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE1_SOF_SET0 LVDS SOF Code Setting LANE1. This is low 32bit.

9.1.3.31. **CMB_LVDS_LANE1_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x234			Register Name: CMB_LVDS_LANE1_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE1_SOF_SET1 LVDS SOF Code Setting LANE1.

			This is high 32bit.

9.1.3.32. **CMB_LVDS_LANE1_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x238			Register Name: CMB_LVDS_LANE1_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE1_SOL_SET0 LVDS SOL Code Setting LANE1. This is low 32bit.

9.1.3.33. **CMB_LVDS_LANE1_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x23C			Register Name: CMB_LVDS_LANE1_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE1_SOL_SET1 LVDS SOL Code Setting LANE1. This is high 32bit.

9.1.3.34. **CMB_LVDS_LANE1_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x240			Register Name: CMB_LVDS_LANE1_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE1_EOL_SET0 LVDS EOL Code Setting LANE1. This is low 32bit.

9.1.3.35. **CMB_LVDS_LANE1_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x244			Register Name: CMB_LVDS_LANE1_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE1_EOL_SET1 LVDS EOL Code Setting LANE1. This is high 32bit.

9.1.3.36. **CMB_LVDS_LANE1_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x248			Register Name: CMB_LVDS_LANE1_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE1_EOF_SET0 LVDS EOF Code Setting LANE1. This is low 32bit.

9.1.3.37. **CMB_LVDS_LANE1_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x24C			Register Name: CMB_LVDS_LANE1_EOF_SET1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LVDS_LANE1_EOF_SET1 LVDS EOF Code Setting LANE1. This is high 32bit.

9.1.3.38. **CMB_LVDS_LANE2_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x250			**Register Name: CMB_LVDS_LANE2_SOF_SET0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE2_SOF_SET0 LVDS SOF Code Setting LANE2. This is low 32bit.

9.1.3.39. **CMB_LVDS_LANE2_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x254			**Register Name: CMB_LVDS_LANE2_SOF_SET1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE2_SOF_SET1 LVDS SOF Code Setting LANE2. This is high 32bit.

9.1.3.40. **CMB_LVDS_LANE2_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x258			**Register Name: CMB_LVDS_LANE2_SOL_SET0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE2_SOL_SET0 LVDS SOL Code Setting LANE2. This is low 32bit.

9.1.3.41. **CMB_LVDS_LANE2_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x25C			**Register Name: CMB_LVDS_LANE2_SOL_SET1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE2_SOL_SET1 LVDS SOL Code Setting LANE2. This is high 32bit.

9.1.3.42. **CMB_LVDS_LANE2_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x260			Register Name: CMB_LVDS_LANE2_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE2_EOL_SET0 LVDS EOL Code Setting LANE2. This is low 32bit.

9.1.3.43. **CMB_LVDS_LANE2_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x264			Register Name: CMB_LVDS_LANE2_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE2_EOL_SET1 LVDS EOL Code Setting LANE2. This is high 32bit.

9.1.3.44. **CMB_LVDS_LANE2_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x268			Register Name: CMB_LVDS_LANE2_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE2_EOF_SET0 LVDS EOF Code Setting LANE2. This is low 32bit.

9.1.3.45. **CMB_LVDS_LANE2_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x26C			Register Name: CMB_LVDS_LANE2_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE2_EOF_SET1 LVDS EOF Code Setting LANE2. This is high 32bit.

9.1.3.46. **CMB_LVDS_LANE3_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x270			Register Name: CMB_LVDS_LANE3_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE3_SOF_SET0 LVDS SOF Code Setting LANE3. This is low 32bit.

9.1.3.47. **CMB_LVDS_LANE3_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x274			Register Name: CMB_LVDS_LANE3_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE3_SOF_SET1 LVDS SOF Code Setting LANE3. This is high 32bit.

9.1.3.48. **CMB_LVDS_LANE3_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x278			Register Name: CMB_LVDS_LANE3_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE3_SOL_SET0 LVDS SOL Code Setting LANE3. This is low 32bit.

9.1.3.49. **CMB_LVDS_LANE3_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x27C			Register Name: CMB_LVDS_LANE3_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE3_SOL_SET1 LVDS SOL Code Setting LANE3. This is high 32bit.

9.1.3.50. **CMB_LVDS_LANE3_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x280			Register Name: CMB_LVDS_LANE3_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE3_EOL_SET0 LVDS EOL Code Setting LANE3. This is low 32bit.

9.1.3.51. **CMB_LVDS_LANE3_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x284			Register Name: CMB_LVDS_LANE3_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE3_EOL_SET1 LVDS EOL Code Setting LANE3. This is high 32bit.

9.1.3.52. **CMB_LVDS_LANE3_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x288			Register Name: CMB_LVDS_LANE3_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE3_EOF_SET0 LVDS EOF Code Setting LANE3. This is low 32bit.

9.1.3.53. **CMB_LVDS_LANE3_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x28C			Register Name: CMB_LVDS_LANE3_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE3_EOF_SET1 LVDS EOF Code Setting LANE3. This is high 32bit.

9.1.3.54. **CMB_LVDS_LANE4_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x290			Register Name: CMB_LVDS_LANE4_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE4_SOF_SET0 LVDS SOF Code Setting LANE4. This is low 32bit.

9.1.3.55. **CMB_LVDS_LANE4_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x294			Register Name: CMB_LVDS_LANE4_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE4_SOF_SET1 LVDS SOF Code Setting LANE4. This is high 32bit.

9.1.3.56. **CMB_LVDS_LANE4_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x298			Register Name: CMB_LVDS_LANE4_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE4_SOL_SET0 LVDS SOL Code Setting LANE4. This is low 32bit.

9.1.3.57. **CMB_LVDS_LANE4_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x29C			Register Name: CMB_LVDS_LANE4_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE4_SOL_SET1 LVDS SOL Code Setting LANE4. This is high 32bit.

9.1.3.58. **CMB_LVDS_LANE4_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2A0			Register Name: CMB_LVDS_LANE4_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE4_EOL_SET0 LVDS EOL Code Setting LANE4. This is low 32bit.

9.1.3.59. **CMB_LVDS_LANE4_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2A4			Register Name: CMB_LVDS_LANE4_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE4_EOL_SET1 LVDS EOL Code Setting LANE4. This is high 32bit.

9.1.3.60. **CMB_LVDS_LANE4_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2A8			Register Name: CMB_LVDS_LANE4_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE4_EOF_SET0 LVDS EOF Code Setting LANE4. This is low 32bit.

9.1.3.61. **CMB_LVDS_LANE4_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2AC			Register Name: CMB_LVDS_LANE4_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE4_EOF_SET1 LVDS EOF Code Setting LANE4. This is high 32bit.

9.1.3.62. **CMB_LVDS_LANE5_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2B0			Register Name: CMB_LVDS_LANE5_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE5_SOF_SET0 LVDS SOF Code Setting LANE5. This is low 32bit.

9.1.3.63. **CMB_LVDS_LANE5_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2B4			Register Name: CMB_LVDS_LANE5_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE5_SOF_SET1 LVDS SOF Code Setting LANE5. This is high 32bit.

9.1.3.64. **CMB_LVDS_LANE5_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2B8			Register Name: CMB_LVDS_LANE5_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE5_SOL_SET0 LVDS SOL Code Setting LANE5. This is low 32bit.

9.1.3.65. **CMB_LVDS_LANE5_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2BC			Register Name: CMB_LVDS_LANE5_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE5_SOL_SET1 LVDS SOL Code Setting LANE5. This is high 32bit.

9.1.3.66. **CMB_LVDS_LANE5_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2C0			Register Name: CMB_LVDS_LANE5_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE5_EOL_SET0 LVDS EOL Code Setting LANE5. This is low 32bit.

9.1.3.67. **CMB_LVDS_LANE5_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2C4			Register Name: CMB_LVDS_LANE5_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE5_EOL_SET1 LVDS EOL Code Setting LANE5. This is high 32bit.

9.1.3.68. **CMB_LVDS_LANE5_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2C8			Register Name: CMB_LVDS_LANE5_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE5_EOF_SET0 LVDS EOF Code Setting LANE5. This is low 32bit.

9.1.3.69. **CMB_LVDS_LANE5_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2CC			Register Name: CMB_LVDS_LANE5_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE5_EOF_SET1 LVDS EOF Code Setting LANE5. This is high 32bit.

9.1.3.70. **CMB_LVDS_LANE6_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2D0			Register Name: CMB_LVDS_LANE6_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE6_SOF_SET0 LVDS SOF Code Setting LANE6. This is low 32bit.

9.1.3.71. **CMB_LVDS_LANE6_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2D4			Register Name: CMB_LVDS_LANE6_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE6_SOF_SET1 LVDS SOF Code Setting LANE6. This is high 32bit.

9.1.3.72. **CMB_LVDS_LANE6_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2D8			Register Name: CMB_LVDS_LANE6_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE6_SOL_SET0 LVDS SOL Code Setting LANE6. This is low 32bit.

9.1.3.73. **CMB_LVDS_LANE6_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2DC			Register Name: CMB_LVDS_LANE6_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE6_SOL_SET1 LVDS SOL Code Setting LANE6. This is high 32bit.

9.1.3.74. **CMB_LVDS_LANE6_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2E0			Register Name: CMB_LVDS_LANE6_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE6_EOL_SET0 LVDS EOL Code Setting LANE6. This is low 32bit.

9.1.3.75. **CMB_LVDS_LANE6_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2E4			Register Name: CMB_LVDS_LANE6_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE6_EOL_SET1 LVDS EOL Code Setting LANE6. This is high 32bit.

9.1.3.76. **CMB_LVDS_LANE6_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2E8			Register Name: CMB_LVDS_LANE6_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE6_EOF_SET0 LVDS EOF Code Setting LANE6. This is low 32bit.

9.1.3.77. **CMB_LVDS_LANE6_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2EC			Register Name: CMB_LVDS_LANE6_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE6_EOF_SET1 LVDS EOF Code Setting LANE6. This is high 32bit.

9.1.3.78. **CMB_LVDS_LANE7_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2F0			Register Name: CMB_LVDS_LANE7_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE7_SOF_SET0 LVDS SOF Code Setting LANE7. This is low 32bit.

9.1.3.79. **CMB_LVDS_LANE7_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2F4			Register Name: CMB_LVDS_LANE7_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE7_SOF_SET1 LVDS SOF Code Setting LANE7. This is high 32bit.

9.1.3.80. **CMB_LVDS_LANE7_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x2F8			Register Name: CMB_LVDS_LANE7_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE7_SOL_SET0 LVDS SOL Code Setting LANE7. This is low 32bit.

9.1.3.81. **CMB_LVDS_LANE7_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x2FC			Register Name: CMB_LVDS_LANE7_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE7_SOL_SET1 LVDS SOL Code Setting LANE7. This is high 32bit.

9.1.3.82. **CMB_LVDS_LANE7_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x300			Register Name: CMB_LVDS_LANE7_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE7_EOL_SET0 LVDS EOL Code Setting LANE7. This is low 32bit.

9.1.3.83. **CMB_LVDS_LANE7_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x304			Register Name: CMB_LVDS_LANE7_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE7_EOL_SET1 LVDS EOL Code Setting LANE7. This is high 32bit.

9.1.3.84. **CMB_LVDS_LANE7_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x308			Register Name: CMB_LVDS_LANE7_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE7_EOF_SET0 LVDS EOF Code Setting LANE7. This is low 32bit.

9.1.3.85. **CMB_LVDS_LANE7_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x30C			Register Name: CMB_LVDS_LANE7_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE7_EOF_SET1 LVDS EOF Code Setting LANE7. This is high 32bit.

9.1.3.86. **CMB_LVDS_LANE8_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x310			Register Name: CMB_LVDS_LANE8_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE8_SOF_SET0 LVDS SOF Code Setting LANE8. This is low 32bit.

9.1.3.87. **CMB_LVDS_LANE8_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x314			Register Name: CMB_LVDS_LANE8_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE8_SOF_SET1 LVDS SOF Code Setting LANE8. This is high 32bit.

9.1.3.88. **CMB_LVDS_LANE8_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x318			Register Name: CMB_LVDS_LANE8_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE8_SOL_SET0 LVDS SOL Code Setting LANE8. This is low 32bit.

9.1.3.89. **CMB_LVDS_LANE8_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x31C			Register Name: CMB_LVDS_LANE8_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE8_SOL_SET1 LVDS SOL Code Setting LANE8. This is high 32bit.

9.1.3.90. **CMB_LVDS_LANE8_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x320			Register Name: CMB_LVDS_LANE8_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE8_EOL_SET0 LVDS EOL Code Setting LANE8. This is low 32bit.

9.1.3.91. **CMB_LVDS_LANE8_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x324			Register Name: CMB_LVDS_LANE8_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE8_EOL_SET1 LVDS EOL Code Setting LANE8. This is high 32bit.

9.1.3.92. **CMB_LVDS_LANE8_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x328			Register Name: CMB_LVDS_LANE8_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE8_EOF_SET0 LVDS EOF Code Setting LANE8. This is low 32bit.

9.1.3.93. **CMB_LVDS_LANE8_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x32C			Register Name: CMB_LVDS_LANE8_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE8_EOF_SET1 LVDS EOF Code Setting LANE8. This is high 32bit.

9.1.3.94. **CMB_LVDS_LANE9_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x330			Register Name: CMB_LVDS_LANE9_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE9_SOF_SET0 LVDS SOF Code Setting LANE9. This is low 32bit.

9.1.3.95. **CMB_LVDS_LANE9_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x334			Register Name: CMB_LVDS_LANE9_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE9_SOF_SET1 LVDS SOF Code Setting LANE9. This is high 32bit.

9.1.3.96. **CMB_LVDS_LANE9_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x338			Register Name: CMB_LVDS_LANE9_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE9_SOL_SET0 LVDS SOL Code Setting LANE9. This is low 32bit.

9.1.3.97. **CMB_LVDS_LANE9_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x33C			Register Name: CMB_LVDS_LANE9_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE9_SOL_SET1 LVDS SOL Code Setting LANE9. This is high 32bit.

9.1.3.98. **CMB_LVDS_LANE9_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x340			Register Name: CMB_LVDS_LANE9_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE9_EOL_SET0 LVDS EOL Code Setting LANE9. This is low 32bit.

9.1.3.99. **CMB_LVDS_LANE9_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x344			Register Name: CMB_LVDS_LANE9_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE9_EOL_SET1 LVDS EOL Code Setting LANE9. This is high 32bit.

9.1.3.100. **CMB_LVDS_LANE9_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x348			Register Name: CMB_LVDS_LANE9_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE9_EOF_SET0 LVDS EOF Code Setting LANE9. This is low 32bit.

9.1.3.101. **CMB_LVDS_LANE9_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x34C			Register Name: CMB_LVDS_LANE9_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE9_EOF_SET1 LVDS EOF Code Setting LANE9. This is high 32bit.

9.1.3.102. **CMB_LVDS_LANE10_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x350			Register Name: CMB_LVDS_LANE10_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE10_SOF_SET0 LVDS SOF Code Setting LANE10. This is low 32bit.

9.1.3.103. **CMB_LVDS_LANE10_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x354			Register Name: CMB_LVDS_LANE10_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE10_SOF_SET1 LVDS SOF Code Setting LANE10. This is high 32bit.

9.1.3.104. **CMB_LVDS_LANE10_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x358			Register Name: CMB_LVDS_LANE10_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE10_SOL_SET0 LVDS SOL Code Setting LANE10. This is low 32bit.

9.1.3.105. **CMB_LVDS_LANE10_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x35C			Register Name: CMB_LVDS_LANE10_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE10_SOL_SET1 LVDS SOL Code Setting LANE10. This is high 32bit.

9.1.3.106. **CMB_LVDS_LANE10_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x360			Register Name: CMB_LVDS_LANE10_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE10_EOL_SET0 LVDS EOL Code Setting LANE10. This is low 32bit.

9.1.3.107. **CMB_LVDS_LANE10_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x364			Register Name: CMB_LVDS_LANE10_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE10_EOL_SET1 LVDS EOL Code Setting LANE10. This is high 32bit.

9.1.3.108. **CMB_LVDS_LANE10_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x368			Register Name: CMB_LVDS_LANE10_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE10_EOF_SET0 LVDS EOF Code Setting LANE10. This is low 32bit.

9.1.3.109. **CMB_LVDS_LANE10_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x36C			Register Name: CMB_LVDS_LANE10_EOF_SET1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LVDS_LANE10_EOF_SET1 LVDS EOF Code Setting LANE10. This is high 32bit.

9.1.3.110. **CMB_LVDS_LANE11_SOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x370			Register Name: CMB_LVDS_LANE11_SOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE11_SOF_SET0 LVDS SOF Code Setting LANE11. This is low 32bit.

9.1.3.111. **CMB_LVDS_LANE11_SOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x374			Register Name: CMB_LVDS_LANE11_SOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE11_SOF_SET1 LVDS SOF Code Setting LANE11. This is high 32bit.

9.1.3.112. **CMB_LVDS_LANE11_SOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x378			Register Name: CMB_LVDS_LANE11_SOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE11_SOL_SET0 LVDS SOL Code Setting LANE11. This is low 32bit.

9.1.3.113. **CMB_LVDS_LANE11_SOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x37C			Register Name: CMB_LVDS_LANE11_SOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE11_SOL_SET1 LVDS SOL Code Setting LANE11. This is high 32bit.

9.1.3.114. **CMB_LVDS_LANE11_EOL_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x380			Register Name: CMB_LVDS_LANE11_EOL_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE11_EOL_SET0 LVDS EOL Code Setting LANE11. This is low 32bit.

9.1.3.115. **CMB_LVDS_LANE11_EOL_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x384			Register Name: CMB_LVDS_LANE11_EOL_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE11_EOL_SET1 LVDS EOL Code Setting LANE11. This is high 32bit.

9.1.3.116. **CMB_LVDS_LANE11_EOF_SET0_REG(Default Value: 0x0000_0000)**

Offset:0x388			Register Name: CMB_LVDS_LANE11_EOF_SET0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE11_EOF_SET0 LVDS EOF Code Setting LANE11. This is low 32bit.

9.1.3.117. **CMB_LVDS_LANE11_EOF_SET1_REG(Default Value: 0x0000_0000)**

Offset:0x38C			Register Name: CMB_LVDS_LANE11_EOF_SET1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LVDS_LANE11_EOF_SET1 LVDS EOF Code Setting LANE11. This is high 32bit.

9.1.3.118. **CMB_HISPI_CTR_REG(Default Value: 0x0000_0000)**

Offset:0x390			Register Name: CMB_HISPI_CTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	HISPI_MODE_SEL In HISPI mode, select the trans data mode. 0:Packetized-SP (Default) 1:Streaming-SP 2:Reserved 3:Reserved
7:5	/	/	/
4	R/W	0x0	HISPI_NORMAL_EN Enable HISPI Normal mode, switch to HISPI and close LVDS. 1:Enable HISPI 0:Disable HISPI
3:1	/	/	/
0	R/W	0x0	HISPI_HDR_EN Enable HISPI interface WDR/HDR 1:Enable 0:Disable

9.1.3.119. **CMB_HISPI_SYNC_CODE_REG(Default Value: 0x0000_0000)**

Offset:0x394			Register Name: CMB_HISPI_SYNC_CODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	HISPI_HDR_EOF_FILD HISPI EOF Field in HDR/WDR mode
15:0	R/W	0x0	HISPI_HDR_SOF_FILD HISPI SOF Field in HDR/WDR mode

9.1.3.120. **CMB_HISPI_CODE_MASK_REG(Default Value: 0x0000_0000)**

Offset:0x398			Register Name: CMB_HISPI_CODE_MASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:0	R/W	0x0	HISPI_CODE_MASK HISPI SYNC Code MASK in HDR/WDR mode

9.1.3.121. **CMB_PHYA_LANE_TE_EN_REG(Default Value: 0x0000_0000)**

Offset:0x0E00			**Register Name: CMB_PHYA_LANE_TE_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	PHYA_C_CK_TE_EN Enable Terminated resistor PHYA C CK Lane 1:Enable 0:disable
17	R/W	0x0	PHYA_B_CK_TE_EN Enable Terminated resistor PHYA B CK Lane.
16	R/W	0x0	PHYA_A_CK_TE_EN Enable Terminated resistor PHYA A CK Lane .
15	/	/	/
14	R/W	0x0	PHYA_C_D3_TE_EN Enable Terminated resistor PHYA C D3 Lane.
13	R/W	0x0	PHYA_B_D3_TE_EN Enable Terminated resistor PHYA B D3 Lane.
12	R/W	0x0	PHYA_A_D3_TE_EN Enable Terminated resistor PHYA A D3 Lane.
11	/	/	/
10	R/W	0x0	PHYA_C_D2_TE_EN Enable Terminated resistor PHYA C D2 Lane.
9	R/W	0x0	PHYA_B_D2_TE_EN Enable Terminated resistor PHYA B D2 Lane.
8	R/W	0x0	PHYA_A_D2_TE_EN Enable Terminated resistor PHYA A D2 Lane .
7	/	/	/
6	R/W	0x0	PHYA_C_D1_TE_EN Enable Terminated resistor PHYA C D1 Lane.
5	R/W	0x0	PHYA_B_D1_TE_EN Enable Terminated resistor PHYA B D1 Lane.
4	R/W	0x0	PHYA_A_D1_TE_EN Enable Terminated resistor PHYA A D1 Lane .
3	/	/	/
2	R/W	0x0	PHYA_C_D0_TE_EN Enable Terminated resistor PHYA C D0 Lane.
1	R/W	0x0	PHYA_B_D0_TE_EN Enable Terminated resistor PHYA B D0 Lane.
0	R/W	0x0	PHYA_A_D0_TE_EN Enable Terminated resistor PHYA A D0 Lane.

9.1.3.122. **CMB_PHYA_CTR_REG(Default Value: 0x0000_0000)**

Offset:0xE04			Register Name: CMB_PHYA_CTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PHYA Enable 0：PHYA Disable 1：PHYA Enable
30	/	/	/
29：28	R/W	0x0	PHYA_TSTRX Bit[28]:Parallel to Serial test enable 0:Normal(Default) 1:TSTIC/D Input Bit[29]:Receiver Amp test enable 0:Normal(Default) 1:TSTADOxx Output
27:26	/	/	/
25	R/W	0x0	PHYA_TSTIND Serial to Parallel test data input
24	R/W	0x0	PHYA_TSTINC Serial to Parallel test clock input
23:22	/	/	/
21	R/W	0x0	PHYA_SB_SEL Significant Bit SEL 0: Normal(LSB[0]) 1: Reverse(MSB[0])
20	R/W	0x0	PHYA_RESET_SEL Reset SEL 0: Sync reset 1: Async reset
19:18	/	/	/
17:16	R/W	0x0	PHYA_OFFSET_SEL Input Differential Offset Range Setting 0: 0 mV(Normal) 1: 12.5mV 2: 25.0mV 3: 37.5mV
15:14	/	/	/
13:12	R/W	0x0	PHYA_LP_VOL_LH LP Low to High Threshold Voltage Select 0:Current Source 0.800V(Default) 1:Voltage Source 0.800V 2:Voltage Source 0.650V 3:Voltage Source 0.500V
11:10	/	/	/
9:8	R/W	0x0	PHYA_LP_VOL_HL LP High to Low Threshold Voltage Select

			0:Current Source 0.650V(Default) 1:Voltage Source 0.650V 2:Voltage Source 0.575V 3:Voltage Source 0.500V
7	R/W	0x0	PHYA_VRM Bias Voltage Control 1:Resistance Split 0:Using BGR Circuits(Default)
6	R/W	0x0	PHYA_IRM Bias Current Control 1:Resistance Split 0:Using BGR Circuits(Default)
5	R/W	0x0	PHYA_IN_CLK_POL 1:Fall Edge 0:Rise Edge(Default)
4	R/W	0x0	PHYA_OUT_CLK_POL 1:Fall Edge 0:Rise Edge(Default)
3:2	R/W	0x0	PHYA_BIT_SEL 0:2-bit Parallel 1:4-bit Parallel 2:8-bit Parallel //3:8-bit Parallel
1	R/W	0x0	PHYA_CKIN_MODE_SEL 1:Using B_CK only 0:Using each(Default)
0	R/W	0x0	PHYA_PWDN 1:Enable 0:Power down

9.1.3.123. **CMB_PHYA_DLY_CTR0_REG(Default Value: 0x0000_0000)**

Offset:0xE08			**Register Name: CMB_PHYA_DLY_CTR0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	PHYA_C_D0_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)

27	/	/	/
26:24	R/W	0x0	PHYA_B_D0_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
23	/	/	/
22:20	R/W	0x0	PHYA_A_D0_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
18:16	R/W	0x0	PHYA_C_CLK_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
15	/	/	/
14:12	R/W	0x0	PHYA_B_CLK_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
11	/	/	/
10:8	R/W	0x0	PHYA_A_CLK_DLY_SET 0:Delay+0

			1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
7:1	/	/	/
0	R/W	0x0	PHYA_DLY_EN 1:Normal Operation(Default),not Adjusting 0:Adjusting Timing(Using DLYxxx[2:0])

9.1.3.124. **CMB_PHYA_DLY_CTR1_REG(Default Value: 0x0000_0000)**

Offset:0xE0C			**Register Name: CMB_PHYA_DLY_CTR1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x0	PHYA_C_D2_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
18:16	R/W	0x0	PHYA_B_D2_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
15	/	/	/
14:12	R/W	0x0	PHYA_A_D2_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4

			5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
11	/	/	/
10:8	R/W	0x0	PHYA_C_D1_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
7	/	/	/
6:4	R/W	0x0	PHYA_B_D1_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
3	/	/	/
2:0	R/W	0x0	PHYA_A_D1_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)

9.1.3.125. **CMB_PHYA_DLY_CTR2_REG(Default Value: 0x0000_0000)**

Offset:0xE10			**Register Name: CMB_PHYA_DLY_CTR2_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:8	R/W	0x0	PHYA_C_D3_DLY_SET 0:Delay+0

			1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
7	/	/	/
6:4	R/W	0x0	PHYA_B_D3_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)
3	/	/	/
2:0	R/W	0x0	PHYA_A_D3_DLY_SET 0:Delay+0 1:Delay+1 2:Delay+2 3:Delay+3 4:Delay+4 5:Delay+5 6:Delay+6 7:Delay+7 Delay+1 about 0.1-0.4nSec(TYP:0.2nSec)

9.1.3.126. **CMB_PHYA_CFG_REG(Default Value: 0x0000_0000)**

Offset:0xE14			**Register Name: CMB_PHYA_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	MODE_SEL Operation Mode Control 0: not use 1: not use 2: D-PHY 3: Sub-LVDS 4: COMS Others:reserved

Chapter 10 ISP

10.1. Overview

The ISP module supports real time image process for RAW sensor. The main functions are as follows.

- Crop
- Black level correction(BLC)
- Sensor built-in wide dynamic range(WDR)
- 2-frame combination WDR
- Digital WDR
- Digital gain
- Dynamic defect pixel correction(DPC)
- Crosstalk correction
- 2D denoise
- 3D denoise
- Auto balance
- Auto exposure
- Auto focus
- 3A statistic output
- Lens shading correction
- Demosaic
- Picture sharpen
- Color management and enhancement
- Dynamic range compression(DRC)
- Gamma correction
- High-precision scale down
- Defog

The processing capability of the ISP module is as follows.

- Supports 8/10/12 bits RAW data input
- **V536-H**: maximum picture resolution of 4224 x 3168
  V526: maximum picture resolution of 2688 x 1600
- Minimum picture resolution of 128 x 100
- **V536-H**: maximum frame rate of 4000 x 3000@30fps or 4224 x 3168@30fps
  V526: maximum frame rate of 2688 x 1600@30fps
- Minimum horizontal blanking region of 96 pixels
- Minimum vertical blanking region of 32 lines

10.2. Block Diagram

The block diagram of the ISP module is as follows.

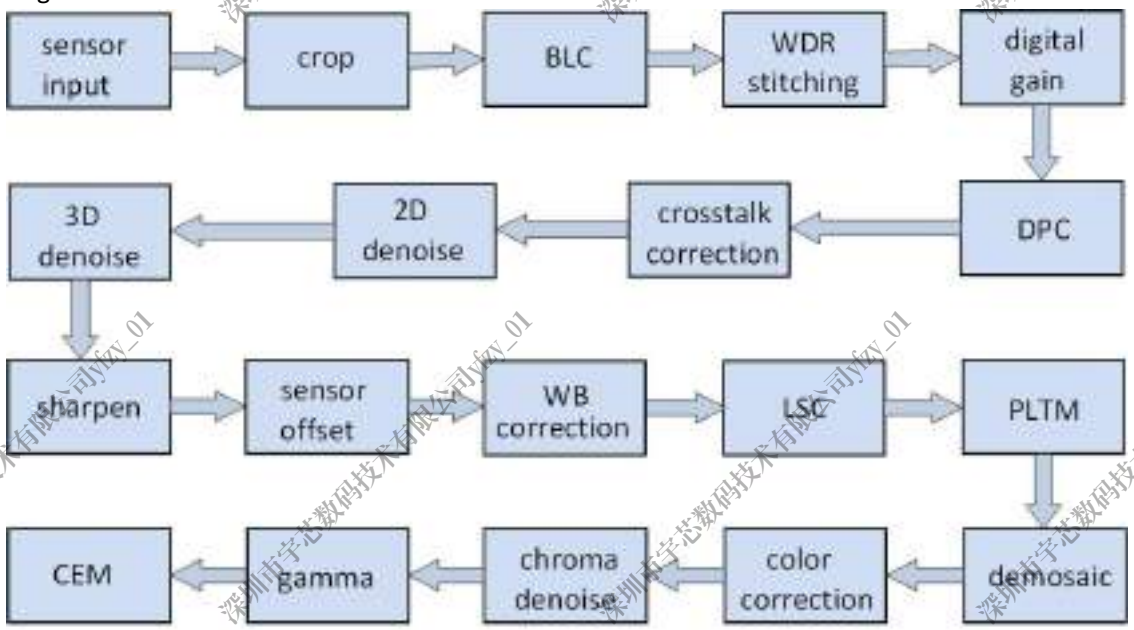


Figure 10-1. ISP Block Diagram

10.3. Module Functions

10.3.1. Crop

The Crop module, which can crop the input picture, is often used to change the aspect ratio of the input picture or extract the region of interest for a picture. For details about the configuration methods, see the <<*image sensor light guide*>>.

10.3.2. BLC

The BLC module adds respectively offset for four Bayer color channels(R,Gr,Gb,and B), to perform optical black correction. The precision of the offset is S13. The module is usually used for wide dynamic sensor.

10.3.3. WDR

The WDR module supports 2-frame combination WDR function.

10.3.4. Digital Gain

The Digital Gain module provides the digital gain, and supports U12Q10-precision .

10.3.5. DPC

The DPC module is used to correct defect pixels in Bayer field. There are two modes to be chosen, normal mode and strong mode. In normal mode, single defect pixel can be corrected. In strong mode, neighbor defect pixels can be corrected.

10.3.6. Crosstalk Correction

The Crosstalk Correction module is used to remove abnormal picture question when Gr and Gb imbalance. Usually, the module is used when sensor CRA unmatches lens CRA.

10.3.7. 2D Denoise

The 2D Denoise module restrains sensor noises in the Bayer field to improve picture quality.

10.3.8. 3D Denoise

The 3D Denoise module implements interframe filtering for sensor noises in the time domain to improve picture quality.

10.3.9. Sharpen

After denoising, the Sharpen module implements picture edge sharpening to improve picture edge information, while picture contour is much clearer.

10.3.10. Sensor Offset

The Sensor Offset module adds respectively offset for four Bayer color channels(R,Gr,Gb,and B) to perform optical black correction. The precision of the offset is S13.

10.3.11. WB Correction

The WB Correction module adds respectively gain for four channels(R,Gr,Gb,and B) to implement white balance correction. The precision of the gain is U12Q8.

10.3.12. LSC

The LSC module implements lens shading correction. According to the radial position of each pixel within picture, the module can lookup R,G,B table to obtain compensation gain and compensate the reduced luminance from picture central to edge. The size of each gain table is 256, and the precision is U12Q10.

10.3.13. PLTM

The PLTM module adjusts the dynamic range of picture. The module adjust the luminance and contrast through histogram statistic of picture, to improve picture quality.

10.3.14. Demosaic

The Demosaic module interpolates Bayer field pixel to RGB field while holding clear picture edge and restraining pseudo color.

10.3.15. Color Correction

The Color Correction module applies a 3x3 color gain matrix and a 3x1 offset matrix on the input R/G/B pixels to restore image color. The precision of each value in gain matrix is S12Q8 and the precision of each value in offset matrix is S13.

$$\begin{pmatrix} R\_out \\ G\_out \\ B\_out \end{pmatrix} = \begin{pmatrix} g_{rr} & g_{gr} & g_{br} \\ g_{rg} & g_{gg} & g_{bg} \\ g_{rb} & g_{gb} & g_{bb} \end{pmatrix} \times \begin{pmatrix} R\_in \\ G\_in \\ B\_in \end{pmatrix} + \begin{pmatrix} offset\_R \\ offset\_G \\ offset\_B \end{pmatrix}$$

10.3.16. Chroma Denoise

The Chroma Denoise module restrains color noises of sensor to improve picture quality.

10.3.17. Gamma

The Gamma module applies gamma correction for each color channel(R,G,and B) through looking-up table. Each gamma table has 256 entries and the precision is U12.

10.3.18. CEM

The CEM module adjusts hue and saturation of picture in YUV field, and enhances or restrains specific colors such as blue sky, plant and complexion based on user preference.

Chapter 11 Audio

11.1. I2S/PCM

11.1.1. Overview

The I2S/PCM controller is designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified mode format, Right-justified mode format, PCM mode format and TDM mode format.

The I2S/PCM controller includes the following features:

- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master/Slave mode
- Adjustable interface voltage
- Clock up to 24.576MHz
- Adjustable audio sample resolution from 8-bit to 32-bit
- Up to 16 channel(fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
- Sample rate from 8 kHz to 384 kHz(CHAN = 2)
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports loop back mode for test

11.1.2. Block Diagram

The block diagram of I2S/PCM interface is shown below.

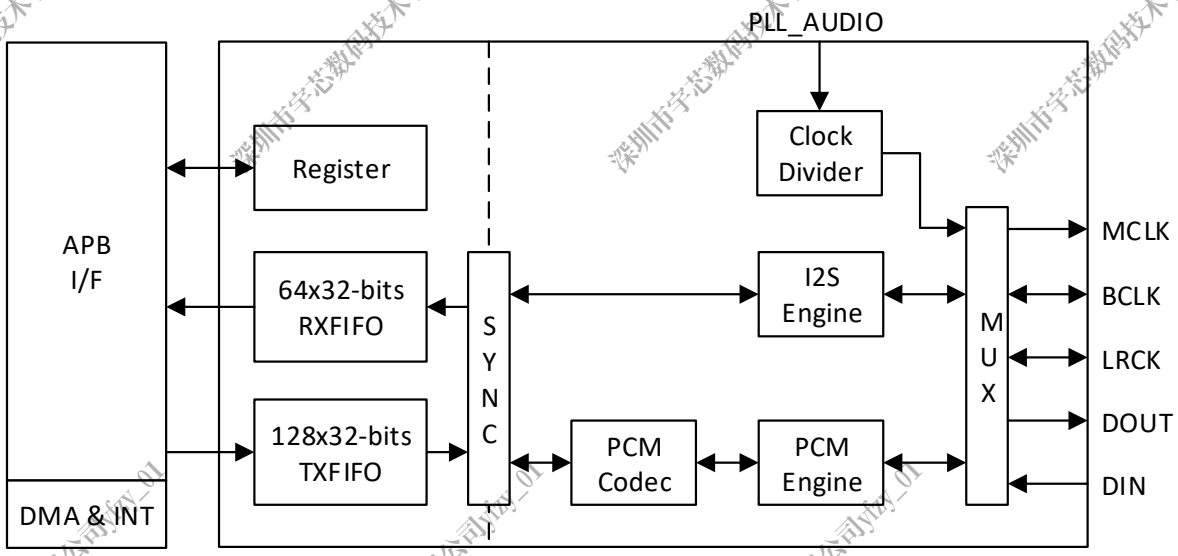


Figure 11-1. I2S/PCM Interface System Block Diagram

11.1.3. Operations and Functional Descriptions

11.1.3.1. External Signals

Table 11-1 describes the external signals of I2S/PCM interface. BCLK and LRCK are bidirectional I/O, when I2S/PCM interface is configured as master device, BCLK and LRCK is output pin; when I2S/PCM interface is configured as slave device, BCLK and LRCK is input pin. MCLK is an output pin for external device. DOUT is always the serial data output pin, and DIN is the serial data input. For information about General Purpose I/O port, see Port Controller.

Table 11-1. I2S/PCM External Signals

Signal Name	Description	Type
I2S0_MCLK	I2S/PCM 0 Master Clock	O
I2S0_BCLK	I2S/PCM 0 Sample Rate Serial Clock	I/O
I2S0_LRCK	I2S/PCM 0 Sample Rate Left and Right Channel Select Clock/Sync	I/O
I2S0_DIN	I2S/PCM 0 Serial Data Input	I
I2S0_DOUT	I2S/PCM 0 Serial Data Output	O
I2S2_MCLK	I2S/PCM 2 Master Clock	O
I2S2_BCLK	I2S/PCM 2 Sample Rate Serial Clock	I/O
I2S2_LRCK	I2S/PCM 2 Sample Rate Left and Right Channel Select Clock/Sync	I/O
I2S2_DIN	I2S/PCM 2 Serial Data Input	I
I2S2_DOUT	I2S/PCM 2 Serial Data Output	O

11.1.3.2. Clock Sources

Table 11-2 describes the clock sources for I2S/PCM. Users can see **Chapter 3.3.CCU** for clock setting, configuration and gating information.

Table 11-2. I2S/PCM Clock Sources

Clock Name	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz serial frequency

11.1.3.3. **Timing Diagram**

The I2S/PCM supports standard I2S mode,Left-justified I2S mode,Right-justified I2S mode,PCM mode and TDM mode. Software can select any modes by setting the **I2S/PCM Control Register**.Figure 11-2 to Figure 11-6 describe the waveforms for LRCK,BCLK and DOUT,DIN.

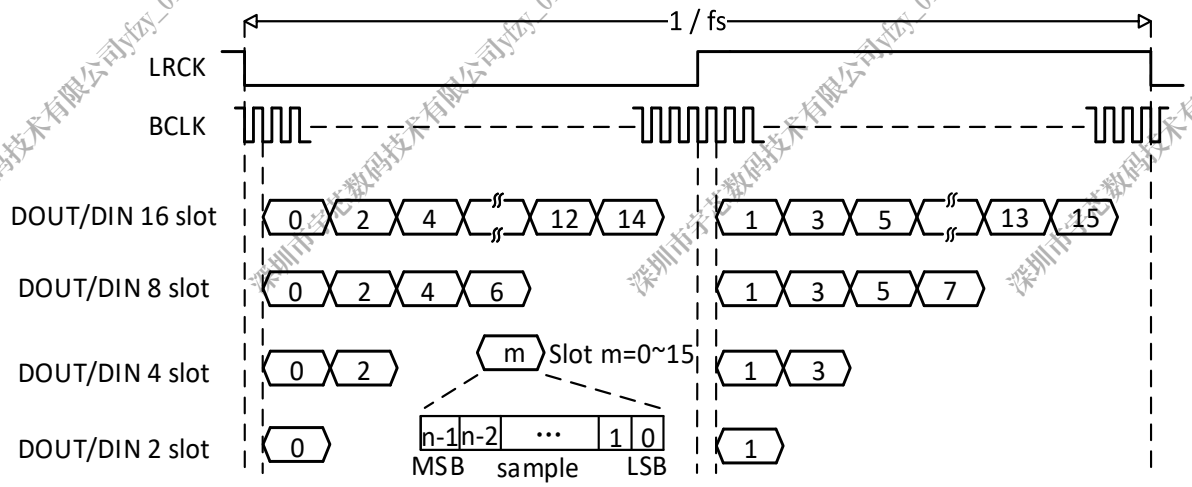


Figure 11-2. I2S Standard Mode Timing

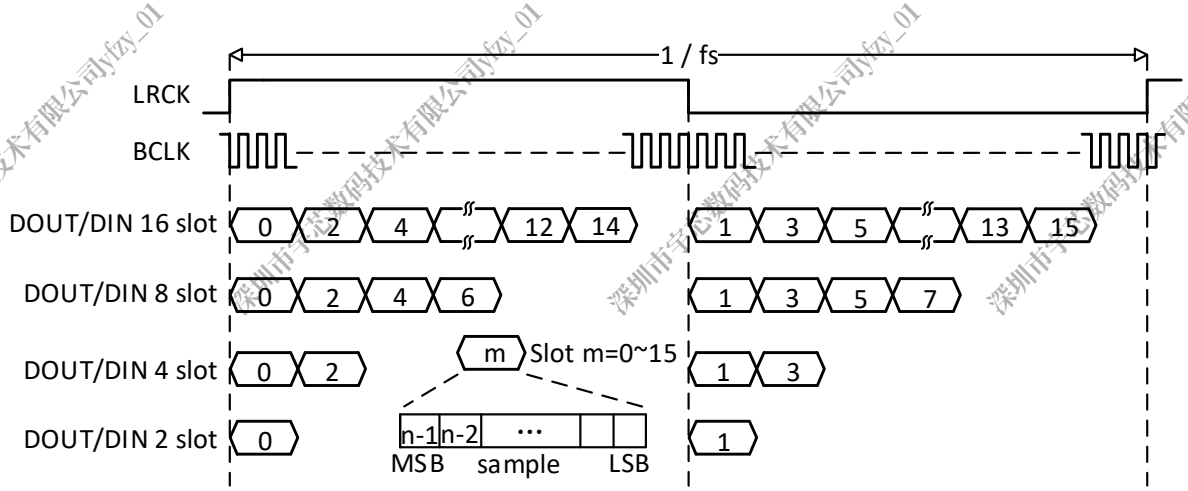


Figure 11-3. Left-Justified Mode Timing

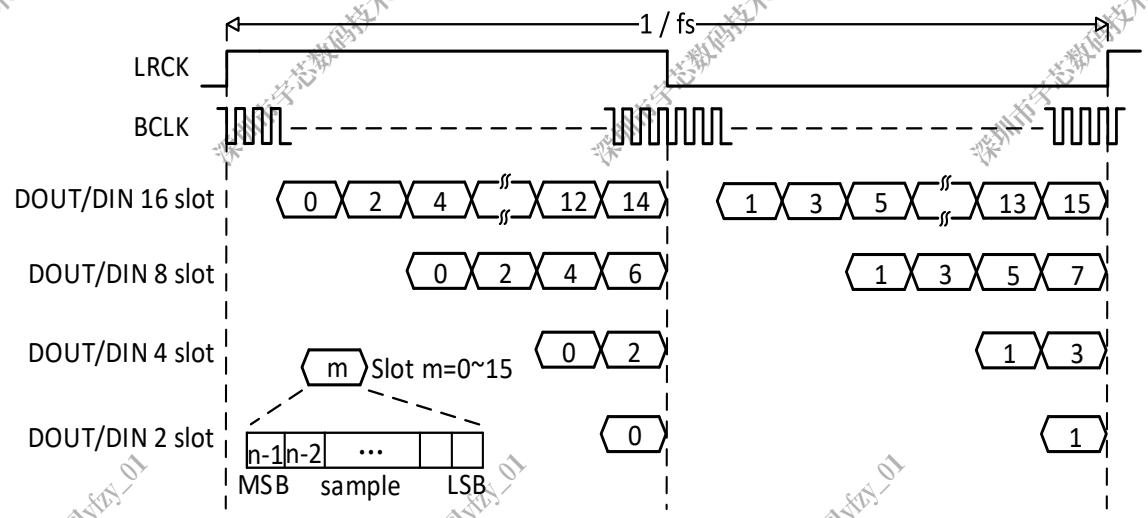


Figure 11-4. Right-Justified Mode Timing

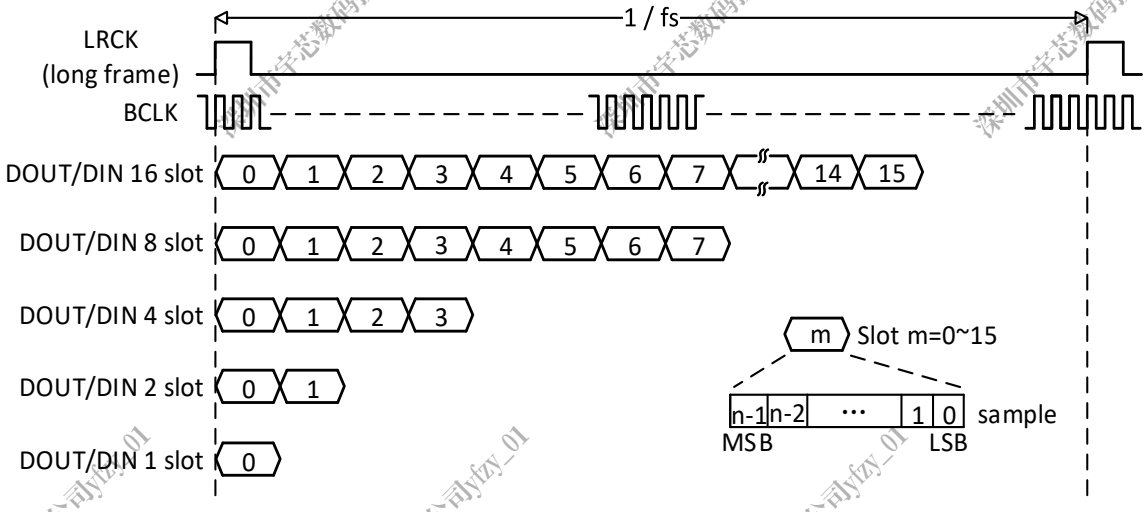


Figure 11-5. PCM Long Frame Mode Timing

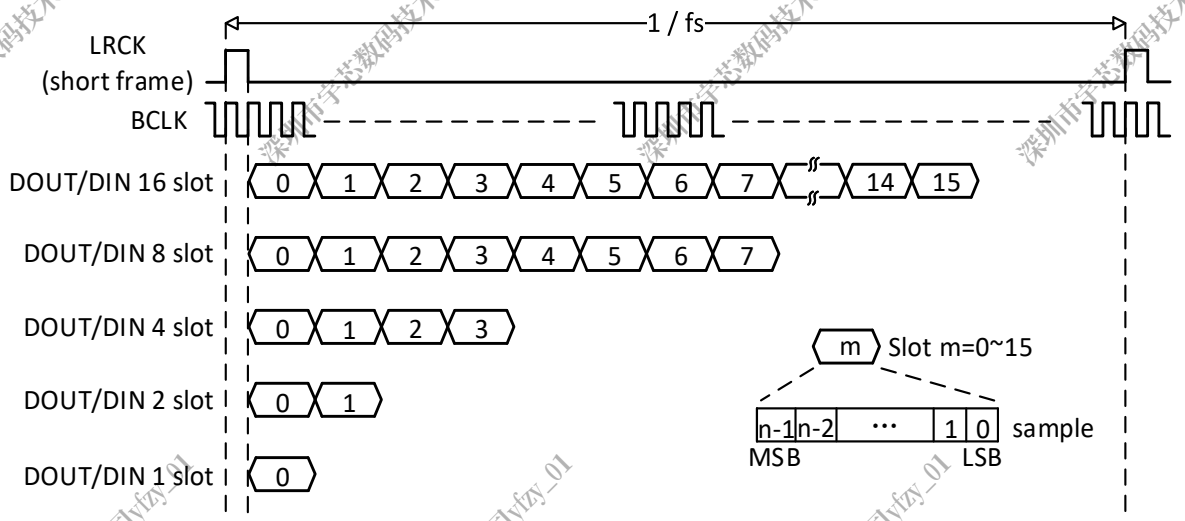


Figure 11-6. PCM Short Frame Mode Timing

11.1.3.4. Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup and Enable/Disable module. These five steps are described in detail in the following sections.

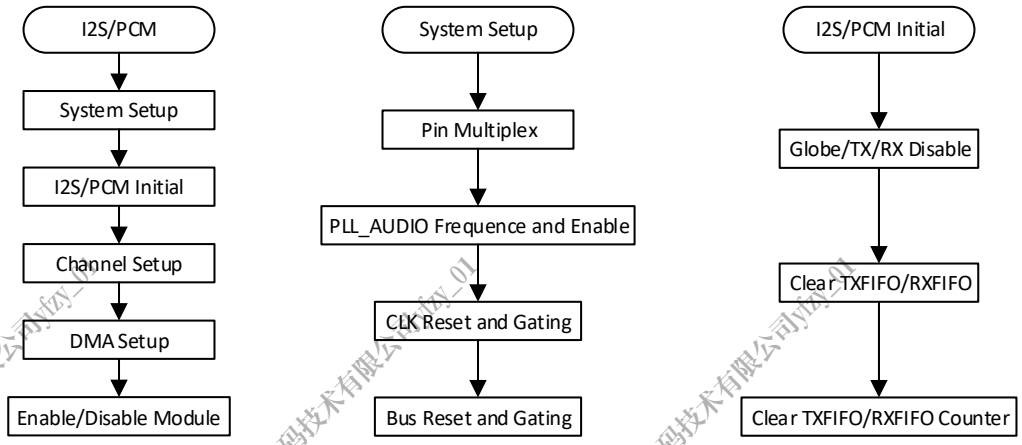


Figure 11-7. I2S/PCM Operation Flow

(1). System Setup and I2S/PCM Initialization

The clock source for the I2S/PCM should be followed. At first you must disable the PLL_AUDIO through the **PLL_ENABLE** bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must set up the frequency of the PLL_AUDIO in the **PLL_AUDIO_CTRL_REG**. After that, you must open the I2S/PCM gating through the **I2S/PCM_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes to 1. At last, you must reset and open the I2S/PCM bus gating in the **CCU_I2S_BGR_REG**.

After the system setup, the register of I2S/PCM can be setup. At first, you should initialization the I2S/PCM. You should close the **Globe Enable** bit(I2S/PCM_CTL[0]) , **Transmitter Block Enable** bit(I2S/PCM_CTL[2]) and **Receiver Block Enable** bit(I2S/PCM_CTL[1]) by writing 0 to it. After that, you must clear the TX/RX FIFO by writing 0 to the bit[25:24] of **I2S/PCM_FCTL**. At last, you can clear the TX FIFO and RX FIFO counter by writing 0 to **I2S/PCM_TXCNT** and **I2S/PCM_RXCNT**.

(2). Channel Setup and DMA Setup

First, you can setup the I2S/PCM of mater and slave. The configuration can be referred to the protocol of I2S/PCM. Then, you can set up the translation mode, the sample resolution, the wide of slot, the channel slot number and the trigger level and so on. The setup of register can be found in the specification.

The I2S/PCM supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3). Enable and Disable I2S/PCM

To enable the function, you can enable TX/RX by writing **the I2S/PCM_CT**L[2:1]. After that, you must enable I2S/PCM by writing the **Globe Enable** bit to 1 in the I2S/PCM_CTL. Write the **Globe Enable** to 0 to disable I2S/PCM.

11.1.4. Register List

Module Name	Base Address

I2S/PCM0	0x05090000
I2S/PCM1(for HDMI)	0x05091000
I2S/PCM2	0x05092000

Register Name	Offset	Description
I2S/PCM_CTL	0x0000	I2S/PCM Control Register
I2S/PCM_FMT0	0x0004	I2S/PCM Format Register 0
I2S/PCM_FMT1	0x0008	I2S/PCM Format Register 1
I2S/PCM_ISTA	0x000C	I2S/PCM Interrupt Status Register
I2S/PCM_RXFIFO	0x0010	I2S/PCM RXFIFO Register
I2S/PCM_FCTL	0x0014	I2S/PCM FIFO Control Register
I2S/PCM_FSTA	0x0018	I2S/PCM FIFO Status Register
I2S/PCM_INT	0x001C	I2S/PCM DMA & Interrupt Control Register
I2S/PCM_TXFIFO	0x0020	I2S/PCM TXFIFO Register
I2S/PCM_CLKD	0x0024	I2S/PCM Clock Divide Register
I2S/PCM_TXCNT	0x0028	I2S/PCM TX Sample Counter Register
I2S/PCM_RXCNT	0x002C	I2S/PCM RX Sample Counter Register
I2S/PCM_CHCFG	0x0030	I2S/PCM Channel Configuration Register
I2S/PCM_TXCHCFG	0x0034	I2S/PCM TX Channel Configuration Register
I2S/PCM_TXCHMAP0	0x0044	I2S/PCM TX Channel Mapping Register0
I2S/PCM_TXCHMAP1	0x0048	I2S/PCM TX Channel Mapping Register1
I2S/PCM_RXCHSEL	0x0064	I2S/PCM RX Channel Select Register
I2S/PCM_RXCHMAP0	0x0068	I2S/PCM RX Channel Mapping Register0
I2S/PCM_RXCHMAP1	0x006C	I2S/PCM RX Channel Mapping Register1

11.1.5. Register Description

11.1.5.1. I2S/PCM Control Register(Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x1	BCLK_OUT 0: Input 1: Output
17	R/W	0x1	LRCK_OUT 0: Input 1: Output
16:12	/	/	/
11	R/W	0x0	DOUT3_EN (Only for I2S/PCM1) 0: Disable, Hi-Z State 1: Enable
10	R/W	0x0	DOUT2_EN (Only for I2S/PCM1) 0: Disable, Hi-Z State

			1: Enable
9	R/W	0x0	DOUT1_EN (Only for I2S/PCM1) 0: Disable, Hi-Z State 1: Enable
8	R/W	0x0	DOUT0_EN (For All I2S/PCM) 0: Disable, Hi-Z State 1: Enable
7	/	/	/
6	R/W	0x0	OUT_MUTE 0: Normal Transfer 1: Force DOUT to output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM Mode (offset 0: Long Frame; offset 1: Short Frame) 01: Left Mode (offset 0: LJ Mode; offset 1: I2S Mode) 10: Right-Justified Mode 11: Reserved
3	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When setting to '1' , the bit indicates that the DOUT connects to the DIN.
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable 0: Disable 1: Enable

11.1.5.2. **I2S/PCM Format Register 0(Default Value: 0x0000_0033)**

Offset: 0x0004			**Register Name: I2S/PCM_FMT0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	LRCK_WIDTH (Only Apply in PCM Mode) LRCK Width 0: LRCK = 1 BCLK Width (Short Frame) 1: LRCK = 2 BCLK Width (Long Frame)

29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY In I2S / Left-Justified / Right-Justified mode: 0: Left Channel when LRCK is low 1: Left channel when LRCK is high In PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge
18	/	/	/
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follows: PCM mode: Number of BCLKs within (Left + Right) channel width. I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) . N+1 For example: N = 7: 8 BCLKs width … N = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY 0: Normal mode, DOUT drives data at negative edge 1: Invert mode, DOUT drives data at positive edge
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3	R/W	0x0	EDGE_TRANSFER 0: DOUT drives data and DIN sample data at the different BCLK edge 1: DOUT drives data and DIN sample data at the same BCLK edge BCLK_POLARITY = 0, EDGE_TRANSFER = 0, DIN sample data at positive edge; BCLK_POLARITY = 0, EDGE_TRANSFER = 1, DIN sample data at negative edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 0, DIN sample data at negative edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 1, DIN sample data at positive edge.
2:0	R/W	0x3	SW Slot Width Select

			000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

11.1.5.3. **I2S/PCM Format Register 1(Default Value: 0x0000_0030)**

Offset: 0x0008			**Register Name: I2S/PCM_FMT1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RX MLS MSB/LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX MLS MSB/LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in Slot [Sample Resolution < Slot Width] 00: Zeros or audio gain padding at LSB position 01: Sign extension at MSB position 10: Reserved 11: Transfer 0 after each sample in each Slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law

11.1.5.4. **I2S/PCM Interrupt Status Register(Default Value: 0x0000_0010)**

Offset: 0x000C	**Register Name: I2S/PCM_ISTA**

Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: TXFIFO underrun pending interrupt Write '1' to clear this interrupt.
5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No pending interrupt 1: TXFIFO overrun pending interrupt Write '1' to clear this interrupt.
4	R/W1C	0x1	TXE_INT TXFIFO Empty Pending Interrupt 0: No pending IRQ 1: TXFIFO empty pending interrupt when data in TXFIFO are less than TX trigger level Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: RXFIFO underrun pending interrupt Write '1' to clear this interrupt.
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Write '1' to clear this interrupt.
0	R/W1C	0x0	RXA_INT RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ when data in RXFIFO are more than RX trigger level Write '1' to clear this interrupt or automatic clear if interrupt condition fails.

11.1.5.5. **I2S/PCM RXFIFO Register(Default Value: 0x0000_0000)**

Offset: 0x0010			Register Name: I2S/PCM_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample

			Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

11.1.5.6. **I2S/PCM FIFO Control Register(Default Value: 0x0004_00F0)**

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0 : Disable 1 : Enable
30:26	/	/	/
25	R/W1C	0x0	FTX Write '1' to flush TXFIFO, self clear to '0'.
24	R/W1C	0x0	FRX Write '1' to flush RXFIFO, self clear to '0'.
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO[31:0] = {APB_WDATA[31:12], 12'h0} Mode 1: TXFIFO[31:0] = {APB_WDATA[19:0], 12'h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of RXFIFO register 01: Expanding received sample sign bit at MSB of RXFIFO register 10: Truncating received samples at high half-word of RXFIFO register and low half-word of RXFIFO register is filled by '0' 11: Truncating received samples at low half-word of RXFIFO register and high half-word of RXFIFO register is expanded by its sign bit Example for 20-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[31:12], 12'h0} Mode 1: APB_RDATA[31:0] = {12{RXFIFO[31]}, RXFIFO[31:12]}

			Mode 2: APB_RDATA [31:0] = {RXFIFO[31:16], 16'h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[31], RXFIFO[31:16]}}

11.1.5.7. **I2S/PCM FIFO Status Register(Default Value: 0x1080_0000)**

Offset: 0x0018			**Register Name: I2S/PCM_FSTA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x1	TXE TXFIFO Empty 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>= 1 Word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available 0: No available data in RXFIFO 1: More than one sample in RXFIFO (>= 1 Word)
7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO available sample word counter

11.1.5.8. **I2S/PCM DMA & Interrupt Control Register(Default Value: 0x0000_0000)**

Offset: 0x001C			**Register Name: I2S/PCM_INT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable When setting to '1', an interrupt happens when writing new audio data if TXFIFO is full.
4	R/W	0x0	TXEI_EN

			TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disable 1: Enable When setting to '1', RXFIFO DMA request line is asserted if data is available in RXFIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

11.1.5.9. I2S/PCM TXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S/PCM_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written to this register one by one. The left channel sample data is first and then the right channel sample.

11.1.5.10. I2S/PCM Clock Divide Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output Whether in slave or master mode, when this bit is set to '1', MCLK should be output.
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO

			0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

11.1.5.11. **I2S/PCM TX Counter Register(Default Value: 0x0000_0000)**

Offset: 0x0028			**Register Name: I2S/PCM_TXCNT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial

			value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

11.1.5.12. **I2S/PCM RX Counter Register(Default Value: 0x0000_0000)**

Offset: 0x002C			Register Name: I2S/PCM_RXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

11.1.5.13. **I2S/PCM Channel Configuration Register(Default Value: 0x0000_0000)**

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ 0: Normal mode for the last half cycle of BCLK in the slot 1: Turn to Hi-Z state for the last half cycle of BCLK in the slot
8	R/W	0x0	TX_STATE 0: Transfer level 0 in non-transferring slot 1: Turn to Hi-Z State (TDM) in non-transferring slot
7:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot number between CPU/DMA and RXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
3:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot number between CPU/DMA and TXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots

11.1.5.14. I2S/PCM TX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S/PCM_TXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX_OFFSET TX offset Tune, TX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX_CHSEL TX Channel (Slot) number select for each output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX_CHEN TX Channel (Slot) Enable, bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

11.1.5.15. I2S/PCM TX Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S/PCM_TXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX_CH15_MAP TX Channel 15 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
27:24	R/W	0x0	TX_CH14_MAP TX Channel 14 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th sample
23:20	R/W	0x0	TX_CH13_MAP

			TX Channel 13 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX_CH12_MAP TX Channel 12 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX_CH11_MAP TX Channel 11 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
11:8	R/W	0x0	TX_CH10_MAP TX Channel 10 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX_CH9_MAP TX Channel 9 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX_CH8_MAP TX Channel 8 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample …

			1111: 16th Sample

11.1.5.16. **I2S/PCM TX Channel Mapping Register 1(Default Value: 0x0000_0000)**

Offset: 0x0048			Register Name: I2S/PCM_TXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX_CH7_MAP TX Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX_CH6_MAP TX Channel 6 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
23:20	R/W	0x0	TX_CH5_MAP TX Channel 5 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX_CH4_MAP TX Channel 4 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX_CH3_MAP TX Channel 3 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample …

			1111: 16th Sample
11:8	R/W	0x0	TX_CH2_MAP TX Channel 2 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX_CH1_MAP TX Channel 1 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX_CH0_MAP TX Channel 0 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

11.1.5.17. **I2S/PCM RX Channel Select Register(Default Value: 0x0000_0000)**

Offset: 0x0064			**Register Name: I2S/PCM_RXCHSEL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	RX_OFFSET RX offset Tune, RX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	RX_CHSEL RX Channel (Slot) Number Select for Input 0000: 1 channel or slot … 0111: 8 channels or slots 1000: 9 channels or slots … 1111:16 channels or slots
15:0	/	/	/

11.1.5.18. **I2S/PCM RX Channel Mapping Register0(Default Value: 0x0000_0000)**

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	RX_CH15_MAP RX Channel 15 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	RX_CH14_MAP RX Channel 14 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
23:20	R/W	0x0	RX_CH13_MAP RX Channel 13 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	RX_CH12_MAP RX Channel 12 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	RX_CH11_MAP RX Channel 11 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
11:8	R/W	0x0	RX_CH10_MAP RX Channel 10 Mapping

			0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	RX_CH9_MAP RX Channel 9 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	RX_CH8_MAP RX Channel 8 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

11.1.5.19. **I2S/PCM RX Channel Mapping Register 1(Default Value: 0x0000_0000)**

Offset: 0x006C			**Register Name: I2S/PCM_RXCHMAP**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	RX_CH7_MAP RX Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	RX_CH6_MAP RX Channel 6 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
23:20	R/W	0x0	RX_CH5_MAP RX Channel 5 Mapping

			0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	RX_CH4_MAP RX Channel 4 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	RX_CH3_MAP RX Channel 3 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
11:8	R/W	0x0	RX_CH2_MAP RX Channel 2 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	RX_CH1_MAP RX Channel 1 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	RX_CH0_MAP RX Channel 0 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

11.2. DMIC

11.2.1. Overview

The DMIC controller supports a 8-channels digital microphone interface, the DMIC controller can output 128fs or 64fs (fs= ADC sample rate).

The DMIC controller includes the following features:

- Supports up to 8 channels
- Sample rate from 8 kHz to 48 kHz

11.2.2. Block Diagram

Figure 11-8 shows a block diagram of the DMIC.

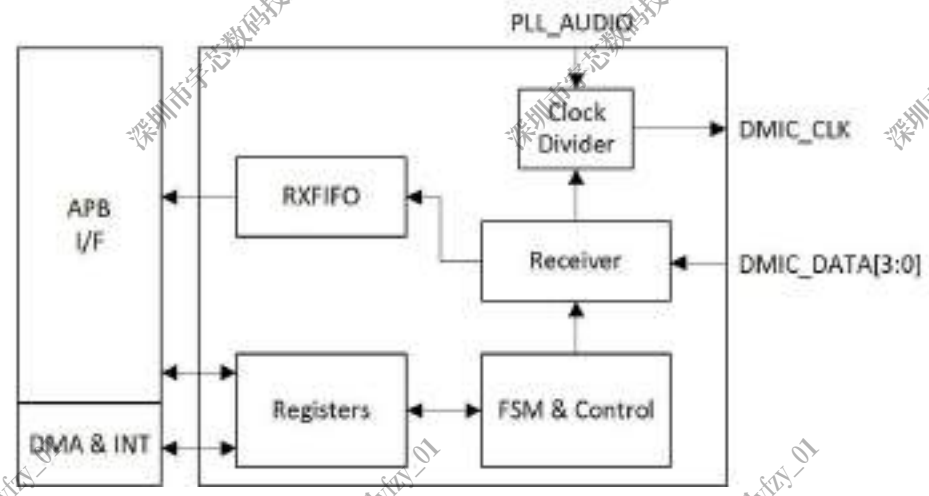


Figure 11-8. DMIC Block Diagram

11.2.3. Operations and Functional Descriptions

11.2.3.1. External Signals

Table 11-3 describes the external signals of DMIC.

Table 11-3. DMIC External Signals

Signal	Description	Type
DMIC_CLK	Digital Microphone Clock Output	O
DMIC_DATA0	Digital Microphone Data Input	I
DMIC_DATA1	Digital Microphone Data Input	I
DMIC_DATA2	Digital Microphone Data Input	I
DMIC_DATA3	Digital Microphone Data Input	I

11.2.3.2. **Clock Sources**

Table 11-4 describes the clock source for DMIC. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 11-4. DMIC Clock Sources

Clock Sources	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz serial frequency.

11.2.3.3. **Operation Mode**

The software operation of the DMIC is divided into five steps: system setup, DMIC initialization, the channel setup, DMA setup and Enable/Disable module. Five steps are described in detail in the following sections.

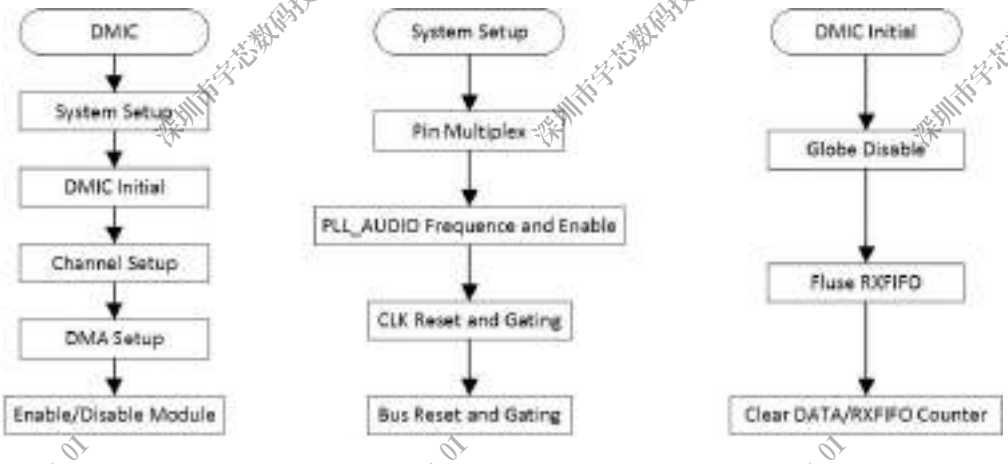


Figure 11-9. DMIC Operation Mode

11.2.3.3.1. System Setup and DMIC Initialization

The first step in the system setup is properly programming the GPIO. Because the DMIC port is a multiplex pin. You can find the function in the pin multiplex specification.

The clock source for the DMIC should be followed. At first you must disable the PLL_AUDIO through the PLL_ENABLE bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must set up the frequency of the PLL_AUDIO in the **PLL_AUDIO_CTRL_REG**. Then enable PLL_AUDIO. After that, you must open the DMIC gating through the **DMIC_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes 1. At last, you must reset and open the DMIC bus gating in the **CCU_DMIC_BGR_REG**.

After the system setup, the register of DMIC can be setup. At first, you should initialize the DMIC. You should close the **globe enable bit**(DMIC_EN[8]) , **data channel enable bit**(DMIC_EN[7:0]) by writing 0 to it. After that, you must flush the RXFIFO by writing 1 to register **DMIC_RXFIFO_CTR**[31]. At last, you can clear the Data/RXFIFO counter by writing 1 to **DMIC_RXFIFO_STA,DMIC_CNT**.

11.2.3.3.2. Channel Setup and DMA Setup

You can set up the sample rate, the sample resolution, the over sample rate, the channel number, the RXFIFO output mode and the RXFIFO trigger level and so on. The setup of register can be found in the specification.
The DMIC supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the DMA specification. In this module, you just enable the DRQ.

11.2.3.3.3. Enable and Disable DMIC

To enable the function, you can enable **data channel enable bit**(DMIC_EN[7:0]) by writing 1 to it. After that, you must enable DMIC by writing the **Globe Enable bit** to 1 in the **DMIC_EN**[8]. Write the **Globe Enable** to 0 to disable DMIC.

11.2.4. Register List

Module Name	Base Address
DMIC	0x05095000

Register Name	Offset	Description
DMIC_EN	0x0000	DMIC Enable Control Register
DMIC_SR	0x0004	DMIC Sample Rate Register
DMIC_CTR	0x0008	DMIC Control Register
DMIC_ DATA	0x0010	DMIC Data Register
DMIC_INTC	0x0014	DMIC Interrupt Control Register
DMIC_INTS	0x0018	DMIC Interrupt Status Register
DMIC_RXFIFO_CTR	0x001C	DMIC RXFIFO Control Register
DMIC_RXFIFO_STA	0x0020	DMIC RXFIFO Status Register
DMIC_CH_NUM	0x0024	DMIC Channel Numbers Register
DMIC_CH_MAP	0x0028	DMIC Channel Mapping Register
DMIC_CNT	0x002C	DMIC Counter Register
DATA0_DATA1_VOL_CTR	0x0030	Data0 and Data1 Volume Control Register
DATA2_DATA3_VOL_CTR	0x0034	Data2 And Data3 Volume Control Register
HPF_EN_CTR	0x0038	High Pass Filter Enable Control Register
HPF_COEF_REG	0x003C	High Pass Filter Coef Register
HPF_GAIN_REG	0x0040	High Pass Filter Gain Register

11.2.5. Register Description

11.2.5.1. DMIC Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMIC_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/

8	R/W	0x0	GLOBE_EN DMIC Globe Enable 0: Disable 1: Enable
7	R/W	0x0	DATA3_CHR_EN DATA3 Right Channel Enable 0: Disable 1: Enable
6	R/W	0x0	DATA3_CHL_EN DATA3 Left Channel Enable 0: Disable 1: Enable
5	R/W	0x0	DATA2_CHR_EN DATA2 Right Channel Enable 0: Disable 1: Enable
4	R/W	0x0	DATA2_CHL_EN DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	DATA1_CHR_EN DATA1 Right Channel Enable 0: Disable 1: Enable
2	R/W	0x0	DATA1_CHL_EN DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	DATA0_CHR_EN DATA0 Right Channel Enable 0: Disable 1: Enable
0	R/W	0x0	DATA0_CHL_EN DATA0 Left Channel Enable 0: Disable 1: Enable

11.2.5.2. **DMIC Sample Rate Register (Default Value: 0x0000_0000)**

Offset: 0x0004			**Register Name: DMIC_SR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	DMIC_SR Sample Rate of DMIC 000: 48 kHz

			010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit.

11.2.5.3. **DMIC Control Register (Default Value: 0x0000_0000)**

Offset: 0x0008			**Register Name: DMIC_CTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:9	R/W	0x0	DMICFDT DMIC RXFIFO Delay Time for Writing Data after GLOBE_EN 00: 5ms 01: 10ms 10: 200ms 11: 30ms
8	R/W	0x0	DMICDFEN DMIC RXFIFO Delay Function for Writing Data after GLOBE_EN 0: Disable 1: Enable
7	R/W	0x0	DATA3 Left Data and Right Data Sweep Enable 0: Disable 1: Enable
6	R/W	0x0	DATA2 Left Data and Right Data Sweep Enable 0: Disable 1: Enable
5	R/W	0x0	DATA1 Left Data and Right Data Sweep Enable 0: Disable 1: Enable
4	R/W	0x0	DATA0 Left Data and Right Data Sweep Enable 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	DMIC Oversample Rate 0: 128 (Support 8 kHz ~ 24 kHz) 1: 64 (Support 16 kHz ~ 48 kHz)

11.2.5.4. **DMIC DATA Register (Default Value: 0x0000_0000)**

Offset: 0x0010	**Register Name: DMIC_DATA**

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMIC_DATA

11.2.5.5. **DMIC Interrupt Control Register (Default Value: 0x0000_0000)**

Offset: 0x0014			Register Name: DMIC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	RXFIFO_DRQ_EN DMIC RXFIFO Data Available DRQ Enable 0: Disable 1: Enable
1	R/W	0x0	RXFIFO_OVERRUN_IRQ_EN DMIC RXFIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	DATA_IRQ_EN DMIC RXFIFO Data Available IRQ Enable 0: Disable 1: Enable

11.2.5.6. **DMIC Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0018			Register Name: DMIC_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	RXFIFO_OVERRUN_IRQ_PENDING DMIC RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Writing '1' to clear this interrupt or automatically clear if interrupt condition fails
0	R/ W1C	0x0	RXFIFO_DATA_IRQ_PENDING DMIC RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ Writing '1' to clear this interrupt or automatically clear if interrupt condition fails.

11.2.5.7. **DMIC RXFIFO Control Register (Default Value: 0x0000_0040)**

Offset: 0x001C			Register Name: DMIC_RXFIFO_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W1C	0x0	DMIC_RXFIFO_FLUSH DMIC RXFIFO Flush Writing '1' to flush RXFIFO, self clear to '0'
30:10	/	/	/
9	R/W	0x0	RXFIFO_MODE RXFIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of RXFIFO register 1: Expanding received sample sign bit at MSB of RXFIFO register For 24-bit received audio sample: Mode 0: RXDATA[31:0] = {RXFIFO_O[23:0], 8'h0} Mode 1: Reserved For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {RXFIFO_O[23:8], 16'h0} Mode 1: RXDATA[31:0] = {16{RXFIFO_O[23]}, RXFIFO_O[23:8]}
8	R/W	0x0	Sample_Resolution 0: 16-bit 1: 24- bit
7:0	R/W	0x40	RXFIFO_TRG_LEVEL RXFIFO Trigger Level (TRLV[7:0]) Interrupt and DMA request trigger level for DMIC RXFIFO normal condition IRQ/DRQ Generated when WLEVEL > TRLV[7:0]) WLEVEL represents the number of valid samples in the DMIC RXFIFO

11.2.5.8. DMIC RXFIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: DMIC_RXFIFO_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DMIC_DATA_CNT DMIC RXFIFO Available Sample Word Counter

11.2.5.9. DMIC Channel Numbers Register (Default Value: 0x0000_0001)

Offset: 0x0024			Register Name: DMIC_CH_NUM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x1	DMIC_CH_NUM DMIC Enable Channel Numbers are (N+1)

11.2.5.10. **DMIC Channel Mapping Register (Default Value: 0x7654_3210)**

Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x7	DMIC_CH7_MAP DMIC Channel 7 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
27:24	R/W	0x6	DMIC_CH6_MAP DMIC Channel 6 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
23:20	R/W	0x5	DMIC_CH5_MAP DMIC Channel 5 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
19:16	R/W	0x4	DMIC_CH4_MAP DMIC Channel 4 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
15:12	R/W	0x3	DMIC_CH3_MAP DMIC Channel 3 Mapping

			0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
11:8	R/W	0x2	DMIC_CH2_MAP DMIC Channel 2 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
7:4	R/W	0x1	DMIC_CH1_MAP DMIC Channel 1 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
3:0	R/W	0x0	DMIC_CH0_MAP DMIC Channel0 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

11.2.5.11. **DMIC Counter Register (Default Value: 0x0000_0000)**

Offset: 0x002C			**Register Name: DMIC_CNT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMIC _CNT RX Sample Counter

			The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value It is used for Audio/Video Synchronization

11.2.5.12. **DATA0 and DATA1 Volume Control Register (Default Value: 0xA0A0_A0A0)**

Offset: 0x0030			**Register Name: DATA0_DATA1_VOL_CTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	DATA1L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …… 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …… 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA1R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …… 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …… 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA0L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …… 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …… 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA0R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB

			…… 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …… 0xFF: 71.25 dB

11.2.5.13. **DATA2 and DATA3 Volume Control Register (Default Value: 0xA0A0_A0A0)**

Offset: 0x0034			**Register Name: DATA2_DATA3_VOL_CTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	DATA3L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …… 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …… 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA3R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …… 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …… 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA2L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …… 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …… 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA2R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB

			…… 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …… 0xFF: 71.25 dB

11.2.5.14. **High Pass Filter Enable Control Register (Default Value: 0x0000_0000)**

Offset: 0x0038			**Register Name: HPF_EN_CTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	HPF_DATA3_CHR_EN High Pass Filter DATA3 Right Channel Enable 0: Disable 1: Enable
6	R/W	0x0	HPF_DATA3_CHL_EN High Pass Filter DATA3 Left Channel Enable 0: Disable 1: Enable
5	R/W	0x0	HPF_DATA2_CHR_EN High Pass Filter DATA2 Right Channel Enable 0: Disable 1: Enable
4	R/W	0x0	HPF_DATA2_CHL_EN High Pass Filter DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	HPF_DATA1_CHR_EN High Pass Filter DATA1 Right Channel Enable 0: Disable 1: Enable
2	R/W	0x0	HPF_DATA1_CHL_EN High Pass Filter DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	HPF_DATA0_CHR_EN High Pass Filter DATA0 Right Channel Enable 0: Disable 1: Enable
0	R/W	0x0	HPF_DATA0_CHL_EN High Pass Filter DATA0 Left Channel Enable 0: Disable 1: Enable

11.2.5.15. **High Pass Filter Coef Register (Default Value: 0x00FF_AA45)**

Offset: 0x003C			Register Name: HPF_COEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFAA45	High Pass Filter Coefficient

11.2.5.16. **High Pass Filter Gain Register (Default Value: 0x00FF_D522)**

Offset: 0x0040			Register Name: HPF_GAIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFD522	High Pass Filter Gain

11.3. Audio Codec

11.3.1. Overview

The Audio Codec has 2 I2S/PCM interfaces, 2 channels DAC and 2 channels ADC with a high level of mixed-signal integration which ideal for smart phone and other portable devices.The DRC in the integrated hardware DAP engine can be used for record and playback paths .

The Audio Codec has the following features:

- Two audio digital-to-analog(DAC) channels
  - 16/20/24-bit sample resolution and 8 kHz to 192 kHz sample rates
  - 95±3dB SNR@A-weight, THD+N -82±3dB, output level 0.55 Vrms
  - DAC power consumption 3.1mA@1.8V
- One audio output:
  - One stereo lineout output(LINEOUTL and LINEOUTR)
- Two audio analog-to-digital(ADC) channels
  - 20-bit sample resolution and 8 kHz to 48 kHz sample rates
  - 95±3dB SNR@A-weight, THD+N -82±3dB
  - ADC power consumption 5.5mA@1.8V
- Three audio inputs:
  - Two differential microphone inputs(MICIN1P and MICIN1N, MICIN2P and MICIN2N), with boost pre-amplifiers
  - One stereo line-in input(LINEINL and LINEINR)
- Supports Dynamic Range Controller(DRC) adjusting the ADC recording output
- Supports Dynamic Range Controller(DRC) adjusting the DAC playback output
- One low-noise analog microphone bias output
- Supports analog/digital volume control
- Analog low-power loop from line-in/microphone to lineout outputs
- Two I2S/PCM interface
- One 128x24-bits FIFO for data transmit, one 64x24-bits FIFO for data receive
- Programmable FIFO thresholds
- Interrupt and DMA Support

11.3.2. Operations and Functional Descriptions

11.3.2.1. External Signals

11.3.2.1.1. Analog I/O Pins

Signal	Type	Description
MICIN1P	I	Positive differential input for MIC1
MICIN1N	I	Negative differential input for MIC1
MICIN2P	I	Positive differential input for MIC2
MICIN2N	I	Negative differential input for MIC2
LINEINL	I	Left single-end input for LINE-IN
LINEINR	I	Right single-end input for LINE-IN

LINEOUTL	O	Left single-end output for LINE-OUT
LINEOUTR	O	Right single-end output for LINE-OUT

11.3.2.1.2. Reference

Signal	Type	Description
MBIAS	O	First bias voltage output for main microphone
VRA1	O	Internal reference voltage
VRA2	O	Internal reference voltage
REXT	O	External reference pin

11.3.2.1.3. Power/Ground

Signal	Type	Description
VDD33	P	Analog power 3.3V
AVCC	P	Analog power 1.8V
AGND	G	Analog ground

11.3.2.2. Clock and Power Requirements

Table 11-5. Typical Application Clock Requirements

Operation Mode	32K	PCLK	24MHz	PLL_AUDIO
Playback	on	on	on	on
Capture	on	on	on	on

Table 11-6. Typical Application Power Requirements

Operating Mode	VDD_SYS	AVCC	CPVIN
Playback(Lineout)	on	on	on
Capture	on	on	off

11.3.2.3. Clock System

The clock source of audio codec can be selected from Audio PLL. The clock PLL_1x_24M from Audio PLL is always provided 24.576 MHz or 22.5792 MHz(fs=48 kHz or 44.1 kHz) for the I2S_AP MCLK and Mux. System clock of audio can be selected from AIF1CLK or AIF2CLK. AIF1CLK is the reference of the first AIF1 clocking zone. AIF2CLK is the reference of the second AIF2 clocking zone. And the system clocking must be synchronized with either of the AIFnCLK. The driver should arrange the divider to generate 512*fs(fs=48 kHz or 44.1 kHz) as the SYSCLK.

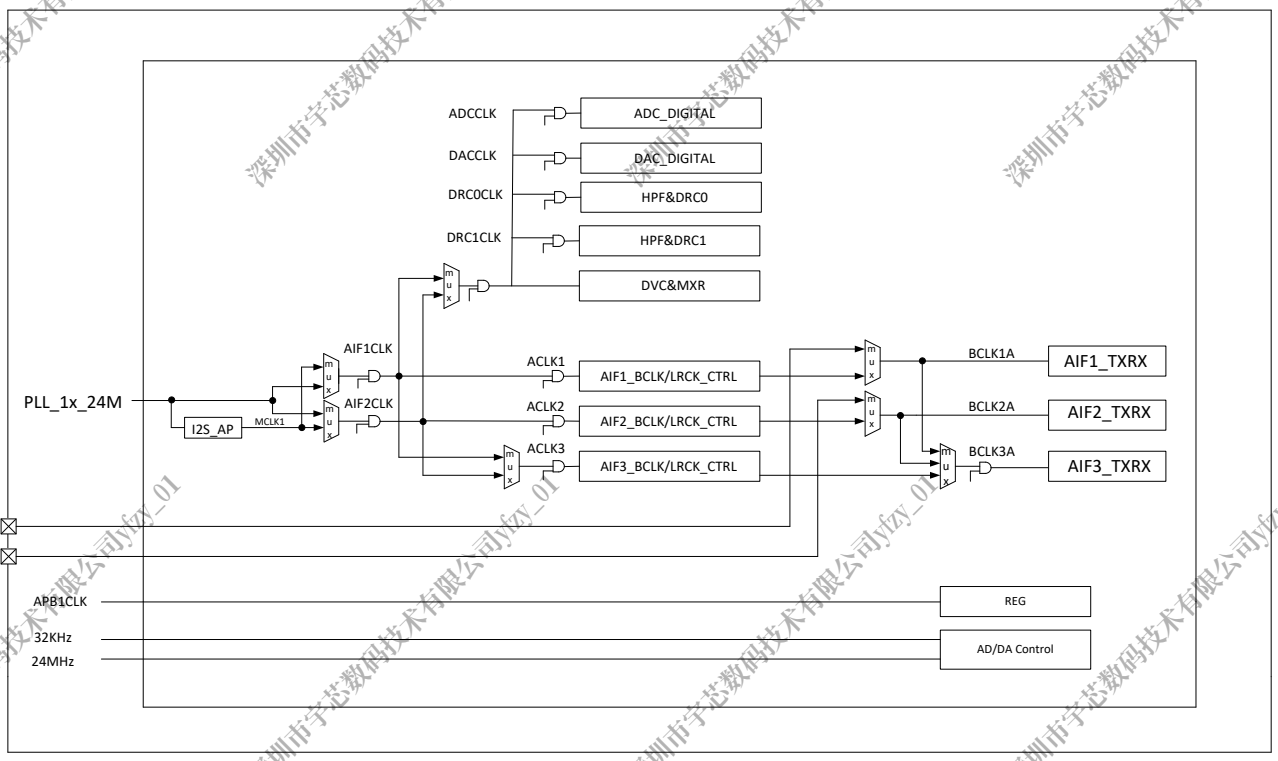


Figure 11-10. System Clock Tree

The device can work either in master clock mode or slave clock mode.In master mode, BCLK and LRCK are derived internally from AIFnCLK. In slave mode, BCLK and LRCK are supplied externally. BCLK and LRCK must be synchronously derived from the system clock with specific rates.

11.3.2.4. **Reset System**

11.3.2.4.1. Digital Part Reset System

The SYS_RST will be provided by the VDD_SYS domain. The codec register part, DVC(Digital Voice Control)&MIX and I2S_AP part will be reset by the SYS_RST during the power on or the system soft writing the reset control logic. The other parts will be reset by the soft configure through writing register.

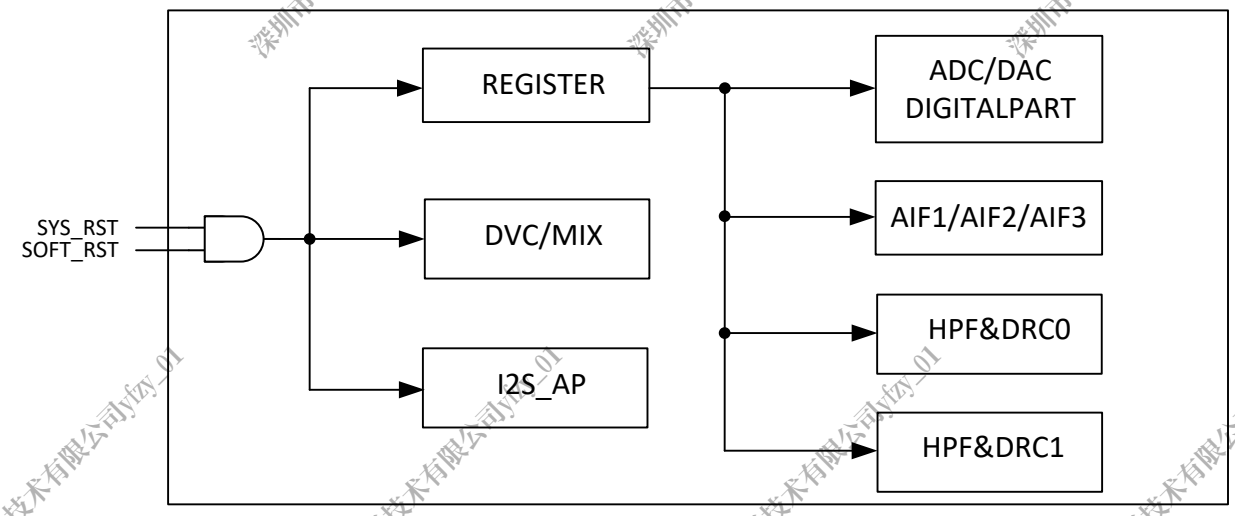


Figure 11-11. Audio Codec Digital Part Reset System

11.3.2.4.2. Analog Part Reset System

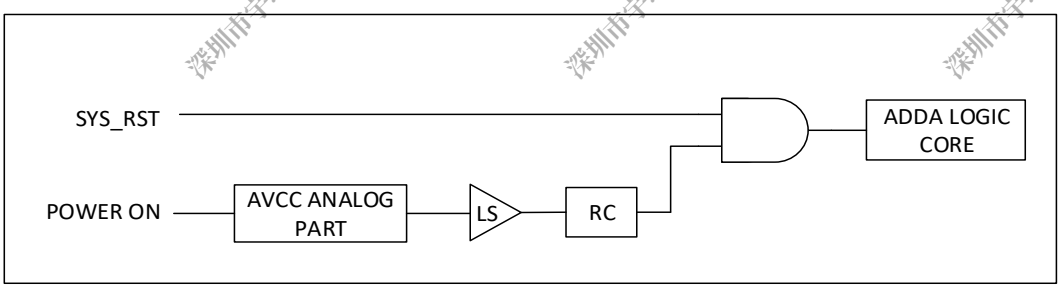


Figure 11-12. Audio Codec Analog Part Reset System

11.3.2.5. Power Domain

Audio Codec needs three powers, AVCC,VDD_SYS and VDD3 show in Figure 11-13. The AVCC is provided to ADC/DAC analog part, mic boost,mixer and reference. VDD_SYS is provided to ADC/DAC digital part, register control. VDD33 is provided to MBIAS.

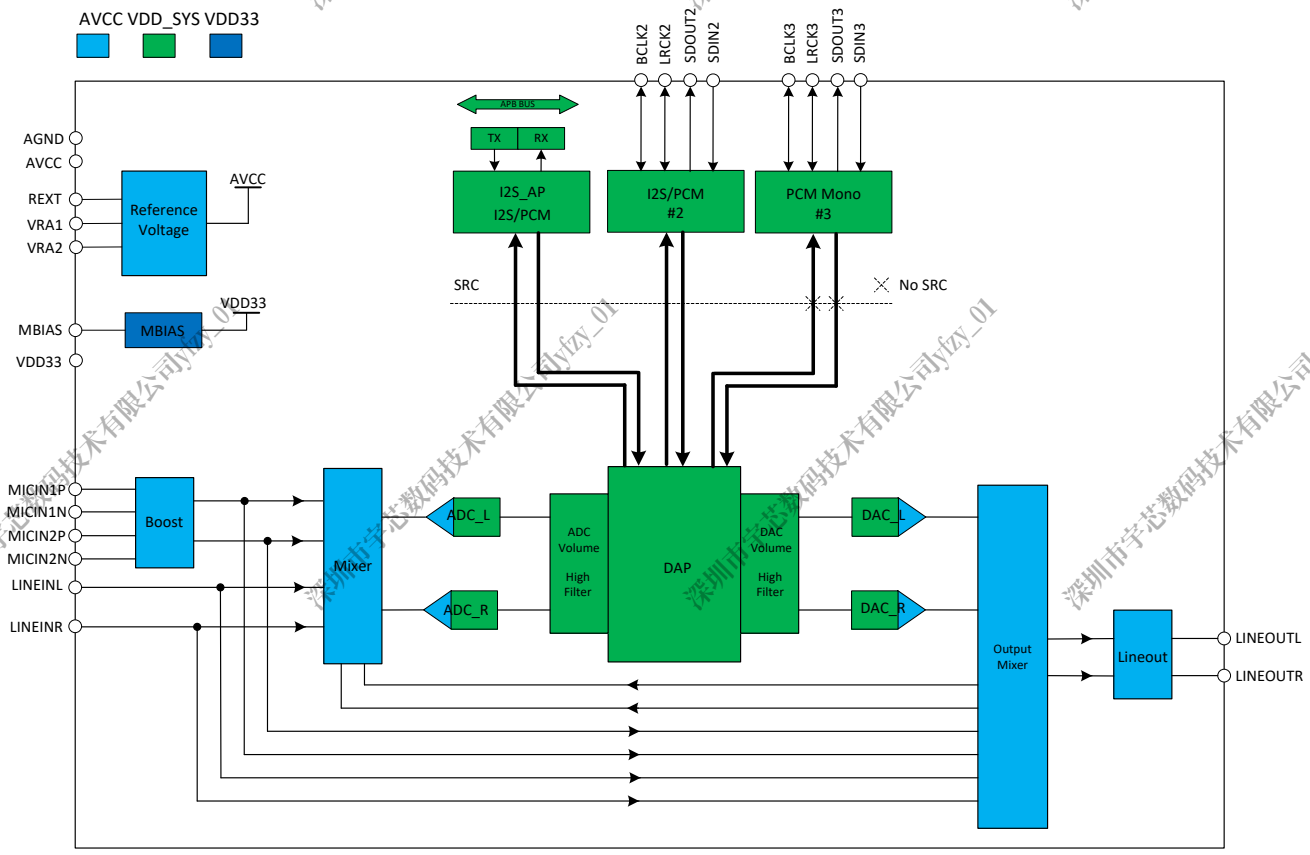


Figure 11-13. Audio Codec Power Domain

11.3.2.6. Data Path Diagram

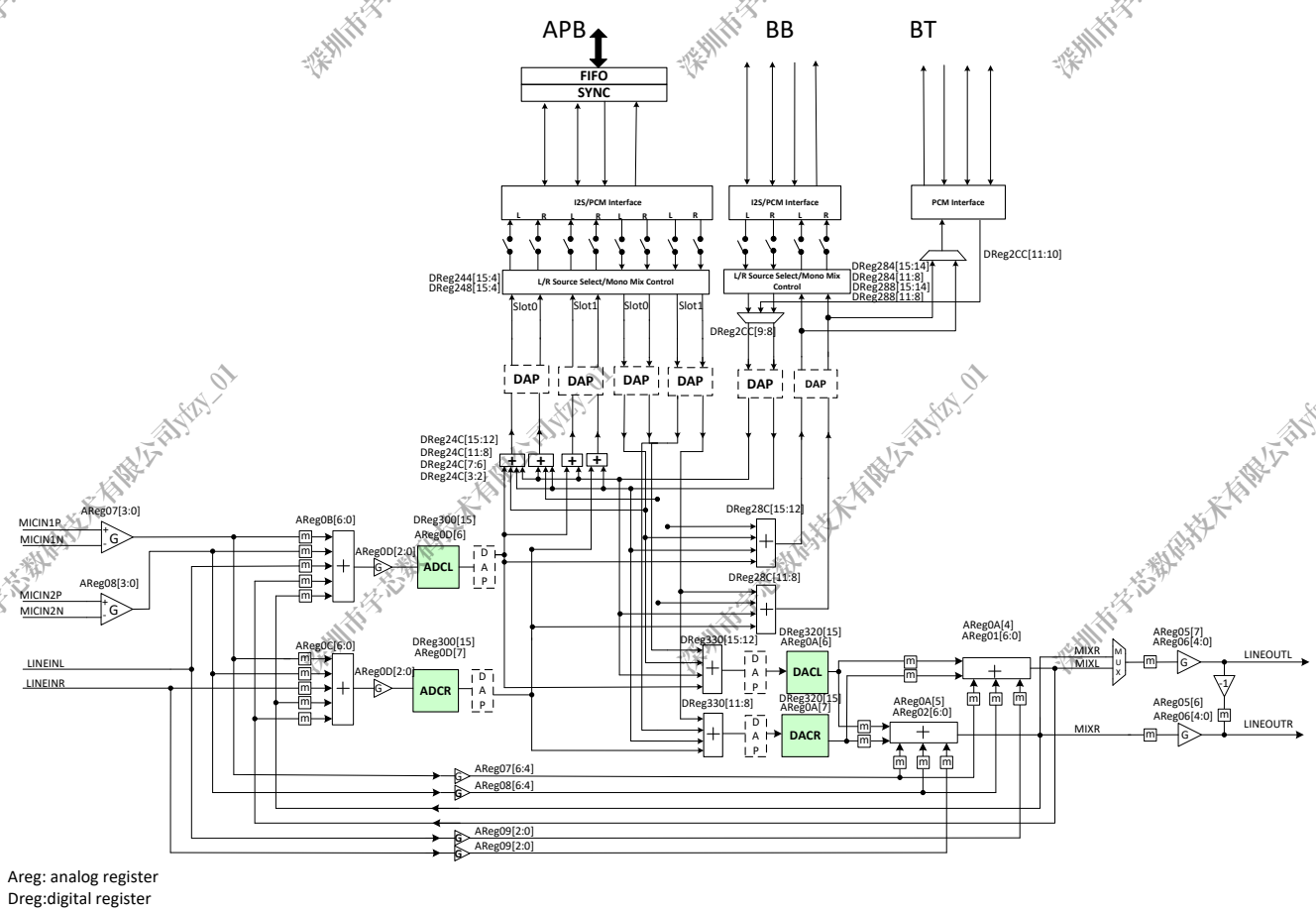


Figure 11-14. Audio Codec Data Path Diagram

11.3.2.7. Stereo ADC

The stereo ADC is used for recording stereo sound. The sample rate of the stereo ADC can not be independent of DAC sample rate. In other words, the stereo ADC and DAC must work at a same sample rate. The sample rate is configured by the register **ADDA_FS_AIF1** or **ADDA_FS_AIF2** depending on which AIFnCLK selected as the system clock(SYSCLK).

In order to save power, the left and right analog ADC part can be enabled/disabled separately by setting register the bit[7:6] of **ADC_CTRL**. The digital ADC part can be enabled/disabled by the bit15 of **ADC_DIG_CTRL**.

The volume control of the stereo ADC is set via **ADC_VOL_CTRL** .

11.3.2.8. Stereo DAC

The stereo DAC sample rate is the same as the stereo ADC. The sample rate is configured by the register **ADDA_FS_AIF1** or **ADDA_FS_AIF2** depending on which AIFnCLK selected as the system clock(SYSCLK).

In order to save power, the left and right DAC can be enabled/disabled separately by setting the bit[7:6] of **MIX_DAC_CTRL**.

The digital DAC part can be enabled/disabled by the bit15 of **DAC_DIG_CTRL**. The volume control of the stereo ADC is set via **DAC_VOL_CTRL** .

11.3.2.9. Mixer

The Codec supports three series of mixers for all function requirements:

- 2 channels DAC Output mixers
- 2 channels ADC Record mixers
- Digital mixers

(1) DAC Output Mixers

The output mixer is used to drive analog output. The following signals can be mixed into the output mixer:

- LINEINL/R
- MICIN1P/N
- MICIN2P/N
- Stereo DAC output

(2) ADC Record Mixers

The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording. The following signals can be mixed into the output mixer:

- LINEINL/R
- MICIN1P/N
- MICIN2P/N
- DAC output mixer

(3) Digital Mixers

The digital mixers are provided for digital audio data mixing on four AIF1 output paths, two AIF2 output paths and two paths to the stereo DAC. It is separately controlled by the register **AIF1_MXR_SRC**, **AIF2_MXR_SRC** and **DAC_MXR_SRC**.

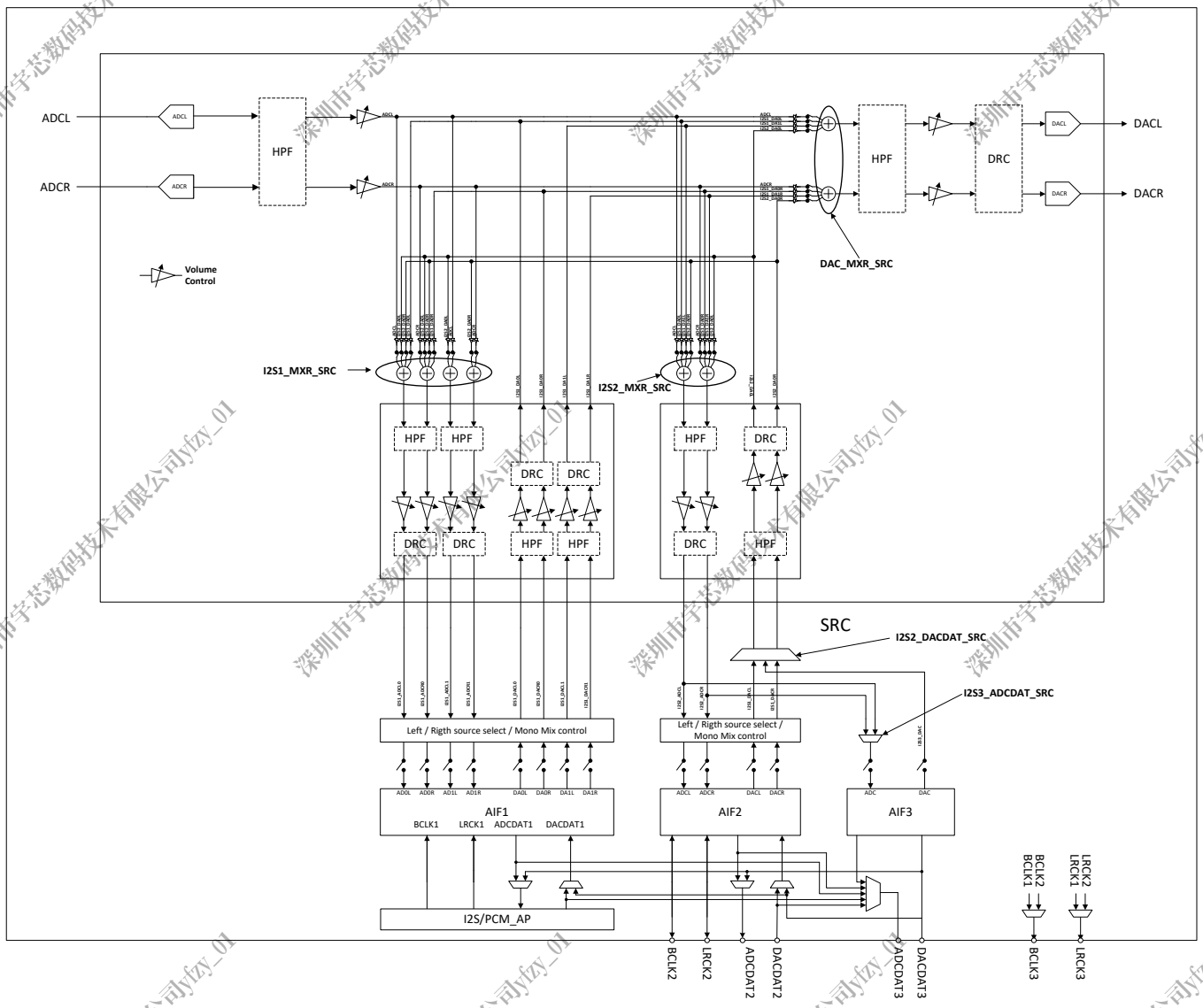


Figure 11-15. Digital Signal Data Path Diagram

11.3.2.10. **Analog Audio Input Path**

The Audio Codec supports three analog audio input paths:

- LINEINL/R
- MICIN1P/N
- MICIN2P/N

11.3.2.10.1. LINEINL/R

Linein provides 2-channel stereo single-ended input that can be mixed into the DAC output mixer and ADC record mixer. The inputs are high impedance and low capacitance, thus ideally suited to receive line level signals from external audio equipment or audio FM module .

11.3.2.10.2. Microphone Input

MICIN1P/N and MICIN2P/N provide differential input that can be mixed into the ADC record mixer, or DAC output mixer. MICIN is high impedance, low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitive. MICIN1P/N are input to the first pre-amplifier, MICIN2P/N are selected to input the 2nd pre-amplifier. Each microphone preamplifier has a separate enable bit. The gain for each pre-amplifier can be set independently . MBIAS provides reference voltage for electret condenser type(ECM) microphones.

11.3.2.11. **Analog Audio Output Path**

LINEOUTL/R provides one stereo output to drive line level signals to external audio equipment . The LINEOUTL output source can be selected from left output mixer or (left+right) output mixer. The LINEOUTR output source can be selected from right output mixer or left output mixer for differential output. The volume control is logarithmic with an 43.5dB rang in 1.5dB step from -43.5dB to 0dB. The LINEOUT output buffer is powered up or down by the bit[7:6] of **LINEOUT_CTRL0** .

11.3.2.12. **DAP**

11.3.2.12.1. DAP Data Flow

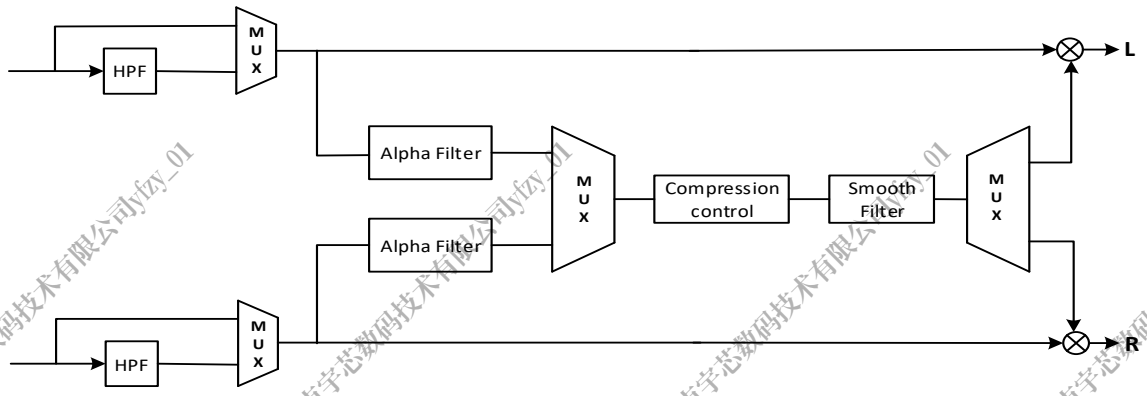


Figure 11-16. DAP Data Flow

11.3.2.12.2. HPF Function

The DAP has individual channel high pass filter (HPF, -3dB cutoff < 1Hz) that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz that can be removed DC offset from ADC recording. The HPF can also be bypassed.

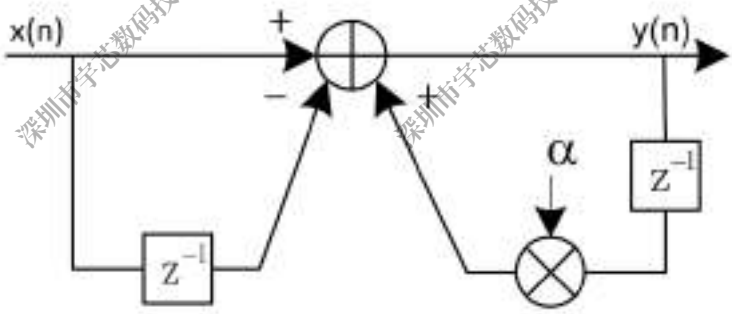


Figure 11-17. HPF Function

11.3.2.13. **AIF Interface**

The AIF2 and AIF3 interfaces provide flexible connectivity with multiple processors.

The AIF2 interface can be configured as master or slave, the AIF3 interface operates in master mode and supports PCM mode only.

In the general case, the digital audio interface uses four pins as below:

- BCLK: Bit clock for data synchronization
- LRCK: Left/Right data alignment clock
- SDOUT: output data for ADC data
- SDIN: input data for DAC data

The AIF2 interface supports four different data formats as below. But the AIF3 interface supports PCM short mode only.

- I2S mode
- Left justified mode
- Right justified mode
- PCM short mode

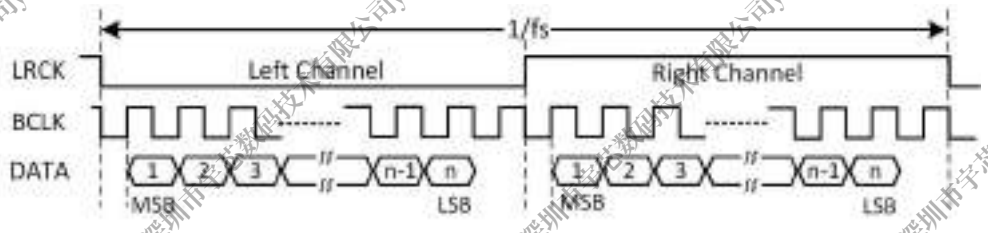


Figure 11-18. I2S Justified Mode

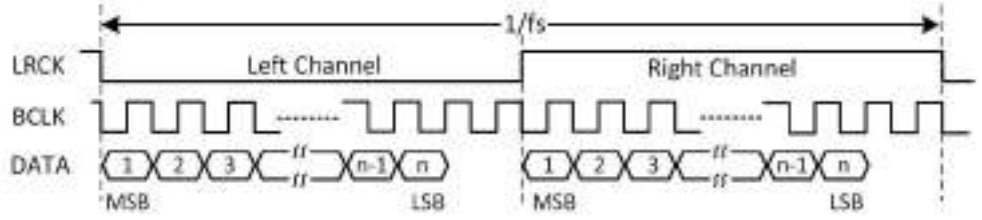


Figure 11-19. Left Justified Mode

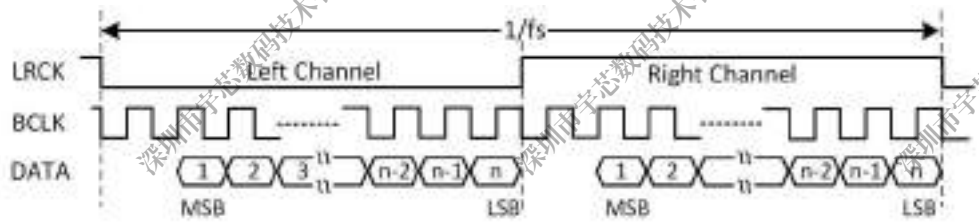


Figure 11-20. Right Justified Mode

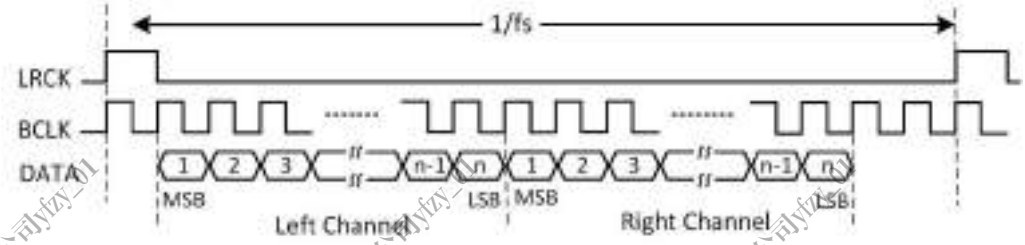


Figure 11-21. PCM Mode (LRCK_INV=0)

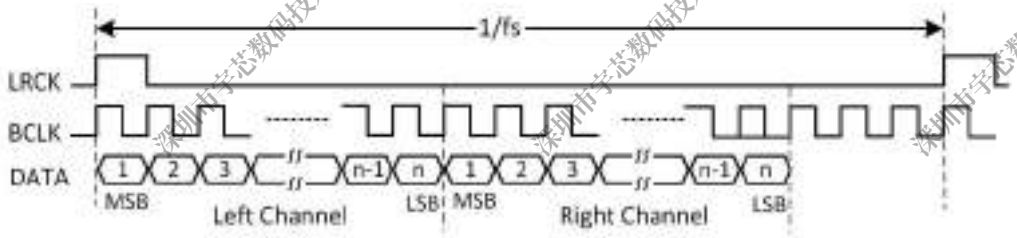


Figure 11-22. PCM Mode (LRCK_INV=1)

11.3.2.14. **Typical Application**

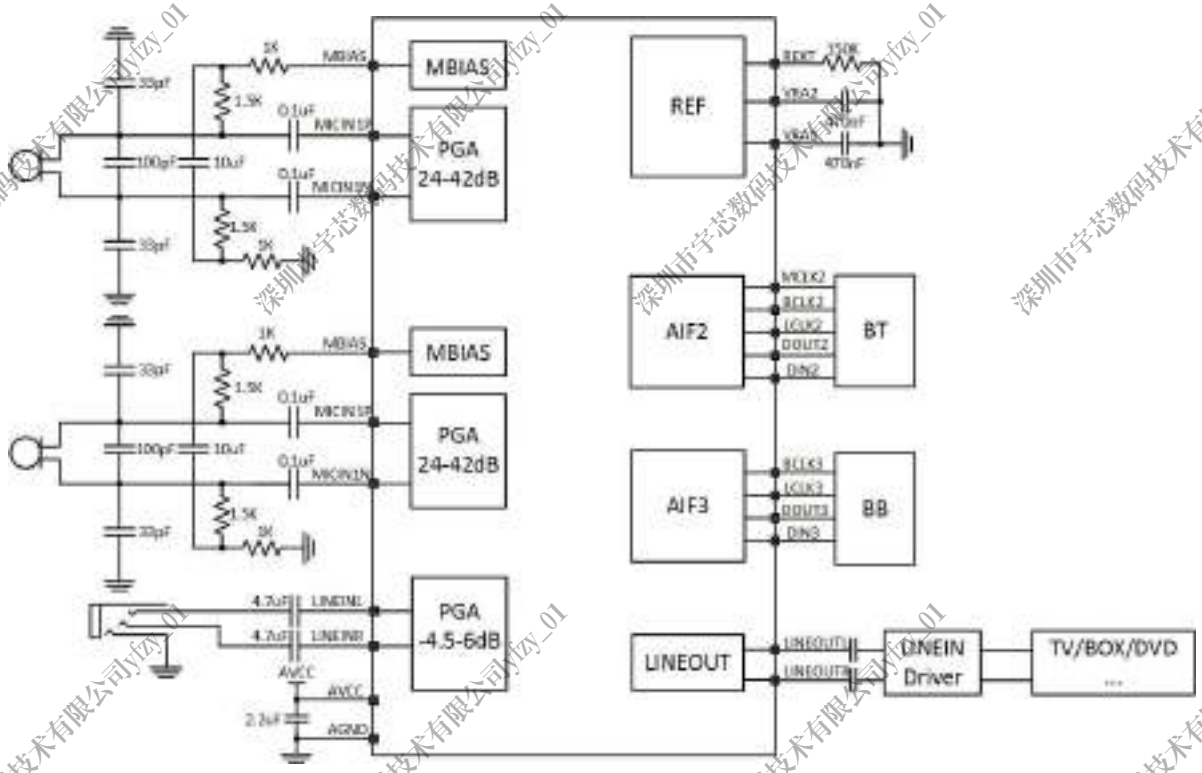


Figure 11-23. Audio Codec Typical Application Diagram

11.3.3. Programming Guidelines

11.3.3.1. Playback Process

(1) Codec initial: Open audio codec bus clock gating and de-assert bus reset through **AUDIO_CODEC_BGR_REG**, configure PLL_Audio frequency and enable PLL_Audio through **PLL_AUDIO_CTRL_REG**. Please refer to CCU in chapter 3.3 about detail.
(2) Configure MIX path.
(3) Set sample rate,configure data transfer format, open DAC.
(4) DMA configure and DMA request.
(5) Enable DAC DRQ and DMA.

11.3.3.2. Record Process

(1) Codec initial: Open audio codec bus clock gating and de-assert bus reset through **AUDIO_CODEC_BGR_REG**, configure PLL_Audio frequency and enable PLL_Audio through **PLL_AUDIO_CTRL_REG**.Please refer to CCU in chapter 3.3 about detail.
(2) Configure MIX path.
(3) Set sample rate,configure data transfer format, open ADC.
(4) DMA configure and DMA request.
(5) Enable ADC DRQ and DMA.

11.3.4. Register List

Module Name	Base Address
Audio Codec	0x05096000

Register Name	Offset	Description
DA_CTL	0x0000	Digital Audio Control Register
DA_FAT0	0x0004	Digital Audio Format Register 0
DA_FAT1	0x0008	Digital Audio Format Register 1
DA_ISTA	0x000C	Digital Audio Interrupt Status Register
DA_RXFIFO	0x0010	Digital Audio RX FIFO Register
DA_FCTL	0x0014	Digital Audio FIFO Control Register
DA_FSTA	0x0018	Digital Audio FIFO Status Register
DA_INT	0x001C	Digital Audio Interrupt Control Register
DA_TXFIFO	0x0020	Digital Audio TX FIFO Register
DA_CLKD	0x0024	Digital Audio Clock Divide Register
DA_TXCNT	0x0028	Digital Audio RX Sample Counter Register
DA_RXCNT	0x002C	Digital Audio TX Sample Counter Register
DA_TXCHSEL	0x0030	Digital Audio TX Channel Select register
DA_TXCHMAP	0x0034	Digital Audio TX Channel Mapping Register
DA_RXCHSEL	0x0038	Digital Audio RX Channel Select register
DA_RXCHMAP	0x003C	Digital Audio RX Channel Mapping Register

SYSCLK_CTL	0x020C	System Clock Control Register
MOD_CLK_ENA	0x0210	Module Clock Control Register
MOD_RST_CTL	0x0214	Module Reset Control Register
SYS_SR_CTRL	0x0218	System Sample rate Configuration Register
SYS_DVC_MOD	0x0220	System DVC Mode Select Register
AIF1CLK_CTRL	0x0240	AIF1 BCLK/LRCK Control Register
AIF1_ADCDAT_CTRL	0x0244	AIF1 ADCDAT Control Register
AIF1_DACDAT_CTRL	0x0248	AIF1 DACDAT Control Register
AIF1_MIXR_SRC	0x024C	AIF1 Digital Mixer Source Select Register
AIF1_VOL_CTRL1	0x0250	AIF1 Volume Control 1 Register
AIF1_VOL_CTRL2	0x0254	AIF1 Volume Control 2 Register
AIF1_VOL_CTRL3	0x0258	AIF1 Volume Control 3 Register
AIF1_VOL_CTRL4	0x025C	AIF1 Volume Control 4 Register
AIF1_MXR_GAIN	0x0260	AIF1 Digital Mixer Gain Control Register
AIF1_RXD_CTRL	0x0264	AIF1 Receiver Data Discarding Control Register
AIF2_CLK_CTRL	0x0280	AIF2 BCLK/LRCK Control Register
AIF2_ADCDAT_CTRL	0x0284	AIF2 ADCDAT Control Register
AIF2_DACDAT_CTRL	0x0288	AIF2 DACDAT Control Register
AIF2_MXR_SRC	0x028C	AIF2 Digital Mixer Source Select Register
AIF2_VOL_CTRL1	0x0290	AIF2 Volume Control 1 Register
AIF2_VOL_CTRL2	0x0298	AIF2 Volume Control 2 Register
AIF2_MXR_GAIN	0x02A0	AIF2 Digital Mixer Gain Control Register
AIF2_RXD_CTRL	0x02A4	AIF2 Receiver Data Discarding Control Register
AIF3_CLK_CTRL	0x02C0	AIF3 BCLK/LRCK Control Register
AIF3_ADCDAT_CTRL	0x02C4	AIF3 ADCDAT Control Register
AIF3_DACDAT_CTRL	0x02C8	AIF3 DACDAT Control Register
AIF_SGP_CTRL	0x02CC	AIF Signal Path Control Register
AIF3_RXD_CTRL	0x02E4	AIF3 Receiver Data Discarding Control Register
ADC_DIG_CTRL	0x0300	ADC Digital Control Register
ADC_VOL_CTRL	0x0304	ADC Volume Control Register
DAC_DIG_CTRL	0x0320	DAC Digital Control Register
DAC_VOL_CTRL	0x0324	DAC Volume Control Register
DAC_DBG_CTRL	0x0328	DAC Debug Control Register
DAC_MXR_SRC	0x0330	DAC Digital Mixer Source Select Register
DAC_MXR_GAIN	0x0334	DAC Digital Mixer Gain Control Register
AC_DAC_DAPCTRL	0x0480	DAC DAP Control Register
AGC_ENA	0x04D0	AGC Enable Register
DRC_ENA	0x04D4	DRC Enable Register
AC_DRC0_HHPFC	0x0600	DRC0 High HPF Coef Register
AC_DRC0_LHPFC	0x0604	DRC0 Low HPF Coef Register
AC_DRC0_CTRL	0x0608	DRC0 Control Register
AC_DRC0_LPFHAT	0x060C	DRC0 Left Peak Filter High Attack Time Coef Register
AC_DRC0_LPFLAT	0x0610	DRC0 Left Peak Filter Low Attack Time Coef Register
AC_DRC0_RPFHAT	0x0614	DRC0 Right Peak Filter High Attack Time Coef Register
AC_DRC0_RPFLAT	0x0618	DRC0 Peak Filter Low Attack Time Coef Register

AC_DRC0_LPFHRT	0x061C	DRC0 Left Peak Filter High Release Time Coef Register
AC_DRC0_LPFLRT	0x0620	DRC0 Left Peak Filter Low Release Time Coef Register
AC_DRC0_RPFHRT	0x0624	DRC0 Right Peak filter High Release Time Coef Register
AC_DRC0_RPFLRT	0x0628	DRC0 Right Peak filter Low Release Time Coef Register
AC_DRC0_LRMSHAT	0x062C	DRC0 Left RMS Filter High Coef Register
AC_DRC0_LRMSLAT	0x0630	DRC0 Left RMS Filter Low Coef Register
AC_DRC0_RRMSHAT	0x0634	DRC0 Right RMS Filter High Coef Register
AC_DRC0_RRMSLAT	0x0638	DRC0 Right RMS Filter Low Coef Register
AC_DRC0_HCT	0x063C	DRC0 Compressor Threshold High Setting Register
AC_DRC0_LCT	0x0640	DRC0 Compressor Threshold Low Setting Register
AC_DRC0_HKC	0x0644	DRC0 Compressor Slope High Setting Register
AC_DRC0_LKC	0x0648	DRC0 Compressor Slope Low Setting Register
AC_DRC0_HOPC	0x064C	DRC0 Compressor High Output at Compressor Threshold Register
AC_DRC0_LOPC	0x0650	DRC0 Compressor Low Output at Compressor Threshold Register
AC_DRC0_HLT	0x0654	DRC0 Limiter Threshold High Setting Register
AC_DRC0_LLT	0x0658	DRC0 Limiter Threshold Low Setting Register
AC_DRC0_HKl	0x065C	DRC0 Limiter Slope High Setting Register
AC_DRC0_LKl	0x0660	DRC0 Limiter Slope Low Setting Register
AC_DRC0_HOPL	0x0664	DRC0 Limiter High Output at Limiter Threshold
AC_DRC0_LOPL	0x0668	DRC0 Limiter Low Output at Limiter Threshold
AC_DRC0_HET	0x066C	DRC0 Expander Threshold High Setting Register
AC_DRC0_LET	0x0670	DRC0 Expander Threshold Low Setting Register
AC_DRC0_HKE	0x0674	DRC0 Expander Slope High Setting Register
AC_DRC0_LKE	0x0678	DRC0 Expander Slope Low Setting Register
AC_DRC0_HOPE	0x067C	DRC0 Expander High Output at Expander Threshold
AC_DRC0_LOPE	0x0680	DRC0 Expander Low Output at Expander Threshold
AC_DRC0_HKN	0x0684	DRC0 Linear Slope High Setting Register
AC_DRC0_LKN	0x0688	DRC0 Linear Slope Low Setting Register
AC_DRC0_SFHAT	0x068C	DRC0 Smooth filter Gain High Attack Time Coef Register
AC_DRC0_SFLAT	0x0690	DRC0 Smooth filter Gain Low Attack Time Coef Register
AC_DRC0_SFHRT	0x0694	DRC0 Smooth filter Gain High Release Time Coef Register
AC_DRC0_SFLRT	0x0698	DRC0 Smooth filter Gain Low Release Time Coef Register
AC_DRC0_MXGHS	0x069C	DRC0 MAX Gain High Setting Register
AC_DRC0_MXGLS	0x06A0	DRC0 MAX Gain Low Setting Register
AC_DRC0_MNGHS	0x06A4	DRC0 MIN Gain High Setting Register
AC_DRC0_MNGLS	0x06A8	DRC0 MIN Gain Low Setting Register
AC_DRC0_EPSHC	0x06AC	DRC0 Expander Smooth Time High Coef Register
AC_DRC0_EPSLC	0x06B0	DRC0 Expander Smooth Time Low Coef Register
AC_DRC0_HPFHGAIN	0x06B8	DRC0 HPF Gain High Coef Register
AC_DRC0_HPFHGAIN	0x06BC	DRC0 HPF Gain Low Coef Register
AC_DRC1_HHPFC	0x0700	DRC1 High HPF Coef Register
AC_DRC1_LHPFC	0x0704	DRC1 Low HPF Coef Register
AC_DRC1_CTRL	0x0708	DRC1 Control Register
AC_DRC1_LPFHAT	0x070C	DRC1 Left Peak Filter High Attack Time Coef Register
AC_DRC1_LPFLAT	0x0710	DRC1 Left Peak Filter Low Attack Time Coef Register

AC_DRC1_RPFHAT	0x0714	DRC1 Right Peak Filter High Attack Time Coef Register
AC_DRC1_RPFLAT	0x0718	DRC1 Peak Filter Low Attack Time Coef Register
AC_DRC1_LPFHRT	0x071C	DRC1 Left Peak Filter High Release Time Coef Register
AC_DRC1_LPFLRT	0x0720	DRC1 Left Peak Filter Low Release Time Coef Register
AC_DRC1_RPFHRT	0x0724	DRC1 Right Peak filter High Release Time Coef Register
AC_DRC1_RPFLRT	0x0728	DRC1 Right Peak filter Low Release Time Coef Register
AC_DRC1_LRMSHAT	0x072C	DRC1 Left RMS Filter High Coef Register
AC_DRC1_LRMSLAT	0x0730	DRC1 Left RMS Filter Low Coef Register
AC_DRC1_RRMSHAT	0x0734	DRC1 Right RMS Filter High Coef Register
AC_DRC1_RRMSLAT	0x0738	DRC1 Right RMS Filter Low Coef Register
AC_DRC1_HCT	0x073C	DRC1 Compressor Threshold High Setting Register
AC_DRC1_LCT	0x0740	DRC1 Compressor Threshold Low Setting Register
AC_DRC1_HKC	0x0744	DRC1 Compressor Slope High Setting Register
AC_DRC1_LKC	0x0748	DRC1 Compressor Slope Low Setting Register
AC_DRC1_HOPC	0x074C	DRC1 Compressor High Output at Compressor Threshold Register
AC_DRC1_LOPC	0x0750	DRC1 Compressor Low Output at Compressor Threshold Register
AC_DRC1_HLT	0x0754	DRC1 Limiter Threshold High Setting Register
AC_DRC1_LLT	0x0758	DRC1 Limiter Threshold Low Setting Register
AC_DRC1_HKl	0x075C	DRC1 Limiter Slope High Setting Register
AC_DRC1_LKl	0x0760	DRC1 Limiter Slope Low Setting Register
AC_DRC1_HOPL	0x0764	DRC1 Limiter High Output at Limiter Threshold
AC_DRC1_LOPL	0x0768	DRC1 Limiter Low Output at Limiter Threshold
AC_DRC1_HET	0x076C	DRC1 Expander Threshold High Setting Register
AC_DRC1_LET	0x0770	DRC1 Expander Threshold Low Setting Register
AC_DRC1_HKE	0x0774	DRC1 Expander Slope High Setting Register
AC_DRC1_LKE	0x0778	DRC1 Expander Slope Low Setting Register
AC_DRC1_HOPE	0x077C	DRC1 Expander High Output at Expander Threshold
AC_DRC1_LOPE	0x0780	DRC1 Expander Low Output at Expander Threshold
AC_DRC1_HKN	0x0784	DRC1 Linear Slope High Setting Register
AC_DRC1_LKN	0x0788	DRC1 Linear Slope Low Setting Register
AC_DRC1_SFHAT	0x078C	DRC1 Smooth filter Gain High Attack Time Coef Register
AC_DRC1_SFLAT	0x0790	DRC1 Smooth filter Gain Low Attack Time Coef Register
AC_DRC1_SFHRT	0x0794	DRC1 Smooth filter Gain High Release Time Coef Register
AC_DRC1_SFLRT	0x0798	DRC1 Smooth filter Gain Low Release Time Coef Register
AC_DRC1_MXGHS	0x079C	DRC1 MAX Gain High Setting Register
AC_DRC1_MXGLS	0x07A0	DRC1 MAX Gain Low Setting Register
AC_DRC1_MNGHS	0x07A4	DRC1 MIN Gain High Setting Register
AC_DRC1_MNGLS	0x07A8	DRC1 MIN Gain Low Setting Register
AC_DRC1_EPSHC	0x07AC	DRC1 Expander Smooth Time High Coef Register
AC_DRC1_EPSLC	0x07B0	DRC1 Expander Smooth Time Low Coef Register
AC_DRC1_HPFHGAIN	0x07B8	DRC1 HPF Gain High Coef Register
AC_DRC1_HPFHGAIN	0x07BC	DRC1 HPF Gain Low Coef Register
Analog Domain Register		
LO_MIX_CTRL	0x01	Left Output Mixer Control Register
RO_MIX_CTRL	0x02	Right Output Mixer Control Register

LINEOUT_CTRL0	0x05	LINEOUT Control Register 0
LINEOUT_CTRL1	0x06	LINEOUT Control Register 1
MIC1_CTRL	0x07	MIC1 Control Register
MIC2_CTRL	0x08	MIC2 Control Register
LINEIN_CTRL	0x09	Linein Control Register
MIX_DAC_CTRL	0x0A	Mixer and DAC Control Register
LO_MIX_CTRL	0x0B	Left Output Mixer Control Register
RO_MIX_CTRL	0x0C	Right Output Mixer Control Register
ADC_CTRL	0x0D	ADC Control Register
MBIAS_CTRL	0x0E	Microphone Bias Control Register
APT_REG	0x0F	Analog Performance Tuning Register
ZC_VOL_CTRL	0x12	Zero Cross &USB Bias Control Register
BD_CAL_CTRL	0x15	Bias & DA16 Calibration Control Register

11.3.5. Register Description

11.3.5.1. I2S_AP Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	SDO_EN 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	ASS Audio sample select when TX FIFO underrun 0: Sending zero 1: Sending last audio sample
5	R/W	0x0	MS Master Slave Select 0: Master 1: Slave
4	R/W	0x0	PCM 0: I2S Interface 1: PCM Interface
3	R/W	0x0	LOOP Loop back test 0: Normal mode 1: Loop back test When set '1', connecting the SDO with the SDI in Master mode.
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable

1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

11.3.5.2. **I2S_AP Format Register 0(Default Value: 0x0000_000C)**

Offset: 0x0004			**Register Name: DA_FAT0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	LRCP Left/ Right Clock Parity 0: Normal 1: Inverted In DSP/ PCM mode 0: MSB is available on 2nd BCLK rising edge after LRC rising edge 1: MSB is available on 1st BCLK rising edge after LRC rising edge
6	R/W	0x0	BCP BCLK Parity 0: Normal 1: Inverted
5:4	R/W	0x0	SR Sample Resolution 00: 16-bit 01: 20-bit 10: 24-bit 11: Reserved
3:2	R/W	0x3	WSS Word Select Size 00: 16 BCLK 01: 20 BCLK 10: 24 BCLK 11: 32 BCLK
1:0	R/W	0x0	FMT Serial Data Format 00: Standard I2S Format 01: Left Justified Format 10: Right Justified Format 11: Reserved

11.3.5.3. **I2S_AP Format Register 1(Default Value: 0x0000_4020)**

Offset: 0x0008			Register Name: DA_FAT1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x4	PCM_SYNC_PERIOD PCM SYNC Period Clock Number 000: 16 BCLK period 001: 32 BCLK period 010: 64 BCLK period 011: 128 BCLK period 100: 256 BCLK period Others : Reserved
11	R/W	0x0	PCM_SYNC_OUT PCM Sync Out 0: Enable PCM_SYNC output in Master mode 1: Suppress PCM_SYNC whilst keeping PCM_CLK running. Some Codec utilize this to enter a low power state.
10	R/W	0x0	PCM Out Mute Write 1 force PCM_OUT to 0
9	R/W	0x0	MLS MSB / LSB First Select 0: MSB First 1: LSB First
8	R/W	0x0	SEXT Sign Extend (only for 16 bit slot) 0: Zeros or audio gain padding at LSB position 1: Sign extension at MSB position When writing the bit is 0, the unused bits are audio gain for 13-bit linear sample and zeros padding for 8-bit companding sample. When writing the bit is 1, the unused bits are both sign extension.
7:6	R/W	0x0	SI Slot Index 00: the 1st slot 01: the 2nd slot 10: the 3rd slot 11: the 4th slot
5	R/W	0x1	SW Slot Width 0: 8 clocks width 1: 16 clocks width For A-law or u-law PCM sample, if this bit is set to 1, eight zero bits are following with PCM sample.
4	R/W	0x0	SSYNC

			Short Sync Select 0: Long Frame Sync 1: Short Frame Sync It should be set '1' for 8 clocks width slot.
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: 16-bit Linear PCM 01: 8-bit Linear PCM 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: 16-bit Linear PCM 01: 8-bit Linear PCM 10: 8-bit u-law 11: 8-bit A-law

11.3.5.4. **I2S_AP Interrupt Status Register(Default Value: 0x0000_0010)**

Offset: 0x000C			**Register Name: DA_ISTA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/WC	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No pending interrupt 1: FIFO underrun pending interrupt Write '1' to clear this interrupt
5	R/WC	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No pending interrupt 1: FIFO overrun pending interrupt Write '1' to clear this interrupt
4	R/WC	0x1	TXE_INT TX FIFO empty pending interrupt 0: No pending IRQ 1: FIFO empty pending interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
3	/	/	/
2	R/WC	0x0	RXU_INT RX FIFO Underrun Pending Interrupt 0: No pending interrupt 1: FIFO underrun pending interrupt Write 1 to clear this interrupt
1	R/WC	0x0	RXO_INT

			RX FIFO Overrun Pending Interrupt 0: No pending IRQ 1: FIFO overrun pending IRQ Write '1' to clear this interrupt
0	R/WC	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.

11.3.5.5. **I2S_AP RX FIFO Register(Default Value: 0x0000_0000)**

Offset: 0x0010			**Register Name: DA_RXFIFO**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

11.3.5.6. **I2S_AP FIFO Control Register(Default Value: 0x0004_00F0)**

Offset: 0x0014			**Register Name: DA_FCTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0: Disable 1: Enable
30:26	/	/	/
25	R/WC	0x0	FTX Write '1' to flush TX FIFO, automatic clear to '0'.
24	R/WC	0x0	FRX Write '1' to flush RX FIFO, automatic clear to '0'.
23:19	/	/	/
18:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. When the number of data is less than Trigger level, the interrupt or DMA pending will be set. Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition.

			When the number of data is higher than Trigger level, the interrupt or DMA pending will be set. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TX FIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bits transmitted audio sample: Mode 0: FIFO_I[23:0] = { APB_WDATA [31:12], 4'h0} Mode 1: FIFO_I[23:0] = { APB_WDATA [19:0], 4'h0}
1:0	R/W	0x0	RXOM RX FIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of DA_RXFIFO register. 01: Expanding received sample sign bit at MSB of DA_RXFIFO register. 10: Truncating received samples at high half-word of DA_RXFIFO register and low half-word of DA_RXFIFO register is filled by '0'. 11: Truncating received samples at low half-word of DA_RXFIFO register and high half-word of DA_RXFIFO register is expanded by its sign bit. Example for 20-bits received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[19:0], 12'h0} Mode 1: APB_RDATA[31:0] = {12{RXFIFO[19]}, RXFIFO[19:0]} Mode 2: APB_RDATA [31:0] = {RXFIFO[19:4], 16'h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[19], RXFIFO[19:4]}

11.3.5.7. I2S_AP FIFO Status Register(Default Value: 0x1080_0000)

Offset: 0x0018			Register Name: DA_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x1	TXE TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
7	/	/	/
6:0	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter

11.3.5.8. **I2S_AP DMA & Interrupt Control Register(Default Value: 0x0000_0000)**

Offset: 0x001C			Register Name: DA_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TX FIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to '1', an interrupt happens when writing new audio data if TX FIFO is full.
4	R/W	0x0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RX_DRQ RX FIFO Data Available DRQ Enable 0: Disable 1: Enable When set to '1', RXFIFO DMA Request line is asserted if Data is available in RX FIFO.
2	R/W	0x0	RXUI_EN RX FIFO Underrun Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable

11.3.5.9. **I2S_AP TX FIFO Register(Default Value: 0x0000_0000)**

Offset: 0x0020			Register Name: DA_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

11.3.5.10. **I2S_AP Clock Divide Register(Default Value: 0x0000_0000)**

Offset: 0x0024			Register Name: DA_CLKD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output Whether in Slave or Master mode, when this bit is set to 1, MCLK should be output.
6:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from MCLK 000: Divide by 2 (BCLK = MCLK/2) 001: Divide by 4 010: Divide by 6 011: Divide by 8 100: Divide by 12 101: Divide by 16 110: Divide by 32 111: Divide by 64
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from Audio PLL Output 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0011: Divide by 6 0100: Divide by 8 0101: Divide by 12 0110: Divide by 16 0111: Divide by 24 1000: Divide by 32 1001: Divide by 48 1010: Divide by 64 Others : Reserved

11.3.5.11. **I2S_AP TX Counter Register(Default Value: 0x0000_0000)**

Offset: 0x0028			Register Name: DA_TXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value.

11.3.5.12. **I2S_AP RX Counter Register(Default Value: 0x0000_0000)**

Offset: 0x002C			Register Name: DA_RXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by I2S_AP Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value.

11.3.5.13. **I2S_AP TX Channel Select Register(Default Value: 0x0000_0001)**

Offset: 0x0030			Register Name: DA_TXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x1	TX_CHSEL TX Channel Select 000: 1-ch 001: 2-ch 010: 3-ch 011: 4-ch

11.3.5.14. **I2S_AP TX Channel Mapping Register(Default Value: 0x7654_3210)**

Offset: 0x0034			Register Name: DA_TXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x3	TX_CH3_MAP TX Channel3 Mapping

			000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 1xx: Reserved
11	/	/	/
10:8	R/W	0x2	TX_CH2_MAP TX Channel2 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 1xx: Reserved
7	/	/	/
6:4	R/W	0x1	TX_CH1_MAP TX Channel1 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 1xx: Reserved
3	/	/	/
2:0	R/W	0x0	TX_CH0_MAP TX Channel0 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 1xx: Reserved

11.3.5.15. **I2S_AP RX Channel Select Register(Default Value: 0x0000_0001)**

Offset: 0x0038			**Register Name: DA_RXCHSEL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x1	RX_CHSEL RX Channel Select 000: 1-ch 001: 2-ch 010: 3-ch 011: 4-ch Others: Reserved

11.3.5.16. **I2S_AP RX Channel Mapping Register(Default Value: 0x0000_3210)**

Offset: 0x003C			Register Name: DA_RXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x3	RX_CH3_MAP RX Channel3 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
11	/	/	/
10:8	R/W	0x2	RX_CH2_MAP RX Channel2 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
7	/	/	/
6:4	R/W	0x1	RX_CH1_MAP RX Channel1 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
3	/	/	/
2:0	R/W	0x0	RX_CH0_MAP RX Channel0 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved

11.3.5.17. **System Clock Control Register(Default Value: 0x0000_0000)**

Offset: 0x020C			Register Name: SYSCLK_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	AIF1CLK_ENA AIF1CLK Enable 0: Disable

			1: Enable
10	R/W	0x0	Reserved
9:8	R/W	0x0	AIF1CLK_SRC AIF1CLK Source Select 00: MCLK1 01: Reserved 1X: PLL2_1x
7	R/W	0x0	AIF2CLK_ENA AIF2CLK Enable 0: Disable 1: Enable
6	R/W	0x0	Reserved
5:4	R/W	0x0	AIF2CLK_SRC AIF2CLK Source Select 00: MCLK1 01: Reserved 1X: PLL2_1x
3	R/W	0x0	SYSCLK_ENA SYSCLK Enable 0: Disable 1: Enable
2:1	R/W	0x0	Reserved
0	R/W	0x0	SYSCLK_SRC System Clock Source Select 0: AIF1CLK 1: AIF2CLK

11.3.5.18. **Module Clock Control Register(Default Value: 0x0000_0000)**

Offset: 0x0210			**Register Name: MOD_CLK_ENA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	Module Clock Enable Control 0: Clock disable 1: Clock enable BIT15-AIF1 BIT14-AIF2 BIT13-AIF3 BIT12-Reserved BIT11-Reserved BIT10-Reserved BIT9-Reserved BIT8-Reserved BIT7- Reserved BIT6-HPF & DRC0

			BIT5-HPF & DRC1 BIT4-Reserved BIT3-ADC Digital BIT2-DAC Digital BIT1-Reserved BIT0-Reserved

11.3.5.19. **Module Reset Control Register(Default Value: 0x0000_0000)**

Offset: 0x0214			**Register Name: MOD_RST_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	Module Reset Control 0: Reset asserted 1: Reset de-asserted BIT15-AIF1 BIT14-AIF2 BIT13-AIF3 BIT12-Reserved BIT11-Reserved BIT10-Reserved BIT9-Reserved BIT8-Reserved BIT7- Reserved BIT6-HPF & DRC0 BIT5-HPF & DRC1 BIT4-Reserved BIT3-ADC Digital BIT2-DAC Digital BIT1-Reserved BIT0-Reserved

11.3.5.20. **System Sample Rate Configuration Register(Default Value: 0x0000_0000)**

Offset: 0x0218			**Register Name: SYS_SR_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	ADDA_FS_AIF1 ADDA sample rate synchronized with AIF1 clock zone 0000: 8 kHz 0001: 11.025 kHz 0010: 12 kHz 0011: 16 kHz 0100: 22.05 kHz

			0101: 24 kHz 0110: 32 kHz 0111: 44.1 kHz 1000: 48 kHz 1001: 96 kHz 1010: 192 kHz Other: Reserved
11:8	R/W	0x0	ADDA_FS_AIF2 ADDA sample rate synchronized with AIF2 clock zone 0000: 8 kHz 0001: 11.025 kHz 0010: 12 kHz 0011: 16 kHz 0100: 22.05 kHz 0101: 24 kHz 0110: 32 kHz 0111: 44.1 kHz 1000: 48 kHz 1001: 96 kHz 1010: 192 kHz Other: Reserved
7:0	/	/	/

11.3.5.21. **System DVC Mode Select Register(Default Value: 0x0000_0000)**

Offset: 0x0220			**Register Name: SYS_DVC_CLK**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	AIFDVC_FS_SEL 0 : DVC output to AIF sync 1 : normal

11.3.5.22. **AIF1 BCLK/LRCK Control Register(Default Value: 0x0000_0000)**

Offset: 0x0240			**Register Name: AIF1CLK_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	AIF1_MSTR_MOD AIF1 audio interface mode select 0: Master mode 1: Slave mode
14	R/W	0x0	AIF1_BCLK_INV AIF1 BCLK polarity 0: Normal

			1: Inverted
13	R/W	0x0	AIF1_LRCK_INV AIF1 LRCK polarity 0: Normal 1: Inverted
12:9	R/W	0x0	AIF1_BCLK_DIV Select the AIF1CLK/BCLK1 ratio 0000: AIF1CLK/1 0001: AIF1CLK/2 0010: AIF1CLK/4 0011: AIF1CLK/6 0100: AIF1CLK/8 0101: AIF1CLK/12 0110: AIF1CLK/16 0111: AIF1CLK/24 1000: AIF1CLK/32 1001: AIF1CLK/48 1010: AIF1CLK/64 1011: AIF1CLK/96 1100: AIF1CLK/128 1101: AIF1CLK/192 1110: Reserved 1111: Reserved
8:6	R/W	0x0	AIF1_LRCK_DIV Select the BCLK1/LRCK ratio 000: 16 001: 32 010: 64 011: 128 100: 256 1xx: Reserved
5:4	R/W	0x0	AIF1_WORD_SIZ AIF1 digital interface word size 00: 8-bit 01: 16-bit 10: 20-bit 11: 24-bit
3:2	R/W	0x0	AIF1_DATA_FMT AIF1 digital interface data format 00: I2S mode 01: Left mode 10: Right mode 11: DSP mode
1	R/W	0x0	DSP_MONO_PCM DSP Mono mode select 0: Stereo mode select

			1: Mono mode select
0	R/W	0x0	AIF1_TDMM_ENA AIF1 TDM mode enable 0: Disable 1: Enable

11.3.5.23. **AIF1 ADCDAT Control Register(Default Value: 0x0000_0000)**

Offset: 0x0244			**Register Name: AIF1_ADCDAT_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	AIF1_ADC0L_ENA AIF1 ADC timeslot 0 left channel enable 0: Disable 1: Enable
14	R/W	0x0	AIF1_ADC0R_ENA AIF1 ADC timeslot 0 right channel enable 0: Disable 1: Enable
13	R/W	0x0	AIF1_ADC1L_ENA AIF1 ADC timeslot 1 left channel enable 0: Disable 1: Enable
12	R/W	0x0	AIF1_ADC1R_ENA AIF1 ADC timeslot 1 right channel enable 0: Disable 1: Enable
11:10	R/W	0x0	AIF1_ADC0L_SRC AIF1 ADC timeslot 0 left channel data source select 00: AIF1 ADC0L 01: AIF1 ADC0R 10: (AIF1 ADC0L+AIF1 ADC0R) 11: (AIF1 ADC0L+AIF1 ADC0R)/2
9:8	R/W	0x0	AIF1_ADC0R_SRC AIF1 ADC timeslot 0 right channel data source select 00: AIF1 ADC0R 01: AIF1 ADC0L 10: (AIF1 ADC0L+AIF1 ADC0R) 11: (AIF1 ADC0L+AIF1 ADC0R)/2
7:6	R/W	0x0	AIF1_ADC1L_SRC AIF1 ADC timeslot 1 left channel data source select 00: AIF1 ADC1L 01: AIF1 ADC1R 10: (AIF1 ADC1L+AIF1 ADC1R) 11: (AIF1 ADC1L+AIF1 ADC1R)/2

5:4	R/W	0x0	AIF1_ADC1R_SRC AIF1 ADC timeslot 1 right channel data source select 00: AIF1 ADC1R 01: AIF1 ADC1L 10: (AIF1 ADC1L+AIF1 ADC1R) 11: (AIF1 ADC1L+AIF1 ADC1R)/2
3	R/W	0x0	AIF1_ADCP_ENA AIF1 ADC companding enable(8-bit mode only) 0: Disable 1: Enable
2	R/W	0x0	AIF1_ADCUL_ENA AIF1 ADC companding mode select 0: A-law 1: u-law
1:0	R/W	0x0	AIF1_SLOT_SIZ Select the slot size(only in TDM mode) 00: 8 01: 16 10: 32 11: Reserved

11.3.5.24. **AIF1 DACDAT Control Register(Default Value: 0x0000_0000)**

Offset: 0x0248			**Register Name: AIF1_DACDAT_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	AIF1_DAC0L_ENA AIF1 DAC timeslot 0 left channel enable 0: Disable 1: Enable
14	R/W	0x0	AIF1_DAC0R_ENA AIF1 DAC timeslot 0 right channel enable 0: Disable 1: Enable
13	R/W	0x0	AIF1_DAC1L_ENA AIF1 DAC timeslot 1 left channel enable 0: Disable 1: Enable
12	R/W	0x0	AIF1_DAC1R_ENA AIF1 DAC timeslot 1 right channel enable 0: Disable 1: Enable
11:10	R/W	0x0	AIF1_DAC0L_SRC AIF1 DAC timeslot 0 left channel data source select 00: AIF1 DAC0L

			01: AIF1 DA0R 10: (AIF1 DAC0L+AIF1 DAC0R) 11: (AIF1 DAC0L+AIF1 DAC0R)/2
9:8	R/W	0x0	AIF1_DAC0R_SRC AIF1 DAC timeslot 0 right channel data source select 00: AIF1 DAC0R 01: AIF1 DAC0L 10: (AIF1 DAC0L+AIF1 DAC0R) 11: (AIF1 DAC0L+AIF1 DAC0R)/2
7:6	R/W	0x0	AIF1_DAC1L_SRC AIF1 DAC timeslot 1 left channel data source select 00: AIF1 DAC1L 01: AIF1 DAC1R 10: (AIF1 DAC1L+AIF1 DAC1R) 11: (AIF1 DAC1L+AIF1 DAC1R)/2
5:4	R/W	0x0	AIF1_DAC1R_SRC AIF1 DAC timeslot 1 right channel data source select 00: AIF1 DAC1R 01: AIF1 DAC1L 10: (AIF1 DAC1L+AIF1 DAC1R) 11: (AIF1 DAC1L+AIF1 DAC1R)/2
3	R/W	0x0	AIF1_DACP_ENA AIF1 DAC companding enable(8-bit mode only) 00: Disable 01: Enable
2	R/W	0x0	AIF1_DACUL_ENA AIF1 DAC companding mode select 0: A-law 1: u-law
1	R/W	0x0	Reserved
0	R/W	0x0	AIF1_LOOP_ENA AIF1 loopback enable 0: No loopback 1: Loopback(ADCDAT1 data output to DACDAT1 data input)

11.3.5.25. **AIF1 Digital Mixer Source Select Register(Default Value: 0x0000_0000)**

Offset: 0x024C			**Register Name: AIF1_MXR_SRC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	AIF1_ADC0L_MXL_SRC AIF1 ADC timeslot 0 left channel mixer source select 0: Disable 1: Enable Bit15: AIF1 DAC0L data

			Bit14: AIF2 DACL data Bit13: ADCL data Bit12: AIF2 DACR data
11:8	R/W	0x0	AIF1_ADC0R_MXR_SRC AIF1 ADC timeslot 0 right channel mixer source select 0: Disable 1: Enable Bit11: AIF1 DAC0R data Bit10: AIF2 DACR data Bit9: ADCR data Bit8: AIF2 DACL data
7:6	R/W	0x0	AIF1_ADC1L_MXR_SRC AIF1 ADC timeslot 1 left channel mixer source select 0: Disable 1: Enable Bit7: AIF2 DACL data Bit6: ADCL data
5:4	R/W	0x0	Reserved
3:2	R/W	0x0	AIF1_ADC1R_MXR_SRC AIF1 ADC timeslot 1 right channel mixer source select 0: Disable 1: Enable Bit3: AIF2 DACR data Bit2: ADCR data
1:0	R/W	0x0	Reserved

11.3.5.26. **AIF1 Volume Control 1 Register(Default Value: 0x0000_A0A0)**

Offset: 0x0250			**Register Name: AIF1_VOL_CTRL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0xA0	AIF1_ADC0L_VOL AIF1 ADC timeslot 0 left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB
7:0	R/W	0xA0	AIF1_ADC0R_VOL AIF1 ADC timeslot 0 right channel volume (-119.25dB To 71.25dB, 0.75dB/Step)

			0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1:0.75dB …… 0xFF: 71.25dB

11.3.5.27. **AIF1 Volume Control 2 Register(Default Value: 0x0000_A0A0)**

Offset: 0x0254			**Register Name: AIF1_VOL_CTRL2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0xA0	AIF1_ADC1L_VOL AIF1 ADC timeslot 1 left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB
7:0	R/W	0xA0	AIF1_ADC1R_VOL AIF1 ADC timeslot 1 right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB

11.3.5.28. **AIF1 Volume Control 3 Register(Default Value: 0x0000_A0A0)**

Offset: 0x0258			**Register Name: AIF1_VOL_CTRL3**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0xA0	AIF1_DAC0L_VOL AIF1 DAC timeslot 0 left channel volume

			(-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB
7:0	R/W	0xA0	AIF1_DAC0R_VOL AIF1 DAC timeslot 0 right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB

11.3.5.29. **AIF1 Volume Control 4 Register(Default Value: 0x0000_A0A0)**

Offset: 0x025C			**Register Name: AIF1_VOL_CTRL4**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0xA0	AIF1_DAC1L_VOL AIF1 DAC timeslot 1 left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB
7:0	R/W	0xA0	AIF1_DAC1R_VOL AIF1 DAC timeslot 1 right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB

			0xA1: 0.75dB …… 0xFF: 71.25dB

11.3.5.30. **AIF1 Digital Mixer Gain Control Register(Default Value: 0x0000_0000)**

Offset: 0x0260			Register Name: AIF1_MXR_GAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	AIF1_ADC0L_MXR_GAIN AIF1 ADC timeslot 0 left channel mixer gain control 0: 0dB 1: -6dB Bit15: AIF1 DAC0L data Bit14: AIF2 DACL data Bit13: ADCL data Bit12: AIF2 DACR data
11:8	R/W	0x0	AIF1_ADC0R_MXR_GAIN AIF1 ADC timeslot 0 right channel mixer gain control 0: 0dB 1: -6dB Bit11: AIF1 DAC0R data Bit10: AIF2 DACR data Bit9: ADCR data Bit8: AIF2 DACL data
7:6	R/W	0x0	AIF1_ADC1L_MXR_GAIN AIF1 ADC timeslot 1 left channel mixer gain control 0: 0dB 1: -6dB Bit7: AIF2 DACL data Bit6: ADCL data
5:4	R/W	0x0	Reserved
3:2	R/W	0x0	AIF1_ADC1R_MXR_GAIN AIF1 ADC timeslot 1 right channel mixer gain control 0: 0dB 1: -6dB Bit3: AIF2 DACR data Bit2: ADCR data
1:0	R/W	0x0	Reserved

11.3.5.31. **AIF1 Receiver Data Discarding Control Register(Default Value: 0x0000_0000)**

Offset: 0x0264			Register Name: AIF1_RXD_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:8	R/W	0x0	After data receiving progress begins, the first N-data will be discarded. N defined as follows: 0x00: None discarded 0x01: 1-data discarded ... 0xFF: 255-data discarded
7:0	R/W	0x0	Reserved

11.3.5.32. **AIF2 BCLK/LRCK Control Register(Default Value: 0x0000_0000)**

Offset: 0x0280			**Register Name: AIF2_CLK_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	AIF2_MSTR_MOD AIF2 audio interface mode select 0: Master mode 1: Slave mode
14	R/W	0x0	AIF2_BCLK_INV AIF2 BCLK polarity 0: Normal 1: Inverted
13	R/W	0x0	AIF2_LRCK_INV AIF2 LRCK polarity 0: Normal 1: Inverted
12:9	R/W	0x0	AIF2_BCLK_DIV Select the AIF2CLK/BCLK2 ratio 0000: AIF2CLK/1 0001: AIF2CLK/2 0010: AIF2CLK/4 0011: AIF2CLK/6 0100: AIF2CLK/8 0101: AIF2CLK/12 0110: AIF2CLK/16 0111: AIF2CLK/24 1000: AIF2CLK/32 1001: AIF2CLK/48 1010: AIF2CLK/64 1011: AIF2CLK/96 1100: AIF2CLK/128 1101: AIF2CLK/192 1110: Reserved 1111: Reserved
8:6	R/W	0x0	AIF2_LRCK_DIV

			Select the BCLK2/LRCK2 ratio 000: 16 001: 32 010: 64 011: 128 100: 256 1xx: Reserved
5:4	R/W	0x0	AIF2_WORD_SIZ AIF2 digital interface world length 00: 8-bit 01: 16-bit 10: 20-bit 11: 24-bit
3:2	R/W	0x0	AIF2_DATA_FMT AIF digital interface data format 00: I2S mode 01: Left mode 10: Right mode 11: DSP mode
1	R/W	0x0	AIF2_MONO_PCM AIF2 Mono PCM mode select 0: Stereo mode select 1: Mono mode select
0	R/W	0x0	Reserved

11.3.5.33. **AIF2 ADCDAT Control Register(Default Value: 0x0000_0000)**

Offset: 0x0284			**Register Name: AIF2_ADCDAT_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	AIF2_ADCL_EN AIF2 ADC left channel enable 0: Disable 1: Enable
14	R/W	0x0	AIF2_ADCR_EN AIF2 ADC right channel enable 0: Disable 1: Enable
13:12	/	/	/
11:10	R/W	0x0	AIF2_ADCL_SRC AIF2 ADC left channel data source select 00: AIF2 ADCL 01: AIF2 ADCR 10: (AIF2 ADCL+AIF2 ADCR) 11: (AIF2 ADCL+AIF2 ADCR)/2

9:8	R/W	0x0	AIF2_ADCR_SRC AIF2 ADC right channel data source select 00: AIF2 ADCR 01: AIF2 ADCL 10: (AIF2 ADCL+AIF2 ADCR) 11: (AIF2 ADCL+AIF2 ADCR)/2
7:4	/	/	/
3	R/W	0x0	AIF2_ADCP_ENA AIF2 ADC companding enable(8-bit mode only) 00: Disable 01: Enable
2	R/W	0x0	AIF2_ADCUL_ENA AIF2 ADC companding mode select 0: A-law 1: u-law
1:0	/	/	/

11.3.5.34. **AIF2 DACDAT Control Register(Default Value: 0x0000_0000)**

Offset: 0x0288			**Register Name: AIF2_DACDAT_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	AIF2_DACL_ENA AIF2 DAC left channel enable 0: Disable 1: Enable
14	R/W	0x0	AIF2_DACR_ENA AIF2 DAC right channel enable 0: Disable 1: Enable
13:12	R/W	0x0	Reserved
11:10	R/W	0x0	AIF2_DACL_SRC AIF2 DAC left channel data source select 00: AIF2 DACL 01: AIF2 DACR 10: (AIF2 DACL+AIF2 DACR) 11: (AIF2 DACL+AIF2 DACR)/2
9:8	R/W	0x0	AIF2_DACR_SRC AIF2 DAC right channel data source select 00: AIF2 DACR 01: AIF2 DACL 10: (AIF2 DACL+AIF2 DACR) 11: (AIF2 DACL+AIF2 DACR)/2
7:4	R/W	0x0	Reserved
3	R/W	0x0	AIF2_DACP_ENA

			AIF2 DAC companding enable(8-bit mode only) 00: Disable 01: Enable
2	R/W	0x0	AIF2_DACUL_ENA AIF2 DAC companding mode select 0: A-law 1: u-law
1	/	/	/
0	R/W	0x0	AIF2_LOOP_EN AIF2 loopback enable 0: No loopback 1: Loopback(ADCDAT2 data output to DACDAT2 data input)

11.3.5.35. **AIF2 Digital Mixer Source Select Register(Default Value: 0x0000_0000)**

Offset: 0x028C			**Register Name: AIF2_MXR_SRC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	AIF2_ADCL_MXR_SRC AIF2 ADC left channel mixer source select 0: Disable 1:Enable Bit15: AIF1 DAC0L data Bit14: AIF1 DAC1L data Bit13: AIF2 DACR data Bit12: ADCL data
11:8	R/W	0x0	AIF2_ADCR_MXR_SRC AIF2 ADC right channel mixer source select 0: Disable 1:Enable Bit11: AIF1 DA0R data Bit10: AIF1 DA1R data Bit9: AIF2 DACL data Bit8: ADCR data
7:0	R/W	0x0	Reserved

11.3.5.36. **AIF2 Volume Control 1 Register(Default Value: 0x0000_A0A0)**

Offset: 0x0290			**Register Name: AIF2_VOL_CTRL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0xA0	AIF2_ADCL_VOL AIF2 ADC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step)

			0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB
7:0	R/W	0xA0	AIF2_ADCR_VOL AIF2 ADC right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB

11.3.5.37. AIF2 Volume Control 2 Register(Default Value: 0x0000_A0A0)

Offset: 0x0298			Register Name: AIF2_VOL_CTRL2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0xA0	AIF2_DACL_VOL AIF2 DAC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB
7:0	R/W	0xA0	AIF2_DACR_VOL AIF2 DAC right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB

			…… 0xFF: 71.25dB

11.3.5.38. **AIF2 Digital Mixer Gain Control Register(Default Value: 0x0000_0000)**

Offset: 0x02A0			Register Name: AIF2_MXR_GAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	AIF2_ADCL_MXR_GAIN AIF2 ADC left channel mixer gain control 0: 0dB 1: -6dB Bit15: AIF1 DAC0L data Bit14: AIF1 DAC1L data Bit13: AIF2 DACR data Bit12: ADCL data
11:8	R/W	0x0	AIF2_ADCR_MXR_GAIN AIF2 ADC right channel mixer gain control 0: 0dB 1: -6dB Bit11: AIF1 DAC0R data Bit10: AIF1 DAC1R data Bit9: AIF2 DACL data Bit8: ADCR data
7:0	R/W	0x0	Reserved

11.3.5.39. **AIF2 Receiver Data Discarding Control Register(Default Value: 0x0000_0000)**

Offset: 0x02A4			Register Name: AIF2_RXD_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	After data receiving progress begins, the first N-data will be discarded. N defined as follows: 0x00: None discarded 0x01: 1-data discarded ... 0xFF: 255-data discarded
7:0	R/W	0x0	Reserved

11.3.5.40. **AIF3 BCLK/LRCK Control Register(Default Value: 0x0000_0000)**

Offset: 0x02C0			Register Name: AIF3_CLK_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**

31:15	/	/	/
14	R/W	0x0	AIF3_BCLK_INV AIF3 BCLK polarity 0: Normal 1: Inverted
13	R/W	0x0	AIF3_LRCK_INV AIF3 LRCK polarity 0: Normal 1: Inverted
12:6	R/W	0x0	Reserved
5:4	R/W	0x0	AIF3_WORD_SIZ AIF3 digital interface world length 00: 8-bit 01: 16-bit 10: 20-bit 11: 24-bit
3:2	R/W	0x0	Reserved
1:0	R/W	0x0	AIF3_CLOCK_SRC AIF3 BCLK/LRCK source control 00: BCLK/LRCK Come from AIF1 01: BCLK/LRCK Come from AIF2 10: BCLK/LRCK is generated by AIF3, and the source clock is AIF1CLK 11: Reserved

11.3.5.41. **AIF3 ADCDAT Control Register(Default Value: 0x0000_0000)**

Offset: 0x02C4			**Register Name: AIF3_ADCDAT_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	AIF3_ADCP_ENA AIF3 ADC companding enable 00: Disable 01: Enable
2	R/W	0x0	AIF3_ADUL_ENA AIF3 ADC companding mode select 0: A-law 1: u-law
1:0	R/W	0x0	Reserved

11.3.5.42. **AIF3 DACDAT Control Register(Default Value: 0x0000_0000)**

Offset: 0x02C8			**Register Name: AIF3_DACDAT_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

3	R/W	0x0	AIF3_DACP_ENA AIF3 DAC companding enable(8-bit mode only) 00: Disable 01: Enable
2	R/W	0x0	AIF3_DAUL_ENA AIF3 DAC companding mode select 00: u-law 01: A-law
1	R/W	0x0	Reserved
0	R/W	0x0	AIF3_LOOP_ENA AIF3 loopback enable 0: No loopback 1: Loopback(ADCDAT3 data output to DACDAT3 data input)

11.3.5.43. **AIF Signal Path Control Register(Default Value: 0x0000_0000)**

Offset: 0x02CC			**Register Name: AIF_SGP_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x0	AIF3_ADC_SRC AIF3 PCM output source select 00: None 01: AIF2 ADC left channel 10: AIF2 ADC right channel 11: Reserved
9:8	R/W	0x0	AIF2_DAC_SRC AIF2 DAC input source select 00: Left and right inputs from AIF2 01: Left input from AIF3; Right input from AIF2 10: Left input from AIF2; Right input from AIF3 11: Reserved
7	R/W	0x0	AIF3_PINS_TRI AIF3 pins tri-state control 0: AIF3 pins operate normally 1: Tri-state all AIF3 interface pins
6:4	R/W	0x0	AIF3_ADCDAT_SRC AIF3 ADCDAT source select 0xx: AIF3 Mono PCM output 100: AIF1 ADCDAT1 101: AIF1 DACDAT1 110: AIF2 ADCDAT2 111: AIF2 DACDAT2
3	R/W	0x0	AIF2_ADCDAT_SRC AIF2 ADCDAT2 source select 0: AIF2 ADCDAT2

			1: AIF3 DACDAT3
2	R/W	0x0	AIF2_DACDAT_SRC AIF2 DACDAT2 source select 0: AIF2 DACDAT2 1: AIF3 DACDAT3
1	R/W	0x0	AIF1_ADCDAT_SRC AIF1 ADCDAT1 source select 0: AIF1 ADCDAT1 1: AIF3 DACDAT3
0	R/W	0x0	AIF1_DACDAT_SRC AIF1 DACDAT1 source select 0: AIF1 DACDAT1 1: AIF3 DACDAT3

11.3.5.44. **AIF3 Receiver Data Discarding Control Register(Default Value: 0x0000_0000)**

Offset: 0x02E4			**Register Name: AIF3_RXD_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	After data receiving progress begins, the first N-data will be discarded. N defined as follows: 0x00: None discarded 0x01: 1-data discarded ... 0xFF: 255-data discarded
7:0	R/W	0x0	Reserved

11.3.5.45. **ADC Digital Control Register(Default Value: 0x0000_0000)**

Offset: 0x0300			**Register Name: ADC_DIG_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	ENAD ADC digital part enable 0: Disable 1: Enable
14	/	/	/
13	R/W	0x0	ADFIR32 Enable 32-tap FIR filter 0: 64-tap 1: 32-tap
12:5	R/W	0x0	Reserved
4	/	/	/
3:2	R/W	0x0	ADOUT_DTS

			ADC delay time for transmitting data after ENAD 00:5ms 01:10ms 10:20ms 11:30ms
1	R/W	0x0	ADOUT_DLY ADC delay function enable for transmitting data after ENAD 0: Disable 1: Enable
0	/	/	/

11.3.5.46. **ADC Volume Control Register(Default Value: 0x0000_A0A0)**

Offset: 0x0304			**Register Name: ADC_VOL_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0xA0	ADC_VOL_L ADC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB
7:0	R/W	0xA0	ADC_VOL_R ADC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB

11.3.5.47. **DAC Digital Control Register(Default Value: 0x0000_0000)**

Offset: 0x0320			**Register Name: DAC_DIG_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

15	R/W	0x0	ENDA DAC digital part enable 0: Disable 1: Enable
14	R/W	0x0	ENHPF HPF function enable 0: Enable 1: Disable
13	R/W	0x0	DAFIR32 Enable 32-tap FIR filter 0: 64-tap 1: 32-tap
12	R/W	0x0	Reserved
11:8	R/W	0x0	MODQU Internal DAC quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
7:0	R/W	0x0	Reserved

11.3.5.48. **DAC Volume Control Register(Default Value: 0x0000_A0A0)**

Offset: 0x0324			**Register Name: DAC_VOL_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0xA0	DAC_VOL_L DAC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB
7:0	R/W	0xA0	DAC_VOL_R DAC right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB ……

			0xFF: 71.25dB

11.3.5.49. **DAC Debug Control Register(Default Value: 0x0000_0000)**

Offset: 0x0328			Register Name: DAC_DBG_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	DASW DAC output channel swap enable 0:Disable 1:Enable
14	R/W	0x0	ENDWA_N DWA function disable 0: Enable 1: Disable
13	R/W	0x0	DAC_MOD_DBG DAC modulator debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode
12:8	R/W	0x0	Reserved
7:6	R/W	0x0	DAC_PTN_SEL DAC pattern select 00: Normal(Audio sample from DAC mixer) 01: -6 dB sin wave 10: -60 dB sin wave 11: zero data
5:0	R/W	0x0	DVC Digital volume control, ATT=DVC[5:0]*(-1.16dB) 64 steps, -1.16dB/step

11.3.5.50. **DAC Digital Mixer Source Select Register(Default Value: 0x0000_0000)**

Offset: 0x0330			Register Name: DAC_MXR_SRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	DACL_MXR_SRC DAC left channel mixer source select 0: Disable 1:Enable Bit15: AIF1 DAC0L Bit14: AIF1 DAC1L Bit13: AIF2 DACL Bit12: ADCL
11:8	R/W	0x0	DACR_MXR_SRC

			DAC right channel mixer source select 0: Disable 1:Enable Bit11: AIF1 DAC0R Bit10: AIF1 DAC1R Bit9: AIF2 DACR Bit8: ADCR
7:0	R/W	0x0	Reserved

11.3.5.51. **DAC Digital Mixer Gain Control Register(Default Value: 0x0000_0000)**

Offset: 0x0334			**Register Name: DAC_MXR_GAIN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	DACL_MXR_GAIN DAC left channel mixer gain control 0: 0dB 1: -6dB Bit15: AIF1 DAC0L Bit14: AIF1 DAC1L Bit13: AIF2 DACL Bit12: ADCL
11:8	R/W	0x0	DACR_MXR_GAIN DAC right channel mixer gain control 0: 0dB 1: -6dB Bit11: AIF1 DAC0R Bit10: AIF1 DAC1R Bit9: AIF2 DACR Bit8: ADCR
7:0	R/W	0x0	Reserved

11.3.5.52. **DAC DAP Control Register(Default Value: 0x0000_0000)**

Offset: 0x0480			**Register Name: AC_DAC_DAPCTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	DRC1 enable control 0: Disable 1: Enable
5	R/W	0x0	DRC1 left channel HPF enable control 0: Disable 1: Enable
4	R/W	0x0	DRC1 right channel HPF enable control

			0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DRC0 enable control 0: Disable 1: Enable
1	R/W	0x0	DRC0 left channel HPF enable control 0: Disable 1: Enable
0	R/W	0x0	DRC0 right channel HPF enable control 0: Disable 1: Enable

11.3.5.53. **DRC Enable Register(Default Value: 0x0000_0000)**

Offset: 0x04D4			**Register Name: DRC_ENA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	AIF1_DAC0_DRC0_ENA AIF1 DAC timeslot 0 DRC0 enable 0: Disable 1: Enable
14	R/W	0x0	AIF1_DAC1_DRC0_ENA AIF1 DAC timeslot 1 DRC0 enable 0: Disable 1: Enable
13	R/W	0x0	AIF2_DAC_DRC0_ENA AIF2 DAC DRC0 enable 0: Disable 1: Enable
12	R/W	0x0	DAC_DRC0_ENA DAC DRC0 enable 0: Disable 1: Enable
11:8	/	/	/
7	R/W	0x0	AIF1_ADC0_DRC1_ENA AIF1 ADC timeslot 0 DRC1 enable 0 : Disable 1 : Enable
6	R/W	0x0	AIF1_ADC1_DRC1_ENA AIF1 ADC timeslot 1 DRC1 enable 0 : Disable 1 : Enable
5	R/W	0x0	AIF2_ADC_DRC1_ENA AIF2 ADC DRC1 enable

			0 : Disable 1 : Enable
4	R/W	0x0	ADC_DRC1_ENA ADC_DRC1 enable 0 : Disable 1 : Enable
3:0	/	/	/

11.3.5.54. **DRC0 High HPF Coef Register(Default Value: 0x0000_00FF)**

Offset: 0x0600			**Register Name: AC_DRC0_HHPFC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0FF	HPF coefficient setting and the data is 3.24 format.

11.3.5.55. **DRC0 Low HPF Coef Register(Default Value: 0x0000_FAC1)**

Offset: 0x0604			**Register Name: AC_DRC0_LHPFC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

11.3.5.56. **DRC0 Control Register(Default Value: 0x0000_0080)**

Offset: 0x0608			**Register Name: AC_DRC0_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when DRC delay function is enable and the DRC function disable. After disable DRC function and this bit go to 0, the user should write the DRC delay function bit to 0. 0 : Not complete 1 : Complete
14:10	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.

7	R/W	0x1	The delay buffer uses or not when the DRC disables and the DRC buffer data outputs completely 0 : Not use the buffer 1 : Use the buffer
6	R/W	0x0	DRC gain max limit enable 0 : Disable 1 : Enable
5	R/W	0x0	DRC gain min limit enable. when this function is enabled, it will overwrite the noise detect function. 0 : Disable 1 : Enable
4	R/W	0x0	Control the DRC to detect noise when ET enable 0 : Disable 1 : Enable
3	R/W	0x0	Signal function select 0 : RMS filter 1 : Peak filter When signal function selects Peak filter, the RMS parameter is unused.(AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function selects RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0 : Disable 1 : Enable When the Delay function enable is disabled, the Signal delay time is unused.
1	R/W	0x0	DRC LT enable 0 : Disable 1 : Enable When the DRC LT is disabled the LT, KI and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0 : Disable 1 : Enable When the DRC ET is disabled the ET, Ke and OPE parameter is unused.

11.3.5.57. DRC0 Left Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)

Offset: 0x060C			Register Name: AC_DRC0_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x00B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

11.3.5.58. **DRC0 Left Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)**

Offset: 0x0610			Register Name: AC_DRC0_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

11.3.5.59. **DRC0 Right Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)**

Offset: 0x0614			Register Name: AC_DRC0_RPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x00B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

11.3.5.60. **DRC0 Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)**

Offset: 0x0618			Register Name: AC_DRC0_RPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

11.3.5.61. **DRC0 Left Peak Filter High Release Time Coef Register(Default Value: 0x0000_00FF)**

Offset: 0x061C			Register Name: AC_DRC0_LPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

11.3.5.62. **DRC0 Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)**

Offset: 0x0620			Register Name: AC_DRC0_LPFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

11.3.5.63. **DRC0 Right Peak Filter High Release Time Coef Register(Default Value: 0x0000_00FF)**

Offset: 0x0624			Register Name: AC_DRC0_RPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0FF	The left peak filter attack time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

11.3.5.64. **DRC0 Right Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)**

Offset: 0x0628			Register Name: AC_DRC0_RPFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

11.3.5.65. **DRC0 Left RMS Filter High Coef Register(Default Value: 0x0000_0001)**

Offset: 0x062C			Register Name: AC_DRC0_LRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x001	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

11.3.5.66. **DRC0 Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)**

Offset: 0x0630			Register Name: AC_DRC0_LRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

11.3.5.67. **DRC0 Right RMS Filter High Coef Register(Default Value: 0x0000_0001)**

Offset: 0x0634			Register Name: AC_DRC0_RRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x001	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

11.3.5.68. **DRC0 Right RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)**

Offset: 0x0638			Register Name: AC_DRC0_RRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

11.3.5.69. **DRC0 Compressor Threshold High Setting Register(Default Value: 0x0000_06A4)**

Offset: 0x063C			Register Name: AC_DRC0_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

11.3.5.70. **DRC0 Compressor Threshold Low Setting Register(Default Value: 0x0000_D3C0)**

Offset: 0x0640			Register Name: AC_DRC0_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

11.3.5.71. **DRC0 Compressor Slope High Setting Register(Default Value: 0x0000_0080)**

Offset: 0x0644			Register Name: AC_DRC0_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0080	The slope of the compressor which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 6.24. (2 : 1)

11.3.5.72. **DRC0 Compressor Slope Low Setting Register(Default Value: 0x0000_0000)**

Offset: 0x0648			Register Name: AC_DRC0_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 6.24. (2 : 1)

11.3.5.73. **DRC0 Compressor High Output at Compressor Threshold Register(Default Value: 0x0000_F95B)**

Offset: 0x064C			Register Name: AC_DRC0_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor which is determined by the equation - OPC/6.0206 The format is 8.24.(-40dB)

11.3.5.74. **DRC0 Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)**

Offset: 0x0650			Register Name: AC_DRC0_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor which is determined by the equation OPC/6.0206 The format is 8.24. (-40dB)

11.3.5.75. **DRC0 Limiter Threshold High Setting Register(Default Value: 0x0000_01A9)**

Offset: 0x0654			Register Name: AC_DRC0_HLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which is set by the equation that LTin = - LT/6.0206, The format is 8.24. (-10dB)

11.3.5.76. **DRC0 Limiter Threshold Low Setting Register(Default Value: 0x0000_34F0)**

Offset: 0x0658			Register Name: AC_DRC0_LLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which is set by the equation that LTin = - LT/6.0206, The format is 8.24. (-10dB)

11.3.5.77. **DRC0 Limiter Slope High Setting Register(Default Value: 0x0000_0005)**

Offset: 0x065C			Register Name: AC_DRC0_HKI
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0005	The slope of the limiter which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 6.24. (50 :1)

11.3.5.78. **DRC0 Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)**

Offset: 0x0660			Register Name: AC_DRC0_LKI
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 6.24. (50 :1)

11.3.5.79. **DRC0 Limiter High Output at Limiter Threshold(Default Value: 0x0000_FBD8)**

Offset: 0x0664			Register Name: AC_DRC0_HOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter which is determined by equation OPT/6.0206. The format is 8.24 .(-25dB)

11.3.5.80. **DRC0 Limiter Low Output at Limiter Threshold(Default Value: 0x0000_FBA7)**

Offset: 0x0668			Register Name: AC_DRC0_LOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter which is determined by equation OPT/6.0206. The format is 8.24 .(-25dB)

11.3.5.81. **DRC0 Expander Threshold High Setting Register(Default Value: 0x0000_0BA0)**

Offset: 0x066C			Register Name: AC_DRC0_HET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

11.3.5.82. **DRC0 Expander Threshold Low Setting Register(Default Value: 0x0000_7291)**

Offset: 0x0670			Register Name: AC_DRC0_LET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

11.3.5.83. **DRC0 Expander Slope High Setting Register(Default Value: 0x0000_0500)**

Offset: 0x0674			Register Name: AC_DRC0_HKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0500	The slope of the expander which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 1/50. The format is 6.24. (1:5)

11.3.5.84. **DRC0 Expander Slope Low Setting Register(Default Value: 0x0000_0000)**

Offset: 0x0678			Register Name: AC_DRC0_LKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 1/50. The format is 6.24. (1:5)

11.3.5.85. **DRC0 Expander High Output at Expander Threshold(Default Value: 0x0000_F45F)**

Offset: 0x067C			Register Name: AC_DRC0_HOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander which is determined by equation OPE/6.0206. The format is 8.24. (-70dB)

11.3.5.86. **DRC0 Expander Low Output at Expander Threshold(Default Value: 0x0000_8D6E)**

Offset: 0x0680			Register Name: AC_DRC0_LOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander which is determined by equation OPE/6.0206. The format is 8.24 .(-70dB)

11.3.5.87. **DRC0 Linear Slope High Setting Register(Default Value: 0x0000_0100)**

Offset: 0x0684			Register Name: AC_DRC0_HKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0100	The slope of the linear which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer . The format is 6.24. (1:1)

11.3.5.88. **DRC0 Linear Slope Low Setting Register(Default Value: 0x0000_0000)**

Offset: 0x0688			Register Name: AC_DRC0_LKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer . The format is 6.24. (1:1)

11.3.5.89. **DRC0 Smooth Filter Gain High Attack Time Coef Register(Default Value:0x0000_0002)**

Offset: 0x068C			Register Name: AC_DRC0_SFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x002	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

11.3.5.90. **DRC0 Smooth Filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)**

Offset: 0x0690			Register Name: AC_DRC0_SFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

11.3.5.91. **DRC0 Smooth Filter Gain High Release Time Coef Register(Default Value:0x0000_0000)**

Offset: 0x0694			Register Name: AC_DRC0_SFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

11.3.5.92. **DRC0 Smooth Filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)**

Offset: 0x0698			Register Name: AC_DRC0_SFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

11.3.5.93. **DRC0 MAX Gain High Setting Register(Default Value: 0x0000_FE56)**

Offset: 0x069C			Register Name: AC_DRC0_MXGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB .(-10dB)

11.3.5.94. **DRC0 MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)**

Offset: 0x06A0			Register Name: AC_DRC0_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB .(-10dB)

11.3.5.95. **DRC0 MIN Gain High Setting Register(Default Value: 0x0000_F95B)**

Offset: 0x06A4			Register Name: AC_DRC0_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting is determined by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB .(-40dB)

11.3.5.96. **DRC0 MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)**

Offset: 0x06A8			Register Name: AC_DRC0_MNGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting is determined by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB .(-40dB)

11.3.5.97. **DRC0 Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)**

Offset: 0x06AC			Register Name: AC_DRC0_EPSHC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

11.3.5.98. **DRC0 Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)**

Offset: 0x06B0			Register Name: AC_DRC0_EPSLC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

11.3.5.99. **DRC0 HPF Gain High Coef Register(Default Value: 0x0000_0100)**

Offset: 0x06B8			Register Name: AC_DRC0_HPFHGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x100	The gain of the HPF coefficient setting. Its format is 3.24.(gain = 1)

11.3.5.100. **DRC0 HPF Gain Low Coef Register(Default Value: 0x0000_0000)**

Offset: 0x06BC			Register Name: AC_DRC0_HPFLGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The gain of the HPF coefficient setting .Its format is 3.24.(gain = 1)

11.3.5.101. **DRC1 High HPF Coef Register(Default Value: 0x0000_00FF)**

Offset: 0x0700			Register Name: AC_DRC1_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0FF	HPF coefficient setting.The data is 3.24 format.

11.3.5.102. **DRC1 Low HPF Coef Register(Default Value: 0x0000_FAC1)**

Offset: 0x0704			Register Name: AC_DRC1_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting .The data is 3.24 format.

11.3.5.103. **DRC1 Control Register(Default Value: 0x0000_0080)**

Offset: 0x0708			Register Name: AC_DRC1_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when DRC delay function is enabled and the DRC function is disabled. After disable DRC function and this bit goes to 0, the user should write the DRC delay function bit to 0. 0 : Not complete 1 : Complete
14:10	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the DRC is disabled and the DRC buffer data outputs completely. 0 : Not use the buffer 1 : Use the buffer
6	R/W	0x0	DRC gain max limit enable 0 : Disable 1 : Enable
5	R/W	0x0	DRC gain min limit enable. When this function is enabled, it will overwrite the noise detect function. 0 : Disable 1 : Enable
4	R/W	0x0	Control the DRC to detect noise when ET is enabled 0 : Disable 1 : Enable
3	R/W	0x0	Signal function select 0 : RMS filter 1 : Peak filter When Signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function selects RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable

			0 : Disable 1 : Enable When the Delay function enable is disabled, the Signal delay time is unused.
1	R/W	0x0	DRC LT enable 0 : Disable 1 : Enable When the DRC LT is disabled the LT, KI and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0 : Disable 1 : Enable When the DRC ET is disabled the ET, Ke and OPE parameter is unused.

11.3.5.104. **DRC1 Left Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)**

Offset: 0x070C			**Register Name: AC_DRC1_LPFHAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x00B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

11.3.5.105. **DRC1 Left Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)**

Offset: 0x0710			**Register Name: AC_DRC1_LPFLAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

11.3.5.106. **DRC1 Right Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)**

Offset: 0x0714			**Register Name: AC_DRC1_RPFHAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x00B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

11.3.5.107. **DRC1 Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)**

Offset: 0x0718			**Register Name: AC_DRC1_RPFLAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

11.3.5.108. **DRC1 Left Peak Filter High Release Time Coef Register(Default Value: 0x0000_00FF)**

Offset: 0x071C			**Register Name: AC_DRC1_LPFHRT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

11.3.5.109. **DRC1 Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)**

Offset: 0x0720			**Register Name: AC_DRC1_LPFLRT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

11.3.5.110. **DRC1 Right Peak filter High Release Time Coef Register(Default Value: 0x0000_00FF)**

Offset: 0x0724			**Register Name: AC_DRC1_RPFHRT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0FF	The left peak filter attack time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

11.3.5.111. **DRC1 Right Peak filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)**

Offset: 0x0728			**Register Name: AC_DRC1_RPFLRT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

11.3.5.112. **DRC1 Left RMS Filter High Coef Register(Default Value: 0x0000_0001)**

Offset: 0x072C			**Register Name: AC_DRC1_LRMSHAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x001	The left RMS filter average time parameter setting, which is determined by

			the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

11.3.5.113. **DRC1 Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)**

Offset: 0x0730			Register Name: AC_DRC1_LRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

11.3.5.114. **DRC1 Right RMS Filter High Coef Register(Default Value: 0x0000_0001)**

Offset: 0x0734			Register Name: AC_DRC1_RRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x001	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

11.3.5.115. **DRC1 Right RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)**

Offset: 0x0738			Register Name: AC_DRC1_RRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

11.3.5.116. **DRC1 Compressor Threshold High Setting Register(Default Value: 0x0000_06A4)**

Offset: 0x073C			Register Name: AC_DRC1_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

11.3.5.117. **DRC1 Compressor Threshold Low Setting Register(Default Value: 0x0000_D3C0)**

Offset: 0x0740			Register Name: AC_DRC1_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

11.3.5.118. **DRC1 Compressor Slope High Setting Register(Default Value: 0x0000_0080)**

Offset: 0x0744			Register Name: AC_DRC1_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0080	The slope of the compressor which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 6.24. (2 : 1)

11.3.5.119. **DRC1 Compressor Slope Low Setting Register(Default Value: 0x0000_0000)**

Offset: 0x0748			Register Name: AC_DRC1_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 6.24. (2 : 1)

11.3.5.120. **DRC1 Compressor High Output at Compressor Threshold Register(Default Value: 0x0000_F95B)**

Offset: 0x074C			Register Name: AC_DRC1_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor which is determined by the equation - OPC/6.0206 The format is 8.24.(-40dB)

11.3.5.121. **DRC1 Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)**

Offset: 0x0750			Register Name: AC_DRC1_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor which is determined by the equation OPC/6.0206. The format is 8.24. (-40dB)

11.3.5.122. **DRC1 Limiter Threshold High Setting Register(Default Value: 0x0000_01A9)**

Offset: 0x0754			Register Name: AC_DRC1_HLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which is set by the equation that LTin = -

			LT/6.0206, The format is 8.24. (-10dB)

11.3.5.123. **DRC1 Limiter Threshold Low Setting Register(Default Value: 0x0000_34F0)**

Offset: 0x0758			Register Name: AC_DRC1_LLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

11.3.5.124. **DRC1 Limiter Slope High Setting Register(Default Value: 0x0000_0005)**

Offset: 0x075C			Register Name: AC_DRC1_HKI
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0005	The slope of the limiter which is determined by the equation that KI = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 6.24. (50 :1)

11.3.5.125. **DRC1 Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)**

Offset: 0x0760			Register Name: AC_DRC1_LKI
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter which is determined by the equation that KI = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 6.24. (50 :1)

11.3.5.126. **DRC1 Limiter High Output at Limiter Threshold(Default Value: 0x0000_FBD8)**

Offset: 0x0764			Register Name: AC_DRC1_HOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter which is determined by equation OPT/6.0206. The format is 8.24 .(-25dB)

11.3.5.127. **DRC1 Limiter Low Output at Limiter Threshold(Default Value: 0x0000_FBA7)**

Offset: 0x0768			Register Name: AC_DRC1_LOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

15:0	R/W	0xFBA7	The output of the limiter which is determined by equation OPT/6.0206. The format is 8.24 .(-25dB)

11.3.5.128. **DRC1 Expander Threshold High Setting Register(Default Value: 0x0000_0BA0)**

Offset: 0x076C			Register Name: AC_DRC1_HET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

11.3.5.129. **DRC1 Expander Threshold Low Setting Register(Default Value: 0x0000_7291)**

Offset: 0x0770			Register Name: AC_DRC1_LET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

11.3.5.130. **DRC1 Expander Slope High Setting Register(Default Value: 0x0000_0500)**

Offset: 0x0774			Register Name: AC_DRC1_HKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0500	The slope of the expander which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 1/50. The format is 6.24. (1:5)

11.3.5.131. **DRC1 Expander Slope Low Setting Register(Default Value: 0x0000_0000)**

Offset: 0x0778			Register Name: AC_DRC1_LKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 1/50. The format is 6.24. (1:5)

11.3.5.132. **DRC1 Expander High Output at Expander Threshold Register(Default Value: 0x0000_F45F)**

Offset: 0x077C			Register Name: AC_DRC1_HOPE
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander which is determined by equation OPE/6.0206. The format is 8.24. (-70dB)

11.3.5.133. **DRC1 Expander Low Output at Expander Threshold Register(Default Value: 0x0000_8D6E)**

Offset: 0x0780			Register Name: AC_DRC1_LOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander which is determined by equation OPE/6.0206. The format is 8.24 .(-70dB)

11.3.5.134. **DRC1 Linear Slope High Setting Register(Default Value: 0x0000_0100)**

Offset: 0x0784			Register Name: AC_DRC1_HKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0100	The slope of the linear which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer . The format is 6.24. (1:1)

11.3.5.135. **DRC1 Linear Slope Low Setting Register(Default Value: 0x0000_0000)**

Offset: 0x0788			Register Name: AC_DRC1_LKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer . The format is 6.24. (1:1)

11.3.5.136. **DRC1 Smooth filter Gain High Attack Time Coef Register(Default Value:0x0000_0002)**

Offset: 0x078C			Register Name: AC_DRC1_SFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x002	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

11.3.5.137. **DRC1 Smooth filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)**

Offset: 0x0790	Register Name: AC_DRC1_SFLAT

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

11.3.5.138. **DRC1 Smooth Filter Gain High Release Time Coef Register(Default Value:0x0000_0000)**

Offset: 0x0794			Register Name: AC_DRC1_SFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

11.3.5.139. **DRC1 Smooth Filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)**

Offset: 0x0798			Register Name: AC_DRC1_SFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

11.3.5.140. **DRC1 MAX Gain High Setting Register(Default Value: 0x0000_FE56)**

Offset: 0x079C			Register Name: AC_DRC1_MXGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting which is determined by equation MXG/6.0206. The format is 8.24 and must be -20dB <MXG< 30dB .(-10dB)

11.3.5.141. **DRC1 MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)**

Offset: 0x07A0			Register Name: AC_DRC1_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting which is determined by equation MXG/6.0206. The format is 8.24 and must be -20dB <MXG < 30dB .(-10dB)

11.3.5.142. **DRC1 MIN Gain High Setting Register(Default Value: 0x0000_F95B)**

Offset: 0x07A4	Register Name: AC_DRC1_MNGHS

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting which is determined by equation MXG/6.0206. The format is 8.24 and must be -60dB ≤MNG ≤ -40dB .(-40dB)

11.3.5.143. **DRC1 MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)**

Offset: 0x07A8			Register Name: AC_DRC1_MNGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting which is determined by equation MNG/6.0206. The format is 8.24 and must be -60dB ≤MNG ≤ -40dB .(-40dB)

11.3.5.144. **DRC1 Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)**

Offset: 0x07AC			Register Name: AC_DRC1_EPSHC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000	The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

11.3.5.145. **DRC1 Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)**

Offset: 0x07B0			Register Name: AC_DRC1_EPSLC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

11.3.5.146. **DRC1 HPF Gain High Coef Register(Default Value: 0x0000_0100)**

Offset: 0x07B8			Register Name: AC_DRC1_HPFHGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x100	The gain of the HPF coefficient setting.Its format is 3.24.(gain = 1)

11.3.5.147. **DRC1 HPF Gain Low Coef Register(Default Value: 0x0000_0000)**

Offset: 0x07BC	Register Name: AC_DRC1_HPFLGAIN

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The gain of the HPF coefficient setting .Its format is 3.24.(gain = 1)

11.3.5.148. **AC Parameter Configuration Register(Default Value: 0x1000_0000)**

Address: 0x050967C0			Register Name: AC_PR_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	AC_PR_RST AC_PR reset 0: Assert 1: De-assert
27:25	/	/	/
24	R/W	0x0	AC_PR_RW AC_PR read or write 0: read 1: write
23:22	/	/	/
21:16	R/W	0x0	AC_PR _ADDR AC_PR address [5:0]
15:8	R/W	0x0	ADDA_PR _WDAT ADDA_PR write data [7:0]
7:0	R/W	0x0	ADDA_PR _RDAT ADDA_PR read data [7:0]

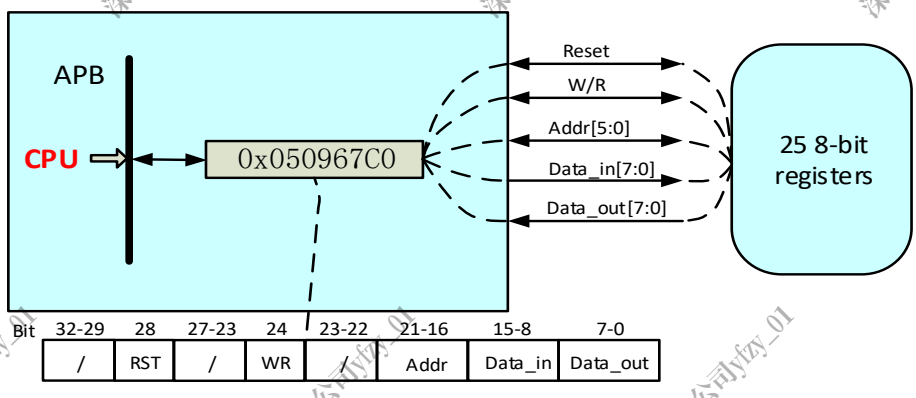
The Analog domain register can be written/read through the AC_PR Configuration Register(AC_PR_CFG_REG) which is in the PRCM Spec. To configure the codec analog domain circuit throught this register.

ADDR[5:0]: AC_PR Address;

W/R: Write/Read Enable;

WDAT[7:0]: Write Data;

RDAT[7:0]: Read Data;



11.3.5.149. **Left Output Mixer Control Register（Default Value: 0x00）**

Offset: 0x01			Register Name: LO_MIX_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	LMIXMUTE Left output mixer mute control 0: Mute 1: Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: / Bit 3: / Bit 2: LINEINL Bit 1: Left channel DAC Bit 0: Right channel DAC

11.3.5.150. **Right Output Mixer Control Register(Default Value: 0x00)**

Offset: 0x02			Register Name: RO_MIX_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	RMIXMUTE Right output mixer mute control 0: Mute 1: Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: / Bit 3: / Bit 2: LINEINR Bit 1: Right channel DAC Bit 0: Left channel DAC

11.3.5.151. **LINEOUT Control Register 0（Default Value: 0x00）**

Offset: 0x05			Register Name: LINEOUT _CTRL0
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	Lineout Left Enable 0: Disable 1: Enable
6	R/W	0x0	Lineout Right Enable 0: Disable 1: Enable

5	R/W	0x0	Left Lineout Source Select 0: Left output mixer 1: Left output mixer + right output mixer
4	R/W	0x0	Right Lineout Source Select 0: Right output mixer 1: Left Lineout, for differential output
3:0	/	/	/

11.3.5.152. **LINEOUT Control Register 1(Default Value: 0x00)**

Offset: 0x06			**Register Name: LINEOUT_CTRL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:5	/	/	/
4:0	R/W	0x0	LINEOUT Volume Control Total 30 level from 0x1F to 0x02 with the volume 0dB to -43.5dB, 1.5dB/step, mute when 00000 & 00001. 0dB(0x1f)

11.3.5.153. **MIC1 Control Register(Default Value: 0x34)**

Offset: 0x07			**Register Name: MIC1_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:4	R/W	0x3	MIC1G MIC1 Boost stage to L or R output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	R/W	0x0	MIC1AMPEN MIC1 Boost AMP enable 0: Disable 1: Enable
2:0	R/W	0x4	MIC1BOOST MIC1 Boost AMP gain control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB

11.3.5.154. **MIC2 Control Register(Default Value: 0x34)**

Offset: 0x08			**Register Name: MIC2_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:4	R/W	0x3	MIC2G MIC2 BOOST stage to L or R output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	R/W	0x0	MIC2AMPEN MIC2 Boost AMP enable

			0: Disable 1: Enable
2:0	R/W	0x4	MIC2BOOST MIC2 Boost AMP gain control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB

11.3.5.155. **Linein Control Register(Default Value: 0x03)**

Offset: 0x09			**Register Name: LINEIN_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:3	/	/	/
2:0	R/W	0x3	LINEING LINEINL/R to L/R output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

11.3.5.156. **Mixer and DAC Control Register(Default Value: 0x00)**

Offset: 0x0A			**Register Name: MIX_DAC_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	DACAREN Internal analog right channel DAC enable 0: Disable 1: Enable
6	R/W	0x0	DACALEN Internal analog left channel DAC enable 0: Disable 1: Enable
5	R/W	0x0	RMIXEN Right analog output Mixer enable 0: Disable 1: Enable
4	R/W	0x0	LMIXEN Left analog output Mixer enable 0: Disable 1: Enable
3:0	/	/	/

11.3.5.157. **Left ADC Mixer Control Register(Default Value: 0x00)**

Offset: 0x0B			**Register Name: L_ADCMIX_SRC**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	LADCMIXMUTE

			Left ADC mixer mute control 0: Mute 1: On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: / Bit 3: / Bit 2: LINEINL Bit 1: Left output mixer Bit 0: Right output mixer

11.3.5.158. **Right ADC Mixer Control Register(Default Value: 0x00)**

Offset: 0x0C			**Register Name: R_ADCMIX_SRC**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	RADCMIXMUTE Right ADC mixer mute control 0: Mute 1: On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: / Bit 3: / Bit 2: LINEINR Bit 1: Right output mixer Bit 0: Left output mixer

11.3.5.159. **ADC Control Register (Default Value: 0x03)**

Offset: 0x0D			**Register Name: ADC_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	ADCREN ADC right channel enable 0: Disable 1: Enable
6	R/W	0x0	ADCLEN ADC left channel enable 0: Disable 1: Enable
5	R/W	0x0	Dither select 0: New dither off 1: New dither on
4:3	/	/	/

2:0	R/W	0x3	ADCG ADC input gain control From -4.5dB to 6dB, 1.5dB/step default is 0dB

11.3.5.160. **Microphone Bias Control Register(Default Value: 0x21)**

Offset: 0x0E			**Register Name: MBIAS_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	MMICBIASEN Master microphone bias enable 0: Disable 1: Enable
6:5	R/W	0x1	MBIASSEL MMICBIAS voltage level select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.50V
4:2	/	/	/
1:0	R/W	0x1	Reserved

11.3.5.161. **Analog Performance Tuning Register(Default Value: 0xD6)**

Offset: 0x0F			**Register Name: APT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x1	MMIC BIAS chopper enable 0: Disable 1: Enable
6:5	R/W	0x2	MMIC BIAS chopper clock select 00: 250 kHz 01: 500 kHz 10: 1 MHz 11: 2 MHz
4	R/W	0x1	DITHER ADC dither on/off control 0: Dither off 1: Dither on
3:2	R/W	0x1	DITHER_CLK_SELECT ADC dither clock select 00: ADC FS * (8/9), about 43kHz when FS=48 kHz 01: ADC FS * (16/15), about 51kHz when FS=48 kHz 10: ADC FS * (4/3), about 64kHz when FS=48 kHz 11: ADC FS * (16/9), about 85kHz when FS=48 kHz
1:0	R/W	0x2	BIHE_CTRL

			BIHE control 00: No BIHE 01: BIHE=7.5 HOSC 10: BIHE=11.5 HOSC 11: BIHE=15.5 HOSC

11.3.5.162. **ZERO Cross &USB Bias Control Register(Default Value: 0x02)**

Offset: 0x12			**Register Name: ZC_VOL_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:3	/	/	/
2:0	R/W	0x2	USB_BIAS_CUR USB bias current tuning From 23uA to 30uA, default is 25uA

11.3.5.163. **Bias Calibration Control Register(Default Value: 0x00)**

Offset: 0x15			**Register Name: BIAS_CAL_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	/
6	R/W	0x0	CURRENT_TEST_SELECT Internal current sink test enable (from LINEIN pin) 0:Normal 1: For Debug
5:0	R/W	0x0	/

Chapter 12 Interfaces

12.1. TWI

12.1.1. Overview

The TWI is designed as an interface between CPU host and the serial TWI bus. It can support all the standard TWI transfer, including slave and master. The communication of the 2-wire bus is carried out by a byte-wise mode based on interrupt or polled handshaking. This TWI can be operated in standard mode (100 kbit/s) or fast-mode, supporting data rate up to 400 kbit/s. Multiple masters and 10-bit addressing mode are supported for this specified application. General call addressing is also supported in slave mode.

The TWI has the following features:

- Six TWIs
- Software-programmable for slave or master
- Supports repeated START signal
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Supports speed up to 400 kbit/s (‘fast mode’)
- Allows operation from a wide range of input clock frequency
- TWI Driver Supports packet transmission and DMA when TWI works in Master mode

12.1.2. Block Diagram

Figure 12-1 shows the block diagram of TWI.

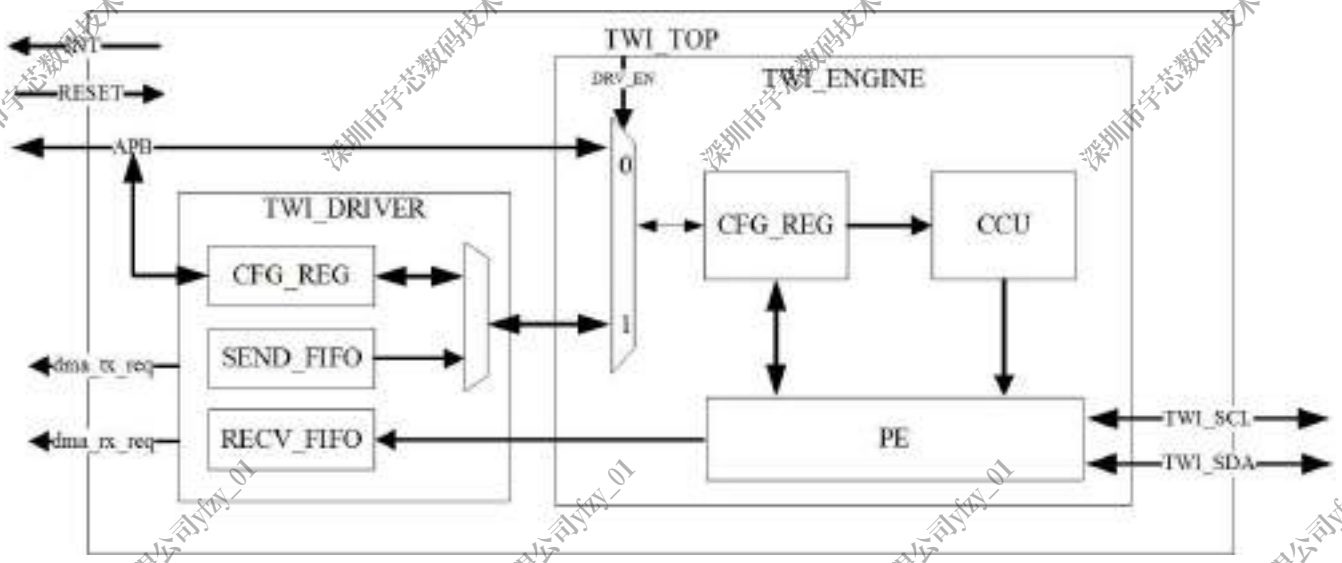


Figure 12-1. TWI Block Diagram

RESET: Module reset signal
INT: Module output interrupt signal
CFG_REG: Module configuration register in TWI
PE: Packet encoding/decoding
CCU: Module clock controller unit

12.1.3. Operations and Functional Descriptions

12.1.3.1. External Signals

The TWI controller has 6 TWIs.Table 12-1 describes the external signals of TWI. TWI_SCK and TWI_SDA are bidirectional I/O,When TWI is configured as Master device,TWI_SCK is output pin;when TWI is configurable as Slave device,TWI_SCK is input pin.other TWI ports are used as General Purpose I/O ports.For information about General Purpose I/O ports,see **Port Controller** in chapter12.

Table 12-1. TWI External Signals

Signal (x=[3:0])	Description	Type
TWIx_SCK	TWI Clock Signal for CPUX	I/O
TWIx_SDA	TWI Serial Data for CPUX	I/O
S_TWI0_SCK	TWI Serial Clock Signal for CPUS	I/O
S_TWI0_SDA	TWI Serial Data Signal for CPUS	I/O
S_TWI1_SCK	TWI Serial Clock Signal for CPUS	I/O
S_TWI1_SDA	TWI Serial Data Signal for CPUS	I/O

12.1.3.2. Clock Sources

Each TWI controller has a fixed clock source.APB2 is the clock source of TWI in CPUX and APBS is the clock source of R-TWI in CPUS.The APB Bus get some clock sources.Users can select one of them to be used as APB clock.Table 12-2

describes the clock sources for TWI.Users can see **Clock Controller Unit(CCU)** in chapter 3 for clock setting, configuration and gating information.

Table 12-2. TWI Clock Sources

Clock Sources	Description
APBS_CLK	TWI in CPUS,for details on APBS refer to PRCM
APB2_CLK	TWI in CPUX,for details on APB2 refer to CCU

After select a proper clock, for using the TWI in CPUX,user must open the gating of TWI and release the reset bit. For using the TWI in CPUS,user also need to open the gating of R-TWI and release the reset bit . For more details on the gating/reset operations ,please refer to the **CCU.**

12.1.3.3. **Master and Slave Mode**

There are four operation modes on the TWI bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to its registers. TWI transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit of the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit to high.

In Slave Mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

12.1.4. TWI Driver

TWI Driver is only supported for master mode. When TWI works in master mode, TWI Driver drives TWI Engine for one or more packet transmission instead of CPU host. Packet transmission is defined as follow, Reg address bytes and Write data bytes are buffered in SEND FIFO, Read data is buffered in RECV FIFO.

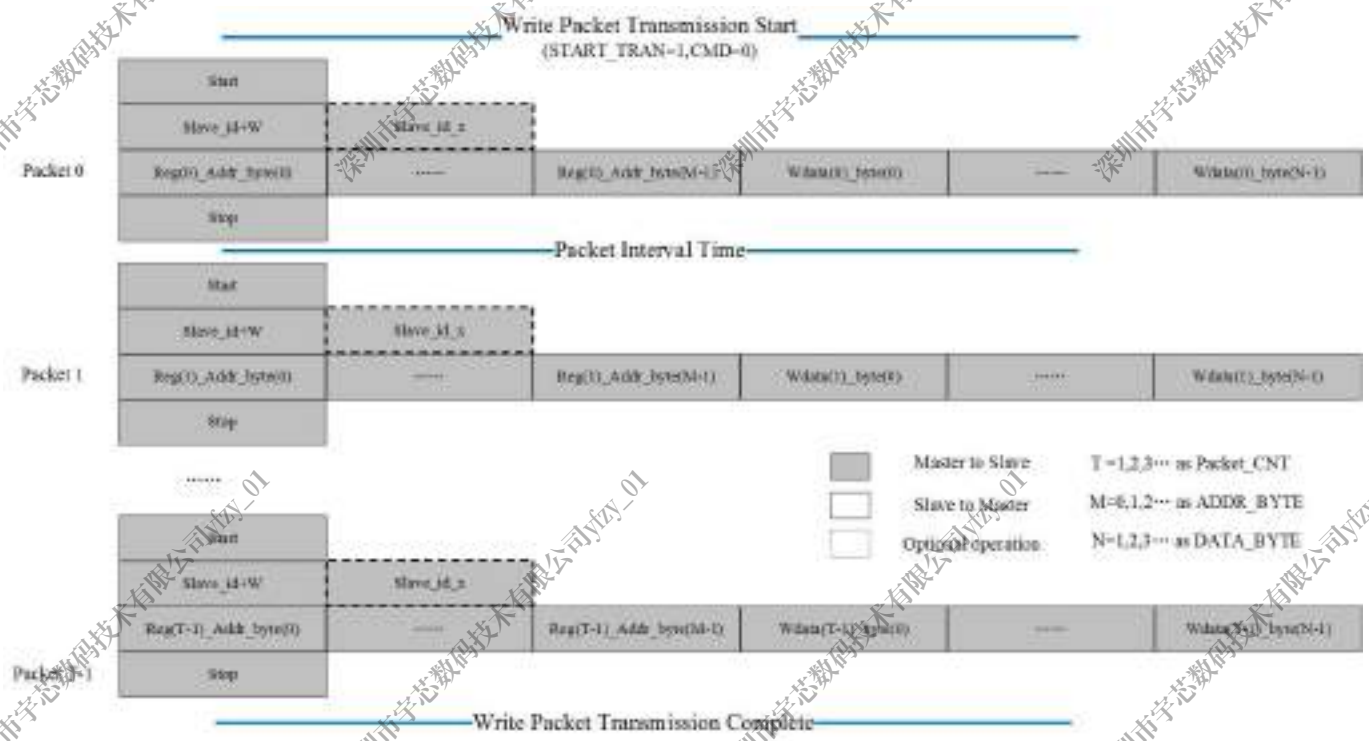


Figure 12-2. TWI Driver Write Packet Transmission

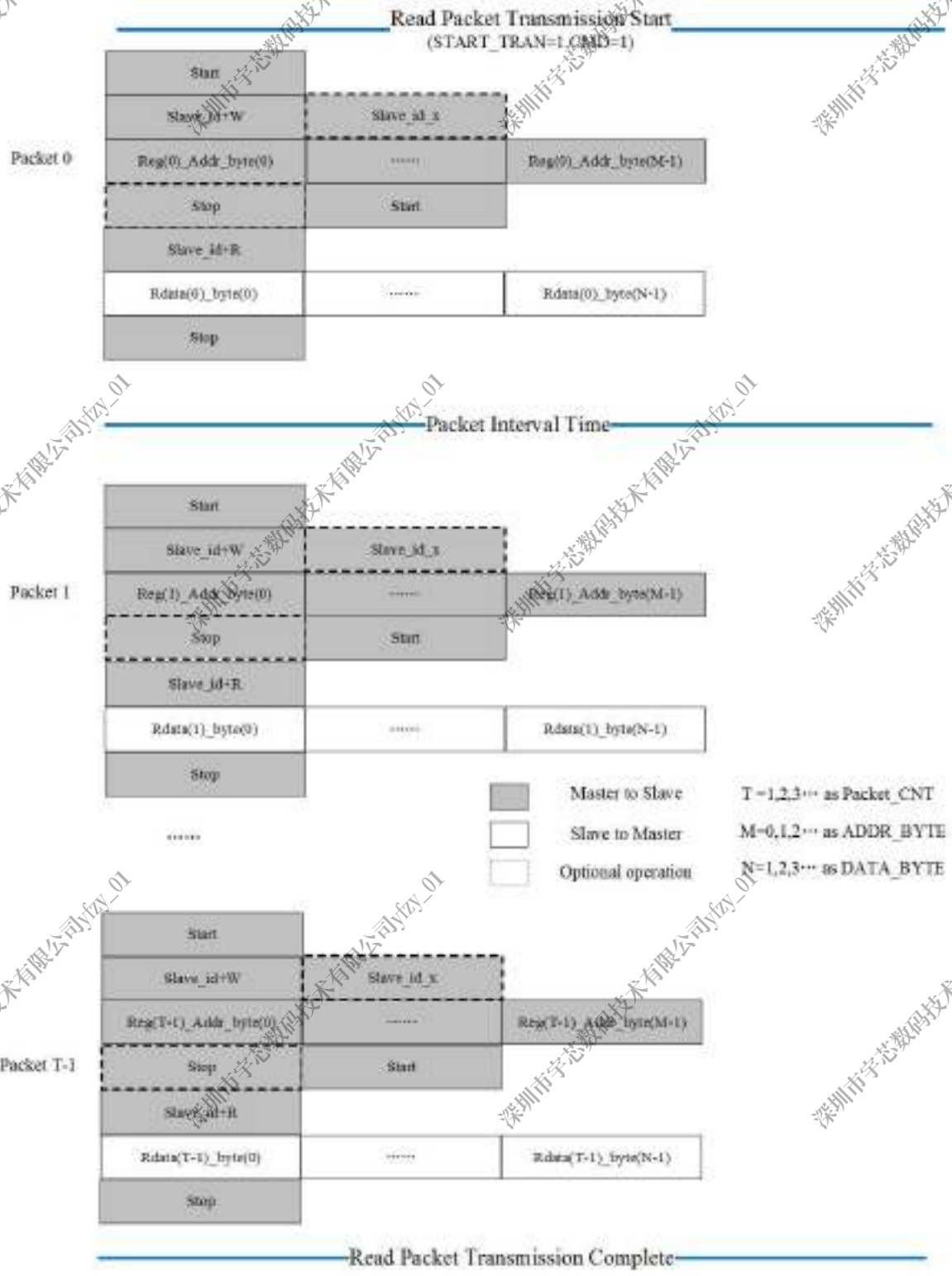


Figure 12-3. TWI Driver Write Packet Transmission

12.1.5. Programming Guidelines

The TWI controller operates in 8-bit data format. The data on the TWI_SDA line is always 8 bits long.At first,the TWI controller will sent a start condition.When in the addressing formats of 7-bit,TWI sends out a 8 bits message which include 7 MSB slave address and 1 LSB read/write flag.The least significant of the salve address indicates the direction of transmission.When TWI works in 10 bit slave address mode,the operation will be divided into two steps,for details on the

operation please refer to **TWI_ADDR** and **TWI_XADDR**.

Figure 12-4 shows a software operation flow of TWI Initialization.

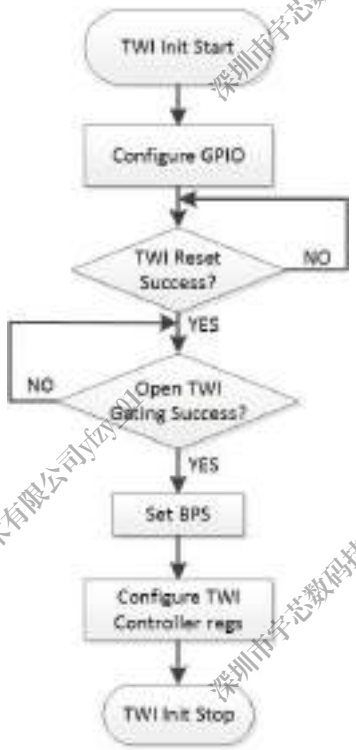


Figure 12-4. TWI Initial Flow

Figure 12-5 shows a software operation flow to control TWI engine write to device.

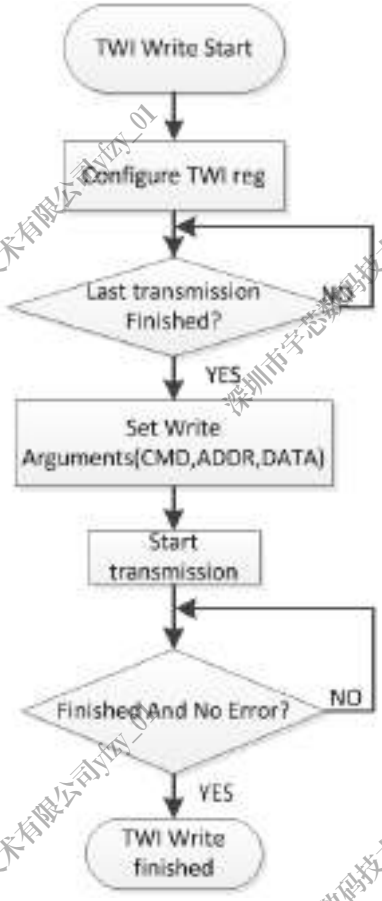


Figure 12-5. TWI Write Flow

Figure 12-6 shows a software operation flow to control TWI engine read from device.

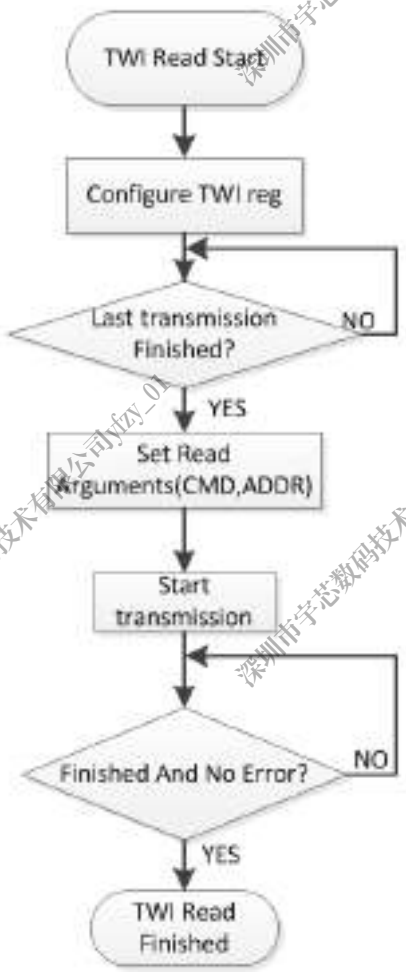


Figure 12-6. TWI Read Flow

Figure 12-7 shows a software operation flow for packet transmission by TWI Driver.

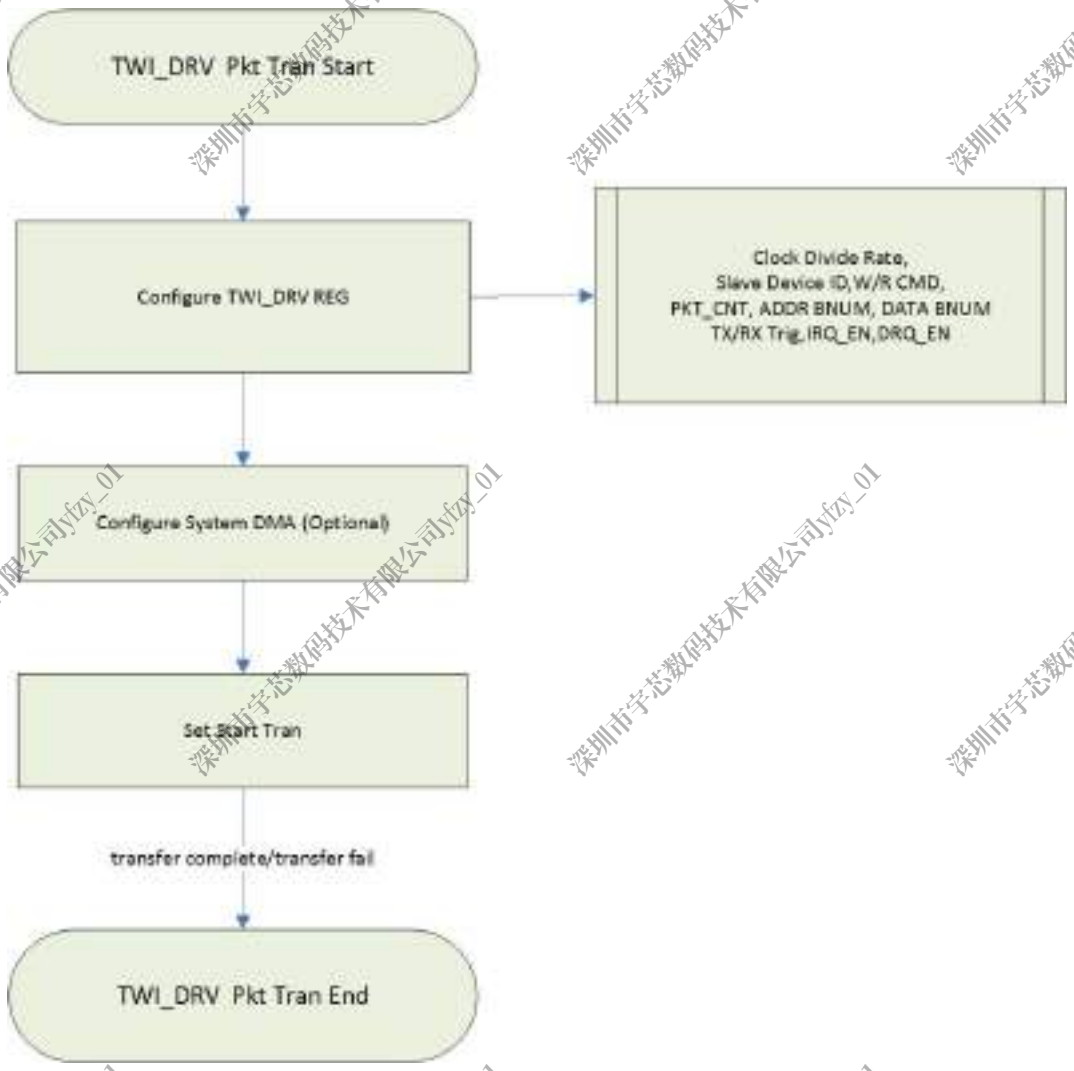


Figure 12-7. TWI Driver Packet Tran Flow

12.1.6. Register List

Module Name	Base Address
TWI0	0x05002000
TWI1	0x05002400
TWI2	0x05002800
TWI3	0x05002C00
R_TWI0	0x07081400
R_TWI1	0x07081800

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave Address
TWI_XADDR	0x0004	TWI Extended Slave Address
TWI_DATA	0x0008	TWI Data Byte
TWI_CNTR	0x000C	TWI Control Register
TWI_STAT	0x0010	TWI Status Register

TWI_CCR	0x0014	TWI Clock Control Register
TWI_SRST	0x0018	TWI Software Reset
TWI_EFR	0x001C	TWI Enhance Feature Register
TWI_LCR	0x0020	TWI Line Control Register
TWI_DRV_CTRL	0x0200	TWI_DRV Control Register
TWI_DRV_CFG	0x0204	TWI_DRV Transmission Configuration Register
TWI_DRV_SLV	0x0208	TWI_DRV Slave ID Register
TWI_DRV_FMT	0x020C	TWI_DRV Packet Format Register
TWI_DRV_BUS_CTRL	0x0210	TWI_DRV Bus Control Register
TWI_DRV_INT_CTRL	0x0214	TWI_DRV Interrupt Control Register
TWI_DRV_DMA_CFG	0x0218	TWI_DRV DMA Configure Register
TWI_DRV_FIFO_CON	0x021C	TWI_DRV FIFO Content Register
TWI_DRV_SEND_FIFO_ACC	0x0300	TWI_DRV Send Data FIFO Access Register
TWI_DRV_RECV_FIFO_ACC	0x0304	TWI_DRV Receive Data FIFO Access Register

12.1.7. Register Description

12.1.7.1. **TWI Slave Address Register(Default Value:0x0000_0000)**

Offset: 0x0000			**Register Name: TWI_ADDR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:1	R/W	0x0	SLA Slave Address 7-bit addressing: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing: 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General Call Address Enable 0: Disable 1: Enable

NOTE

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

12.1.7.2. **TWI Extend Address Register(Default Value:0x0000_0000)**

Offset: 0x0004			Register Name: TWI_XADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

12.1.7.3. **TWI Data Register(Default Value:0x0000_0000)**

Offset: 0x0008			Register Name: TWI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte transmitted or received

12.1.7.4. **TWI Control Register(Default Value:0x0000_0000)**

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus ISDA/ISCL is ignored and the TWI Controller will not respond to any address on the bus 1: The TWI will respond to calls to its slave address – and to the general call address if the GCE bit in the ADDR register is set. In master operation mode, this bit should be set to '1'.
5	R/WAC	0x0	M_STA Master Mode Start When M_STA is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released.

			The M_STA bit is cleared automatically after a START condition has been sent. Writing a '0' to this bit has no effect.
4	R/W1C	0x0	M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will indicate if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically, writing a '0' to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: 1. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. 2. The general call address has been received and the GCE bit in the ADDR register is set to '1'. 3. A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	/	/	/

12.1.7.5. **TWI Status Register(Default Value:0x0000_00F8)**

Offset: 0x0010			**Register Name: TWI_STAT**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte **Code Status** 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

12.1.7.6. **TWI Clock Register(Default Value:0x0000_0000)**

Offset: 0x0014			**Register Name: TWI_CCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:3	R/W	0x0	CLK_M
2:0	R/W	0x0	CLK_N

			The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48MHz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48MHz/2^2=12MHz, F1= F0/(10*(2+1)) = 0.4MHz For 100kHz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48MHz/2^2=12MHz, F1=F0/(10*(11+1)) = 0.1MHz

12.1.7.7. **TWI Soft Reset Register(Default Value:0x0000_0000)**

Offset: 0x0018			**Register Name: TWI_SRST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write ‘1’ to this bit to reset the TWI and clear to ‘0’ when completing Soft Reset operation.

12.1.7.8. **TWI Enhance Feature Register(Default Value:0x0000_0000)**

Offset: 0x001C			**Register Name: TWI_EFR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
0:1	R/W	0x0	DBN Data Byte Number Follow Read Command Control 00 : No data byte can be written after read command 01 : Only 1 byte data can be written after read command 10 : 2 bytes data can be written after read command 11 : 3 bytes data can be written after read command

12.1.7.9. **TWI Line Control Register(Default Value:0x0000_003A)**

Offset: 0x0020			**Register Name: TWI_LCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R	0x1	SCL_STATE Current State of TWI_SCL

			0 : Low 1 : High
4	R	0x1	SDA_STATE Current State of TWI_SDA 0 : Low 1 : High
3	R/W	0x1	SCL_CTL TWI_SCL Line State Control Bit When line control mode is enabled (bit[2] set), this bit decides the output level of TWI_SCL. 0 : Output low level 1 : Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL Line State Control Enable When this bit is set, the state of TWI_SCL is controlled by the value of bit[3]. 0 : Disable TWI_SCL line control mode 1 : Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA Line State Control Bit When line control mode is enabled (bit[0] set), this bit decides the output level of TWI_SDA. 0 : Output low level 1 : Output high level
0	R/W	0x0	SDA_CTL_EN TWI_SDA Line State Control Enable When this bit is set, the state of TWI_SDA is controlled by the value of bit[1]. 0 : Disable TWI_SDA line control mode 1 : Enable TWI_SDA line control mode

12.1.7.10. **TWI_DRV Control Register(Default Value:0x00F8_0000)**

Offset: 0x0200			**Register Name: TWI_DRV_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	START_TRAN 0: Transmission idle 1: Start transmission Automatically cleared to '0' when finished. If slave not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. All format setting and data will be loaded from registers and FIFO when transmission start.
30	/	/	/
29	R/W	0x0	RESTART_MODE 0: RESTART 1: STOP+START Define the TWI_DRV action after sending register address.

28	R/W	0x0	READ_TRAN_MODE 0: send slave_id+W 1: do not send slave_id+W **Setting this bit to 1 if reading from a slave which register width is equal to 0**.
27:24	R	0x0	TRAN_RESULT 000: OK 001: FAIL Other: Reserved
23:16	R	0xf8	TWI_STA 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9th SCL clk Other: Reserved
15:2	/	/	/
1	R/W	0x0	SOFT_RESET 0: normal 1: reset
0	R/W	0x0	TWI_DRV_EN 0: Module disable 1: Module enable (only use in TWI Master Mode)

12.1.7.11. **TWI_DRV Transmission Configuration Register(Default Value:0x1000_0001)**

Offset: 0x0204			**Register Name: TWI_DRV_CFG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x10	TIMEOUT_N When sending the 9th clock, assert fail signal when slave device did not response after **N*F$_{SCL}$** cycles. And software must do a reset to TWI_DRV module and send a stop condition to slave.
23:16	R/W	0x0	PKT_INTERVAL Define the interval between each packet in 32*F$_{SCL}$ cycles. 0~255
15:0	R/W	0x1	PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format.

12.1.7.12. **TWI_DRV Slave ID Register(Default Value:0x0000_0000)**

Offset: 0x0208			Register Name: TWI_DRV_SLV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:9	R/W	0x0	SLV_ID Slave device ID • 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 • 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
8	R/W	0x0	CMD R/W operation to slave device 0: write 1: read
7:0	R/W	0x0	SLV_ID_X SLAX[7:0], low 8 bits for slave device ID with 10-bit addressing

12.1.7.13. **TWI_DRV Packet Format Register(Default Value:0x0001_0001)**

Offset: 0x020C			Register Name: TWI_DRV_FMT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x1	ADDR_BYTE How many bytes be sent as slave device reg address 0~255
15:0	R/W	0x1	DATA_BYTE How many bytes be sent/received as data 1~65535

12.1.7.14. **TWI_DRV Bus Control Register(Default Value:0x0000_00C0)**

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x0	CLK_N TWI_DRV bus sampling clock F0=24MHz/2^CLK_N
11:8	R/W	0x0	CLK_M TWI_DRV output SCL frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status

5:4	/	/	/
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output en
0	R/W	0x0	SDA_MOE SDA manual output en

12.1.7.15. **TWI_DRV Interrupt Control Register(Default Value:0x0000_0000)**

Offset: 0x0214			**Register Name: TWI_DRV_INT_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
19	R/W	0x0	RX_REQ_INT_EN
18	R/W	0x0	TX_REQ_INT_EN
17	R/W	0x0	TRAN_ERR_INT_EN
16	R/W	0x0	TRAN_COM_INT_EN
15:4	/	/	/
3	R/W1C	0x0	RX_REQ_PD Set when the data byte number in RECV_FIFO reaches RX_TRIG
2	R/W1C	0x0	TX_REQ_PD Set when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO
1	R/W1C	0x0	TRAN_ERR_PD Packet transmission failed pending
0	R/W1C	0x0	TRAN_COM_PD Packet transmission completed pending

12.1.7.16. **TWI_DRV DMA Configure Register(Default Value:0x0010_0010)**

Offset: 0x0218			**Register Name: TWI_DRV_DMA_CFG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DMA_RX_EN
23:22	/	/	/
21:16	R/W	0x10	RX_TRIG When DMA_RX_EN set, send DMA RX Req when the data byte number in RECV_FIFO reaches RX_TRIG or Read Packet Transmission completed with RECV_FIFO not empty
15:9	/	/	/
8	R/W	0x0	DMA_TX_EN
7:6	/	/	/

5:0	R/W	0x10	TX_TRIG When DMA_TX_EN set, send DMA TX Req when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO

12.1.7.17. **TWI_DRV FIFO Content Register(Default Value:0x0000_0000)**

Offset: 0x021C			**Register Name: TWI_DRV_FIFO_CON**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/WAC	0x0	RECV_FIFO_CLEAR Set this bit to clear RECV_FIFO pointer, and this bit cleared automatically
21:16	R	0x0	RECV_FIFO_CONTENT The number of data in RECV_FIFO
15:7	/	/	/
6	R/WAC	0x0	SEND_FIFO_CLEAR Set this bit to clear SEND_FIFO pointer, and this bit cleared automatically
5:0	R	0x0	SEND_FIFO_CONTENT The number of data in SEND_FIFO

12.1.7.18. **TWI_DRV Send Data FIFO Access Register(Default Value:0x0000_0000)**

Offset: 0x0300			**Register Name: TWI_DRV_SEND_FIFO_ACC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	SEND_DATA_FIFO Address of a 32x8 SEND_FIFO ,which stores reg address and data sending to slave device

12.1.7.19. **TWI_DRV Receive Data FIFO Access Register(Default Value:0x0000_0000)**

Offset: 0x0304			**Register Name: TWI_DRV_RECV_FIFO_ACC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	RECV_DATA_FIFO Address of a 32x8 RECV_FIFO ,which stores data received from slave device

12.2. UART

12.2.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in systems where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR Mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

The UART has the following features:

- Compatible with industry-standard 16550 UARTs
- 256 Bytes Transmit and Receive data FIFOs
- Capable of speed up to 5 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports Even, Odd or No Parity
- Supports DMA controller interface
- Supports Software/ Hardware Flow Control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

12.2.2. Block Diagram

Figure 12-5 shows a block diagram of the UART.

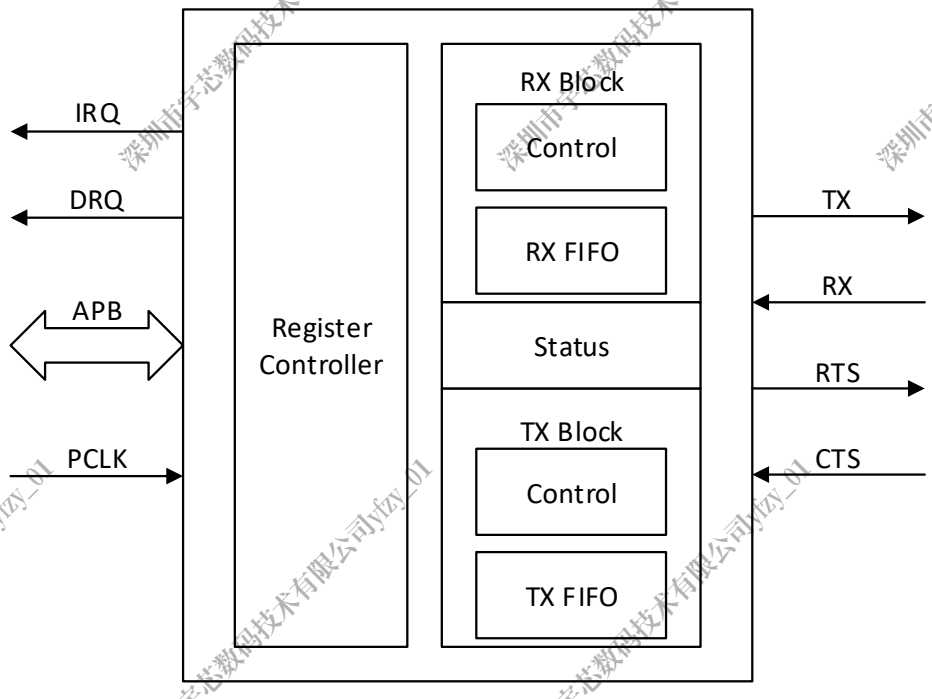


Figure 12-8. UART Block Diagram

12.2.3. Operations and Functional Descriptions

12.2.3.1. External Signals

Table 12-3 describes the external signals of UART.

Table 12-3. UART External Signals

Signal	Type	Description
UART0_TX	O	Serial Data Output
UART0_RX	I	Serial Data Input
UART1_TX	O	Serial Data Output
UART1_RX	I	Serial Data Input
UART1_CTS	I	Clear to Send
UART1_RTS	O	Request to Send
UART2_TX	O	Serial Data Output
UART2_RX	I	Serial Data Input
UART2_CTS	I	Clear to Send
UART2_RTS	O	Request to Send
UART3_TX	O	Serial Data Output
UART3_RX	I	Serial Data Input
UART3_CTS	I	Clear to Send
UART3_RTS	O	Request to Send
UART4_TX	O	Serial Data Output
UART4_RX	I	Serial Data Input
UART4_CTS	I	Clear to Send
UART4_RTS	O	Request to Send

S_UART_TX	O	Serial Data Output
S_UART_RX	I	Serial Data Input

12.2.3.2. **Clock Sources**

Table 12-4 describes the clock sources of UART.

Table 12-4. UART Clock Sources

Clock Sources	Description
APB2_CLK	Clock of APB2

12.2.3.3. **Typical Application**

Figure 12-9 shows the application block diagram of UART.

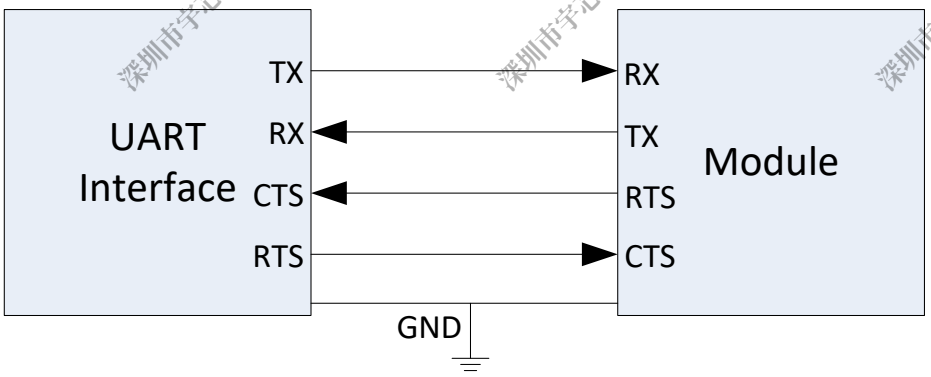


Figure 12-9. UART Application Diagram

12.2.3.4. **UART Timing Diagram**

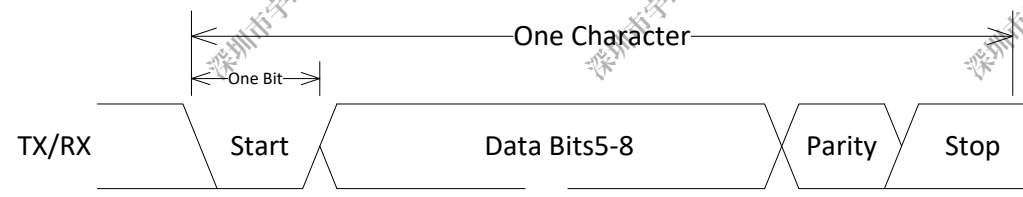


Figure 12-10. UART Serial Data Format

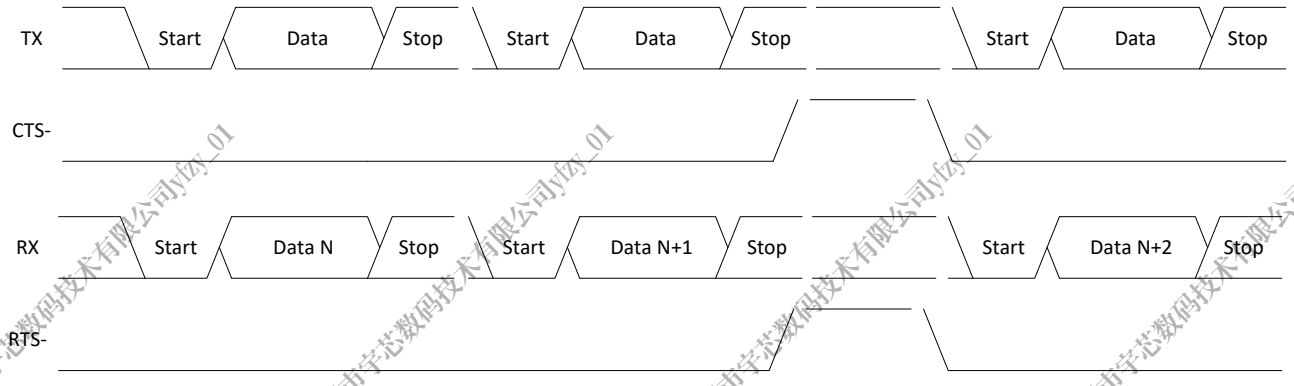


Figure 12-11. RTS/CTS Autoflow Control Timing

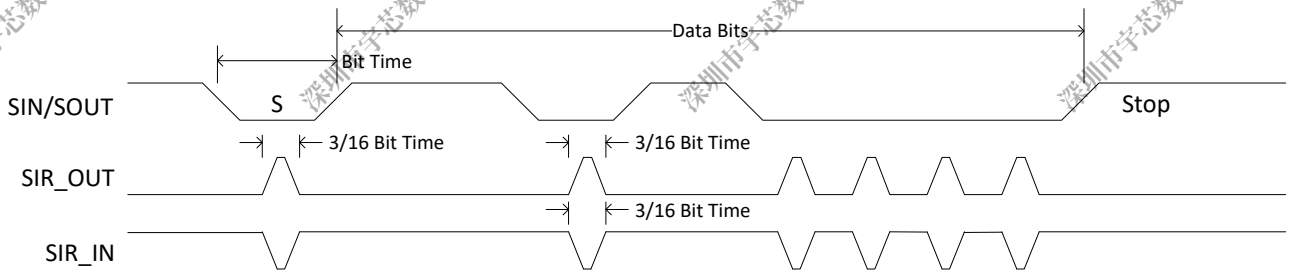


Figure 12-12. Serial IrDA Data Format

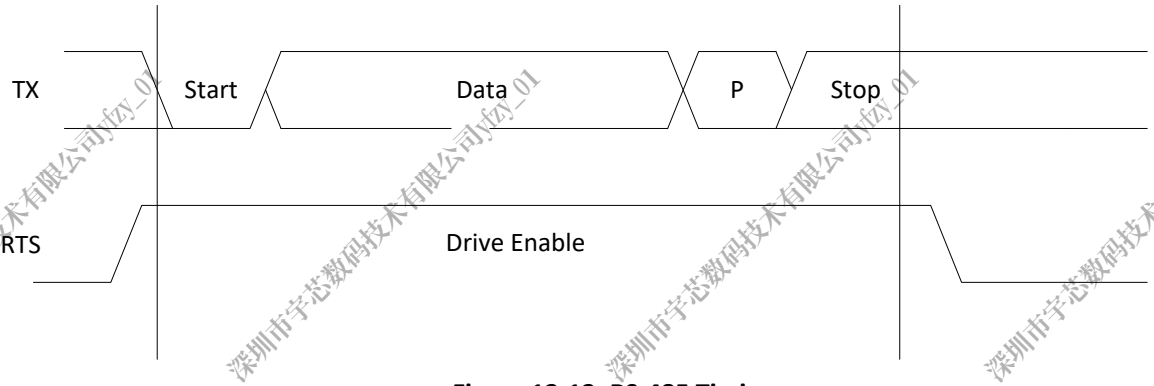


Figure 12-13. RS-485 Timing

12.2.3.5. **UART Operating Mode**

12.2.3.5.1. Basic Mode Setting

The UART_LCR register can set basic parameter of a data frame: data width, stop bit number, parity type.

A frame transfer of the UART includes the start signal, data signal, parity bit and stop signal. The LSB is transmitted first.

- Start signal(start bit): It is the start flag of a data frame. According to UART protocol, the low level of TXD signal indicates the start of a data frame. When the UART does transmit data, the level need hold high.
- Data signal(data bit): The data bit width can be configured as 5-bit,6-bit,7-bit,8-bit through different applications.
- Parity bit: It is 1-bit error correction signal. Parity bit includes odd parity, even parity. The UART can enable and disable the parity bit by setting the UART_LCR register.
- Stop Signal(stop bit): It is the stop bit of a data frame. The stop bit can be set to 1-bit,1.5-bit and 2-bit by the UART_LCR register. The high level of TXD signal indicates the end of a data frame.

12.2.3.5.2. Baud Rate Setting

The baud rate is calculated as follows: Baud rate = SCLK /（16 * divisor）.SCLK is usually APB2 and can be set in CCU.

Divisor is frequency divider of UART. The frequency divider has 16-bit,the low 8-bit is in the UART_DLL register, the high 8-bit is in the UART_DLH register.

The relationship between different UART mode and error rate is as follows.

Table 12-5. UART Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Over sampling	Error(%)

24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
64000000	7	576000	16	-0.794
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
64000000	1	4000000	16	0

Table 12-6. IrDA Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	3/16	0
24000000	2500	600	3/16	0
24000000	1250	1200	3/16	0
24000000	625	2400	3/16	0
24000000	313	4800	3/16	-0.16
24000000	156	9600	3/16	0.16
24000000	78	19200	3/16	0.16
24000000	39	38400	3/16	0.16
24000000	26	57600	3/16	0.16
24000000	13	115200	3/16	0.16

Table 12-7. RS485 Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16

12.2.3.5.3. DLAB Setting

DLAB control bit (UART_LCR[7]) is the access control bit of divisor Latch register.
If DLAB is 0, then 0x00 offset address is TX/RX FIFO register, 0x04 offset address is IER register.
If DLAB is 1, then 0x00 offset address is DLL register, 0x04 offset address is DLH register.
When UART initial, divisor need be set. That is, writing 1 to DLAB can access the DLL and DLH register, after finished setting, writing 0 to DLAB can access the TX/RX FIFO register.

12.2.3.5.4. CHCFG_AT_BUSY Setting

The function of CHCFG_AT_BUSY(UART_HALT[1]) and CHANGE_UPDATE(UART_HALT[2]) are as follows.
CHCFG_AT_BUSY(configure at busy): Enable the bit, software can also set UART controller when UART is busy, such as the LCR,DLH,DLL register.
CHANGE_UPDATE(change update): If CHCFG_AT_BUSY is enabled, and CHANGE_UPDATE is written to 1, the configuration of UART controller can be updated. After completed update, the bit is cleared to 0 automatically.
Setting divisor, performs the following steps:
Step1 Write CHCFG_AT_BUSY to 1
Step2 Write DLAB to 1, and set DLH and DLL
Step3 Write CHANGE_UPDATE to update configuration. The bit is cleared to 0 automatically after completed update.

12.2.3.5.5. UART Busy

UART_USR[0] is a busy flag of UART controller or not.
When TX transmits data, or RX receives data,or TX FIFO is not empty, or RX FIFO is not empty, then the BUSY flag bit can be set to 1 by hardware, which indicates the UART controller is busy.

12.2.4. Programming Guidelines

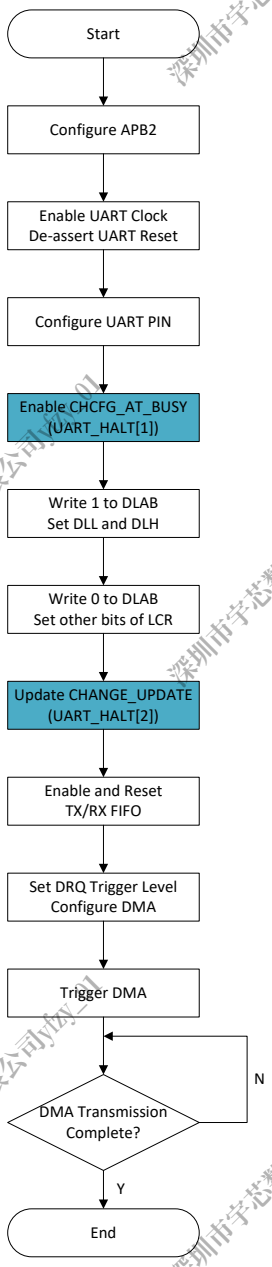


Figure 12-14. UART DRQ Flow Chart

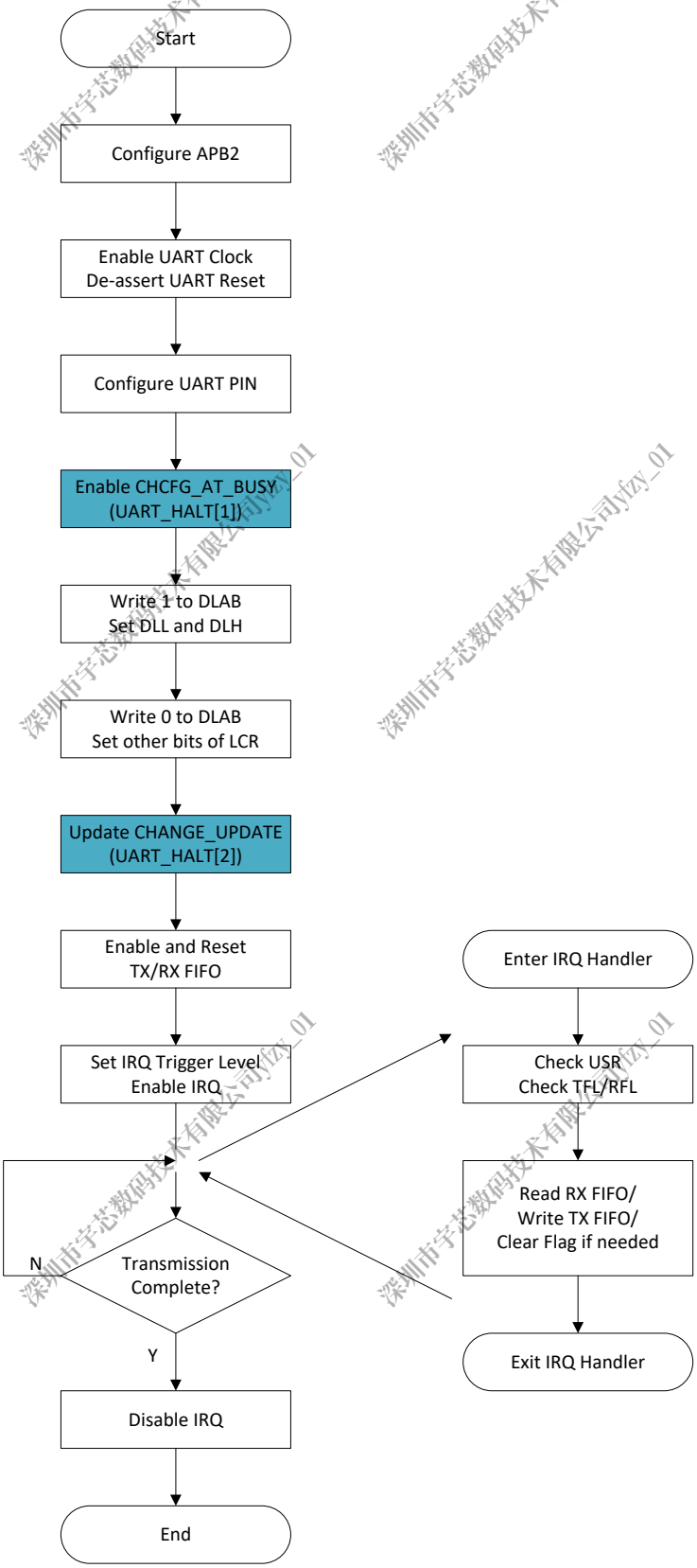


Figure 12-15. UART IRQ Flow Chart

12.2.5. Register List

Module Name	Base Address

UART0	0x05000000
UART1	0x05000400
UART2	0x05000800
UART3	0x05000C00
UART4	0x05001000
R_UART	0x07080000

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level Register
UART_RFL	0x0084	UART Receive FIFO Level Register
UART_HSK	0x0088	UART DMA Handshake Configuration Register
UART_HALT	0x00A4	UART Halt TX Register
UART_DBG_DLL	0x00B0	UART Debug DLL Register
UART_DBG_DLH	0x00B4	UART Debug DLH Register
UART_485_CTL	0x00C0	UART RS485 Control and Status Register
RS485_ADDR_MATCH	0x00C4	UART RS485 Address Match Register
BUS_IDLE_CHK	0x00C8	UART RS485 Bus Idle Check Register
TX_DLY	0x00CC	UART TX Delay Register

12.2.6. Register Description

12.2.6.1. UART Receiver Buffer Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_RBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set.

			If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

12.2.6.2. **UART Transmit Holding Register(Default Value: 0x0000_0000)**

Offset: 0x0000			**Register Name: UART_THR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	THR Transmit Holding Register Data be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

12.2.6.3. **UART Divisor Latch Low Register(Default Value: 0x0000_0000)**

Offset: 0x0000			**Register Name: UART_DLL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

12.2.6.4. **UART Divisor Latch High Register(Default Value: 0x0000_0000)**

Offset: 0x0004			**Register Name: UART_DLH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLH Divisor Latch High

			Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

12.2.6.5. **UART Interrupt Enable Register(Default Value: 0x0000_0000)**

Offset: 0x0004			**Register Name: UART_IER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	RS485_INT_EN RS485 Interrupt Enable 0:Disable 1:Enable
3	R/W	0x0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0x0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0x0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0x0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

12.2.6.6. **UART Interrupt Identity Register(Default Value: 0x0000_0001)**

Offset: 0x0008			Register Name: UART_IIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0011: RS485 Interrupt 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Fourth	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Fifth	Transmit holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow	Reading the Modem status Register

			control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

12.2.6.7. **UART FIFO Control Register(Default Value: 0x0000_0000)**

Offset: 0x0008			**Register Name: UART_FCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	W	0x0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO when the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0x0	TFT TX Empty Trigger This is used to select the empty threshold level when the THRE Interrupts are generated and the mode is active. It also determines when the dma_tx_req_n signal is asserted in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0x0	DMAM DMA Mode 0: Mode 0 In this mode, if PTE is high and TX FIFO is enabled, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is high and TX FIFO is disabled, the TX DMA request will send when THRE is empty. If PTE is low, the TX DMA request will send when the TX FIFO is empty. If dma_pte_rx is high and RX FIFO is enabled, the rx drq will send when RFL is equal to or more than FIFO Trigger Level. 1: Mode 1 In this mode, if TX FIFO is enabled and the PTE is high, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is low, the TX DMA request will send when TX FIFO is empty and the request stops only when TX FIFO is full. If RFL is equal to or more than FIFO Trigger Level, the rx drq will be set 1, in otherwise, it will be set 0.
2	W	0x0	XFIFOR XMIT FIFO Reset

			The bit resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0x0	RFIFOR RCVR FIFO Reset The bit resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0x0	FIFOE Enable FIFOs The bit enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed, both the XMIT and RCVR controller portion of FIFOs is reset.

12.2.6.8. **UART Line Control Register(Default Value: 0x0000_0000)**

Offset: 0x000C			**Register Name: UART_LCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0x0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to 1, the serial output is forced to the spacing (logic 0) state. When not in Loopback mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE is enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0x0	EPS Even Parity Select It is writeable only when UART is not busy (USR[0] is zero) and always writable/readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is unset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4] In RS485 mode, it is the 9th bit--address bit. 11:9th bit = 0, indicates that this is a data byte. 10:9th bit = 1, indicates that this is an address byte. When using this function, PEN(LCR[3]) must be set to 1.
3	R/W	0x0	PEN Parity Enable

			It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: Parity disabled 1: Parity enabled
2	R/W	0x0	STOP Number of stop bits It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to 0, one stop bit is transmitted in the serial data. If set to 1 and the data bits are set to 5 (LCR[1:0] is set to 0), one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0x0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

12.2.6.9. **UART Modem Control Register(Default Value: 0x0000_0000)**

Offset: 0x0010			**Register Name: UART_MCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	UART_FUNCTION Select IrDA or RS485 00:UART Mode 01:IrDA SIR Mode 10:RS485 Mode 11:Reserved
5	R/W	0x0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled
4	R/W	0x0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n,

			cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0x0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The RTS (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0x0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. 0: dtr_n de-asserted (logic 1) 1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

12.2.6.10. **UART Line Status Register(Default Value: 0x0000_0060)**

Offset:0x0014			**Register Name: UART_LSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided, there are no subsequent errors in the FIFO.
6	R	0x1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	0x1	THRE TX Holding Register Empty

			If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0x0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sir_in, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	RC	0x0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	RC	0x0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	RC	0x0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at

			the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0x0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

12.2.6.11. **UART Modem Status Register(Default Value: 0x0000_0000)**

Offset: 0x0018			**Register Name: UART_MSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted, it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0x0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted, it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0x0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted, it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	R	0x0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted, it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1)

			1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RC	0x0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. If the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	RC	0x0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	RC	0x0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	RC	0x0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

12.2.6.12. **UART Scratch Register(Default Value: 0x0000_0000)**

Offset: 0x001C			**Register Name: UART_SCH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

12.2.6.13. **UART Status Register(Default Value: 0x0000_0006)**

Offset: 0x007C			Register Name: UART_USR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0x0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	0x1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	0x1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0x0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

12.2.6.14. **UART Transmit FIFO Level Register(Default Value: 0x0000_0000)**

Offset: 0x0080			Register Name: UART_TFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

12.2.6.15. **UART Receive FIFO Level Register(Default Value: 0x0000_0000)**

Offset: 0x0084			Register Name: UART_RFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	RFL

			Receive FIFO Level This is indicates the number of data entries in the receive FIFO.

12.2.6.16. **UART DMA Handshake Configuration Register(Default Value: 0x0000_00E5)**

Offset: 0x0088			Register Name: UART_HSK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xE5	Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode

12.2.6.17. **UART Halt TX Register(Default Value: 0x0000_0000)**

Offset: 0x00A4			Register Name: UART_HALT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTE The sending of TX_REQ. In DMA1 mode (FIFO on), if PTE is set to 1, when TFL is less than trig, send the DMA request. If PTE is set to 0, when FIFO is empty, send the DMA request. The DMA request will stop when FIFO is full. In DMA0 mode, if PTE is set to 1 and FIFO is on, when TFL is less than trig, send DMA request. If PTE is set to 1 and FIFO is off, when THRE is empty, send DMA request. If PTE is set to 0, when FIFO is empty, send DMA request.
6	R/W	0x0	DMA_PTE_RX The sending of RX_DRQ. In DMA1 mode, when RFL is more than or equal to trig or receive timeout, send DRQ. In DMA0 mode, if DMA_PTE_RX = 1 and FIFO is on, when RFL is more than trig, send DRQ. In other case, once the receive data is valid, send DRQ.
5	R/W	0x0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0x0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/WAC	0x0	CHANGE_UPDATE After the user uses HALT[1] to change the baud rate or LCR configuration, write 1 to update the configuration and wait this bit self clear to 0 to finish update process. Writing 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0x0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration and baud rate register (DLH and DLL) when the UART is busy. 1: Enable change when busy
0	R/W	0x0	HALT_TX

			Halt TX This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled If FIFOs are not enabled, the setting has no effect on operation.

12.2.6.18. **UART DBG DLL Register(Default Value: 0x0000_0000)**

Offset: 0x00B0			**Register Name: UART_DBG_DLL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLL

12.2.6.19. **UART DBG DLH Register(Default Value: 0x0000_0000)**

Offset: 0x00B4			**Register Name: UART_DBG_DLH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLH

12.2.6.20. **UART RS485 Control and Status Register(Default Value: 0x0000_0000)**

Offset: 0x00C0			**Register Name: UART_485_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	AAD_ADDR_F In AAD mode, when UART receives an address byte and the byte is the same as RS485_ADDR_MATCH, this bit will be set to 1.If RS485 interrupt is enabled, the RS485 interrupt will arrive. Write 1 to clear this bit and reset the RS485 interrupt.
5	R/W1C	0x0	RS485_ADDR_DET_F This is a flag of the detecting of address bytes. When UART receives an address byte, this bit will be set to 1.If the RS485 Interrupt is enabled, the RS485 interrupt will arrive. 1:An address byte is detected 0:No address byte is detected Write 1 to clear this bit and reset the RS485 interrupt.
4	/	/	/
3	R/W	0x0	RX_BF_ADDR In NMM mode, If setting this bit to 1, UART will receive all the bytes into FIFO before receiving an address byte. If setting to 0, it will not. 1:Receive 0:Not Receive
2	R/W	0x0	RX_AF_ADDR In NMM mode, if setting this bit to 1, UART will receive all the bytes into FIFO after receiving an address byte. If setting to 0, it will not. 1:Receive

			0:Not Receive
1:0	R/W	0x0	RS485_SLAVE_MODE_SEL RS485 Slave Mode 00: Normal Multidrop Operation(NMM) 01: Auto Address Detection Operation(AAD) 10: Reserved 11: Reserved

12.2.6.21. **UART RS485 Address Match Register(Default Value: 0x0000_0000)**

Offset: 0x00C4			**Register Name: RS485_ADDR_MATCH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	ADDR_MATCH The matching address uses in AAD mode. It is only available for AAD.

12.2.6.22. **UART RS485 Bus Idle Check Register(Default Value: 0x0000_0000)**

Offset: 0x00C8			**Register Name: BUS_IDLE_CHK**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	BUS_IDLE_CHK_EN 0: Disable bus idle check function 1: Enable bus idle check function
6	R	0x0	BUS_STATUS The Flag of Bus Status 0:Idle 1:Busy
5:0	R	0x0	ADJ_TIME Bus Idle Time The unit is 8*16*Tclk.

12.2.6.23. **UART TX Delay Register(Default Value: 0x0000_0000)**

Offset: 0x00CC			**Register Name: TX_DLY**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLY The delay time between the last stop bit and the next start bit. The unit is 16*Tclk. It is used to control the space between two bytes in TX.

12.3. RSB

12.3.1. Overview

The RSB(reduced serial bus) Host Controller is designed to communicate with RSB Device using two push-pull wires. It supports a simplified two wire protocol on a push-pull bus. The transfer speed can be up to 20MHz and the performance will be improved much. The RSB bus protocol is designed and implemented by the Allwinner Technology. Allwinner technology has the final interpretation of the IP.

The RSB has the following features:

- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0.
- Speed up to 20MHz with ultra low power
- Push-Pull bus
- Supports host mode
- Programmable output delay of CD signal
- Parity check for address and data transmission
- Supports multi-devices

12.3.2. Block Diagram

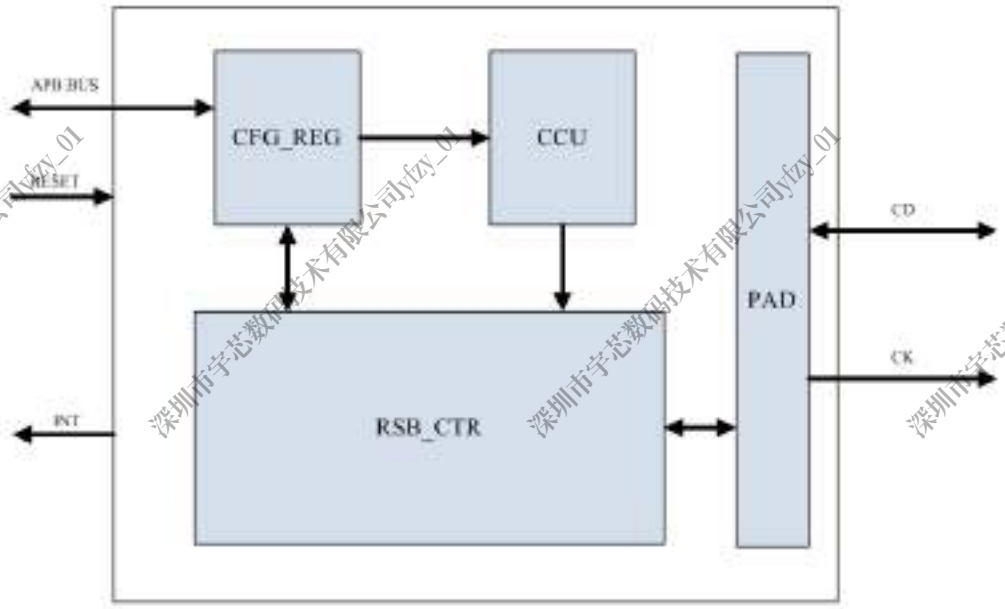


Figure 12-16. RSB Block Diagram

RESET: Module reset signal

INT: Module output interrupt signal

CFG_REG: Module configuration register

RSB_CTR: Packet encoding/decoding

CCU: Module clock controller unit

12.4. SPI

12.4.1. Overview

The SPI is a full-duplex, synchronous, serial communication interface which allows rapid data communication with software interrupts. The SPI controller contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at master mode and slave mode.

The SPI has the following features:

- Full-duplex synchronous serial interface
- 5 clock sources
- Master/slave configurable
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Supports Mode0, Mode1, Mode2 and Mode3
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 0 bit to 32 bits
- Supports Standard SPI,Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI

12.4.2. Block Diagram

Figure 12-17 shows a block diagram of the SPI.

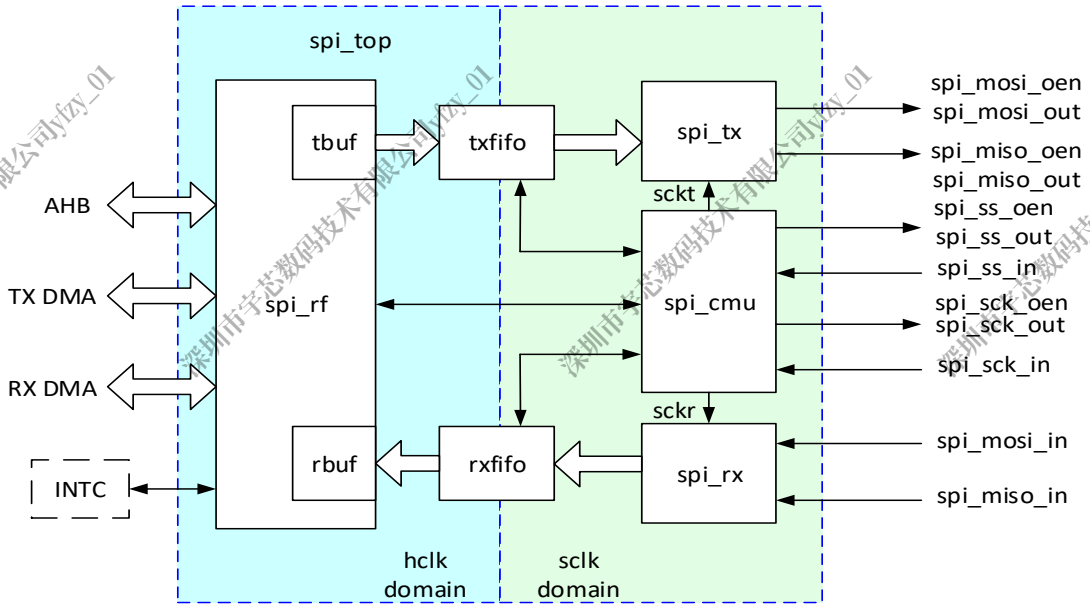


Figure 12-17. SPI Block Diagram

The SPI comprises with:

spi_rf: Responsible for implementing the internal register, interrupt and DMA Request.

spi_tbuf: The data length transmitted from AHB to txfifo is converted into 8bits,then the data is written into the rxfifo.

spi_rbuf: The block is used as converted the rxfifo data into read data length of AHB.

txfifo, rxfifo: For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the txfifo; data received from the external serial device into SPI is pushed into the rxfifo.

spi_cmu: Responsible for implementing SPI bus clock, chip select, internal sample and the generation of transfer clock.

spi_tx: Responsible for implementing SPI data transfer ,the interface of the internal txfifo and status register.
spi_rx: Responsible for implementing SPI data receive, the interface of the internal rxfifo and status register.

12.4.3. Operations and Functional Descriptions

12.4.3.1. External Signals

Table 12-8 describes the external signals of SPI. MOSI and MISO are bidirectional I/O, when SPI is configured as master device, CLK and CS are output pin; when SPI is configurable as slave device, CLK and CS are input pin. The unused SPI ports are used as General Purpose I/O ports.

Table 12-8. SPI External Signals

Signal	Description	Type
SPI0_CS0	SPI0 chip select signal0, low active	I/O
SPI0_CS1	SPI0 chip select signal1, low active	I/O
SPI0_CLK	SPI0 clock signal	I/O
SPI0_MOSI	SPI0 master data out, slave data in	I/O
SPI0_MISO	SPI0 master data in, slave data out	I/O
SPI0_WP	Write protection and active low, or serial data input and output for quad input or quad output	I/O
SPI0_HOLD	The HOLD pin is used to temporarily pause serial communication without deselecting or resetting the device. While the HOLD pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, or serial data input and output for quad input or quad output	I/O
SPI1_CS0	SPI1 chip select signal0, low active	I/O
SPI1_CS1	SPI1 chip select signal1, low active	I/O
SPI1_CLK	SPI1 clock signal	I/O
SPI1_MOSI	SPI1 master data out, slave data in	I/O
SPI1_MISO	SPI1 master data in, slave data out	I/O
SPI2_CS0	SPI2 chip select signal0, low active	I/O
SPI2_CLK	SPI2 clock signal	I/O
SPI2_MOSI	SPI2 master data out, slave data in	I/O
SPI2_MISO	SPI2 master data in, slave data out	I/O
SPI3_CS0	SPI3 chip select signal0, low active	I/O
SPI3_CLK	SPI3 clock signal	I/O
SPI3_MOSI	SPI3 master data out, slave data in	I/O
SPI3_MISO	SPI3 master data in, slave data out	I/O

12.4.3.2. Clock Sources

Each SPI controller gets five different clocks, users can select one of them to make SPI clock source. Table 12-9 describes the clock sources for SPI.

Table 12-9. SPI Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH0(2X)	Peripheral Clock, default value is 1200MHz
PLL_PERIPH1(2X)	Peripheral Clock, default value is 1200MHz

12.4.3.3. **Typical Application**

Figure 12-18 shows the application block diagram when the SPI master device is connected to a slave device.

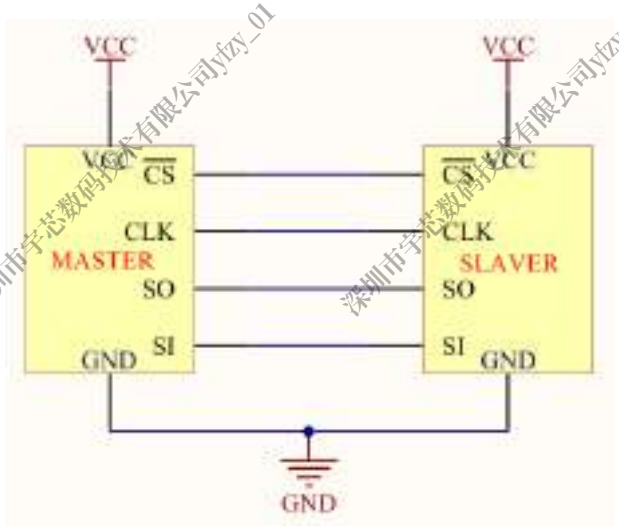


Figure 12-18. SPI Application Block Diagram

12.4.3.4. **SPI Transmit Format**

The SPI supports 4 different formats for data transfer. Software can select one of the four modes in which the SPI works by setting the bit1(Polarity) and bit0(Phase) of **SPI Transfer Control Register**. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four modes are listed in Table 12-10.

Table 12-10. SPI Transmit Format

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample

2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

Figure 12-19 and Figure 12-20 describe four waveforms for SPI_SCLK.

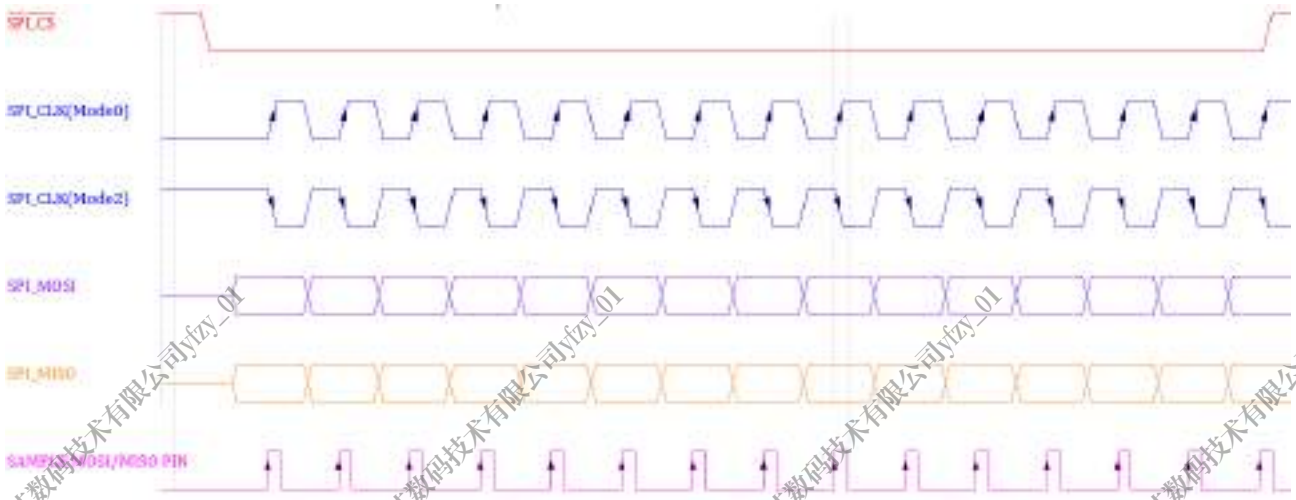


Figure 12-19. SPI Phase 0 Timing Diagram

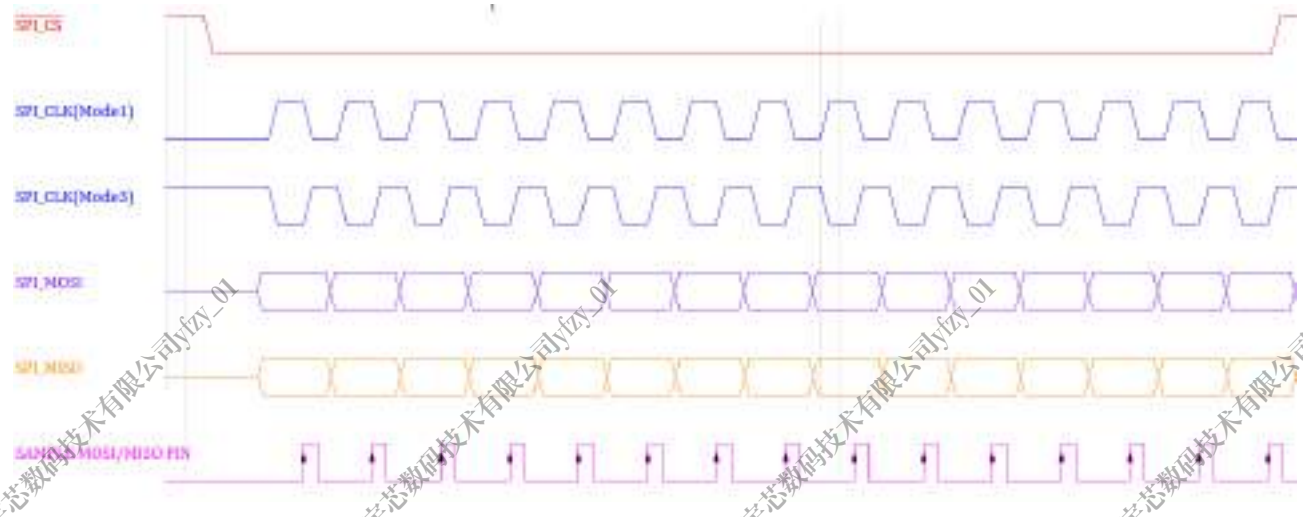


Figure 12-20. SPI Phase 1 Timing Diagram

12.4.3.5. **SPI Master and Slave Mode**

The SPI controller can be configured to a master or slave device. Master mode is selected by setting the **MODE** bit in the **SPI Global Control Register;** slave mode is selected by clearing the the **MODE** bit in the **SPI Global Control Register**.

In master mode, SPI_CLK is generated and transmitted to external device, and data from the TX FIFO is transmitted on the MOSI pin, the data from slave is received on the MISO pin and sent to RX FIFO. Chip Select(SPI_SS) is active low signal. SPI_SS must be set low before data are transmitted or received. SPI_SS can be selected SPI auto control or software manual control. When using auto control, **SS_OWNER**(the bit 6 in the **SPI Transfer Control Register**) must be cleared(default value is 0);when using manual control, **SS_OWNER** must be set, Chip Select level is controlled by **SS_LEVEL** bit(the bit 7 in the **SPI Transfer Control Register**).

In slave mode, after software selects the **MODE** bit to '0',it waits for master initiate a transaction. When the master

assertes SPI_SS and SPI_CLK is transmitted to the slave, the slave data is transmitted from TX FIFO on MISO pin and data from MOSI pin is received in RX FIFO.

12.4.3.6. **SPI 3-Wire Mode**

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and selected when the **Work Mode Select(bit[1:0])** is equal to 0x2 in the **SPI Bit-Aligned Transfer Configure Register**. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes this mode.

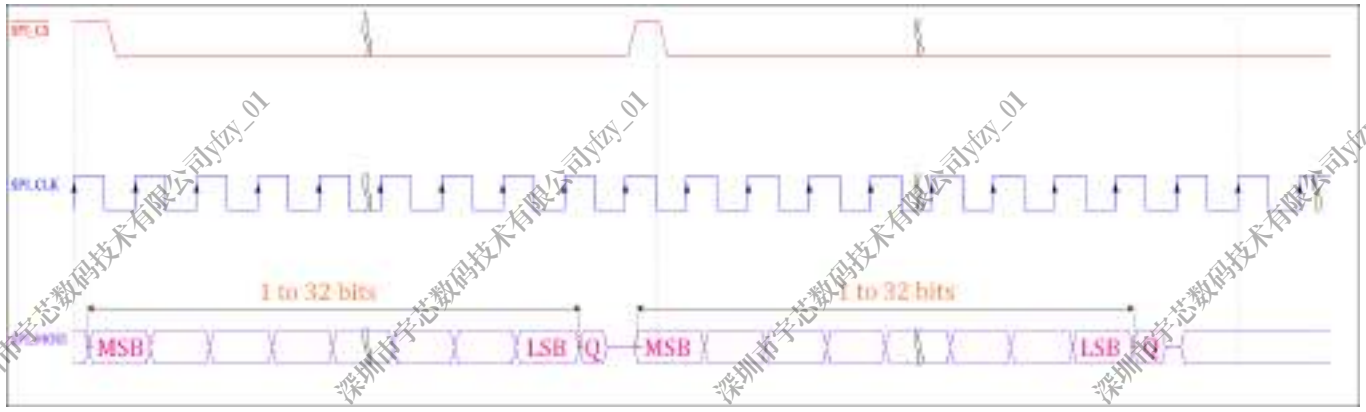


Figure 12-21. SPI 3-Wire Mode

12.4.3.7. **SPI Dual Read Mode**

The dual read mode(SPI x2) is selected when the **DRM**(bit28) is set in the **SPI Master Burst Control Counter Register**. Using the dual mode allows data to be transferred to or from the device at two times the rate of standard single mode SPI devices, data can be read at fast speed using two data bits(MOSI and MISO) at a time. The following figure describes the Dual Input/Dual Output SPI(Figure 12-22) and the Dual IO SPI(Figure 12-23).

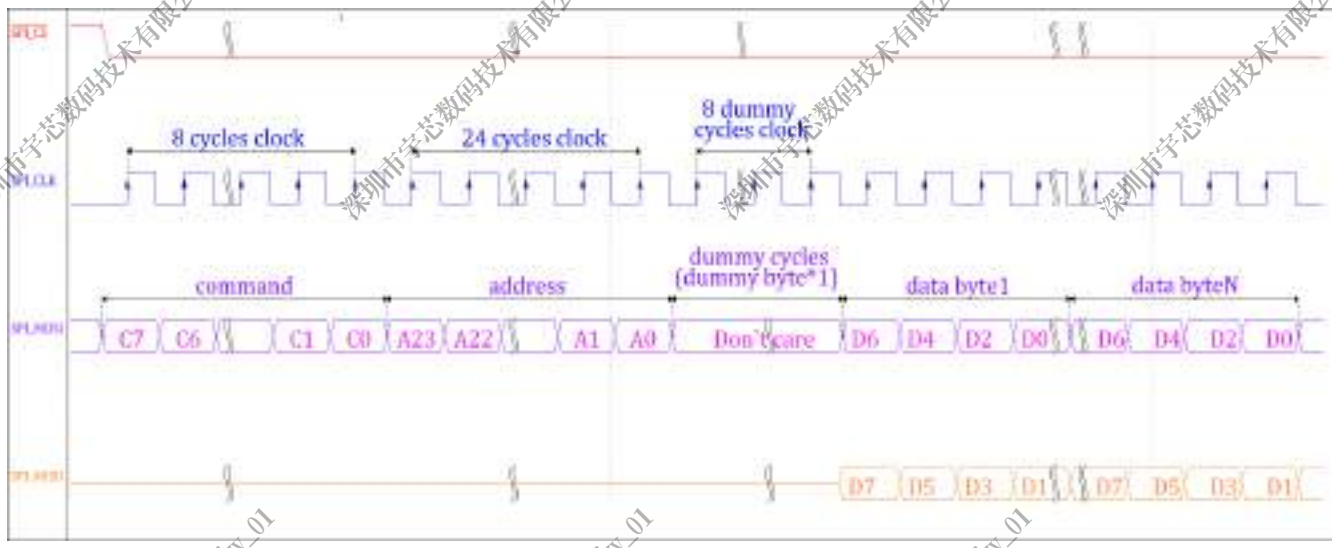


Figure 12-22. SPI Dual Read Mode

In the dual input/dual output SPI, the command, address, and the dummy bytes outputs in unit of a single bit in serial mode through SPI_MOSI line, only the data bytes are output(write) and input(read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

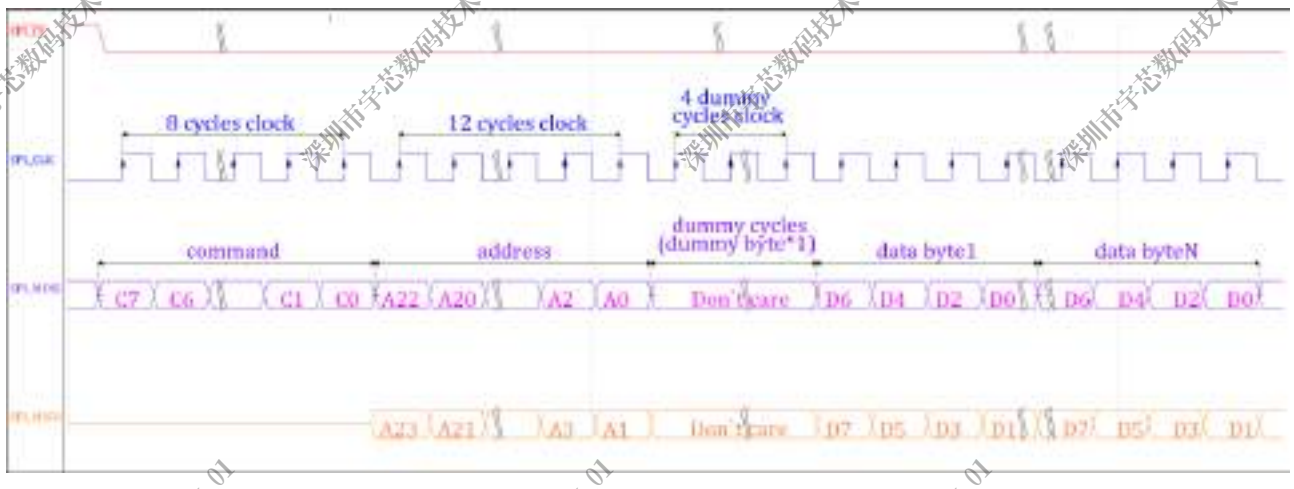


Figure 12-23. SPI Dual IO Mode

In the dual IO SPI, only the command bytes are output in unit of a single bit in serial mode through SPI_MOSI line. The address bytes and the dummy bytes are output in unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes are output(write) and input(read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

12.4.3.8. **SPI Quad Mode**

The quad read mode(SPI x4) is selected when the **Quad_EN**(bit29) is set in the **SPI Master Burst Control Counter Register**. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, data can be read at fast speed using four data bits(MOSI, MISO, IO2(WP#)and IO3(HOLD#)) at the same time. The following figure describes the Quad Input/Quad Output SPI.

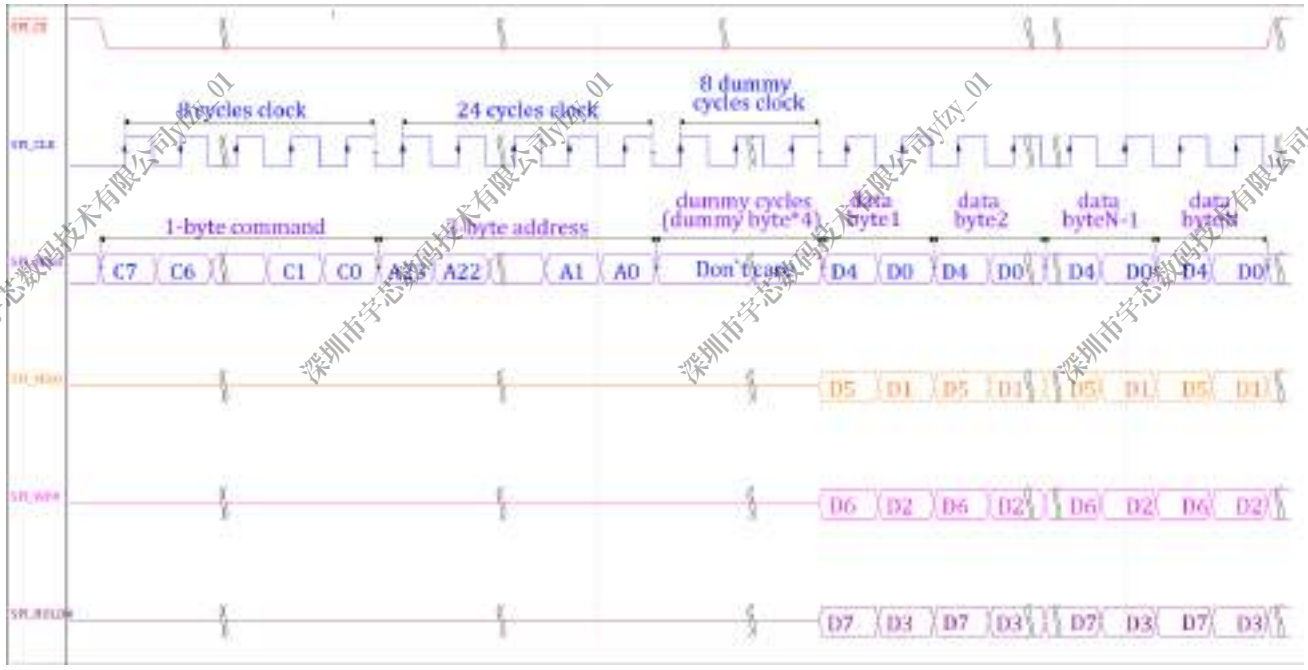


Figure 12-24. SPI Quad Read Mode

In the quad input/quad output SPI, the command, address, and the dummy bytes are output in unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes are output(write) and input(read) in unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP# and SPI_HOLD#.

12.4.4. Programming Guidelines

12.4.4.1. CPU or DMA Operation

The SPI transfers serial data between the processor and external device. CPU and DMA are the two main operational modes for SPI. For each SPI, data is simultaneously transmitted(shifted out serially) and received (shifted in serially).SPI has 2 channels, TX channel and RX channel. TX channel has the path from TX FIFO to external device. RX channel has the path from external device to RX FIFO.

Write Data: CPU or DMA must write data on the register SPI_TXD, data on the register are automatically moved to TX FIFO.

Read Data: To Read data from RX FIFO,CPU or DMA must access the register SPI_RXD and data are automatically sent to the register SPI_RXD.

In CPU or DMA mode, the SPI sends an completed interrupt(the TC bit in SPI Interrupt Status Register) to the processor at the end of each transfer.

12.4.4.2. Transmit/Receive Burst in Master Mode

In SPI master mode, the transmit and receive burst(byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmit bursts are written in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** The transmit bursts in single mode before automatically sending dummy burst are written in STC(bit[23:0]) of **SPI Master Burst Control Counter Register.** For dummy data, SPI controller can automatically sent before receive by writing DBC(bit[27:24]) in **SPI Master Burst Control Counter Register**. If users donot use SPI controller to sent dummy data automatically, then the dummy bursts are used as the transmit counters to write together in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** In master mode, the total burst numbers are written in MBC(bit[23:0]) of **SPI Master Burst Counter Register.** When all transmit burst and receive burst are transferred, SPI controller will send an completed interrupt, at the same time, SPI controller will clear DBC,MWTC and MBC.

12.4.4.3. SPI Sample Mode and Run Clock Configuration

The SPI controller runs at 3 kHz~100 MHz at its interface to external SPI devices. The internal SPI Clock should run at the same frequency as the outgoing clock in master mode. The SPI clock is selected different clock sources, SPI must configure different work mode. There are three work modes: normal sample mode, delay half cycle sample mode, delay one cycle sample mode. Delay half cycle sample mode is the default mode of SPI controller. When SPI runs at 40 MHz or below 40 MHz, SPI can work at normal sample mode or delay half cycle sample mode. When SPI runs over 75 MHz,Set the **SDC** bit in **SPI Transfer Control Register** to '1' to make the internal read sample point with a half cycle delay of SPI_CLK, which is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. The different configuration of SPI sample mode shows in Table 12-11.

Table 12-11. SPI Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24MHz
delay half cycle sample	0	0	<=40MHz
delay one cycle sample	0	1	>=75MHz

12.4.4.4. SPI Error Conditions

If any error conditions occur, hardware will set the corresponding status bits in the **SPI Interrupt Status Register** and stop the transfer. For the SPI controller, the following error scenarios can happen:

(1) TX_FIFO Underrun

TX_FIFO underrun happens when the CPU/DMA reads from TX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_UDF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the TF_UDF bit. To start a new transaction, software has to reset the fifo by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(2) TX_FIFO Overflow

TX_FIFO overflow happens when the CPU/DMA writes into the TX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_OVF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the TF_OVF bit. To start a new transaction, software has to reset the fifo by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(3) RX_FIFO Underrun

RX_FIFO underrun happens when the CPU/DMA reads from RX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_UDF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the RF_UDF bit. To start a new transaction, software has to reset the fifo by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(4) RX_FIFO Overflow

RX_FIFO overflow happens when the CPU/DMA writes into the RX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_OVF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the RF_OVF bit. To start a new transaction, software has to reset the fifo by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

12.4.5. Register List

Module Name	Base Address
SPI0	0x05010000
SPI1	0x05011000
SPI2	0x05012000
SPI3	0x05013000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control Register
/	0x000C	/
SPI_IER	0x0010	SPI Interrupt Control Register
SPI_ISR	0x0014	SPI Interrupt Status Register
SPI_FCR	0x0018	SPI FIFO Control Register
SPI_FSR	0x001C	SPI FIFO Status Register
SPI_WCR	0x0020	SPI Wait Clock Counter Register

SPI_CCR	0x0024	SPI Clock Rate Control Register
/	0x0028	/
/	0x002C	/
SPI_MBC	0x0030	SPI Burst Counter Register
SPI_MTC	0x0034	SPI Transmit Counter Register
SPI_BCC	0x0038	SPI Burst Control Register
SPI_BATCR	0x003C	SPI Bit-Aligned Transfer Configure Register
SPI_3W_CCR	0x0040	SPI 3Wire Clock Configuration Register
SPI_TBR	0x0044	SPI TX Bit Register
SPI_RBR	0x0048	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data Register
SPI_RXD	0x0300	SPI RX Data Register

12.4.6. Register Description

12.4.6.1. SPI Global Control Register(Default Value: 0x0000_0080)

Offset:0x0004			Register Name: SPI_GCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	SRST Soft reset Writing '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes Writing '0' has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1: Stop transmit data when RXFIFO full 0: Normal operation, ignore RXFIFO status Cannot be written when XCH=1
6:2	/	/	/
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode Cannot be written when XCH=1
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable After transforming from bit_mode to byte_mode, it must enable the SPI module again.

12.4.6.2. **SPI Transfer Control Register(Default Value: 0x0000_0087)**

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Writing “1” to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Writing “1” to SRST will also clear this bit. Writing ‘0’ to this bit has no effect. Cannot be written when XCH=1.
30:15	/	/	/
14	R/W	0x0	SDDM Sending Data Delay Mode 0:Normal sending 1:Delay sending Set the bit to"1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual IO mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 0: Delay sample mode 1: Normal sample mode In normal sample mode, SPI master samples the data at the correct edge for each SPI mode; In delay sample mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first Cannot be written when XCH=1.
11	R/W	0x0	SDC Master Sample Data Control Set this bit to ‘1’ to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point Cannot be written when XCH=1.
10	R/W	0x0	RPSM Rapids Mode Select Select rapid mode for high speed write.

			0: Normal write mode 1: Rapid write mode Cannot be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Cannot be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts. 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. Cannot be written when XCH=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high Cannot be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software Cannot be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices. 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Cannot be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Cannot be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle)

			1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Cannot be written when XCH=1.

12.4.6.3. **SPI Interrupt Control Register(Default Value: 0x0000_0000)**

Offset: 0x0010			**Register Name: SPI_IER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip select signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN

			TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

12.4.6.4. **SPI Interrupt Status Register(Default Value: 0x0000_0032)**

Offset: 0x0014			**Register Name: SPI_ISR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer completed
11	R/W1C	0x0	TF_UDF TXFIFO Underrun This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it.

			0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available 1: RXFIFO is overflowed
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. TX_WL is the water level of RXFIFO.
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty . Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY

			RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. RX_WL is the water level of RXFIFO.

12.4.6.5. **SPI FIFO Control Register(Default Value: 0x0040_0001)**

Offset: 0x0018			**Register Name: SPI_FCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Writing ‘1’ to this bit will reset the control portion of the TX FIFO and auto clear to ‘0’ when completing reset operation, writing to ‘0’ has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: Disable 1: Enable In normal mode, TX FIFO can only be read by SPI controller, writing ‘1’ to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, donot set in normal operation and donot set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_ DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Writing ‘1’ to this bit will reset the control portion of the receiver FIFO, and auto clear to ‘0’ when completing reset operation, writing ‘0’ to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, RX FIFO can only be written by SPI controller, writing ‘1’ to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, donot set in normal operation and donot set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_ DRQ_EN RX FIFO DMA Request Enable

			0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

12.4.6.6. **SPI FIFO Status Register(Default Value: 0x0000_0000)**

Offset: 0x001C			**Register Name: SPI_FSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO … 64: 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO … 64: 64 bytes in RX FIFO other: Reserved

12.4.6.7. **SPI Wait Clock Register(Default Value: 0x0000_0000)**

Offset: 0x0020			**Register Name: SPI_WCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	SWC

			Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. Cannot be written when XCH=1.
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted Cannot be written when XCH=1.

12.4.6.8. **SPI Clock Control Register(Default Value: 0x0000_0002)**

Offset: 0x0024			**Register Name: SPI_CCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2 Cannot be written when XCH=1.
11:8	R/W	0x0	CDR1_M Clock Divide Rate 1 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2^CDR1_M). Cannot be written when XCH=1.
7:0	R/W	0x2	CDR2_N Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR2_N + 1)). Cannot be written when XCH=1.

12.4.6.9. **SPI Master Burst Counter Register(Default Value: 0x0000_0000)**

Offset: 0x0030			**Register Name: SPI_MBC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number.

			0: 0 burst 1: 1 burst … N: N bursts Total transfer data, include the TXD, RXD and dummy burst. Cannot be written when XCH=1.

12.4.6.10. **SPI Master Transmit Counter Register(Default Value: 0x0000_0000)**

Offset: 0x0034			**Register Name: SPI_MTC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.

12.4.6.11. **SPI Master Burst Control Counter Register(Default Value: 0x0000_0000)**

Offset: 0x0038			**Register Name: SPI_BCC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable Quad mode includes Quad-Input and Quad-Output. Cannot be written when XCH=1.
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode Cannot be written when XCH=1; It is only valid when Quad_Mode_EN=0.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data does not care by the device.

			0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1

12.4.6.12. **SPI Bit-Aligned Transfer Configure Register(Default Value: 0x0000_00A0)**

Offset: 0x0040			**Register Name: SPI_BATC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start to transfer the serial bits frame, it is only valid when ***Work Mode Select==0x10/0x11.*** 0: Idle 1: Initiates transfer. Writing "1" to this bit will start to transfer serial bits frame(the value comes from the ***SPI TX Bit Register*** or ***SPI RX Bit Register***), and will auto clear after the bursts transfer completely. Writing '0' to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 1: Standard Sample Mode 0: Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in ***SPI TX Bit Register****(or* ***SPI RX Bit Register****)* has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed

			It is only valid when ***Work Mode Select==0x10/0x11.***
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable It is only valid when ***Work Mode Select==0x10/0x11.***
23:22	/	/	/
21:16	R/W	0x00	Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit … 100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and cannot be written when TCE=1.
15:14	/	/	/
13:8	R/W	0x00	Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit … 100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and cannot be written when TCE=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually , set this bit to '1' or '0' to control the level of SS signal. 0: Set SS to low 1: Set SS to high It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.

4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted It is only valid when ***Work Mode Select= =0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
1:0	R/W	0x0	Work Mode Select 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserved 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

12.4.6.13. **SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)**

Offset: 0x0044			**Register Name: SPI_BA_CCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)). This register is only valid when ***Work Mode Select==0x10/0x11***.

12.4.6.14. **SPI TX Bit Register(Default Value: 0x0000_0000)**

Offset: 0x0048			**Register Name: SPI_TBR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. In the process of transmission, the LSB is transmitted first. This register is only valid when ***Work Mode Select==0x10/0x11***.

12.4.6.15. **SPI RX Bit Register(Default Value: 0x0000_0000)**

Offset: 0x004C			**Register Name: SPI_RBR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VRB

			The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first. This register is only valid when ***Work Mode Select==0x10/0x11***.

12.4.6.16. **SPI Normal DMA Mode Control Register(Default Value: 0x0000_00E5)**

Offset: 0x0088			**Register Name: NDFC_NDMA_MODE_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x11	00:dma_active is low 01:dma_active is high 10:dma_active is controlled by dma_request(DRQ) 11:dma_active is controlled by controller
5	R/W	0x1	0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	Delay Cycles The counts of hold cycles from DMA last signal high to dma_active high

12.4.6.17. **SPI TX Data Register(Default Value: 0x0000_0000)**

Offset: 0x0200			**Register Name: SPI_TXD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increased by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **NOTE** **This address is writable-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.**

12.4.6.18. **SPI RX Data Register(Default Value: 0x0000_0000)**

Offset: 0x0300			**Register Name: SPI_RXD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RDATA Receive Data

			This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decreased by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4.  **NOTE** **This address is readable-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

12.5. USB2.0 OTG

12.5.1. Overview

The USB2.0 OTG is a dual-role device controller, which supports both device and host functions which can also be configured as a Host-only or Device-only controller, fully compliant with the USB2.0 Specification. It can support high-speed (HS, 480 Mbit/s), full-speed (FS, 12 Mbit/s), and low-speed (LS, 1.5 Mbit/s) transfers in Host mode. It can support high-speed (HS, 480 Mbit/s), and full-speed (FS, 12 Mbit/s) in Device mode. Standard USB transceiver can be used through its UTMI+PHY Level3 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. For saving CPU bandwidth, USB-OTG DMA interface can support external DMA controller to take care of the data transfer between the memory and USB-OTG FIFO. The USB-OTG core also supports USB power saving functions.

The USB2.0 OTG has the following features:

- Complies with USB2.0 Specification
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s) in Host mode
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in Device mode
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports bi-directional endpoint0 for Control transfer
- Supports up to 8 User-Configurable Endpoints for Bulk, Isochronousl and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4)
- Supports up to (4KB+64Bytes) FIFO for EPs (including EP0)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Includes interface to an external Normal DMA controller for every EPs

12.5.2. Block Diagram

Figure 12-25 shows the block diagram of USB2.0 OTG Controller.

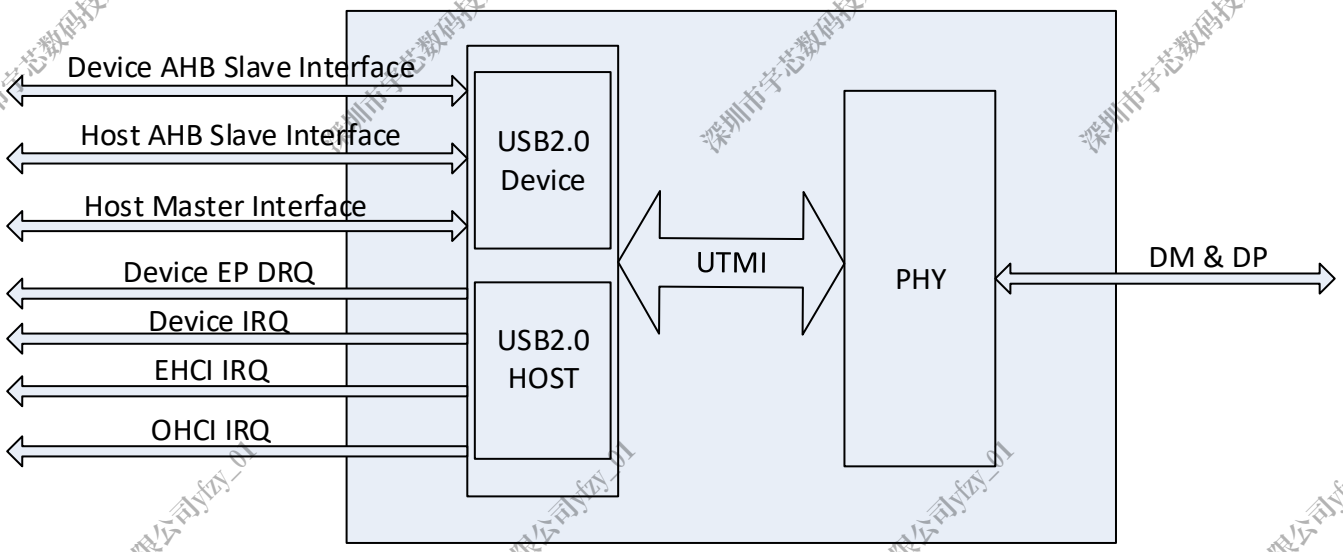


Figure 12-25. USB2.0 OTG Controller Block Diagram

12.5.3. External Signals

Table 12-12. USB2.0 OTG External Signals

Signal	Description	Type
USB0-DP	USB2.0 OTG differential signal postive	AI/O
USB0-DM	USB2.0 OTG differential signal negative	AI/O

12.6. One Wire Interface

12.6.1. Overview

The One Wire Interface implements the hardware protocol of the Master function of the 1-Wire protocol, which uses a single wire for communication between the Master (1-Wire controller) and the Slaves (1-Wire external compliant devices). The One Wire Interface is implemented as an open-drain output at the device level. Therefore, an external pull-up resistance is required and protocol use the return-to-1 mechanism (that is, after any command by any of the connected devices, the line is pulled to a logical high level).

The One Wire Interface can work at simple mode or standard mode at one time.

The One Wire Interface has the following features:

- Hardware implement of 1-Wire protocol
- Supports master function
- Supports simple mode and standard mode

12.6.2. Block Diagram

The block diagram of the One Wire Interface is shown below.

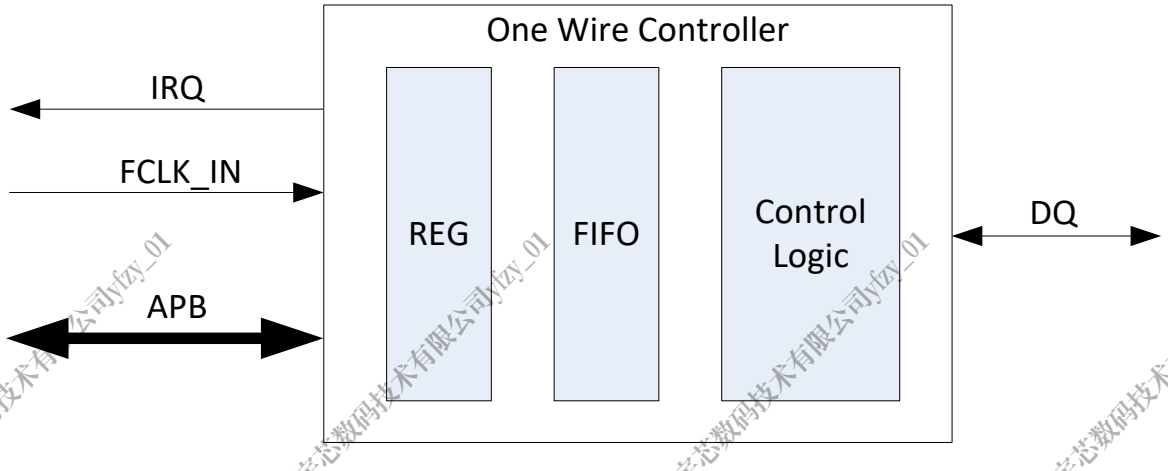


Figure 12-26. One Wire Interface Block Diagram

12.6.3. Operations and Functional Descriptions

12.6.3.1. External Signals

Table 12-13 describes the external signals of One Wire Interface.

Table 12-13. One Wire Interface External Signals

Signal Name	Description	Type
ONEWIRE	Data In/Out of One Wire Interface	I/O

12.6.3.2. Clock and Reset

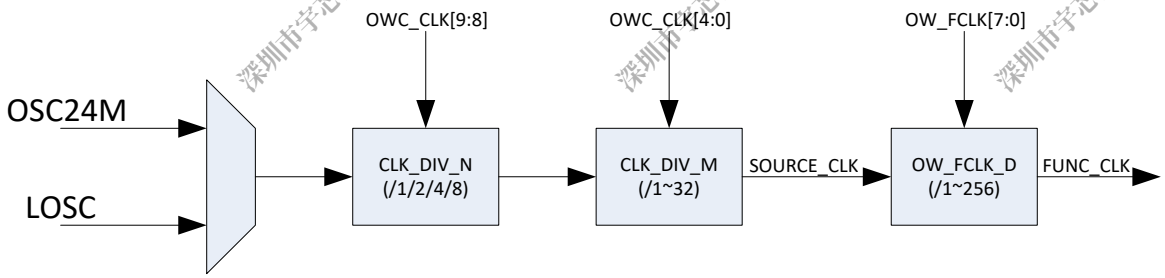


Figure 12-27. One Wire Interface Clock Description

12.6.3.3. Typical Application

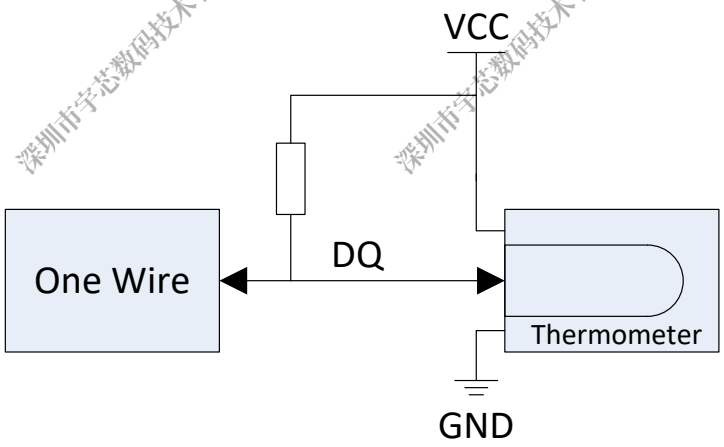


Figure 12-28. Typical Application

12.6.3.4. Function Implementation

12.6.3.4.1. Simple Mode

The bus of Simple Mode is a master-slave bus system using a simple one-wire, asynchronous, bi-directional, serial interface with a maximum bit-rate of about 5 Kbit/s.

It is a command-based protocol in which the host sends a command byte to the slave. The command directs the slave either to store the next eight bits of data received to a register specified by the command byte (Write command), or to output the eight bits of data from a register specified by the command byte (Read command). Command and data bytes consist of a stream of bits where the least-significant bit of a command or data byte is transmitted first. The first 7 bits of the command word are the register address and the last command bit transmitted is the read/write (R/W) bit. The following figure illustrates a typical read cycle.

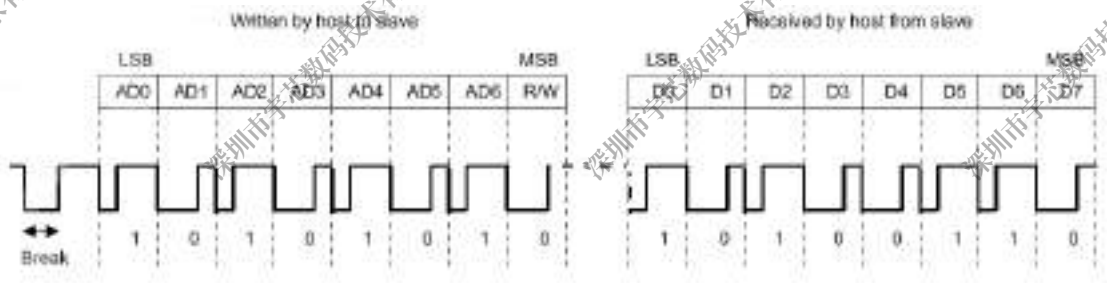


Figure 12-29. Typical Read Cycle

In the figure, the 1 of the R/W bit indicates a write command where the 0 indicates the read command.

In Simple mode, the slave can be reset by using the break pulse. If the host does not get an expected response from the slave or if the host needs to restart a communication before it is complete, the host can hold the line low and generate a break to reset the communication engine. The break timing is illustrated as follow.

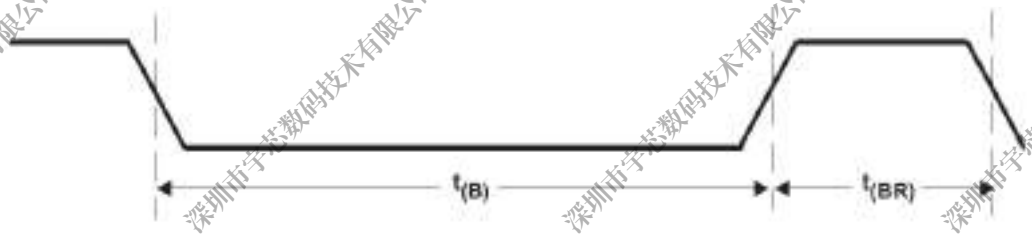


Figure 12-30. Break Timing

Table 12-14. Break Timing Parameters

Timing Parameter	For Device	Minimum	Maximum
t(B)	All	190us	
t(BR)	All	40us	

It is not required, but it is recommended to precede each communication with a break for the reliable communication.

After a successful break pulse (if have), the host and slave are ready for bit transmission. Each bit to transmit (either from the host to the slave or from the slave to the host) is preceded by a low-going edge on the line.

The host transmitted bit timing is shown in Figure 12-31.

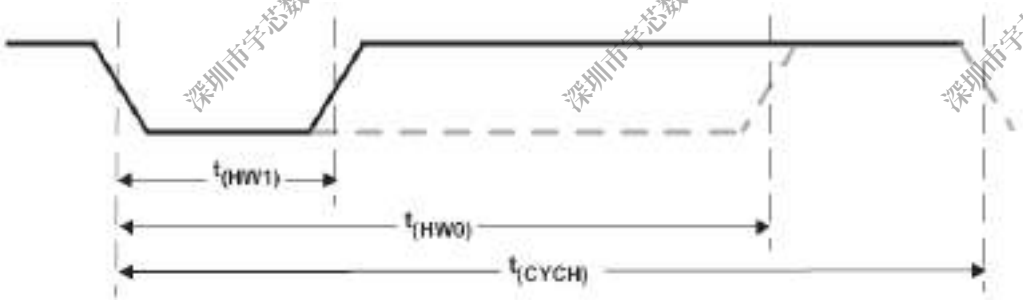


Figure 12-31. Host Bit Timing

And the slave transmitted bit timing is shown in Figure 12-32.

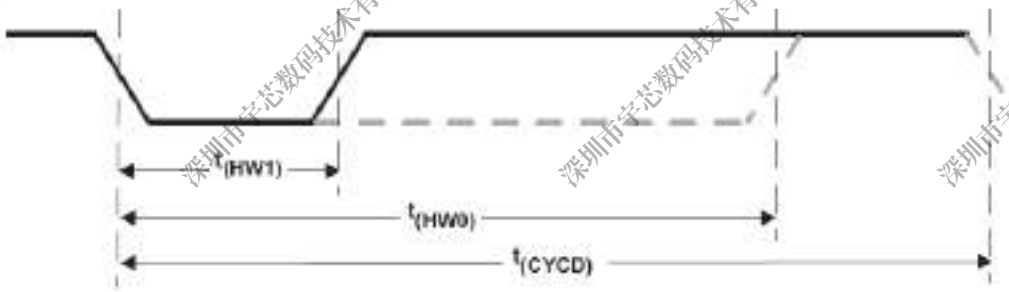


Figure 12-32. Slave Bit Timing

After the last bit of address is sent on a read cycle, the slave starts outputting the data after the specified response time, t(RSPS). The response time is measured from the fall time of the command R/W bit to the fall time of the first data bit returned by the slave and therefore includes the entire bit time for the R/W bit. Because the minimum response time equal to the minimum bit cycle time, this means that the first data bit may begin as soon as the command R/W bit time ends. The timing is shown as follows.

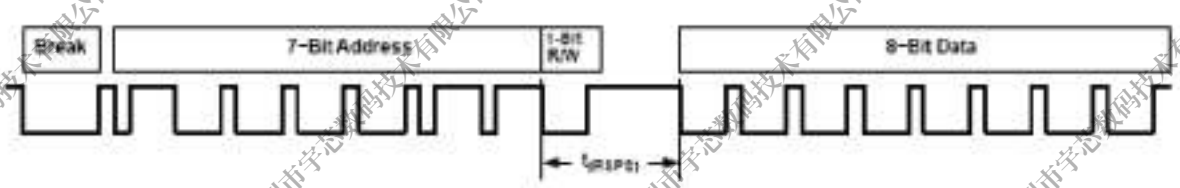


Figure 12-33. t(RSPS) Requirement

Table 12-15.Response Time Parameters

Timing Parameter	For Device	Minimum	Maximum
t(RSPS)	All	190us	320us

Also, to avoid short noise spike coupled onto the HDQ line, some filtering may be prudent.

12.6.3.4.2. Standard Mode

The Standard mode consists of 4 types of signaling on the data line, which are Initialization Sequence, Write Zero, Write One and Read Data.

The host first sends an initialization pulse and then waits for the slave to respond with a presence pulse before enabling any communication sequence. The initialization pulse and presence pulse are shown as follows.

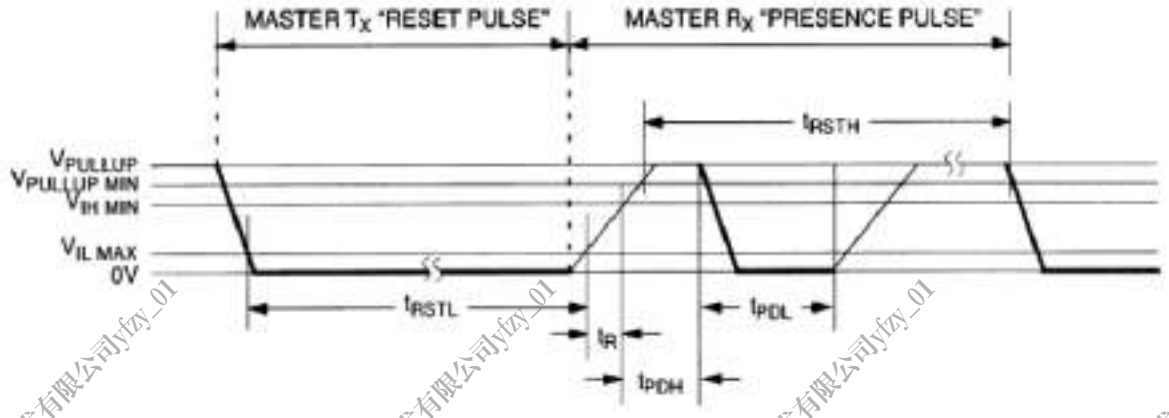


Figure 12-34. Initialization Pulse and Presence Pulse

Table 12-16. Initialization Pulse and Presence Pulse Timing Parameters

Timing Parameter	Minimum	Maximum
t(RSTL)	480us	
t(RSTH)	480us	
t(PDH)	15us	60us
t(PDL)	60us	240us

The other two types of signaling are Writing Zero and Writing One. The both write time slots must be a minimum of 60us in duration with a minimum of a 1us recovery time between individual write cycles. The slave device sample the data line in a window of 15us to 60us after the data line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs.

The Write Zero time slot is shown as follows.

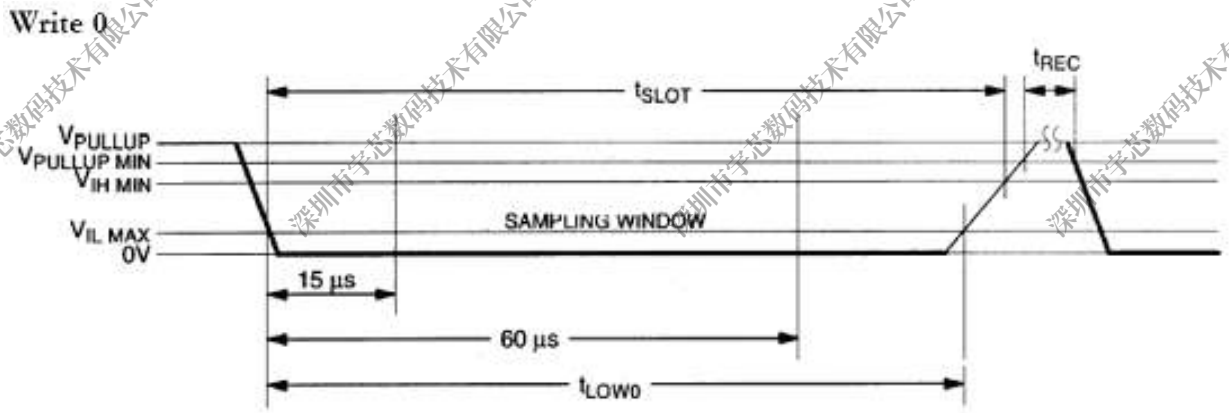


Figure 12-35. Write 0 Time Slot

Table 12-17. Write 0 Time Slot Timing Parameters

Timing Parameter	Minimum	Maximum
T(LOW0)	60us	t(SLOT)
t(SLOT)	T(LOW0)	120 us
t(REC)	1us	

When Write One occurs, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15us after the start of the write time slot. The Write One time slot is shown as follows.

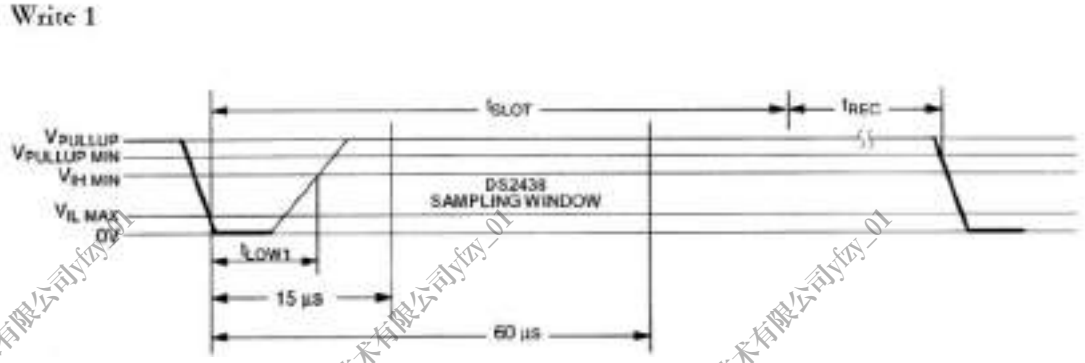


Figure 12-36. Write 1 Time Slot

Table 12-18. Write 1 Time Slot Timing Parameters

Timing Parameter	Minimum	Maximum
t(SLOT)	60us	120 us
t(LOW1)	1us	15us
t(REC)	1us	

The last signaling type is Read Data. A read time slot is initiated when the bus master pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 us; output data from the slave is then valid within the next 14 us maximum.

The bus master therefore must stop driving the data line low in order to read its state 15 us from the start of the read slot. All read time slots must be a minimum of 60us in duration with a minimum of a 1 us recovery time between individual read slots. The Read Data slot is shown as follows.

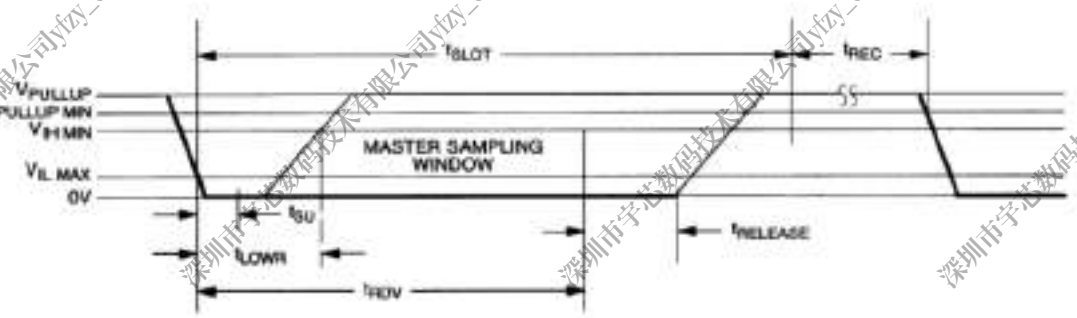


Figure 12-37. Read Data Slot

Table 12-19. Read Data Slot Timing Parameters

Timing Parameter	Minimum	Maximum
t(SU)		1us
t(LOWR)	1us	15us
t(RDV)	(= 15us)	
t(RELEASE)	0us	45us
t(SLOT)	60 us	120 us
t(REC)	1us	

Cyclic Redundancy Check (CRC) is used by One Wire devices to ensure data integrity. Two different CRC are commonly found in Standard Mode. There are one 8 bit CRC and one 16 bit CRC. CRC8 is used in the ROM section of all devices. CRC8 is also in some devices used to verify other data, like commands issued on the bus. CRC16 is used by some devices to check for errors on larger data sets.

12.6.4. Programming Guidelines

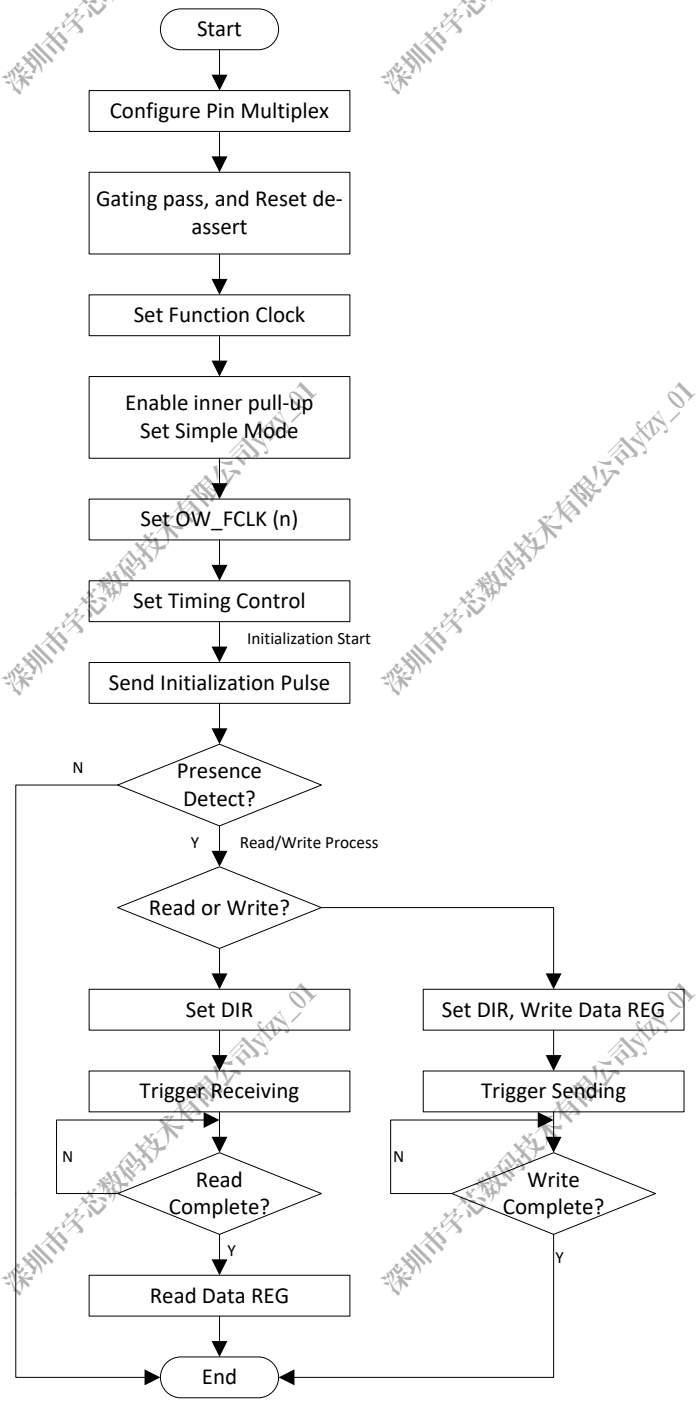


Figure 12-38. One Wire Interface Write/Read Process

12.6.5. Register List

Module Name	Base Address
R_OWC	0x07040400

Register Name	Offset	Description
OW_DATA	0x0000	One Wire Data Register

OW_CTL	0x0004	One Wire Control Register
OW_SMSC	0x0008	One Wire Standard Mode Special Control Register
OW_SMCRC	0x000C	One Wire Standard Mode CRC Register
OW_INT_STATUS	0x0010	One Wire Interrupt Status Register
OW_INT_MASK	0x0014	One Wire Interrupt Mask Register
OW_FCLK	0x0018	One Wire Function Clock Register
OW_LC	0x001C	One Wire Line Control Register
SM_WR_RD_TCTL	0x0020	Standard Mode Write Read Timing Control Register
SM_RST_PRESENCE_TCTL	0x0024	Standard Mode Reset Presence Timing Control Register
SP_WR_RD_TCTL	0x0028	Simple Mode Timing Control Register
SP_BR_TCTL	0x002C	Simple Mode Break Timing Control Register

12.6.6. Register Description

12.6.6.1. **One Wire Data Register(Default Value: 0x0000_0000)**

Offset: 0x0000			**Register Name: OW_DATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	SM_DATA These fields are for Simple Mode data send or receive in a one wire transmission. After this byte data transfer finishing, a transmission complete interrupt will generate.
15:8	/	/	/
7:0	R/W	0x0	OW_DATA Data byte for transmitting or received In Simple mode, these fields are for the command byte transmission. When GO bit is set (the INITIALIZATION/BREAK bit is not set at the same time), these fields will be sent as the address and command for a Simple Mode transfer. After the command byte transmission finished, the controller in Simple Mode will send next 8 bit data from SM_DATA when the DIR bit is 1 or receive one byte data to SM_DATA when the DIR bit is 0. In Standard Mode, if the INITIALIZATION/BREAK bit is not set, the controller samples/sends data to/from these fields determining by the DIR bit when the Go bit is set. When the ONE_WIRE_SINGLE_BIT is enabled, only the first bit of these fields is available.

12.6.6.2. **One Wire Control Register (Default Value: 0x0003_0000)**

Offset: 0x0004			**Register Name: OW_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	/	/	/

19:16	R/W	0x3	SAMPLE_TIME These fields determine the sample times in digital circuit.
15:10	/	/	/
9	R/W	0x0	INNER_PULL_UP_ENABLE When this bit is set, the inner pull up for one wire bus is determined by inner output (pull up is off when bus is drive 0) 0: Inner pull up is on 1: Inner pull up is off when bus is drive 0
8	R/W	0x0	AUTOIDLE Auto Idle 0: Module clock is free-running 1: Module clock is in power saving mode: the function clock is running only when module is accessed or inside logic is in function to process events.
7	/	/	/
6	R	0x0	PRESENCEDETECT Slave Presence Indicator This read-only flag is only used in Standard mode. The value of this field indicates whether there is Presence Pulse responding to the host initialization pulse. The flag is updated when the OW_INT_STATUS[0] Presence Detect Interrupt Flag is set.
5	R/W	0x0	STANDARD_MODE_SINGLE_BIT The single-bit mode is only supported for Standard mode. After the bit is transferred, Tx-complete or Rx-complete interrupt will generate for corresponding transfer operation. 0: Disabled 1: Enabled
4	R/W	0x0	Go Go Bit Write 1 to start the appropriate operation. If the INITIALIZATION/BREAK bit is set, the controller generates the initialization or break pulse. If the INITIALIZATION/BREAK bit is not set, the controller in Standard mode samples/sends data to/from the OW_DATA fields determining by the DIR bit, or controller in Simple mode begins a transfer sequence with the command byte in OW_DATA. Bit returns to 0 after the operation is complete.
3	R/W	0x0	INITIALIZATION/BREAK Initialization/Break Bit Write 1 to send initialization pulse for the Standard mode or break pulse for the Simple mode. The OW_DATA register will be flushed when initialization or the break situation is generating. Bit returns to 0 after pulse is sent. The pulse generates after the Go bit is set.
2	R/W	0x0	DIR Direction Bit In Standard mode, this field determines if next operation (byte operation or bit operation) is read or write.

			In Simple mode, this field determines if the current transfer sequence is read or write. 0 : Read 1: Write The operation starts after the Go bit is set.
1	R/W	0x0	MS Mode Selection Bit 0: Standard Mode 1: Simple Mode
0	R/W	0x0	GEN Global Enable This field is used to enable or disable the One Wire Controller. A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

12.6.6.3. **One Wire Standard Mode Special Control Register(Default Value: 0x0000_0000)**

Offset: 0x0008			**Register Name: OW_SMSC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:6	/	/	/
5	R/W	0x0	CRC_ERROR_STATUS These fields indicate the result of the CRC comparing. 0: CRC comparing right 1: CRC comparing wrong
4	/	/	/
3	R/W	0x0	MEM_CRC_COMPARE This field is only used in Standard mode. When this field is set, the controller will compare the value in the CRC_RECEV field with the data read from the CRC_CALC_INDICATE field, and then returns corresponding result in the CRC_ERROR_STATUS field and generates CRC finish interrupt. The CRC shift register and CRC_CALC_INDICATE field will be cleared to 0. This field will be automatically cleared when the CRC compare is finished.
2	R/W	0x0	CRC_16BIT_EN This field is only used in Standard mode. and is set to 1 to select 16-bit CRC, else the 8-bit CRC is selected. 0: CRC_8BIT_EN 1: CRC_16BIT_EN
1	R/W	0x0	WR_MEM_CRC_REQ This field is only used in One Wire mode. When this bit is set, the bit send to the device will be took into calculate the CRC value (CRC8 or CRC16). The calculation will stop when this bit is cleared. The value will be preserved in the corresponding CRC (CRC8 or CRC16) shift register then.
0	R/W	0x0	RD_MEM_CRC_REQ

			This field is only used in Standard Mode. When this bit is set, the bit received from the device will be took into calculate the CRC value (CRC8 or CRC16). The calculation will stop when this bit is cleared. The value will be preserved in the corresponding CRC (CRC8 or CRC16) shift register then.

12.6.6.4. **One Wire Standard Mode CRC Register(Default Value: 0x0000_0000)**

Offset: 0x000C			**Register Name: OW_SMCRC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	CRC_CALC_INDICATE This field indicates the CRC value calculated by the CRC shift register.
15:0	R/W	0x0	CRC_RECEV The data CRC value (CRC8 or CRC16) will be written to these fields by software for CRC comparing.

12.6.6.5. **One Wire Interrupt Status Register(Default Value: 0x0000_0000)**

Offset: 0x0010			**Register Name: OW_INT_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W1C	0x0	Deglitch Detected Interrupt Flag This flag indicates a deglitch in the bus. The controller looks for any glitch in the sample window for at least 1us. If the Deglitch Interrupt is enabled, an interrupt will issue when any deglitch occurs in the bus. The interrupt condition is cleared by writing “1” to this field.
4	R/W1C	0x0	CRC Comparing Complete Interrupt Flag This flag is used in Standard mode, and is used to indicate the CRC comparing has finished. The interrupt condition is cleared by writing “1” to this field.
3	R/W1C	0x0	Transmission Complete Interrupt Flag In Standard mode, the flag is set when a write operation of one byte or one bit in single-bit mode was completed. The interrupt is generated then. In Simple mode, the flag is set when a write operation of one byte was completed. The interrupt is also generated. The interrupt condition is cleared by writing “1” to this field.
2	R/W1C	0x0	Read Complete Interrupt Flag In Standard mode, the flag is set when a byte or a bit in single-bit mode has been successfully read. The interrupt is generated then. In Simple mode, the flag is set when a byte has been successfully read. The interrupt is also generated then. The interrupt condition is cleared by writing “1” to this field.
1	R/W1C	0x0	Time-out Interrupt Flag This flag is only used in Simple mode. The flag is set when two event happened. The one event is that after a read command initiated by the host,

			the slave did not pull the line low within the specified time (512 us). The other event is that another bit transfer does not begin after a specified time (512 us) from the pre-bit beginning. When the above situation occurs, the interrupt generates and the value of this field is set. The interrupt condition is cleared by writing “1” to this field.
0	R/W1C	0x0	Presence Detect Interrupt Flag In Standard mode, this interrupt status is set when the Initialization Pulse is completed. The interrupt is generated then and the PRESENCEDETECT bit is updated. In Simple mode, the flag is set when the successful completion of a break pulse. The interrupt is also generated then. The interrupt condition is cleared by writing “1” to this field.

12.6.6.6. **One Wire Interrupt Mask Register(Default Value: 0x0000_0000)**

Offset: 0x0014			**Register Name: OW_INT_MASK**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	Deglitch Detected Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	CRC Comparing Complete Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	Transmission Complete Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	Read Complete Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	Time-out Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	Presence Detect Interrupt Enable 0: Disable 1: Enable

12.6.6.7. **HDQ/One Wire Function Clock Register(Default Value: 0x0000_0000)**

Offset: 0x0018			**Register Name: OW_FCLK**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	OW_FCLK (n)

			n-MHz clock is needed to use as a time reference by the machine. Transitions between the states of the state machine as well as actions triggered at precise time deadlines are expressed using the n – MHz clock.
15:8	/	/	/
7:0	R/W	0x0	OW_FCLK_D OW_FCLK = SOURCE_CLK/OW_FCLK_D

12.6.6.8. **One Wire Line Control Register(Default Value: 0x0000_0004)**

Offset: 0x001C			**Register Name: OW_LC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x1	Current state of One Wire line 0: Low 1: High
1	R/W	0x0	One Wire line state control bit When the line control mode is enabled (bit [0] set), value of this bit decides the output level of the One Wire line. 0: Output low level 1: Output high level
0	R/W	0x0	One Wire line state control enable When this bit is set, the state of One Wire line is controlled by the value of bit [1]. 0: Disable line control mode 1: Enable line control mode

12.6.6.9. **Standard Mode Write Read Timing Control Register(Default Value: 0x213D_E0BC)**

Offset: 0x0020			**Register Name: OW_SMSC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:29	R/W	0x1	TSU Read Data Setup. In standard speed, range: t(SU) < 1 00: 0.5us 01: 1us 10: 2us 11: 4us
28	/	/	/
27:24	R/W	0x1	REC Recovery Time, t(recovery) = N us. In standard speed, range: 1us <= t(recovery)
23	/	/	/
22:18	R/W	0xf	TRDV Read data valid time, t(rdv) = N us. In standard speed, range: Exactly 15

17:11	R/W	0x3c	TLOW0 Write Zero time low, Tlow0 = N us. The range setting for TLOW0 is from 0x3c to 0x77. In standard mode, range:60<= t(low0) < t(tslot) <120
10:7	R/W	0x1	TLOW1 Write One time low, or TLOWR both are same. t(low1) = N us. The range setting for TLOW1 and TLOWR here is from 0x1 to 0xf. In standard speed, range:1 <= t(low1) < 15. t(lowR) = N owr clks. In standard speed, rang = 1 <= t(lowR) <15
6:0	R/W	0x3c	TSLOT Active time slot for write and read data, t(slot) = N us. The range setting for TSLOT is from 0x3c to 0x78. In standard mode, range:60 <= t(slot) <120

12.6.6.10. **Standard Mode Reset Presence Timing Control Register(Default Value: 0x3C3F_C1E0)**

Offset: 0x0024			**Register Name: SM_RST_PRESENCE_TCTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x3c	TPDL PRESENCE_DETECT_LOW t(pdl) = N us. The range setting for TPDL in these fields is from 0 to 0xf0. In standard speed, Range: 60 <= t(pdl) <240.
23:18	R/W	0xf	TPDH PRESENCE_DETECT_HIGH t(pdh) = N us. The range setting for TPDH in these fields is from 0xf to 0x3c. In standard speed, range: 15 <= t(pdh) < 60 .
17:9	R/W	0x1e0	TRSTL RESET_TIME_LOW t(rstl) = N us. The range setting for TRSTL in these fields is from 0 to 0xff. In standard speed, Range: 480 <= t(rstl) < infinity
8:0	R/W	0x1e0	TRSTH RESET_TIME_HIGH, t(rsth) = N us. The range setting for TRSTH in these fields is from 0 to 0xff. In standard speed, Range : 480 <= t(rsth) < infinity

12.6.6.11. **Simple Mode Write Read Timing Control Register(Default Value: 0x0A01_58BE)**

Offset: 0x0028			**Register Name: SP_WR_RD_TCTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	RD_SAMPLE_POINT When controller of the Simple Mode read, the default sample point is at the middle of the THW1 point and the THW0 point, named S(middle). When these fields are set, the corresponding new sample point will be determined.

0000	S(middle)		1000	S(middle)-30us
0001	S(middle)+5us		1001	S(middle)+40us
0010	S(middle)-5us		1010	S(middle)-40us
0011	S(middle)+10us		1011	S(middle)+50us
0100	S(middle)-10us		1100	S(middle)-50us
0101	S(middle)+20us		1101	S(middle)+60us

			0110 S(middle)-20us; 0111 S(middle)+30us; 1110 S(middle)-60us; 1111 reserve
27:22	R/W	0x28	THW1_INT t(HW1_INT) = N us. The range setting for THW1_INT in these fields is from 0 to 0x3f, which is the integer part of the THW1. In HDQ mode, Range: t(HW0) <= 50 us.
21:18	R/W	0x0	THW1_DEC THW1_DEC is the decimal part of the THW1. t(HW1_DEC) = N ow_clks. The value for the THW1 = THW1_INT + THW1_DEC.
17:10	R/W	0x56	THW0 t(HW0) = N us. The range setting for THW0 in these fields is from 0 to 0xff. In HDQ mode, Range: t(HW0) <= 145 us.
9:0	R/W	0xbe	TCYCH t(CYCH) = N us. The range setting for TCYCH in these fields is from 0 to 0x3ff. In HDQ mode, Rang: 190 us <= t(CYCH) <= infinity.

12.6.6.12. **Simple Mode Break Timing Control Register(Default Value: 0x00BE_0028)**

Offset: 0x002C			**Register Name: HDQ_ BR_TCTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0xbe	TB t(B) = N us. The range setting for TB in these fields is from 0 to 0x 3ff. In HDQ mode, Rang: 190 us <= t(B) <= infinity.
15:10	/	/	/
9:0	R/W	0x28	TBR t(BR) = N us. The range setting for TBR in these fields is from 0 to 0xff. In HDQ mode, Rang: 40 us <= t(BR) <= infinity.

12.7. Port Controller

12.7.1. Overview

The Port Controller can be configured with multi-functional input/output pins. All these ports can be configured as GPIO only if multiplexed functions not used. The total 8 group external PIO interrupt sources are supported and interrupt mode can be configured by software.

The Port Controller has the following features:

- 8 ports(PC,PD,PE,PF,PG,PH,PI,PL)
- Software control for each signal pin
- GPIO peripheral can produce interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Up to 118 interrupts
- Configurable interrupt edges
- IO withstand voltage mode: 1.8V/3.3V configurable

12.7.2. Block Diagram

The block diagram of port controller is shown in Figure 12-39.

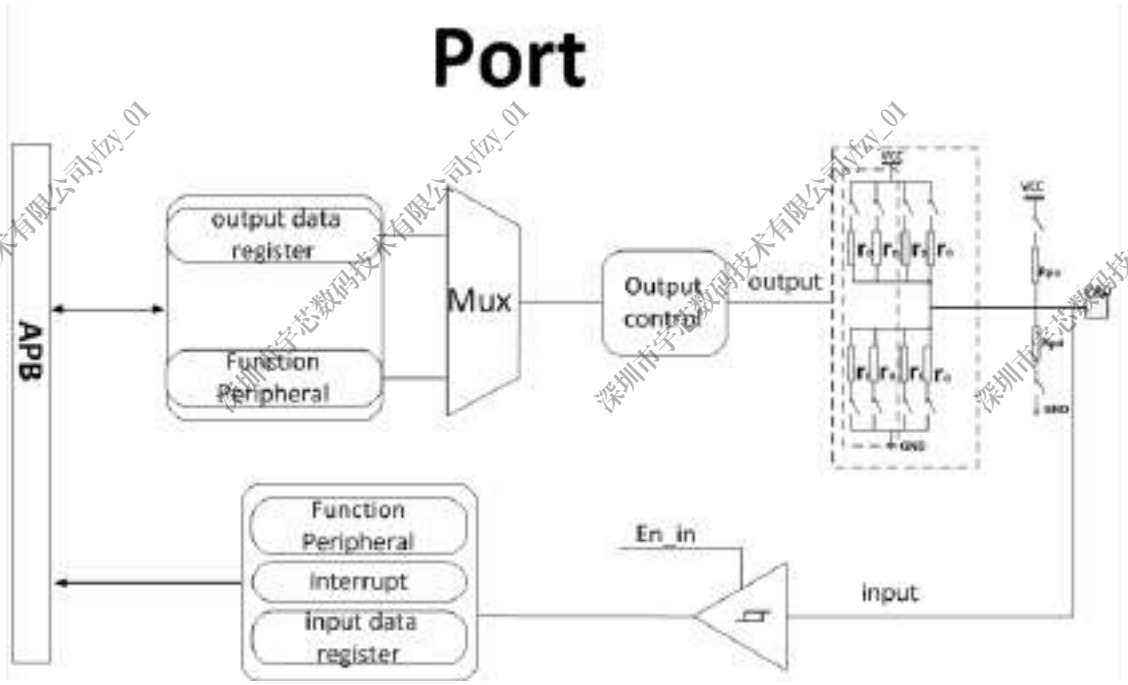


Figure 12-39. Port Controller Block Diagram

Port controller consists of digital part(GPIO, external interface) and IO analog part(output buffer, dual pull down, pad, etc). Digital part can select output interface by MUX switch; analog part can configure pull up/down, buffer strength. When executing GPIO read state, the port controller reads the current level of pin into internal register bus. When not executing GPIO read state, external pin and internal register bus is off-status, that is high-impedance.

12.7.3. Operations and Functional Descriptions

12.7.3.1. Multi-function Port Table

V536-H/V526 includes 118 multi-functional input/output port pins.There are 8 ports as listed below.

Table 12-20. Multi-function Port Table

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Power
PC	15	Schmitt	CMOS	NAND/SDC/SPI	1.8/3.3V
PD	23	Schmitt	CMOS	LCD/I2S/BT1120/PWM	1.8/3.3V
PE	22	Schmitt	CMOS	CSI/TWI/LCD/RGMII/SPI/UART/SYNC	1.8V/2.8V/ 3.3V
PF	7	Schmitt	CMOS	SDC/UART/JTAG	1.8V/3.3V
PG	14	Schmitt	CMOS	SDC/UART/AIF/I2S	1.8/3.3V
PH	16	Schmitt	CMOS	I2S/AIF/DMIC/JTAG/UART/SPI/TWI/ HDMI	3.3V
PI	7	Schmitt	CMOS	CSI/LCD/SPI/TWI	1.8V/2.8V/ 3.3V
PL	14	Schmitt	CMOS	RSB/UART/TWI/JTAG/PWM/IR	3.3V

12.7.3.2. Port Functiom

Port Controller supports 8 GPIOs, every GPIO can configure as Input,Output,Function Peripheral,IO disable or Interrupt function. The configuration instruction of every function is as follows.

Table 12-21. Port Function

	Function	Buffer Strength	Pull Up	Pull Down
Input	GPIO/Multiplexing Input	/	X	X
Output	GPIO/Multiplexing Output	Y	X	X
Disable	Pull Up	/	Y	N
	Pull Down	/	N	Y
Interrupt	Trigger	/	X	X

/ : non-configure, configuration is invalid

Y : configure

X : Select configuration according to actual situation

N : Forbid to configure

12.7.3.3. Pull up/down Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

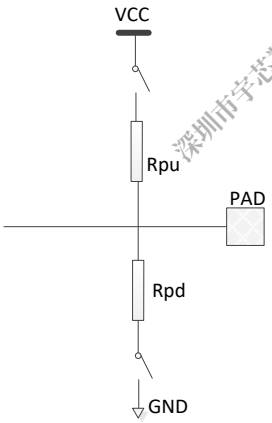


Figure 12-40. Pull up/down Logic

High-impedance, the output is float state, all buffer is off, the level is decided by external high/low level. When high-impedance, software configures the switch on Rpu and Rpd as off ,and the multiplexing function of IO is set as IO disable or input by software.

Pull-up, an uncertain signal is pulled high by a resistance, the resistance has current-limiting function. When pulling up, the switch on Rpu is breakover by software configuration, IO is pulled up to VCC by Rpu.

Pull-down, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is breakover by software configuration, IO is pulled down to GND by Rpd.

The pull-up/down of each IO is weak pull-up/down, the resistance is about 100kΩ.

The setting of pull-down,pull-up,high-impledance is decided by external circuit.

12.7.3.4. Buffer Strength

Each IO can be set as different buffer strength.The IO buffer diagram is as follows.

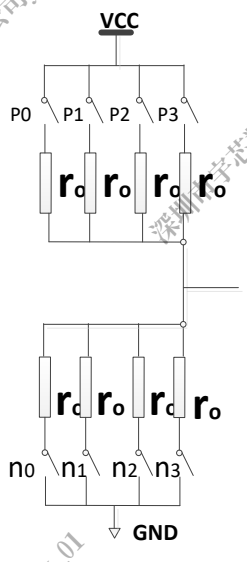


Figure 12-41. IO Buffer Strength Diagram

When output high level, the n0,n1,n2,n3 of NMOS is off, the p0,p1,p2,p3 of PMOS is on. When buffer strength is set to 0(buffer strength is weakest), only p0 is on, the output impedance is maximum ,the impedance value is r0. When buffer strength is set to 1, only p0 and p1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2.When buffer strength is 2, only p0,p1 and p2 is on, the output impedance is equivalent to three r0 in parallel, the

impedance value is r0/3.When buffer strength is 3, p0,p1,p2 and p3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0,p1,p2,p3 of PMOS is off, the n0,n1,n2,n3 of NMOS is on. When buffer strength is set to 0(buffer strength is weakest), only n0 is on, the output impedance is maximum ,the impedance value is r0. When buffer strength is set to 1, only n0 and n1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When buffer strength is 2, only n0,n1 and n2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, n0,n1,n2 and n3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between output driver circuit and port is unconnected, driver configuration is invalid.

12.7.3.5. **Interrupt**

Each group IO has independent interrupt number.IO within group uses one interrupt number, when one IO generates interrupt, Port Controller sent interrupt request to GIC. External Interrupt Status Register is used to query which IO generates interrupt.

Interrupt trigger of GPIO supports the following trigger types.

- Positive Edge : When low level changes to high level, the interrupt will generate. No matter how long high level keeps, the interrupt generates only once.
- Negative Edge: When high level changes to low level, the interrupt will generate. No matter how long low level keeps, the interrupt generates only once.
- High Level : Just keep high level and the interrupt will always generate.
- Low Level : Just keep low level and the interrupt will always generate.
- Double Edge : Positive and negative edge.

External Interrupt Configure Register is used to configure trigger type.

GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using lower sample clock, to reach the debounce effect because of the dither frequency of signal is higher than sample frequency.

Set sample clock source by PIO_INT_CLK_SELECT and prescale factor by DEB_CLK_PRE_SCALE.

12.7.4. CPUX Port Register List

Module Name	Base Address
GPIO	0x0300B000

Register Name	Offset	Description
Pn_CFG0	n*0x0024+0x00	Port n Configure Register 0 (n =2~8)
Pn_CFG1	n*0x0024+0x04	Port n Configure Register 1 (n =2~8)
Pn_CFG2	n*0x0024+0x08	Port n Configure Register 2 (n =2~8)
Pn_CFG3	n*0x0024+0x0C	Port n Configure Register 3 (n =2~8)
Pn_DAT	n*0x0024+0x10	Port n Data Register (n =0~9)
Pn_DRV0	n*0x0024+0x14	Port n Multi-Driving Register 0 (n =2~8)
Pn_DRV1	n*0x0024+0x18	Port n Multi-Driving Register 1 (n =2~8)
Pn_PUL0	n*0x0024+0x1C	Port n Pull Register 0 (n =2~8)

Pn_PUL1	n*0x0024+0x20	Port n Pull Register 1 (n =2~8)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrupt Configure Register 0(n =2~8)
Pn _INT_CFG1	0x200+n*0x20+0x04	PIO Interrupt Configure Register 1(n =2~8)
Pn _INT_CFG2	0x200+n*0x20+0x08	PIO Interrupt Configure Register 2(n =2~8)
Pn _INT_CFG3	0x200+n*0x20+0x0C	PIO Interrupt Configure Register 3(n =2~8)
Pn _INT_CTL	0x200+n*0x20+0x10	PIO Interrupt Control Register(n =2~8)
Pn _INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register(n =2~8)
Pn _INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register(n =2~8)
PIO_POW_MOD_SEL	0x0340	PIO Group Withstand Voltage Mode Select Register
PIO_POW_MS_CTL	0x0344	PIO Group Withstand Voltage Mode Select Control Register
PIO_POW_VAL	0x0348	PIO Group Power Value Register

12.7.5. CPUX Port Register Description

12.7.5.1. PC Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0048			Register Name: PC_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PC7_SELECT 000:Input001:Output 010:NAND_DQ6 100:Reserved 110:PC_EINT7	 011:SDC2_D4 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PC6_SELECT 000:Input 010:NAND_DQ7 100:Reserved 110:PC_EINT6	 001:Output 011:SDC2_D3 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PC5_SELECT 000:Input 010:NAND_RB0 100:Reserved 110:PC_EINT5	 001:Output 011:SDC2_CMD 101:BOOT_SEL5 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PC4_SELECT 000:Input 010:NAND_RE 100:Reserved 110:PC_EINT4	 001:Output 011:SDC2_CLK 101:BOOT_SEL4 111:IO Disable
15	/	/	/	

14:12	R/W	0x7	PC3_SELECT 000:Input 010:NAND_CE0 100:SPI0_MISO 110:PC_EINT3	 001:Output 011:Reserved 101:BOOT_SEL3 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC2_SELECT 000:Input 010:NAND_CLE 100:SPI0_MOSI 110:PC_EINT2	 001:Output 011:Reserved 101:BOOT_SEL2 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PC1_SELECT 000:Input 010:NAND_ALE 100:SPI0_CS0 110:PC_EINT1	 001:Output 011:SDC2_RST 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PC0_SELECT 000:Input 010:NAND_WE 100:SPI0_CLK 110:PC_EINT0	 001:Output 011:SDC2_DS 101:Reserved 111:IO Disable

12.7.5.2. **PC Configure Register 1 (Default Value: 0x7777_7777)**

Offset: 0x004C			**Register Name: PC_CFG1**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PC14_SELECT 000:Input 010:NAND_DQ0 100:SPI0_HOLD 110:PC_EINT14	 001:Output 011:SDC2_D7 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PC13_SELECT 000:Input 010:NAND_DQ1 100:SPI0_WP 110:PC_EINT13	 001:Output 011:SDC2_D2 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PC12_SELECT 000:Input 010:NAND_DQ2	 001:Output 011:SDC2_D6

			100:Reserved 110:PC_EINT12	101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PC11_SELECT 000:Input 010:NAND_DQ3 100:Reserved 110:PC_EINT11	 001:Output 011:SDC2_D1 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC10_SELECT 000:Input 010:NAND_DQS 100:SPI0_CS1 110:PC_EINT10	 001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PC9_SELECT 000:Input 010:NAND_DQ4 100:Reserved 110:PC_EINT9	 001:Output 011:SDC2_D5 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PC8_SELECT 000:Input 010:NAND_DQ5 100:Reserved 110:PC_EINT8	 001:Output 011:SDC2_D0 101:Reserved 111:IO Disable

12.7.5.3. **PC Data Register (Default Value: 0x0000_0000)**

Offset: 0x0058			**Register Name: PC_DAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:0	R/W	0x0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

12.7.5.4. **PC Multi-Driving Register 0 (Default Value: 0x5555_5555)**

Offset: 0x005C			**Register Name: PC_DRV0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x1	PC14_DRV

			PC14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PC13_DRV PC13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PC12_DRV PC12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PC11_DRV PC11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PC10_DRV PC10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PC9_DRV PC9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PC8_DRV PC8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PC7_DRV PC7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PC6_DRV PC6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PC5_DRV PC5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PC4_DRV PC4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PC3_DRV PC3 Multi-Driving Select 00: Level 0 01: Level 1

			10: Level 2	11: Level 3
5:4	R/W	0x1	PC2_DRV PC2 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PC1_DRV PC1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PC0_DRV PC0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

12.7.5.5. **PC Pull Register 0 (Default Value: 0x4000_0440)**

Offset: 0x0064			**Register Name: PC_PULL0**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	/	/	/	
29:28	R/W	0x0	PC14_PULL PC14 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
27:26	R/W	0x0	PC13_PULL PC13 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
25:24	R/W	0x0	PC12_PULL PC12 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
23:22	R/W	0x0	PC11_PULL PC11 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
21:20	R/W	0x1	PC10_PULL PC10 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
19:18	R/W	0x0	PC9_PULL PC9 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
17:16	R/W	0x0	PC8_PULL PC8 Pull-up/down Select	

			00: Pull-up/down disable 10: Pull-down	01: Pull-up 11: Reserved
15:14	R/W	0x0	PC7_PULL PC7 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
13:12	R/W	0x0	PC6_PULL PC6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x1	PC5_PULL PC5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x1	PC4_PULL PC4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x1	PC2_PULL PC2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x1	PC1_PULL PC Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

12.7.5.6. **PD Configure Register 0 (Default Value: 0x7777_7777)**

Offset: 0x006C			**Register Name: PD_CFG0**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD7_SELECT 000:Input 010:LCD_D11 100:VO_D6 110:PD_EINT7	 001:Output 011:PWM_6 101:Reserved 111:IO Disable

27	/	/	/
26:24	R/W	0x7	PD6_SELECT 000:Input 001:Output 010:LCD_D10 011:PWM_5 100:VO_D5 101:Reserved 110:PD_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PD5_SELECT 000:Input 001:Output 010:LCD_D7 011:PWM_4 100:VO_D4 101:Reserved 110:PD_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PD4_SELECT 000:Input 001:Output 010:LCD_D6 011:PWM_3 100:VO_D3 101:Reserved 110:PD_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PD3_SELECT 000:Input 001:Output 010:LCD_D5 011:PWM_2 100:VO_D2 101:Reserved 110:PD_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PD2_SELECT 000:Input 001:Output 010:LCD_D4 011:PWM_1 100:VO_D1 101:Reserved 110:PD_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PD1_SELECT 000:Input 001:Output 010:LCD_D3 011:PWM_0 100:VO_D0 101:Reserved 110:PD_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD0_SELECT 000:Input 001:Output 010:LCD_D2 011:Reserved 100:Reserved 101:Reserved 110:PD_EINT0 111:IO Disable

12.7.5.7. **PD Configure Register 1 (Default Value: 0x7777_7777)**

Offset: 0x0070			Register Name: PD_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	R/W	0x7	PD15_SELECT 000:Input 010:LCD_D21 100:VO_D13 110:PD_EINT15	001:Output 011:I2S1_DOUT2 101:Reserved 111:IO Disable
30:28	/	/	/	
27	R/W	0x7	PD14_SELECT 000:Input 010:LCD_D20 100:VO_D12 110:PD_EINT14	001:Output 011:I2S1_DOUT1 101:Reserved 111:IO Disable
26:24	/	/	/	
23	R/W	0x7	PD13_SELECT 000:Input 010:LCD_D19 100:VO_D11 110:PD_EINT13	001:Output 011:I2S1_DOUT0 101:Reserved 111:IO Disable
22:20	/	/	/	
19	R/W	0x7	PD12_SELECT 000:Input 010:LCD_D18 100:VO_D10 110:PD_EINT12	001:Output 011:I2S1_LRCK 101:Reserved 111:IO Disable
18:16	/	/	/	
15	R/W	0x7	PD11_SELECT 000:Input 010:LCD_D15 100:VO_D9 110:PD_EINT11	001:Output 011:I2S1_BCLK 101:Reserved 111:IO Disable
14:12	/	/	/	
11	R/W	0x7	PD10_SELECT 000:Input 010:LCD_D14 100:VO_D8 110:PD_EINT10	001:Output 011:I2S1_MCLK 101:Reserved 111:IO Disable
10:8	/	/	/	
7	R/W	0x7	PD9_SELECT 000:Input 010:LCD_D13 100:Reserved 110:PD_EINT9	001:Output 011:Reserved 101:Reserved 111:IO Disable
6:4	/	/	/	

3	R/W	0x7	PD8_SELECT 000:Input 010:LCD_D12 100:VO_D7 110:PD_EINT8	001:Output 011:PWM_7 101:Reserved 111:IO Disable
2:0	R/W	0x7	PD15_SELECT 000:Input 010:LCD_D21 100:VO_D13 110:PD_EINT15	001:Output 011:I2S1_DOUT2 101:Reserved 111:IO Disable

12.7.5.8. **PD Configure Register 2 (Default Value: 0x0777_7777)**

Offset: 0x0074			**Register Name: PD_CFG2**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PD22_SELECT 000:Input 010:PWM_8 100:Reserved 110:PD_EINT22	001:Output 011:Reserved 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PD21_SELECT 000:Input 010:LCD_VSYNC 100:VO_VSYNC 110:PD_EINT21	001:Output 011:Reserved 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD20_SELECT 000:Input 010:LCD_HSYNC 100:VO_HSYNC 110:PD_EINT20	001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD19_SELECT 000:Input 010:LCD_DE 100:VO_FIELD 110:PD_EINT19	001:Output 011:TCON_TRIG 101: Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD18_SELECT 000:Input 010:LCD_CLK 100:VO_CLK 110:PD_EINT18	001:Output 011:Reserved 101:Reserved 111:IO Disable

7	/	/	/
6:4	R/W	0x7	PD17_SELECT 000:Input 001:Output 010:LCD_D23 011:I2S1_DIN 100:VO_D15 101:Reserved 110:PD_EINT17 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD16_SELECT 000:Input 001:Output 010:LCD_D22 011:I2S1_DOUT3 100:VO_D14 101:Reserved 110:PD_EINT16 111:IO Disable

12.7.5.9. **PD Data Register (Default Value: 0x0000_0000)**

Offset: 0x007C			**Register Name: PD_DAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:0	R/W	0x0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

12.7.5.10. **PD Multi-Driving Register 0 (Default Value: 0x5555_5555)**

Offset: 0x0080			**Register Name: PD_DRV0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PD15_DRV PD15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PD14_DRV PD14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PD13_DRV PD13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PD12_DRV PD12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

23:22	R/W	0x1	PD11_DRV PD11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PD10_DRV PD10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PD9_DRV PD9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PD8_DRV PD8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PD7_DRV PD7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PD6_DRV PD6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PD5_DRV PD5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PD4_DRV PD4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PD3_DRV PD3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PD2_DRV PD2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PD1_DRV PD1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PD0_DRV PD0 Multi-Driving Select

			00: Level 0	01: Level 1
			10: Level 2	11: Level 3

12.7.5.11. **PD Multi-Driving Register 1 (Default Value: 0x0000_1555)**

Offset: 0x0084			Register Name: PD_DRV1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:14	/	/	/	
13:12	R/W	0x1	PD22_DRV PD22 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PD21_DRV PD21 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PD20_DRV PD20 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PD19_DRV PD19 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PD18_DRV PD18 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PD17_DRV PD17 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PD16_DRV PD16 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

12.7.5.12. **PD Pull Register 0 (Default Value: 0x0000_0000)**

Offset: 0x0088			Register Name: PD_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x0	PD15_PULL PD15 Pull-up/down Select 00: Pull-up/down disable	 01: Pull-up

			10: Pull-down	11: Reserved
29:28	R/W	0x0	PD14_PULL PD14 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
27:26	R/W	0x0	PD13_PULL PD13 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
25:24	R/W	0x0	PD12_PULL PD12 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
23:22	R/W	0x0	PD11_PULL PD11 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
21:20	R/W	0x0	PD10_PULL PD10 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
19:18	R/W	0x0	PD9_PULL PD9 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
17:16	R/W	0x0	PD8_PULL PD8 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
15:14	R/W	0x0	PD7_PULL PD7 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x0	PD3_PULL	

			PD3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PD1_PULL PD1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PD0_PULL PD0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

12.7.5.13. **PD Pull Register 1 (Default Value: 0x0000_0000)**

Offset: 0x008C			**Register Name: PD_PULL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	PD22_PULL PD22 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PD21_PULL PD21 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PD20_PULL PD20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD19_PULL PD19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PD17_PULL PD17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

1:0	R/W	0x0	PD16_PULL PD16 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	01: Pull-up 11: Reserved

12.7.5.14. **PE Configure Register 0 (Default Value: 0x7777_7777)**

Offset: 0x0090			Register Name: PE_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PE7_SELECT 000:Input 010:NCSI0_D3 100:Reserved 110:PE_EINT7	001:Output 011:RGMII_TXD3 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PE6_SELECT 000:Input 010:NCSI0_D2 100:Reserved 110:PE_EINT6	001:Output 011:RGMII_CLKIN/RMII_RXER 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PE5_SELECT 000:Input 010:NCSI0_D1 100:Reserved 110:PE_EINT5	001:Output 011:RGMII_RXCTL/RMII_CRS_DV 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PE4_SELECT 000:Input 010:NCSI0_D0 100:Reserved 110:PE_EINT4	001:Output 011:RGMII_RXCK 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PE3_SELECT 000:Input 010:NCSI0_VSYNC 100:Reserved 110:PE_EINT3	001:Output 011:RGMII_RXD0/RMII_RXD0 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PE2_SELECT 000:Input 010:NCSI0_HSYNC 100:Reserved 110:PE_EINT2	001:Output 011:RGMII_RXD1/RMII_RXD1 101:Reserved 111:IO Disable

7	/	/	/
6:4	R/W	0x7	PE1_SELECT 000:Input 001:Output 010:CSI_MASTERCLK1 011:RGMII_RXD2 100:Reserved 101:Reserved 110:PE_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PE0_SELECT 000:Input 001:Output 010:NCSI0_PCLK 011:RGMII_RXD3 100:Reserved 101:Reserved 110:PE_EINT0 111:IO Disable

12.7.5.15. **PE Configure Register 1 (Default Value: 0x7777_7777)**

Offset: 0x0094			**Register Name: PE_CFG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PE15_SELECT 000:Input 001:Output 010: NCSI0_D11 011:EPHY_25M 100:Reserved 101: Reserved 110:PE_EINT15 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PE14_SELECT 000:Input 001:Output 010: NCSI0_D10 011:MDIO 100:Reserved 101:TWI3_SDA 110:PE_EINT14 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PE13_SELECT 000:Input 001:Output 010: NCSI0_D9 011:MDC 100:Reserved 101:TWI3_SCK 110:PE_EINT13 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PE12_SELECT 000:Input 001:Output 010: NCSI0_D8 011:RGMII_TXCTL/RMII_TXEN 100:Reserved 101:UART2_TX 110:PE_EINT12 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PE11_SELECT 000:Input 001:Output 010:NCSI0_D7 011:RGMII_TXCK/RMII_TXCK

			100:Reserved 110:PE_EINT11	101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PE10_SELECT 000:Input 010:NCSI0_D6 100:Reserved 110:PE_EINT10	 001:Output 011:RGMII_TXD0/RMII_TXD0 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PE9_SELECT 000:Input 010:NCSI0_D5 100:Reserved 110:PE_EINT9	 001:Output 011:RGMII_TXD1/RMII_TXD1 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PE8_SELECT 000:Input 010: NCSI0_D4 100:Reserved 110:PE_EINT8	 001:Output 011:RGMII_TXD2 101:Reserved 111:IO Disable

12.7.5.16. **PE Configure Register 2 (Default Value: 0x0000_0077)**

Offset: 0x0098			**Register Name: PE_CFG2**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:23	/	/	/	
22:20	R/W	0x7	PE21_SELECT 000:Input 010:NCSI0_D15 100:SPI2_CS0 110:PE_EINT21	 001:Output 011:LCD_D17 101:UART2_CTS 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PE20_SELECT 000:Input 010:NCSI0_D14 100:SPI2_MISO 110:PE_EINT20	 001:Output 011:LCD_D16 101:UART2_RTS 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PE19_SELECT 000:Input 010:NCSI0_D13 100:SPI2_MOSI 110:PE_EINT19	 001:Output 011:LCD_D9 101:UART2_RX 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PE18_SELECT	

			000:Input 010: NCSI0_D12 100:SPI2_CLK 110:PE_EINT18	001:Output 011:LCD_D8 101:UART2_TX 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PE17_SELECT 000:Input 010:CSI_CCI1_SDA 100:Reserved 110:PE_EINT17	 001:Output 011:LCD_D1 101:TWI1_SDA 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PE16_SELECT 000:Input 010:CSI_CCI1_SCK 100:Reserved 110:PE_EINT16	 001:Output 011:LCD_D0 101:TWI1_SCK 111:IO Disable

12.7.5.17. **PE Data Register (Default Value: 0x0000_0000)**

Offset: 0x00A0			**Register Name: PE_DAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:0	R/W	0x0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

12.7.5.18. **PE Multi-Driving Register 0 (Default Value: 0x5555_5555)**

Offset: 0x00A4			**Register Name: PE_DRV0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PE15_DRV PE15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PE14_DRV PE14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PE13_DRV PE13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

25:24	R/W	0x1	PE12_DRV PE12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PE11_DRV PE11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PE10_DRV PE10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PE9_DRV PE9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PE8_DRV PE8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PE7_DRV PE7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PE6_DRV PE6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PE5_DRV PE5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PE4_DRV PE4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PE3_DRV PE3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PE2_DRV PE2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PE1_DRV PE1 Multi-Driving Select

			00: Level 0 10: Level 2	01: Level 1 11: Level 3
1:0	R/W	0x1	PE0_DRV PE0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

12.7.5.19. **PE Multi-Driving Register 1 (Default Value: 0x0000_0005)**

Offset: 0x00A8			Register Name: PE_DRV1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:12	/	/	/	
11:10	R/W	0x1	PE21_DRV PE21 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PE20_DRV PE20 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PE19_DRV PE19 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PE18_DRV PE18 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PE17_DRV PE17 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PE16_DRV PE16 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

12.7.5.20. **PE Pull Register 0 (Default Value: 0x0000_0000)**

Offset: 0x00AC			Register Name: PE_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x0	PE15_PULL PE15 Pull-up/down Select 00: Pull-up/down disable	 01: Pull-up

			10: Pull-down	11: Reserved
29:28	R/W	0x0	PE14_PULL PE14 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
27:26	R/W	0x0	PE13_PULL PE13 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
25:24	R/W	0x0	PE12_PULL PE12 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
23:22	R/W	0x0	PE11_PULL PE11 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
21:20	R/W	0x0	PE10_PULL PE10 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
19:18	R/W	0x0	PE9_PULL PE9 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
15:14	R/W	0x0	PE7_PULL PE7 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
13:12	R/W	0x0	PE6_PULL PE6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PE5_PULL PE5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x0	PE4_PULL PE4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x0	PE3_PULL	

			PE3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PE1_PULL PE1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PE0_PULL PE0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

12.7.5.21. **PE Pull Register 1 (Default Value: 0x0000_0000)**

Offset: 0x00B0			**Register Name: PE_PULL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x0	PE21_PULL PE21 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PE20_PULL PE20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PE19_PULL PE19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PE18_PULL PE18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PE17_PULL PE17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PE16_PULL PE16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

12.7.5.22. **PF Configure Register 0 (Default Value: 0x0777_7777)**

Offset: 0x00B4			Register Name: PF_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PF6_SELECT 000:Input 010:Reserved 100:Reserved 110:PF_EINT6	 001:Output 011:Reserved 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PF5_SELECT 000:Input 010:SDC0_D2 100:Reserved 110:PF_EINT5	 001:Output 011:JTAG_CK 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PF4_SELECT 000:Input 010:SDC0_D3 100:Reserved 110:PF_EINT4	 001:Output 011:UART0_RX 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PF3_SELECT 000:Input 010:SDC0_CMD 100:Reserved 110:PF_EINT3	 001:Output 011:JTAG_DO 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PF2_SELECT 000:Input 010:SDC0_CLK 100:Reserved 110:PF_EINT2	 001:Output 011:UART0_TX 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PF1_SELECT 000:Input 010:SDC0_D0 100:Reserved 110:PF_EINT1	 001:Output 011:JTAG_DI 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PF0_SELECT 000:Input 010:SDC0_D1	 001:Output 011:JTAG_MS

			100:Reserved 110:PF_EINT0	101:Reserved 111:IO Disable

12.7.5.23. **PF Data Register (Default Value: 0x0000_0000)**

Offset: 0x00C4			Register Name: PF_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R/W	0x0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

12.7.5.24. **PF Multi-Driving Register 0 (Default Value: 0x0000_1555)**

Offset: 0x00C8			Register Name: PF_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	PF6_DRV PF6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PF5_DRV PF5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PF4_DRV PF4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PF3_DRV PF3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PF2_DRV PF2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PF1_DRV PF1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PF0_DRV

			PF0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

12.7.5.25. **PF Pull Register 0 (Default Value: 0x0000_0000)**

Offset: 0x00D0			Register Name: PF_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:14	/	/	/	
13:12	R/W	0x0	PF6_PULL PF6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PF0_PULL PF0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

12.7.5.26. **PG Configure Register 0 (Default Value: 0x7777_7777)**

Offset: 0x00D8			Register Name: PG_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PG7_SELECT

			000:Input 010:UART1_RX 100:Reserved 110:PG_EINT7	001:Output 011:Reserved 101:RMII_TXD1 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PG6_SELECT 000:Input 010:UART1_TX 100:Reserved 110:PG_EINT6	 001:Output 011:Reserved 101:RMII_RXER 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PG5_SELECT 000:Input 010:SDC1_D3 100:Reserved 110:PG_EINT5	 001:Output 011:Reserved 101:RMII_CRS_DV 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PG4_SELECT 000:Input 010:SDC1_D2 100:Reserved 110:PG_EINT4	 001:Output 011:Reserved 101: RMII_RXD0 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PG3_SELECT 000:Input 010:SDC1_D1 100:Reserved 110:PG_EINT3	 001:Output 011:Reserved 101: RMII_RXD1 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PG2_SELECT 000:Input 010:SDC1_D0 100:Reserved 110:PG_EINT2	 001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PG1_SELECT 000:Input 010:SDC1_CMD 100:Reserved 110:PG_EINT1	 001:Output 011:Reserved 101:CPU_BIST1 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PG0_SELECT 000:Input 010:SDC1_CLK 100:Reserved 110:PG_EINT0	 001:Output 011:Reserved 101:CPU_BIST0 111:IO Disable

12.7.5.27. **PG Configure Register 1 (Default Value: 0x0077_7777)**

Offset: 0x00DC			Register Name: PG_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:23	/	/	/	
22:20	R/W	0x7	PG13_SELECT 000:Input 010:AIF3_DIN 100:Reserved 110:PG_EINT13	 001:Output 011:I2S2_DIN 101:EPHY_25M 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PG12_SELECT 000:Input 010:AIF3_DOUT 100:Reserved 110:PG_EINT12	 001:Output 011:I2S2_DOUT 101:MDIO 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PG11_SELECT 000:Input 010:AIF3_SYNC 100:Reserved 110:PG_EINT11	 001:Output 011:I2S2_LRCK 101:MDC 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PG10_SELECT 000:Input 010:AIF3_BCLK 100:Reserved 110:PG_EINT10	 001:Output 011:I2S2_BCLK 101:RMII_TXEN 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PG9_SELECT 000:Input 010:UART1_CTS 100:Reserved 110:PG_EINT9	 001:Output 011:I2S2_MCLK 101:RMII_TXCK 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PG8_SELECT 000:Input 010:UART1_RTS 100:Reserved 110:PG_EINT8	 001:Output 011:Reserved 101:RMII_TXD0 111:IO Disable

12.7.5.28. **PG Data Register (Default Value: 0x0000_0000)**

Offset: 0x00E8			Register Name: PG_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

12.7.5.29. **PG Multi-Driving Register 0 (Default Value: 0x0555_5555)**

Offset: 0x00EC			Register Name: PG_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:26	R/W	0x1	PG13_DRV PG13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PG12_DRV PG12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PG11_DRV PG11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PG10_DRV PG10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PG9_DRV PG9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PG8_DRV PG8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PG7_DRV PG7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PG6_DRV

			PG6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PG5_DRV PG5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PG4_DRV PG4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PG3_DRV PG3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PG2_DRV PG2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PG1_DRV PG1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PG0_DRV PG0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

12.7.5.30. **PG Pull Register 0 (Default Value: 0x0000_0000)**

Offset: 0x00F4			**Register Name: PG_PULL0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:26	R/W	0x0	PG13_PULL PG13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PG12_PULL PG12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PG11_PULL PG11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

21:20	R/W	0x0	PG10_PULL PG10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PG9_PULL PG9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PG8_PULL PG8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PG7_PULL PG7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PG6_PULL PG6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PG5_PULL PG5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PG4_PULL PG4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PG3_PULL PG3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PG2_PULL PG2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PG1_PULL PG1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PG0_PULL PG0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

12.7.5.31. **PH Configure Register 0 (Default Value: 0x7777_7777)**

Offset: 0x00FC			Register Name: PH_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PH7_SELECT 000:Input 010:DMIC_DATA2 100:Reserved 110:PH_EINT7	 001:Output 011:UART0_TX 101:UART3_RTS 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PH6_SELECT 000:Input 010:DMIC_DATA1 100:Reserved 110:PH_EINT6	 001:Output 011:JTAG_CK 101:UART3_RX 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PH5_SELECT 000:Input 010:DMIC_DATA0 100:Reserved 110:PH_EINT5	 001:Output 011:JTAG_MS 101:UART3_TX 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PH4_SELECT 000:Input 010:AIF2_DIN 100:Reserved 110:PH_EINT4	 001:Output 011:I2S0_DIN 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PH3_SELECT 000:Input 010:AIF2_DOUT 100:Reserved 110:PH_EINT3	 001:Output 011:I2S0_DOUT 101:UART4_RTS 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH2_SELECT 000:Input 010: AIF2_SYNC 100:Reserved 110:PH_EINT2	 001:Output 011:I2S0_LRCK 101:UART4_CTS 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH1_SELECT 000:Input 010:AIF2_BCLK 100:Reserved 110:PH_EINT1	 001:Output 011:I2S0_BCLK 101:UART4_RX 111:IO Disable

3	/	/	/	
2:0	R/W	0x7	PH0_SELECT 000:Input 010:Reserved 100:Reserved 110:PH_EINT0	001:Output 011:I2S0_MCLK 101:UART4_TX 111:IO Disable

12.7.5.32. **PH Configure Register 1 (Default Value: 0x7777_7777)**

Offset: 0x0100			**Register Name: PH_CFG1**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PH15_SELECT 000:Input 010:DMIC_CLK 100:SPI1_CS1 110:PH_EINT15	001:Output 011:HDMI_CEC (Only for V536-H) 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PH14_SELECT 000:Input 010:Reserved 100:SPI1_CS0 110:PH_EINT14	001:Output 011:HDMI_SDA (Only for V536-H) 101:TWI0_SDA 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PH13_SELECT 000:Input 010:Reserved 100:SPI1_MISO 110:PH_EINT13	001:Output 011:HDMI_SCL (Only for V536-H) 101:TWI0_SCK 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PH12_SELECT 000:Input 010:Reserved 100:SPI1_MOSI 110:PH_EINT12	001:Output 011:Reserved 101:TWI1_SDA 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PH11_SELECT 000:Input 010:Reserved 100:SPI1_CLK 110:PH_EINT11	001:Output 011:Reserved 101:TWI1_SCK 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH10_SELECT 000:Input 010:Reserved	001:Output 011:JTAG_DI

			100:Reserved 110:PH_EINT10	101:TWI2_SDA 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH9_SELECT 000:Input 010:Reserved 100:Reserved 110:PH_EINT9	 001:Output 011:JTAG_DO 101:TWI2_SCK 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH8_SELECT 000:Input 010:DMIC_DATA3 100:Reserved 110:PH_EINT8	 001:Output 011:UART0_RX 101:UART3_CTS 111:IO Disable

12.7.5.33. **PH Data Register (Default Value: 0x0000_0000)**

Offset: 0x010C			**Register Name: PH_DAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

12.7.5.34. **PH Multi-Driving Register 0 (Default Value: 0x5555_5555)**

Offset: 0x0110			**Register Name: PH_DRV0**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x1	PH15_DRV PH15 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
29:28	R/W	0x1	PH14_DRV PH14 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
27:26	R/W	0x1	PH13_DRV PH13 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
25:24	R/W	0x1	PH12_DRV PH12 Multi-Driving Select	

			00: Level 0 10: Level 2	01: Level 1 11: Level 3
23:22	R/W	0x1	PH11_DRV PH11 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
21:20	R/W	0x1	PH10_DRV PH10 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
19:18	R/W	0x1	PH9_DRV PH9 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
17:16	R/W	0x1	PH8_DRV PH8 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
15:14	R/W	0x1	PH7_DRV PH7 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
13:12	R/W	0x1	PH6_DRV PH6 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PH5_DRV PH5 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PH4_DRV PH4 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PH3_DRV PH3 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PH2_DRV PH2 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PH1_DRV PH1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

1:0	R/W	0x1	PH0_DRV PH0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

12.7.5.35. **PH Pull Register 0 (Default Value: 0x0000_0000)**

Offset: 0x0118			Register Name: PH_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PH15_PULL PH15 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
29:28	R/W	0x0	PH14_PULL PH14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PH13_PULL PH13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PH10_PULL PH10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PH8_PULL PH8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PH7_PULL PH7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

13:12	R/W	0x0	PH6_PULL PH6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PH5_PULL PH5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PH4_PULL PH4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PH3_PULL PH3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PH2_PULL PH2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PH1_PULL PH1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PH0_PULL PH0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

12.7.5.36. **PI Configure Register 0 (Default Value: 0x7777_7777)**

Offset: 0x0120			**Register Name: PI_CFG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x7	PI6_SELECT 000:Input 001:Output 010:CSI_CCI0_SDA 011:Reserved 100:SPI3_CS0 101:TWI0_SDA 110:PI_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PI5_SELECT 000:Input 001:Output 010:CSI_CCI0_SCK 011:Reserved 100:SPI3_MISO 101:TWI0_SCK 110:PI_EINT5 111:IO Disable

19	/	/	/
18:16	R/W	0x7	PI4_SELECT 000:Input 001:Output 010:Reserved 011:TCON_TRIG 100:SPI3_MOSI 101:TWI2_SDA 110:PI_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PI3_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:SPI3_CLK 101:TWI2_SCK 110:PI_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PI2_SELECT 000:Input 001:Output 010:CSI_MASTERCLK0 011:Reserved 100:Reserved 101:Reserved 110:PI_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PI1_SELECT 000:Input 001:Output 010:CSI_SM_VS 011:Reserved 100:Reserved 101:TWI3_SDA 110:PI_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PI0_SELECT 000:Input 001:Output 010:CSI_SM_HS 011:Reserved 100:Reserved 101:TWI3_SCK 110:PI_EINT0 111:IO Disable

12.7.5.37. **PI Data Register (Default Value: 0x0000_0000)**

Offset: 0x0130			**Register Name: PI_DAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R/W	0x0	PI_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

12.7.5.38. **PI Multi-Driving Register 0 (Default Value: 0x5555_5555)**

Offset: 0x0134			Register Name: PI_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	PI6_DRV PI6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PI5_DRV PI5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PI4_DRV PI4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PI3_DRV PI3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PI2_DRV PI2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PI1_DRV PI1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PI0_DRV PI0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

12.7.5.39. **PI Pull Register 0 (Default Value: 0x0000_0000)**

Offset: 0x013C			Register Name: PI_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	PI6_PULL PI6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PI5_PULL PI5 Pull-up/down Select

			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PI4_PULL PI4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PI3_PULL PI3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PI2_PULL PI2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PI1_PULL PI1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PI0_PULL PI0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

12.7.5.40. **PC External Interrupt Configure Register 0 (Default Value: 0x0000_0000)**

Offset: 0x0240			**Register Name: PC_EINT_CFG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode

			0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.41. **PC External Interrupt Configure Register 1 (Default Value: 0x0000_0000)**

Offset: 0x0244			Register Name: PC_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative)

			Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.42. **PC External Interrupt Control Register (Default Value: 0x0000_0000)**

Offset: 0x0250			**Register Name: PC_EINT_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable

			0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

12.7.5.43. **PC External Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0254			**Register Name: PC_EINT_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	EINT14_STATUS

			External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit

			0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

12.7.5.44. **PC External Interrupt Debounce Register (Default Value: 0x0000_0000)**

Offset: 0x0258			**Register Name: PC_EINT_DEB**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

12.7.5.45. **PD External Interrupt Configure Register 0 (Default Value: 0x0000_0000)**

Offset: 0x0260			Register Name: PD_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode

			0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.46. **PD External Interrupt Configure Register 1 (Default Value: 0x0000_0000)**

Offset: 0x0264			**Register Name: PD_EINT_CFG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode

			0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.47. **PD External Interrupt Configure Register 2 (Default Value: 0x0000_0000)**

Offset: 0x0268			Register Name: PD_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT22_CFG External INT22 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative)

			Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.48. **PD External Interrupt Control Register (Default Value: 0x0000_0000)**

Offset: 0x0270			**Register Name: PD_EINT_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W	0x0	EINT22_CTL External INT22 Enable 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable

			0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable

5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

12.7.5.49. **PD External Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0274			**Register Name: PD_EINT_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W	0x0	EINT22_STATUS External INT22 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
21	R/W	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
20	R/W	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS

			External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit

			0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

12.7.5.50. **PD External Interrupt Debounce Register (Default Value: 0x0000_0000)**

Offset: 0x0278			**Register Name: PD_EINT_DEB**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

12.7.5.51. **PE External Interrupt Configure Register 0 (Default Value: 0x0000_0000)**

Offset: 0x0280			**Register Name: PE_EINT_CFG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG

			External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative)

			Others: Reserved

12.7.5.52. **PE External Interrupt Configure Register 1 (Default Value: 0x0000_0000)**

Offset: 0x0284			Register Name: PE_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative)

			Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.53. **PE External Interrupt Configure Register 2 (Default Value: 0x0000_0000)**

Offset: 0x0288			**Register Name: PE_EINT_CFG2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

			0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.54. PE External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PE_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL

			External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable

			1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

12.7.5.55. **PE External Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0294			**Register Name: PE_EINT_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	EINT21_STATUS External INT21 Pending Bit

			0: No IRQ pending 1: IRQ pending Write '1' to clear
20	R/W	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending

			1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending

			Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

12.7.5.56. **PE External Interrupt Debounce Register (Default Value: 0x0000_0000)**

Offset: 0x0298			**Register Name: PE_EINT_DEB**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

12.7.5.57. **PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)**

Offset: 0x02A0			**Register Name: PF_EINT_CFG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level

			0100: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.58. **PF External Interrupt Control Register (Default Value: 0x0000_0000)**

Offset: 0x02B0			Register Name: PF_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

12.7.5.59. **PF External Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x02B4			Register Name: PF_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit

			0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

12.7.5.60. PF External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02B8			Register Name: PF_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select

			0: LOSC 32768Hz 1: HOSC 24MHz

12.7.5.61. **PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)**

Offset: 0x02C0			Register Name:PG_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level

			0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.62. **PG External Interrupt Configure Register 1 (Default Value: 0x0000_0000)**

Offset: 0x02C4			**Register Name: PG_EINT_CFG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level

			0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.63. PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: PG_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable

12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable

			0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

12.7.5.64. **PG External Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x02D4			Register Name: PG_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending

			1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

12.7.5.65. **PG External Interrupt Debounce Register (Default Value: 0x0000_0000)**

Offset: 0x02D8			**Register Name: PG_EINT_DEB**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n

			The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32768Hz 1: HOSC 24MHz

12.7.5.66. **PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)**

Offset: 0x02E0			Register Name:PH_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode

			0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.67. **PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)**

Offset: 0x02E4			**Register Name: PH_EINT_CFG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode

			0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.68. **PH External Interrupt Control Register (Default Value: 0x0000_0000)**

Offset: 0x02F0			**Register Name: PH_EINT_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable

			1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

12.7.5.69. **PH External Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x02F4			**Register Name: PH_EINT_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS

			External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit

			0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

12.7.5.70. **PH External Interrupt Debounce Register (Default Value: 0x0000_0000)**

Offset: 0x02F8			**Register Name: PH_EINT_DEB**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32768Hz 1: HOSC 24MHz

12.7.5.71. **PI External Interrupt Configure Register 0 (Default Value: 0x0000_0000)**

Offset: 0x0300			Register Name: PI_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG

			External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

12.7.5.72. **PI External Interrupt Control Register (Default Value: 0x0000_0000)**

Offset: 0x0310			**Register Name: PI_EINT_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable

0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

12.7.5.73. **PI External Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0314			**Register Name: PI_EINT_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

12.7.5.74. **PI External Interrupt Debounce Register (Default Value: 0x0000_0000)**

Offset: 0x0318			Register Name: PI_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

12.7.5.75. **PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)**

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCC-IO POWER MODE Select 0: 3.3V 1: 1.8V
11:9	/	/	/
8	R/W	0x0	PI_POWER MODE Select 0: 3.3V 1: 1.8V If PI_Port Power Source selects VCC-IO,this bit is invalid
7	R/W	0x0	PH_POWER MODE Select 0: 3.3V 1: 1.8V
6	R/W	0x0	PG_POWER MODE Select 0: 3.3V 1: 1.8V If PG_Port Power Source selects VCC-IO,this bit is invalid
5	R/W	0x0	PF_POWER MODE Select 0: 3.3V 1: 1.8V If PF_Port Power Source selects VCC-IO,this bit is invalid
4	R/W	0x0	PE_POWER MODE Select 0: 3.3V 1: 1.8V If PE_Port Power Source selects VCC-IO,this bit is invalid
3	R/W	0x0	PD_POWER MODE Select

			0: 3.3V 1: 1.8V If PD_Port Power Source selects VCC-IO,this bit is invalid
2	R/W	0x0	PC_POWER MODE Select 0: 3.3V 1: 1.8V If PC_Port Power Source selects VCC-IO,this bit is invalid
1	/	/	/
0	/	/	/

NOTE

For 0x0340 register ,when the power domain of GPIO is larger than 1.8V, then the withstand voltage is set to 3.3V mode, that is, the corresponding register value is set to 0; when the power domain of GPIO is 1.8V,then the withstand voltage is set to 1.8V mode, that is, the corresponding register value is set to 1.

12.7.5.76. **PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)**

Offset: 0x0344			**Register Name: PIO_POW_MS_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCC-IO Withstand Voltage Mode Select Control 0：Enable 1：Disable
11:9	/	/	/
8	R/W	0x0	VCC-PI Withstand Voltage Mode Select Control 0：Enable 1：Disable
7	R/W	0x0	VCC-PH Withstand Voltage Mode Select Control 0：Enable 1：Disable
6	R/W	0x0	VCC-PG Withstand Voltage Mode Select Control 0：Enable 1：Disable
5	R/W	0x0	VCC-PF Withstand Voltage Mode Select Control 0：Enable 1：Disable
4	R/W	0x0	VCC-PE Withstand Voltage Mode Select Control 0：Enable 1：Disable
3	R/W	0x0	VCC-PD Withstand Voltage Mode Select Control 0：Enable 1：Disable
2	R/W	0x0	VCC-PC Withstand Voltage Mode Select Control 0：Enable 1：Disable

1	/	/	/
0	/	/	/

12.7.5.77. **PIO Group Power Value Register**

Offset: 0x0348			Register Name: PIO_POW_VAL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	/	VCC-IO Power Value
15:9	/	/	/
8	R	/	PI_Port Power Value
7	/	/	PH_Port Power Value
6	R	/	PG_Port Power Value
5	R	/	PF_Port Power Value
4	R	/	PE_Port Power Value
3	R	/	PD_Port Power Value
2	R	/	PC_Port Power Value
1	/	/	/
0	R	/	/

NOTE

IO pressure mode is more than 2.5V when reading 0;IO pressure mode is less than 2.0V when reading 1.

12.7.5.78. **PIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)**

Offset: 0x0350			Register Name: PIO_PV_SEL_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	VCC-PF Power Voltage Select Control 0：1.8V 1：3.3V

NOTE

IO pressure mode is 1.8V when reading 0;IO pressure mode is 3.3V when reading 1.

12.7.6. CPUS Port Register List

Module Name	Base Address
R_GPIO	0x07022000

Register Name	Offset	Description
Pn_CFG0	n*0x0024+0x00	Port n Configure Register 0 (n=0)
Pn_CFG1	n*0x0024+0x04	Port n Configure Register 1 (n=0)

Pn_CFG2	n*0x0024+0x08	Port n Configure Register 2 (n=0)
Pn_CFG3	n*0x0024+0x0C	Port n Configure Register 3 (n=0)
Pn_DAT	n*0x0024+0x10	Port n Data Register (n=0)
Pn_DRV0	n*0x0024+0x14	Port n Multi-Driving Register 0 (n=0)
Pn_DRV1	n*0x0024+0x18	Port n Multi-Driving Register 1 (n=0)
Pn_PUL0	n*0x0024+0x1C	Port n Pull Register 0 (n=0)
Pn_PUL1	n*0x0024+0x20	Port n Pull Register 1 (n=0)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrupt Configure Register 0 (n=0)
Pn _INT_CFG1	0x200+ n*0x20+0x04	PIO Interrupt Configure Register 1 (n=0)
Pn _INT_CFG2	0x200+ n*0x20+0x08	PIO Interrupt Configure Register 2 (n=0)
Pn _INT_CFG3	0x200+ n*0x20+0x0C	PIO Interrupt Configure Register 3 (n=0)
Pn _INT_CTL	0x200+ n*0x20+0x10	PIO Interrupt Control Register (n=0)
Pn _INT_STA	0x200+ n*0x20+0x14	PIO Interrupt Status Register (n=0)
Pn _INT_DEB	0x200+ n*0x20+0x18	PIO Interrupt Debounce Register (n=0)
PIO_POW_MOD_SEL	0x0340	PIO Group Withstand Voltage Mode Select Register
PIO_POW_VAL	0x0348	PIO Group Power Value Register

12.7.7. CPUS Register Description

12.7.7.1. PL Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0000			Register Name: PL_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PL7_SELECT 000:Input 001:Output 010:S_JTAG_DI 111:ONEWIRE 100:Reserved 101:Reserved 110:S_PL_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PL6_SELECT 000:Input 001:Output 010:S_JTAG_DO 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PL5_SELECT 000:Input 001:Output 010:S_JTAG_CK 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PL4_SELECT 000:Input 001:Output 010:S_JTAG_MS 011:Reserved

			100:Reserved 110:S_PL_EINT4	101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PL3_SELECT 000:Input 010:S_UART_RX 100:Reserved 110:S_PL_EINT3	001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PL2_SELECT 000:Input 010:S_UART_TX 100:Reserved 110:S_PL_EINT2	001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PL1_SELECT 000:Input 010:S_RSB_SDA 100:Reserved 110:S_PL_EINT1	001:Output 011:S_TWI0_SDA 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PL0_SELECT 000:Input 010:S_RSB_SCK 100:Reserved 110:S_PL_EINT0	001:Output 011:S_TWI0_SCK 101:Reserved 111:IO Disable

12.7.7.2. **PL Configure Register 1 (Default Value: 0x0077_7777)**

Offset: 0x0004			**Register Name: PL_CFG1**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:23	/	/	/	
22:20	R/W	0x7	PL13_SELECT 000:Input 010:S_CIR_RX 100:Reserved 110:S_PL_EINT13	001:Output 011:Reserved 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PL12_SELECT 000:Input 010:S_PWM_2 100:Reserved 110:S_PL_EINT12	001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PL11_SELECT	

			000:Input 010:S_PWM_1 100:Reserved 110:S_PL_EINT11	001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PL10_SELECT 000:Input 010:S_PWM_0 100:Reserved 110:S_PL_EINT10	 001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PL9_SELECT 000:Input 010:S_TWI1_SDA 100:Reserved 110:S_PL_EINT9	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PL8_SELECT 000:Input 010:S_TWI1_SCK 100:Reserved 110:S_PL_EINT8	 001:Output 011:Reserved 101:Reserved 111:IO Disable

12.7.7.3. **PL Data Register (Default Value: 0x0000_0000)**

Offset: 0x0010			**Register Name: PL_DAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	PL_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

12.7.7.4. **PL Multi-Driving Register 0 (Default Value: 0x0555_5555)**

Offset: 0x0014			**Register Name: PL_DRV0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:26	R/W	0x1	PL13_DRV PL13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PL12_DRV

			PL12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PL11_DRV PL11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PL10_DRV PL10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PL9_DRV PL9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PL8_DRV PL8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PL7_DRV PL7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PL6_DRV PL6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PL5_DRV PL5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PL4_DRV PL4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PL3_DRV PL3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PL2_DRV PL2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PL1_DRV PL1 Multi-Driving Select 00: Level 0 01: Level 1

			10: Level 2	11: Level 3
1:0	R/W	0x1	PL0_DRV PL0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

12.7.7.5. **PL Pull Register 0 (Default Value: 0x0000_0005)**

Offset: 0x001C			**Register Name: PL_PULL0**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:28	/	/	/	
27:26	R/W	0x0	PL13_PULL PL13 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
25:24	R/W	0x0	PL12_PULL PL12 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
23:22	R/W	0x0	PL11_PULL PL11 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
21:20	R/W	0x0	PL10_PULL PL10 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
19:18	R/W	0x0	PL9_PULL PL9 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
17:16	R/W	0x0	PL8_PULL PL8 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
15:14	R/W	0x0	PL7_PULL PL7 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
13:12	R/W	0x0	PL6_PULL PL6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PL5_PULL PL5 Pull-up/down Select	

			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PL4_PULL PL4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PL3_PULL PL3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PL2_PULL PL2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x1	PL1_PULL PL1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x1	PL0_PULL PL0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

12.7.7.6. **PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)**

Offset: 0x0200			**Register Name:PL_EINT_CFG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode

			0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

12.7.7.7. **PL External Interrupt Configure Register 1 (Default Value: 0x0000_0000)**

Offset: 0x0204			Register Name: PL_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative)

			Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

12.7.7.8. **PL External Interrupt Control Register (Default Value: 0x0000_0000)**

Offset: 0x0210			**Register Name: PL_EINT_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable

			0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

12.7.7.9. **PL External Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0214			**Register Name: PL_EINT_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending

			1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending

			Write ‘1’ to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

12.7.7.10. **PL External Interrupt Debounce Register (Default Value: 0x0000_0000)**

Offset: 0x0218			**Register Name: PL_EINT_DEB**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32768Hz 1: HOSC 24MHz

12.7.7.11. **PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)**

Offset: 0x0340			**Register Name: PIO_POW_MOD_SEL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	PL_POWER MODE Select 0: 3.3V 1: 1.8V If PL_Port Power Source selects VCC-IO,this bit is invalid

NOTE

For 0x0340 register ,when the power domain of GPIO is larger than 1.8V, then the withstand voltage is set to 3.3V mode, that is, the corresponding register value is set to 0; when the power domain of GPIO is 1.8V,then the withstand voltage is set to 1.8V mode, that is, the corresponding register value is set to 1.

12.7.7.12. **PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)**

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	VCC-PL Withstand Voltage Mode Select Control 0：Enable 1：Disable

12.7.7.13. **PIO Group Power Value Register**

Offset: 0x0348			Register Name: PIO_POW_VAL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	/	PL_Port Power Value If PL_Port Power Source selects VCC-IO,this bit is invalid

NOTE

IO pressure mode is more than 2.5V when reading 0;IO pressure mode is less than 2.0V when reading 1.

12.8. GPADC

12.8.1. Overview

The General Purpose ADC(GPADC) is a 12-bit sampling analog to digital converter with 4 channels multiplexer. This ADC is a type of successive approximation register (SAR) converter.

The GPADC has the following features:

- 12-bit resolution
- 8-bit effective SAR type A/D converter
- 64 FIFO depth of data register
- Power supply voltage: 1.8 V
- Analog input range: 0 V to 1.8 V
- Maximum sampling frequency: 1 MHz
- Supports data compare and interrupt
- Supports three operation modes:
  - Single conversion mode
  - Continuous conversion mode
  - Burst conversion mode

12.8.2. Block Diagram

Figure 12-42 shows the block diagram of the GPADC.

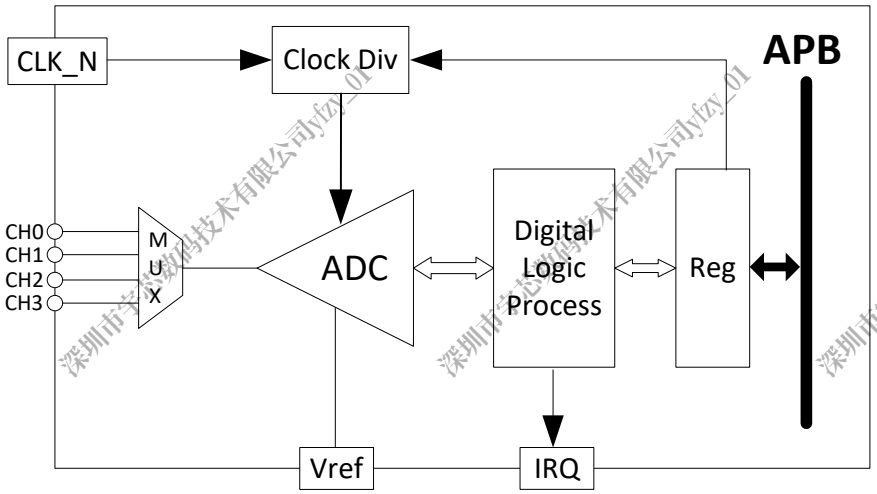


Figure 12-42. GPADC Block Diagram

12.8.3. Operations and Functional Descriptions

12.8.3.1. **External Signals**

Table 12-22 describes the external signals of GPADC.

Table 12-22. GPADC External Signals

Signal	Description	Type
GPADC0	ADC Input Channel0	AI
GPADC1	ADC Input Channel1	AI
GPADC2	ADC Input Channel2	AI
GPADC3	ADC Input Channel3	AI

12.8.3.2. Clock Sources

GPADC has one clock source. Table 12-23 describes the clock source for GPADC. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 12-23. GPADC Clock Sources

Clock Sources	Description
OSC24M	24MHz

12.8.3.3. GPADC Work Mode

(1).Single conversion mode

GPADC completes one conversion in specified channel, the converted data is updated at the data register of corresponding channel.

(2).Continuous conversion mode

GPADC has continuous conversion in specified channel until the software stops, the converted data is updated at the data register of corresponding channel.

(3).Burst conversion mode

GPADC samples and converts in the specified channel, and sequentially stores the results in FIFO.

12.8.3.4. Clock and Timing Requirements

CLK_IN = 24MHz

CONV_TIME(Conversion Time) = 1/(24MHz/14Cycles) =0.583 (us)

TACQ> 10RC (R is output impedance of ADC sample circuit, C= 6.4pF)

ADC Sample Frequency > TACQ+CONV_TIME

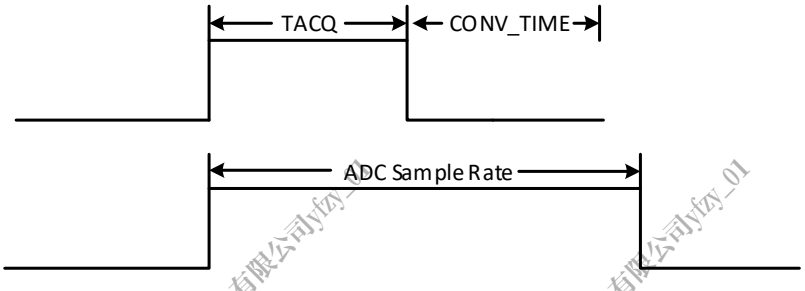


Figure 12-43. GPADC Clock and Timing Requirement

12.8.4. Programming Guidelines

(1) GPADC initial process is as follows.

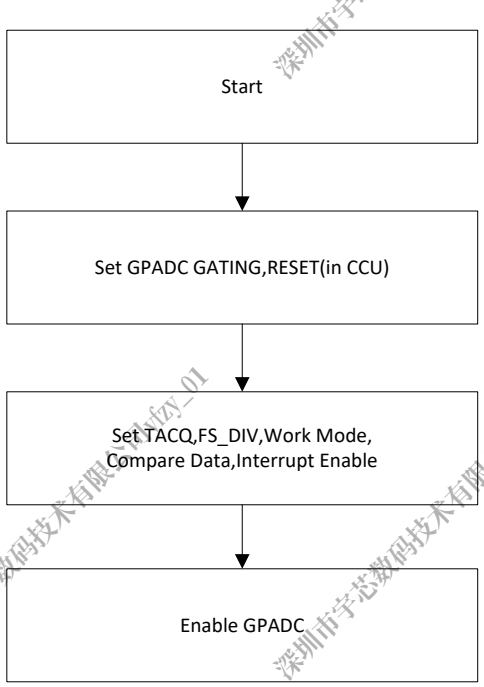


Figure 12-44. GPADC Initial Process

(2) Input voltage range: 0~1.8V

(3) Calculate formula: GPADC_DATA = Vin/V_{REF}*4096, V_{REF}=1.8V

12.8.5. Register List

Module Name	Base Address
GPADC	0x05070000

Register Name	Offset	Description
GP_SR_CON	0x0000	GPADC Sample Rate Configure Register
GP_CTRL	0x0004	GPADC Control Register
GP_CS_EN	0x0008	GPADC Compare and Select Enable Register
GP_FIFO_INTC	0x000C	GPADC FIFO Interrupt Control Register
GP_FIFO_INTS	0x0010	GPADC FIFO Interrupt Status Register
GP_FIFO_DATA	0x0014	GPADC FIFO Data Register
GP_CDATA	0x0018	GPADC Calibration Data Register
GP_DATAL_INTC	0x0020	GPADC Data Low Interrupt Configure Register
GP_DATAH_INTC	0x0024	GPADC Data High Interrupt Configure Register
GP_DATA_INTC	0x0028	GPADC Data Interrupt Configure Register
GP_DATAL_INTS	0x0030	GPADC Data Low Interrupt Status Register
GP_DATAH_INTS	0x0034	GPADC Data High Interrupt Status Register
GP_DATA_INTS	0x0038	GPADC Data Interrupt Status Register
GP_CH0_CMP_DATA	0x0040	GPADC CH0 Compare Data Register
GP_CH1_CMP_DATA	0x0044	GPADC CH1 Compare Data Register

GP_CH2_CMP_DATA	0x0048	GPADC CH2 Compare Data Register
GP_CH3_CMP_DATA	0x004C	GPADC CH3 Compare Data Register
GP_CH0_DATA	0x0080	GPADC CH0 Data Register
GP_CH1_DATA	0x0084	GPADC CH1 Data Register
GP_CH2_DATA	0x0088	GPADC CH2 Data Register
GP_CH3_DATA	0x008C	GPADC CH3 Data Register

12.8.6. Register Description

12.8.6.1. GPADC Sample Rate Configure Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: GP_SR_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 16	R/W	0x1DF	FS_DIV ADC sample frequency divider CLK_IN/(n+1) Default value: 50K
15:0	R/W	0x2F	TACQ ADC acquire time CLK_IN/(N+1) Default value: 2us

12.8.6.2. GPADC Control Register (Default Value: 0x0080_0000)

Offset: 0x0004			Register Name: GP_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/ W	0x0	ADC_FIRST_DLY ADC First Convert Delay Setting. ADC conversion of each channel is delayed by N samples.
23	R/ W	0x1	ADC_AUTOCALI_EN ADC Auto Calibration
22	/	/	/
21:20	R/W	0x0	ADC_OP_BIAS ADC OP Bias Adjust the bandwidth of the ADC amplifier
19:18	R/W	0x0	GPADC Work Mode 00: Single conversion mode 01: Reserved 10: Continuous conversion mode 11: Burst conversion mode
17	R/W	0x0	ADC_CALI_EN ADC Calibration 1: Start calibration, it is cleared to 0 after calibration
16	R/W	0x0	ADC_EN

			ADC Function Enable. Before the bit is enabled, configure ADC parameters including the work mode and channel number,etc. 0: Disable 1: Enable
15:0	/	/	/

12.8.6.3. **GPADC Compare and Select Enable Register (Default Value: 0x0000_0000)**

Offset: 0x0008			**Register Name: GP_CS_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	ADC_CH3_CMP_EN Channel 3 Compare Enable 0: Disable 1: Enable
18	R/W	0x0	ADC_CH2_CMP_EN Channel 2 Compare Enable 0: Disable 1: Enable
17	R/W	0x0	ADC_CH1_CMP_EN Channel 1 Compare Enable 0: Disable 1: Enable
16	R/W	0x0	ADC_CH0_CMP_EN Channel 0 Compare Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0x0	ADC_CH3_SELECT Analog Input Channel 3 Select 0: Disable 1: Enable
2	R/W	0x0	ADC_CH2_SELECT Analog Input Channel 2 Select 0: Disable 1: Enable
1	R/W	0x0	ADC_CH1_SELECT Analog Input Channel 1 Select 0: Disable 1: Enable
0	R/W	0x0	ADC_CH0_SELECT Analog Input Channel 0 Select 0: Disable 1: Enable

12.8.6.4. **GPADC FIFO Interrupt Control Register (Default Value: 0x0000_1F00)**

Offset: 0x000C			Register Name: GP_FIFO_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	FIFO_OVERRUN_IRQ_EN ADC FIFO Overrun IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	FIFO_DATA_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13:8	R/W	0x1F	FIFO_TRIG_LEVEL Interrupt Trigger Level for ADC Trigger Level = TXTL + 1
7:5	/	/	/
4	R/W1C	0x0	FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, clear automatically to '0'.
3:0	/	/	/

12.8.6.5. **GPADC FIFO Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0010			Register Name: GP_FIFO_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	FIFO_OVERRUN_PENDING ADC FIFO Overrun IRQ Pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
16	R/W1C	0x0	FIFO_DATA_PENDING ADC FIFO Data Available Pending Bit 0: No Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
15:14	/	/	/
13:8	R	0x0	RXA_CNT ADC FIFO available sample word counter

7:0	/	/	/

12.8.6.6. **GPADC FIFO Data Register**

Offset: 0x0014			Register Name: GP_FIFO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	UDF	GP_FIFO_DATA GPADC Data in FIFO

12.8.6.7. **GPADC Calibration Data Register (Default Value: 0x0000_0000)**

Offset: 0x0018			Register Name: GP_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	GP_CDATA GPADC Calibration Data

12.8.6.8. **GPADC Low Interrupt Configure Register (Default Value: 0x0000_0000)**

Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	CH3_LOW_IRQ_EN 0: Disable 1: Enable
2	R/W	0x0	CH2_LOW_IRQ_EN 0: Disable 1: Enable
1	R/W	0x0	CH1_LOW_IRQ_EN 0: Disable 1: Enable
0	R/W	0x0	CH0_LOW_IRQ_EN 0: Disable 1: Enable

12.8.6.9. **GPADC High Interrupt Configure Register (Default Value: 0x0000_0000)**

Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	CH3_HIG_IRQ_EN

			0: Disable 1: Enable
2	R/W	0x0	CH2_HIG_IRQ_EN 0: Disable 1: Enable
1	R/W	0x0	CH1_HIG_IRQ_EN 0: Disable 1: Enable
0	R/W	0x0	CH0_HIG_IRQ_EN 0: Disable 1: Enable

12.8.6.10. **GPADC DATA Interrupt Configure Register (Default Value: 0x0000_0000)**

Offset: 0x0028			**Register Name: GP_DATA_INTC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	CH3_DATA_IRQ_EN 0: Disable 1: Enable
2	R/W	0x0	CH2_DATA_IRQ_EN 0: Disable 1: Enable
1	R/W	0x0	CH1_DATA_IRQ_EN 0: Disable 1: Enable
0	R/W	0x0	CH0_DATA_IRQ_EN 0: Disable 1: Enable

12.8.6.11. **GPADC Low Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0030			**Register Name: GP_DATAL_INTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	CH3_LOW_PENGDING 1: Channel 3 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
2	R/W1C	0x0	CH2_LOW_PENGDING 1: Channel 2 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
1	R/W1C	0x0	CH1_LOW_PENGDING

			1: Channel 1 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	R/W1C	0x0	CH0_LOW_PENGDING 1: Channel 0 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

12.8.6.12. **GPADC High Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0034			**Register Name: GP_DATAH_INTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	CH3_HIG_PENGDING 0: No Pending IRQ 1: Channel 3 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
2	R/W1C	0x0	CH2_HIG_PENGDING 0: No Pending IRQ 1: Channel 2 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
1	R/W1C	0x0	CH1_HIG_PENGDING 0: No Pending IRQ 1: Channel 1 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	R/W1C	0x0	CH0_HIG_PENGDING 0: No Pending IRQ 1: Channel 0 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

12.8.6.13. **GPADC Data Interrupt Status Register (Default Value: 0x0000_0000)**

Offset: 0x0038			**Register Name: GP_DATA_INTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	CH3_DATA_PENGDING 0: No Pending IRQ 1: Channel 3 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

2	R/W1C	0x0	CH2_DATA_PENGDING 0: No Pending IRQ 1: Channel 2 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
1	R/W1C	0x0	CH1_DATA_PENGDING 0: No Pending IRQ 1: Channel 1 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	R/W1C	0x0	CH0_DATA_PENGDING 0: No Pending IRQ 1: Channel 0 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

12.8.6.14. **GPADC CH0 Compare Data Register (Default Value: 0x0BFF_0400)**

Offset: 0x0040			**Register Name: GP_CH0_CMP_DATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH0_CMP_HIG_DATA Channel 0 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH0_CMP_LOW_DATA Channel 0 Voltage Low Value

12.8.6.15. **GPADC CH1 Compare Data Register (Default Value: 0x0BFF_0400)**

Offset: 0x0044			**Register Name: GP_CH1_CMP_DATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH1_CMP_HIG_DATA Channel 1 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH1_CMP_LOW_DATA Channel 1 Voltage Low Value

12.8.6.16. **GPADC CH2 Compare Data Register (Default Value: 0x0BFF_0400)**

Offset: 0x0048			**Register Name: GP_CH2_CMP_DATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

27:16	R/W	0xBFF	CH2_CMP_HIG_DATA Channel 2 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH2_CMP_LOW_DATA Channel 2 Voltage Low Value

12.8.6.17. **GPADC CH3 Compare Data Register (Default Value: 0x0BFF_0400)**

Offset: 0x004C			**Register Name: GP_CH3_CMP_DATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH3_CMP_HIG_DATA Channel 3 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH3_CMP_LOW_DATA Channel 3 Voltage Low Value

12.8.6.18. **GPADC CH0 Data Register (Default Value: 0x0000_0000)**

Offset: 0x0080			**Register Name: GP_CH0_DATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x000	GP_CH0_DATA Channel 0 Data

12.8.6.19. **GPADC CH1 Data Register (Default Value: 0x0000_0000)**

Offset: 0x0084			**Register Name: GP_CH1_DATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x000	GP_CH1_DATA Channel 1 Data

12.8.6.20. **GPADC CH2 Data Register (Default Value: 0x0000_0000)**

Offset: 0x0088			**Register Name: GP_CH2_DATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x000	GP_CH2_DATA Channel 2 Data

12.8.6.21. GPADC CH3 Data Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: GP_CH3_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x000	GP_CH3_DATA Channel 3 Data

12.9. CIR Receiver

12.9.1. Overview

The CIR (Consumer Infrared) receiver is a capturer of the pulse from IR Receiver Module and uses Run-Length Code (RLC) to encode the pulse. The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in a 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal. The high level is represented as '1' and the low level is represented as '0'. The rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

In the air, there is always some noise. One threshold can be set to filter the noise to reduce system loading and improve the system stability.

The CIR receiver has the following features:

- Full physical layer implementation
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Programmable FIFO thresholds
- Interrupt support
- Sample clock up to 1 MHz

12.9.2. Block Diagram

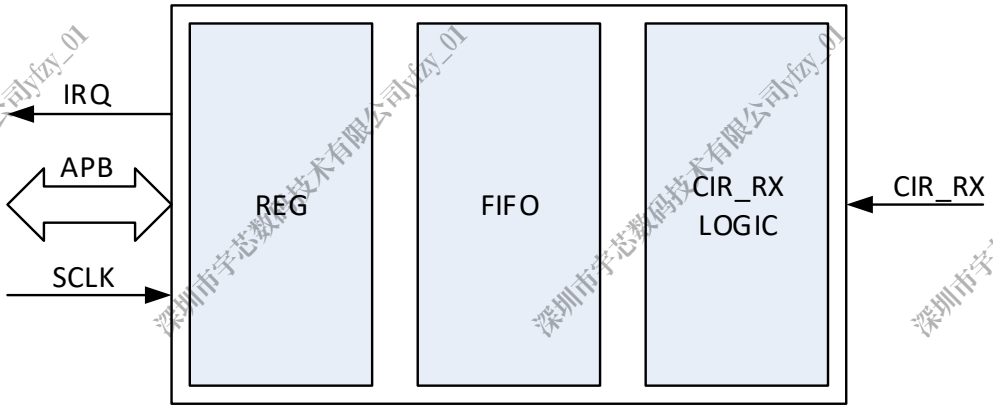


Figure 12-45. CIR Receiver Block Diagram

12.9.3. Operations and Functional Descriptions

12.9.3.1. External Signals

Table 12-24 describes the external signals of CIR Receiver.

Table 12-24. CIR Receiver External Signals

Signal	Description	Type
S_CIR_RX	CIR input signal	I

12.9.3.2. **Clock Sources**

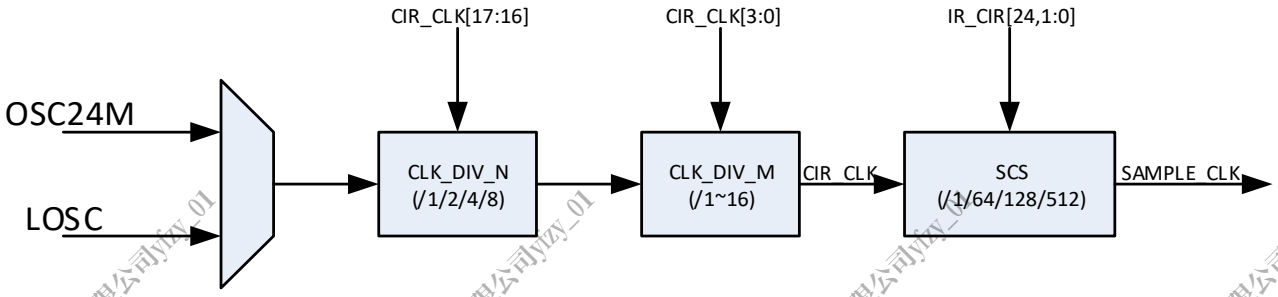


Figure 12-46. CIR Receiver Clock

12.9.3.3. **Typical Application**

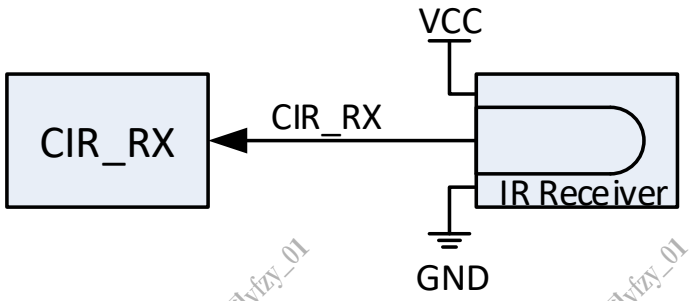


Figure 12-47. CIR Receiver Application Diagram

12.9.3.4. **Function Implementation**

Figure 12-48. NEC Protocol

In fact, CIR receiver module is a timer with capture function.

When CIR_RX signals satisfy ATHR (Active Threshold), CIR receiver can start to capture. In the process, the signal is ignored if the pulse width of the signal is less than NTHR. when CIR_RX signals satisfy ITHR (Idle Threshold), the capture process is stopped and the Receiver Packet End interrupt is generated, then Receiver Packet End Flag is asserted.

In a capture process, every effective pulse is buffered to FIFO in bytes according to the form of Run-Length Code. The MSB bit of a byte is polarity of pulse, and the rest 7 bits is pulse width by taking Sample Clock as basic unit. This is the

code form of RLC-Byte. When the level changes or the pulse width counting overflows, RLC-Byte is buffered to FIFO. The CIR_RX module receives infrared signals transmitted by the infrared remote control, the software decodes the signals.

12.9.3.5. **Operating Mode**

- Sample Clock

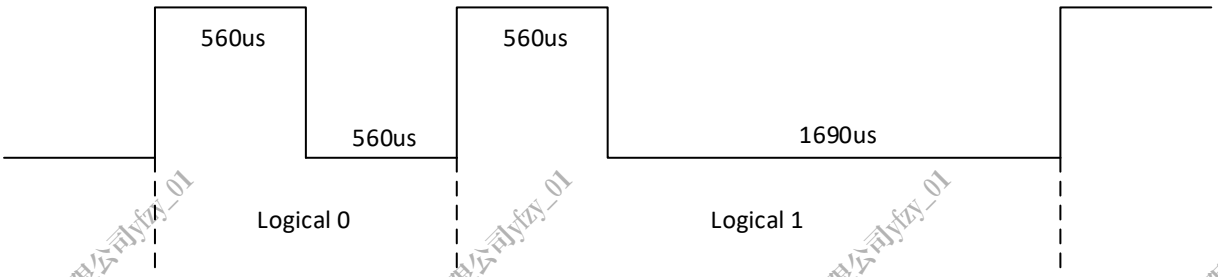


Figure 12-49. Logical '0' and Logical '1' of NEC Protocol

For NEC protocol, a logical "1" takes 2.25ms(560us+1680us) to transmit, while a logical "0" is only half of that, being 1.12ms(560us+560us). For example, if sample clock is 31.25 kHz, sample cycle is 32us,then 18 sample cycles is 560us.So the RLC of 560us low level is 0x12, the RLC of 560us high level is 0x92. Then a logical "1" takes code 0x12 and code 0xb5 to transmit, a logical "0" takes code 0x12 and code 0x92 to transmit.

- ATHR(Active Threshold)

When CIR receiver is in Idle state,if electrical level of CIR_RX signal changes (positive jump or negative jump), and the duration reaches this threshold, then CIR takes the starting of the signal as a lead code, turns into active state and starts to capture CIR_RX signals.

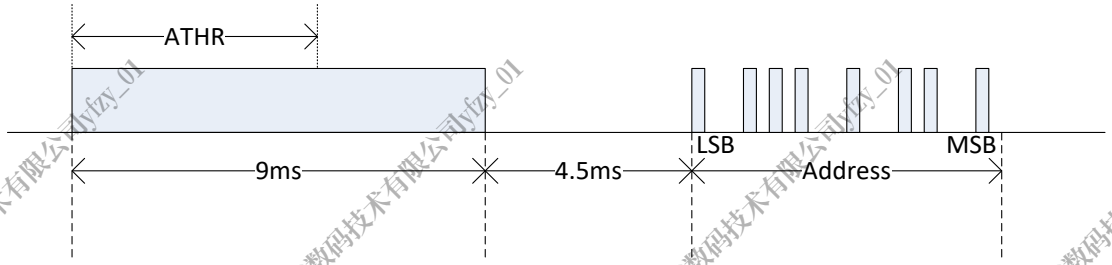


Figure 12-50. ATHR Definition

- ITHR(Idle Threshold)

If electrical level of CIR_RX signals has no change, and the duration reaches this threshold, then CIR receiver enters into Idle state and ends this capture.

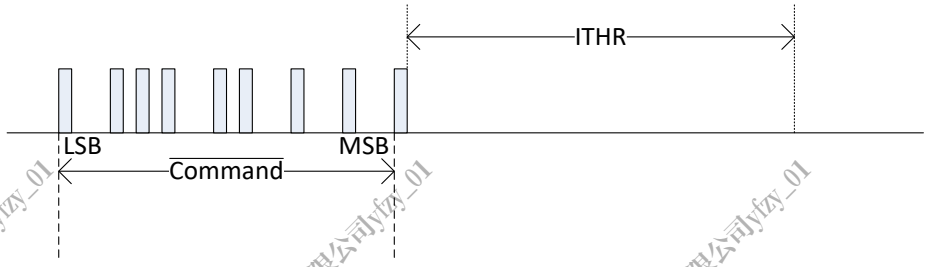


Figure 12-51. ITHR Definition

- NTHR(Noise Threshold)

In capture process,the pulse is ignored if the pulse width is less than Noise Threshold.

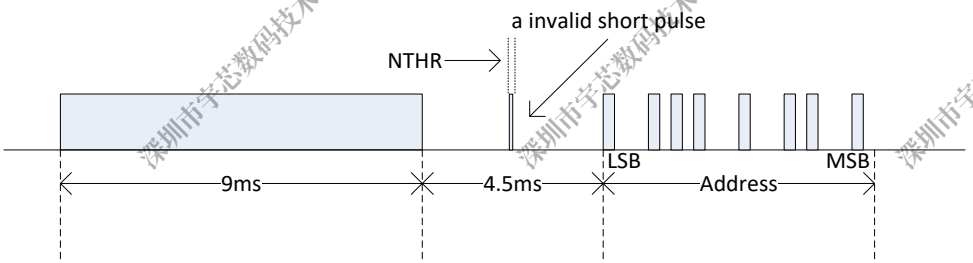


Figure 12-52. NTHR Definition

- APAM(Active Pulse Accept Mode)

APAM is used to fit the type of lead code. If a pulse does not fit the type of lead code, it is not regarded as a lead code even if the pulse width reaches ATHR.

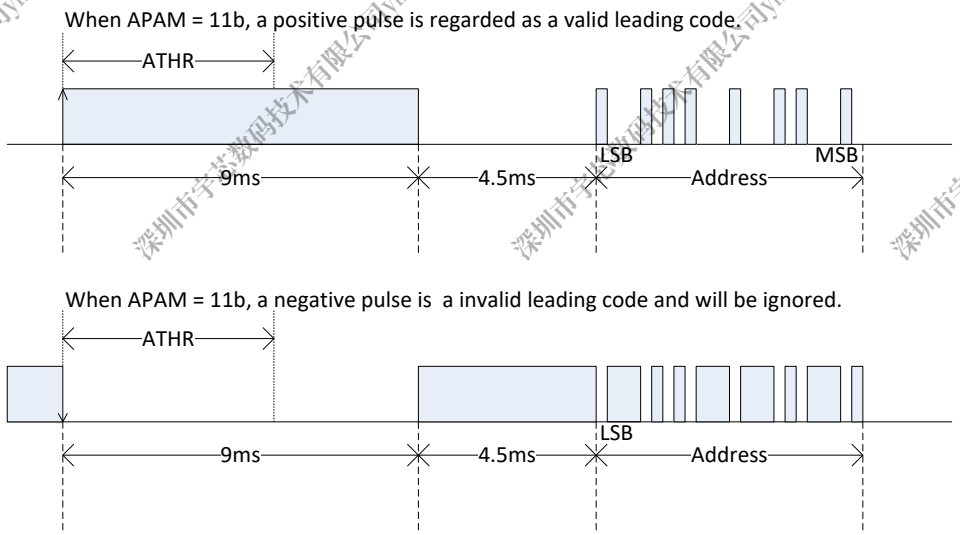


Figure 12-53. APAM Definition

12.9.4. Programming Guidelines

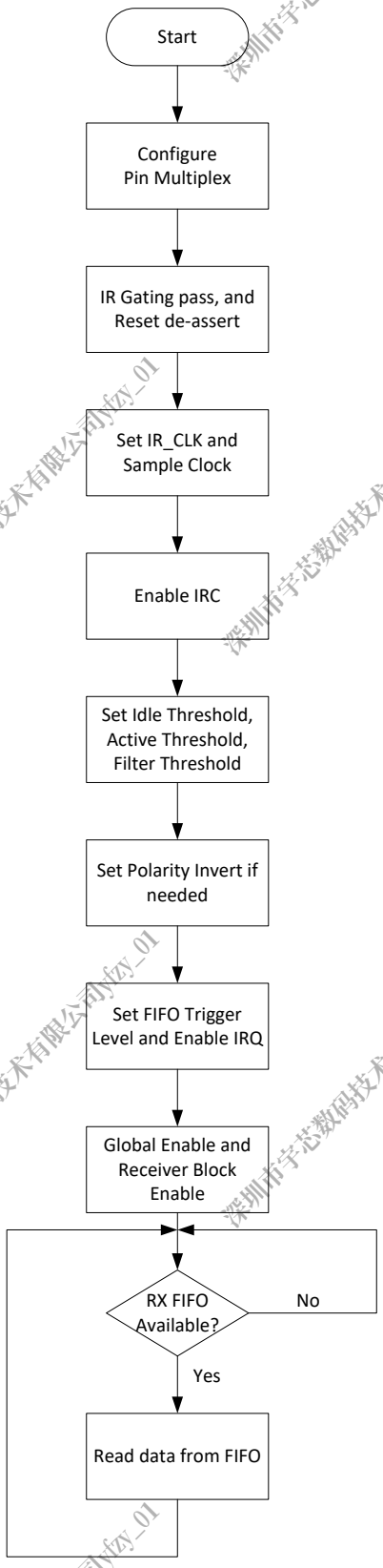


Figure 12-54. CIR Receiver Process

12.9.5. Register List

Module Name	Base Address
R_CIR_RX	0x07040000

Register Name	Offset	Description
CIR_CTL	0x0000	CIR Control Register
CIR_RXPCFG	0x0010	CIR Receiver Pulse Configure Register
CIR_RXFIFO	0x0020	CIR Receiver FIFO Register
CIR_RXINT	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x0030	CIR Receiver Status Register
CIR_RXCFG	0x0034	CIR Receiver Configure Register

12.9.6. Register Description

12.9.6.1. **CIR Receiver Control Register(Default Value: 0x0000_0000)**

Offset: 0x0000			Register Name: CIR_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	APAM Active Pulse Accept Mode 00, 01: Both positive and negative pulses are valid as a leading code. 10: Only negative pulse is valid as a leading code. 11: Only positive pulse is valid as a leading code.
5:4	R/W	0x0	CIR ENABLE 00~10: Reserved 11: CIR mode enable
3:2	/	/	/
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

12.9.6.2. **CIR Receiver Pulse Configure Register(Default Value: 0x0000_0004)**

Offset: 0x0010			Register Name: CIR_RXPCFG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:3	/	/	/
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert. 0: Do not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

12.9.6.3. **CIR Receiver FIFO Register(Default Value: 0x0000_0000)**

Offset: 0x0020			**Register Name: CIR_RXFIFO**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	Receiver Byte FIFO

12.9.6.4. **CIR Receiver Interrupt Control Register(Default Value: 0x0000_0000)**

Offset: 0x002C			**Register Name: CIR_RXINT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R/W	0x0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when condition fails.
4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

12.9.6.5. **CIR Receiver Status Register(Default Value: 0x0000_0000)**

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R	0x0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1 byte available data in RX FIFO 2: 2 byte available data in RX FIFO … 64: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0: Idle 1: busy
6:5	/	/	/
4	R/W	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/
1	R/W	0x0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7’b0000,000 and 8’b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

12.9.6.6. **CIR Receiver Configure Register(Default Value: 0x0000_1828)**

Offset: 0x0034			Register Name: CIR_RXCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:25	/	/	/
24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.

<table>
<tr><td>23</td><td>R/W</td><td>0x0</td><td>ATHC
Active Threshold Control for CIR
0: ATHR in Unit of (Sample Clock)
1: ATHR in Unit of (128*Sample Clocks)</td></tr>
<tr><td>22:16</td><td>R/W</td><td>0x0</td><td>ATHR
Active Threshold for CIR
These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1)*(ATHC? Sample Clock: 128*Sample Clock)).</td></tr>
<tr><td>15:8</td><td>R/W</td><td>0x18</td><td>ITHR
Idle Threshold for CIR
The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enabled, the interrupt line is asserted to CPU. When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.</td></tr>
<tr><td>7:2</td><td>R/W</td><td>0xa</td><td>NTHR
Noise Threshold for CIR
When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware.
0: all samples are recorded into RX FIFO
1: If the signal is only one sample duration, it is taken as noise and discarded.
2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded.
…
61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>0x0</td><td>SCS
Sample Clock Select for CIR
<table>
<tr><td>SCS2</td><td>SCS[1]</td><td>SCS[0]</td><td>Sample Clock</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>CIR_CLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>CIR_CLK /128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>CIR_CLK /256</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>CIR_CLK /512</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>CIR_CLK</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
</table>

12.10. PWM

12.10.1. Overview

PWM controller has 9 PWM channels(PWM0,PWM1,PWM2,PWM3,PWM4,PWM5,PWM6,PWM7,PWM8), and divides to 4 PWM pairs: PWM01 pair,PWM23 pair,PWM45 pair,PWM67 pair. PWM01 pair consists of PWM0 and PWM1, PWM23 pair consists of PWM2 and PWM3, PWM45 pair consists of PWM4 and PWM5, PWM67 pair consists of PWM6 and PWM7,PWM8 has no pair.

The PWM has the following features:

- 9 PWM channels
- Supports pulse,cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveform: continuous waveform,pulse waveform and complementary pair
- Output frequency range: 0~ 24MHz/100MHz
- Various duty-cycle: 0% ~100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input

12.10.2. Block Diagram

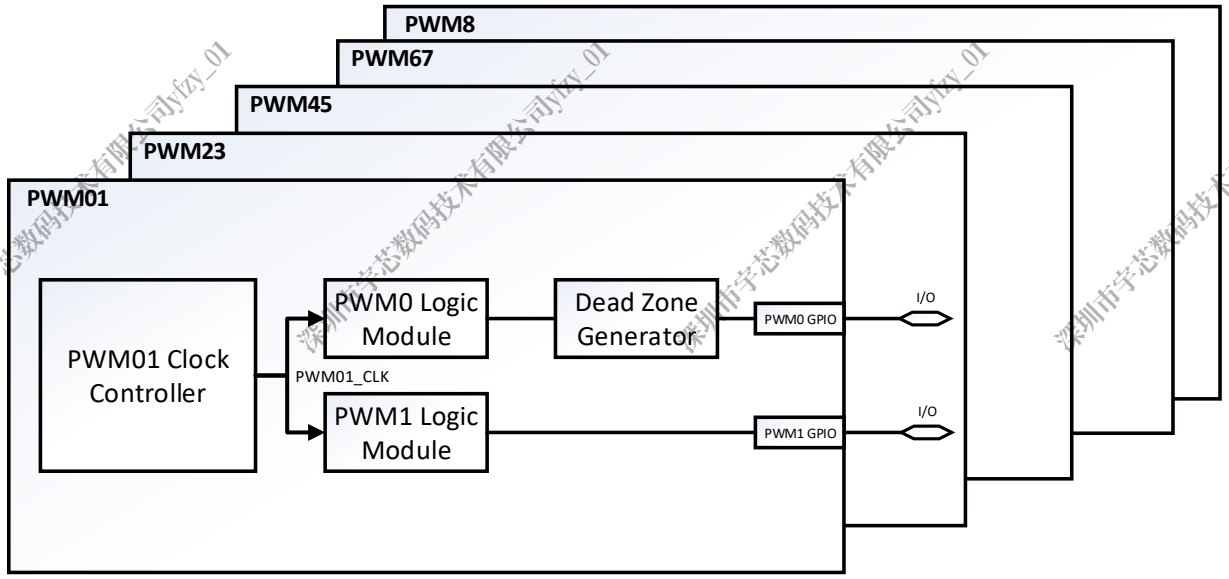


Figure 12-55. PWM Block Diagram

Each PWM pair consists of 1 clock module, 2 timer logic module and 1 programmable dead-time generator.

12.10.3. Operations and Functional Descriptions

12.10.3.1. Clock Controller

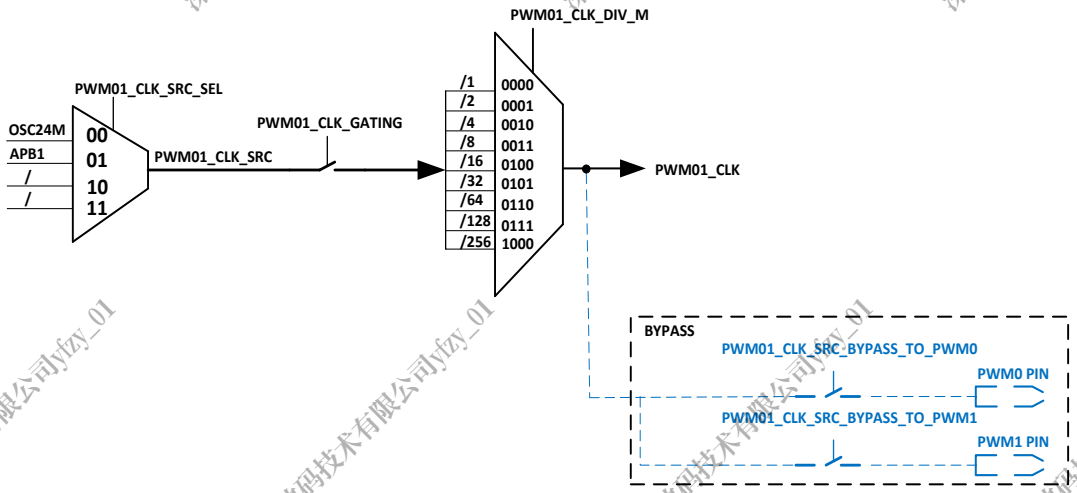


Figure 12-56. PWM01 Clock Controller Diagram

The clock controller of each PWM pair includes clock source select(PWM01_CLK_SRC_SEL),1~256 scaler (PWM01_CLK_DIV_M), clock source bypass(CLK_SRC_BYPASS) and clock swith(PWM01_CLK_GATING).

The clock sources of PWM have OSC24M and APB1 Bus. OSC24M comes from external high frequency oscillator, APB1 is APB1 bus clock,usually is 100MHz.

The clock source bypass function is that clock source directly accesses PWM output,the PWM output waveform is the waveform of clock controller output. The BYPASS gridlines in the above figure indicates clock source bypass function,the details about implement ,please see Figure 12-56. At last the output clock of the clock controller is sent to PWM logic module.

12.10.3.2. PWM Output

Using PWM01 as an example,Figure 12-57 indicates PWM01 output logic module diagram.Other PWM pairs(PWM23, PWM45, PWM67) logic module diagrams are the same as PWM01, PWM8 logic module diagram is the same as PWM1.

PWM Timer Logic consists of one 16-bit up-counter and one 16-bit comparator. The up-counter is used to control period, and the comparator is used to control duty-cycle. The up-counter and the comparator support cache-loading, PWM output is enabled, the register value of the counter and the comparator can be changed at any time,the changed value is cached to the cache register,when the value of up-counter is equal to **PWM_ENTIRE_CYCLE**, the value of the cache register is loaded to the counter and the comparator. Cache-loading is good to avoid unstable PWM output waveform with burred feature when updating the counter value and the comparator value.

PWM supports cycle and pulse waveform output.

Cycle mode: When the value of up-counter reaches **PWM_ENTIRE_CYCLE**, the value of up-counter is loaded automatically to 0 and the up-counter continues to count, then the output waveform is a continuous waveform.

Pulse mode: When the value of up-counter reaches **PWM_ENTIRE_CYCLE**, the value of up-counter is loaded automatically to 0 and the up-counter stops counting, then the output waveform is a pulse waveform.

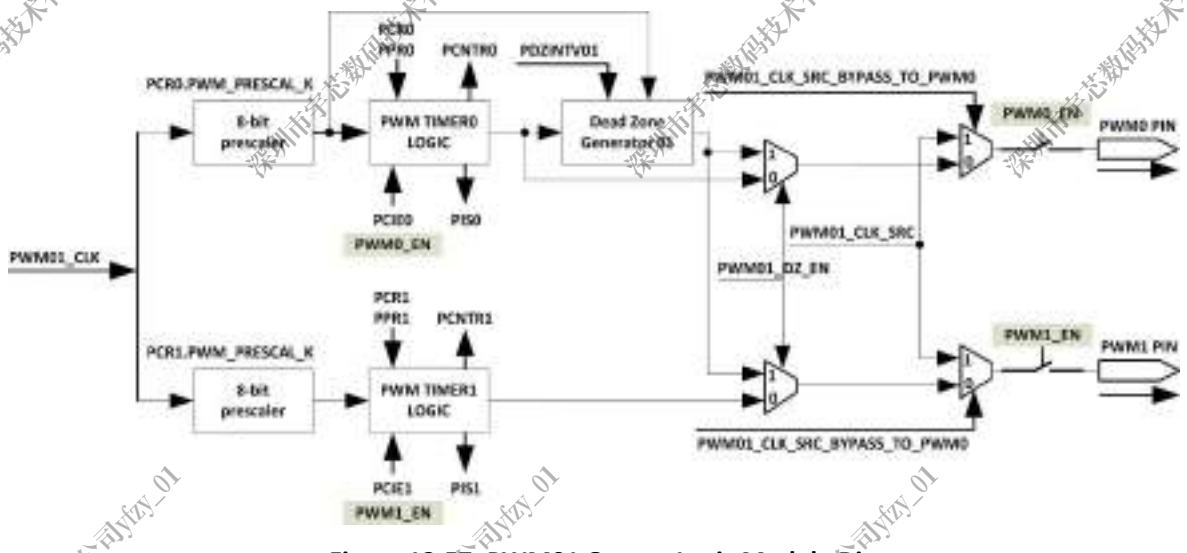


Figure 12-57. PWM01 Output Logic Module Diagram

12.10.3.3. **Up-Counter and Comparator**

The period, duty-cycle and active state of PWM output waveform are decided by the up-counter and comparator. The rule of the comparator is as follows.

PCNTR >= (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “active state”

PCNTR < (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “~ (active state)”

(1) Active state of PWM0 channel is high level (PCR0. PWM_ACT_STA = 1)

When PCNTR0 >= (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1.

When PCNTR0 < (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0.

The formula of PWM output period and duty-cycle is as follows.

T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0. PWM_ENTIRE_CYCLE

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE)

Duty-cycle = (high level time) / (1 period time)

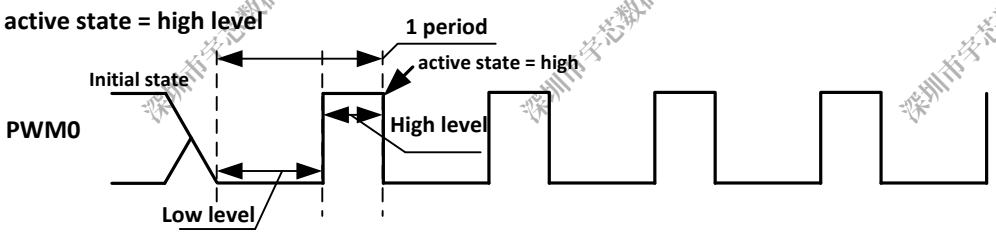


Figure 12-58. PWM0 High Level Active State

(2) Active state of PWM0 channel is low level (PCR0. PWM_ACT_STA = 0)

When PCNTR0 >= (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0.

When PCNTR0 < (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1.

The formula of PWM output period and duty-cycle is as follows.

T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0. PWM_ENTIRE_CYCLE

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE)

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE

Duty-cycle = (low level time) / (1 period time)

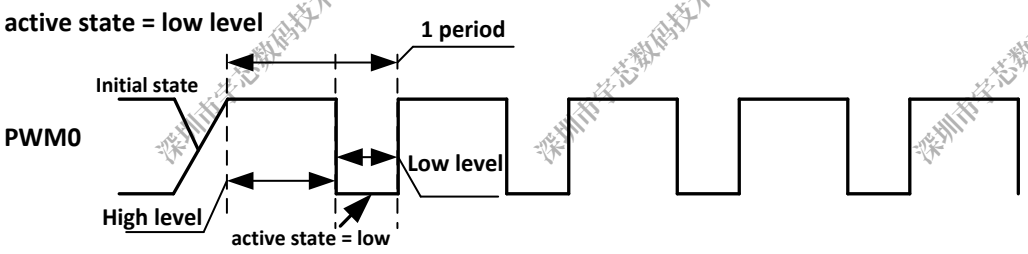


Figure 12-59. PWM0 Low Level Active State

12.10.3.4. **Pulse Mode and Cycle Mode**

PWM output supports pulse mode and cycle mode. PWM in pulse mode outputs one pulse waveform, but PWM in cycle mode outputs continuous waveform.Figure 12-60 shows the PWM output waveform in pulse mode and cycle mode.

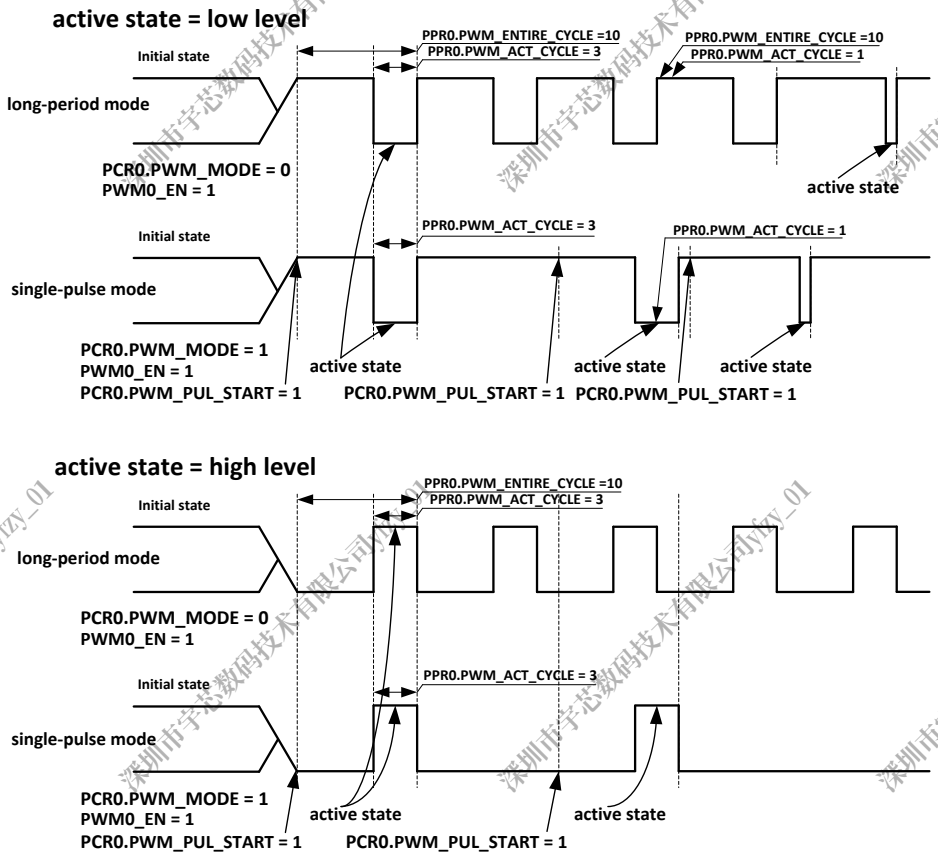


Figure 12-60. PWM0 Output Waveform in Pulse Mode and Cycle Mode

When PCR0.PWM_MODE is 0, PWM0 outputs cycle waveform.The calculating formula of T_{period} and $T_{active\text{-}state}$ is as follows.

T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0. PWM_ENTIRE_CYCLE

$T_{active\ state}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE

When PCR0.PWM_ACT_STA is 0, the active state of cycle waveform is low level.

When PCR0.PWM_ACT_STA is 1, the active state of cycle waveform is high level,

When PCR0.PWM_MODE is 1, PWM0 outputs pulse waveform.The calculating formula of pulse length is as follows.

Pulse length = PWM01_CLK / PWM0_PRESCALE_K * PPR0. PWM _ACT_CYCLE

When PCR0.PWM_ACT_STA is 0, the pulse level is low level, PWM0 channel outputs low pulse.

When PCR0.PWM_ACT_STA is 1, the pulse level is high level, PWM0 channel outputs high pulse.

After PWM0 channel enabled, PCR0. PWM_PUL_START need be set to 1 when PWM0 need output pulse waveform, after completed output, PCR0. PWM_PUL_START can be cleared to 0 by hardware.

The up-counter and comparator for PWM0 channel support cache loading, after PWM0 channel enabled, whether cycle mode or pulse mode, PPR0 value is modified and cached to the buffer register of PPR0 , when the up-counter value reaches PPR0. PWM_ENTIRE_CYCLE , the value in the buffer register will be loaded to up-counter and comparator, namely the value of up-counter and comparator will be overloaded in the next cycle.

Take Figure 12-60(active state =low level) as an example.
In cycle mode, the initial PPR0.PWM_ENTIRE_CYCLE value is 10, the initial PPR0. PWM _ACT_CYCLE value is 3. At some time, the value of PPR0 PPR0. PWM _ACT_CYCLE value is modified to 1, during the current cycle, the modified PPR0 values is cached to PPR0 buffer register, at the beginning of the next cycle, the value of PPR0 buffer register is loaded into up-counter and comparator, then up-counter starts to work.
In pulse mode, the initial value of PPR0. PWM _ACT_CYCLE is 3, in the generation process of a single pulse , the value of PPR0. PWM _ACT_CYCLE is modified to 1,during the current cycle, the modified PPR0 values is cached to PPR0 buffer register, when the value of up-counter reaches PPR0. PWM_ENTIRE_CYCLE, then the pulse waveform output ends,the value of PPR0 buffer register is loaded into up-counter and comparator, at the next time,after PCR0. PWM_PUL_START is set to 1, PPR0 modified value has taken effect.

NOTE

The time that the value of PPR0 buffer register is loaded into up-counter and comparator is very short, which can be ignored, and not affect the PWM output.

12.10.3.5. **Complementary Pair Output**

Every PWM pair supports complementary pair output and PWM pair with dead-time.Figure 12-61 shows the complementary pair output of PWM01.

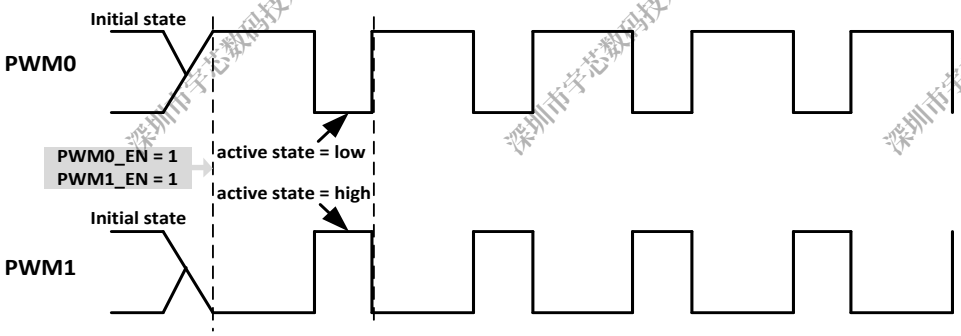


Figure 12-61. PWM01 Complementary Pair Output

The complementary pair output need satisfy the following three conditions:

- The same frequency,the same duty-cycle
- Opposite active state
- Enable two channels of PWM pair at the same time

12.10.3.6. **Dead-time Generator**

Every PWM pair has a programmable dead-time generator.When the dead-time function of PWM pair enabled,PWM01 output waveform is desided by PWM timer logic and DeadZone Generator.Figure 12-62 shows the output waveform.

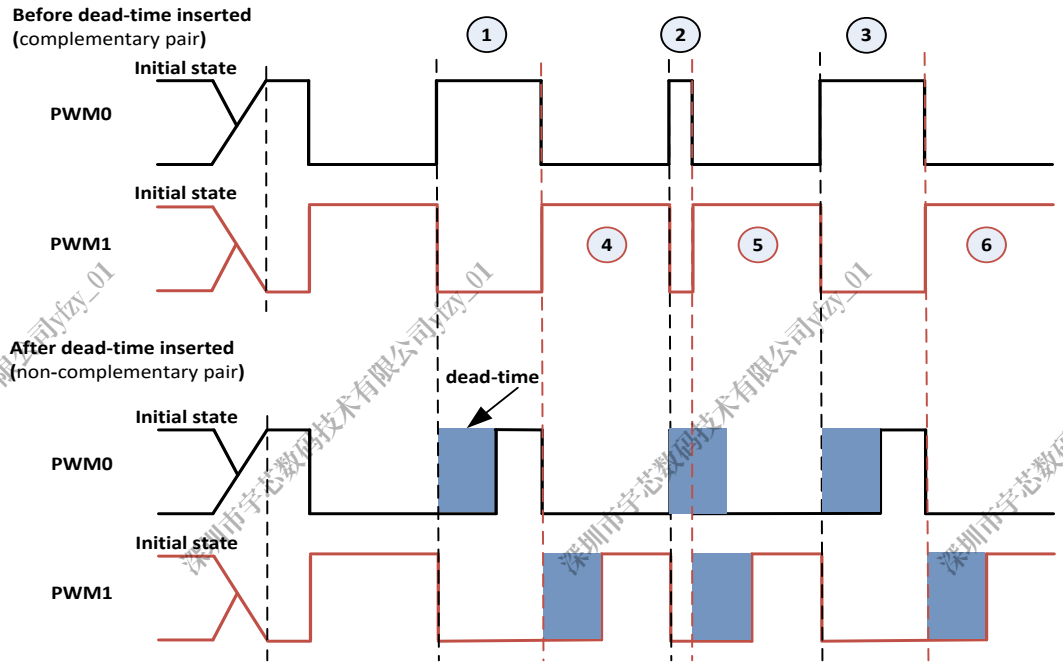


Figure 12-62. Dead-time Output Waveform

Before dead-time inserted: a complementary waveform pair of non-inserted dead-time in Dead Zone Generator 01.
After dead-time inserted: a non-complementary PWM waveform pair inserted dead-time in a complementary waveform pair of Dead Zone Generator 01.The PWM waveform pair at last outputs to PWM0 pin and PWM1 pin.
For complementary pair of Dead Zone Generator 01 ,the principle of inserting dead-time is that to inserte dead-time as soon as the rising edge came. If high level time for mark② in the above figure is less than dead-time,then dead-time will override the high level.The setting of dead-time need consider the period and duty-cycle of output waveform.Dead-time formula is defined as follows:
Dead-time = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PDZINTV01

12.10.3.7. **Capture Input**

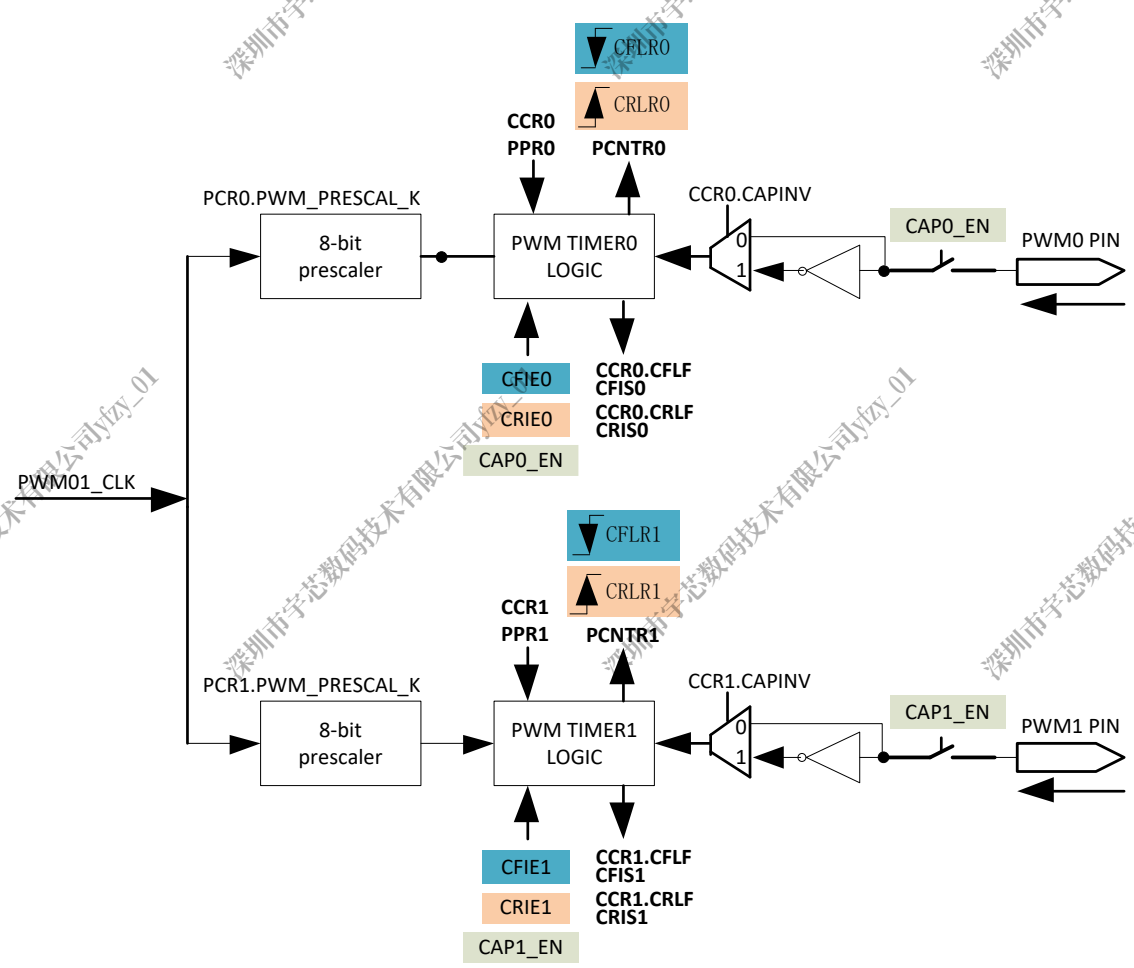


Figure 12-63. PWM01 Capture Logic Module Diagram

Besides the timer logic module of every PWM channel generates PWM output, it can be used to capture rising edge and falling edge of the external clock.Using PWM0 channel as an example,PWM0 channel has one **CFLR** and one **CRLR** for capturing up-counter value in falling edge, in rising edge,respectively.You can calculate the period of external clock by **CFLR** and **CRLR**.

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CRLR0

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CFLR0

$T_{period} = T_{high\text{-}level} + T_{low\text{-}level}$

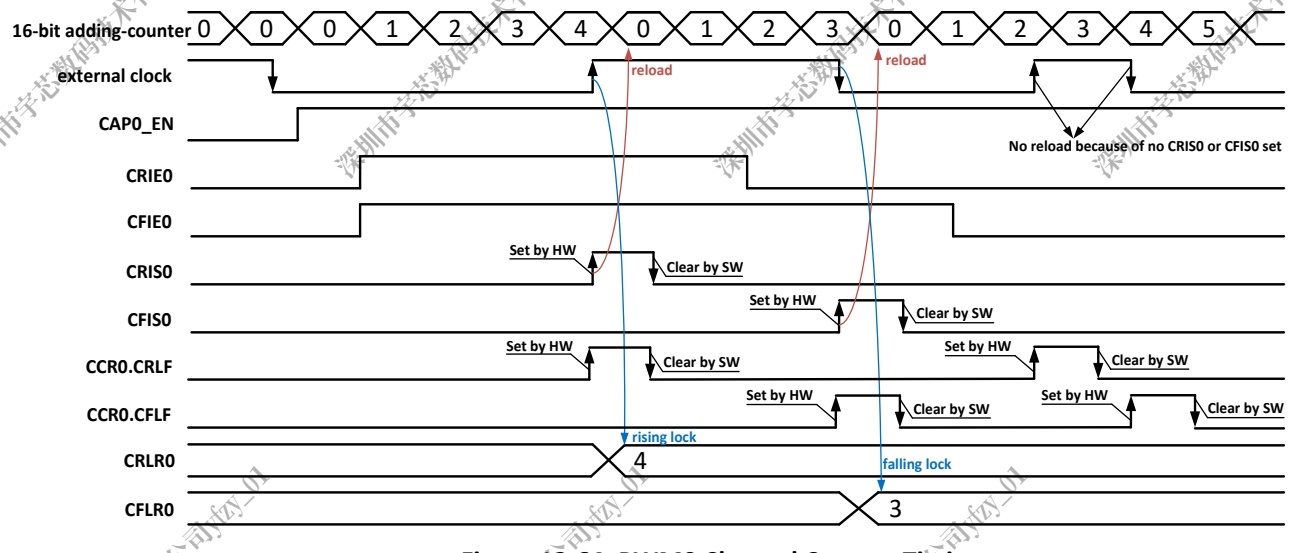


Figure 12-64. PWM0 Channel Capture Timing

When the capture input function of PWM channel is enabled, the up-counter of PWM0 channel starts to work.

when the timer logic module of PWM0 captures one rising edge,the current value of up-counter is locked to **CRLR**, and **CRLF** is set to 1 . If **CRIE0** is 1, then **CRIS0** is set to 1, PWM0 channel sends interrupt request, and the up-counter is loaded to 0 and continues to count. If **CRIE0** is 0, the up-counter is not loaded to 0.

When the timer logic module of PWM0 captures one falling edge, the current value of up-counter is locked to **CFLR**, and **CFLF** is set to 1 . If **CFIE0** is 1, then **CFIS0** is set to 1, PWM0 channel sends interrupt request, and the up-counter is loaded to 0 and continues to count. If **CFIE0** is 0, the up-counter is not loaded to 0.

12.10.3.8. **Interrupt**

PWM supports interrupt generation when PWM channel is configured to PWM output or capture input .

For PWM output function, whether pulse mode or cycle mode, if the value of the up-counter reaches **PWM_ENTIRE_CYCLE**, the timer logic module will automatically set the PIS(PWM Interrupt Status) bit to 1 by hardware. But the PIS bit is cleared by software.

For capture input function, when the timer logic module of the capture channel0 captures rising edge, and **CRIE0** is 1, then **CRIS0** is set to 1; when the timer logic module of the capture channel0 captures falling edge, and **CFIE0** is 1, then **CFIS0** is set to 1.

12.10.4. Register List

Module Name	Base Address
PWM	0x0300A000

Register Name	Offset	Description
PIER	0x0000	PWM IRQ Enable Register
PISR	0x0004	PWM IRQ Status Register
CIER	0x0010	Capture IRQ Enable Register
CISR	0x0014	Capture IRQ Status Register
PCCR01	0x0020	PWM01 Clock Configuration Register

PCCR23	0x0024	PWM23 Clock Configuration Register
PCCR45	0x0028	PWM45 Clock Configuration Register
PCCR67	0x002C	PWM67 Clock Configuration Register
PDZCR01	0x0030	PWM01 Dead Zone Control Register
PDZCR23	0x0034	PWM23 Dead Zone Control Register
PDZCR45	0x0038	PWM45 Dead Zone Control Register
PDZCR67	0x003C	PWM67 Dead Zone Control Register
PER	0x0040	PWM Enable Register
CER	0x0044	Capture Enable Register
PCR	0x0060+0x00+N*0x20(N=0~8)	PWM Control Register
PPR	0x0060+0x04+N*0x20(N=0~8)	PWM Period Register
PCNTR	0x0060+0x08+N*0x20(N=0~8)	PWM Count Register
CCR	0x0060+0x0C+N*0x20(N=0~8)	Capture Control Register
CRLR	0x0060+0x10+N*0x20(N=0~8)	Capture Rise Lock Register
CFLR	0x0060+0x14+N*0x20(N=0~8)	Capture Fall Lock Register
PCCR8	0x0300	PWM8 Clock Configuration Register

12.10.5. Register Description

12.10.5.1. PWM IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0000			Register Name: PWM_IRQ_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	PCIE8 PWM Channel 8 Interrupt Enable 0: PWM channel 8 interrupt disable 1: PWM channel 8 interrupt enable
7	R/W	0x0	PCIE7 PWM Channel 7 Interrupt Enable 0: PWM channel 7 interrupt disable 1: PWM channel 7 interrupt enable
6	R/W	0x0	PCIE6 PWM Channel 6 Interrupt Enable 0: PWM channel 6 interrupt disable 1: PWM channel 6 interrupt enable
5	R/W	0x0	PCIE5 PWM Channel 5 Interrupt Enable 0: PWM channel 5 interrupt disable 1: PWM channel 5 interrupt enable
4	R/W	0x0	PCIE4 PWM Channel 4 Interrupt Enable 0: PWM channel 4 interrupt disable 1: PWM channel 4 interrupt enable

3	R/W	0x0	PCIE3 PWM Channel 3 Interrupt Enable 0: PWM channel 3 interrupt disable 1: PWM channel 3 interrupt enable
2	R/W	0x0	PCIE2 PWM Channel 2 Interrupt Enable 0: PWM channel 2 interrupt disable 1: PWM channel 2 interrupt enable
1	R/W	0x0	PCIE1 PWM Channel 1 Interrupt Enable 0: PWM channel 1 interrupt disable 1: PWM channel 1 interrupt enable
0	R/W	0x0	PCIE0 PWM Channel 0 Interrupt Enable 0: PWM channel 0 interrupt disable 1: PWM channel 0 interrupt enable

12.10.5.2. **PWM IRQ Status Register (Default Value: 0x0000_0000)**

Offset:0x0004			**Register Name: PWM_IRQ_STATUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W1C	0x0	PIS8 PWM Channel 8 Interrupt Status When PWM channel 8 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 8 interrupt is not pending. Reads 1: PWM channel 8 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 8 interrupt status.
7	R/W1C	0x0	PIS7 PWM Channel 7 Interrupt Status When PWM channel 7 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 7 interrupt is not pending. Reads 1: PWM channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 7 interrupt status.
6	R/W1C	0x0	PIS6 PWM Channel 6 Interrupt Status When PWM channel 6 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 6 interrupt is not pending. Reads 1: PWM channel 6 interrupt is pending. Writes 0: No effect.

			Writes 1: Clear PWM channel 6 interrupt status.
5	R/W1C	0x0	PIS5 PWM Channel 5 Interrupt Status When PWM channel 5 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 5 interrupt is not pending. Reads 1: PWM channel 5 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 5 interrupt status.
4	R/W1C	0x0	PIS4 PWM Channel 4 Interrupt Status When PWM channel 4 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 4 interrupt is not pending. Reads 1: PWM channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 4 interrupt status.
3	R/W1C	0x0	PIS3 PWM Channel 3 Interrupt Status When PWM channel 3 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. Reads 1: PWM channel 3 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 3 interrupt status.
2	R/W1C	0x0	PIS2 PWM Channel 2 Interrupt Status When PWM channel 2 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending. Reads 1: PWM channel 2 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 2 interrupt status.
1	R/W1C	0x0	PIS1 PWM Channel 1 Interrupt Status When PWM channel 1 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. Reads 1: PWM channel 1 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0 PWM Channel 0 Interrupt Status When PWM channel 0 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending.

			Reads 1: PWM channel 0 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 0 interrupt status.

12.10.5.3. **PWM Capture IRQ Enable Register (Default Value: 0x0000_0000)**

Offset:0x0010			Register Name: PWM_CAPTURE_IRQ_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	CFIE8 If the bit is set 1, when capturing channel 8 captures falling edge, it generates a capturing channel 8 pending. 0: Capturing channel 8 fall lock interrupt disable 1: Capturing channel 8 fall lock interrupt enable.
16	R/W	0x0	CRIE8 If the bit is set 1, when capturing channel 8 captures rising edge, it generates a capturing channel 8 pending. 0: Capturing channel 8 rise lock interrupt disable 1: Capturing channel 8 rise lock interrupt enable.
15	R/W	0x0	CFIE7 If the bit is set 1, when capturing channel 7 captures falling edge, it generates a capturing channel 7 pending. 0: Capturing channel 7 fall lock interrupt disable 1: Capturing channel 7 fall lock interrupt enable.
14	R/W	0x0	CRIE7 If the bit is set 1, when capturing channel 7 captures rising edge, it generates a capturing channel 7 pending. 0: Capturing channel 7 rise lock interrupt disable 1: Capturing channel 7 rise lock interrupt enable.
13	R/W	0x0	CFIE6 If the bit is set 1, when capturing channel 6 captures falling edge, it generates a capturing channel 6 pending. 0: Capturing channel 6 fall lock interrupt disable 1: Capturing channel 6 fall lock interrupt enable.
12	R/W	0x0	CRIE6 If the bit is set 1, when capturing channel 6 captures rising edge, it generates a capturing channel 6 pending. 0: Capturing channel 6 rise lock interrupt disable 1: Capturing channel 6 rise lock interrupt enable.
11	R/W	0x0	CFIE5 If the bit is set 1, when capturing channel 5 captures falling edge, it generates a capturing channel 5 pending. 0: Capturing channel 5 fall lock interrupt disable 1: Capturing channel 5 fall lock interrupt enable.
10	R/W	0x0	CRIE5

			If the bit is set 1, when capturing channel 5 captures rising edge, it generates a capturing channel 5 pending. 0: Capturing channel 5 rise lock interrupt disable 1: Capturing channel 5 rise lock interrupt enable.
9	R/W	0x0	CFIE4 If the bit is set 1, when capturing channel 4 captures falling edge, it generates a capturing channel 4 pending. 0: Capture channel 4 fall lock interrupt disable 1: Capture channel 4 fall lock interrupt enable.
8	R/W	0x0	CRIE4 If the bit is set 1, when capturing channel 4 captures rising edge, it generates a capturing channel 4 pending. 0: Capturing channel 4 rise lock interrupt disable 1: Capturing channel 4 rise lock interrupt enable.
7	R/W	0x0	CFIE3 If the bit is set 1, when capturing channel 3 captures falling edge, it generates a capturing channel 3 pending. 0: Capturing channel 3 fall lock interrupt disable 1: Capturing channel 3 fall lock interrupt enable.
6	R/W	0x0	CRIE3 If the bit is set 1, when capturing channel 3 captures rising edge, it generates a capturing channel 3 pending. 0: Capturing channel 3 rise lock interrupt disable 1: Capturing channel 3 rise lock interrupt enable.
5	R/W	0x0	CFIE2 If the bit is set 1, when capturing channel 2 captures falling edge, it generates a capturing channel 2 pending. 0: Capturing channel 2 fall lock interrupt disable 1: Capturing channel 2 fall lock interrupt enable.
4	R/W	0x0	CRIE2 If the bit is set 1, when capturing channel 2 captures rising edge, it generates a capturing channel 2 pending. 0: Capturing channel 2 rise lock interrupt disable 1: Capturing channel 2 rise lock interrupt enable.
3	R/W	0x0	CFIE1 If the bit is set 1, when capturing channel 1 captures falling edge, it generates a capturing channel 1 pending. 0: Capturing channel 1 fall lock interrupt disable 1: Capturing channel 1 fall lock interrupt enable.
2	R/W	0x0	CRIE1 If the bit is set 1, when capturing channel 1 captures rising edge, it generates a capturing channel 1 pending. 0: Capturing channel 1 rise lock interrupt disable 1: Capturing channel 1 rise lock interrupt enable.
1	R/W	0x0	CFIE0 If the bit is set 1, when capturing channel 0 captures falling edge, it

			generates a capturing channel 0 pending. 0: Capturing channel 0 fall lock interrupt disable 1: Capturing channel 0 fall lock interrupt enable.
0	R/W	0x0	CRIE0 If the bit is set 1, when capturing channel 0 captures rising edge, it generates a capturing channel 0 pending. 0: Capturing channel 0 rise lock interrupt disable 1: Capturing channel 0 rise lock interrupt enable.

12.10.5.4. **PWM Capture IRQ Status Register (Default Value: 0x0000_0000)**

Offset:0x0014			**Register Name: PWM_CAPTURE_IRQ_STATUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	CFIS8 Capturing channel 8 falling lock interrupt status. When capturing channel 8 captures falling edge, if capturing channel 8 fall lock interrupt (**CFIE8**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 8 interrupt is not pending. Reads 1: Capturing channel 8 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 8 interrupt status.
16	R/W1C	0x0	CRIS8 Capturing channel 8 rising lock interrupt status. When capturing channel 8 captures rising edge, if capturing channel 8 rise lock interrupt (**CRIE8**) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capturing channel 8 interrupt is not pending. Reads 1: Capturing channel 8 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 8 interrupt status.
15	R/W1C	0x0	CFIS7 Capturing channel 7 falling lock interrupt status. When capturing channel 7 captures falling edge, if capturing channel 7 fall lock interrupt (**CFIE7**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 7 interrupt is not pending. Reads 1: Capturing channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 7 interrupt status.
14	R/W1C	0x0	CRIS7 Capturing channel 7 rising lock interrupt status. When capturing channel 7 captures rising edge, if capturing channel 7 rise lock interrupt (**CRIE7**) is enabled, this bit is set 1 by hardware. Write 1 to

			clear this bit. Reads 0: Capturing channel 7 interrupt is not pending. Reads 1: Capturing channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 7 interrupt status.
13	R/W1C	0x0	CFIS6 Capturing channel 6 falling lock interrupt status. When capturing channel 6 captures falling edge, if capturing channel 6 fall lock interrupt (**CFIE6**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 6 interrupt is not pending. Reads 1: Capturing channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 6 interrupt status.
12	R/W1C	0x0	CRIS6 Capturing channel 6 rising lock interrupt status. When capturing channel 6 captures rising edge, if capturing channel 6 rise lock interrupt (**CRIE6**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capturing channel 6 interrupt is not pending. Reads 1: Capturing channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 6 interrupt status.
11	R/W1C	0x0	CFIS5 Capturing channel 5 falling lock interrupt status. When capturing channel 5 captures falling edge, if capturing channel 5 fall lock interrupt (**CFIE5**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 5 interrupt is not pending. Reads 1: Capturing channel 5 interrupt is pending. Writes 0: No effect. Reads 1: Clear capturing channel 5 interrupt status.
10	R/W1C	0x0	CRIS5 Capturing channel 5 rising lock interrupt status. When capturing channel 5 captures rising edge, if capturing channel 5 rise lock interrupt (**CRIE5**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capturing channel 5 interrupt is not pending. Reads 1: Capturing channel 5 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 5 interrupt status.
9	R/W1C	0x0	CFIS4 Capturing channel 4 falling lock interrupt status. When capturing channel 4 captures falling edge, if capturing channel 4 fall lock interrupt (**CFIE4**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit.

			Reads 0: Capturing channel 4 interrupt is not pending. Reads 1: Capturing channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 4 interrupt status.
8	R/W1C	0x0	CRIS4 Capturing channel 4 rising lock interrupt status. When capturing channel 4 captures rising edge, if capturing channel 4 rise lock interrupt (**CRIE4**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capturing channel 4 interrupt is not pending. Reads 1: Capturing channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 4 interrupt status.
7	R/W1C	0x0	CFIS3 Capture channel 3 falling lock interrupt status. When capture channel 3 captures falling edge, if capture channel 3 fall lock interrupt (**CFIE3**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 3 interrupt status.
6	R/W1C	0x0	CRIS3 Capture channel 3 rising lock interrupt status. When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (**CRIE3**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2 Capture channel 2 falling lock interrupt status. When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (**CFIE2**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. Reads 1: Capture channel 2 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 2 interrupt status.
4	R/W1C	0x0	CRIS2 Capture channel 2 rising lock interrupt status. When capture channel 2 captures rising edge, if capture channel 2 rise lock interrupt (**CRIE2**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending.

			Reads 1: Capture channel 2 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 2 interrupt status.
3	R/W1C	0x0	CFIS1 Capture channel 1 falling lock interrupt status. When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (**CFIE1**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 1 interrupt status.
2	R/W1C	0x0	CRIS1 Capture channel 1 rising lock interrupt status. When capture channel 1 captures rising edge, if capture channel 1 rise lock interrupt (**CRIE1**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 1 interrupt status.
1	R/W1C	0x0	CFIS0 Capture channel 0 falling lock interrupt status. When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (**CFIE0**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 0 interrupt status.
0	R/W1C	0x0	CRIS0 Capture channel 0 rising lock interrupt status. When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (**CRIE0**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 0 interrupt status.

12.10.5.5. PWM01 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: PWM01_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/

8:7	R/W	0x0	PWM01_CLK_SRC Select PWM01 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6	R/W	0x0	PWM01_CLK_SRC_BYPASS_TO_PWM1 Bypass PWM01 Clock Source to PWM1 Output 0: Not bypass 1: Bypass
5	R/W	0x0	PWM01_CLK_SRC_BYPASS_TO_PWM0 Bypass PWM01 Clock Source to PWM0 Output 0: Not bypass 1: Bypass
4	R/W	0x0	PWM01_CLK_GATING Gating Clock for PWM01 0: Mask 1: Pass
3:0	R/W	0x0	PWM01_CLK_DIV_M PWM01 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

12.10.5.6. **PWM23 Clock Configuration Register (Default Value: 0x0000_0000)**

Offset:0x0024			**Register Name: PWM23_CLOCK_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM23_CLK_SRC_SEL Select PWM23 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6	R/W	0x0	PWM23_CLK_SRC_BYPASS_TO_PWM3 Bypass PWM23 Clock Source to PWM3 Output 0: Not bypass 1: Bypass
5	R/W	0x0	PWM23_CLK_SRC_BYPASS_TO_PWM2

			Bypass PWM23 Clock Source to PWM2 Output 0: Not bypass 1: Bypass
4	R/W	0x0	PWM23_CLK_GATING Gating Clock for PWM23 0: Mask 1: Pass
3:0	R/W	0x0	PWM23_CLK_DIV_M PWM23 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

12.10.5.7. **PWM45 Clock Configuration Register (Default Value: 0x0000_0000)**

Offset:0x0028			**Register Name: PWM45_CLOCK_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM45_CLK_SRC_SEL Select PWM45 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6	R/W	0x0	PWM45_CLK_SRC_BYPASS_TO_PWM5 Bypass PWM45 Clock Source to PWM5 Output 0: Not bypass 1: Bypass
5	R/W	0x0	PWM45_CLK_SRC_BYPASS_TO_PWM4 Bypass PWM45 Clock Source to PWM4 Output 0: Not bypass 1: Bypass
4	R/W	0x0	PWM45_CLK_GATING Gating Clock for PWM45 0: Mask 1: Pass
3:0	R/W	0x0	PWM45_CLK_DIV_M PWM45 Clock Divide M 0000: /1

			0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

12.10.5.8. **PWM67 Clock Configuration Register (Default Value: 0x0000_0000)**

Offset:0x002C			**Register Name: PWM67_CLOCK_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM67_CLK_SRC_SEL Select PWM67 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6	R/W	0x0	PWM67_CLK_SRC_BYPASS_TO_PWM7 Bypass PWM67 Clock Source to PWM7 Output 0: Not bypass 1: Bypass
5	R/W	0x0	PWM67_CLK_SRC_BYPASS_TO_PWM6 Bypass PWM67 Clock Source to PWM6 Output 0: Not bypass 1: Bypass
4	R/W	0x0	PWM67_CLK_GATING Gating Clock for PWM67 0: Mask 1: Pass
3:0	R/W	0x0	PWM67_CLK_DIV_M PWM67 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

12.10.5.9. **PWM01 Dead Zone Control Register (Default Value: 0x0000_0000)**

Offset:0x0030			Register Name: PWM01_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM01_DZ_INTV PWM01 Dead Zone Interval Value
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN PWM01 Dead Zone Enable 0: Dead Zone disable 1: Dead Zone enable

12.10.5.10. **PWM23 Dead Zone Control Register (Default Value: 0x0000_0000)**

Offset:0x0034			Register Name: PWM23_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0x0	PWM23_DZ_INTV PWM23 Dead Zone Interval Value
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN PWM23 Dead Zone Enable 0: Dead Zone disable 1: Dead Zone enable

12.10.5.11. **PWM45 Dead Zone Control Register (Default Value: 0x0000_0000)**

Offset:0x0038			Register Name: PWM45_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0x0	PWM45_DZ_INTV PWM45 Dead Zone Interval Value
7:1	/	/	/
0	R/W	0x0	PWM45_DZ_EN PWM45 Dead Zone Enable 0: Dead Zone disable 1: Dead Zone enable

12.10.5.12. **PWM67 Dead Zone Control Register (Default Value: 0x0000_0000)**

Offset:0x003C			Register Name: PWM67_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0x0	PWM67_DZ_INTV PWM67 Dead Zone Interval Value

7:1	/	/	/
0	R/W	0x0	PWM67_DZ_EN PWM67 Dead Zone Enable 0: Dead Zone disable 1: Dead Zone enable

12.10.5.13. **PWM Enable Register (Default Value: 0x0000_0000)**

Offset:0x0040			**Register Name: PWM_ENABLE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	PWM8_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel8 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
7	R/W	0x0	PWM7_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel7 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
6	R/W	0x0	PWM6_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel6 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
5	R/W	0x0	PWM5_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel5 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
4	R/W	0x0	PWM4_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel4 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
3	R/W	0x0	PWM3_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel3 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
2	R/W	0x0	PWM2_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel2 is permitted to output PWM waveform. 0: PWM disable

			1: PWM enable
1	R/W	0x0	PWM1_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel1 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
0	R/W	0x0	PWM0_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel0 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable

12.10.5.14. **PWM Capture Enable Register (Default Value: 0x0000_0000)**

Offset:0x0044			**Register Name: PWM_CAPTURE_ENABLE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	CAP8_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel8 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
7	R/W	0x0	CAP7_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel7 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
6	R/W	0x0	CAP6_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel6 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
5	R/W	0x0	CAP5_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel5 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
4	R/W	0x0	CAP4_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel4 is permitted to capture external falling edge or rising edge.

			0: Capture disable 1: Capture enable
3	R/W	0x0	CAP3_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
2	R/W	0x0	CAP2_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
1	R/W	0x0	CAP1_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
0	R/W	0x0	CAP0_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel0 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

12.10.5.15. **PWM Control Register (Default Value: 0x0000_0000)**

Offset:0x0060+0x0+N*0x20(N=0~8)			**Register Name: PWM_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R	0x0	PWM_PERIOD_RDY PWM Period Register Ready 0: PWM period register is ready to write 1: PWM period register is busy
10	R/W1S	0x0	PWM_PUL_START PWM Pulse Output Start 0: No effect 1: Output 1 pulse After finishing configuration for outputting pulse, set this bit once and then PWM would output one pulse. After the pulse is finished, the bit will be cleared automatically.
9	R/W	0x0	PWM_MODE PWM Output Mode Select

			0: Cycle mode 1: Pulse mode
8	R/W	0x0	PWM_ACT_STA PWM Active State 0: Low Level 1: High Level
7:0	R/W	0x0	PWM_PRESCAL_K PWM pre-scale K, actual pre-scale is (K+1). K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 ..... K = 255, actual pre-scale: 256

12.10.5.16. **PWM Period Register**

Offset:0x0060+0x04+N*0x20(N=0~8)			**Register Name: PWM_PRD_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	PWM_ENTIRE_CYCLE Number of the entire cycles in the PWM clock. 0: 1 cycle 1: 2 cycles … N: N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK.
15:0	R/W	UDF	PWM_ACT_CYCLE Number of the active cycles in the PWM clock. 0: 0 cycle 1: 1 cycle … N: N cycles

12.10.5.17. **PWM Counter Register**

Offset:0x0060+0x08+N*0x20(N=0~8)			**Register Name: PWM_CTR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	UDF	PWM output or capture input. The field indicates the current value of the PWM 16-bit up-counter.

12.10.5.18. **PWM Capture Control Register (Default Value: 0x0000_0000)**

Offset:0x0060+0x0C+N*0x20(N=0~8)			Register Name: PWM_CAPTURE_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	CRLF When capturing channel captures the rising edge,the current value of the 16-bit up-counter is latched to **CRLR** and the bit is set to 1 by hardware.Writing 1 to clear the bit.
1	R/W1C	0x0	CFLF When capturing channel captures the falling edge,the current value of the 16-bit up-counter is latched to **CFLR** and the bit is set to 1 by hardware.Writing 1 to clear the bit.
0	R/W	0x0	CAPINV Inversing the input signal from the capturing channel before the 16-bit counter of the capturing channel. 0: Not inverse 1: Inverse

12.10.5.19. **PWM Capture Rise Lock Register**

Offset:0x0060+0x10+N*0x20(N=0~8)			Register Name: PWM_CAPTURE_RISE_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	UDF	CRLR When the capturing channel captures the rising edge,the current value of the 16-bit up-counter is latched to the register.

12.10.5.20. **PWM Capture Fall Lock Register**

Offset:0x0060+0x14+N*0x20(N=0~7)			Register Name: PWM_CAPTURE_FALL_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	UDF	CFLR When the capturing channel captures the falling edge,the current value of the 16-bit up-counter is latched to the register.

12.10.5.21. **PWM8 Clock Configuration Register (Default Value: 0x0000_0000)**

Offset:0x0300			Register Name: PWM8_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM8_CLK_SRC_SEL

			Select PWM8 clock source 00: OSC24M 01: APB1 Others: /
6	/	/	/
5	R/W	0x0	PWM8_CLK_ BYPASS Bypass clock source to PWM8 output 0: Not bypass 1: Bypass
4	R/W	0x0	PWM8_CLK_GATING Gating clock for PWM8 0: Mask 1: Pass
0:3	R/W	0x0	PWM8_CLK_DIV_M PWM8 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

Chapter 13 Security System

13.1. Crypto Engine

13.1.1. Overview

The Crypto Engine(CE) module is one encryption/decryption algorithms accelerator. It supports kinds of symmetric, asymmetric, HASH, and RNG algorithms. There are two software interfaces for secure and non-secure world each. Algorithm control information is written in memory by task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels each world, and has an internal DMA controller to transfer data between CE and memory. It supports parallel running for symmetric, HASH, asymmetric algorithms.

The CE has the following features:

- Supports Symmetrical Algorithm: AES, DES, 3DES, XTS.
- Supports Hash Algorithms: MD5, SHA, HMAC.
- Supports Public Key Algorithms: RSA, ECC.
- Supports RNG Algorithms: PRNG, TRNG.
- Supports 128-bit, 192-bit and 256-bit key size for AES
- Supports 256-bit, 512-bit key for XTS
- AES supports ECB, CBC, CTR, CTS, CFB, OFB, CBC-MAC modes.
- AES-CFB mode supports CFB1, CFB8, CFB64, CFB128
- AES-CTR supports CTR16, CTR32, CTR64, CTR128
- DES supports ECB, CBC, CTR, CBC-MAC mode
- DES-CTR supports CTR16, CTR32, CTR64 mode
- Supports SHA1, SHA224, SHA256, SHA384, SHA512 for SHA. Supports HMAC-SHA1, HMAC-SHA256 for HMAC. Supports multi-package mode for these ones
- MD5, SHA, HMAC are padded using hardware, if not last package, input should aligned with computation block, namely 512bits or 1024bits
- RSA supports 512/1024/2048/3072/4096 bit width
- ECC supports 160/224/256/384/521 width
- Supports 160-bits hardware PRNG with 175 bits seed. Output aligns with 5 words
- Supports 256-bits hardware TRNG. Post-process SHA256 is added after sample, HASH value used as next's IV input. Output aligns with 8 words
- Supports secure and non-secure interfaces respectively, each world issues task request through its own interface, don't know each other's existence
- Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other
- Supports task chain mode for each request. Task or task chain are executed at request order

- Symmetric, asymmetric, HASH ctrl logics are separate, can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time.
- 8 scatter group(sg) are supported for both input and output data. sg size is input/output word number. DMA reads and write at word aligned.
- DMA has multiple channel, each corresponding to one suit of algorithms.

13.1.2. Block Diagram

The following figure shows the block diagram of Crypto Engine.

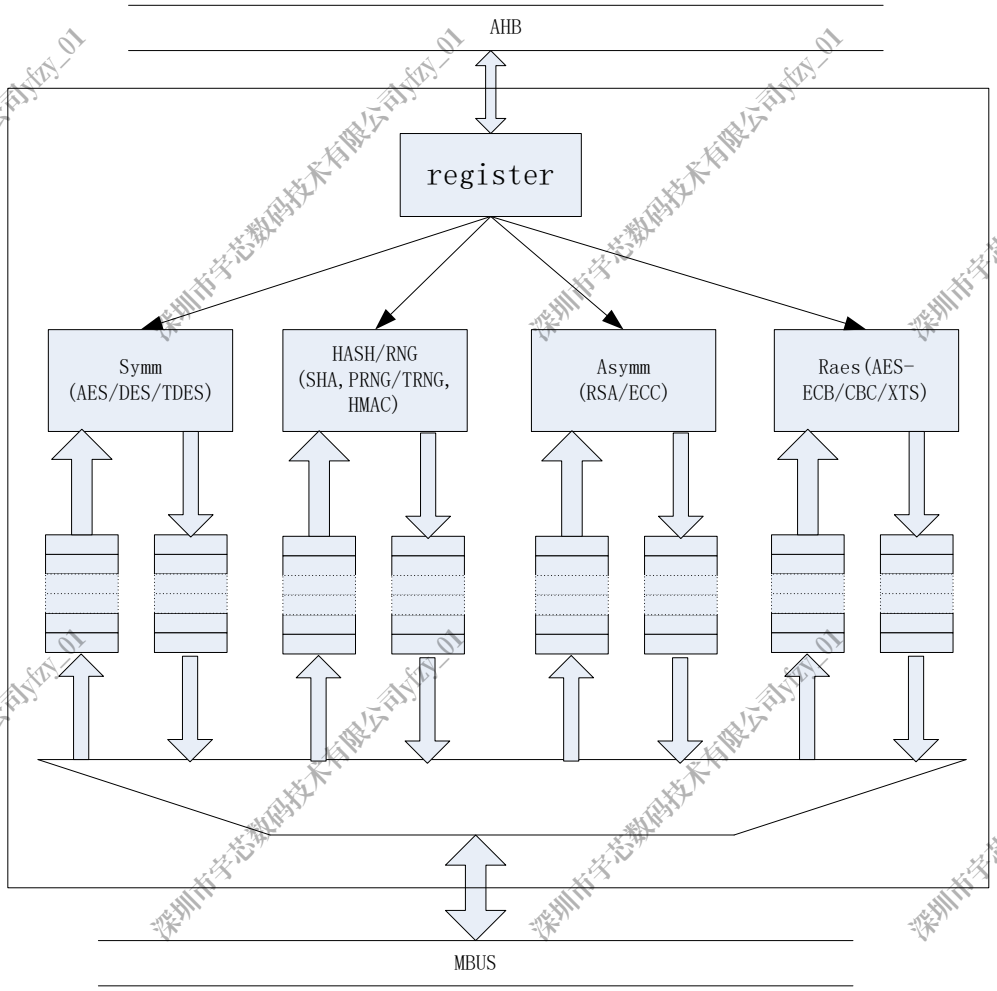


Figure 13-1. CE Block Diagram

13.1.3. Operations and Functional Descriptions

13.1.3.1. **Task Descriptor**

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination address and size, etc. The task descriptor is as follows.

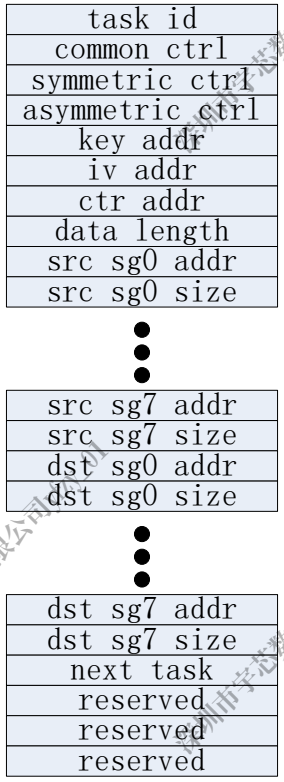


Figure 13-2. Task Chaining

Task chaining id supports 0~3.

13.1.3.2. **Task Descriptor Queue Common Control**

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	Interrupt enable for current task 0: disable interrupt 1: enable interrupt
30:17	/	/	/
16	R/W	0x0	IV mode IV mode for SHA1/SHA224/SHA256/SHA384/SHA512/MD5 or constants 0: use initial constants defined in FIPS-180 1: use input iv
15	R/W	0x0	HASH/HMAC plaintext last 0: not the last HASH/HMAC plaintext package, need not padding 1: the last HASH/HMAC plaintext package, need to padding
14:9	/	/	/
8	R/W	0x0	OP DIR Algorithm Operation Direction 0: Encryption 1: Decryption
7	/	/	/
6:0	R/W	0x0	Algorithm type 0x0: AES

			0x1: DES 0x2: Triple DES (3DES) 0x3~0xf: reserved 0x10: MD5 0x11: SHA-1 0x12: SHA-224 0x13: SHA-256 0x14: SHA-384 0x15: SHA-512 0x16: HMAC-SHA1 0x17: HMAC-SHA256 0x18~0x1b: reserved 0x1c: TRNG 0x1d: PRNG others: reserved 0x20: RSA 0x21: ECC others: reserved 0x30: RAES Others: reserved

13.1.3.3. **Task Descriptor Queue Symmetric Control**

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	KEY_SELECT key select for AES 0000: Select input CE_KEYx (Normal Mode) 0001: Select {SSK} 0010: Select {HUK} 0011: Select {RSSK} 0100-0111: Reserved 1000-1111: Select internal Key n (n from 0 to 7)
19:18	R/W	0x0	CFB_WIDTH For AES-CFB width 00: CFB1 01: CFB8 10: CFB64 11: CFB128
17	R/W	0x0	PRNG_LD Load new 15bits key into lfsr for PRNG
16	R/W	0x0	AES CTS last package flag

			When set to '1', it means this is the last package for AES-CTS mode(the size of the last package >128bit).
15:14	/	/	/
13	R/W	0	xts_last 0: not last block for XTS 1: last block for XTS
12	R/W	0	xts_first 0: not first block for XTS 1: first block for XTS
11:8	R/W	0x0	ALGORITHM_MODE CE algorithm mode 0000: Electronic Code Book (ECB) mode 0001: Cipher Block Chaining (CBC) mode 0010: Counter (CTR) mode 0011: CipherText Stealing (CTS) mode 0100: Output feedback (OFB)mode 0101: Cipher feedback (CFB)mode 0110: CBC-MAC mode 1001: XTS mode Other: Reserved
7:4	/	/	/
3:2	R/W	0x0	CTR WIDTH Counter Width for CTR Mode 00: 16-bit Counter 01: 32-bit Counter 10: 64-bit Counter 11: 128-bit Counter
1:0	R/W	0x0	AES KEY SIZE 00: 128-bit 01: 192-bit 10: 256-bit 11: Reserved

13.1.3.4. Task Descriptor Queue Asymmetric Control

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	PKC algorithm mode. For modular computation: 00000: modular exponent(RSA) 00001: modular add 00010: modular minus 00011: modular multiplication others: reserved

			For ECC: 00000: point add 00001: point double 00010: point multiplication 00011: point verification 00100: encryption 00101: decryption 00110: sign 00111: sign verify others: reserved
15:8	/	/	/
7:0	R/W	0	Asymmetric algorithms operation width field. It indicates how much width this request apply, as words.

NOTE

key addr field is address for each algorithm's key, and for HASH's total length address when last package, also for extension feature micro codes address. when indicate HASH's total length address,it must be 64bit data length with 64bit address align.

iv addr field is address for IV or modulus, or tweak value address for XTS.

ctr addr is address for next block's IV, and for HMAC K1 address.

src/dst sgX addr field indicate 32bit address for source and destination data.

src/dst sgX size field indicates size for each sg respectively

next task field should be set to 0 when no next task, else set to next task's descriptor.

13.1.3.5. **Task Request**

Basically, there are 4 steps for one task handling from software.

Step1: software should configure task descriptor in memory, including all fields in descriptor. Channel id corresponds to one channel in CE, from 0 to 3 for secure and non secure world respectively. According to algorithm type, software should set the fields in common control, symmetric control, asymmetric control, then provide key/iv/ctr address and this task's data length. Source and destination sg address and size are set based on upper application. If there is another task concatenating after this task, then set it's descriptor address at next descriptor field.

Step 2: Software should set registers, including task descriptor address, interrupt control.

Step 3: Software reads load register to ensure that the bit0 is zero, then starts request by pulling up the bit0 of the load register.

Step 4: Wait task end.

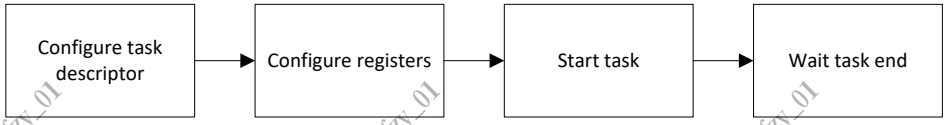


Figure 13-3. Task Request Process

13.1.3.6. Data Length Setting

For HASH algorithms, data length field indicates valid source data bit number, for others indicates source data byte number.
For PRNG, data length should be 20 byte aligned.
For TRNG should be 32 byte aligned.
For HASH algorithms data length should be 512/1024bit aligned if current request is not the last data block, because of hardware padding.
Data size in source and destination sg is as words, whose value should corresponds with data length field, or else CE will report error and stop execution.

13.1.3.7. Security Operation

When CPU issues request to CE module, CE module will save CPU's secure mode. When executing this request, this state bit works as access tag for inner and system resource. For HUK/RSSK/SSK from SID, only secure mode can access, or else these keys will be used as 0. For access to SID and keysram module through AHB bus, only secure mode can success, or else will read 0 or can not write. When issuing MBUS read and write requests, CE will use send this secure mode bit to BUS, so secure request can access secure and non secure space, but non secure request only can access non secure space.

13.1.3.8. Task Parallel

Algorithms are divided into 3 types: symmetric, HASH/RNG, asymmetric. Each type has a task queue with 8 elements for requests. Tasks in each queue are handled in sequence. Among these 3 types, task request and complete time are not sure. If one type uses the outcome of another type, software should make sure that start one type after another type is finished.
CE supports 4 channels in each world, and 3 suits algorithm type which can run in parallel. When software issues request, it first checks if load bit is low which means software can request. If load bit is high which means last request is not registered by CE, software should wait until load bit is low. If software makes several requests with the same type, these tasks will be executed in request sequence. If software makes several requests with different types, these tasks will be executed in parallel. Because parallel tasks would finish out of order, software should make different type request with different channel id, which results in generating different interrupt status bit.

13.1.3.9. PKC Microcode

PKC module supports RSA, ECC asymmetric algorithms in the form of microcode. It implements basic modular add, minus, multiplication, point add, point double, and logic computing, etc. Complete RSA/ECC encryption, decryption, sign, verify are implemented with these microcode.
Asymmetric algorithms RSA/ECC are implemented as microcode in PKC module. Asymmetric encryption, decryption, sign, verify operations are composed with certain fixed microcode with hardware.

13.1.3.10. PKC Configuration

Before starting PKC, task description must be configured. Parameters to PKC are assigned to source sg, outcome is put to

destination sg.

For RSA, parameters should be at the order of key, modulus, plaintext.

For ECC point add P2 = P0 + P1, parameters should be at the order of p, P0x, P0y, P1x, P1y. Output is at the order of P2x, P2y.

For ECC point double P2 = 2*P0, parameters should be at the order of p, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point multiplication P2 = k*P0, parameters should be at the order of p, k, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point verification, parameters should be at the order of p, a, P0x, P0y, b. Output is 1 or 0.

For ECC encryption, parameters should be at the order of random k, p, a, Gx, Gy, Qx, Qy, m. Output is at the order of Rx, Ry, c.

For ECC decryption, parameters should be at the order of random k, p, a, Rx, Ry, c. Output is m.

For ECC signature, parameters should be at the order of random k, p, a, Gx, Gy, n, d, e. Output is at the order of r, s.

For ECC signature verification, parameters should be at the order of n, s, e, r, p, a, Gx, Gy, Qx, Qy, n, r. Output is 1 or 0.

13.1.3.11. **Error Check**

CE module includess error detection for task configuration, data computing error, and authentication invalid. When algorithm type in task description is read into module, CE will check if this type is supported through checking algorithm type field in common ctrl. If type value accede support scope, CE will issue interrupt signal and set error state. Each type has certain input and output data size. After getting task descriptor, input size and output size configuration will be checked to avoid size error. If size configuration is wrong, CE will issue interrupt signal and set error state. To protect keys would be put into keysram from disclose, if request using RSSK is for AES decryption and destination address is not in keysram space, CE would not execute this task. It will issue interrupt signal and set error state.

13.1.3.12. **Clock Requirement**

Clock Name	Description	Requirement
ahb_clk	AHB bus clock	24MHz - 200MHz
m_clk	MBUS clk	24MHz - 400MHz
ce_clk	CE work clock	24MHz - 300MHz

13.1.4. Register List

Module Name	Base Address
CE_NS	0x01904000
CE_S	0x01904800

Register Name	Offset	Description
CE_TDA	0x00	Task Descriptor Address
CE_ICR	0x08	Interrupt Control Register
CE_ISR	0x0C	Interrupt Status Register
CE_TLR	0x10	Task Load Register

CE_TSR	0x14	Task Status Register
CE_ESR	0x18	Error Status Register
CE_SCSA	0x24	Symmetric Algorithm DMA Current Source Address
CE_SCDA	0x28	Symmetric Algorithm DMA Current Destination Address
CE_HCSA	0x34	HASH Algorithm DMA Current Source Address
CE_HCDA	0x38	HASH Algorithm DMA Current Destination Address
CE_ACSA	0x44	Asymmetric Algorithm DMA Current Source Address
CE_ACDA	0x48	Asymmetric Algorithm DMA Current Destination Address
CE_XCSA	0x54	XTS Algorithm DMA Current Source Address
CE_XCDA	0x58	XTS Algorithm DMA Current Destination Address

13.1.5. Register Description

13.1.5.1. CE Task Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Task Descriptor Address

13.1.5.2. CE Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	Task Channel3~0 Interrupt Enable 0: Disable 1: Enable

13.1.5.3. CE Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W1C	0x0	Task Channel3~0 End Pending 0: Not finished 1: Finished It indicates if task has been completed . Write '1' to clear it.

13.1.5.4. CE Task Load Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR
Bit	**Read/Write**	**Default/Hex**	**Description**

31:15	/	/	/
14:8	R/W	0x0	Algorithm type, the same with type field in description common control.
7:1	/	/	/
0	R/W	0x0	Task Load When set, CE can load the descriptor of task if task FIFO is not full.

13.1.5.5. **CE Task Status Register(Default Value: 0x0000_0000)**

Offset: 0x0014			**Register Name: CE_TSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R	0x0	indicate which channel in run for XTS. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
23:18	/	/	/
17:16	R	0x0	indicate which channel in run for asymmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
15:10	/	/	/
9:8	R	0x0	indicate which channel in run for digest. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
7:2	/	/	/
1:0	R	0x0	indicate which channel in run for symmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3

13.1.5.6. **CE Error Status Register(Default Value: 0x0000_0000)**

Offset: 0x0018			**Register Name: CE_ESR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W1C	0x0	Task channel 3 error type. (the same for other channels) Bit 24: algorithm not support Bit 25: data length error Bit 26: keysram access error. Write '1' to clear. Bit 29: address invalid

			other: reserved
23:16	R/W1C	0x0	Task channel 2 error type. Bit 16: algorithm not support Bit 17: data length error Bit 18: keysram access error. Write '1' to clear. Bit 21: address invalid other: reserved
15:8	R/W1C	0x0	Task channel 1 error type. Bit 8: algorithm not support Bit 9: data length error Bit 10: keysram access error. Write '1' to clear. Bit 13: address invalid other: reserved
7:0	R/W1C	0x0	Task channel 0 error type. Bit 0: algorithm not support Bit 1: data length error Bit 2: keysram access error. Write '1' to clear. Bit 5: address invalid other: reserved

13.1.5.7. CE Symmetric Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_SCSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Symmetric algorithm current source address DMA reads.

13.1.5.8. CE Symmetric Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_SCDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Symmetric algorithm current destination address DMA writes.

13.1.5.9. CE HASH Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CE_HCSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HASH algorithm current source address DMA reads.

13.1.5.10. CE HASH Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CE_HCDA
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R	0x0	HASH algorithm current destination address DMA writes.

13.1.5.11. **CE Asymmetric Current Source Address Register(Default Value: 0x0000_0000)**

Offset: 0x0044			**Register Name: CE_ACSA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Asymmetric algorithm current source address DMA reads.

13.1.5.12. **CE Asymmetric Current Destination Address Register(Default Value: 0x0000_0000)**

Offset: 0x0048			**Register Name: CE_ACDA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Asymmetric algorithm current destination address DMA writes.

13.1.5.13. **CE XTS Current Source Address Register(Default Value: 0x0000_0000)**

Offset: 0x0054			**Register Name: CE_XCSA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	XTS algorithm current source address DMA reads.

13.1.5.14. **CE XTS Current Destination Address Register(Default Value: 0x0000_0000)**

Offset: 0x0058			**Register Name: CE_XCDA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	XTS algorithm current destination address DMA writes.

13.2. Security ID

The Security ID(SID) is 2Kbits electrical fuse for saving key, which includes chip ID, thermal sensor, HASH code and security key.

The SID module has the following features:

- A fuse only can program one time
- Loading the key to CE

Chapter 14 Carrier, Storage and Baking Information

14.1. Carrier

14.1.1. Matrix Tray Information

Table 14-1 shows the V536-H/V526 matrix tray carrier information.

Table 14-1. Matrix Tray Carrier Information

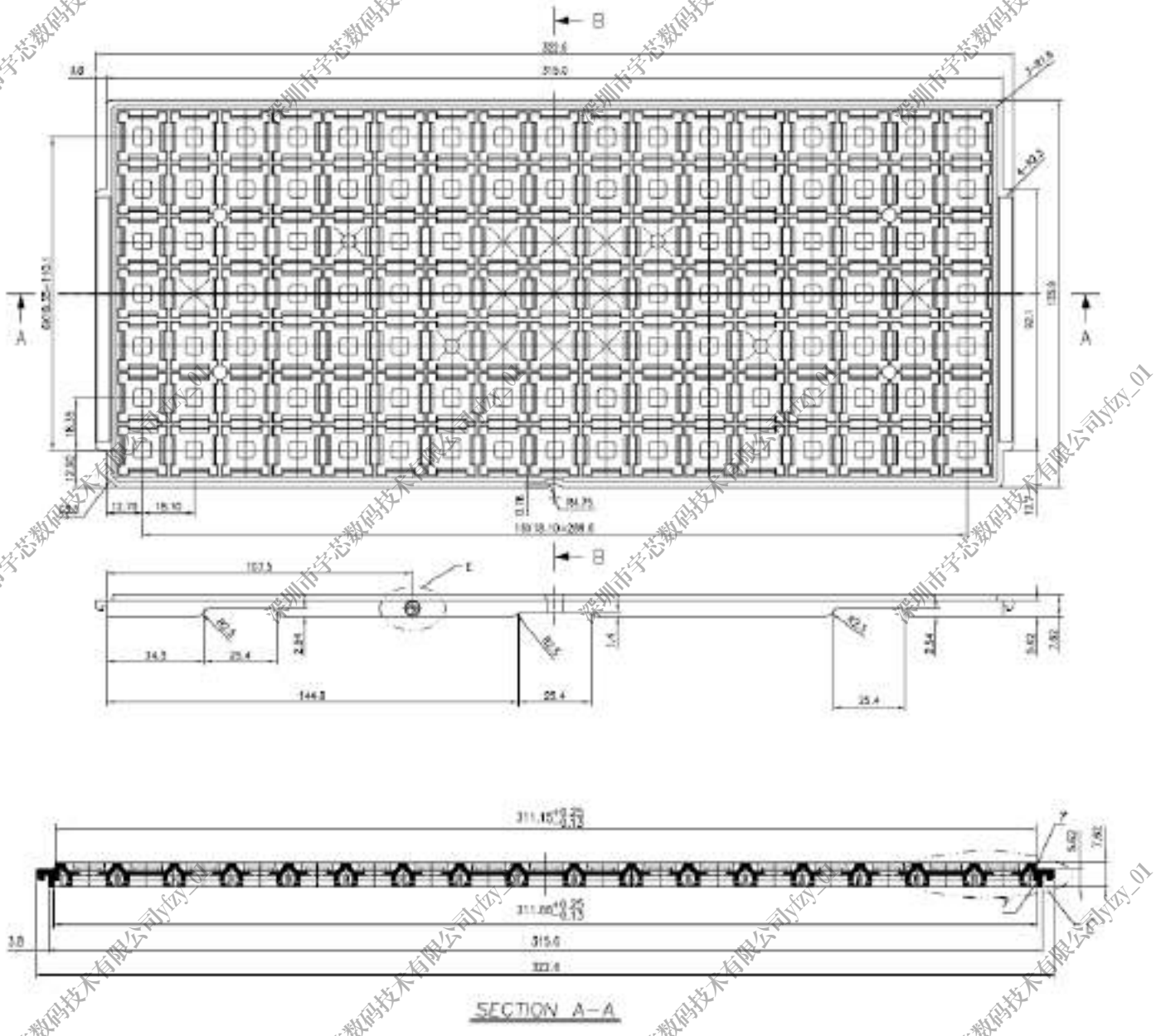
Item	Color	Size	Note
Tray	Black	315mm x 136mm x 7.62mm	119 Qty/Tray
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm	Surface impedance:$10^9\Omega$ Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm	
Inner Box	White	396mm x 196mm x 96mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420mm x 410mm x 320mm	6 Inner box/Carton

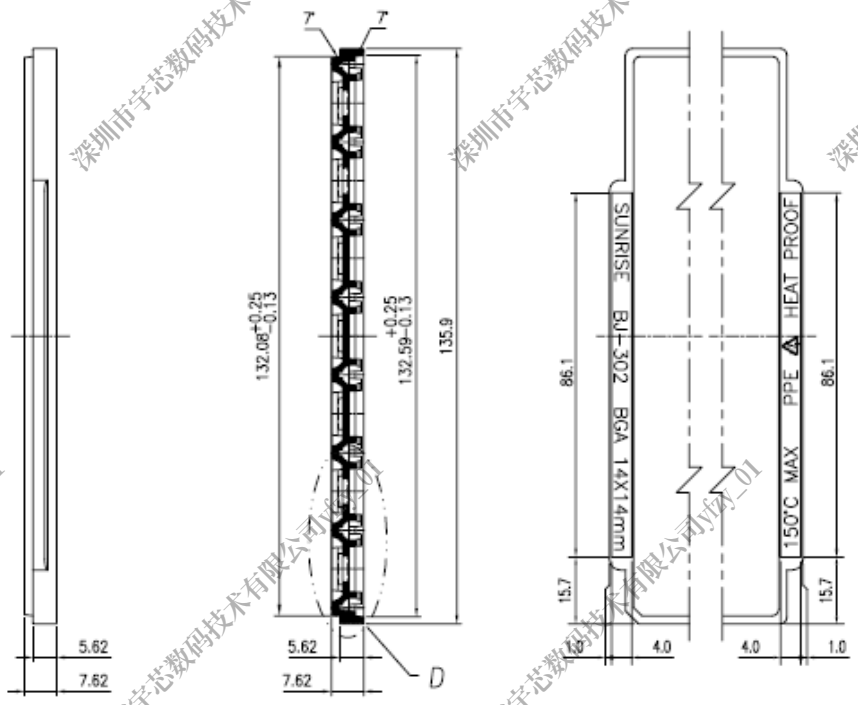
Table 14-2 shows the V536-H/V526 packing quantity.

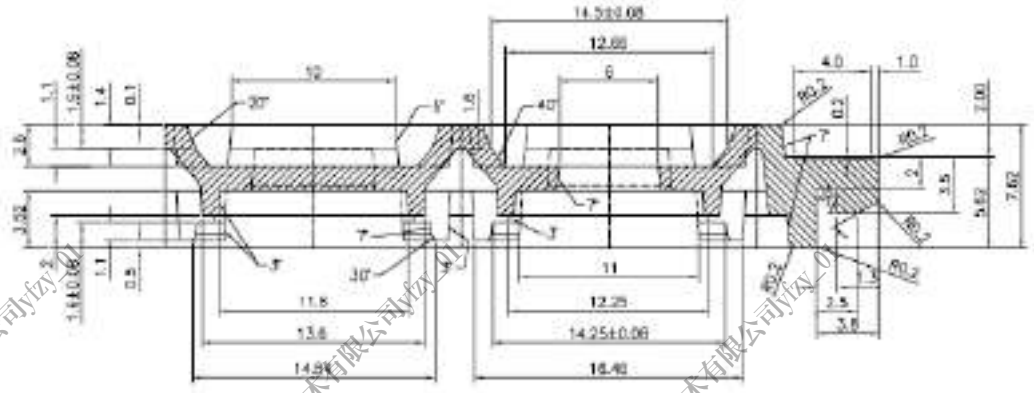
Table 14-2. Packing Quantity Information

Sample	Size(mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
V536-H, V526	14 x 14	119	10	1190	6	7140

Figure 14-1 shows tray dimension drawing of the V536-H/V526.







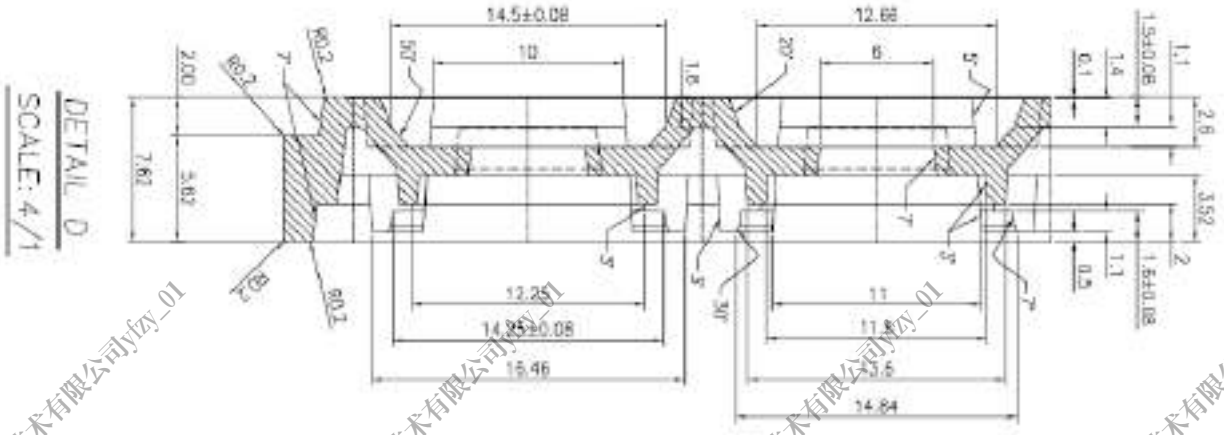


Table 14-3. Tray Dimension Drawing

14.2. Storage

Reliability is affected if any condition specified in Section 14.2.2 and Section 14.2.3 has been exceeded.

14.2.1. Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL are defined in Table 14-4.

Table 14-4. MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label(TOL)	≤30°C / 60%RH

NOTE

The V536-H/V526 device samples are classified as MSL3.

14.2.2. Bagged Storage Conditions

The shelf life of the V536-H/V526 device samples are defined in Table 14-5.

Table 14-5. Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

14.2.3. Out-of-bag Duration

It is defined by the device MSL rating, the out-of-bag duration of the V536-H/V526 are as follows.

Table 14-6. Out-of-bag Duration

Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Moisture sensitive level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

14.3. Baking

It is not necessary to bake the V536-H/V526 if the conditions specified in Section 14.2.2 and Section 14.2.3 have not been exceeded. It is necessary to bake the V536-H/V526 if any condition specified in Section 14.2.2 and Section 14.2.3 has been exceeded.

It is necessary to bake the V536-H/V526 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that baking should not exceed 3 times, and the tray baking should not exceed 1 time, with a distortion risk.

Chapter 15 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, please contact with Allwinner FAE.

The lead-free reflow profile conditions are given in Table 15-1. The table is for reference only.

Table 15-1. Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

Figure 15-1 shows the typical lead-free reflow profile.

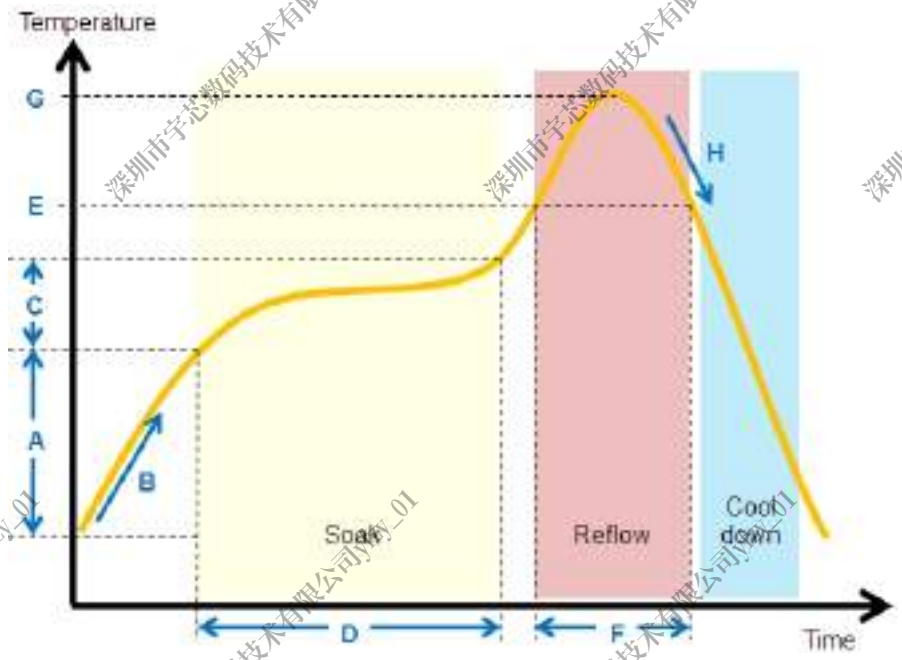


Figure 15-1. Typical Lead-free Reflow Profile

NOTE

The above reflow profile is solder joint testing result, it is for reference only, please adjust depending on actual production conditions.

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 15-2.

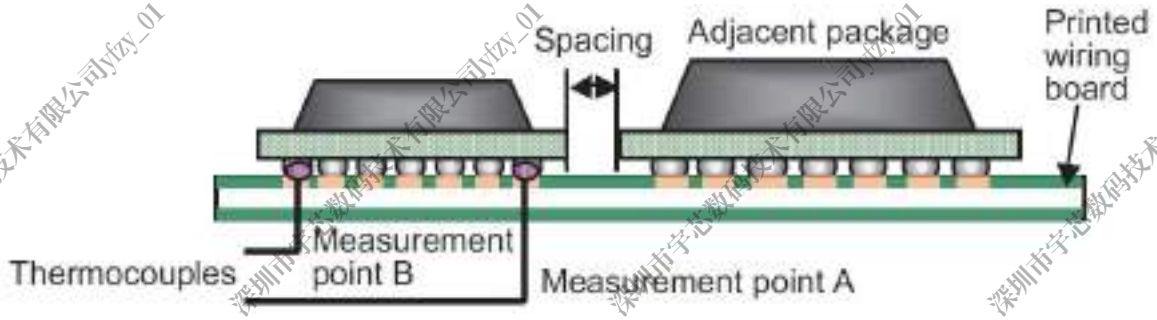


Figure 15-2. Measuring the Reflow Solding Process

NOTE

To measure the temperature of QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

Chapter 16 Part Marking

16.1. V536-H

Figure 16-1 shows the V536-H marking.

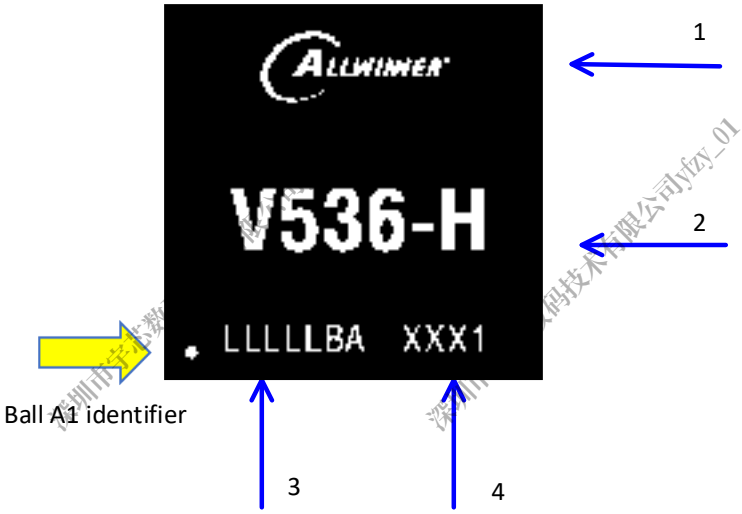


Figure 16-1. V536-H Marking

Table 16-1 describes the V536 marking definitions.

Table 16-1. V536-H Marking Definitions

NO.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V536-H	Product name	Fixed
3	LLLLLBA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

16.2. V526

Figure 16-2 shows the V526 marking.

Figure 16-2. V526 Marking

Table 16-2 describes the V526 marking definitions.

Table 16-2. V526 Marking Definitions

NO.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V526	Product name	Fixed
3	LLLLLBA	Lot number	Dynamic
4	XXX2	Date code	Dynamic

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