
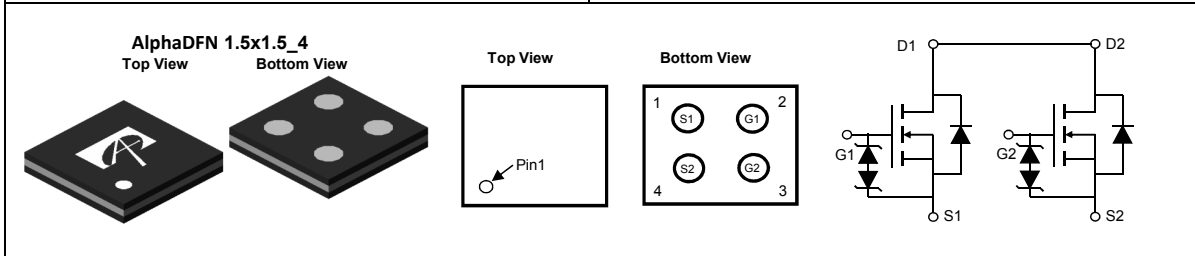


<p>General Description</p> <ul style="list-style-type: none"> • Trench Power AlphaMOS (αMOS LV) technology • Low $R_{SS(ON)}$ • Fully protected AlphaDFN package • With ESD protection to improve battery performance and safety • Common drain configuration for design simplicity • RoHS and Halogen-Free Compliant <p>Applications</p> <ul style="list-style-type: none"> • Battery protection switch • Mobile device battery charging and discharging 	<p>Product Summary</p> <table style="width: 100%; border: none;"> <tr> <td style="width: 70%;">V_{SS}</td> <td style="text-align: right;">20V</td> </tr> <tr> <td>$R_{SS(ON)}$ (at $V_{GS}=4.5V$)</td> <td style="text-align: right;">< 34mΩ</td> </tr> <tr> <td>$R_{SS(ON)}$ (at $V_{GS}=4.0V$)</td> <td style="text-align: right;">< 38mΩ</td> </tr> <tr> <td>$R_{SS(ON)}$ (at $V_{GS}=3.7V$)</td> <td style="text-align: right;">< 40mΩ</td> </tr> <tr> <td>$R_{SS(ON)}$ (at $V_{GS}=3.1V$)</td> <td style="text-align: right;">< 45mΩ</td> </tr> <tr> <td>$R_{SS(ON)}$ (at $V_{GS}=2.5V$)</td> <td style="text-align: right;">< 56mΩ</td> </tr> </table> <p>Typical ESD protection HBM Class 3A</p> <div style="text-align: right;">  </div>	V_{SS}	20V	$R_{SS(ON)}$ (at $V_{GS}=4.5V$)	< 34mΩ	$R_{SS(ON)}$ (at $V_{GS}=4.0V$)	< 38mΩ	$R_{SS(ON)}$ (at $V_{GS}=3.7V$)	< 40mΩ	$R_{SS(ON)}$ (at $V_{GS}=3.1V$)	< 45mΩ	$R_{SS(ON)}$ (at $V_{GS}=2.5V$)	< 56mΩ
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Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOC2804B	AlphaDFN 1.5x1.5_4	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Rating	Units
Source-Source Voltage	V_{SS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Source Current(DC) ^{Note1}	I_S	6	A
Source Current(Pulse) ^{Note2}	I_{SM}	60	
Power Dissipation ^{Note1}	P_D	1.3	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Units
Maximum Junction-to-Ambient	$R_{\theta JA}$	85	$^\circ C/W$
Maximum Junction-to-Ambient		96	$^\circ C/W$

Note 1. I_S rated value is based on bare silicon. Mounted on 70mmx70mm FR-4 board.
Note 2. PW <10 μs pulses, duty cycle 1% max.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{SSS}	Source-Source Breakdown Voltage	I _S =250μA, V _{GS} =0V Test Circuit 6	20			V
I _{SSS}	Zero Gate Voltage Source Current	V _{SS} =20V, V _{GS} =0V Test Circuit 1			1	μA
		T _J =55°C			5	
I _{GSS}	Gate leakage current	V _{SS} =0V, V _{GS} =±10V Test Circuit 2			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{SS} =V _{GS} , I _S =250μA Test Circuit 3	0.5	0.9	1.3	V
R _{SS(ON)}	Static Source to Source On-Resistance	V _{GS} =4.5V, I _S =3A Test Circuit 4	20	28	34	mΩ
		T _J =125°C	27	38.5	47	
		V _{GS} =4.0V, I _S =3A Test Circuit 4	22	30.5	38	mΩ
		V _{GS} =3.7V, I _S =3A Test Circuit 4	23	32	40	mΩ
		V _{GS} =3.1V, I _S =3A Test Circuit 4	25	35	45	mΩ
		V _{GS} =2.5V, I _S =3A Test Circuit 4	30	42.5	56	mΩ
g _{FSS}	Forward Transconductance	V _{SS} =5V, I _S =3A Test Circuit 3		20		S
V _{FSS}	Forward Source to Source Voltage	I _S =1A, V _{GS} =0V Test Circuit 5		0.72	1	V
DYNAMIC PARAMETERS						
R _g	Gate resistance	f=1MHz		2		KΩ
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{G1S1} =4.5V, V _{SS} =10V, I _S =3A		9.5		nC
t _{D(on)}	Turn-On DelayTime	V _{G1S1} =4.5V, V _{SS} =10V, R _L =3.3Ω, R _{GEN} =3Ω Test Circuit8		0.85		μs
t _r	Turn-On Rise Time			2.2		μs
t _{D(off)}	Turn-Off DelayTime			2.0		μs
t _f	Turn-Off Fall Time			4.3		μs

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

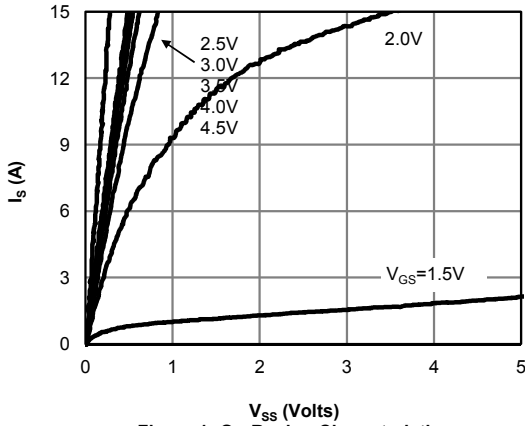


Figure 1: On-Region Characteristics

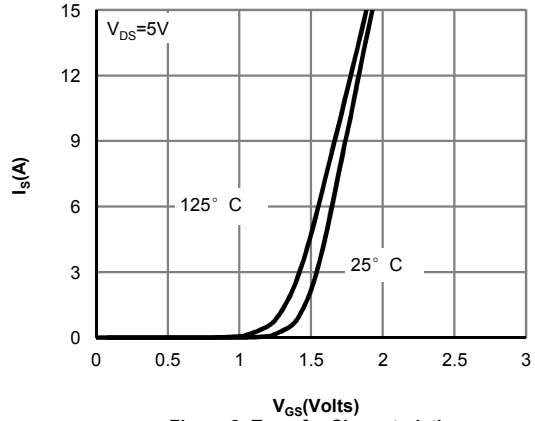


Figure 2: Transfer Characteristics

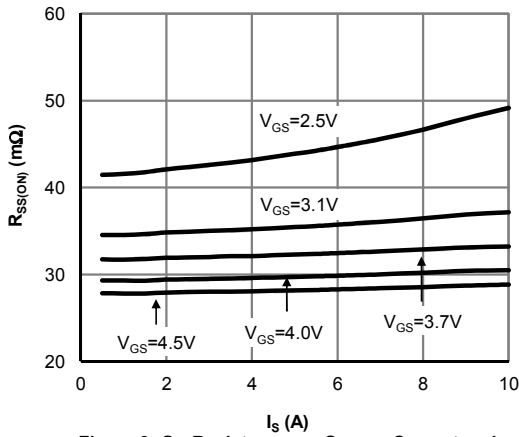


Figure 3: On-Resistance vs. Source Current and Gate Voltage

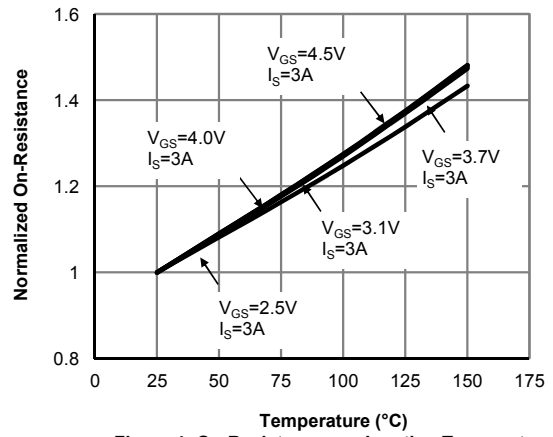


Figure 4: On-Resistance vs. Junction Temperature

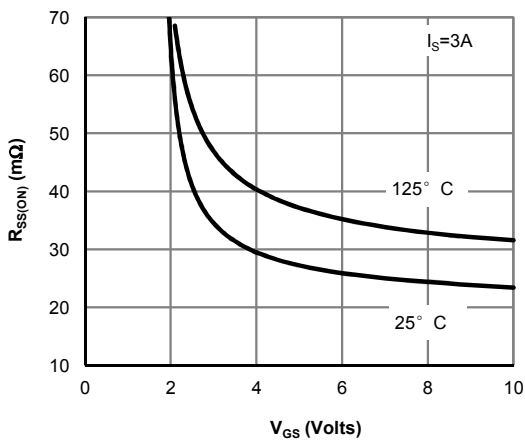


Figure 5: On-Resistance vs. Gate-Source Voltage

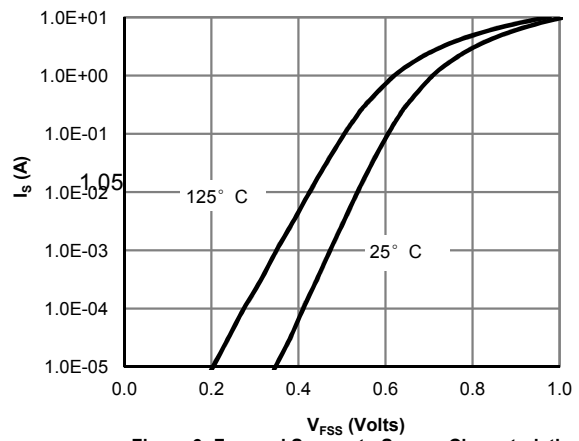


Figure 6: Forward Source to Source Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

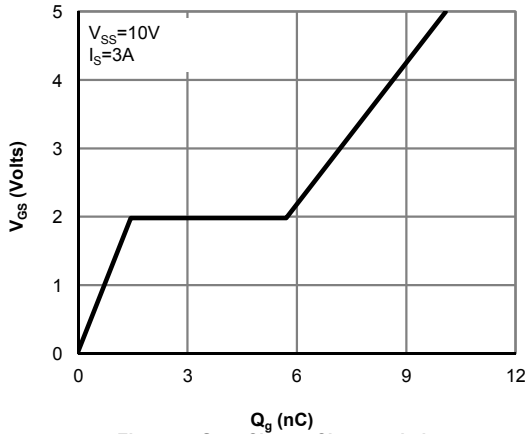


Figure 7: Gate-Charge Characteristics

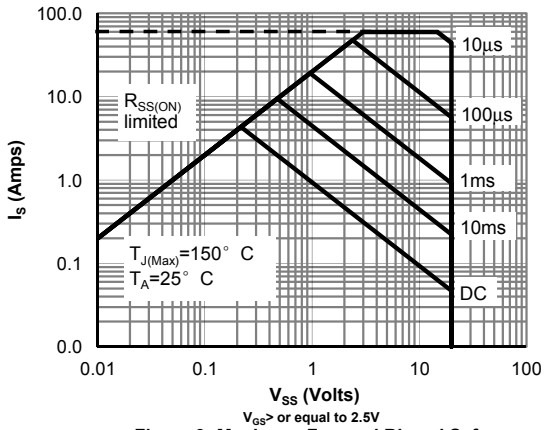


Figure 9: Maximum Forward Biased Safe Operating Area (Note1)

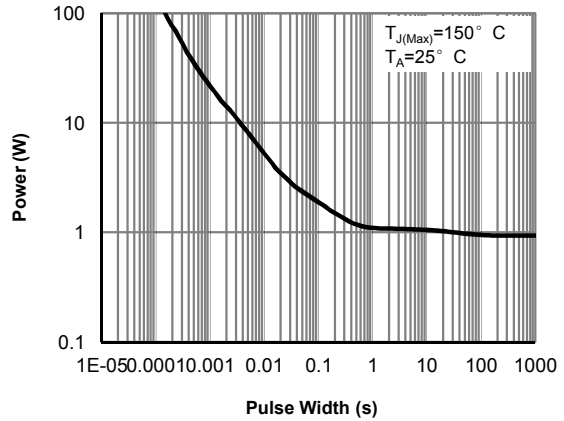


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note1)

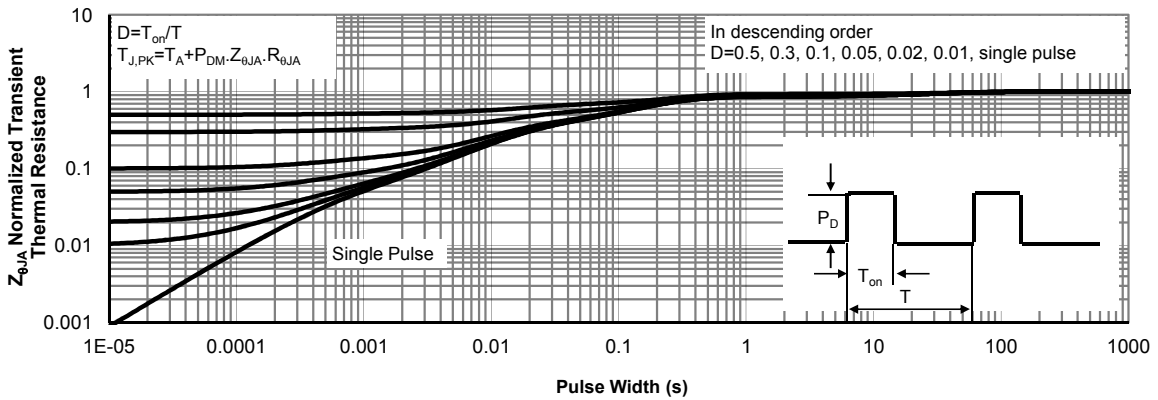
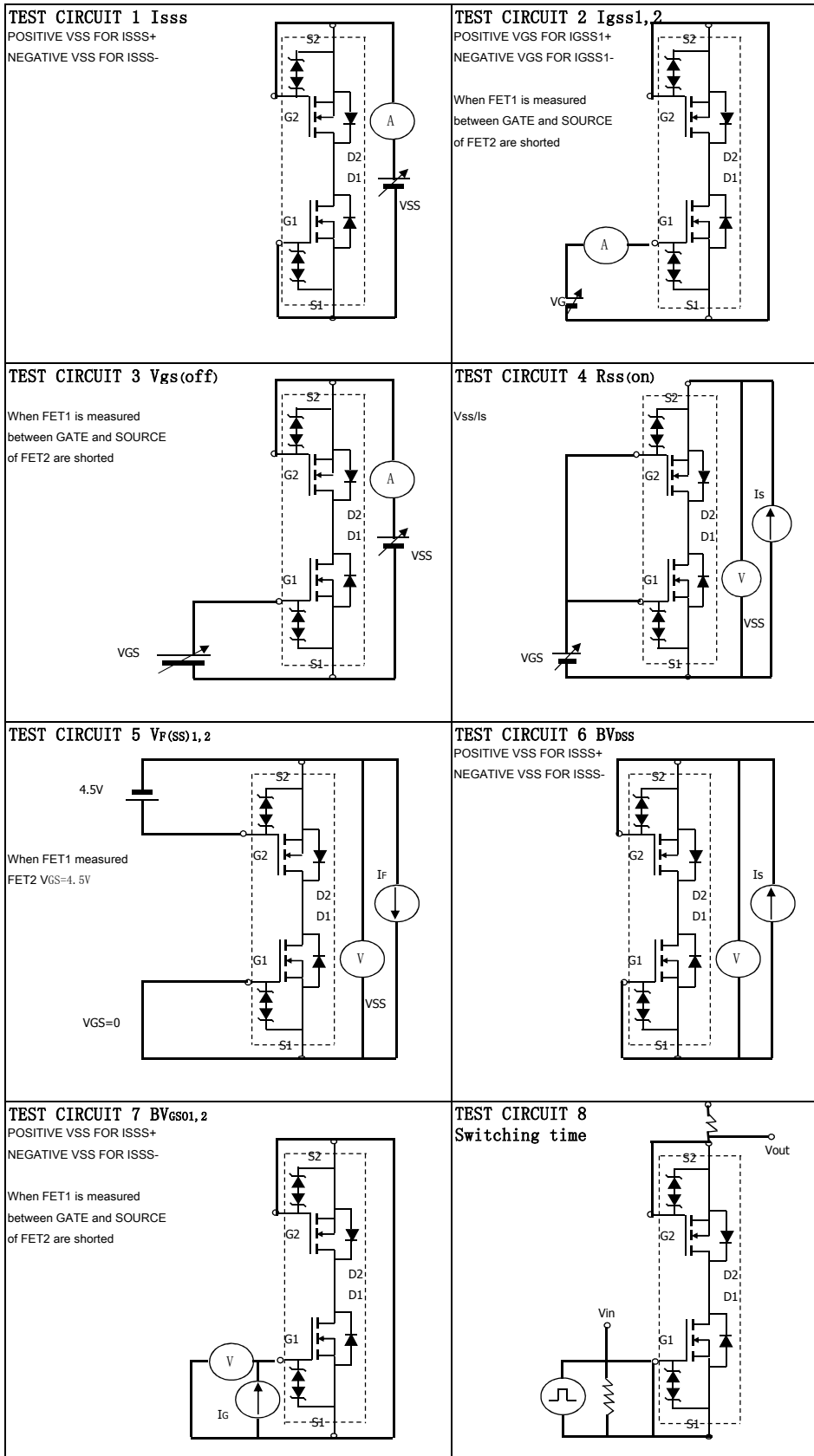


Figure 11: Normalized Maximum Transient Thermal Impedance (Note1)



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