ALPHA & OMEGA SEMICONDUCTOR

AOC3870A
## 12V Common-Drain Dual N-Channel MOSFET

General Description

• Trench Power MOSFET technology
• Low $R_{SS(ON)}$
• With ESD protection to improve battery performance and safety
• Common drain configuration for design simplicity
• RoHS and Halogen-Free Compliant

Applications

• Battery protection switch
• Mobile device battery charging and discharging

Product Summary

V_{SS}	12V
$R_{SS(ON)}$ (at V_{GS}=4.5V)	< 3.7mΩ
$R_{SS(ON)}$ (at V_{GS}=4.0V)	< 3.8mΩ
$R_{SS(ON)}$ (at V_{GS}=3.8V)	< 4mΩ
$R_{SS(ON)}$ (at V_{GS}=3.1V)	< 4.6mΩ
$R_{SS(ON)}$ (at V_{GS}=2.5V)	< 5.6mΩ
Typical ESD protection	**HBM Class 2**

Green Product

AlphaDFN™ 3.01x1.52A_10
Top View **Bottom View**

Pin1

Pin1

1, 2, 7, 8: Source(FET1)   5: Gate(FET1)
3, 4, 9, 10: Source(FET2) 6: Gate(FET2)

G1   G2   S1   S2
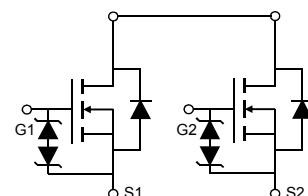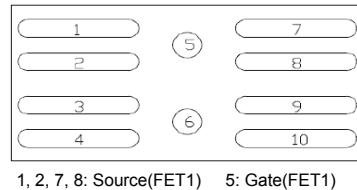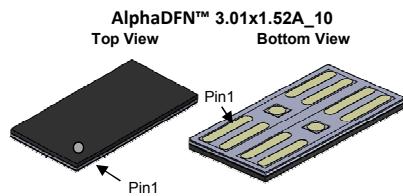
Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOC3870A	AlphaDFN 3.01x1.52A_10	Tape & Reel	8000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Source-Source Voltage		V_{SS}	12	V
Gate-Source Voltage		V_{GS}	±8	V
Source Current(DC) Note1	T_A=25°C	I_S	22	A
Source Current(Pulse) Note2		I_{SM}	130	
Power Dissipation Note1	T_A=25°C	P_D	2.3	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typical	Units
Maximum Junction-to-Ambient	t ≤ 10s	$R_{θJA}$	45	°C/W
Maximum Junction-to-Ambient	Steady-State		55	°C/W

Note 1. I_s rated value is based on bare silicon.Mounted on 70mmx70mm FR-4 board.

Note 2. PW <10 µs pulses, duty cycle 1% max.

Electrical Characteristics (T$_J$=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{SSS}$	Source-Source Breakdown Voltage	I$_S$=250µA, V$_{GS}$=0V	Test Circuit 6	12			V
I$_{SSS}$	Zero Gate Voltage Source Current	V$_{SS}$=12V, V$_{GS}$=0V	Test Circuit 1			1	µA
			T$_J$=55°C			5	
I$_{GSS}$	Gate leakage current	V$_{SS}$=0V, V$_{GS}$=±8V	Test Circuit 2			±10	µA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{SS}$=V$_{GS,}$ I$_S$=250µA	Test Circuit 3	0.4	0.7	1.1	V
R$_{SS(ON)}$	Static Source to Source On-Resistance	V$_{GS}$=4.5V, I$_S$=5A	Test Circuit 4	2.1	2.95	3.7	mΩ
			T$_J$=125°C	2.9	4.05	5.0	mΩ
		V$_{GS}$=4.0V, I$_S$=5A	Test Circuit 4	2.2	3.05	3.8	mΩ
		V$_{GS}$=3.8V, I$_S$=5A	Test Circuit 4	2.3	3.1	4.0	mΩ
		V$_{GS}$=3.1V, I$_S$=5A	Test Circuit 4	2.4	3.4	4.6	mΩ
		V$_{GS}$=2.5V, I$_S$=5A	Test Circuit 4	2.8	3.9	5.6	mΩ
g$_{FS}$	Forward Transconductance	V$_{SS}$=5V, I$_S$=5A	Test Circuit 3		50		S
V$_{FSS}$	Forward Source to Source Voltage	I$_S$=1A,V$_{GS}$=0V	Test Circuit 5		0.57	1	V
DYNAMIC PARAMETERS							
R$_g$	Gate resistance	f=1MHz			1.2		KΩ
SWITCHING PARAMETERS							
Q$_g$	Total Gate Charge	V$_{G1S1}$=4.5V, V$_{SS}$=6V, I$_S$=5A			32		nC
t$_{D(on)}$	Turn-On DelayTime				1.2		µs
t$_r$	Turn-On Rise Time	V$_{G1S1}$=4.5V, V$_{SS}$=6V, R$_L$=1.2Ω, R$_{GEN}$=3Ω	Test Circuit8		3.0		µs
t$_{D(off)}$	Turn-Off DelayTime				3.1		µs
t$_f$	Turn-Off Fall Time				8.2		µs

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 1: On-Region Characteristics
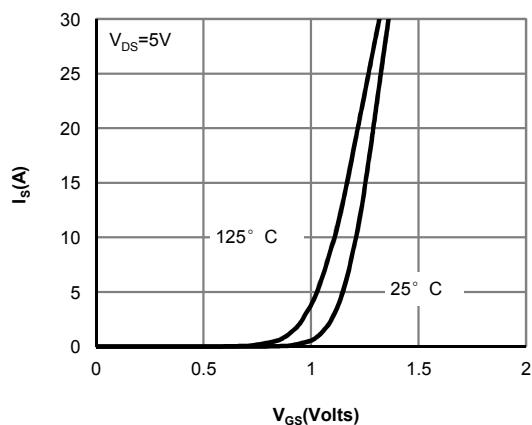

Figure 2: Transfer Characteristics
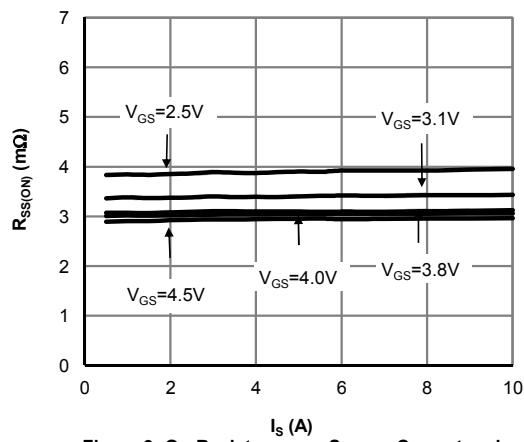
Figure 3: On-Resistance vs. Source Current and Gate Voltage
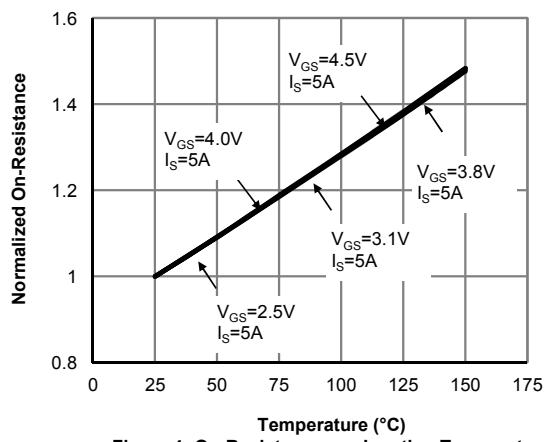

Figure 4: On-Resistance vs. Junction Temperature
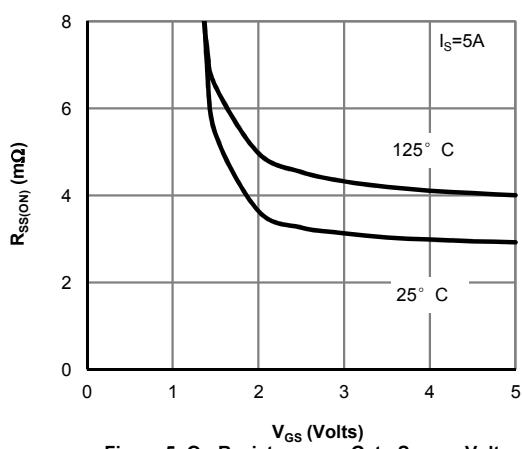
Figure 5: On-Resistance vs. Gate-Source Voltage
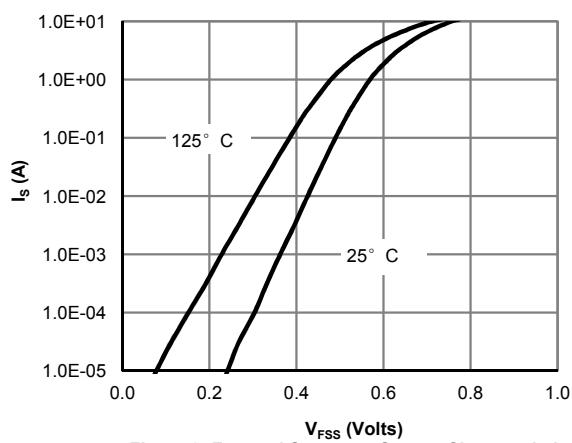
Figure 6: Forward Source to Source Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

V_{SS}=6V
I_S=5A
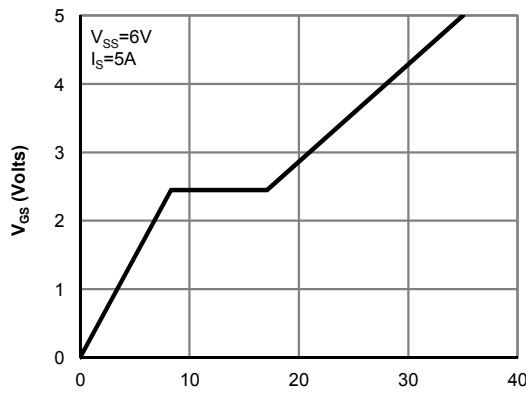
Q_g (nC)
Figure 7: Gate-Charge Characteristics

$R_{SS(ON)}$ limited

10μs
100μs
1ms
10ms
DC

$T_{J(Max)}$=150°C
T_A=25°C
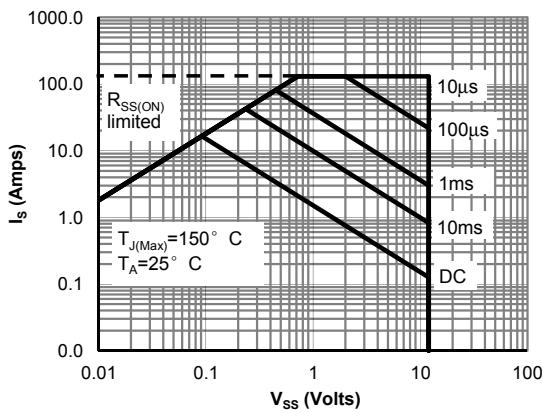
V_{SS} (Volts)
V_{GS}> or equal to 2.5V
Figure 8: Maximum Forward Biased Safe Operating Area (Note1)

$T_{J(Max)}$=150°C
T_A=25°C
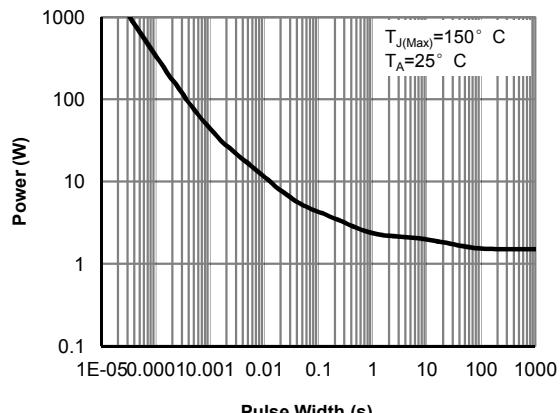
Pulse Width (s)
Figure 9: Single Pulse Power Rating Junction-to-Ambient (Note1)

$D=T_{on}/T$
$T_{J,PK}=T_A+P_{DM}\cdot Z_{\theta JA}\cdot R_{\theta JA}$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse

P_D

T_{on}
T
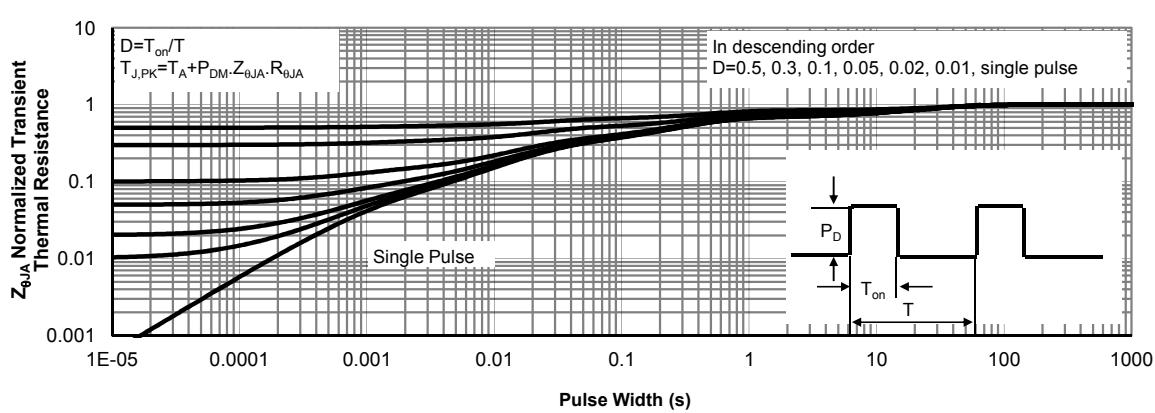
Pulse Width (s)
Figure 10: Normalized Maximum Transient Thermal Impedance (Note1)

TEST CIRCUIT 1 Isss

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-
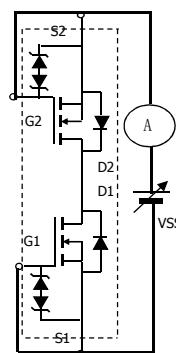
TEST CIRCUIT 2 Igss1,2

POSITIVE VGS FOR IGSS1+
NEGATIVE VGS FOR IGSS1-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted
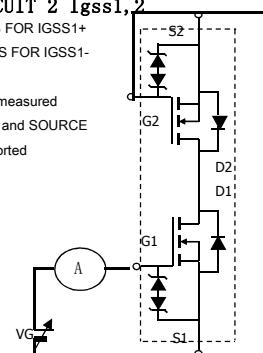
TEST CIRCUIT 3 Vgs(off)

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted
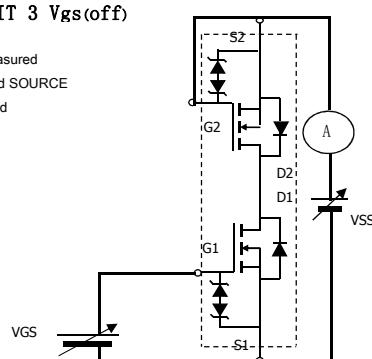
TEST CIRCUIT 4 Rss(on)

Vss/Is
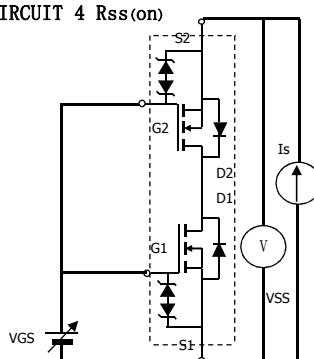
TEST CIRCUIT 5 VF(SS)1,2

4.5V

When FET1 measured
FET2 VGS=4.5V
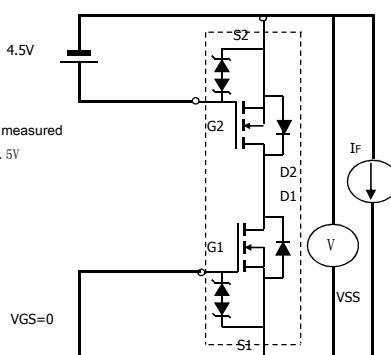
VGS=0

TEST CIRCUIT 6 BVDSS

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-
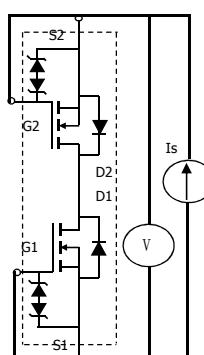
TEST CIRCUIT 7 BVGS01,2

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted
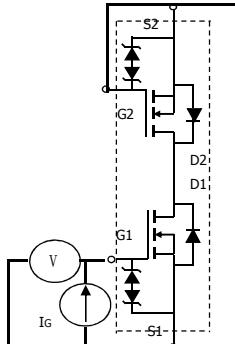
TEST CIRCUIT 8
Switching time
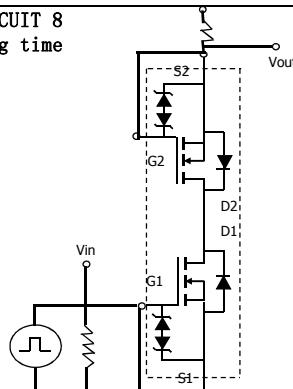
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