AOD423/AOI423/AOY423

30V P-Channel MOSFET

ALPHA & OMEGA SEMICONDUCTOR

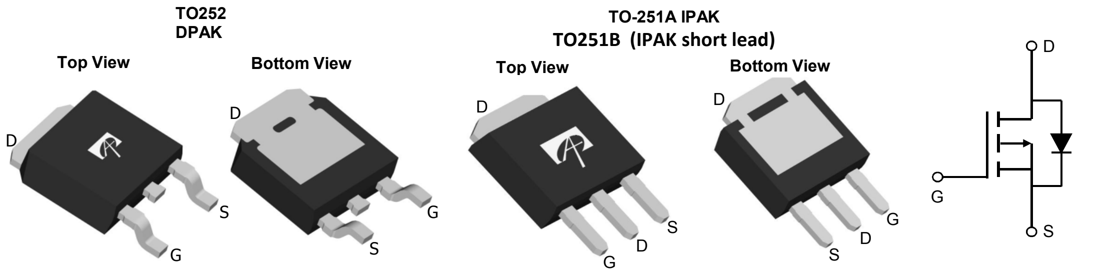
General Description

The AOD423/AOI423/AOY423 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK/IPAK package, this device is well suited for high current load applications.

Product Summary

V_{DS}	-30V	
I_D (at V_{GS}= -20V)	-70A	
$R_{DS(ON)}$ (at V_{GS}= -20V)	< 6.2mΩ	(< 6.7mΩ*)
$R_{DS(ON)}$ (at V_{GS} = -10V)	< 8mΩ	(< 8.5mΩ*)

100% UIS Tested
100% R_g Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOD423	TO-252	Tape & Reel	2500
AOI423	TO-251A	Tube	4000
AOY423	TO-251B	Tube	4000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current [G]	T_C=25°C	I_D	-70	A
	T_C=100°C		-67	
Pulsed Drain Current [C]		I_{DM}	-200	
Continuous Drain Current	T_A=25°C	I_{DSM}	-15	A
	T_A=70°C		-12	
Avalanche Current [C]		I_{AS}, I_{AR}	-50	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	125	mJ
Power Dissipation [B]	T_C=25°C	P_D	90	W
	T_C=100°C		45	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.5	W
	T_A=70°C		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	16	20	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		41	50	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	0.9	1.6	°C/W

* package TO251A, TO251B

ALPHA & OMEGA SEMICONDUCTOR

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V		-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V				-1	µA
			T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±25V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA		-1.5	-2.5	-3.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V		-200			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-20V, I_D=-20A TO252			5.1	6.2	mΩ
			T_J=125°C		7.6	9.2	
		V_{GS}=-10V, I_D=-20A TO252			6.2	8	mΩ
		V_{GS}=-20V, I_D=-20A TO251A, TO251B			5.6	6.7	mΩ
		VGS=-10V, ID=-20A TO251A, TO251B			6.7	8.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-20A			42		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V			-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current[G]					-70	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz			2760		pF
C_{oss}	Output Capacitance				550		pF
C_{rss}	Reverse Transfer Capacitance				375		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.5	3	6.0	Ω
SWITCHING PARAMETERS							
Q_g	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-20A			45	65	nC
Q_{gs}	Gate Source Charge				10		nC
Q_{gd}	Gate Drain Charge				12		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=0.75Ω, R_{GEN}=3Ω			13		ns
t_r	Turn-On Rise Time				23		ns
$t_{D(off)}$	Turn-Off DelayTime				35		ns
t_f	Turn-Off Fall Time				26		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-20A, dI/dt=500A/µs			15		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-20A, dI/dt=500A/µs			30		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

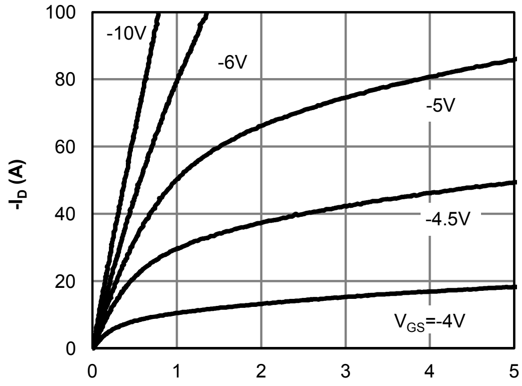


Fig 1: On-Region Characteristics (Note E)

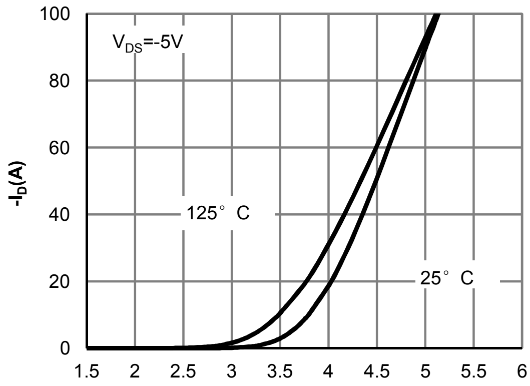


Figure 2: Transfer Characteristics (Note E)

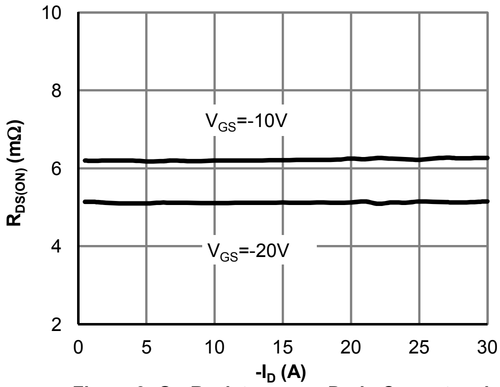


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

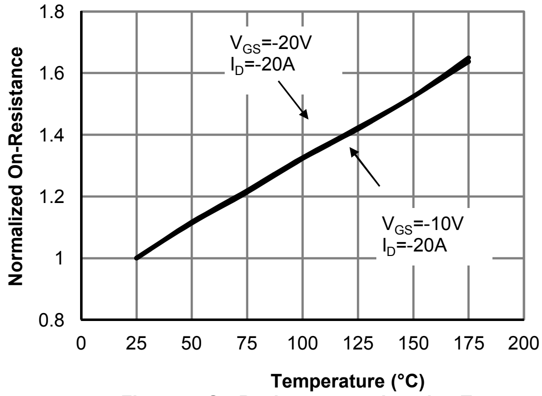


Figure 4: On-Resistance vs. Junction Temperature (Note E)

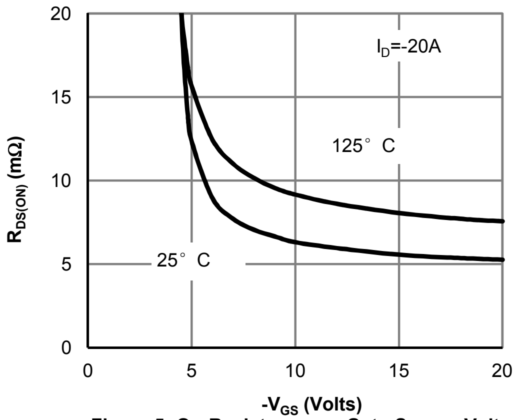


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

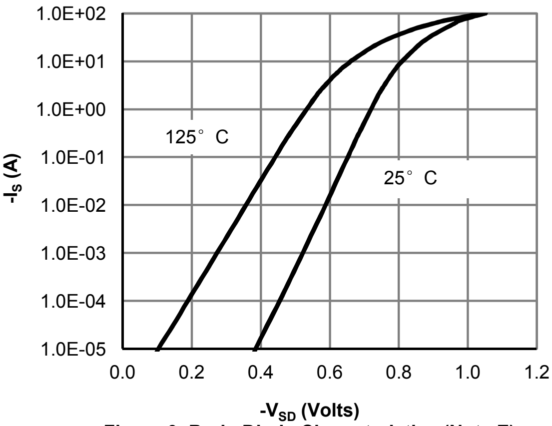


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

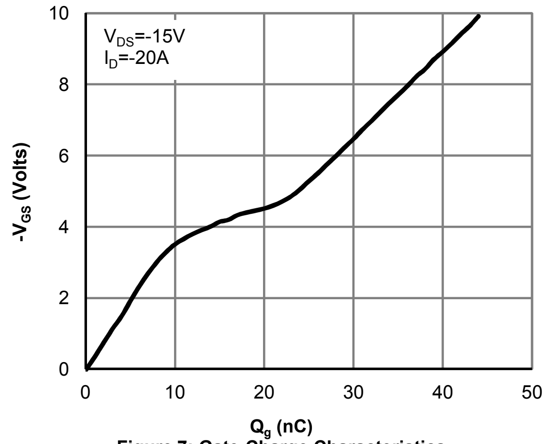


Figure 7: Gate-Charge Characteristics

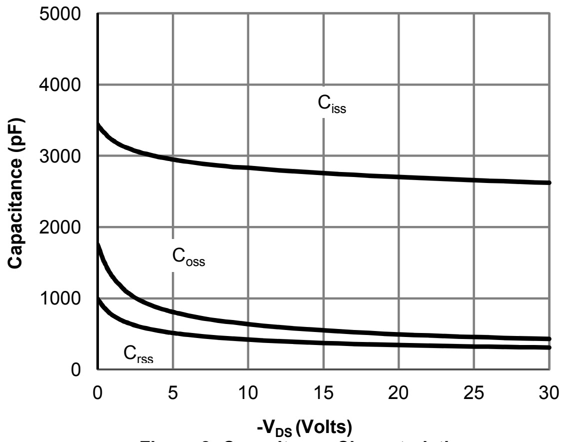


Figure 8: Capacitance Characteristics

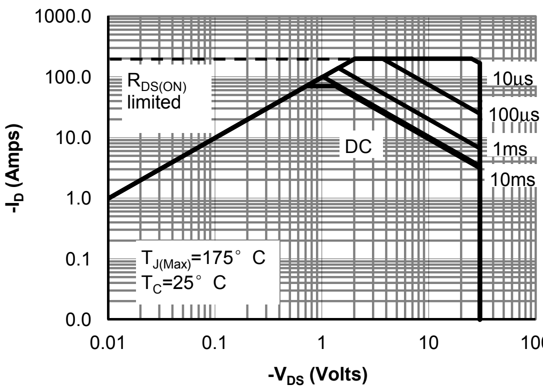


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

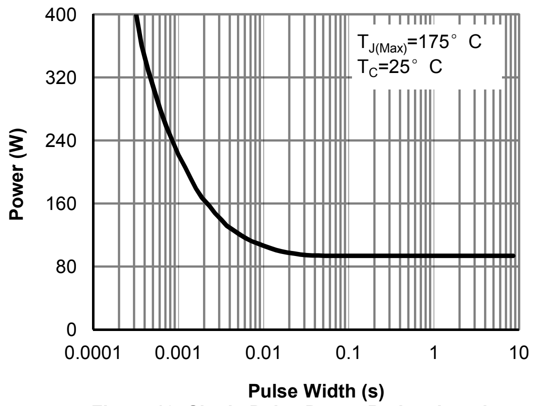


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

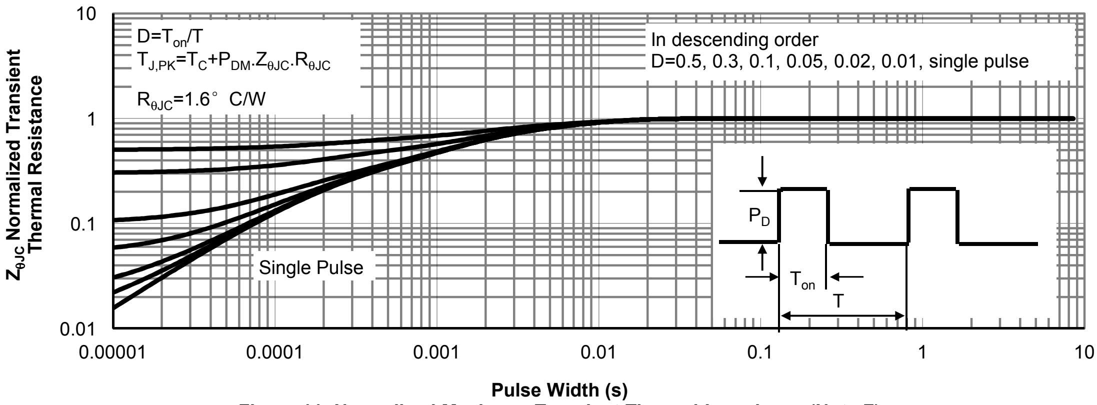


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

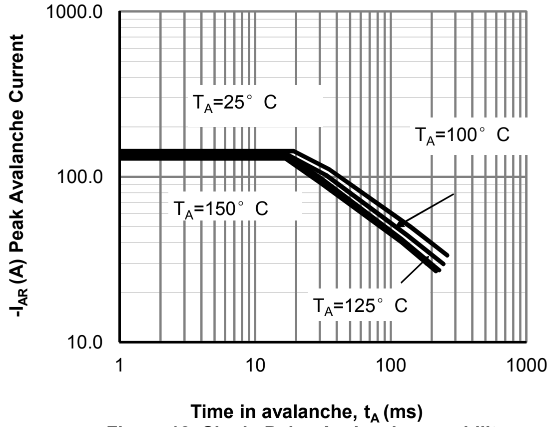


Figure 12: Single Pulse Avalanche capability (Note C)

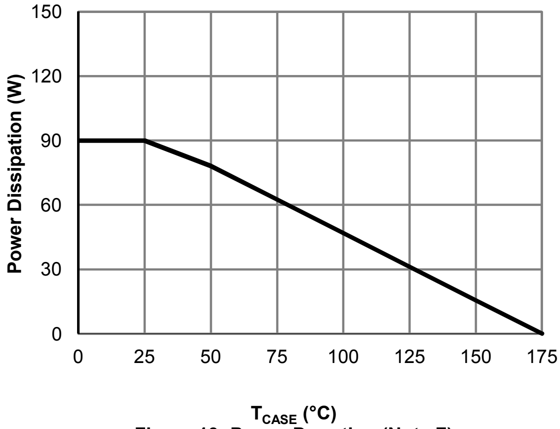


Figure 13: Power De-rating (Note F)

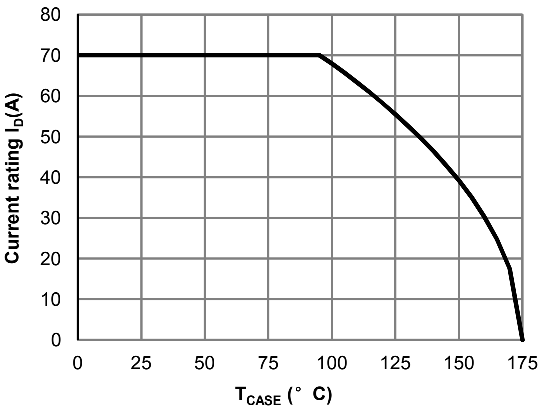


Figure 14: Current De-rating (Note F)

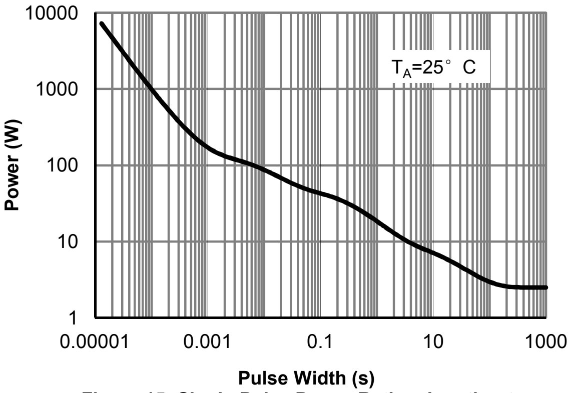


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

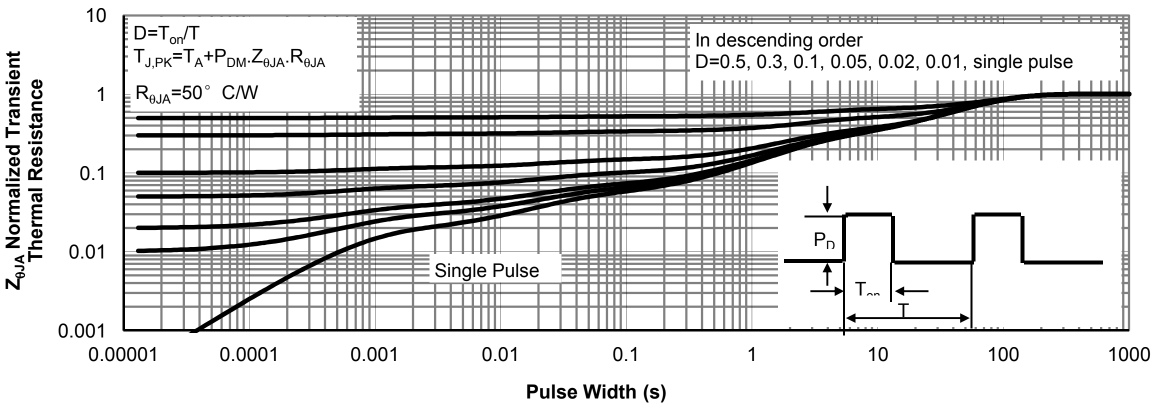
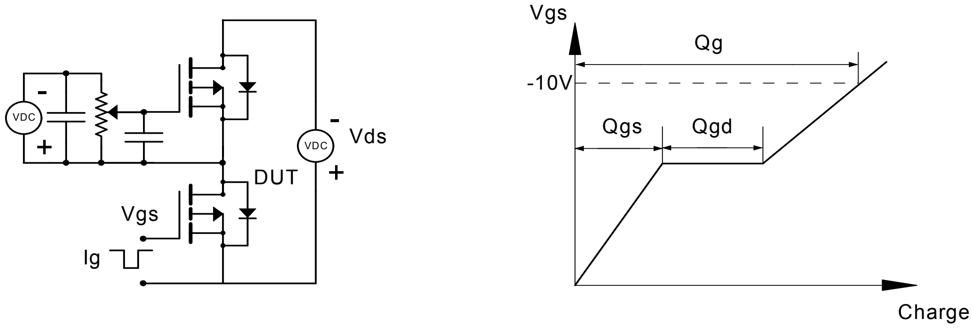
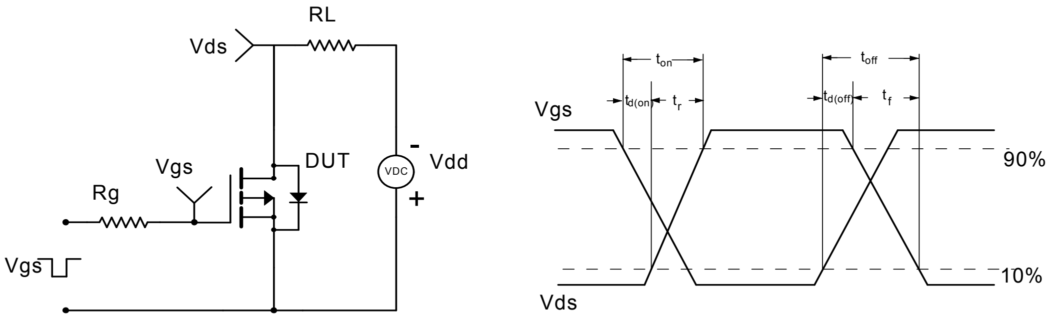


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

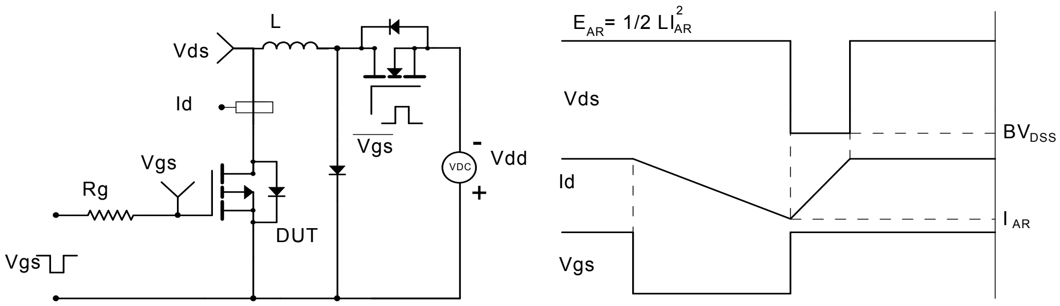
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms