



**ALPHA & OMEGA**  
SEMICONDUCTOR

**AONS66916**  
**100V N-Channel AlphaSGT™**

### General Description

- Trench Power AlphaSGT™ technology
- Low  $R_{DS(ON)}$
- Low Gate Charge
- Optimized for fast-switching applications
- RoHS and Halogen-Free Compliant

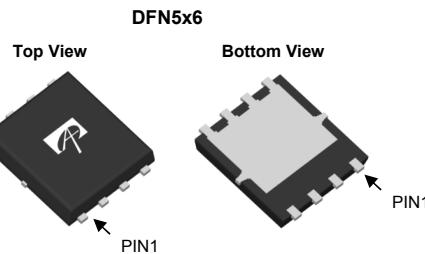
### Applications

- Synchronous Rectification in DC/DC and AC/DC Converters
- Industrial and Motor Drive applications

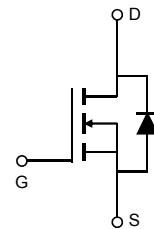
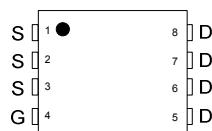
### Product Summary

$V_{DS}$	100V
$I_D$ (at $V_{GS}=10V$ )	100A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 3.6mΩ
$R_{DS(ON)}$ (at $V_{GS}=6V$ )	< 5mΩ

100% UIS Tested  
100%  $R_g$  Tested



Top View



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS66916	DFN 5x6	Tape & Reel	3000

### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	100	A
		100	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	400	
Continuous Drain Current	$I_{DSM}$	30	A
		24	
Avalanche Current <sup>C</sup>	$I_{AS}$	70	A
Avalanche energy	$E_{AS}$	245	mJ
Power Dissipation <sup>B</sup>	$P_D$	215	W
		86	
Power Dissipation <sup>A</sup>	$P_{DSM}$	6.2	W
		4.0	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	15	20	°C/W
		40	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.43	0.58	°C/W

**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$		1		$\mu\text{A}$
			$T_J=55^\circ\text{C}$		5	
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm20\text{V}$			$\pm100$	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.2	2.9	3.6	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$		3.0	3.6	$\text{m}\Omega$
			$T_J=125^\circ\text{C}$	5.0	6.0	
		$V_{GS}=6\text{V}, I_D=20\text{A}$		3.8	5.0	
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		100		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.67	1	V
$I_S$	Maximum Body-Diode Continuous Current <sup>G</sup>				100	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=50\text{V}, f=1\text{MHz}$		5325		pF
$C_{oss}$	Output Capacitance			1240		pF
$C_{rss}$	Reverse Transfer Capacitance			16		pF
$R_g$	Gate resistance	f=1MHz	0.3	0.65	1.2	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, I_D=20\text{A}$		67	95	nC
$Q_{gs}$	Gate Source Charge			19		nC
$Q_{gd}$	Gate Drain Charge			9		nC
$t_{D(\text{on})}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, R_L=2.5\Omega, R_{\text{GEN}}=3\Omega$		18		ns
$t_r$	Turn-On Rise Time			7		ns
$t_{D(\text{off})}$	Turn-Off DelayTime			30		ns
$t_f$	Turn-Off Fall Time			10		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=20\text{A}, \text{di}/\text{dt}=500\text{A}/\mu\text{s}$		42		ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, \text{di}/\text{dt}=500\text{A}/\mu\text{s}$		215		nC

A. The value of  $R_{\text{JJA}}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{\text{DSM}}$  is based on  $R_{\text{JJA}} \leq 10\text{s}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B. The power dissipation  $P_D$  is based on  $T_{J(\text{MAX})}=150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature  $T_{J(\text{MAX})}=150^\circ\text{C}$ .

D. The  $R_{\text{JJA}}$  is the sum of the thermal impedance from junction to case  $R_{\text{JJC}}$  and case to ambient.

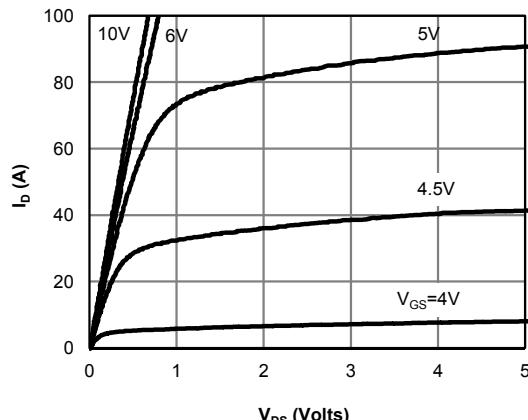
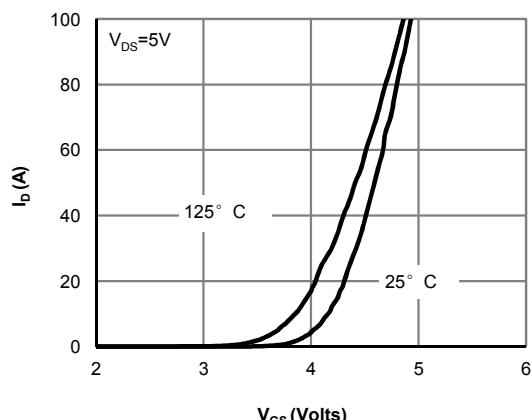
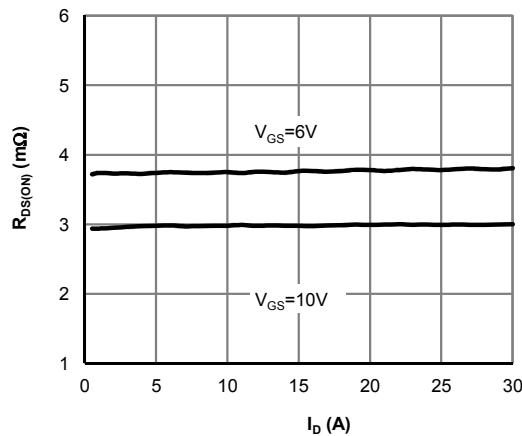
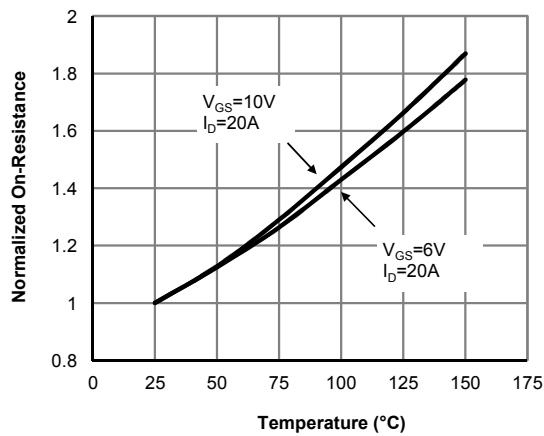
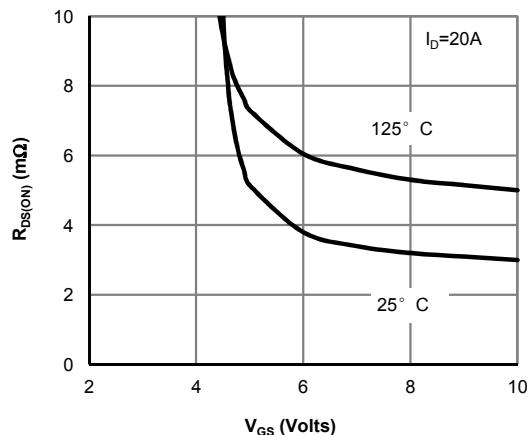
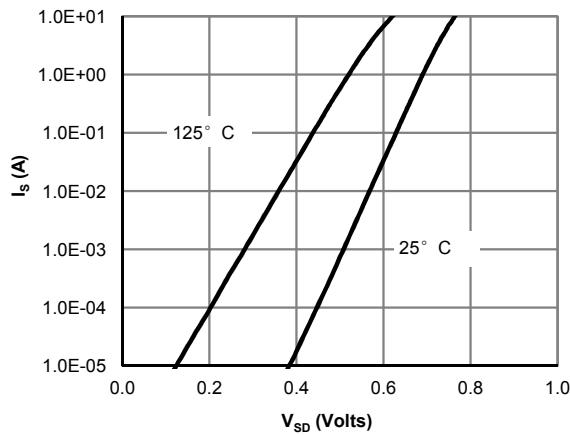
E. The static characteristics in Figures 1 to 6 are obtained using <300 $\mu\text{s}$  pulses, duty cycle 0.5% max.

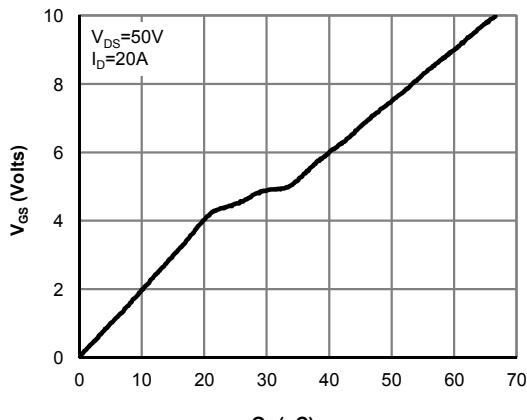
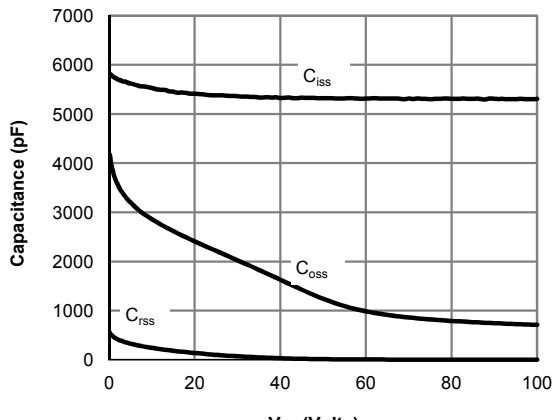
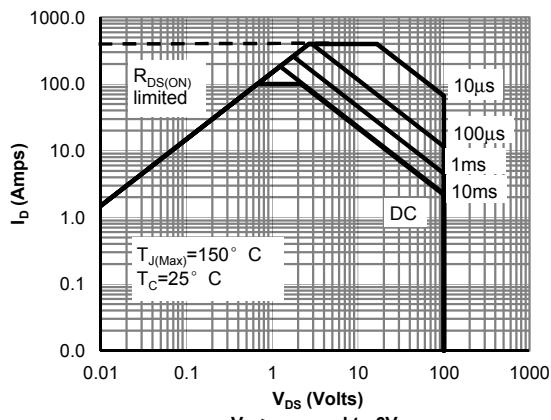
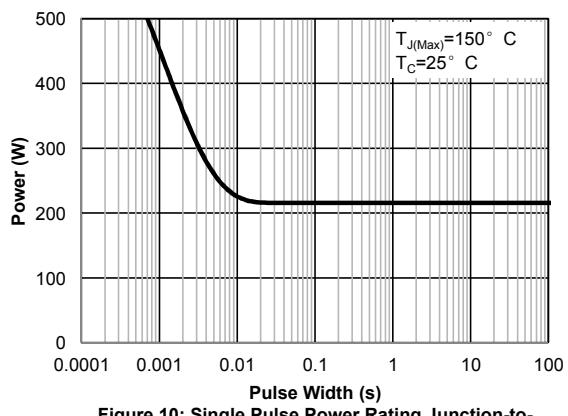
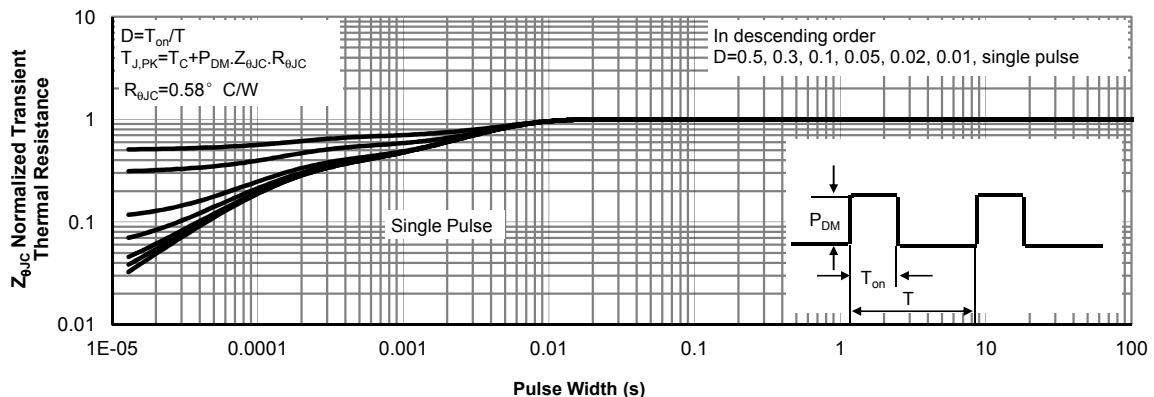
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(\text{MAX})}=150^\circ\text{C}$ . The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ .

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 1: On-Region Characteristics (Note E)**

**Figure 2: Transfer Characteristics (Note E)**

**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

**Figure 6: Body-Diode Characteristics (Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 7: Gate-Charge Characteristics**

**Figure 8: Capacitance Characteristics**

**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

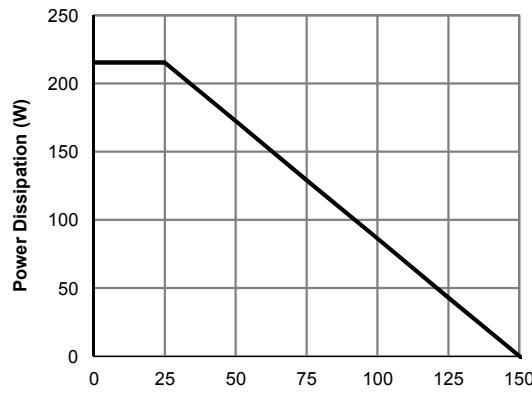
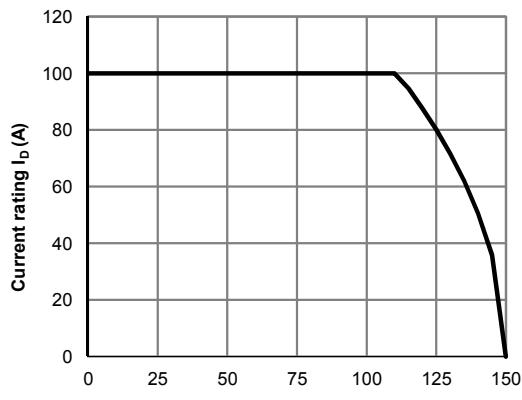
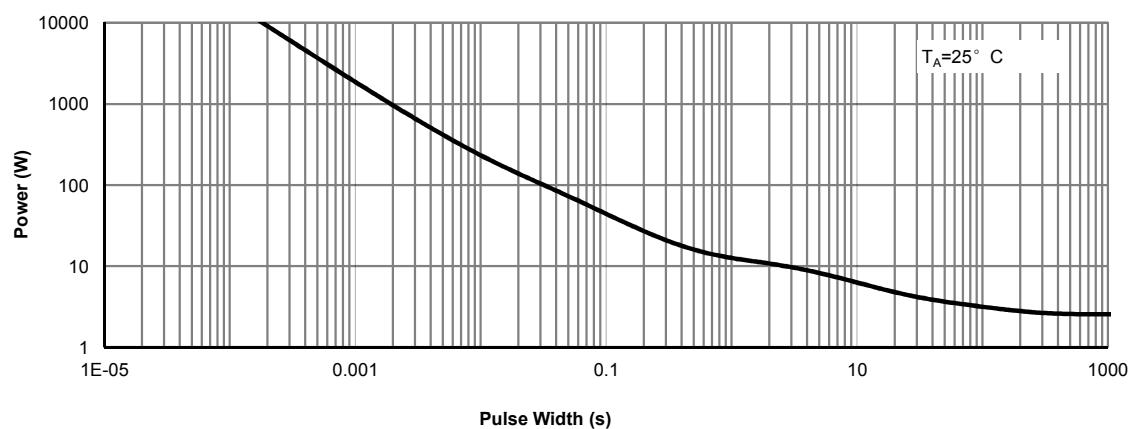
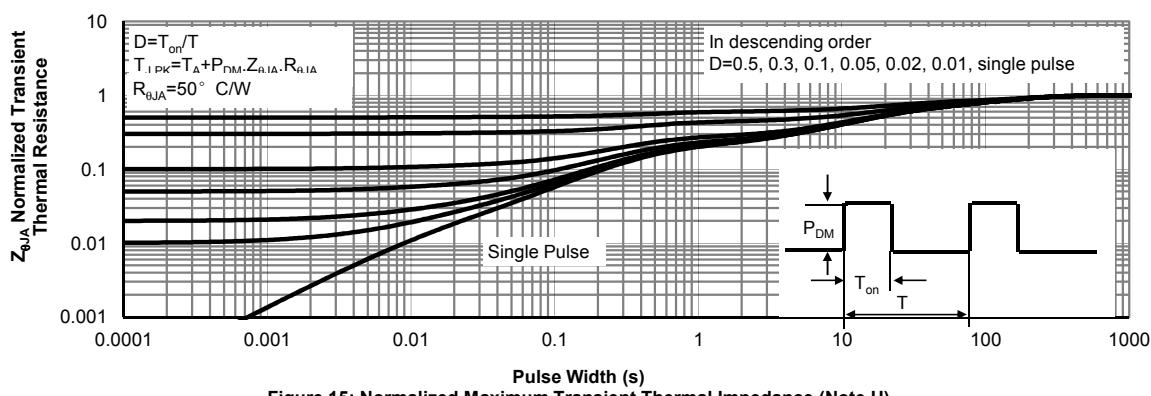
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 12: Power De-rating (Note F)**

**Figure 13: Current De-rating (Note F)**

**Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)**

**Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)**

Figure A: Gate Charge Test Circuit &amp; Waveforms

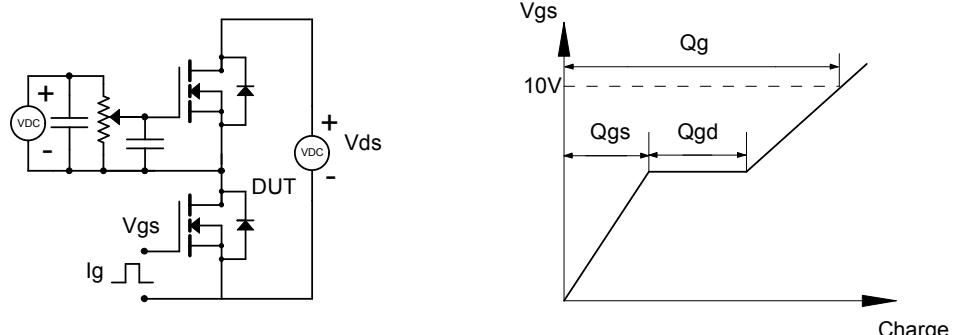


Figure B: Resistive Switching Test Circuit &amp; Waveforms

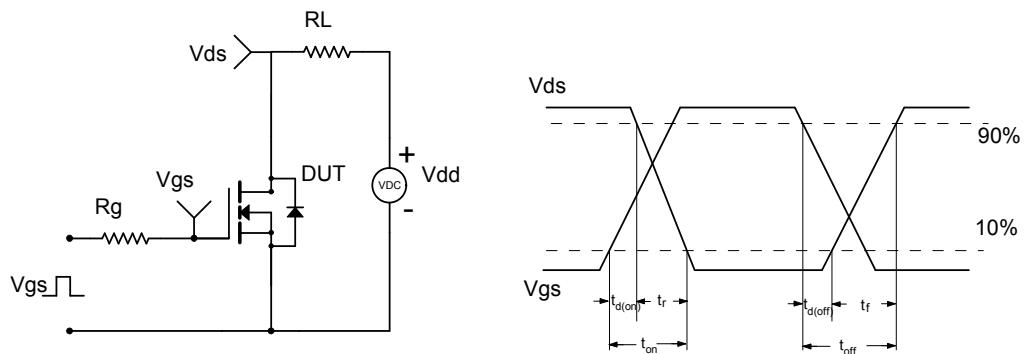


Figure C: Unclamped Inductive Switching (UIS) Test Circuit &amp; Waveforms

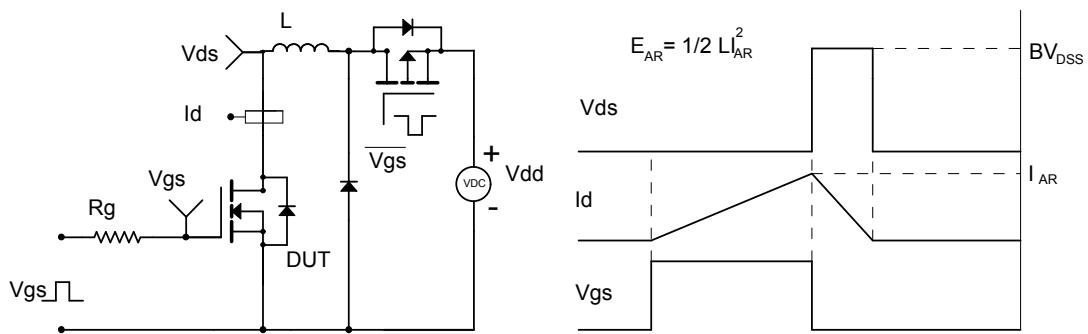
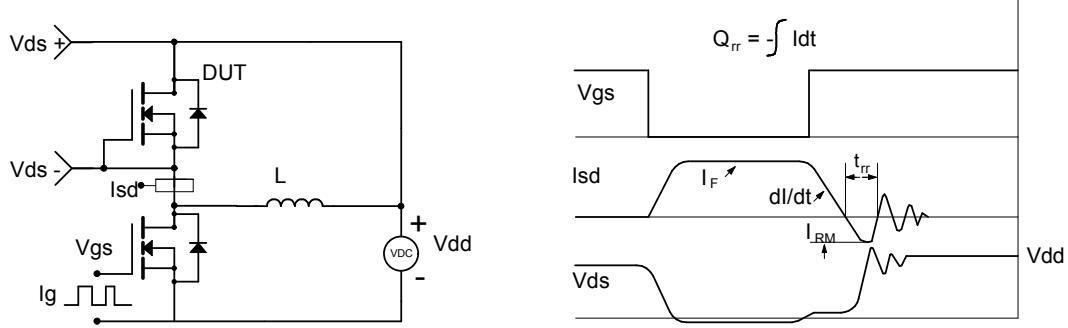


Figure D: Diode Recovery Test Circuit &amp; Waveforms



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