ALPHA & OMEGA SEMICONDUCTOR

AOSD26313C

30V Complementary MOSFET

General Description

- Latest Advanced Trench Technology
- Low $R_{DS(ON)}$
- High Current Capability
- RoHS and Halogen-Free Compliant

Applications

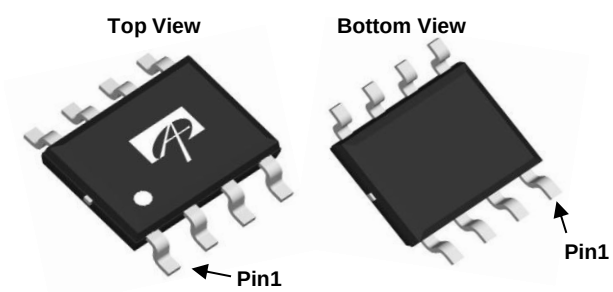
- Notebook AC-in Load Switch
- Battery Protection Charge/Discharge

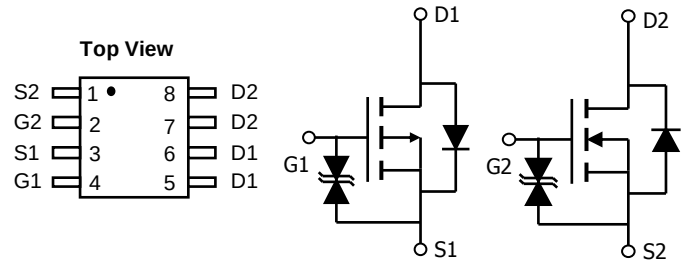
Product Summary

P-Channel	N-Channel
V_{DS}= -30V	V_{DS}= 30V
I_D=-5.7A (V_{GS}=-10V)	I_D= 7A (V_{GS}=10V)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 32mΩ (V_{GS}=-10V)	< 20mΩ (V_{GS}=10V)
< 55mΩ (V_{GS}=-4.5V)	< 26mΩ (V_{GS}=4.5V)
ESD protection	
100% UIS Tested	100% UIS Tested
100% R_g Tested	100% R_g Tested

Green Product

SO-8





Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOSD26313C	SO-8	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	-30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_A=25°C	I_D	-5.7	7	A
	T_A=70°C		-4.4	5.4	
Pulsed Drain Current [C]		I_{DM}	-23	34	
Avalanche Current [C]		I_{AS}	20	15	A
Avalanche energy	L=0.1mH [C]	E_{AS}	20	11	mJ
Power Dissipation [B]	T_A=25°C	P_D	1.7	1.7	W
	T_A=70°C		1.1	1.1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1	Max Q1	Typ Q2	Max Q2	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	52	70	52	70	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		80	100	80	100	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	35	45	35	45	°C/W

P-CH Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
advanced	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=-250µA	-1.2	-1.7	-2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-5.7A		25	32	mΩ
		T_J=125°C		32	41	
		V_{GS}=-4.5V, I_D=-4.4A		35	55	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-5.7A		17		S
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V		-0.8	-1	V
I_S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		1100		pF
C_{oss}	Output Capacitance			120		pF
C_{rss}	Reverse Transfer Capacitance			105		pF
R_g	Gate resistance	f=1MHz		11	18	Ω
SWITCHING PARAMETERS						
$Q_{g(10V)}$	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-5.7A		22	33	nC
$Q_{g(4.5V)}$	Total Gate Charge			11	18	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			6.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=2.63Ω, R_{GEN}=3Ω		12		ns
t_r	Turn-On Rise Time			9		ns
$t_{D(off)}$	Turn-Off DelayTime			55		ns
t_f	Turn-Off Fall Time			19		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-5.7A, di/dt=500A/µs		12		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-5.7A, di/dt=500A/µs		17		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

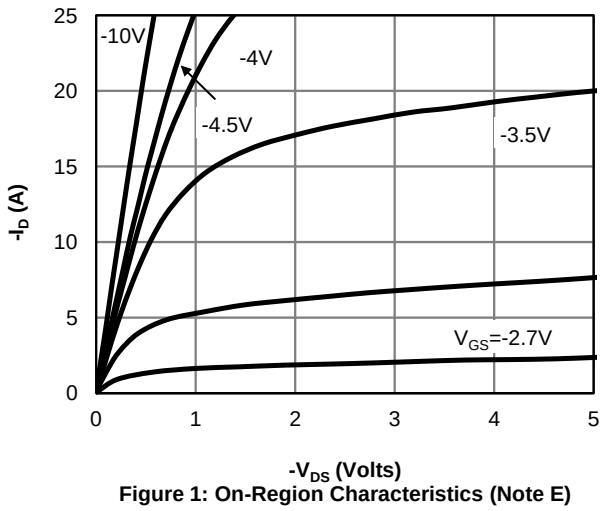


Figure 1: On-Region Characteristics (Note E)

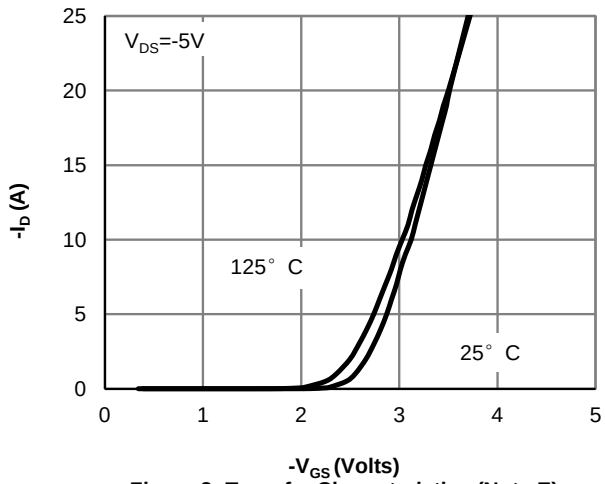


Figure 2: Transfer Characteristics (Note E)

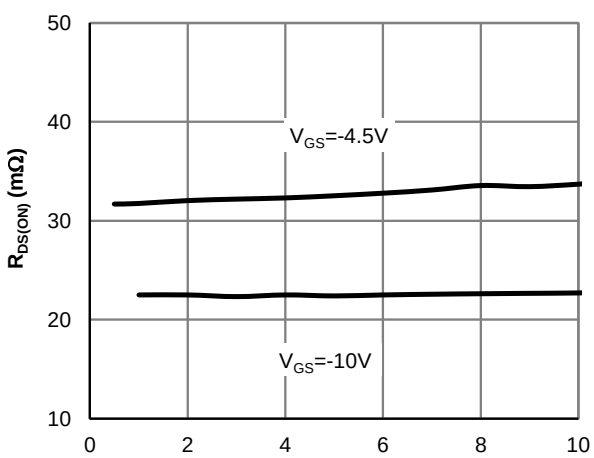


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

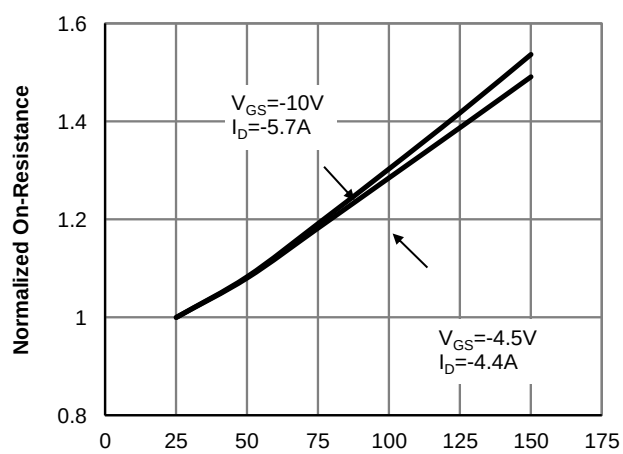


Figure 4: On-Resistance vs. Junction Temperature (Note E)

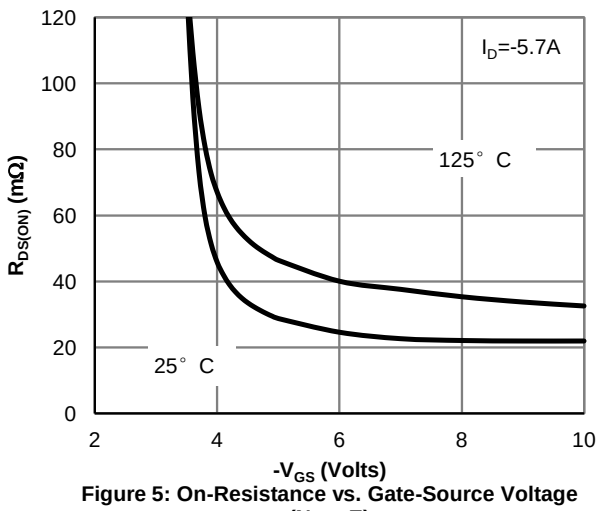


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

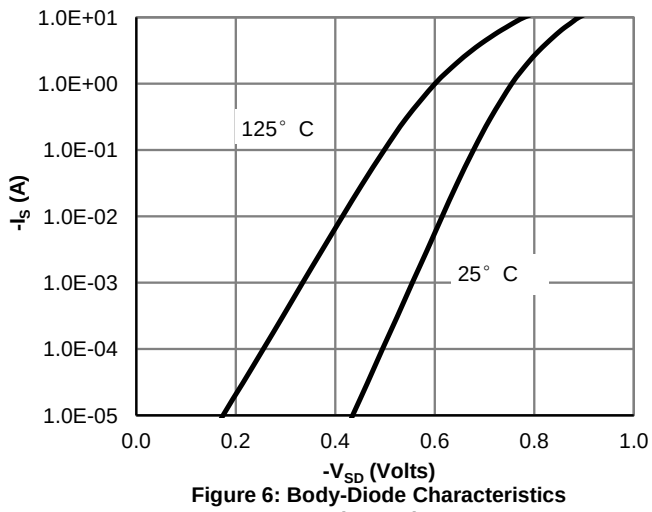


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

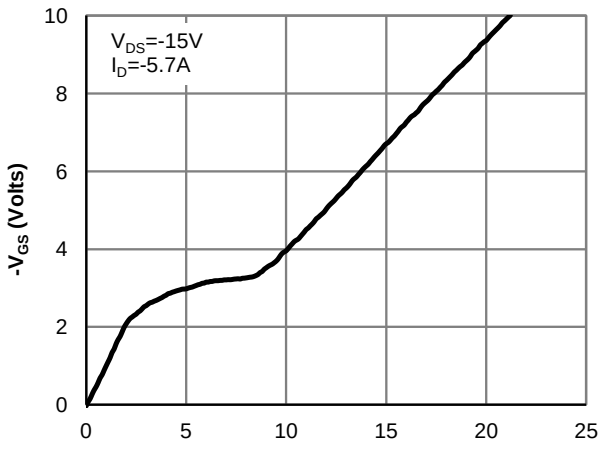


Figure 7: Gate-Charge Characteristics

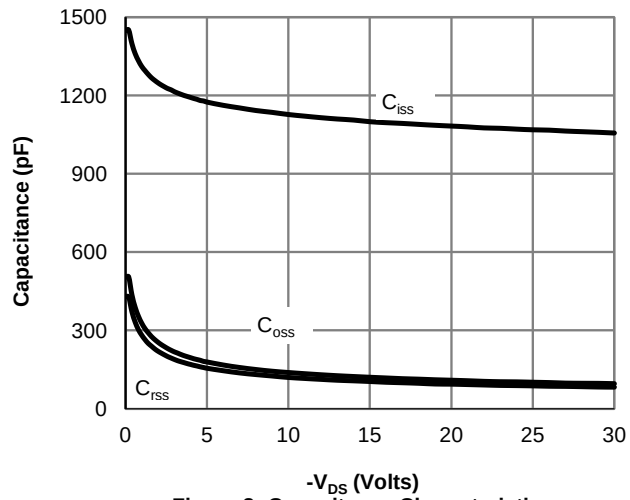
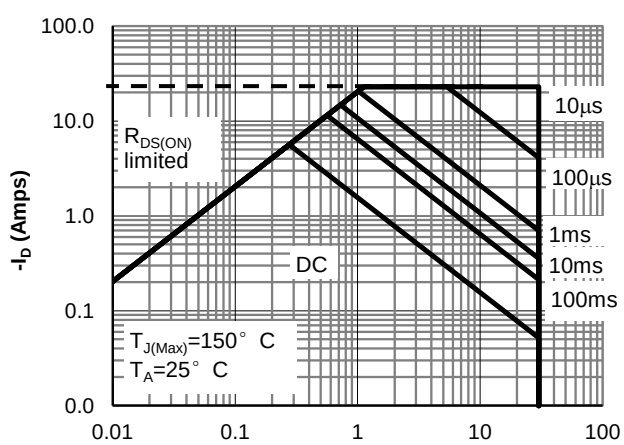


Figure 8: Capacitance Characteristics



V_{GS}> or equal to -4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

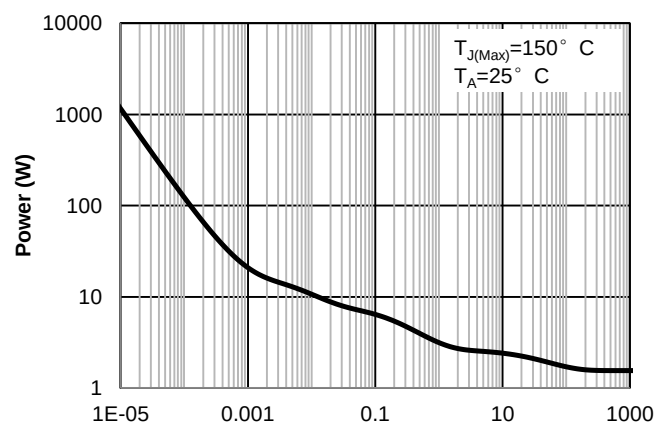


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

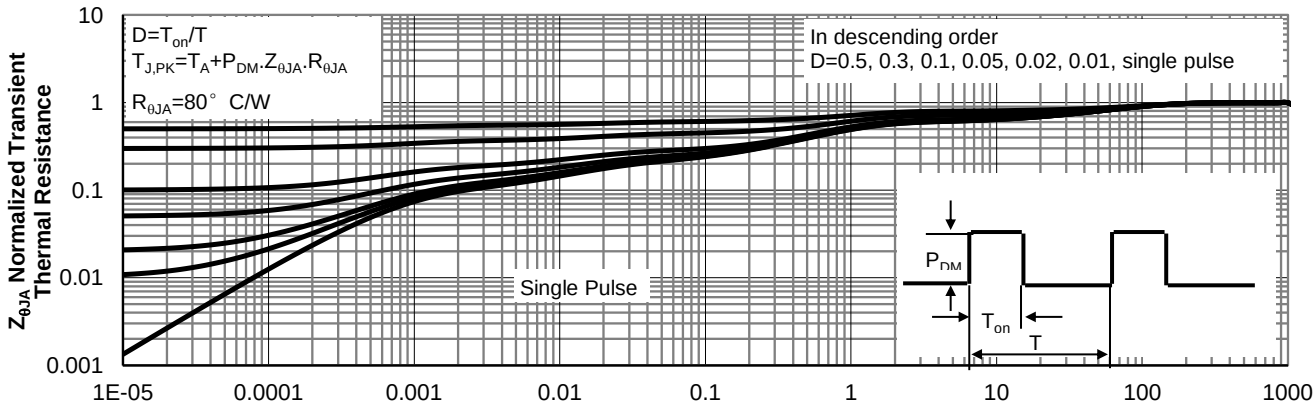
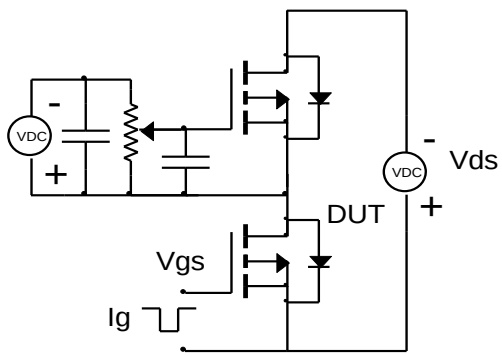
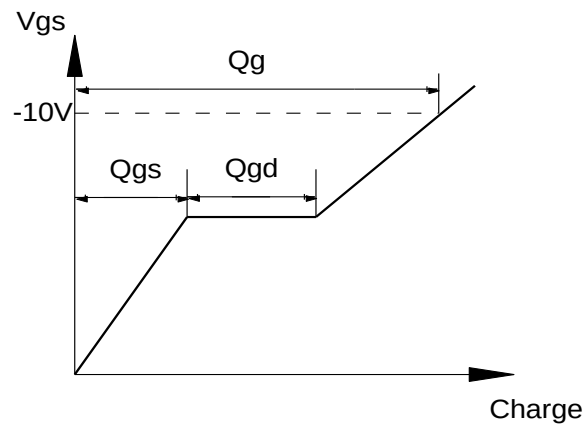


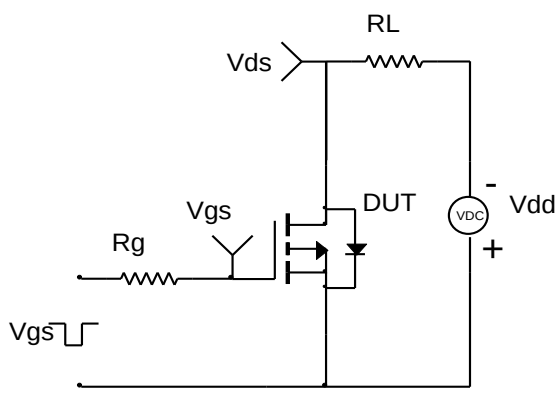
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

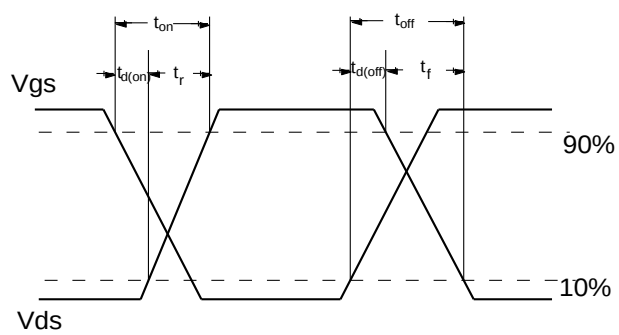
Gate Charge Test Circuit & Waveform



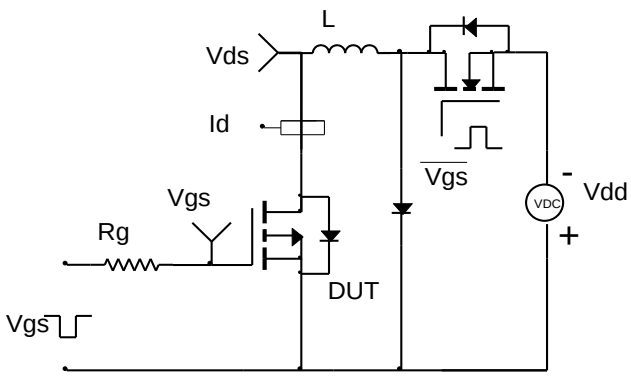


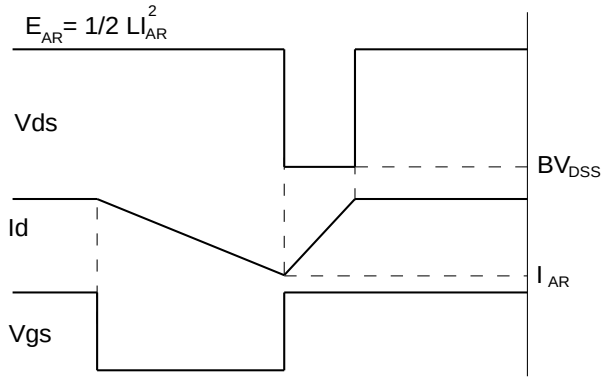
Resistive Switching Test Circuit & Waveforms



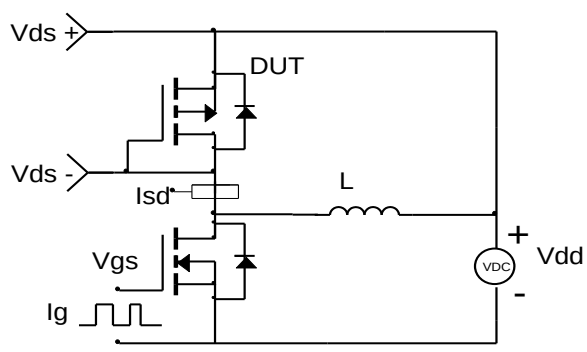


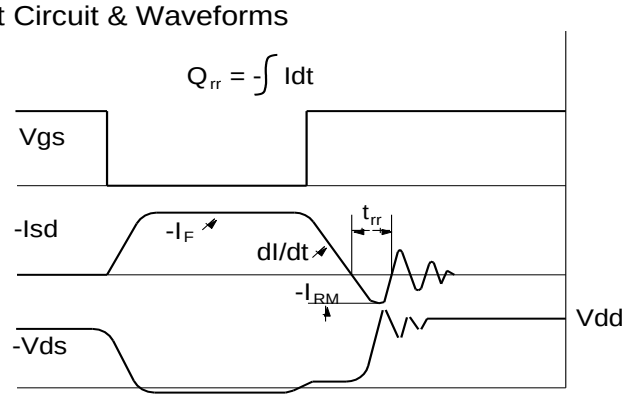
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





N-CH Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	ID=250µA, VGS=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1.3	1.8	2.3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=7A		16	20	mΩ
		T_J=125°C		24	30	
		V_{GS}=4.5V, I_D=6.3A		20	26	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=7A		33		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		600		pF
C_{oss}	Output Capacitance			70		pF
C_{rss}	Reverse Transfer Capacitance			60		pF
R_g	Gate resistance	f=1MHz	1.2	2.4	3.6	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=7A		12	20	nC
Q_g(4.5V)	Total Gate Charge			6	12	nC
Q_{gs}	Gate Source Charge			2.2		nC
Q_{gd}	Gate Drain Charge			2.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=2.143Ω, R_{GEN}=3Ω		4.5		ns
t_r	Turn-On Rise Time			4		ns
$t_{D(off)}$	Turn-Off DelayTime			20		ns
t_f	Turn-Off Fall Time			4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=7A, di/dt=500A/µs		5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=7A, di/dt=500A/µs		6		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

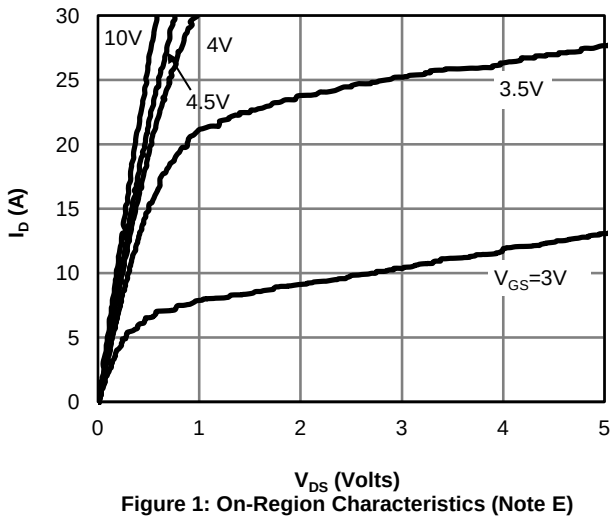


Figure 1: On-Region Characteristics (Note E)

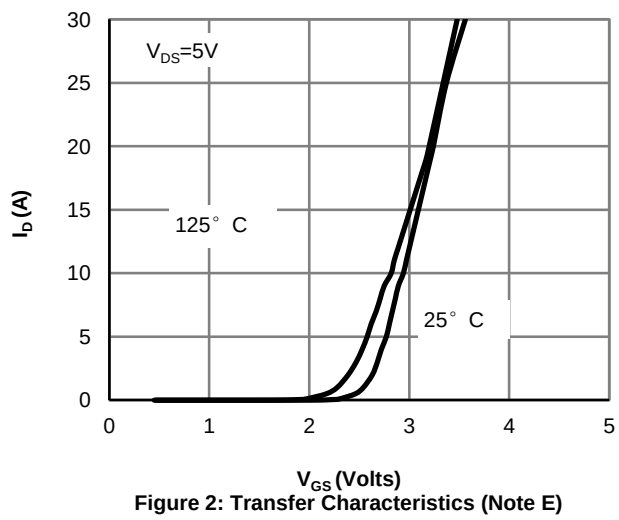


Figure 2: Transfer Characteristics (Note E)

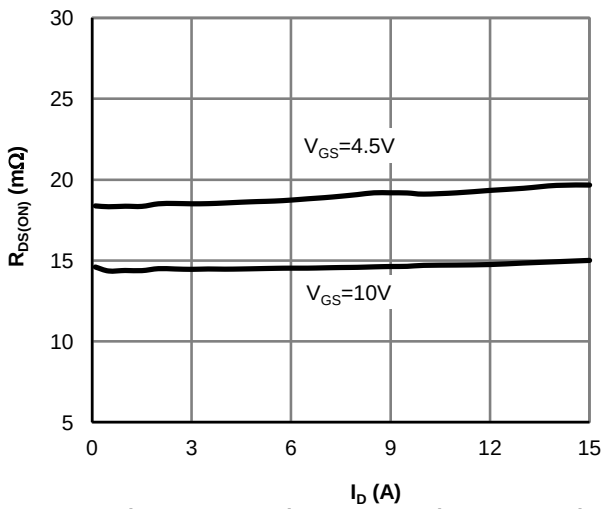


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

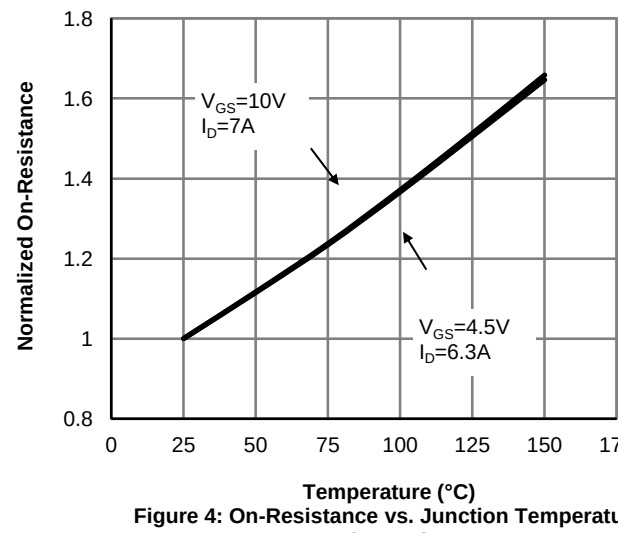


Figure 4: On-Resistance vs. Junction Temperature (Note E)

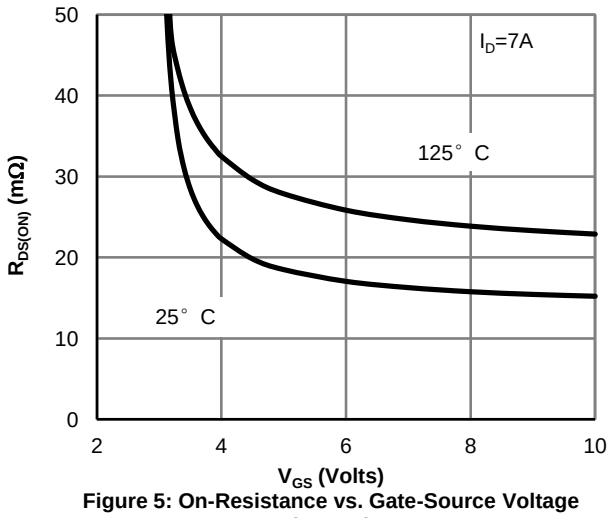


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

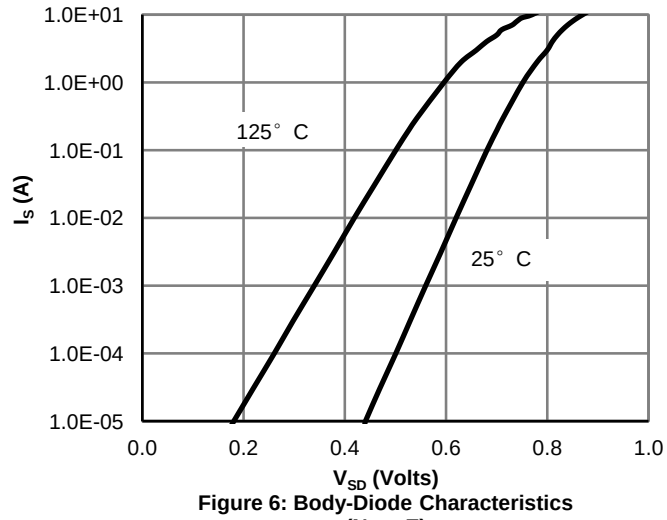


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

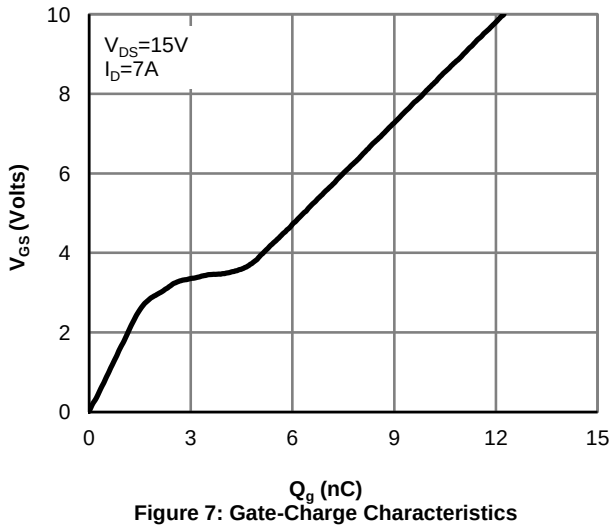


Figure 7: Gate-Charge Characteristics

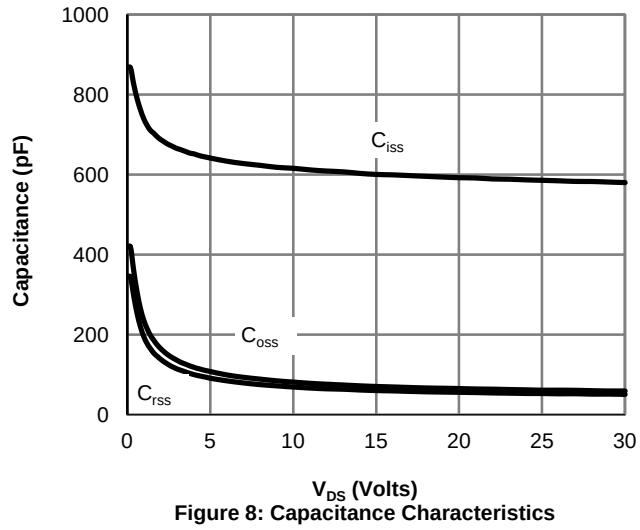
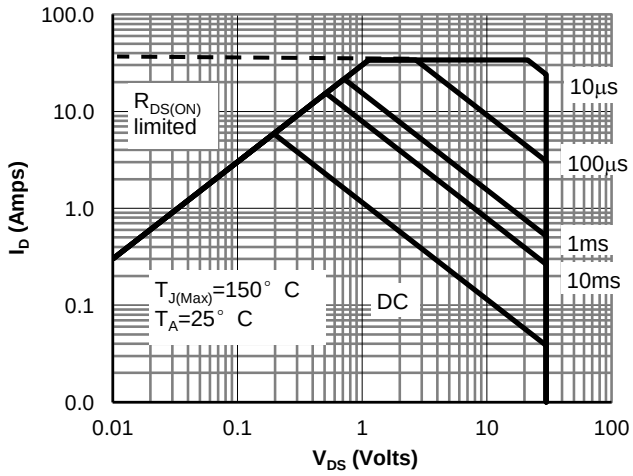


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

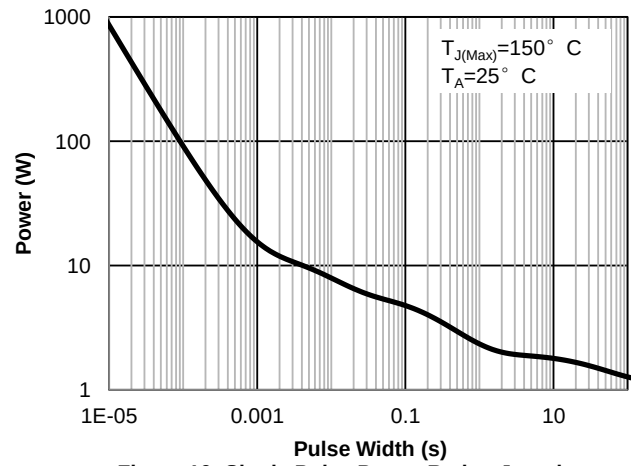


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

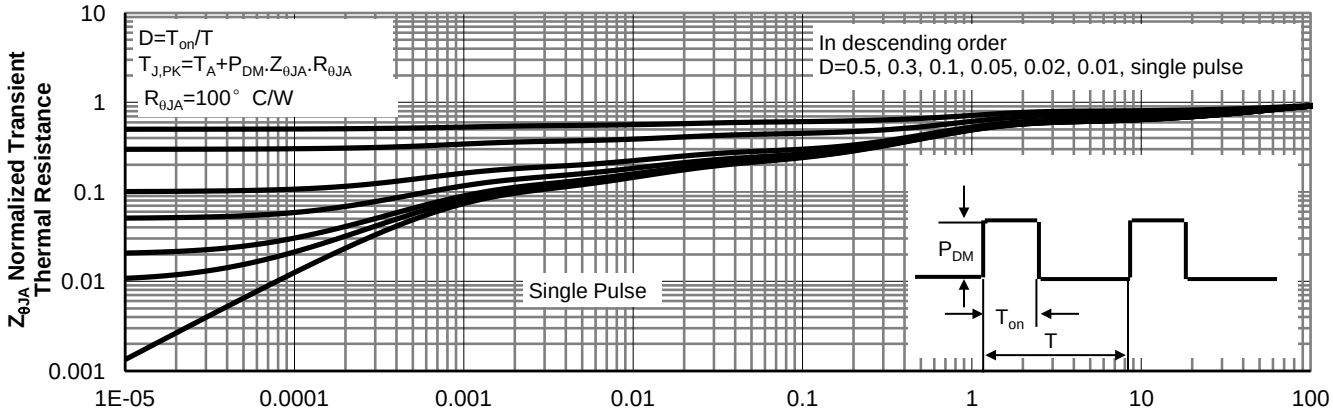


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Figure A: Gate Charge Test Circuit & Waveforms

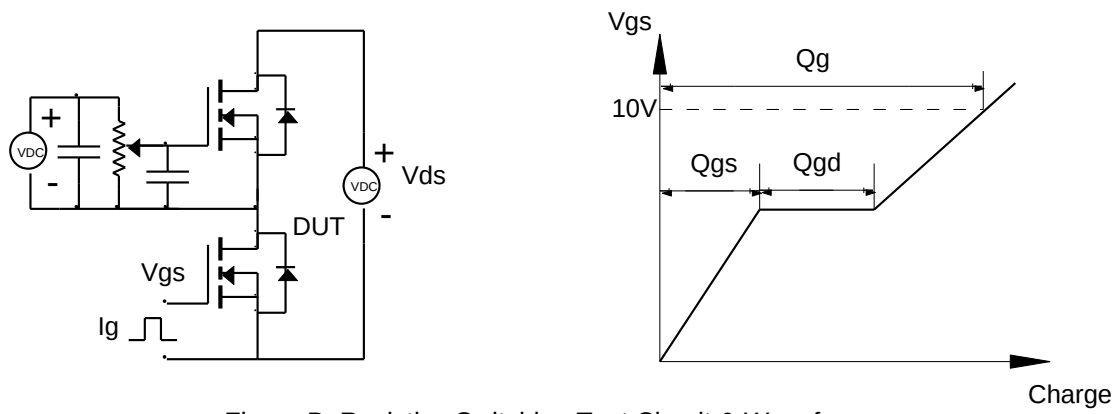


Figure B: Resistive Switching Test Circuit & Waveforms

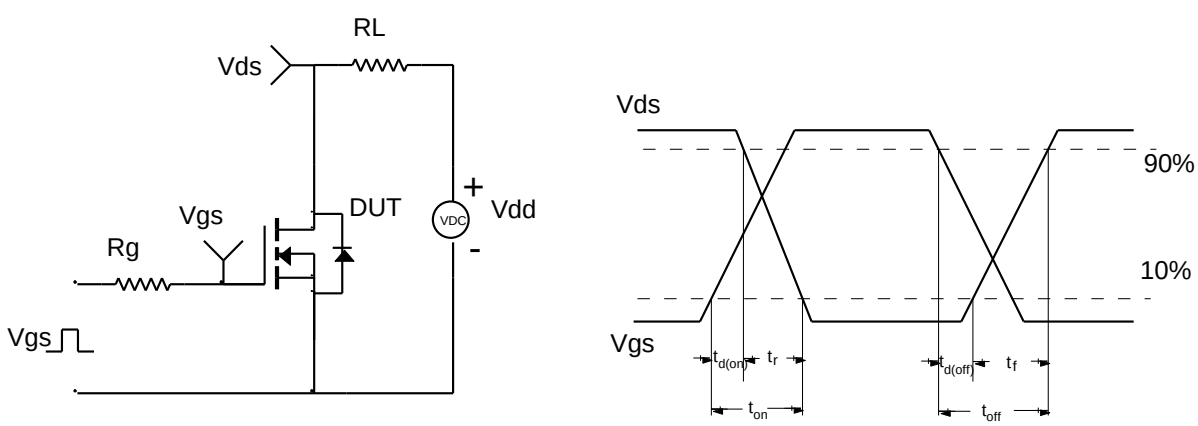


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

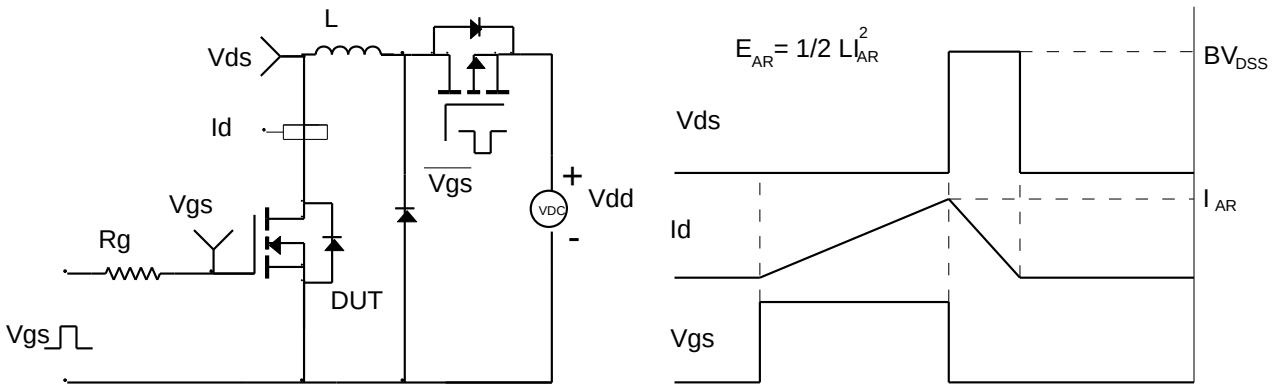
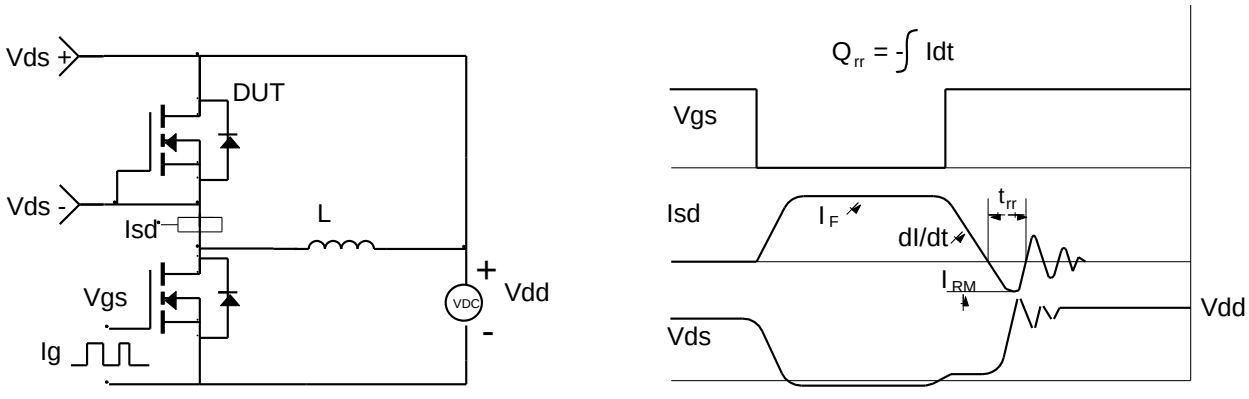


Figure D: Diode Recovery Test Circuit & Waveforms



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