ALPHA & OMEGA SEMICONDUCTOR

AOT42S60L/AOB42S60L
## 600V 37A αMOS^{TM} Power Transistor

General Description

The AOT42S60L & AOB42S60L have been fabricated using the advanced αMOS^{TM} high voltage process that is designed to deliver high levels of performance and robustness in switching applications.

By providing low $R_{DS(on)}$, Q_g and E_{OSS} along with guaranteed avalanche capability these devices can be adopted quickly into new and existing offline power supply designs.

Product Summary

V_{DS} @ $T_{j,max}$	700V
I_{DM}	166A
$R_{DS(ON),max}$	0.109Ω
$Q_{g,typ}$	40nC
E_{oss} @ 400V	9.2µJ

100% UIS Tested
100% R_g Tested

Green Product
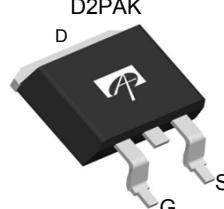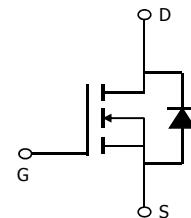
Top View

TO-220

AOT42S60L

TO-263 D2PAK

AOB42S60L

Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOT42S60L	TO-220 Green	Tube	1000
AOB42S60L	TO-263 Green	Tape & Reel	800

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	AOT42S60L/AOB42S60L	Units
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C=25°C	I_D	37	A
	T_C=100°C		23	
Pulsed Drain Current [C]		I_{DM}	166	
Avalanche Current [C]		I_{AR}	11	A
Repetitive avalanche energy [C]		E_{AR}	234	mJ
Single pulsed avalanche energy [G]		E_{AS}	1345	mJ
Power Dissipation [B]	T_C=25°C	P_D	417	W
	Derate above 25°C		3.3	W/ °C
MOSFET dv/dt ruggedness		dv/dt	100	V/ns
Peak diode recovery dv/dt [H]			20	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds [J]		T_L	300	°C

Thermal Characteristics

Parameter	Symbol	AOT42S60L/AOB42S60L	Units
Maximum Junction-to-Ambient [A,D]	$R_{\theta JA}$	65	°C/W
Maximum Case-to-sink [A]	$R_{\theta CS}$	0.5	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.3	°C/W

Electrical Characteristics (T$_J$=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V, T$_J$=25°C	600	-	-	V
		I$_D$=250µA, V$_{GS}$=0V, T$_J$=150°C	650	700	-	
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=600V, V$_{GS}$=0V	-	-	1	µA
		V$_{DS}$=480V, T$_J$=150°C	-	10	-	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$=±30V	-	-	±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=5V,I$_D$=250µA	2.5	3.2	3.8	V
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=21A, T$_J$=25°C	-	0.095	0.109	Ω
		V$_{GS}$=10V, I$_D$=21A, T$_J$=150°C	-	0.27	0.31	Ω
V$_{SD}$	Diode Forward Voltage	I$_S$=21A,V$_{GS}$=0V, T$_J$=25°C	-	0.84	-	V
I$_S$	Maximum Body-Diode Continuous Current		-	-	37	A
I$_{SM}$	Maximum Body-Diode Pulsed Current		-	-	166	A
DYNAMIC PARAMETERS						
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz	-	2154	-	pF
C$_{oss}$	Output Capacitance		-	135	-	pF
C$_{o(er)}$	Effective output capacitance, energy related [H]	V$_{GS}$=0V, V$_{DS}$=0 to 480V, f=1MHz	-	103	-	pF
C$_{o(tr)}$	Effective output capacitance, time related [I]		-	344	-	pF
C$_{rss}$	Reverse Transfer Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz	-	2.7	-	pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz	-	1.7	-	Ω
SWITCHING PARAMETERS						
Q$_g$	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=480V, I$_D$=21A	-	40	-	nC
Q$_{gs}$	Gate Source Charge		-	11.7	-	nC
Q$_{gd}$	Gate Drain Charge		-	11.9	-	nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=400V, I$_D$=21A, R$_G$=25Ω	-	38.5	-	ns
t$_r$	Turn-On Rise Time		-	53	-	ns
t$_{D(off)}$	Turn-Off DelayTime		-	136	-	ns
t$_f$	Turn-Off Fall Time		-	46	-	ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=21A,dI/dt=100A/µs,V$_{DS}$=400V	-	473	-	ns
I$_{rm}$	Peak Reverse Recovery Current	I$_F$=21A,dI/dt=100A/µs,V$_{DS}$=400V	-	38.5	-	A
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=21A,dI/dt=100A/µs,V$_{DS}$=400V	-	10.5	-	µC

A. The value of R$_{θJA}$ is measured with the device in a still air environment with T$_A$=25° C.
B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150° C, Ratings are based on low frequency and duty cycles to keep initial T$_J$ =25° C.
D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. L=60mH, I$_{AS}$=6.7A, V$_{DD}$=150V, Starting T$_J$=25° C
H. C$_{o(er)}$ is a fixed capacitance that gives the same stored energy as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.
I. C$_{o(tr)}$ is a fixed capacitance that gives the same charging time as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.
J. Wavesoldering only allowed at leads.
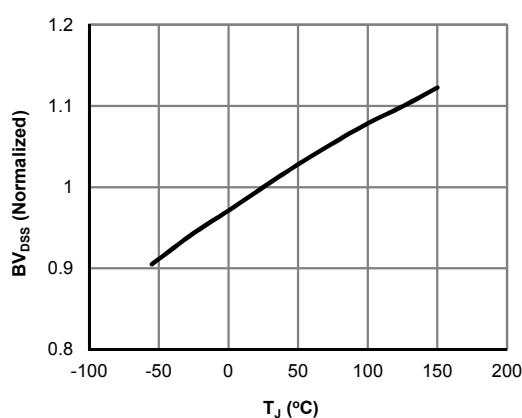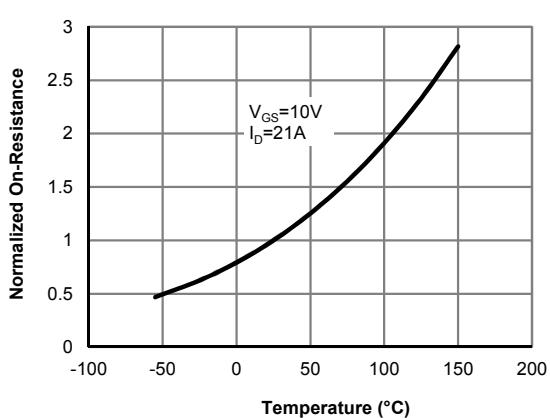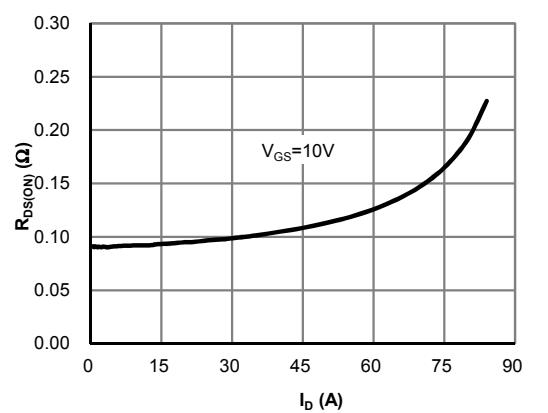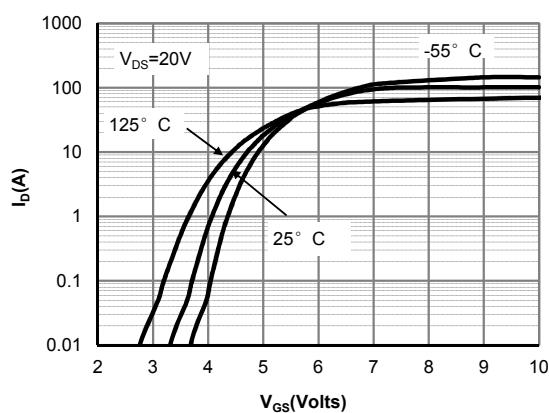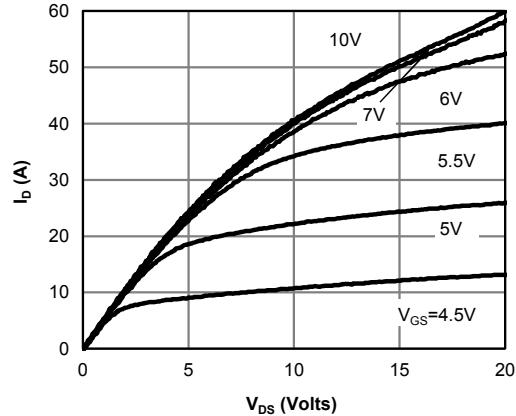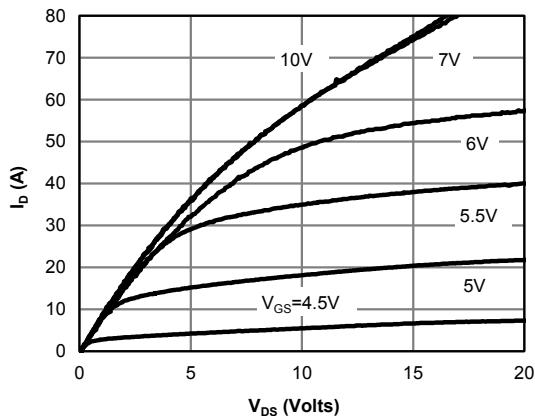
## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

**Figure 1: On-Region Characteristics@25°C**

**Figure 2: On-Region Characteristics@125°C**

**Figure 3: Transfer Characteristics**

**Figure 4: On-Resistance vs. Drain Current and Gate Voltage**

**Figure 5: On-Resistance vs. Junction Temperature**

Figure 6: Break Down vs. Junction Temperature

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
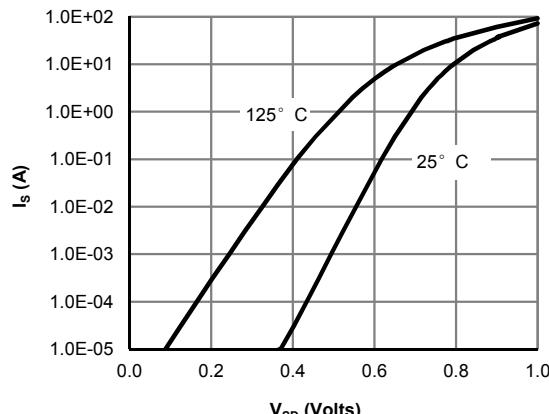
Figure 7: Body-Diode Characteristics (Note E)
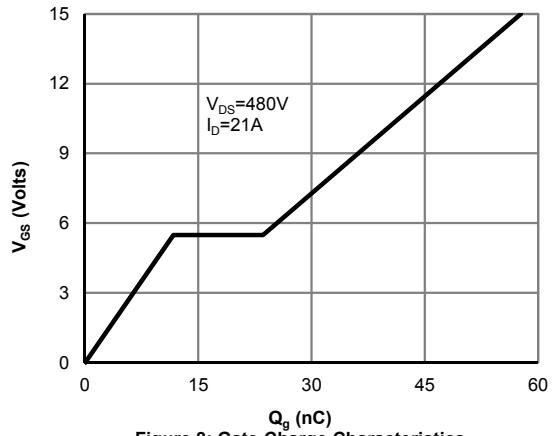
Figure 8: Gate-Charge Characteristics
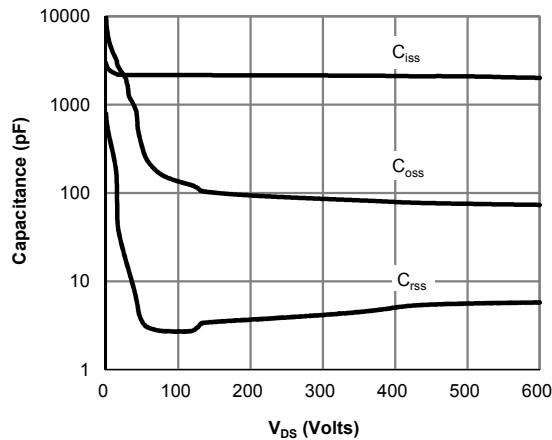
Figure 9: Capacitance Characteristics
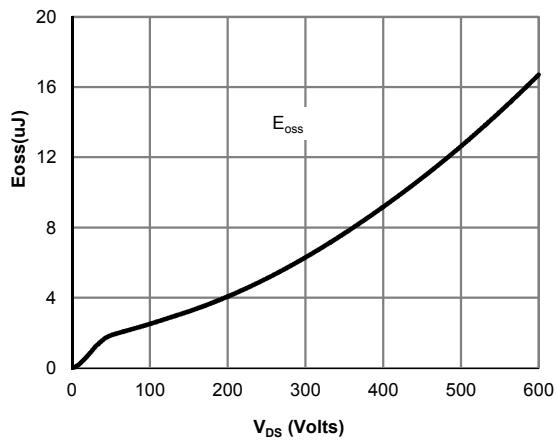
Figure 10: Coss stored Energy
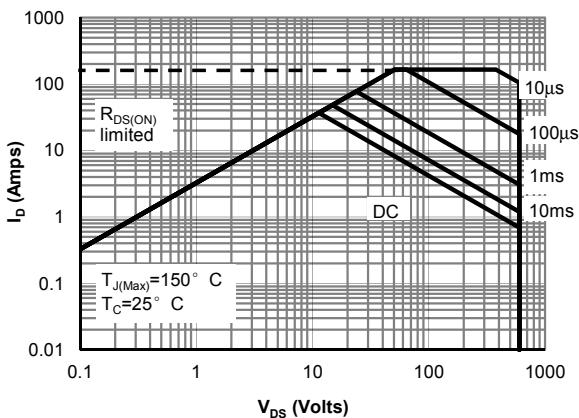
Figure 11: Maximum Forward Biased Safe
Operating Area for AOT(B)42S60L(Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
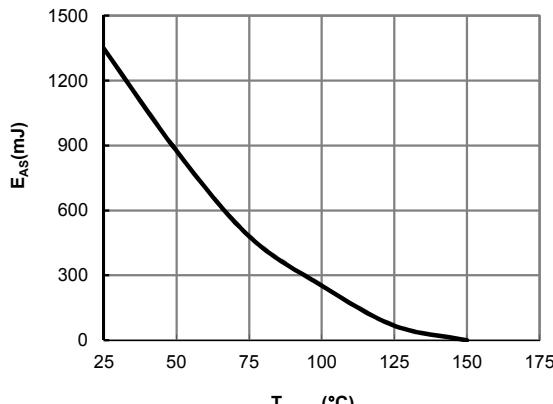

Figure 12: Avalanche energy
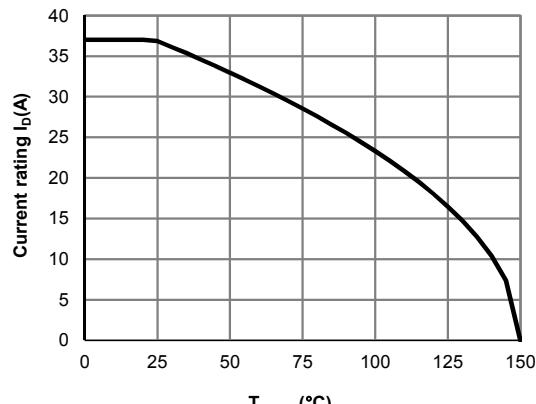
Figure 13: Current De-rating (Note B)

$D=T_{on}/T$
$T_{J,PK}=T_C+P_{DM}\cdot Z_{\theta JC}\cdot R_{\theta JC}$
$R_{\theta JC}=0.3^\circ$ C/W

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse
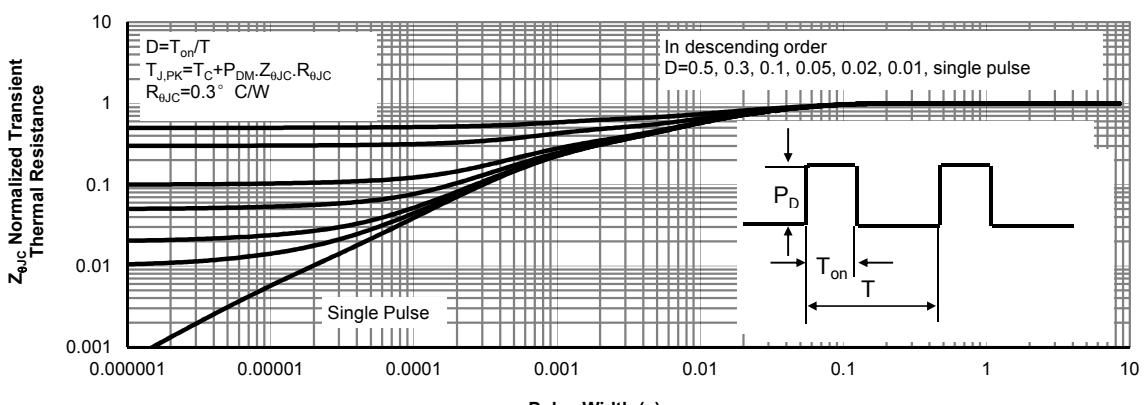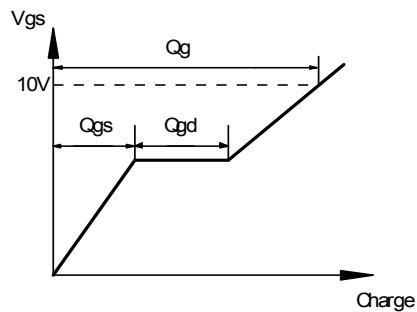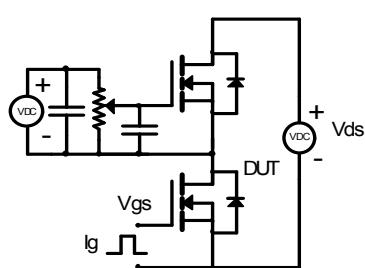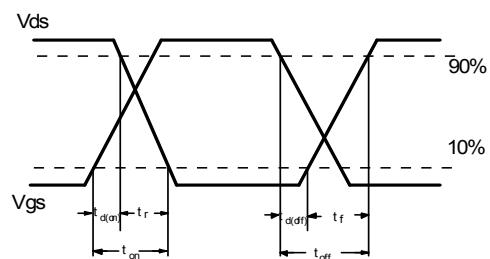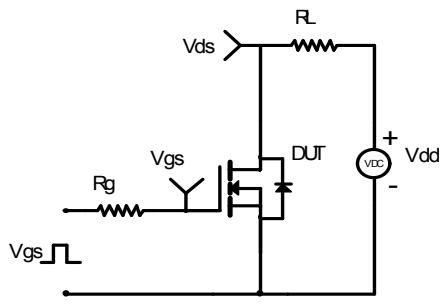
Pulse Width (s)
Figure 14: Normalized Maximum Transient Thermal Impedance for AOT(B)42S60L(Note F)
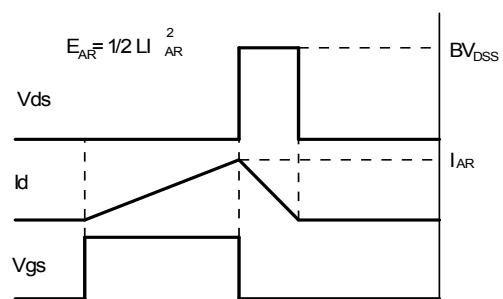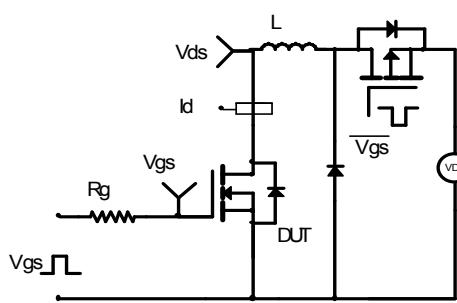
Gate Charge Test Circuit & Waveform
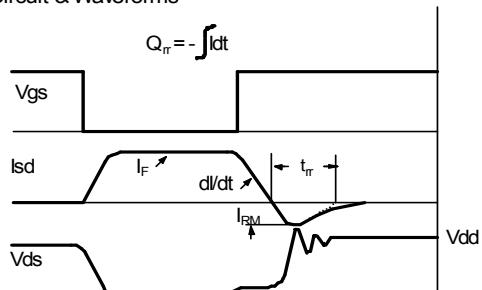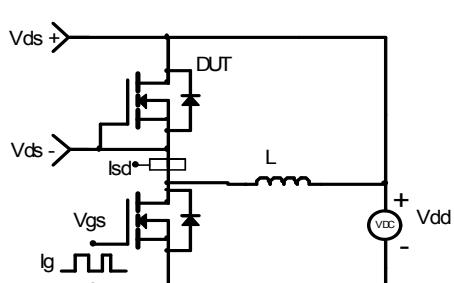
Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2 \, LI^2_{AR}$$

Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int I \, dt$$

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