Document Title

High Performance 315/433/868/915MHz FSK/GFSK Transceiver with 2K ~ 250Kbps

Revision History

Rev. No.	History	Issue Date	Remark
0.1	Initial issue	Feb., 2011	Preliminary,
0.2	Update technical data and add GFSK modulation.	Apr., 2011	
0.3	Add TX power setting and modify Figure 12.2	July, 2011	
0.4	Modify GRS bit (00h), Figure 12.2, Strobe command and tape reel information. Add Shenzhen office address.	July, 2011	
0.5	Modify TX matching (L2) to reduce TX current for 868MHz. Add 315MHz RF data and schematic.	Sep., 2011	
0.6	Modify description of CH9 (PLL II, WRCKS, PCS), Ch 12 and Ch 13. Correct Figure 12.1.	Jan., 2012	

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1. General Description

A7108 is a monolithic low-IF architecture CMOS FSK/GFSK TRX for wireless applications in the 315/433/470/510/868/915MHz ISM bands. In addition, this device is especially suitable for the 470MHz ~ 510MHz wireless AMR (Auto Meter Reading) in China.

A7108 is one of AMICCOM's high performance Sub 1GHz family chips. This device offers a low cost solution with advanced radio features such as high output power amplifier up to 20 dBm (433MHz band, excluding LPF and HPF) and low phase noise receiver (- 114 dBm @ 10Kbps, -110dBm @50Kbps). Therefore, A7108 is very suitable for long LOS (line-of-sight) applications without the need to add an external LNA or PA.

The on-chip data rate divider supports programmable on-air data rates from 2K to 250Kbps to satisfy different system requirements. For a battery powered system, A7108 supports fast PLL settling time (35 us), Xtal settling time (500 us) and on-chip Regulator settling time (450 us) to reduce average power consumption.

For packet handling, A7108 supports direct mode as well as FIFO mode. In the RX direct mode, GIO1 or GIO2 can be serially output the raw data from the digital demodulator. In the TX direct mode, MCU can serially feed the digital data to GIO1 or GIO2 which is connected to the modulator. In the other hand, a packet in FIFO mode, the preamble is self generated and the physical packet ID is programmable up to 8 bytes. The built-in separated 64-bytes TX/RX FIFO is treated as payload for data buffering including CRC of error detection, FEC of error correction, data whitening for data encryption / decryption, and Manchester encoding.

Additional device features such as on-chip regulator, low battery detect, carrier detect, preamble detect, frame sync in FIFO mode, AGC (Auto Gain Control), AFC (Auto Frequency compensation), Auto calibration (VCO and IF Filter), programmable IF Filter, multi Xtal sources, on-chip Xtal compensated capacitors, and RSSI for the clear channel assistance are used to simplify system development and cost. Overall, A7108 is a high performance and a highly integrated ISM bands TRX with low BOM cost.

2. Typical Applications

- Wireless ISM band data communication
- Remote Control
- RKE (Remote Keyless Entry)
- Wireless Energy Management
- Home Automation
- AMR (Auto Meter Reading)

3. Features

- Small size (QFN 4X4, 20 pins).
- Frequency band: 315/433/470/868/915 MHz.
- FSK and GFSK modulation.
- Supports 3-wire or 4-wire SPI.
- Deep sleep current (0.2uA).
- Low sleep current (2 uA).
- TX Current consumption 433MHz: 30mA @ 10dBm, 70mA @ 17dBm.
- TX Current consumption 868MHz: 37mA @ 10dBm, 52mA @ 13dBm.
- RX Current consumption (AGC Off) 434MHz: 13.5 mA and 868MHz: 14 mA.
- On chip regulator, supports input voltage 2.0 ~ 3.6 V.
- Programmable data rate from 2Kbps to 250Kbps.
- Physical 64 bytes TX/RX FIFO buffers.
- FIFO extension up to 256 bytes.
- High RX sensitivity 433.92MHz.
  - -117dBm at 2Kbps on-air data rate.
  - -114dBm at 10Kbps on-air data rate.
  - -110dBm at 50Kbps on-air data rate.
  - -107dBm at 100Kbps on-air data rate.
  - -106dBm at 150Kbps on-air data rate.
  - -103dBm at 250Kbps on-air data rate.
- Fast PLL settling time (35 us).
- On-chip full range VCO and Fractional-N PLL synthesizer.
- On-chip low power RC oscillator for WOR (Wake on RX) function.
- AFC (Auto Frequency Compensation) for frequency drift due to Xtal aging.
- Supports low cost crystal (12,8 / 16 MHz).
- On chip 9-bit ADC and RSSI (Received Signal Strength Indicator).
- Programmable IF filter bandwidth (50K / 100K / 150KHz / 250KHz).
- Programmable threshold of carrier detect.

- Frame synchronization recognition in FIFO mode.
- FEC / Manchester / data whitening / CRC-16 (CRC-CCITT).

4. Pin Configurations

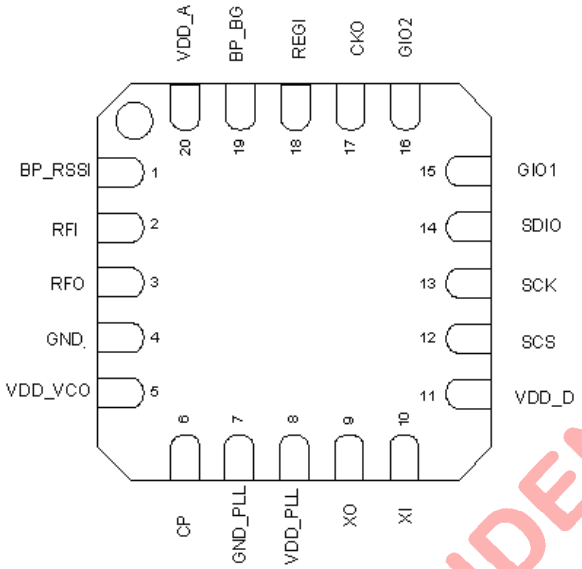


Figure 4.1 QFN4x4 Package Top View

5. RF Chip Block Diagram

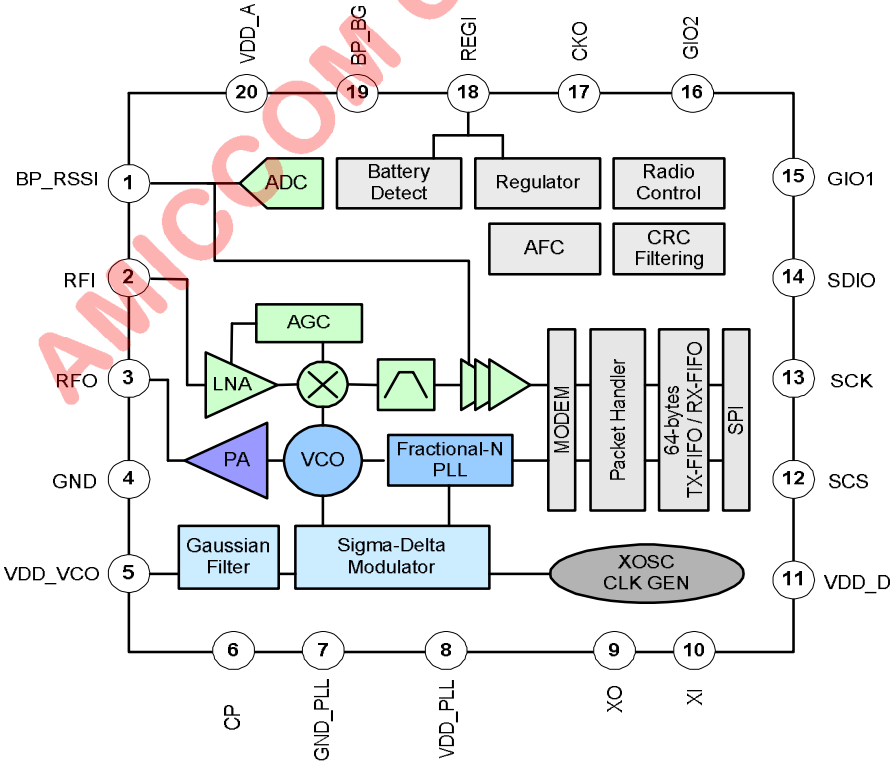


Figure 5.1 Block Diagram

6. Pin Descriptions

Note: I (input), O(output), G(Ground), D(Digital).

Pin No.	Symbol	I/O	Function Description
1	BP_RSSI	I/O	I: ADC input. O: RSSI bypass. Connect to bypass capacitor.
2	RFI	I	RF input. Connect to matching circuit.
3	RFO	O	RF output. Connect to matching circuit. (recommend powered by VDD directly).
4	GND	G	Ground.
5	VDD_VCO	I	VCO supply voltage input.
6	CP	O	Charge-pump output. Connect to loop filter.
7	GND_PLL	O	PLL ground pin.
8	VDD_PLL	I	PLL supply voltage input driven by pin 11, VDD_D.
9	XO	O	Crystal oscillator output. Connect to tank capacitor.
10	XI	I	Crystal oscillator input. Connect to tank capacitor.
11	VDD_D	O	Digital supply voltage output. Connect to bypass capacitor.
12	SCS	DI	SPI chip select input.
13	SCK	DI	SPI clock input.
14	SDIO	DI/O	SPI data IO.
15	GIO1	DI/O	Multi-function IO 1 / SPI data output.
16	GIO2	DI/O	Multi-function IO 2 / SPI data output.
17	CKO	DO	Multi-function clock output.
18	REGI	I	Regulator input. Connect to VDD supply.
19	BP_BG	O	Band-gap bypass. Connect to bypass capacitor.
20	VDD_A	O	Analog supply voltage output. Connect to bypass capacitor.
	Back side plate	**G**	**Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

7. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Max. Input RF level		10	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM*	± 2K	V
	MM*	± 100	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).
* RFO pin is MM ± 25V and HBM ± 500V

8. Specification

(Ta=25℃, **VDD=3.3V**, F_{XTAL} =12.8MHz, FSK modulation with Matching circuit and low/high pass filter, On Chip Regulator = **1.8V**, **RFO is powered by VDD = 3.3V**, unless otherwise noted.)

Parameter	Description	Min.	Typ.	Max.	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage		2.0	3.3	3.6	V
Current Consumption	Deep Sleep Mode (no register retention) [1]		0.2		uA
	Sleep Mode [1]		2		uA
	Idle Mode(Xtal off)		0.25		mA
	Standby Mode(Xtal on)		1.5		mA
Current Consumption 433MHz band	PLL mode		8.5		mA
	RX mode (AGC Off)		13.5		mA
	RX mode (AGC On)		14.5		mA
	TX -12dBm (TBG=0, TDC=0, PAC=0)		16		mA
	TX 1dBm (TBG=1, TDC=0, PAC=0)		20		mA
	TX 5dBm (TBG=2, TDC=0, PAC=0)		22		mA
	TX 10dBm (TBG=3, TDC=0, PAC=0)		30		mA
	TX 13dBm (TBG=4, TDC=0, PAC=0)		39		mA
	TX 15dBm (TBG=5, TDC=0, PAC=0)		48		mA
	TX 16dBm (TBG=6, TDC=0, PAC=0)		55		mA
	TX 17dBm (TBG=7, TDC=2, PAC=1)		70		mA
	TX 17.5dBm (TBG=7, TDC=3, PAC=3)		78		mA
Current Consumption 315MHz band	TX 20dBm (TBG=7, TDC=2, PAC=1) Without LPF and HPF.		70		mA
Current Consumption 868MHz band	PLL mode		8.5		mA
	RX mode (AGC Off)		14		mA
	RX mode (AGC On)		15.5		mA
	TX -16dBm (TBG=0, TDC=0, PAC=0)		16		mA
	TX -2dBm (TBG=3, TDC=0, PAC=0)		20		mA
	TX 2dBm (TBG=4, TDC=0, PAC=0)		23		mA
	TX 6dBm (TBG=5, TDC=0, PAC=0)		29		mA
	TX 10dBm (TBG=6, TDC=0, PAC=0)		37		mA
	TX 12dBm (TBG=7, TDC=0, PAC=0)		45		mA
	TX 13dBm (TBG=6, TDC=1, PAC=0)		52		mA
	TX 15dBm (TBG=7, TDC=1, PAC=0)		60		mA
	TX 16dBm (TBG=7, TDC=2, PAC=0)		70		mA
	TX 17dBm (TBG=7, TDC=3, PAC=0)		75		mA
	TX 18dBm (TBG=7, TDC=2, PAC=3)		93		mA
Phase Locked Loop					
X'TAL Settling Time [2]	Idle to standby, 49US type		0.5		ms
X'TAL frequency	General case		**12.8**/16		MHz
	Data rate = 250Kbps		16		MHz
	Data rate = 32.768K or 16.384Kbps		12.582912		MHz
	Data rate = 38.4Kbps		19.6608		MHz

X'TAL ESR				100	Ohm
X'TAL Capacitor Load (Cload)	Recommended		20		pF
433MHz PLL Phase noise (loop component: R1=820,C1=33nF,C2=2.2nF)	PN @100k offset		90		dBc/Hz
	PN @1M offset		110		dBc/Hz
	PN @10M offset		130		dBc/Hz
868MHz PLL Phase noise (loop component: R1=560,C1=47nF,C2=3.3nF)	PN @100k offset		85		dBc/Hz
	PN @1M offset		105		dBc/Hz
	PN @10M offset		125		dBc/Hz
PLL Settling Time @settle to 25kHz	Standby to PLL		35		us
Reference spur			80		dBc
Transmitter					
TX Power Range	433MHz (excluding LPF and HPF)	-12	13	20	dB
	868MHz (excluding LPF and HPF)	-16	12	20	dB
TX Settling Time	PLL to TX		30		µs
TX Spurious Emission 1. Pout = 12 dBm 2. With LPF and HPF	f < 1GHz (RBW =100kHz)			-36	dBm
	47MHz< f <74MHz 87.5MHz< f <118MHz 174MHz< f <230MHz 470MHz< f <862MHz (RBW =100kHz)			-54	dBm
	Above 1GHz (RBW = 1MHz)			-30	dBm
	2nd Harmonic			-30	dBm
	3rd Harmonic			-30	dBm
Receiver					
IF Frequency	50K Mode		100		KHz
	100K Mode		200		
	150K Mode		300		
	250K Mode		500		
IF Filter Bandwidth	50K Mode (10 ppm Xtal needed)		50		KHz
	100K Mode		100		
	150K Mode		150		
	250K Mode		250		
315MHz RX Sensitivity [3] @BER=0.1% high gain mode	50kbps (Fdev = 18.75KHz)		-111		dBm
	100kbps (Fdev = 37.5KHz)		-108		
	150kbps (Fdev = 56.25KHz)		-107		
	250kbps (Fdev = 93.75KHz),16MHz Xtal		-104		
480MHz RX Sensitivity [3] @BER=0.1% high gain mode	10kbps (FSK) (IFBW = 50KHz, Fdev = 25KHz)		-115		dBm
	10kbps (GFSK) (IFBW = 50KHz, Fdev = 25KHz)		-114		
433MHz RX Sensitivity [3] @BER=0.1% high gain mode	2kbps (IFBW = 50KHz, Fdev = 8KHz)		-117		dBm
	2kbps (IFBW = 100KHz, Fdev = 8KHz)		- 114		dBm
	10kbps (IFBW = 50KHz, Fdev = 18.75KHz)		-114		dBm
	10kbps (IFBW = 100KHz, Fdev = 37.5KHz)		-112		dBm
	50kbps (Fdev = 18.75KHz)		-110		dBm
	100kbps (Fdev = 37.5KHz)		-107		
	150kbps (Fdev = 56.25KHz)		-106		
	250kbps (Fdev = 93.75KHz) ,16MHz Xtal		-103		
868MHz RX Sensitivity [3] @BER=0.1% high gain mode	2kbps (IFBW = 50KHz, Fdev = 8KHz)		-114		dBm
	2kbps (IFBW = 100KHz, Fdev = 8KHz)		-109		dBm
	10kbps (IFBW = 50KHz, Fdev = 18.75KHz)		-110		dBm
	10kbps (IFBW = 100KHz, Fdev = 37.5KHz)		-111		dBm

	50kbps (Fdev = 18.75KHz)		-106		dBm
	100kbps (Fdev = 37.5KHz)		-103		
	150kbps (Fdev = 56.25KHz)		-102		
	250kbps (Fdev = 93.75KHz),16MHz Xtal		-100		
915MHz RX Sensitivity [3] @BER=0.1% high gain mode	50kbps (Fdev = 18.75KHz)		-105		dBm
	100kbps (Fdev = 37.5KHz)		-101		
	150kbps (Fdev = 56.25KHz)		-100		
	250kbps (Fdev = 93.75KHz),16MHz Xtal		-97		
Image rejection			20		dB
Interference (868.3MHz, 100Kbps)	Co-channel		-14		dB
	ACR1 (C/I_{ch1})		21		dB
	ACR2 (C/I_{ch2})		37		dB
	Offset ± 10MHz		50		dB
RX Spurious	25MHz ~ 1GHz			-57	dBm
	Above 1GHz			-47	dBm
RSSI Range	AGC on	-110		-30	dBm
Max Operation Input Power	@ RF input (BER = 0.1%)			10	dBm
RX Settling Time	PLL to RX		30		us
	Standby to RX		250		us
Regulator					
Regulator settling time	Pin 19 connected to 1nF		450		µs
Band-gap reference voltage			1.2		V
Regulator output voltage		1.8	**1.8**	2.1	V
Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Note 1: When digital I/O pins are configured as input, those pins shall NOT be floating but pull either high or low (SCS shall be pulled high only); otherwise, leakage current will be induced.

Note 2: Xtal settling time is depend on Xtal package type, Xtal ESR and Xtal Cm.

Note 3: Max Data rate= 50kbps @50K Mode, Max Data rate= 150kbps @150K Mode.

9. Control Register

A7108 chip contains 28 x 16-bit control registers, and can read or write data via 3-wire or 4-wire SPI interface（SCS, SCK, SDIO, GIOx）. All control registers are listed below.

9.1 Control Register Table

Add/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h Systemclock	W	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
	R	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
01h PLL I	W	RXCC	RXCP1	RXCP0	MDIV	RRC3	RRC2	RRC1	RRC0	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
02h PLL II	W	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
03h PLL III	W	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
	R	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
04h PLL IV	W	ROSCS	RSIS	CKX2	MD1	PDL2	PDL1	PDL0	MD0	VCS1	VCS0	CPS	CPC1	CPC0	SDPW	NSDO	EDI
05h Crystal	W	PGAS3	PGAS2	PGAS1	PGAS0	--	CRCINV	RTOE	RTCI	RTC1	RTC0	RTCE	XCC	XCP1	XCP0	CGS	XS
06h PA0(TX I)	W	--	LODV1	LODV0	TME	GS	FDP2	FDP1	FDP0	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
06h PA1(WORI)	W	WOR_AC5	WOR_AC4	WOR_AC3	WOR_AC2	WOR_AC1	WOR_AC0	WOR_SL9	WOR_SL8	WOR_SL7	WOR_SL6	WOR_SL5	WOR_SL4	WOR_SL3	WOR_SL2	WOR_SL1	WOR_SL0
	R	--	--	--	--	--	--	--	--	VBD	RCO6	RCO5	RCO4	RCO3	RCO2	RCO1	RCO0
06h PA2(WOR2)	W	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0	HWCKS	WN3	WN2	WN1	WN0	CALWR	RCOSE	TSEL	TWSOE	RCOT1	RCOT0
	R	--	--	--	--	--	--	--	--	--	--	CALWR	--	--	--	--	--
06h PA3(RFI)	W	QCLIM	RF23D1	RF23D0	PRRC1	PRRC0	PRIC1	PRIC0	RMP1	RMP0	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
	R	RHM7	RHM6	RHM5	RHM4	RHM3	RHM2	RHM1	RHM0	RLM7	RLM6	RLM5	RLM4	RLM3	RLM2	RLM1	RLM0
06h PA4(PM)	W	CST	POWRS	CELS	STS	LVR	RGS	RGC1	RGC0	SPSS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BDS
06h PA5(RTH)	W	IRTH7	IRTH6	IRTH5	IRTH4	IRTH3	IRTH2	IRTH1	IRTH0	IRTL7	IRTL6	IRTL5	IRTL4	IRTL3	IRTL2	IRTL1	IRTL0
06h PA6(AGC)	W	--	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0	HDM	AGCE	MXD	EXRSI	LGM1	LGM0	MGM1	MGM0
	R	--	--	--	--	--	--	--	--	--	--	--	--	LGC1	LGC0	MGC1	MGC0
06h PA7(AGC2)	W	--	--	--	--	--	--	--	--	--	--	--	--	TXIB1	TXIB0	RSA1	RSA0
06h PA8(GPIO)	W	WRCKS	MCNT1	MCNT0	DDPC	GIO2S3	GIO2S2	GIO2S1	GIO2S0	G2I	G2OE	GIO1S3	GIO1S2	GIO1S1	GIO1S0	G1I	G1OE
06h PA9(CKO)	W	INTXC	XCL4	XCL3	XCL2	XCL1	XCL0	WSEL2	WSEL1	WSEL0	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCT
06h PA10(VCB)	W	--	--	--	--	--	--	--	--	--	--	--	VCOC3	VCOC2	VCOC1	VCOC0	MVCS
	R	--	--	--	--	--	--	--	--	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
06h PA11(CHG1)	W	--	--	--	--	FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
	R	--	--	--	--	FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
06h PA12(CHG2)	W	--	--	--	--	FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
	R	--	--	--	--	FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
07h TX II	W	MCNTR	DPR2	DPR1	DPR0	BT1	BT0	TDL1	TDL0	TXDI	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
	R	ID15	ID14	ID13	ID12	ID11	ID10	ID09	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
08h RX I	W	ETH2	DMT	MPL1	MPL0	SLF2	SLF1	SLF0	ETH1	ETH0	DMOS	DMG1	DMG0	IFBW1	IFBW0	ULS	HGM
09h RX II	W	RXDI	PMD1	PMD0	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0	DCL2	DCL1	DCL0	DCM1	DCM0
	R	--	--	--	--	--	--	--	ADCO8	ADCO7	ADCO6	ADCO5	ADCO4	ADCO3	ADCO2	ADCO1	ADCO0
0Ah ADC	W	ARSSI	RADC	AVSEL1	AVSEL0	MVSEL1	MVSEL0	XADS	CDM	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	PWR	XEM	PLLEM	TRSM	TREM	--			ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
0Bh FIFO	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
0Ch Code	W	ERSSM	IDL1	WS6	WS5	WS4	WS3	WS2	WS1	WS0	MCS	WHTS	FECS	CRCS	IDL0	PML1	PML0
0Dh Pin control	W	RFT2	RFT1	RFT0	PRS	SCMDS	PCS1	PCS0	IRQI	IRQ1	IRQ0	IRQE	CKOI	CKO1	CKO0	CKOE	SCKI
0Eh Calibration	W	MSCRC	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MFBS	MFB3	MFB2	MFB1	MFB0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0
0Fh	W	DFCD	VBS	SWT	RSSC	VCC	--	WORE	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM

Modecontrol	R	--	--	--	RSSC	VCC	FECF	CRCF	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM

Legend: -- = unimplemented

9.2 Control Register Description

9.2.1 System clock (Address: 00h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h System clock	W	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
	R	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
Reset		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

SDR[6:0]: Data Rate Divider.

If DMOS (08h) = 0, $Data\,rate = \frac{1}{128} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$ (recommended).

If DMOS (08h) = 1, $Data\,rate = \frac{1}{64} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$

GRS: Reference Clock Selection for the internal PLL CLK Generator.
[0]: PLL CLK Gen. = F_{CGRF} x 48, where F_{CGRF} is from below GRC divider
[1]: PLL CLK Gen. = F_{CGRF} x 32

GRC[4:0]: Generation Reference Clock Divider.
GRC [4:0] is the clock divider to generate a PFD clock for the internal CLK Generator.

$$f_{CGRF} = \frac{f_{xtal}}{GRC[4:0]+1}$$

CSC[2:0]: System Clock Divider setting.
CSC is the clock divider of F_{MSCK} to generate the wanted data clock and IF calibration clock where F_{MSCK} is either from Xtal itself (CGS = 0) or from the internal CLK Generator (CGS = 1).

$$f_{CSCK} = \frac{f_{MSCK}}{CSC[2:0]+1}$$

F_{CSCK} shall be set appropriately, otherwise, IF Filter calibration will be failure.

Please refer to chapter 12 for details.

9.2.2 PLL I (Address: 01h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h PLL I	W	RXCC	RXCP1	RXCP0	MDIV	RRC3	RRC2	RRC1	RRC0	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
Reset		0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0

RXCC: Reserved for internal usage. Shall be [0].

RXCP[1:0]: Reserved for internal usage. Shall be [00].

MDIV: RF Divider Range setting.
[0]: Range of IP[7:0] is 32~67.
[1]: Range of IP[7:0] is 68 ~ 255.

RRC[3:0]: RF PLL Reference Counter.
RRC [3:0] is the clock divider to generate a PFD clock for RF_PLL to lock the wanted LO frequency.

$$f_{PFD} = \frac{f_{xtal}}{RRC[3:0]+1}$$, please refer to Chapter 13 for details.

IP[7:0]: LO frequency Integer Part setting.
Pease refer to Chapter 13 for detail.

9.2.3 PLL II (Address: 02h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h PLL II	W	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FP[15:0]: LO Frequency Fractional Part setting.

$$f_{RF} = \frac{1}{n} f_{PFD} \cdot (IP[7:0] + \frac{FP[15:0]}{2^{16}})$$ (unit: Hz)

where f_{RF} is the wanted RF frequency and ***n*** is the VCO divider.

where $f_{PFD} = f_{Xtal} \div (RRC[3:0]+1)$, is the comparison frequency of RF_PLL.

Where n = 2 by setting MD = [01] for 868M / 915MHz band
Where n = 4 by setting MD = [10] for 433M / 510MHz band
Where n = 6 by setting MD = [11] for 315MHz band

Note1: MD[1:0] is located at address 04h [Bit12, Bit8].

Note2: please refer to Chapter 13 for details.

9.2.4 PLL III (Address: 03h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h PLL III	W	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
	R	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AFC: Auto Frequency Compensation selection. Recommend AFC = [1].
[0]: manual
[1]: auto

MC[14:0]: PLL Fractional Part Compensation value.
[Write]：Manual setting to LO fractional part compensation value when AFC = [0].
[Read]：Frequency offset value when AFC = [1].

9.2.5 PLL IV (Address: 04h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h PLL IV	W	ROSCS	RSIS	CKX2	MD1	PDL2	PDL1	PDL0	MD0	VCS1	VCS0	CPS	CPC1	CPC0	SDPW	NSDO	EDI
Reset		0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	0

ROSCS: RC Oscillator for WOR (Wake-On-RX) function.
[0]: single mode
[1]: differential mode

RSIS: Reserved. RSIS shall be [0].

CKX2: Reserved. CKX2 shall be [0].

MD[1:0]: RF Band select, [Bit12, Bit8].
[00]: RF in 868MHz and 915MHz Band.
[01]: RF in 868MHz and 915MHz Band.
[10]: RF in 433MHz / 510MHz Band.
[11]: RF in 315MHz Band.

Note: MD[1:0] is used for the wanted RF formula (02h) and the wanted Fdev (06h, page0).

PDL[2:0]: PLL Settling Delay Time setting.

PDL [2:0]	PLL Delay Timer	Note
000	20 us	
001	40 us	
010	60 us	
011	80 us	Recommend
100	100 us	
101	120 us	
110	140 us	
111	160 us	

VCS[1:0]: VCO Current setting. Recommend VCS = [01].

CPS: Charge Pump tri-state setting. Recommend CPS = [1].
[0]: Tri-state.**[1]:** Normal operation.

CPC[1:0]: Charge Pump Current setting. Recommend CPC = [01].
[00]: 0.5mA. **[01]:** 1mA. **[10]:** 1.5mA. **[11]:** 2mA.

SDPW: Pulse Width of sigma-delta modulator. SDPW shall be [1].

NSDO: Mash sigma delta order setting. Recommend NSDO = [0].
[0]: order 2. **[1]:** order 3.

EDI: Dither Noise setting. Recommend EDI = [0].
[0]: Disable. **[1]:** Enable.

9.2.6 Crystal (Address: 05h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h Crystal	W	PGAS3	PGAS2	PGAS1	PGAS0	CRCDNP	CRCINV	RTOE	RTCI	RTC1	RTC0	RTCE	XCC	XCP1	XCP0	CGS	XS
Reset		0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

PGAS[3:0]: Page selector for the 06h register.

CRCDNP: CRC Mode. Shall be [0]
[0]: CRC-CCITT ($X^{16}+X^{12}+X^{5}+1$). **[1]:** Reserved.

CRCINV: CRC Inverted Select.
[0]: disable. **[1]:** enable

RTOE: Reserved. Shall be set to [0].

RTCI: Reserved. Shall be set to [0].

RTC[1:0]: Reserved. Shall be set to [00].

RTCE: Reserved. Shall be set to [0].

XCC: Crystal Current setting. Recommend XCC = [0].
[0]: Low current. **[1]:** High current.

XCP[1:0]: Crystal Regulating Couple setting. Recommend XCP = [00].

CGS: Clock Generation Selection.
[0]: disable, main clk, F_{MSCK}, is from Xtal itself.
[1]: enable, main clk, F_{MSCK}, is from the internal CLK Generator. Please refer to chapter 12 for details.

XS: Crystal Oscillator Selection. Recommend XS = [1].
[0]: disable, use external clock source from XI pin.
[1]: enable, use Xtal from XI and XO pin.

9.2.7 TX I (Address: 06h) Page 0

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h TX I	W		LODV1	LODV0	TME	GS	FDP2	FDP1	FDP0	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset			0	0	1	0	1	0	1	0	1	0	0	0	0	0	0

LODV [1:0]: Reserved. Shall be [01].

TME: TX Modulation Enable.
[0]: Disable (Test Mode to check single tone).
[1]: Enable (Normal Operation).

TME shall be set no matter in FIFO mode or Direct mode,
Then, the TX modulator will be active automatically after PDL and TDL delay timer.

GS: Gaussian Filter Selection.
[0]: Disable. **[1]:** Enable.

FDP[2:0]: Frequency Deviation Exponential Coefficient setting.

FD[7:0]: TX Frequency Deviation setting.

For both Gaussian filter is enabled (GS =1) or disabled（GS = 0）：

$$f_{dev} = \frac{1}{n} \cdot f_{PFD} \cdot FD[7:0] \cdot \frac{2^{FDP[2:0]}}{2^{19}} \quad \text{(unit: Hz)}$$

where $f_{PFD} = f_{Xtal} \div (RRC[3:0]+1)$, is the comparison frequency of RF_PLL.

Where n = 2 by setting MD = [01] for 868M / 915MHz band
Where n = 4 by setting MD = [10] for 433M / 510MHz band
Where n = 6 by setting MD = [11] for 315MHz band

Note1: MD[1:0] is located at address 04h [Bit12, Bit8].

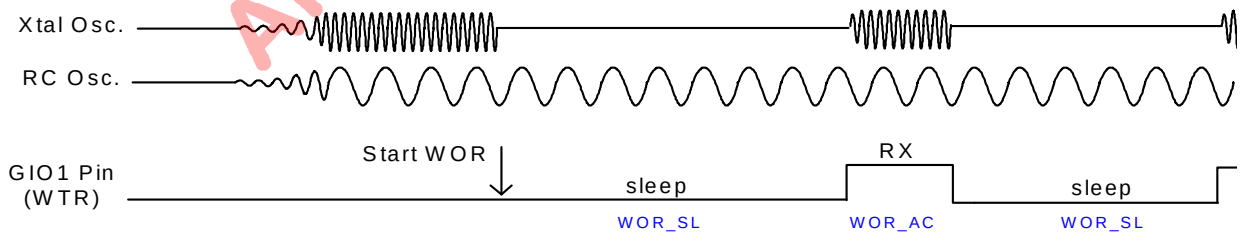
Note2: please refer to Chapter 13 for details.

9.2.7.1 WOR I (Address: 06h) Page 1

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8
06h WOR I	W	WOR_AC5	WOR_AC4	WOR_AC3	WOR_AC2	WOR_AC1	WOR_AC0	WOR_SL9	WOR_SL8
	R								
Reset		0	0	0	0	0	0	0	0
Address/Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
06h WOR I	W	WOR_SL7	WOR_SL6	WOR_SL5	WOR_SL4	WOR_SL3	WOR_SL2	WOR_SL1	WOR_SL0
	R	VBD	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
Reset		0	0	0	0	0	0	0	0

WOR_AC [5:0]: 6-bits WOR Active Period.
WOR Active Period = (WOR_AC[5:0]+1) x (1/4092), (244us ~ 15.6ms).

WOR_SL [9:0]: 10-bits WOR Sleep Period.
WOR Sleep Period = (WOR_SL[9:0]+1) x (1/4092), (7.8ms ~ 7.99s).



VBD: Battery Detection flag (Read Only).
[0]: Battery Low.
[1]: Battery High.

RCOC[6:0]: RC Oscillator Calibration value (Read Only).

9.2.7.2 WOR II (Address: 06h) Page 2

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

06h WOR II	W	RSSC _D1	RSSC _D0	RS _DLY2	RS _DLY1	RS _DLY0	HWCKS	WN3	WN2	WN1	WN0	CALWR	RCOSE	TSEL	TWSOE	RCOT1	RCOT0
												CALWR					
Reset		0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0

RSSC_D [1:0]: RSSI calibration Delay setting. Recommend RSSC_D = [00].
[00]: 10us. **[01]:** 20us. **[10]:** 30us. **[11]:** 40us.

RS_DLY [2:0]: RSSI Measurement Delay while in RX mode. Recommend RS_DLY = [000].
[000]: 10us. **[001]:** 20us. **[010]:** 30us. **[011]:** 40us. **[100]:** 50us. **[101]:** 60us. **[110]:** 70us. **[111]:** 80us.

HWCKS: WOR Clock Select. Recommend HWCKS = [0].
[0]: 4.096KHz **[1]:** 2.048KHz.

WN[3:0]: The number of RX wake up times.
Wake up times = (WN[3:0] + 1).

CALWR: WOR Calibration Flag.
[0]: pass. **[1]:** fail.

RCOSC_E: RC Oscillator for WOR.
[0]: Disable. **[1]:** Enable.

TSEL: TWOR Timer select.
[0]: Use WOR_AC [5:0]. (where WOR_AC is located in 06h, page 1)
[1]: Use WOR_SL [9:0]. (where WOR_SL is located in 06h, page 1)

TWSOE: Wake up MCU Mode select.
[0]: WOR mode. Wake up MCU when receiving ID code word.
[1]: TWOR mode. Wake up MCU by TWOR timer.

RCOT [1:0]: RC Oscillator current setting. Recommend RCOT = [00].

9.2.7.3 RF Current (Address: 06h) Page 3

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h RF Current	W	QCLIM	RF23D1	RF23D0	PRRC1	PRRC0	PRIC1	PRIC0	RMP1	RMP0	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
	R	RHM7	RHM6	RHM5	RHM4	RHM3	RHM2	RHM1	RHM0	RLM7	RLM6	RLM5	RLM4	RLM3	RLM2	RLM1	RLM0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

QCLIM: Reserved. Shall be [0].

RF23D [1:0]: Reserved. Shall be [00].

PRRC [1:0]: Reserved.RF divider by 2/3 current setting. Recommend PRRC = [00].

PRIC [1:0]: Reserved. Shall be [00].

RMP [1:0]: PA Ramp up/down Timing Scale setting. Recommend RMP = [00].
[00]: 1. **[01]:** 2. **[10]:** 4. **[11]:** 8.

TRT [2:0]: TX Ramp down discharge current select. Recommend TRT =[000].

ASMV [2:0]: TX Ramp up Timing Select. Recommend ASMV =[111].
[000]: 2us, **[001]:** 4us. **[010]:** 6us. **[011]:** 8us. **[100]:** 10us, **[101]:** 12us. **[110]:** 14us. **[111]:** 16us.

Actual TX ramp up time = ASMV [2:0] x RMP[1:0]

AMVS : PA Ramp Up Enable. Recommend AMVS = [1].
[0]: Disable. **[1]:** Enable.

RHM [7:0]: RSSI calibration high threshold level (Read Only).

RLM [7:0]: RSSI calibration low threshold (Read Only).

9.2.7.4 Power Manage (Address: 06h) Page 4

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h PM	W	CST	POWRS	CELS	STS	LVR	RGS	RGC1	RGC0	SPSS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BDS
Reset		-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CST: DC average length selection. Shall be [0].

[0]: DC average length unchanged. **[1]:** DC average length halves.

POWRS: Reserved. Shall be [0].

CELS: Reserved. Shall be [0].

STS: Reserved. Shall be [0].

LVR: Reserved. Shall be [1].

RGS: Low power Regulator Voltage select. Recommend RGS = [0].
[0]: 1.8V **[1]:** 1.6V

RGC[1:0]: Regulator Select. Shall be [01].
[00]: 0. **[01]:** 1. **[10]:** 2. **[11]:** 3.

SPSS: Mode Back select if WOR is enabled. Recommend SPSS = [0].
[0]: Standby mode. **[1]:** PLL mode.

RGV [1:0]: Regulator Voltage select. Recommend RGV = [11].
[00]: 2.1V. **[01]:** 2.0V. **[10]:** 1.9V. **[11]:** 1.8V.

QDS: VDD_A Quick Discharge select. Recommend QDS = [1].
[0]: Normal. **[1]:** Quick discharge.

BVT [2:0]: Battery Voltage Threshold select.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V. **[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

BDS: Battery Detection selection.
[0]: Disable. **[1]:** Enable.

9.2.7.5 AGC RSSI Threshold (Address: 06h) Page 5

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h RTH	W	IRTH7	IRTH6	IRTH5	IRTH4	IRTH3	IRTH2	IRTH1	IRTH0	IRTL7	IRTL6	IRTL5	IRTL4	IRTL3	IRTL2	IRTL1	IRTL0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IRTH[7:0]: AGC high Threshold. Recommend IRTH = [0x07].

IRTL[7:0]: AGC low Threshold. Recommend IRTL = [0x04].

If ADC ≤ IRTL. DVT[1:0] (0Eh) = 11.
If ADC ≥ IRTH. DVT[1:0] (0Eh) = 00.
If IRTL ≤ ADC ≤ IRTH. DVT[1:0] (0Eh) = 01.

9.2.7.6 AGC Control 1 (Address: 06h) Page 6

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h AGC	W	--	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0	HDM	AGCE	MXD	EXRSI	LGM1	LGM0	MGM1	MGM0
	R	--	--	--	--	--	--	--	--	--	--	--	--	LGC1	LGC0	MGC1	MGC0
Reset		--	--	0	0	0	0	0	0	0	0	0	0	1	1	1	1

VRSEL: AGC Function select. Recommend VRSEL = [0].
[0]: RSSI AGC. **[1]:** wideband AGC.

MS: AGC Manual Scale select. Recommend MS = [0].
[0]: Auto (RL−RH).
[1]: Manual (MSCL[4:0], 06h, page 6).

MSCL[4:0]: AGC Manual Scale setting. Reserved, shall set MSCL = [00000].

HDM: AGC HOLD select. Recommend HDM = [0].
[0]: No hold.
[1]: Hold Gain Switching when ID is sync.

AGCE: Auto Gain Control enable.
[0]: Disable. **[1]:** Enable.

MXD: Mixer Bias Select enable. Recommend MXD = [1].
[0]: Disable. **[1]:** Enable.

EXRSI: Reserved. Shall be [0].

LGM [1:0]: LNA Gain Attenuation select. Recommend LGM = [11].
[00]: 0dB. **[01]:** -6dB. **[10]:** -12dB. **[11]:** -18dB.

MGM [1:0]: Mixer Gain Attenuation select. Recommend MGM = [11].
[00]: 0dB. **[01]:** -6dB. **[10]:** -12dB. **[11]:** -18dB.

LGC[1:0]: LNA Gain Check (Read Only).

MGC[1:0]: Mixer Gain Check (Read Only).

9.2.7.7 AGC Control 2(Address: 06h) Page 7

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h AGC2	W	--	--	--	--	--	--	--	--	--	--	--	--	TXIB1	TXIB0	RSAGC1	RSAGC0
	R	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--
Reset		--	--	--	--	--	--	--	--	--	--	--	--	0	0	0	0

TXIB[1:0]: Reserved. Shall be [00].

RSAGC[1:0]: Reserved. Shall be [00].

9.2.7.8 GPIO (Address: 06h) Page 8

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h GPIO	W	WRCKS	MCNT1	MCNT0	DDPC	GIO2S3	GIO2S2	GIO2S1	GIO2S0	G2I	G2OE	GIO1S3	GIO1S2	GIO1S1	GIO1S0	G1I	G1OE
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WRCKS: WOR Reference clock select.
[0]: WOR Ref clock when PF8M is equal or close to 6.4MHz.
[1]: WOR Ref clock when PF8M is equal or close to 8MHz.

MCNT[1:0]: Main Clock Divider.

[00]: $f_{MCNT} = f_{MSCK}$

[01]: $f_{MCNT} = f_{MSCK} / 2$

[10]: $f_{MCNT} = f_{MSCK} / 3$

[11]: $f_{MCNT} = f_{MSCK} / 4$

Please refer to Chapter 12 for details.

DDPC (Direct mode data pin control): Direct mode modem data can be accessed via SDIO pin.
[0]: Disable. **[1]:** Enable.

GIO2S [3:0]: GIO2 pin function select.

GIO2S [3:0]	TX state	RX state
[0000]	WTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC(frame sync)
[0010]	TMEO(TX modulation enable)	CD(carrier detect)
[0011]	Preamble Detect Output (PMDO)	
[0100]	MCU wakeup signal (TWOR)	
[0101]	In phase demodulator input(DMII) or DVT[0](AGC)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	PDN_RX	
[1011]	External FSYNC input in RX direct mode *	
[1100]	In phase demodulator output (DMOI)	
[1101]	FPF	
[1110]	PDN_TX	
[1111]	FMTDO (FIFO mode TX Data Output testing)	

If GIO2S = [1011] and direct mode is selected, the internal frame sync function will be disabled. In such case, A7108 supports to accept an external frame sync signal from MCU to feed to GIO2 pin to determine the timing of fixing DC estimation voltage of demodulator.

G2I: GIO2 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

G2OE: GIO2 pin output enable.
[0]: High Z. **[1]:** Enable.

GIO1S [3:0]: GIO1 pin function select.

GIO1S [3:0]	TX state	RX state
[0000]	WTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC(frame sync)
[0010]	TMEO(TX modulation enable)	CD(carrier detect)
[0011]	External sync input(for direct mode)(only in SCT=0) Preamble Detect Output (PMDO)(only in SCT=1)	
[0100]	MCU wakeup signal (TWOR)	
[0101]	Quadrature phase demodulator input (DMIQ).or DVT[1](AGC)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	PDN_TX	
[1011]	External FSYNC input in RX direct mode *	
[1100]	Quadrature phase demodulator input (DMOQ).	
[1101]	FPF	
[1110]	Battery Detect flag.(BDF)	
[1111]	FMRDI. (FIFO mode RX input for internal test)	

If GIO1S = [1011] and direct mode is selected, the internal frame sync function will be disabled. In such case, A7108 supports to accept an external frame sync signal from MCU to feed to GIO1 pin to determine the timing of fixing DC estimation voltage of demodulator.

G1I: GIO1 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

G2OE: GIO1pin output enable.
[0]: High Z. **[1]:** Enable.

9.2.7.9 CKO (Address: 06h) Page 9

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h CKO	W	INTXC	XCL4	XCL3	XCL2	XCL1	XCL0	WSEL2	WSEL1	WSEL0	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCT
Reset		0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

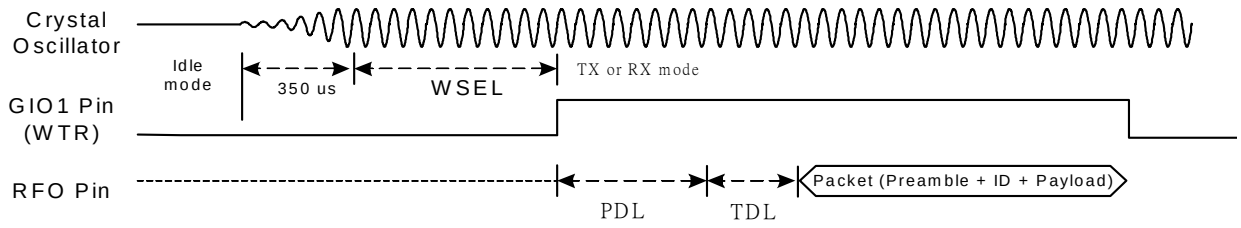
INTXC: Internal Crystal Load selection. Recommend INTXC = [1].
[0]: Use external capacitors. **[1]:** Use on-chip capacitors.

XCL[4:0]: On-chip Crystal Capacitor Load setting. Recommend XCL = [10000] if Xtal Cload = 20pF.
XCL is active when INTXC=1 and Each XCL step is 1.68 pF.
XCL is the on-chip capacitor for Xtal oscillator to fine tune offset frequency of the wanted RF carrier.
Please refer to chapter 11 or contact AMICCOM's FAE.

XCL[4:0]	Xtal C-load (pF)
00000	0
00001	1.68
00010	3.36
…	
11110	50.4
11111	52.08

WSEL[2:0]: Crystal Settling Delay setting (200us ~ 2.5ms). Recommend WSEL = [001].
[000]: 200us. **[001]:** 400us. **[010]:** 800us. **[011]:** 600us.

[100]: 1ms. **[101]:** 1.5ms. **[110]:** 2ms. **[111]:** 2.5ms.



CKOS [3:0]: CKO pin output select.
[0000]: DCK (TX data clock).
[0001]: RCK (RX recovery clock).
[0010]: FPF (FIFO pointer flag for FIFO extension).
[0011]: Logic OR gate by EOP, EOVBC, EOFBC, EOVCC, EOVDC and RSSC_OK. (Internal usage).
[0100]: BBCK. (Internal usage)
[0101]: BBCK. (Internal usage)
[0110]: BBCK. (Internal usage)
[0111]: RTCIN (RTC timer input).
[1000]: WCK. (Internal usage)
[1001]: PF8M. (Internal usage)
[1010]: ROSC.
[1011]: EOADC.
[1100]: OKADCN. (Internal usage)
[1101]: 0. (Internal usage)
[1110]: RTCO (RTC timer output).
[1111]: Reserved

CKOI: CKO pin Output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

CKOE: CKO pin Output Enable.
[0]: High Z. **[1]:** Enable.

SCT: Reserved. Shall be = [1].

9.2.7.10 VCO current (Address: 06h) Page 10

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h VCO Current	W	-	-	-	-	-	-	-	-	-	-	-	VCOC3	VCOC2	VCOC1	VCOC0	MVCS
	R												VCCF	VCB3	VCB2	VCB1	VCB0
Reset		-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0

VCOC [3:0]: VCO Current Bank Calibration result.
If SWT = [0]: VCOC= [1000].
If SWT = [1]: VCOC[3:0] = Manual setting. Recommend VCOC = [0000].
Note: SWT is located at 0Fh.

MVCS: VCO current calibration select. Recommend MVCS = [0].
[0]: Auto.
[1]: Manual.
VCO band calibration result can be read from VCB [2:0].

VCCF : VCO Current Auto Calibration Flag (Read Only).
[0]: Pass. **[1]:** Fail.

VCB [2:0]: VCO Current Bank Calibration Value (Read Only).
If MVCS= 0 (bit 0), VCB [2:0] is auto calibration value.
If MVCS= 1 (bit 0), VCB [2:0] is manual calibration value.

9.2.7.11 Channel Group (I) (Address: 06h) Page 11

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h CHG1	W					FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
	R					FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0

Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FPL [3:0]: VCO Calibration Fractional Part Setting for Low Boundary Channel Group.
Please refer to A7108's reference code for the wanted RF band.

IPL [7:0]: VCO Calibration Integer Part Setting for Low Boundary Channel Group.
Please refer to A7108's reference code for the wanted RF band.

9.2.7.12 Channel Group (II) (Address: 06h) Page 12

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h CHG2	W					FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
	R					FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FPH [3:0]: VCO Calibration Frational Part Setting for High Boundary Channel Group.
Please refer to A7108's reference code for the wanted RF band.

IPH [7:0]: VCO Calibration Integer Part Setting for High Boundary Channel Group.
Please refer to A7108's reference code for the wanted RF band.

9.2.8 TX II (Address: 07h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h TX II	W	MCNTR	DPR2	DPR1	DPR0	BT1	BT0	TDL1	TDL0	TXDI	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
	R	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset		0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

MCNTR: Divided by 2 select.
[0]: $PF8M = f_{\mathrm{MCNT}} \div 2$ where PF8M is one of baseband clock sources.
[1]: $PF8M = f_{\mathrm{MCNT}}$

where $f_{\mathrm{MCNT}} = f_{MSCK} \div (MCNT[1:0])$, located in 0x06 page 8.

Please refer to Chapter 12 for details.

DPR [2:0]: Scaling setting for PDL[2:0] and TDL[1:0]. Recommend DPR = [000].

BT [1:0]: Moving average for Gaussian filter select.
If GS = [0],Gaussian filter is disabled, **BT = [00]:** not average. **[01]:** 2 bit average. **[10]:** 4 bit average. **[11]:** 8 bit average
If GS = [1],Gaussian filter is enabled, **BT = [00]:** 2.0. **[01]:** 1.0. **[10]:** 0.5. **[11]:** 0.5

TDL[1:0]:TX Settling Delay select.

TDL [1:0]	TX Delay Timer	Note
00	20 us	Recommend
01	40 us	
10	60 us	
11	80 us	

TXDI: TX data inverted. Recommend TXDI = [0].
[0]: normal. **[1]:** invert

PAC[1:0]: PA current setting.

Please refer to Chapter 8 and A7108 App. Note for programmable TX output power.

TDC[1:0]: TX Driver current setting.

Please refer to Chapter 8 and A7108 App. Note for programmable TX output power.

TBG[2:0]: TX Buffer Gain setting.

Please refer to Chapter 8 and A7108 App. Note for programmable TX output power.

ID [15:0]: device ID data. Read the IC ID code in this register (Read Only).

9.2.9 RX I (Address: 08h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h RX I	W	ETH2	DMT	MPL1	MPL0	SLF2	SLF1	SLF0	ETH1	ETH0	DMOS	DMG1	DMG0	IFBW1	IFBW0	ULS	HGM
Reset		0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0

DMT: Demodulator test bit. DMT shall be [0].
[0]: Normal mode.
[1]: Test mode.

MPL [1:0]: Symbol recovery loop filter setting after ID SYNC. MPL shall be [01].

SLF [2:0]: Symbol recovery loop filter setting. SLF shall be [100].

ETH [2:0]: ID code error bit tolerance [Bit15, Bit8, Bit7]. Recommend ETH = [001].
[000]: 0 bit. **[001]:** 1bit. **[010]:** 2 bits. **[011]:** 3 bits. **[100]:** 4 bits. **[101]:** 5 bits. **[110]:** 6 bits. **[111]:** 7 bits.

ETH is used to set acceptable ID error bit during ID sync scheme.

DMOS: Demodulator over-sample select. Recommend DMOS = [0].
[0]: x64. **[1]:** x32.

DMG [1:0]: Demodulator Gain select. Recommend DMG = [01].
[00]: x1. **[01]:** x3. **[1x]:** x5.

IFBW [1:0]: IF Band Pass Filter select.
[00]: 50KHz. data rate ≦50Kbps. (Xtal shall be chosen ± 10 ppm stability in case of RX sensitivity degradation.)
[01]: 100KHz. 50K < data rate ≦100Kbps.
[10]: 150KHz. 100K < data rate ≦150Kbps.
[11]: 250KHz. 150K < data rate ≦250Kbps.

Since A7108 is a low-IF TRX, on-chip IFBW is implemented with 4 optional Filter Bandwidth.
The IF Filter shall be calibrated after power on reset. In performance point of view, the narrower IFBW results the better RX sensitivity. To make a successful IFBW calibration, an appreciated setting of calibration clock is necessary.
Please refer to Chapter 12 and A7108's reference code for details.

ULS: RX Up/Low side band select. Recommend ULS = [0].
[0]: Up side band, TX A-terminal frequency – IF = RX B-terminal frequency
[1]: Low side band, TX A-terminal frequency + IF = RX B-terminal frequency

HGM: LNA Gain mode select. Recommend HGM = [1].
[0]: Low. **[1]:** High.

9.2.10 RX II (Address: 09h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h RX II	W	RXDI	PMD1	PMD0	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0	DCL2	DCL1	DCL0	DCM1	DCM0
	R								ADCO 8	ADCO 7	ADCO 6	ADCO 5	ADCO 4	ADCO 3	ADCO 2	ADCO 1	ADCO 0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RXDI: RX Data Invert. Recommend RXDI = [0].
[0]: normal. **[1]:** inverted.

PMD[1:0]: Preamble pattern detection. Recommend PMD = [11].
[00]: 0 bit **[01]:** 4 bits **[10]:** 8 bits **[11]:** 16 bits
When DCM[1:0] = 01, 10, 11, PMD setting is active.

DCV[7:0]: Data DC average value setting. Recommend DCV = [0000-0000].
This setting is only active when DCM (09h) = [00] for internal usage.

DCL[2:0]: Data Length of Peak Detect average setting. Recommend DCL = [010].
DCL[2:0] is used to let A7108 detects n times "0" or n times "1" to result DC estimation voltage of demodulator.

DCL[2:0]	DC average		Note
	Before ID Sync (preamble detect)	After ID Sync	
000	4	32	

001	8	32	
010	16	32	Recommend
011	32	32	
100	4	64	
101	8	64	
110	16	64	
111	32	64	

For example,
If DCL[2:0] = 010,
Before ID sync, by peak detect method to update a new DC value for every 16 times 1" and 4 times "0" .
After ID sync, by peak detect method, to update a new DC value for every 32 times "1" and 32 times "0" .

DCM [1:0]: Demodulator DC estimation mode. Recommend DCM = [01].
[00]: DC average set by DCV[7:0],(09h).
[01]: DC holds after preamble detected.
[10]: DC holds after ID detected.
[11]: DC value when chip receive specific data length (set by DCL[:2:0])..

ADCO[8:0]: Digital RSSI, 9-bits, output when AGC is enabled. (Read Only).

9.2.11 ADC (Address: 0Ah)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah ADC	W	ARSSI	RADC	AVSEL1	AVSEL0	MVSEL1	MVSEL0	XADS	CDM	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	PWR	XEM	PLLEM	TRSM	TREM		VBD1	VBD0	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Reset		0	0	0	0	0	0	0	0	0	0	01	0	0	0	0	0

ARSSI: Auto RSSI measurement enable.
[0]: Disable. **[1]:** Enable.
ARSSI shall be set [1] for auto RSSI measurement before MCU issues RX strobe command.

RADC: ADC Read Out Average Mode.
[0]: 1, 2, 4, 8 average mode. If RADC = 0, ADC average is set by AVSEL[1:0] (0Ah).
[1]: 8, 16, 32, 64 average mode. If RADC = 1, ADC average is set by MVSEL[1:0] (0Ah).

AVSEL [1:0]: ADC average mode. Recommend AVSEL = [00].
[00]: No average. **[01]:** 2. **[10]:** 4. **[11]:** 8.

MVSEL [1:0]: ADC average mode for VCO calibration and RSSI. Recommend MVSEL = [11].
[00]: 8. **[01]:** 16. **[10]:** 32. **[11]:** 64.

XADS: ADC input signal source select.
[0]: internal temperature sensor or RSSI signal.
[1]: external signal source.

CDM: Carrier Detect enable
[0]: RSSI/Temperature measurement.
[1]: Carrier detect

RTH[7:0]: Threshold value of Carrier Detect (Active in RX mode only).
CD (Carrier Detect) =1 when RSSI ≧ RTH.
CD (Carrier Detect) =0 when RSSI < RTH.

PWR: Power Status (Read Only).
[0]: Power off. **[1]:** Power on.

XEM: Crystal Oscillator Status (Read Only).
[0]: Disable. **[1]:** Enable.

PLLEM: PLL Mode Status (Read Only).
[0]: Disable. **[1]:** Enable.

TRSM: TRX Mode Status (Read Only).
[0]: RX mode. **[1]:** TX mode.

TREM: TRX Operation Status (Read Only).
[0]: Disable. **[1]:** Enable.

VBD[1:0]: VCO bias detect (Read Only).

ADC[7:0]: ADC value (Read Only).

9.2.12 FIFO (Address: 0Bh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh FIFO	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1

FPM [1:0]: FIFO Pointer Margin.

Used in FIFO extension mode.

FPM[1:0]	Bytes in TX FIFO	Bytes in RX FIFO
[00]	4	60
[01]	8	56
[10]	12	52
[11]	16	48

PSA [5:0]: Used for Segment FIFO.
Used in FIFO segment mode.

FEP [7:0]: FIFO End Pointer for TX FIFO and Rx FIFO.
FIFO Length Setting = FEP [7:0] +1.
For example if FEP = 0x3F, it means FIFO length is 64 bytes.

9.2.13 Code (Address: 0Ch)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch Code	W	ERSSM	IDL1	WS6	WS5	WS4	WS3	WS2	WS1	WS0	MCS	WHTS	FECS	CRCS	IDL0	PML1	PML0
Reset		0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1

ERSSM : Ending for RSSI measurement. Recommend ERSSM = [0].
[0]: RSSI value frozen before leaving RX.
[1]: RSSI value frozen when valid frame sync (ID and header check ok).

IDL[1:0]: ID code length in FIFO mode [Bit14, Bit2]. Recommend IDL=[01].
[00]: 2 bytes. **[01]:** 4 bytes. **[10]:** 6 bytes. **[11]:** 8 bytes.

WS [6:0]: Data Whitening Seed (data encryption key).

MCS: Manchester Code Enable.
[0]: Disable. **[1]:** Enable.

WHTS: Data Whitening (Data Encryption) Select.
[0]: Disable. **[1]:** Enable (The data is whitened by multiplying with PN7).

FECS: FEC Select.
[0]: Disable. **[1]:** Enable (The FEC is (7, 4) Hamming code).

CRCS: CRC Select.
[0]: Disable. **[1]:** Enable.

PML [1:0]: Preamble Length in FIFO mode. Recommend PML= [11].
[00]: 1 byte. **[01]:** 2 bytes. **[10]:** 3 bytes. **[11]:** 4 bytes.

9.2.14 Pin Control (Address: 0Dh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh Pin control	W	RFT2	RFT1	RFT0	PRS	SCMDS	PCS1	PCS	IRQI	IRQ1	IRQ0	IRQE	CKOI	CKO1	CKO0	CKOE	SCKI
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RFT [2:0]: RF Analog Pin Configuration. Recommend RFT= [000].

{XADS, RFT[2:0]}	BP_BG (Pin 19)	RSSI (Pin 1)
[0000]	Band-gap voltage	RSSI voltage

[0001]	Analog temperature voltage	RSSI voltage
[0010]	Band-gap voltage	No connection
[0011]	Analog temperature voltage	No connection
[0100]	BPF positive in phase output	BPF negative in phase output
[0101]	BPF positive quadrature phase output	BPF negative quadrature phase output
[0110]	RSSI voltage	No connection
[0111]	RSSI voltage	No connection
[1000]	Band-gap voltage	External ADC input source
[1001]	Analog temperature voltage	External ADC input source
[1010]	Band-gap voltage	External ADC input source
[1011]	Analog temperature voltage	External ADC input source
[1100]	No connection	External ADC input source
[1101]	No connection	External ADC input source
[1110]	No connection	External ADC input source
[1111]	No connection	External ADC input source

PRS: Read frequency mode when AFC=1. Recommend PRS= [0].
[0]: no frequency compensation.
[1]: frequency offset in AFC mode

SCMDS: Strobe Command select. Recommend SCMDS= [1].
[0]: register control. **[1]:** strobe control.

PCS1: PWR Setting. Shall be [1].
[0]: Reserved.
[1]: PWR is controlled by register or strobe command.

PCS: TRE and TRS pin control. Shall be [0].
[0]: TRE and TRS are controlled by register or strobe command.
[1]: Reserved.

IRQI: IRQ Pin Output invert. Shall be [0].

IRQ[1:0]: Reserved. Use GIOP instead. Shall be [00].

IRQE: Reserved. Use GIOP instead. Shall be [0].

CKOI: CKO pin output invert. Use 06h page 9 instead. Shall be [0].

CKO[1:0]: CKO Pin Output select. Use 06h page 9 CKOS instead. Shall be [00].

CKOE: CKO Pin Output enable. Use 06h page 9 instead. Shall be [0].

SCKI: 3-wire SPI - Clock Inverted. Recommend SCKI= [0].
[0]: Normal. **[1]:** Inverted.

9.2.15 Calibration (Address: 0Eh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh Calibration	W	MSCRC	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MIFS	MIF3	MIF2	MIF1	MIF0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0
Reset		0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

MSCRC: CRC Filtering Enable. Recommend MSCRC = [1].
[0]: Disable.
[1]: Enable.
For FIFO mode only, if MSCRC = 1, A7108 will ignore the coming packet once CRC error occurs. That means, this device will not exit RX mode but keep WTR signal high. Therefore, MCU will not be disturbed by this unsuccessful packet.

VTL[2:0]: VT low threshold setting for VCO calibration. Recommend VTL = [100].
[000]: VTL=0.1V. **[001]:** VTL=0.2V. **[010]:** VTL=0.3V. **[011]:** VTL=0.4V. **[100]:** VTL=0.5V. **[101]:** VTL=0.6V.
[110]: VTL=0.7V. **[111]:** VTL=0.8V.

VTH[2:0]: VT high threshold setting for VCO calibration. Recommend VTH = [100].
[000]: VTH=Vdd-0.1V. **[001]:** VTH=Vdd-0.2V. **[010]:** VTH=Vdd-0.3V. **[011]:** VTH=Vdd-0.4V. **[100]:** VTH=Vdd-0.5V.
[101]: VTH=Vdd-0.6V. **[110]:** VTH=Vdd-0.7V. **[111]:** VTH=Vdd-0.8V.

MVBS: VCO band calibration select. Recommend MVBS = [0].
[0]: Auto. **[1]:** Manual.

MVB[2:0]: VCO bank manual setting. VCO frequency increases when MVB decreases. Recommend MVB = [000].

MIFS: IF Filter Calibration Select. Recommend MIFS = [0].
[0]: Auto. **[1]:** Manual.

MIF[3:0]: IF filter Manual Setting. Recommend MIF = [0000].

FCD [4:0]: IF Filter Auto Calibration Deviation from Goal (read only).

DVT[1:0]: VT output (Read Only).
[00]: VT< VTL< VTH.
[01]: VTL< VT< VTH.
[10]: No used.
[11]: VTL< VTH< VT.

VBCF: VCO Band Auto Calibration Flag (Read Only).
[0]: Pass. **[1]:** Fail.

VB[2:0]: VCO Bank Auto Calibration Result (Read Only).

FBCF: IF Filter Auto Calibration Flag (Read Only).
[0]: Pass. **[1]:** Fail.

FB[3:0]: IF Filter Auto Calibration Result (Read Only).

9.2.16 Mode control (Address: 0Fh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh Mode control	W	DFCD	VBS	SWT	RSSC	VCC	--	WORE	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
	R	--	--	--	RSSC	--	FECF	CRCF	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DFCD: Data Filter by CD. The received packet is filtered if the input power level is below RTH (0Ah).
[0]: Disable. **[1]:** Enable.

VBS: VCO Band adjustment for 433MHz and 868MHz.
[0]: For 315MHz / 470MHz / 915MHz band
[1]: For 433MHz / 868MHz band

SWT: Reserved. Recommend SWT = [0].

RSSC: RSSI Calibration.
[0]: Disable. **[1]:** Enable.

VCC: VCO Current Calibration.
[0]: Disable. **[1]:** Enable.

WORE: WOR or TWOR Enable.
[0]: Disable. **[1]:** Enable.

FMT: Reserved for internal usage only. Shall be set to [0].

FMS: Direct/FIFO mode select.
[0]: Direct mode. **[1]:** FIFO mode.

CER: Chip enable by register.
[0]: chip turn-off. **[1]:** chip turn-on.

PLLE: PLL enable by register.
[0]: PLL off. **[1]:** PLL on.

TRSR: TRX Mode select by register.
[0]: RX mode. **[1]:** TX mode.
When bit TRER=1, the chip will enter TX or RX mode by TRSR register.

TRER: TRX mode enable by register.
[0]: Reserved.
[1]: By register control (CER and TRSR). In FIFO mode, this bit will be cleared after end of packet encountered.

VBC: VCO Bank Calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

FBC: IF Filter Bank Calibration enable (Auto clear when done).

[0]: Disable . **[1]:** Enable.

ADCM: ADC measurement (Auto clear when done).
[0]: Disable. **[1]:** Enable.

	Non-Rx mode	RX mode
[0]	None	None
[1]	Temperature measurement	RSSI, carrier detect or external signal source conversion

FECF: FEC flag. (FECF is read clear.)
[0]: FEC pass. **[1]:** FEC error.

CRCF: CRC flag. (CRCF is read clear.)
[0]: CRC pass. **[1]:** CRC error.

10. SPI Format

The A7108 communicates with a host MCU via 3-wire SPI interface (SCS, SCK, SDIO) or 4-wire SPI (SDO from GIO1 or GIO2) with a max data rate 10Mbps. A SPI transition is a 24-bits sequence which consists of an 8-bits address and a 16-bits data word. The MCU should set SCS (SPI chip select) pin low in order to access A7108. Via the SPI interface, user can access the **control registers** and issue **Strobe commands**. The SPI data will be latched into the registers at the rising edge of SCK. When reading registers from the RF chip, after input the wanted register address, the bit data will be transferred from the falling edge of SCK.

10.1 SPI Format

Address Byte(8 bits)								Data words(16 bits)															
R/W	Command			Address				Data															
A7	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

SPI format

Address Byte (8 bits):

Bit A7: R/W bit
[0]: Write.
[1]: Read.

Bit A6~A4: Command
[00x]: read/write control register.
[01x]: read/write ID code.
[10x]: read/write FIFO register.
[110]: reset TX/RX FIFO pointer.
[111]: RF chip Reset (soft reset and all registers will be clean to initial value).

Bit A3~A0: Address of control register

Strobe Command table:

Address Byte (8 bits)								description
A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	A3	A2	A1	A0	Write control register
1	0	0	x	A3	A2	A1	A0	Read control register
0	0	1	x	x	X	x	x	Write ID code command
1	0	1	x	x	X	x	x	Read ID code command
0	1	0	x	x	X	x	x	TX FIFO write command
1	1	0	x	x	X	x	x	RX FIFO read command
X	1	1	1	x	X	x	x	Software Reset command
0	1	1	0	x	X	x	x	TX FIFO address pointer reset command
1	1	1	0	x	X	x	x	RX FIFO address pointer reset command
0	0	0	1	0	0	0	0	Sleep mode
0	0	0	1	0	0	1	0	Idle mode
0	0	0	1	0	1	0	0	Standby mode
0	0	0	1	0	1	1	0	PLL mode
0	0	0	1	1	0	0	0	RX mode
0	0	0	1	1	0	1	0	TX mode
0	0	0	1	1	1	0	0	Deep sleep mode (tri-state)
0	0	0	1	1	1	1	1	Deep sleep mode (pull-high)

Remark: X (Don't care).

Data Words (16-bits) : On-chip registers in sequence of D15~D0.

10.2 SPI Timing Chart

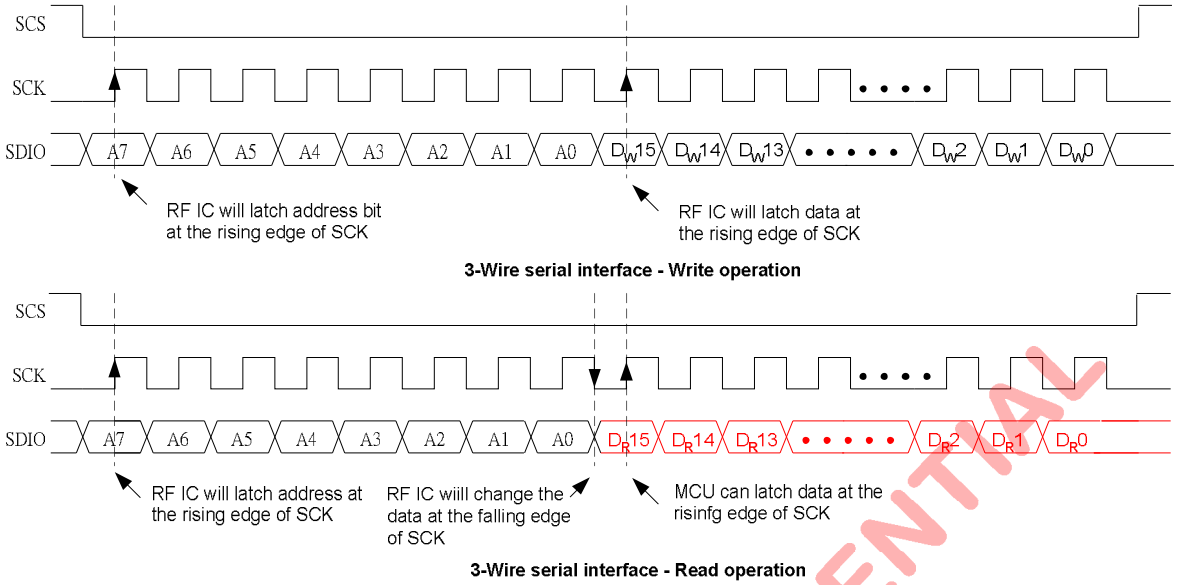


Figure 10.1. SPI read/write sequence

10.3 Control register access

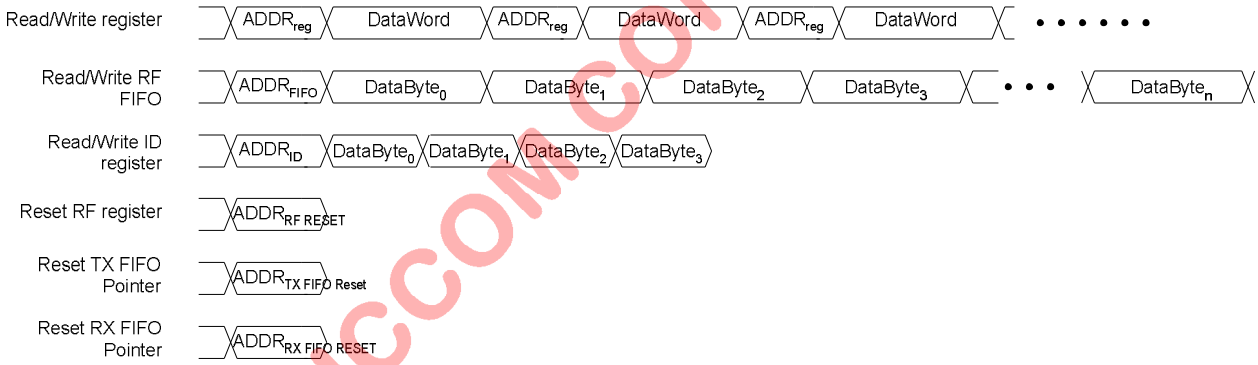


Figure 10.2. Access type of control register

10.4 SPI Timing Specification

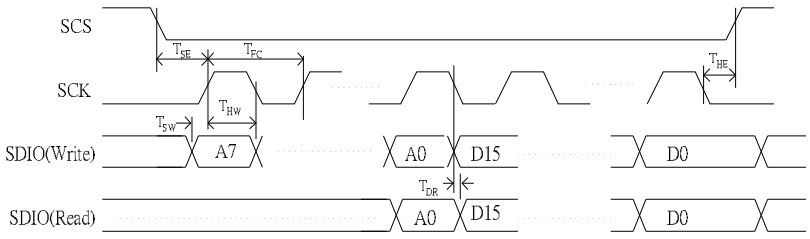


Figure 10.3 SPI timing sequence

Parameter	Description	Min.	Max.	Unit
T_{FC}	Clock frequency.		10	MHz
T_{SE}	SCS setup time.	50		ns

T_{HE}	SCS hold time.	50		ns
T_{SW}	SDIO setup time.	50		ns
T_{HW}	SDIO hold time.	50		ns
T_{DR}	SDIO delay time.	0	100	ns
T_{HR}	SDIO hold time.	0		ns

10.5 Reset Command

The MCU could issue a software reset command to A7108 by sending a Reset Command through the SPI interface as shown below. After a reset command, A7108 is in standby mode.

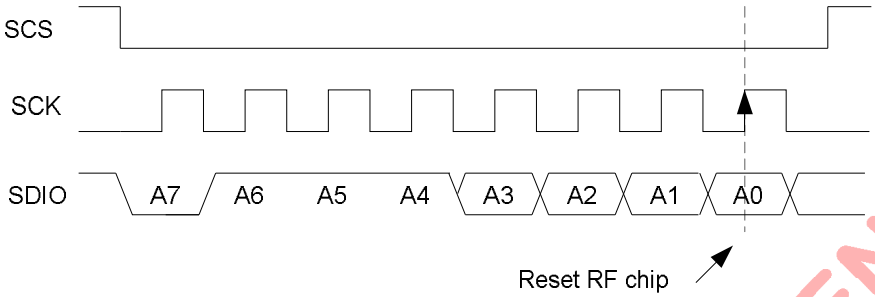


Figure 10.5 Reset Command

10.6 Reset TX FIFO Pointer

The SPI timing sequences for resetting TX FIFO Pointer is shown below. The address pointer of TX FIFO is reset to 0x00 at the rising edge of SCK at bit A0.

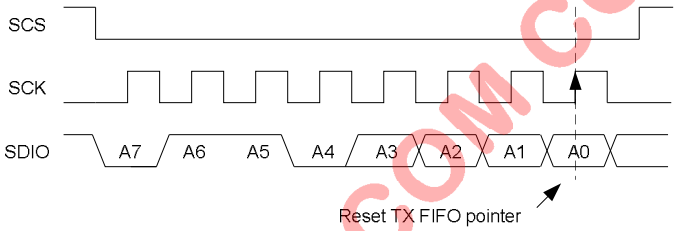


Figure 10.6 TX FIFO Pointer Reset

10.7 Reset Rx FIFO Pointer

The SPI timing sequences for resetting RX FIFO Pointer is shown below. The address pointer of RX FIFO is reset to 0x00 at the rising edge of SCK at bit A0.

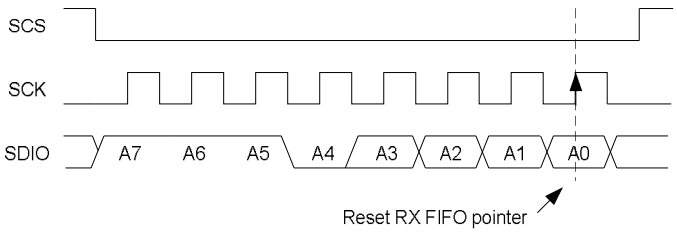


Figure 10.7 RX FIFO Pointer Reset

10.8 ID Read/Write Command

A7108 has built-in 32-bits ID Registers for customized identification code. It is accessed via SPI interface. ID length is recommended to be 32 bits by setting IDL. the timing sequences are shown below. First execute the ID Red/write command in address byte, and then write data bytes with length of the 4 bytes.

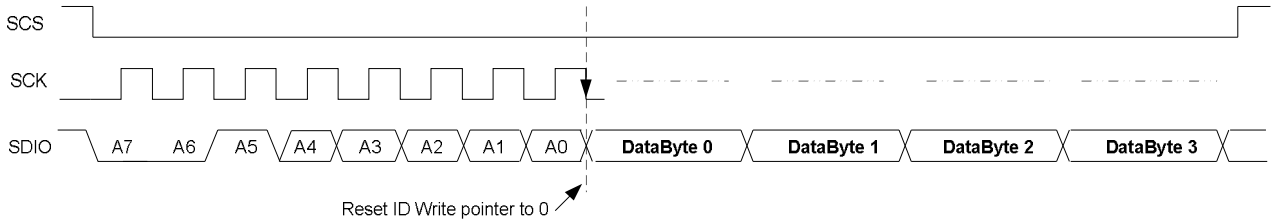


Figure 10.8 ID Write Command

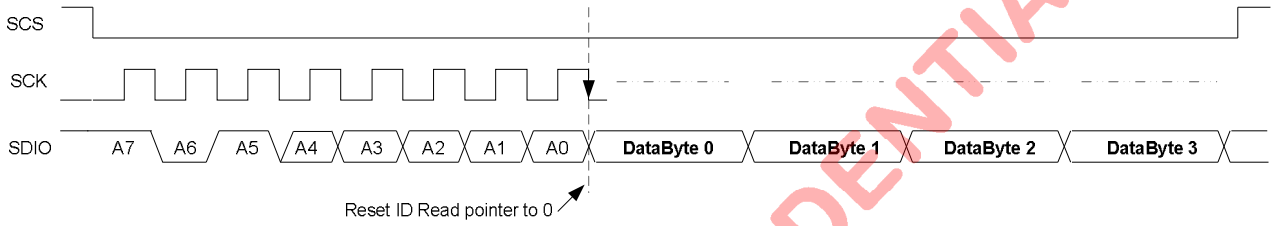


Figure 10.9 ID Read Command

10.9 FIFO R/W Command

TX FIFO Write Command

To execute the TX FIFO write procedure, according to the command table, user should write the corresponding command into Address Byte, and then write data into the Data Bytes. After completing the writing action, toggle SCS=1 to end the TX FIFO writing procedure.

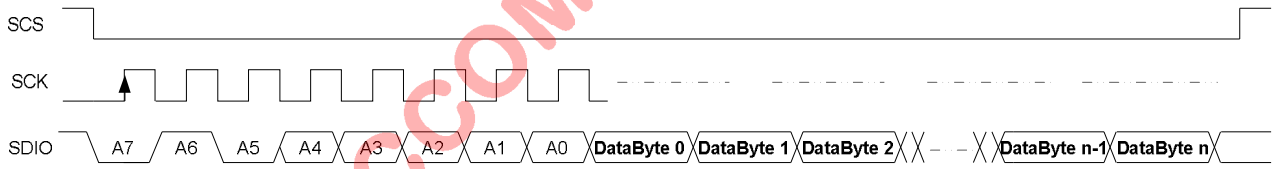


Figure 10.10 TX FIFO Write Command

RX FIFO Write Command

To execute the RX FIFO read procedure, according to the command table, user should write the corresponding command into Address Byte, and then read out RX FIFO. After completing the reading action, toggle SCS=1 to end the RX FIFO writing procedure.

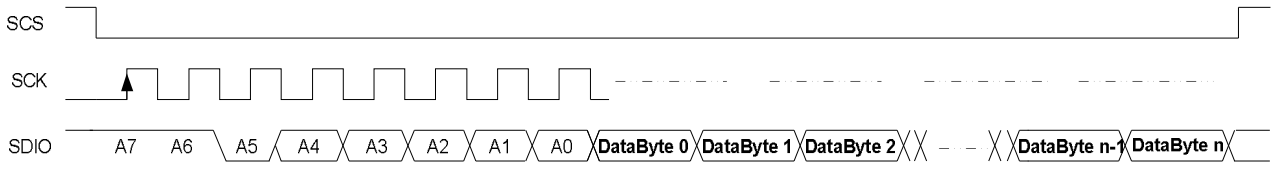


Figure 10.11 RX FIFO Read Command

11 Crystal Oscillator

A7108 needs external crystal or external clock to generate the internal wanted clock sources.

Relative Control Register

Crystal (Address: 05h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h Crystal	W	PGAS3	PGAS2	PGAS1	PGAS0	CRCE	CRCINV	RTOE	RTCI	RTC1	RTC0	RTCE	XCC	XCP1	XCP0	CGS	XS
Reset		0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

11.1 Use External Crystal

Figure 11.1 shows the connection of crystal network between XI and XO pins. C1 and C2 capacitance have been built inside A7108 are used to adjust different crystal loading. User can set INTXC [4:0] (06h, page 9) to meet crystal loading requirement. A7108 supports low cost crystal within ± 30 ppm accuracy. Be aware that crystal accuracy requirement includes initial tolerance, temperature drift, aging and crystal loading.

CKO (Address: 06h) Page 9

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h CKO	W	INTXC	XCL4	XCL3	XCL2	XCL1	XCL0	WSEL2	WSEL1	WSEL0	CKS3	CKS2	CKS1	CKS0	CKOI	CKOE	SCT
Reset		0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Note: set XS= 1 (05h) and INTXC(06h, page 9) to enable external crystal oscillator.

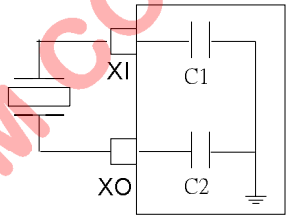
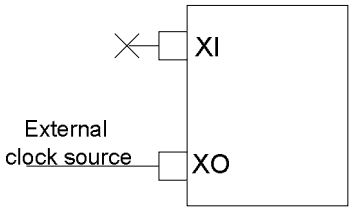


Figure11.1 Crystal network connection for using external crystal

11.2 Use External Clock

A7108 has built-in AC couple capacitor to support external clock input. Figure 11.2 shows how to connect. In such case, XI pin is left opened.

Note: set XS = 0 (05h) to select external clock (AC couple capacitor active.). And the frequency accuracy of external clock shall be controlled within ± 30 ppm and the clock swing (peak-to-peak) shall be larger than 1.0V.



External clock is controlled within ± 30ppm and Vpp is above 1.0V.

Figure 11.2 Connect to external clock source

12. System Clock

A7108's main system clock, F_{MSCK}, can be either come from Xtal oscillator itself or from the internal clock generator. The purpose of the internal clock generator is used to support multi Xtal frequency and/or special requirements of the wanted data rate.

12.1 Clock Domain

Since F_{MSCK} is the root of the IF Filter calibration clock, data rate clock as well as baseband clock, therefore, there are several clock dividers implemented by configurable registers such as CSC, SDR, DMOS, MCNT and MCNTR. Table 12.1 lists the most important constraints how to configure those registers successfully and figure 12.1 illustrates the detailed clock domain.

Signal	Constraints	Note
F_{MSCK} (main system clk)	If CGS = 0, F_{MSCK} = Xtal freq. If CGS = 1, F_{MSCK} = Clk Gen	If using Clk Gen, F_{MSCK} range can be from 20M ~ 50MHz that depends on GRC and GRS.
DCK (data rate clock)	$DCK = \frac{1}{128} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$	DCK = the wanted data rate
Demodulator Oversample	F_{MSCK} = F_{IFREF} x (64)	Use 64 oversample by set DMOS = 0
IFBW calibration	F_{IFREF} = IF Filter BW x (2)	F_{IFREF} is derived from F_{MSCK}
PF8M	equal or close to 6.4MHz	Set WRCKS = 0 for successful WOR calibration
	equal or close to 8MHz	Set WRCKS = 1 for successful WOR calibration

Table 12.1 Constraints of the key signals and its usage.

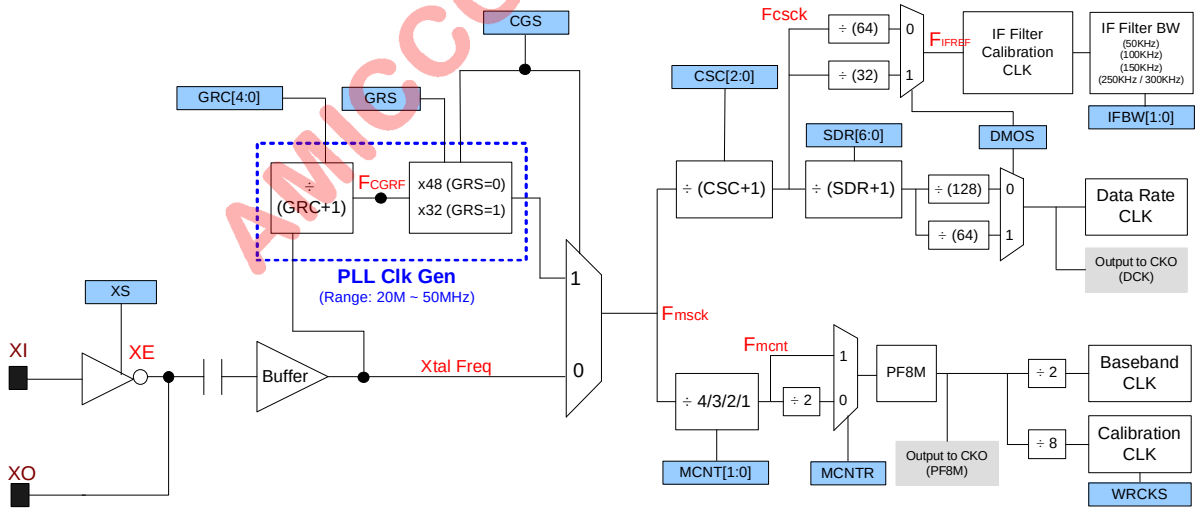


Figure 12.1 Illustrations from Xtal oscillator to main system clock and its clock domain.

12.2 System Clock and IF Filter

In general, data rate is almost the first consideration to start a new design. While choosing a wanted data rate, A7108 offers 4 optional IFBW (50KHz / 100KHz / 150KHz / 250KHz) to trade off RX sensitivity and frequency offset.

Table 12.2 lists the recommended IFBW vs data rate. For example, 10Kbps data rate is mapping to 50KHz IFBW. In this case, using ± 10 ppm Xtal is necessary because the narrower IFBW the poorer tolerance of frequency offset, but, the better RX sensitivity. However, user can also choose 100KHz IFBW to deal with a larger frequency offset, that means using a larger Xtal tolerance is ok, i.e. ± 20 ppm. But, its disadvantage is to suffer RX sensitivity.

Data rate	IFBW	F_{IFREF}	Constraints
2K ~ 50kbps	~ 50kHz	~ 50kHz x 2	The actual F_{IFREF} ,which is derived from system clock, is double of IFBW
≦100kbps	~ 100kHz	~ 100kHz x2	
≦150kbps	~ 150kHz	~ 150kHz x2	
≦250kbps	~ 250kHz	~ 250kHz x2	

Table 12.2 General case of IFBW mapping to Data Rate.

12.3 Example of 10Kbps data rate by 12.8MHz Xtal

Since IFBW is so important to impact RX sensitivity, A7108 has an IFBW calibration procedure to overcome the process deviation of semiconductor. To make a successful IFBW calibration, the relationships among F_{MSCK}, F_{IFREF} and DCK must be satisfied. Figure 12.2 illustrates the detailed configurations to clock dividers.

1. Data rate = 10Kbps
2. Xtal = 12.8MHz
3. Clk Gen = disable
4. IFBW[1:0] = [00], targeted BW = 50KHz

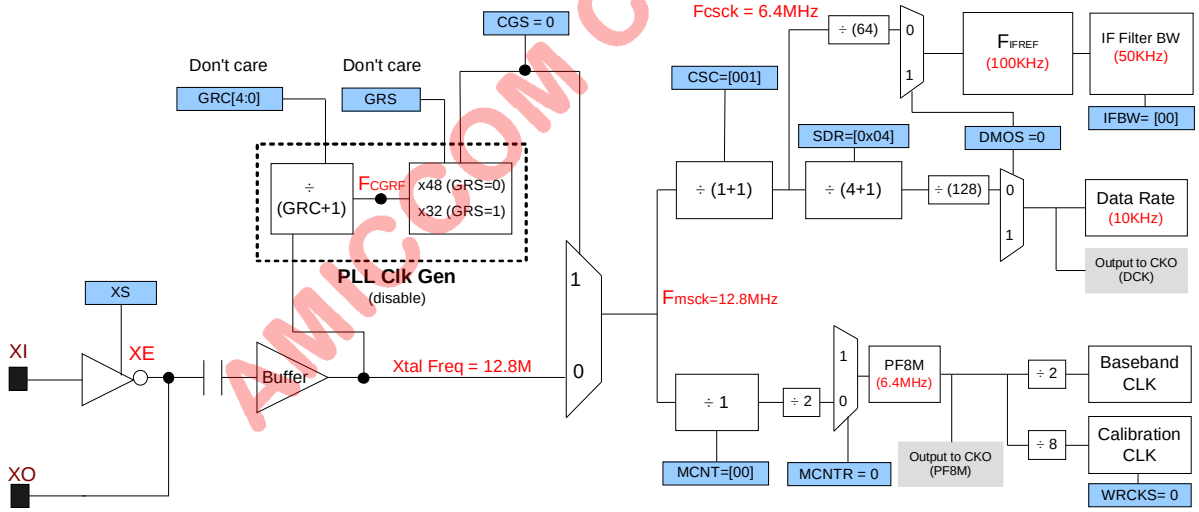


Figure 12.2 Configurations of 10Kbps when IFBW = 50KHz

5. If choosing IFBW = 100KHz, figure 12.3 illustrates the different results of CSC and F_{CSCK}.
6. Data rate = 10Kbps
7. Xtal = 12.8MHz
8. Clk Gen = disable
9. IFBW[1:0] = [01], targeted BW = 100KHz

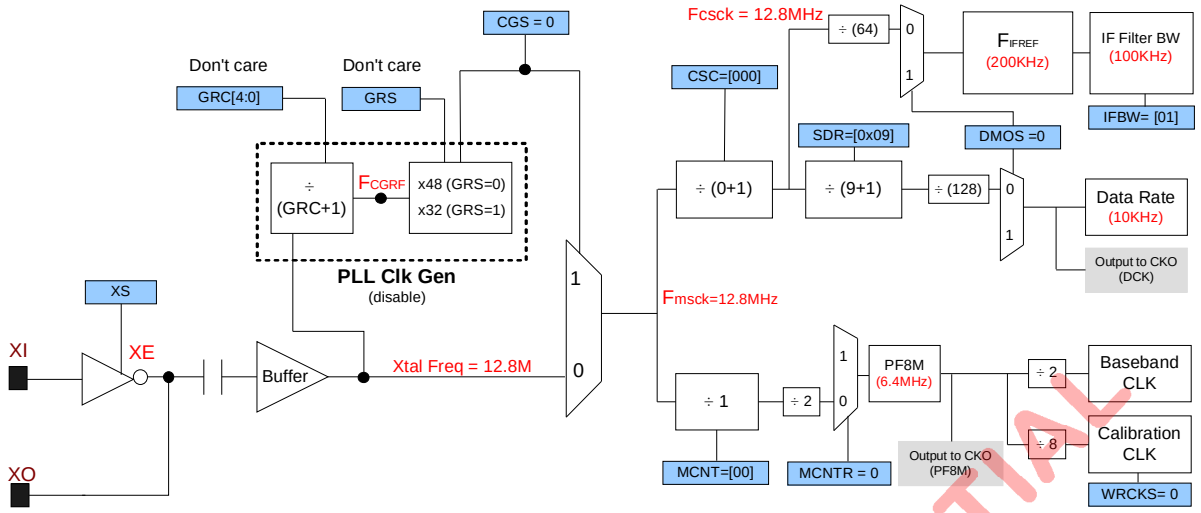


Figure 12.3 Configurations of 10Kbps when IFBW = 100KHz

12.3 Example of special data rate by 19.6608MHz Xtal.

A7108 can support most general data rate such as 10K, 50K, 100K, 150K, 250Kbps. For special data rate such as 38.4Kbps, the internal Clk Gen can be enabled with a special Xtal frequency to get the wanted DCK and IFBW. Figure 12.4 illustrates the detailed configurations to clock dividers.

1. Data rate = 38.4Kbps
2. Xtal = 19.6608MHz
3. Clk Gen = disable
4. IFBW[1:0]= [10] , targeted BW = 150KHz

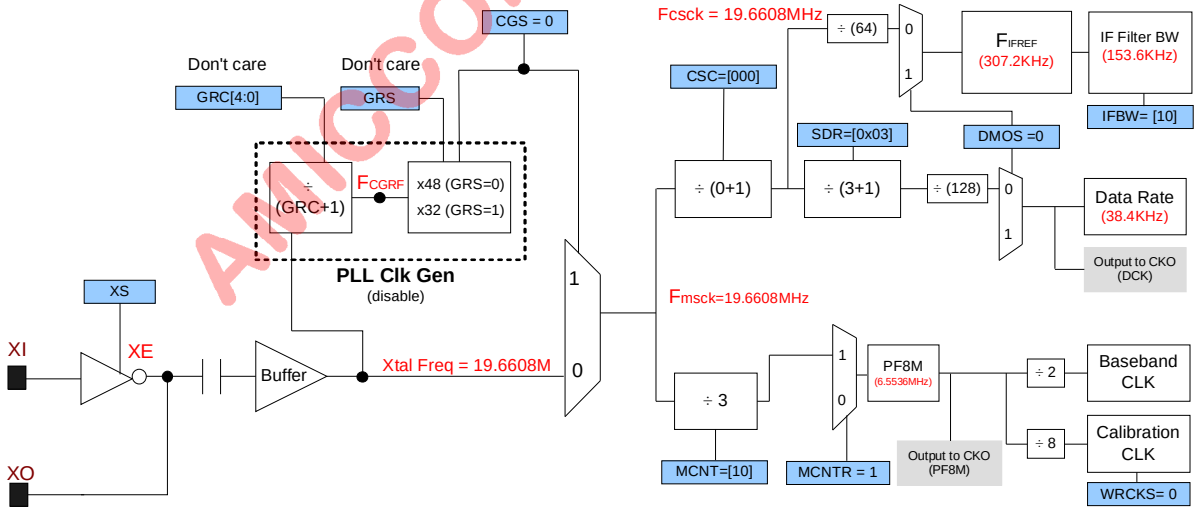


Figure 12.4Configurations of 38.4Kbps when IFBW = 153.6KHz

5. If choosing IFBW = [11]. IFBW will become 307.2KHz instead of the expected 250KHz because of F_{IFREF} (higher F_{IFREF} results larger IF bandwidth if IF Filter Calibration is successful.). Figure 12.5 illustrates the different results of CSC and FCSCK.
6. Data rate = 38.4Kbps
7. Xtal = 19.6608MHz
8. Clk Gen = enable
9. IFBW = 307.2KHz

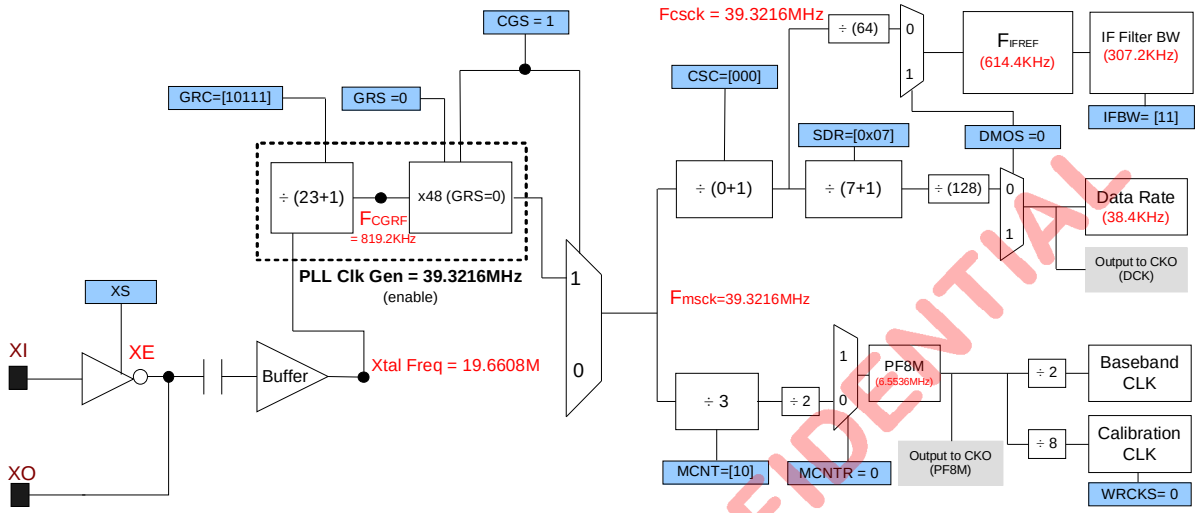


Figure 12.5Configurations of 38.4Kbps when IFBW = 307.2KHz

13. Tranceiver Frequency

A7108 supports wide range of RF operation among 315/433/470/868/915MHz band. Hence, VCO frequency (F_{LO}) is implemented to be related to MD and VBS divider to result RF frequency (F_{RF}). Figure 13.1 and below formula illustrate how to get a wanted RF frequency.

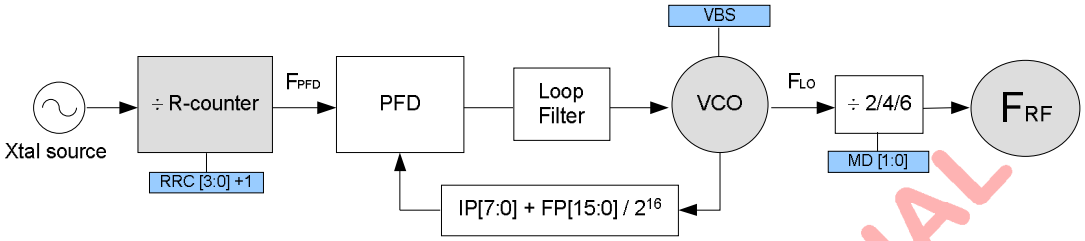


Figure 13.1 Frequency synthesizer block diagram

$$f_{RF} = \frac{1}{n} f_{PFD} \cdot (IP[7:0] + \frac{FP[15:0]}{2^{16}}) \quad \text{(unit: Hz)}$$

where f_{RF} is the wanted RF frequency and ***n*** is the VCO divider.

where $f_{PFD} = f_{Xtal} \div (RRC[3:0]+1)$, is the comparison frequency of RF_PLL.

Where n = 2 by setting MD = [01] for 868M / 915MHz band
Where n = 4 by setting MD = [10] for 433M / 510MHz band
Where n = 6 by setting MD = [11] for 315MHz band

Note1: MD[1:0] is located at address 04h [Bit12, Bit8].

Example:
How to get (F_{RF}) = 433.921MHz by a 12.8MHz Xtal.

1. Set RRC = [000], (F_{PFD}) = Xtal frequency = 12.8MHz.
2. Set VBS (0Fh) = [1] for 433MHz band.
3. Set MD (04h) = [10] for 433MHz band. Then, n = 4.
4. Set IP [7:0] for integer part. Set IP[7:0] = 135 = 0x87

   Based on IP [7:0] range, MDIV (01h) shall be [1] because of below formula.
   MDIV = [0], when 32 ≦ IP[7:0] ≦ 67.
   MDIV = [1], when 68 ≦ IP[7:0] ≦ 255.
5. Set FP [15:0] for fractional part. Set FP = 39342 = 0x99AE
6. $$f_{RF} = \frac{1}{n} f_{PFD} \cdot (IP[7:0] + \frac{FP[15:0]}{2^{16}}) = \frac{1}{4} \times 12.8 \times (135 + \frac{39342}{2^{16}}) = 433.921 \text{ (MHz)}$$
7. For TX radio frequency (F_{TXRF}) is equal to F_{RF}.
8. RX LO frequency (F_{RXLO}) is shall be set to ONE F_{IF} offset because low-IF architecture.

   RX LO frequency $F_{RXLO} = F_{TXRF} - F_{IFREF}$; when ULS (08h)= 0, up side band.

14. State machine

A7108 has seven major operation modes from current consumption point of view as shown in Table 14.1. From accessing data point of view, if FMS=1 (0Fh), FIFO mode is enabled, otherwise, A7108 is in direct mode.

14.1 Key Strobe Commands

A7108 has below 7 operation modes in current consumption point of view. Those are,
(1) Deep Sleep mode
(2) Sleep mode
(3) Idle mode
(4) Standby mode
(5) PLL mode
(6) TX mode
(7) RX mode

After power on reset or software reset or deep sleep mode, user has to do calibration process because all control registers are in initial values. The calibration process of A7108 is very easy, user only needs to issue Strobe commands and enable calibration registers. If so, the calibrations are automatically completed by A7108's internal state machine. Table 14.1 shows a summary of key circuitry among those strobe commands.

Mode	Register retention	Regulator	Xtal Osc.	VCO	PLL	RX	TX	Strobe Command
Deep Sleep (Tri-state)	No	OFF	OFF	OFF	OFF	OFF	OFF	(0001-1100)b
Deep Sleep (pull-high)	No	OFF	OFF	OFF	OFF	OFF	OFF	(0001-1111)b
Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	(0001-0000)b
Idle	Yes	ON	OFF	OFF	OFF	OFF	OFF	(0001-0010)b
Standby	Yes	ON	ON	OFF	OFF	OFF	OFF	(0001-0100)b
PLL	Yes	ON	ON	ON	ON	OFF	OFF	(0001-0110)b
TX	Yes	ON	ON	ON	ON	OFF	ON	(0001-1000)b
RX	Yes	ON	ON	ON	ON	ON	OFF	(0001-1010)b
SW RST								(x111-xxxx)b

Remark: x means "don't care"

Table 14.1. Operation mode and strobe command

14.2 FIFO mode

This mode is suitable for the requirements of general purpose applications and can be chosen by setting FMS = 1. After calibration, user can issue Strobe command to enter standby mode where write TX FIFO or read RX FIFO. From standby mode to packet data transmission, only one Strobe command is needed. Once transmission is done, A7108 is auto back to standby mode. Figure 14.1 and Figure 14.2 are TX and RX timing diagram respectively. Figure 14.3 illustrates state diagram of FIFO mode.

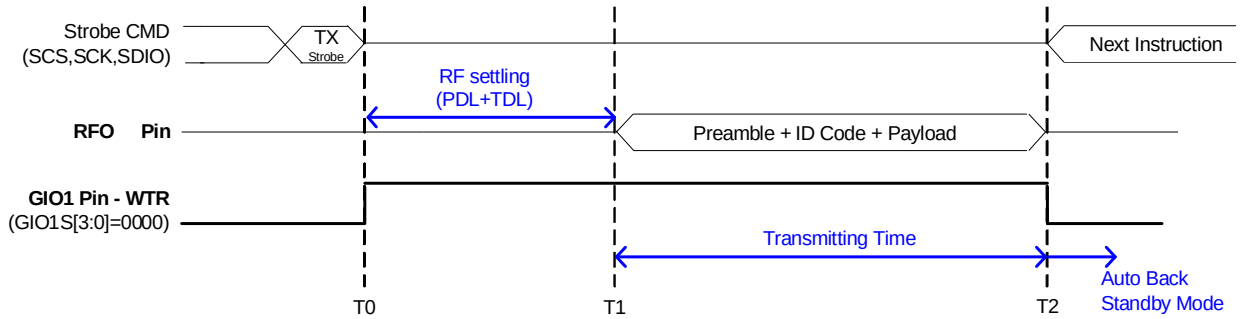


Figure 14.1 TX timing of FIFO Mode

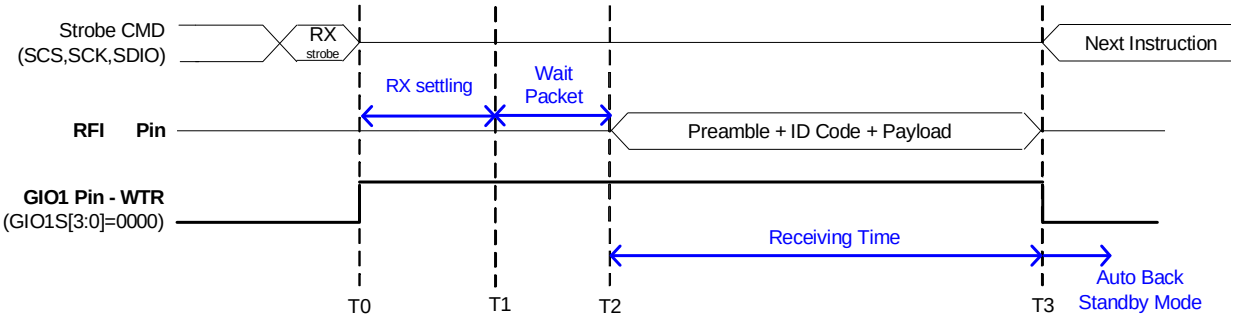


Figure 14.2 RX timing of FIFO Mode

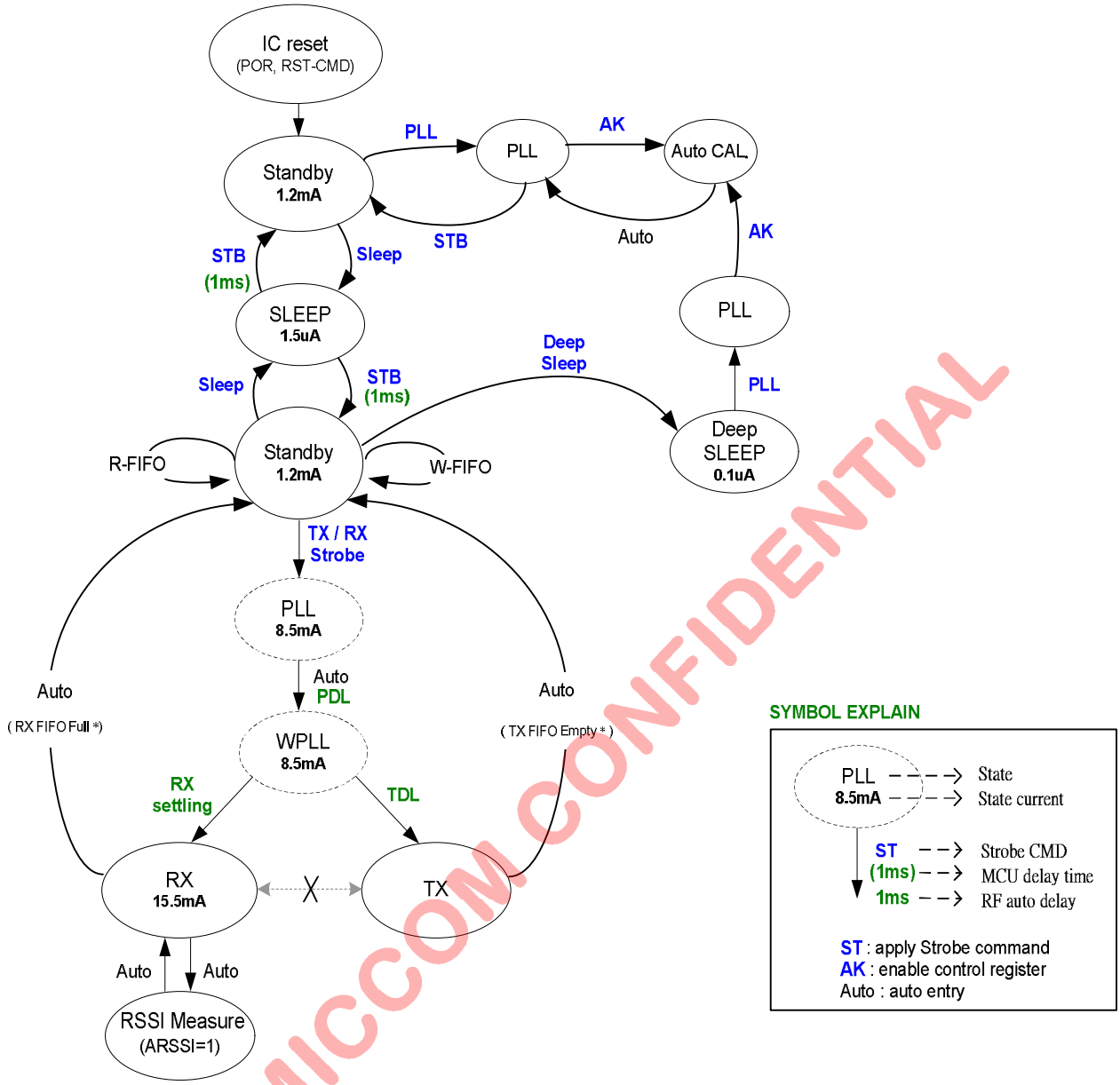


Figure 14.3 State diagram of FIFO Mode

14.3 Direct mode

This mode is suitable to let MCU to drive customized packet to A7108 directly by setting FMS = 0. In TX mode, MCU shall send customized packet in bit sequence (simply called raw TXD) to GIO1 or GIO2 pin. In RX mode, the receiving raw bit streams (simply called RXD) can be configured output to GIO1 or GIO2 pin. Be aware that a customized packet shall be preceded by a 32 bits preamble to let A7108 get a suitable DC estimation voltage. After calibration flow, for every state transition, user has to issue Strobe command to A7108 for fully control. This mode is also suitable for the requirement of versatile packet format.

Figure 14.4 and Figure 14.5 are TX and RX timing diagram in direct mode respectively. Figure 14.3 illustrates state diagram of direct mode.

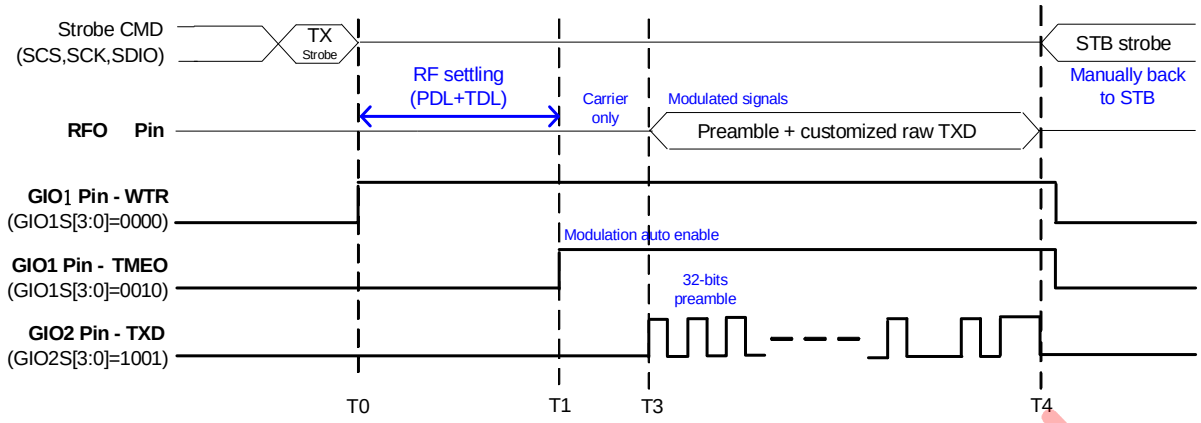


Figure 14.4 TX timing of Direct Mode

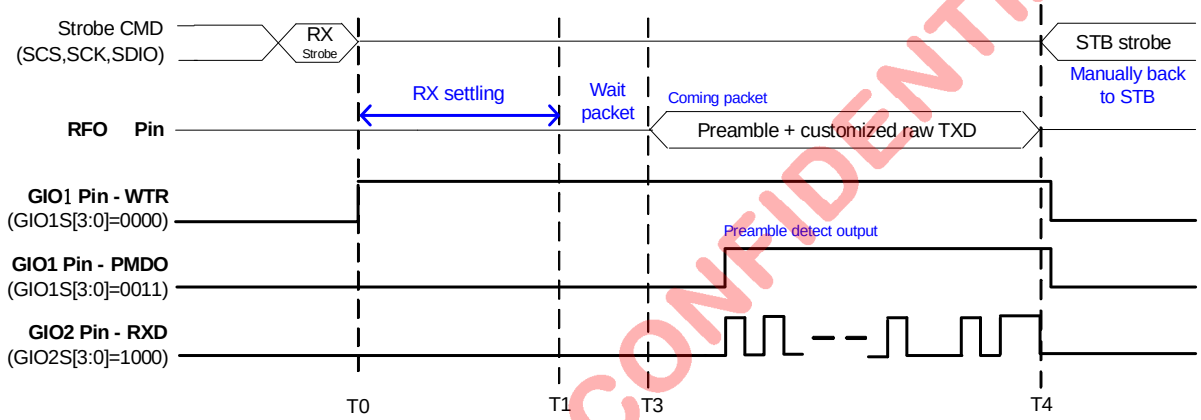


Figure 14.5 RX timing of Direct Mode

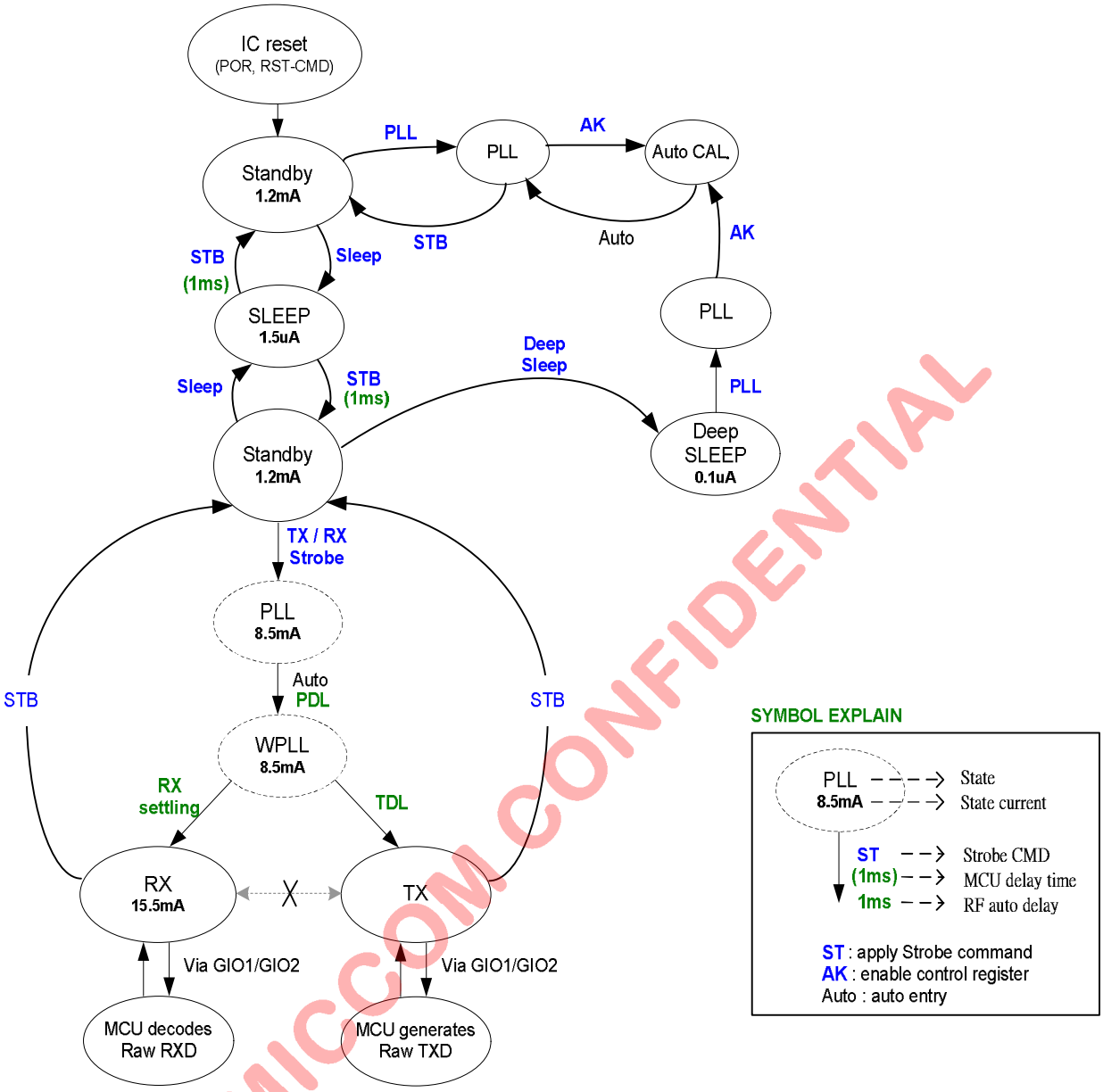


Figure 14.6 State diagram of Direct Mode

15. Calibration

A7108 needs calibration process during initialization with 2 calibration items, they are IF CAL (IF Filter calibration) and VCO band CAL (VCO band calibration).

1. VCO Bank Calibration is to select best VCO frequency bank for the calibrated frequency.
2. IF Filter Bank Calibration is to calibrate IF filter bandwidth and center frequency.

Please notice that VCO Current, Bank and Deviation should be calibrated in PLL mode by sequence. IF Filter Bank and RSSI could be calibrated in either standby or PLL mode.

15.1 IF Calibration Process

Under the Stand by state (XOSC is on), set bit MIFS=0(auto calibration) or bit MIFS=1(Manual calibration) to execute the IF calibration. When the mode control register bit FBC=1, the chip will enter CAL state, and starts the calibration process.

If RF chip is not in the STB state when bit FBC is set to 1, RF chip will not start the calibration process until it enters the STB state. Once the calibration is completed, bit FBC will be cleared to 0 automatically, and RF chip will leave from CAL state and back to STB state.

If the mode control register bit TRER=1, FBC=1 or VBC=1are set simultaneously, RF chip will enter the CAL state first, and after completion of IF filter calibration or VCO band calibration process, RF chip can then enter into TX/RX state. The maximum time required for A7108 RF chip to perform IF Calibration process is about 16 * 256 * (1 / system clock).

15.2. VCO band Calibration Process

Before the VCO band calibration, user should first set operating frequency in PLL I and PLL II registers, meanwhile, the range of VT (VTH[2:0], VTL[2:0]) and VCO also needs to be set properly.

Under the Stand by state (XOSC is on), set bit MVBS=0(auto calibration) or bit MVBS=1(manual calibration) to execute the VCO band calibration. After setting the mode control register bit VBC=1, the chip will enter CAL state, and starts the calibration process. If RF chip is not in the STB state when bit VBC is set to 1, RF chip will not start the calibration process until it entering STB state. When the calibration is completed, bit VBC will be cleared to 0 automatically, and chip will leave from CAL state and back to STB state.

If the mode control register bit TRER=1, FBC=1 or VBC=1are set simultaneously, RF chip will enter the CAL state first, and after completion of IF filter calibration or VCO band calibration process, RF chip can then enter into TX/RX state. The maximum time required for A7108 RF chip to perform IF Calibration process is about 16 * 256 * (1 / system clock). The maximum time required for A7108 RF chip to perform VCO band Calibration process is about 4 * PLL settling time.

Calibration (Address: 0Eh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh Calibration	W		VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MIFS	MIF3	MIF2	MIF1	MIF0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0

16. FIFO (First In First Out)

A7108 supports separated 64-bytes TX and RX FIFO by enabling FMS =1 (0Fh). TX FIFO represents transmitted payload. On the other hand, once RX circuitry synchronizes ID Code, received payload is stored into RX FIFO.

16.1 Packet Format

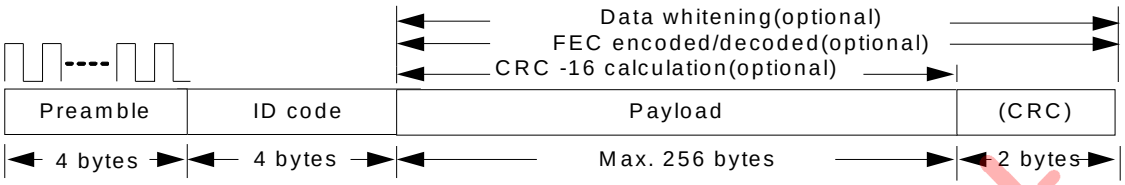


Figure 16.1 Packet Format of FIFO mode

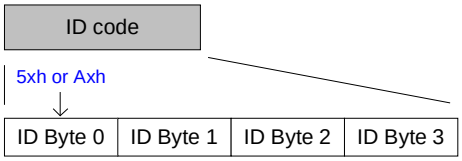


Figure 16.2 ID Code Format

Preamble:
The packet is led by preamble composed of alternate 0 and 1. If the first bit of ID code is 0, preamble shall be 0101…0101. In the contrast, if the first bit of ID code is 1, preamble shall be 1010…1010.
Preamble length is recommended to set 4 bytes by PML [1:0] (0Ch).

ID code:
ID code is recommended to set 4 bytes by IDL=1 (0Ch). ID Code is sequenced by Byte 0, 1, 2 and 3 (Recommend to set ID Byte 0 = 5xh or Axh). If RX circuitry checks the ID code correct, received payload will be stored into RX FIFO. In special case, ID code could be set error tolerance (0~ 3bit error) by ETH [1:0] (08h) for ID synchronization check.

Payload:
Payload length is programmable by FEP [7:0] (0Bh) from 1 byte to 64 bytes. The physical FIFO depth is 64 bytes. A7108 also supports logical FIFO extension up to 256 bytes. See section 16.4.3 for details.

CRC (option):
In FIFO mode, if CRC is enabled (CRCS=1, 0Ch), 2-bytes of CRC value is transmitted automatically after payload. In the same way, RX circuitry will check CRC value and show the result to CRC Flag (0Fh).

16.2 Bit Stream Process

A7108 supports 3 optional bit stream processes for payload, they are,

(1) CCITT-16 CRC ($x^{16} + x^{15} + x^2 + 1$).
(2) (7, 4) Hamming FEC
(3) Data Whitening by XOR PN7 (7-bits Pseudo Random Sequence).

CRC (Cyclic Redundancy Check):

1. CRC is enabled by CRCS= 1 (0Ch). TX circuitry calculates the CRC value of payload (preamble, ID code excluded) and transmits 2-bytes CRC value after payload.
2. RX circuitry checks CRC value and shows the result to CRC Flag (0Fh). If CRCF=0, received payload is correct, else error occurred. (CRCF is read only, it is revised internally while receiving every packet.)

FEC (Forward Error Correction):

1. FEC is enabled by FECS= 1 (0Ch). Payload and CRC value (if CRCS=1) are encoded by (7, 4) Hamming code.
2. Each 4-bits (nibble) of payload is encoded into 7-bits code word as well as delivered out automatically. **(ex. 64 bytes payload will be encoded to 128 code words, each code word is 7 bits.)**
3. RX circuitry decodes received code words automatically. FEC supports 1-bit error correction each code word. Once 1-bit error occurred, FEC flag=1 (00h). (FECF is read only, it is revised internally while receiving every packet.)

Data Whitening:

1. Data whitening is enabled by WHTS= 1 (0Ch). The initial seed of PN7 is WS [6:0] (0Ch). Payload is always encrypted by bit XOR operation with PN7. CRC and/or FEC are also encrypted if CRCS=1 and/or if FECS=1.
2. RX circuitry decrypts received payload and 2-bytes CRC (if CRCS=1) automatically. Please notice that user shall set the same WS [6:0] (0Ch) to TX and RX.

16.3 Transmission Time

Based on CRC and FEC options, the transmission time differs depending on the chosen of CRC and FEC options. See table 16.1 for details.

Data Rate = 250 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 4 us = 2.304 ms
32	32	512	16 bits	Disable	592 bit X 4 us = 2.368 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 4 us = 3.840 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 4 us = 3.952 ms

Data Rate = 125 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 8 us = 4.608 ms
32	32	512	16 bits	Disable	592 bit X 8 us = 4.736 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 8 us = 7.580 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 8 us = 7.904 ms

Data Rate = 50 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 20 us = 11.52 ms
32	32	512	16 bits	Disable	592 bit X 20 us = 11.84 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 20 us = 19.20 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 20 us = 19.76 ms

Data Rate = 2 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 0.5 ms = 0.288 s
32	32	512	16 bits	Disable	592 bit X 0.5 ms = 0.296 s
32	32	512	Disable	512 x 7 / 4	960 bit X 0.5 ms = 0.480 s
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 0.5 ms = 0.494 s

Table 16.1 Transmission time

16.4 Usage of TX and RX FIFO

In application points of view, A7108 supports 3 options of FIFO arrangement.
(1) Easy FIFO
(2) Segment FIFO
(3) FIFO Extension

16.4.1 Easy FIFO Mode

In Easy FIFO mode, max FIFO length is 64 bytes. FIFO length is equal to **(FEP [7:0] +1)**. User just needs to control FEP [7:0] and disable PSA and FPM as shown below.

Register setting

TX	RX	Control Registers		
TX-FIFO (byte)	RX-FIFO (byte)	FEP[7:0]	PSA [5:0]	FPM [1:0]
1	1	0x00	0	0
8	8	0x07	0	0
16	16	0x0F	0	0
32	32	0x1F	0	0
64	64	0x3F	0	0

Table 16.2 Control registers of Easy FIFO

Procedure of TX FIFO Transmitting

1. Initialize all control registers (refer to A7108 reference code).
2. Set FEP [7:0] = 0x3F for 64-bytes FIFO.
3. Issue TX FIFO write pointer reset.
4. MCU writes 64-bytes data to TX FIFO.
5. Issue TX mode.
6. Done.

Procedure of RX FIFO Reading

1. When RX FIFO is full, WTR (or FSYNC) can be used to trigger MCU for RX FIFO reading.
2. Issue RX FIFO read pointer reset.
3. MCU read 64-bytes from RX FIFO.
4. Done

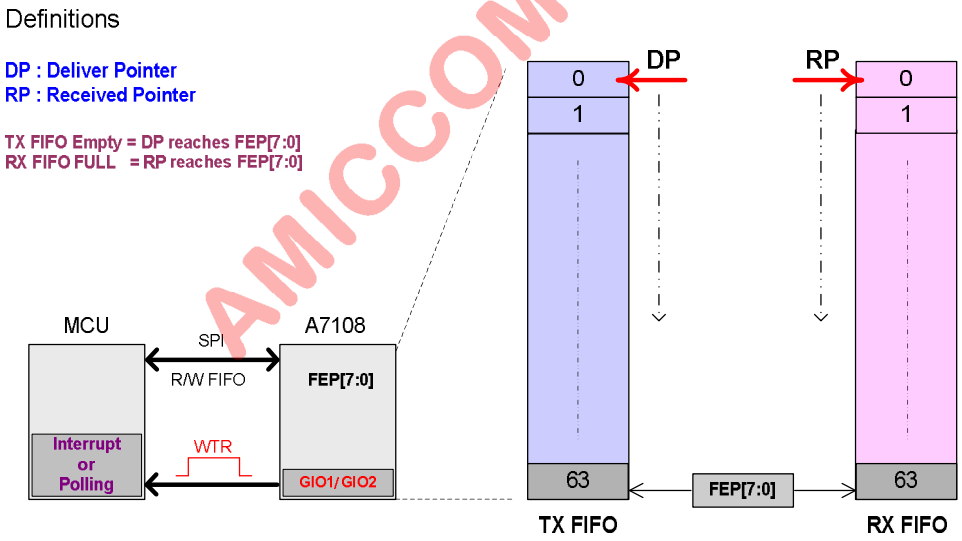


Figure 16.3 Easy FIFO mode

17. Analog Digital Converter

A7108 contains a built-in 8-bit ADC for internal temperature measurement, RSSI measurement.

XADS	CDM	None Rx state	RX state
0	0	Temperature measurement	RSSI measurement
0	1	N/A	Carrier detector

The conversion time of 8-bit ADC is depends on the clock input to ADC. It takes 20 cycles to complete the conversion. The clock source of ADC comes from Crystal oscillator, and according to the setting of bit GRC[4:0] in system clock register, user can select the ADC clock source to be 800KHz or 1.2MHz.

17.1 Temperature Measurement

A7108 has a simple on-chip temperature sensor. Set bit =0 in ADC register first, then enable bit ADCM=1 in the mode control register to start the measurement of temperature. When the measurement is completed, the bit ADCM will be cleared to 0. User can then read the ADC[7:0] values from the ADC register.

17.2 RSSI Measurement

A7108 has a built-in RSSI (received signal strength indicator) read from ADC to measure the received RF signal strength. When the measurement procedure is completed, the RSSI value can be read form ADC register, the range of RSSI is 0~511. Larger signal strength is corresponding to smaller RSSI value, and vice versa. In RX state, set bit CDM=0 in ADC register, and then set bit ADCM=1 in mode control register to start the RSSI measurement. Once the measurement is completed, the bit ADCM will be cleared to 0. User can read the RSSI value from ADCO[8:0] (0x09).

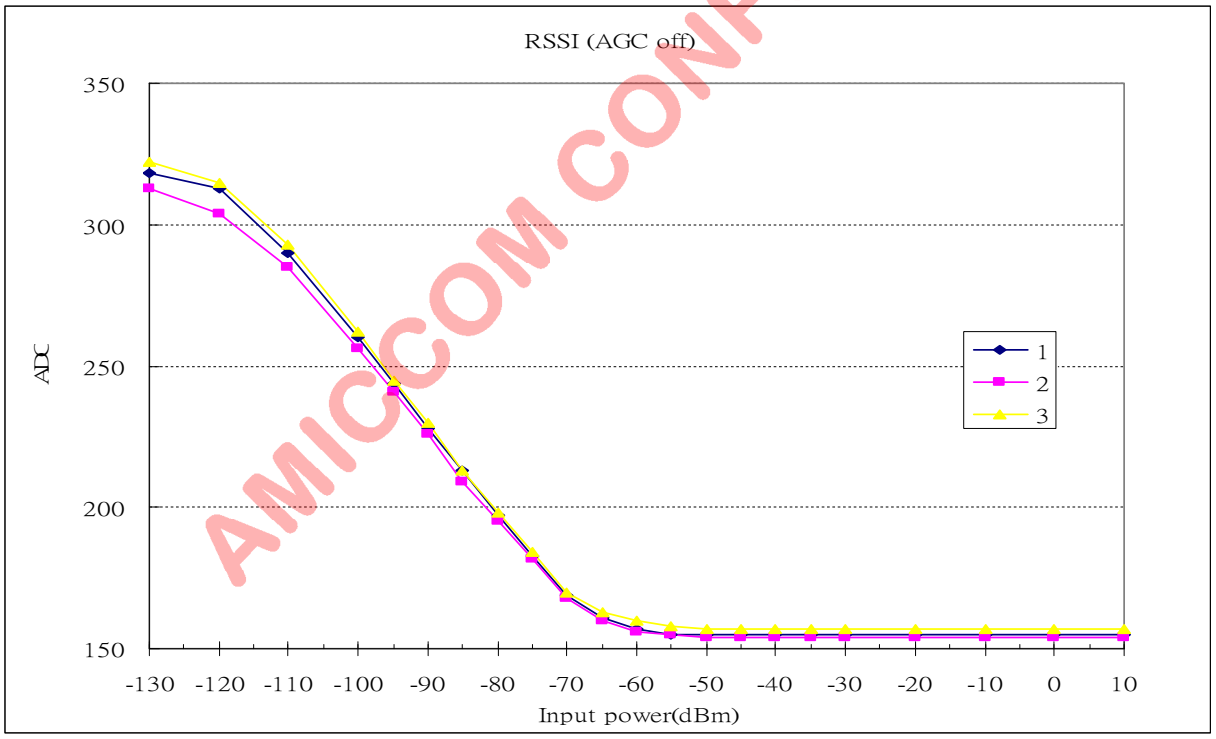


Figure 17.1 RSSI curve when AGC is disabled

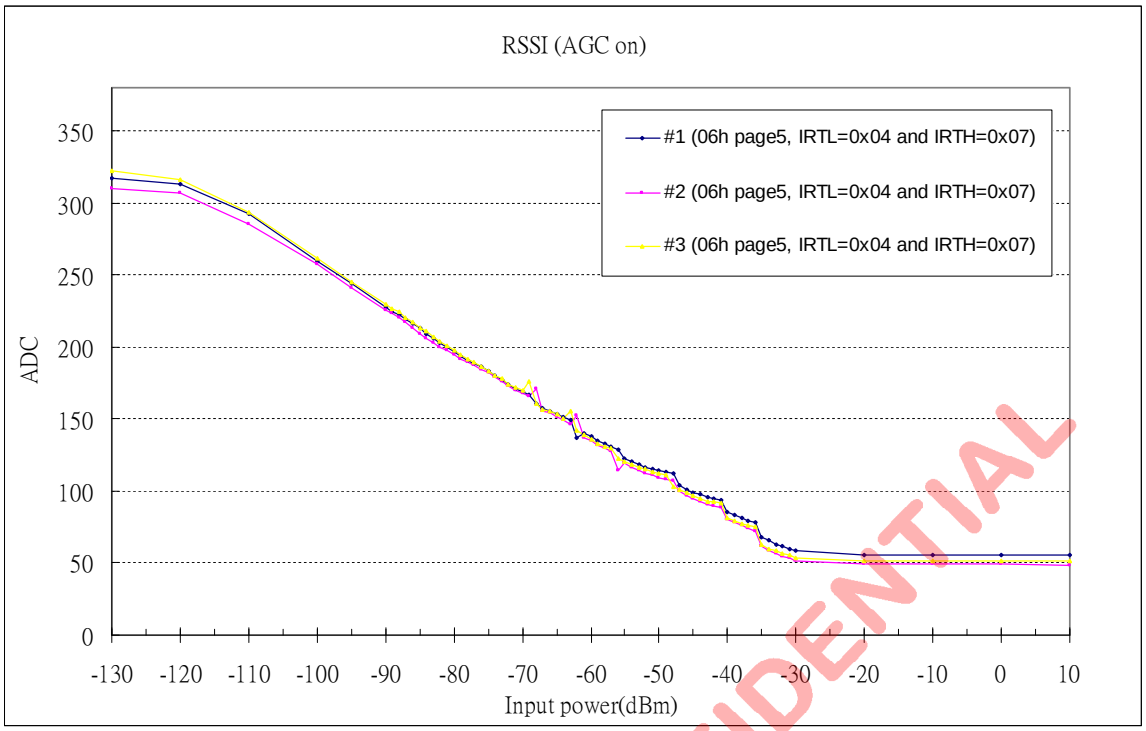


Figure 17.1 RSSI curve when AGC is enabled

17.3 Carrier detect

A7108 provides an CD signal (output from GIO1 or GIO2) to monitor that there is a carrier or not. If the carrier signal strength is greater than the value set by bit RTH[7:0] in ADC register, CD will go high, or it will stay low. In RX state, set ADC register bit CDM=1, set mode control register bit ADCM=1 to start the carrier signal measurement. The value is stored in bit ADC[7:0] and it will be updated in each measurement period till the end of detection action.

18. Battery Detect

A7108 has built-in battery detector to check supply voltage (REGI pin). After enable battery detect function, user can read VBD flag or output VBD to GIO1 or GIO2. The detect range is 2.0V ~ 2.7V in 8 levels.

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h PM	W	-	POWRS	CELS	STS	LVR	RGS	RGC1	RGC0	SPSS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BDS
Reset		-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BVT [2:0]: Battery Voltage Threshold select.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V. **[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

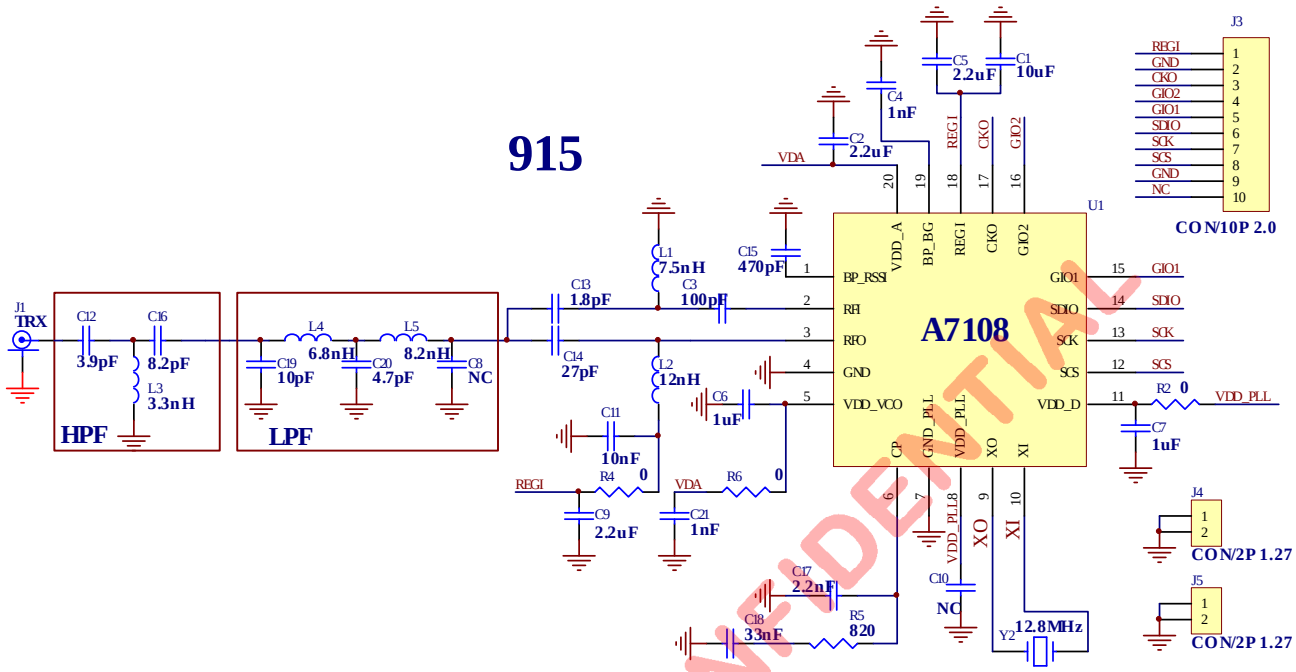
BDS: Battery Detection selection.
[0]: Disable. **[1]:** Enable.

Below is the procedure of battery detect for low voltage detection (ex., below 2.1V):

1. Set A7108 in standby or PLL mode.
2. Set detection level by BVT [2:0] = [001] and enable BDS = 1.
3. After 5 us, BDS is auto clear.
4. MCU check VBD flag.
   If REGI pin > 2.1V,
   VBD = 1. Else, VBD = 0.

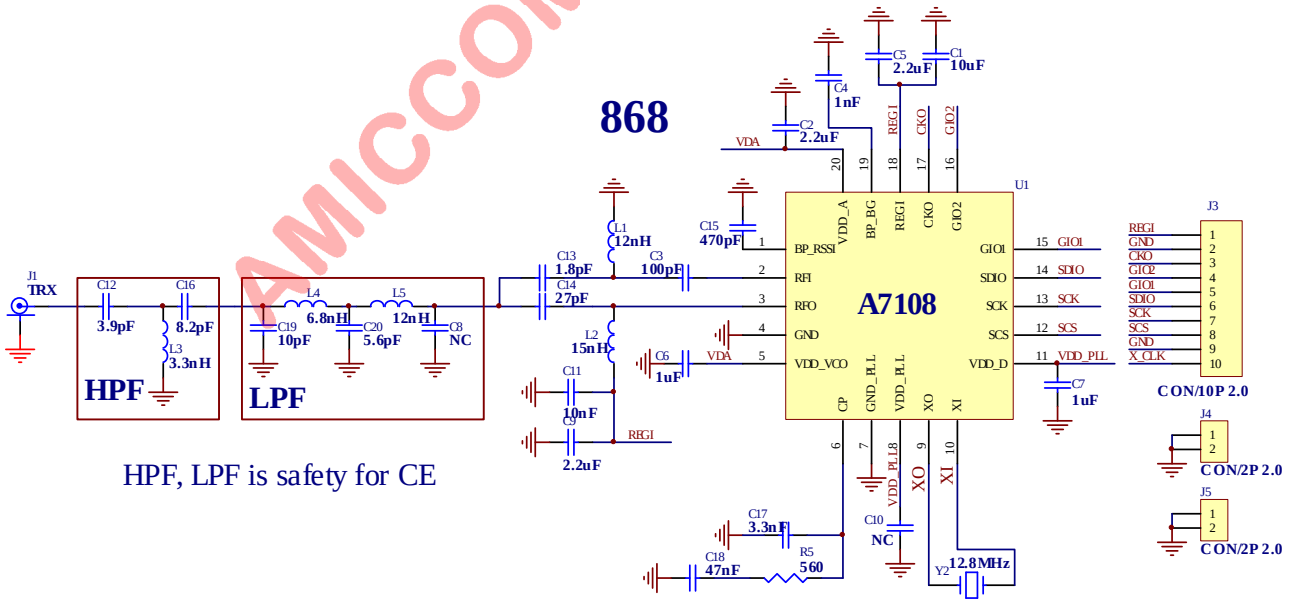
19. Application Circuit

19.1 MD7108-A90 (915MHz Band)



Recommend Xtal Cload = 20 pF

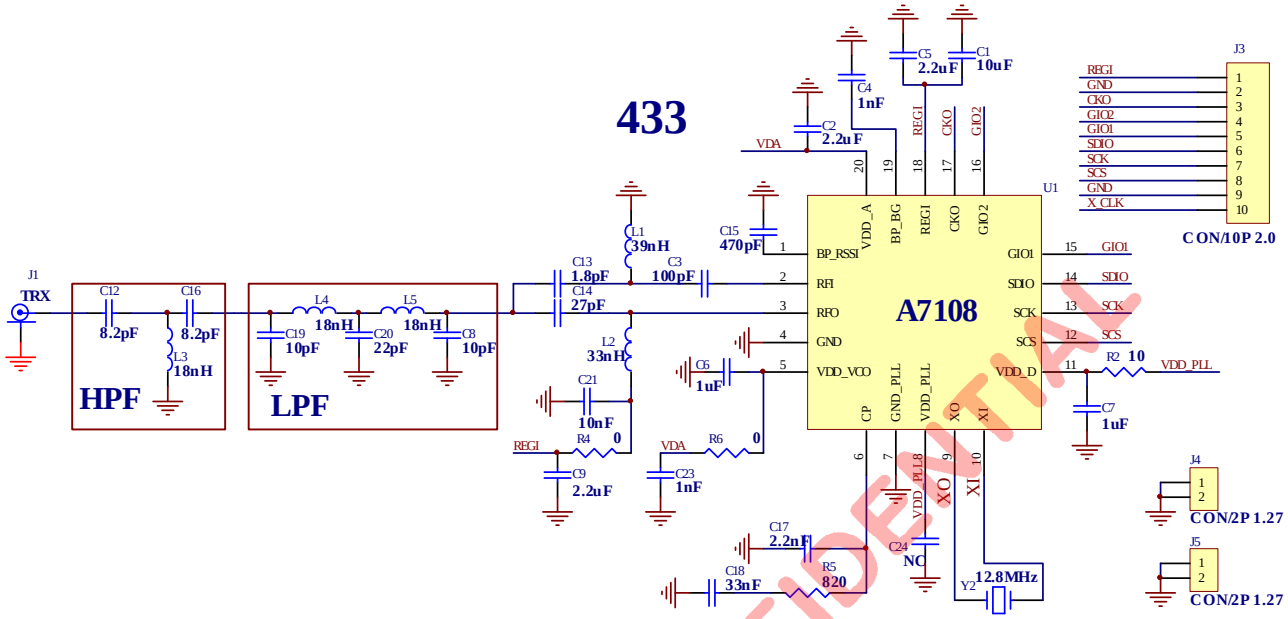
19.2 MD7108-A80 (868MHz Band)



HPF, LPF is safety for CE

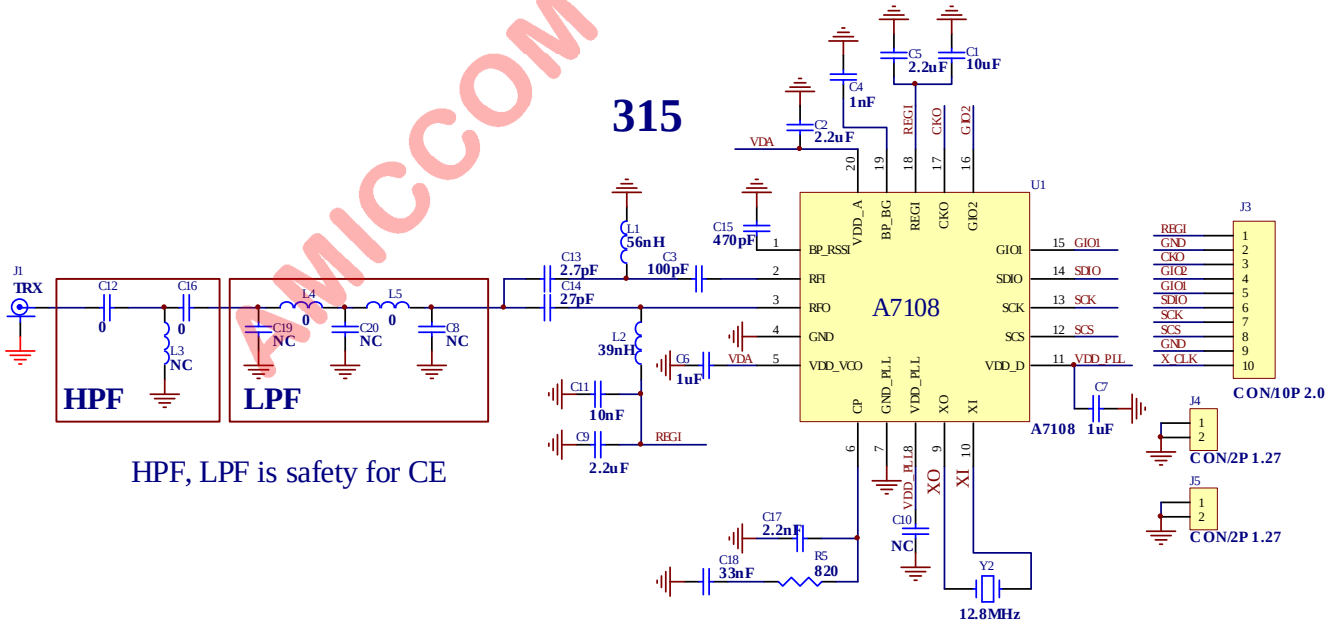
Recommend Xtal Cload = 20 pF

19.3 MD7108-A40 (433MHz Band)



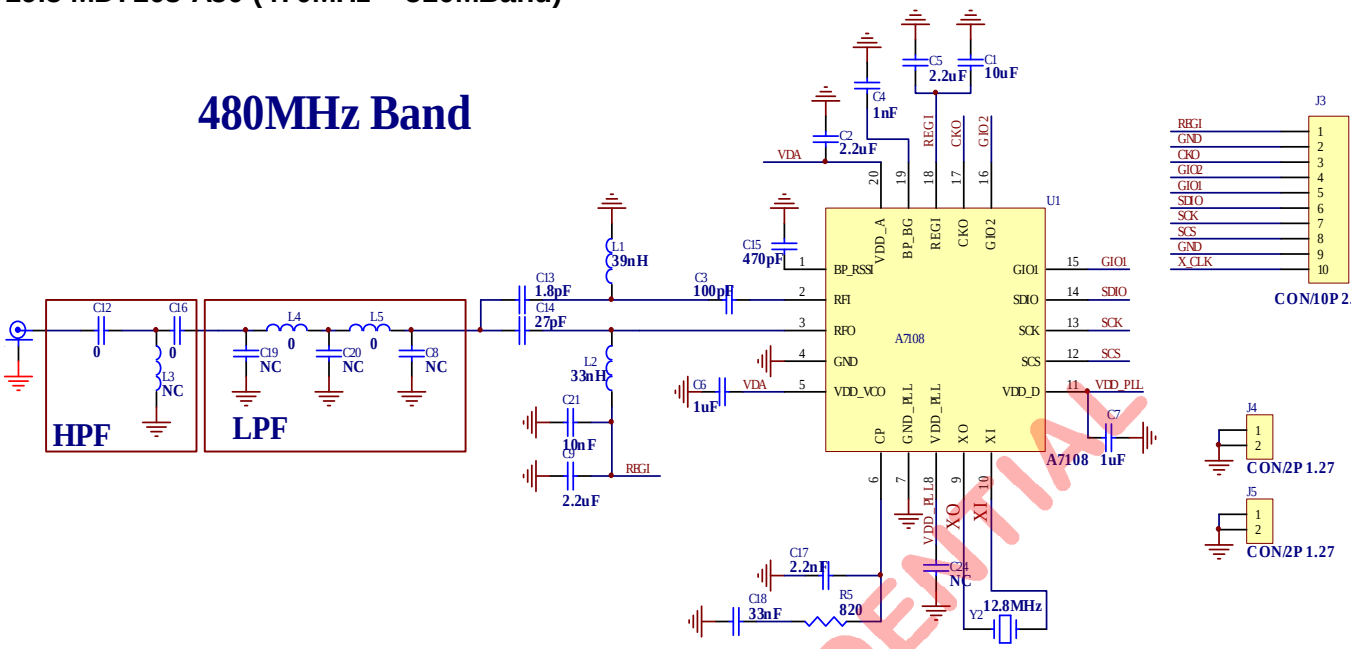
Recommend Xtal Cload = 20 pF

19.4 MD7108-A30 (315MHz Band)



Recommend Xtal Cload = 20 pF

19.5 MD7108-A50 (470MHz ~ 510MBand)



Recommend Xtal Cload = 20 pF

20. Abbreviations

ADC	Analog to Digital Converter
AFC	Automatic Frequency Compensation
AGC	Automatic Gain Control
BER	Bit Error Rate
BW	Bandwidth
CD	Carrier Detect
CRC	Cyclic Redundancy Check
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	PLL
PLL	Phase Lock Loop
POR	Power on Reset
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXRF	Transmitter Radio Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

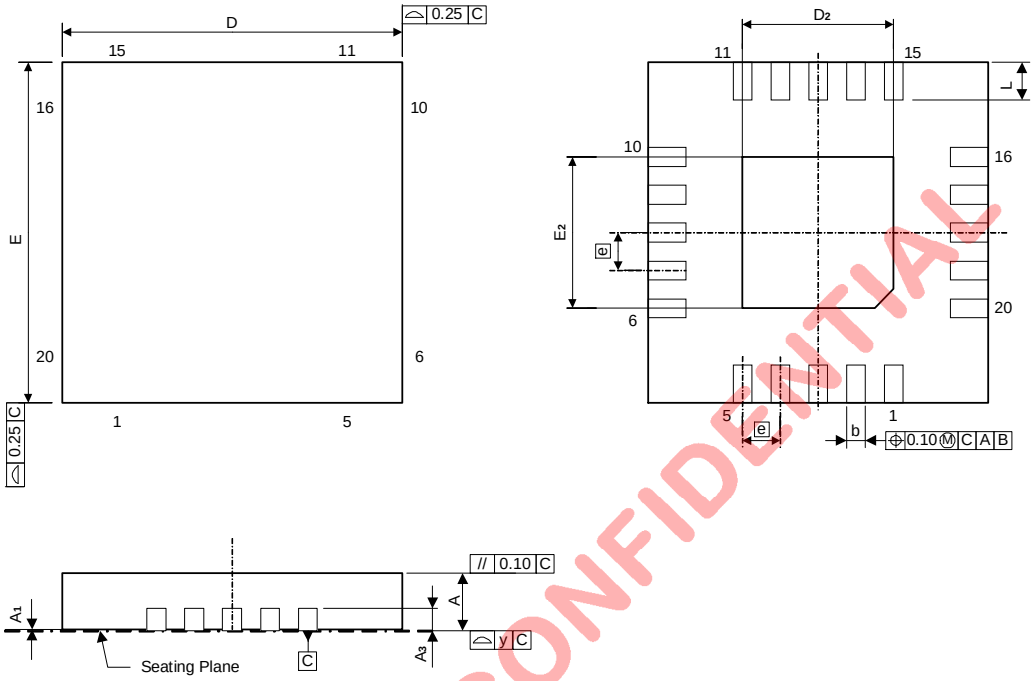
21. Ordering Information

Part No.	Package	Units Per Reel / Tray
A71X08AQFI/Q	QFN20L, Pb Free, Tape & Reel, -40℃～85℃	3K
A71X08AQFI	QFN20L, Pb Free, Tray, -40℃～85℃	490EA
A71X08AH	Die form, -40℃～85℃	100EA

22. Package Information

QFN 20L (4 X 4 X 0.8mm) Outline Dimensions unit: inches/mm

TOP VIEW **BOTTOM VIEW**

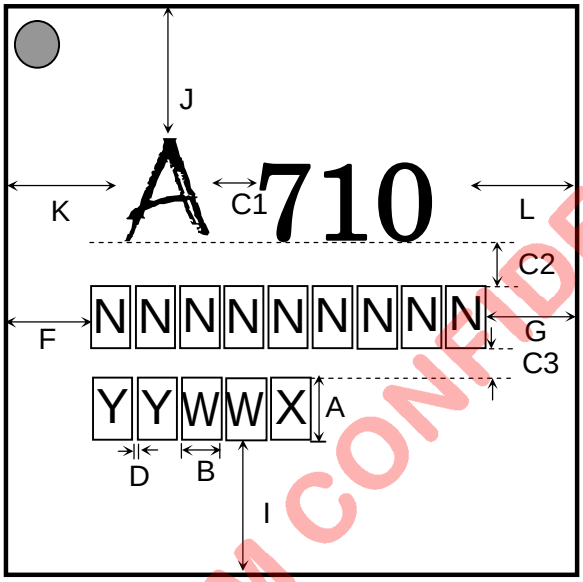


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3	0.008 REF			0.203 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.154	0.158	0.161	3.90	4.00	4.10
D_2	0.075	0.079	0.083	1.90	2.00	2.10
E	0.154	0.158	0.161	3.90	4.00	4.10
E_2	0.075	0.079	0.083	1.90	2.00	2.10
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50
y	0.003			0.08		

23. Top Marking Information

A71X08AQFI

- Part No. : **A71X08AQFI**
- Pin Count : **20**
- Package Type : **QFN**
- Dimension : **4*4 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**



❖ **CHARACTER SIZE : (Unit in mm)**

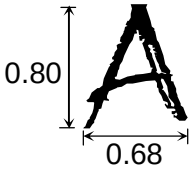
A : 0.55
B : 0.36
C1 : 0.25 C2 : 0.3 C3 : 0.2
D : 0.03

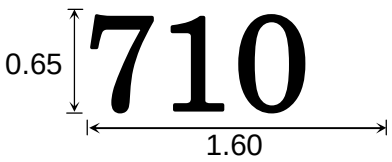
F=G
I=J
K=L

Y Y W W : DATECODE

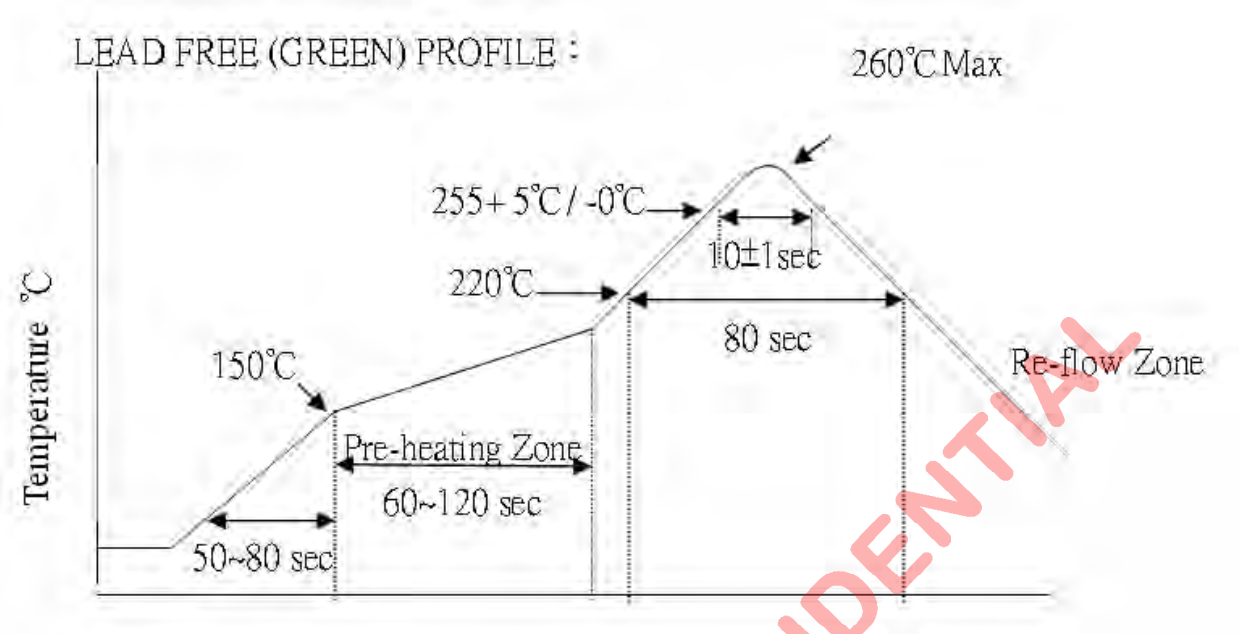
X : PKG HOUSE ID

N N N N N N N N N : LOT NO.
(max. 9 characters)



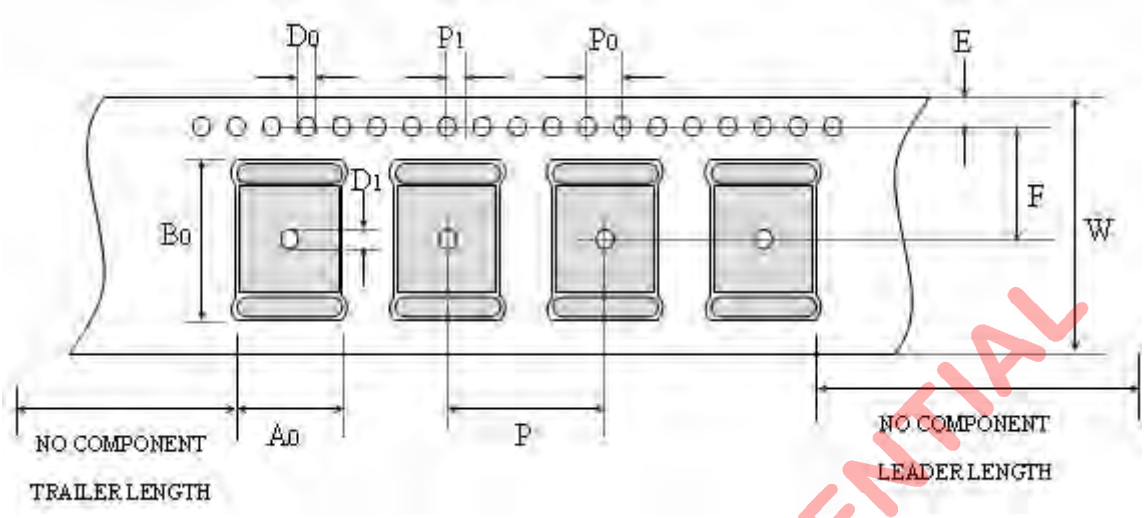


24. Reflow Profile



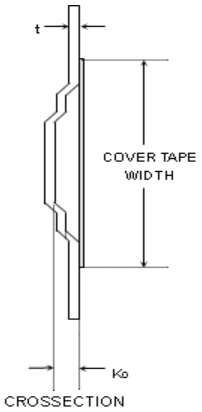
25. Tape Reel Information

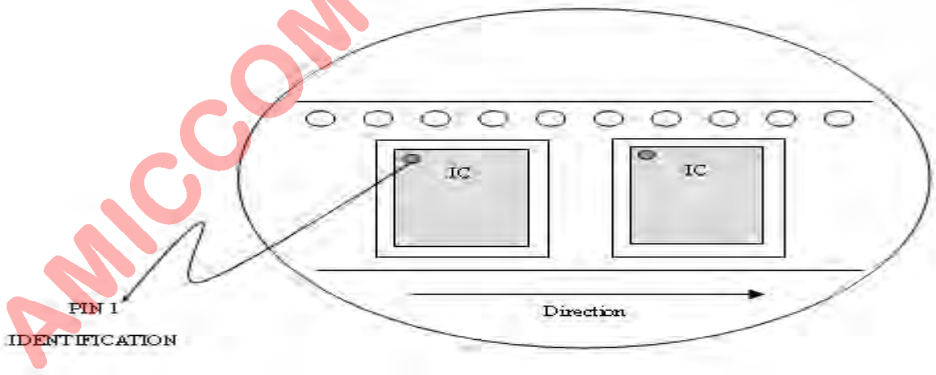
Cover / Carrier Tape Dimension



Unit: mm

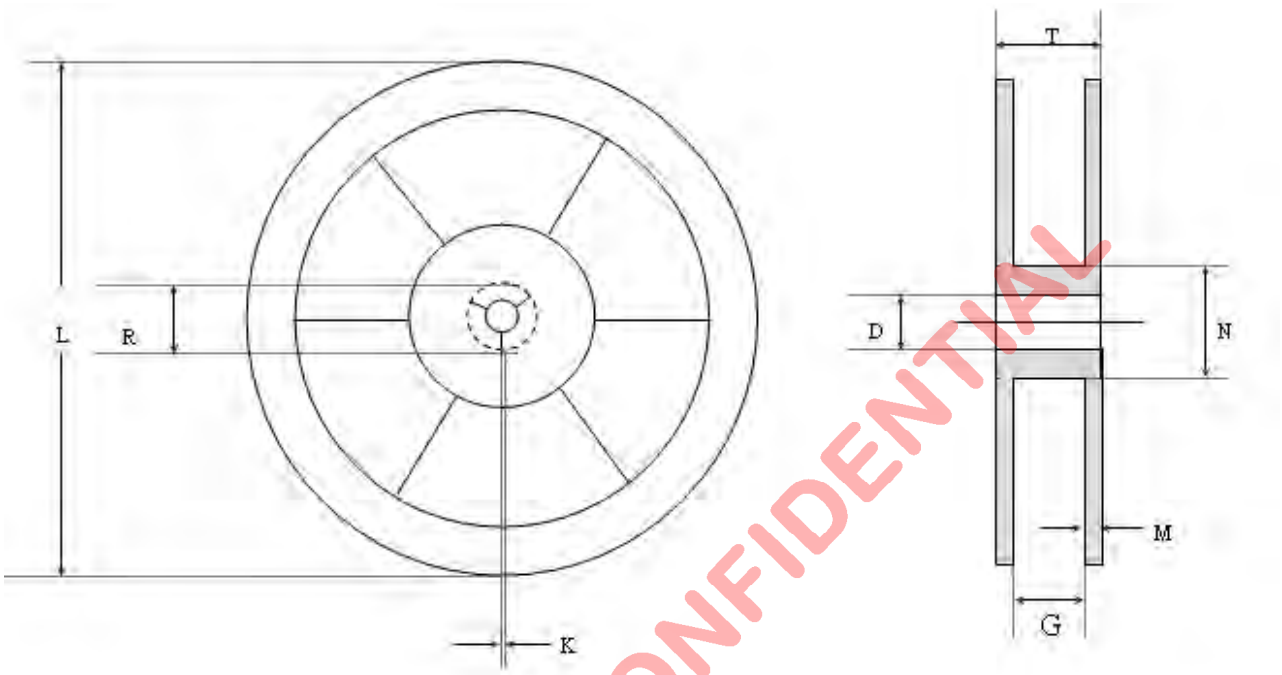
TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4*4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4*4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5*5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
QFN3*3 / DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16





TYPE	K0	t	COVER TAPE WIDTH
20 QFN (4X4)	1.1	0.3	9.2
24 QFN (4X4)	1.4	0.3	9.2
32 QFN (5X5)	1.1	0.3	9.2
QFN3*3 / DFN-10	0.75	0.25	8
20 SSOP	2.5	0.3	13.3
24 SSOP	2.1	0.3	13.3

REEL DIMENSIONS



Unit: mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) QFN(3X3) / DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330＋0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330＋0.00/-1.0	20.2

26. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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