Document Title

A7103A Data Sheet, 315MHz / 434MHz ASK Transceiver with 1~10Kbps data rate
, 315MHz / 434MHz FSK Transceiver with 1~20Kbps data rate

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial Issue	2007/7/19	
0.1	Modify specifications	2007/9/21	
0.2	Modify Logo and title	2007/10/5	
0.3	Modify register setting	2008/2/27	
0.4	Modify register setting for TX power control and Xtal start up time description	2008/3/28	
0.5	Add top marking info., reflow profile, Carry tape & reel dimensions. Add hardware control mode description	2008/9/14	
0.6	Modify ordering information	2008/11/4	
0.7	Add look-up-table of setting of TRx frequency. Add look-up-table in HW control and SPI control mode. Add look-up-table of frequency deviation in FSK modulation. Add RX sensitivity vs different IF BW filter. Add RX sensitivity at BER < 1E-2. Add Preamble format. Modify A7103B's IF BW = mid. in HW control mode. Rename Off mode to Shut-down mode. Remove constrain of Vdd = 3.3 V operation.	2009/01/14	
0.8	Separate A7103A / A7103B datasheet. Remove CKO pin / Remove CKO function. Remove programmable IF Filter, fix IFBW = mid only. Modify RC filters in front of VDD_A and VDD_D. ASK data rate 1K ~ 10Kbps, 2,2V ~ 3,0V operation range.	2010/Jan	
1.0	Add HW control mode schematic. Add Note 2 in Table 9.5.3 for FSK modulation.	2010/Nov.	Full Production
1.1	Update RF range of (310M ~ 318MHz)	2011/July	Full Production
1.2	Modify the tape reel information and add Shenzhen office address.	2011/July	Full Production

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Table of Content

1. General Description

A7103A is a very **easy-to-use** CMOS RF transceiver for sub 1GHz license free ISM band (315/434MHz). It is a FSK/ASK single chip RF transceiver with high sensitivity receiver (-110dBm @ 2.4Kbps, 433.92MHz ASK, -106dBm @ 2.4Kbps, 433.92MHz FSK) as well as 4-steps programmable power amplifier (max. 10dBm @ 315 / 434MHz). This device integrates a double balanced image reject mixer, low IF frequency (424KHz) architecture, IF filter, I/Q limiter with RSSI generation, as well as a fully VCO and PLL synthesizer. A7103A's carrier frequency F_{RF} is determined by the frequency of the reference Xtal F_{XTAL}. The integer-N PLL synthesizer ensures that each RF value, ranging from 310 MHz to 318 MHz and 420 MHz to 447 MHz with PLL steps of 848KHz, can be achieved. This is done by using a Xtal as a reference frequency according to: $F_{RF} = F_{XTAL} \times N / 2R$, where N is the PLL feedback divider ratio and R is Xtal divider to support 13.5732MHz crystal. Besides, A7103A supports AIF (Auto IF) function, user has no need to consider IF offset between TX and RX, but, use this formula ($F_{RF} = F_{XTAL} \times N / 2R$) directly to calculate radio frequency in both TX and RX site.

A7103A supports ASK data rate from 1K to 10Kbps and FSK from 1K to 20Kbps which is determined via external capacitors applied on data filter and data slicer. In FSK modulation, this device's Fdev (frequency deviation) is controlled by Xtal detuning of series an external capacitor (typical 75pF for ± 12.5KHz). However, this capacitor is not necessary in ASK modulation.

For **easy-to-use**, A7103A has only two control registers, register 0 and 1. MCU can configure two registers via 3-wire SPI bus. In addition to SPI control mode, A7103A has a special mode called **HW control mode**. In HW control mode, user just needs to apply pin settings. Then radio control is done (register 0 and register 1 are in default values). No matter HW or SPI control mode, A7103A is very easy to use by a low cost MCU or encoder/decoder. Those features are all integrated in a small SSOP 24 pins package.

For packet handling, there is no FIFO inside A7103A. Hence, in TX mode, MCU or Encoder just delivers the defined packet (preamble + sync word + payload) to TX_DATA pin. Then, in RX mode, MCU or Decoder can receive the packet (preamble + sync word + payload) from RX_DATA pin. Be aware that A7103A needs different preamble formats between ASK and FSK in order to get the best RX sensitivity.

2. Typical Applications

- Remote Control.
- Alarm and Security System.
- Smart Energy Management.
- AMR (Auto Meter Reading)
- Wireless Toys.
- RKE (Remote Keyless Entry).
- Garage Door Opener.
- Home Automation.

3. Features

- FSK Operating range: VDD=2,2~3,3V. T=-40~+85℃.
- ASK Operating range: VDD=2,2~3,0V. T=-40~+85℃.
- Easy to use
  - HW or 3-wire SPI control mode selection.
  - HW control mode (no need MCU for radio control, default max TX power).
  - Auto calibration.
  - Auto start-up sequence, Xtal→Auto Calibration→PLL→ RX / TX.
- TX current 18mA (FSK, 10dBm) / 11mA (ASK, 10dBm, 50% duty cycle).
- RX current 9mA (FSK and ASK).
- Shut down mode current 0,5 uA.
- Two stages PA in class-C, 4-steps programmable TX Power : 2 / 5 / 8 / 10 dBm.
- High ASK RX sensitivity down to – 110 dBm at BER<1E-3 (2.4Kbps, 433.92MHz).
- High FSK RX sensitivity down to – 106 dBm at BER<1E-3 (2.4Kbps, 433.92MHz).
- Customized digital I/O level (2,0 ~ 3,6V) by VIO pin.
- Fully integrated VCO, on chip loop filter and PLL synthesizer.
- Integrated IF Filter = mid. (250KHz in ASK, 150KHz in FSK).
- Tunable data filter via external capacitors depending on data rate.
- Tunable data slicer via an external capacitor depending on data rate.
- Direct ASK modulation by switching PA.
- Direct FSK modulation (frequency deviation) by Xtal detuning via external capacitor.
- Support low cost Xtal (13.5732MHz with ± 50ppm tolerance).

- Analog RSSI output.

4. Block Diagram

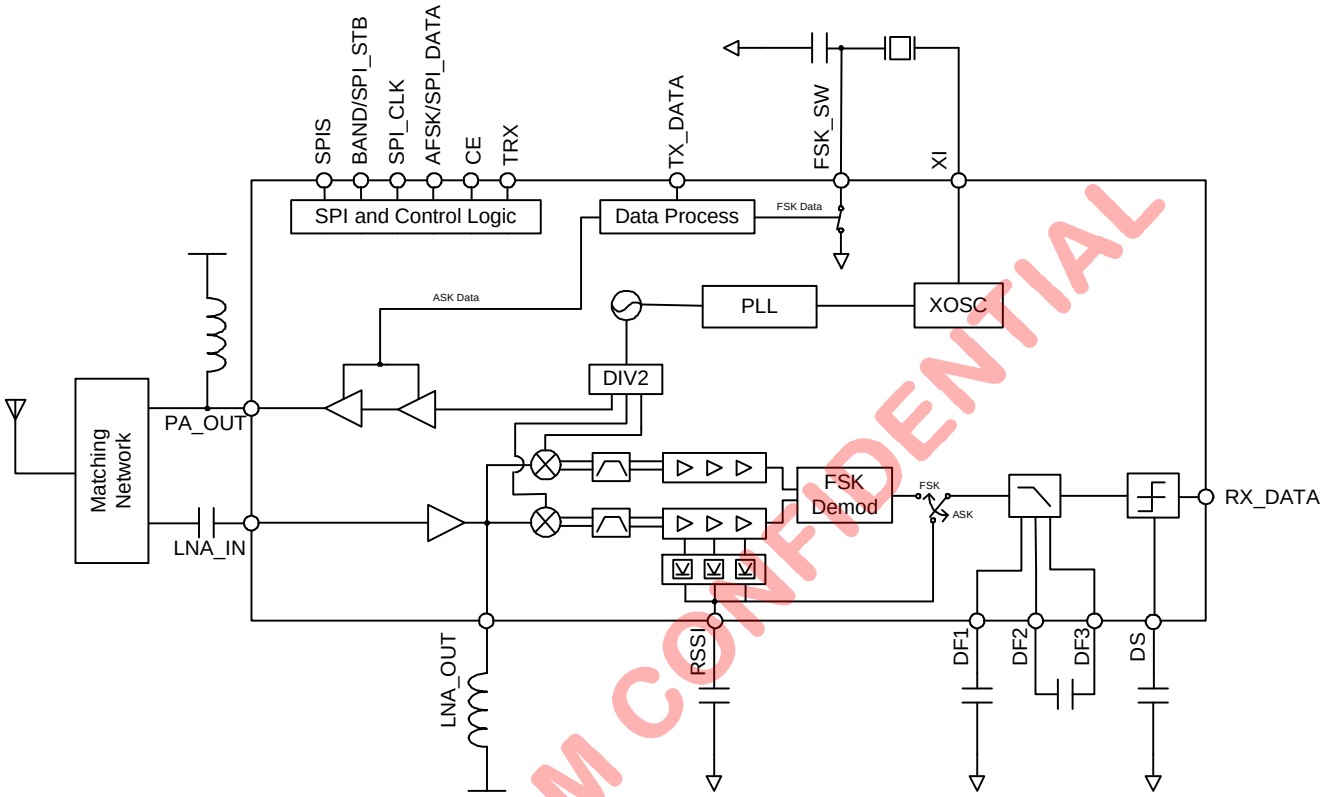
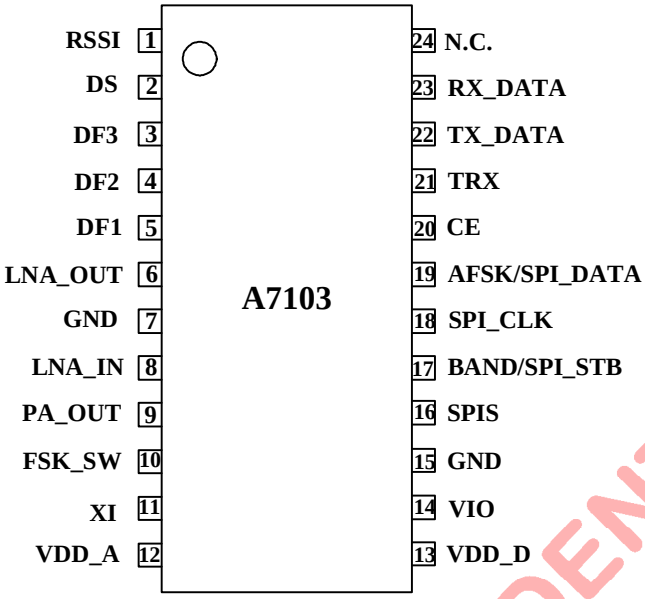


Fig 4 A7103A's Block Diagram

5. Pin Configuration



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6. Absolute Maximum Ratings

Characteristic	With respect to	Rating	Unit
Power supply voltage		-0.3~5	V
Input pin voltage		-0.3~5	V
Max input RF level		5	dBm
Storage temperature range	T_{stg}	-55~150	°C
ESD Rating	HBM *	± 2K	V
	MM *	± 100	V

*Pin 9 (PA_OUT) is -2KV and -100V of HBM and MM respectively.

*Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).

7. Pin Description

Pin No.	Pin Name	Description
1	RSSI	Analog RSSI output. Connect a capacitor to GND.
2	DS	Data slicer by pass. Capacitor value depending to data rate.
3	DF3	Data filter capacitors. Capacitor values depending to data rate.
4	DF2	
5	DF1	
6	LNA_OUT	LNA output matching.
7	GND	Connect to PCB ground.
8	LNA_IN	RX LNA input matching.
9	PA_OUT	TX power amplifier output.
10	FSK_SW	FSK deviation setting. Capacitor value determines the Freq. deviation.
11	XI	Xtal oscillator input. (Recommend Xtal **Cload = 16pF**)
12	VDD_A	Analog power input. (**Need low pass RC filter on this pin**.)
13	VDD_D	Digital power input. (**Need low pass RC filter on this pin**.)
14	VIO	I/O voltage level Assignment, Range 2.0~3.6V, (**Need low pass RC filter on this pin**.)
15	GND	Connect to PCB ground.
16	SPIS	Control Mode selection. Low→ HW control mode (Use Pin 17 / 19 /20 / 21 to do radio control.) High→ SPI control mode.
17	BAND	HW control mode only. Low→315MHz, High→ 434MHz.
	SPI_STB	SPI control mode (Strobe).
18	SPI_CLK	SPI clock (Must be Low in HW control mode).
19	AFSK	HW control mode only. Low → FSK. High →ASK.
	SPI_DATA	SPI control mode (data input)
20	CE	HW control mode, Low→Shut down mode. High→Active mode. SPI control mode, Refer to Register 1, bit D4.
21	TRX	HW control mode. Low→RX. High→TX. SPI control mode, Refer to Register 1 bit D3.
22	TX_DATA	TX data input.
23	RX_DATA	RX data output.
24	Reserved	NC. (Shall be **open** for normal operation.)

8. Specification

General Test Conditions: Ta = 25°C, VDD=2.5V, Crystal=13.5732MHz, IFB[1:0]=mid, with matching network, PN9 pattern

Parameter		Description		Min.	Typ.	Max.	Unit
General							
Operating temperature				-40		85	°C
Supply voltage		ASK		2.2	2.5	3.0	V
		FSK		2.2	2.5	3.3	V
Current consumption		Shut down mode (all circuit off)		0.1	0.5		uA
		RX mode			9		mA
		TX mode (FSK, 10dBm)			18		
		TX mode (ASK, 10dBm, 50 % duty cycle)			11		
RF Frequency Range		848KHz PLL step			310 ~ 318 420 ~ 447		MHz
Xtal Frequency (F_{XTAL})		Recommend Cload = 16pF[1].			**13.5732** **13.56**		MHz
Xtal Series Resistance (ESR)		Cload =16pF.				60	ohm
Xtal Tolerance		IFB[1:0] = 10 (mid.)			+/-50		ppm
Xtal settling time		with Xtal compensated capacitor, Ccomp. = 10pF when Xtal Cload=20pF.			4.5		ms
		without Ccomp			1		ms
TX settling time		Xtal stable to TX ready			0.3		ms
RX settling time		Xtal stable to RX ready			3		ms
Data Rate		ASK		1		10	Kbps
		FSK		1		20	Kbps
TX							
Max Output Power		315MHz, VDD=2.5V			10		dBm
		434MHz, VDD=2.5V			10		
Output Power Control Range					8		dB
Phase Noise		Offset=100KHz			-95		dBc/Hz
		Offset=1MHz			-105		
Spurious Emission[2]		f < 1GHz (RBW =100kHz)				-36	dBm
		47MHz< f <74MHz 87.5MHz< f <118MHz 174MHz< f <230MHz 470MHz< f <862MHz (RBW =100kHz)				-54	dBm
		Above 1GHz (RBW = 1MHz)				-30	
RX							
IF frequency		Xtal frequency =13.5732 / 13.56MHz			424		KHz
		Xtal frequency =12 / 16MHz			400		
IF Bandwidth		FSK	IFB[1:0]=10 (Mid)		150		KHz
		ASK	IFB[1:0]=10 (Mid)		250		
315 MHz Sensitivity (BER<1E-3)	2.4Kbps	FSK (Fdev = 12.5KHz)	IFB[1:0]=10 (Mid)		-106		dBm
	2.4Kbps	ASK	IFB[1:0]=10 (Mid)		-110		dBm
	20Kbps	FSK (Fdev = 12.5KHz)	IFB[1:0]=10 (Mid)		-106		dBm

	10Kbps	ASK	IFB[1:0]=10 (Mid)		-110		dBm
433.92 MHz Sensitivity(3) (BER<1E-3)	2.4Kbps	FSK (Fdev = 12.5KHz)	IFB[1:0]=10 (Mid)		-106		dBm
	2.4Kbps	ASK	IFB[1:0]=10 (Mid)		-110		dBm
	20Kbps	FSK (Fdev = 12.5KHz)	IFB[1:0]=10 (Mid)		-106		dBm
	10Kbps	ASK	IFB[1:0]=10 (Mid)		-110		dBm
Max operation input power (BER<1E-3)		ASK	TX source On-Off ratio = 40dB		-25		dBm
			TX source On-Off ratio = 60dB		-15		
			TX source On-Off ratio = 90dB		-5		
		FSK			+5		
RSSI		Dynamic range			70		dB
		Lower level			-115		dBm
		Upper level			-45		dBm
Spurious Emission		25MHz ~ 1GHz				-57	dBm
		Above 1GHz				-47	
Image rejection					20		dB
Interference blocking(4)		+/- 0.4MHz			30		dBc
		+/- 1.5MHz			50		
		+/- 3MHz			45		
		+/- 13MHz			40		
		+/- 20MHz			50		

(1) To get a very accurate carrier frequency, Cload of the Xtal maybe change with different layout and PCB thickness
(2) Pin 12 / 13 / 14 are critical paths to get good spurious emission. Use suitable RC filters on those pins for noiseless power supply is very important. A RC filter also shall be added on Pin 22 for PA data shaping
(3) Please refer to section 9.8 for sensitivity vs Vdd.
(4) Set wanted signal to be 3 dBm above of sensitivity level to get the carrier / interference ration.

9. Circuit Description

A7103A supports SPI and HW control mode by setting SPIS pin. If SPIS = 0, A7103A is in HW control mode by pin setting for radio control. If SPIS = 1, A7103A is in SPI mode (program Register 0 and Register 1). CE pin is recommended to be controlled by MCU. When CE pin goes from low to high, A7103A is enabled from shut down mode to active mode via auto calibration.

For RX part, A7103A features a low-IF architecture with high receiving sensitivity. The received signal is via LNA to down-converted mixer to the IF (intermediate frequency) circuitry. Signal is RF-IN and Digital-Out to RX_DATA pin.

For TX part, signal is Digital-IN to RF-Out from TX_DATA pin to PA_OUT pin. In ASK modulation, data input modulates PA switching directly and therefore leads to an ASK signal. In FSK modulation, frequency deviation is determined by Xtal detuning via external capacitor and therefore leads to an FSK signal.

9.1 Functional Block

A7103A is an integer-N PLL synthesizer via feedback mechanism N-counter (Na + Nb). The VCO frequency is generated as a integer multiple of Phase Detect comparison frequency (848KHz) which is dividing by R-counter (16) from Xtal (13.5732MHz).The phase detector tunes the VCO in the locked state at wanted frequency $F_{VCO} = F_{RF}$ **x 2.** See figure 9.1 for details.

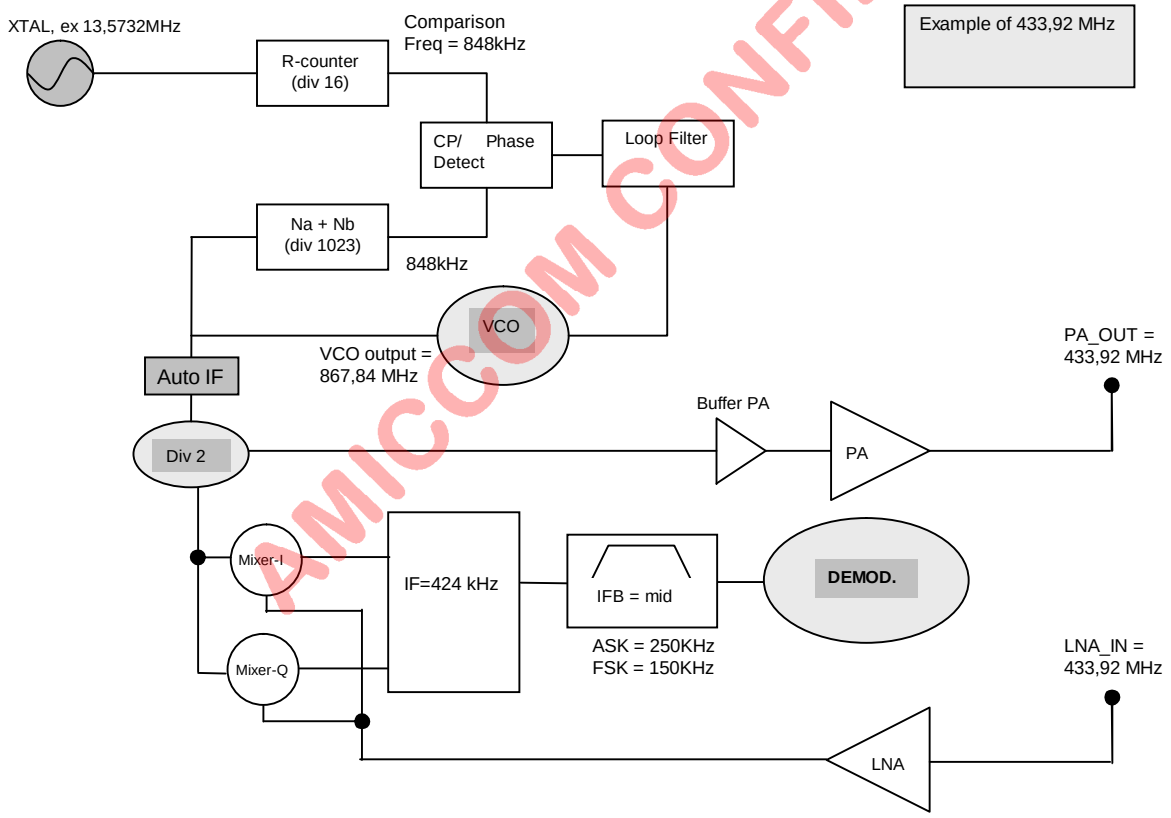


Figure 9.1.1 VCO Topology.

9.2 Data Filter and Data Slicer

Figure 9.2.1 shows A7103A's DEMOD block diagram. The data filter architecture is Butterworth Multiple feedback. Its bandwidth is adjustable via external data filter capacitors for different data rate operation. A7103A's data slicer is also adjustable to act like a data comparator to convert analog-to-digital to RX_DATA pin.

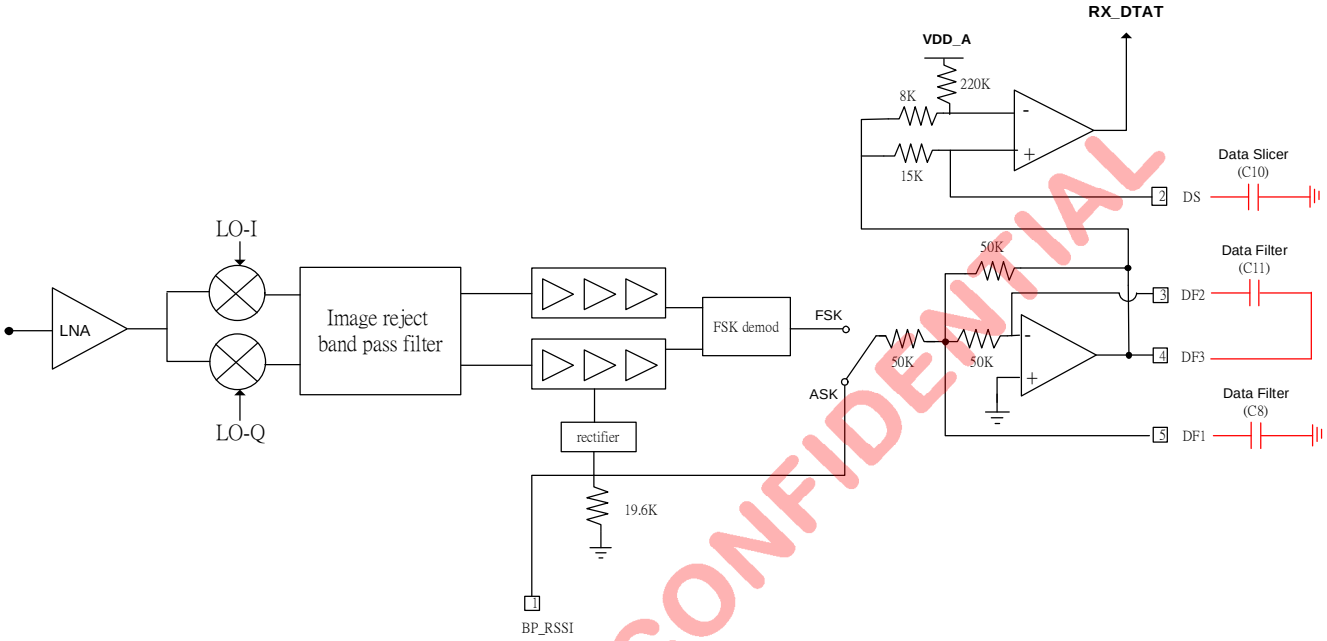


Figure 9.2.1 DEMOD Topology.

C10, C11 and C8 can be adjusted in different data rate operation in order to obtain the best receiving sensitivity where Table 9.2.1 shows recommended values. Due to different PCB design, user can fine tune C10, C11 and C8 to gain the best RX sensitivity.

Data Rate (Kbps)	Data Filter (C8)	Data Filter (C11)	Data Slicer (C10)
1,2	8,2 nF	1,5 nF	4,7 uF
2,4	3,9 nF	820 pF	2,2 uF
4,8	1 nF	220 pF	1 uF
9,6	560 pF	120 pF	0,47 uF
20	270 pF	56 pF	0,22 uF

Table 9.2.1 Recommended value for data filter and data slicer capacitors

9.3 HW Control Mode

Set SPIS pin = 0 for HW control mode, MCU has no extra efforts to do radio control but only needs to control CE and TRX pin. Table 9.3.1 shows how to do pin settings for radio control. If so, A7103A is set at default values (max TX power, IFB = mid, AGC is enabled). Hence, MCU just needs to deliver TX data to TX_DATA pin as well as decode received data via RX_DATA pin. For different wanted frequency allocations, refer to Table 9.3.2 for Xtal selection.

HW Pin Setting								
Pin 23 RX_DATA	**Pin 22 TX_DATA**	**Pin 20 CE**	**Pin 21 TRX**	**Pin 19 AFSK**	**Pin 18 SPI_CLK**	**Pin 17 BAND**	**Pin 16 SPIS**	**Pin 14 VIO**
		Shut down = 0	TX = 1	ASK = 1	Must be 0	315M = 0	Must be 0	Note 1
		Active = 1	RX = 0	FSK = 0		434M = 1		

Note1 Digital I/O level assignment (2.0 ~ 3.6V).

Table 9.3.1 Pin setting in HW control mode.

Band 315MHz			Band 434MHz		
Xtal (MHz)	**Pin 17**	**F_{RF} (MHz)**	**Xtal (MHz)**	**Pin 17**	**F_{RF} (MHz)**
13.0498	0	303	13.2785	1	424.5
13.064	0	303.33	13.3337	1	426.2625
13.0853	0	303.825	13.3407	1	426.4875
13.0875	0	303.875	13.3517	1	426.8375
13.1036	0	304.25	13.4663	1	430.5
13.1144	0	304.5	13.5445	1	433
13.2866	0	308.5	13.5288	1	432.5
13.3513	0	310	13.542	1	432.92
13.3943	0	311	13.546	1	433.05
13.397	0	311.062	13.5576	1	433.42
13.502	0	313.5	13.56	1	433.496
13.5235	0	314	13.5717	1	433.87
13.545	0	314.5	13.5732	1	433.92
13.56	0	314.846	13.5804	1	434.15
13.5666	0	315	13.5889	1	434.42
13.5732	0	315.1527	13.8181	1	441.75
13.5752	0	315.2			
13.5881	0	315.5			
13.6097	0	316			
13.6442	0	316.8			
13.6958	0	318			
$F_{RF} = F_{XTAL}$ x 743 / 32			**$F_{RF} = F_{XTAL}$ x 1023 / 32**		

Table 9.3.2 Xtal selection guide in HW control mode

Default setting in HW Mode	
TX Power	Max (typical 10 dBm)
IFB [1:0]	[10] (mid)
AGC	Enable

Table 9.3.3 Default settings in HW control mode.

9.4 SPI Control Mode

Set SPIS = 1 for SPI control mode, MCU is very easy to do radio control via 3-wire SPI because A7103A has only two 16-bit-write-only registers (Register 0 and Register 1). Then, MCU can control the device's features to meet system requirements instead of using its default settings. Please note, bit sequence is 16 bits from D0 to D15 (LSB first, D0 and D1 are address bit), but it is not a standard SPI for data bits.

For Register 0, it is used to define R counter and N counter. R counter supports 3 Xtal options by 12/13.5732/16MHz. N counter is separated into NA and NB to support wanted F_{RF} in every 848KHz step. Refer to section 9.4.2 for details.

For Register 1, it is used to set AGC, TX output power, IF BW, FSK, ASK as well as Band Selection. Refer to section 9.4.3 for details.

SPI Pin Setting								
Pin 23 RX_DATA	**Pin 22 TX_DATA**	**Pin 20 CE**	**Pin 21 TRX**	**Pin 19 SPI_DATA**	**Pin 18 SPI_CLK**	**Pin 17 SPI_STB**	**Pin 16 SPIS**	**Pin 14 VIO**
		See Register 1-D2	See Register 1-D2	3-wire SPI			Must be 1	Note 1

Note1 Digital I/O level assignment (2.0 ~ 3.6V).

Table 9.4.1 Pin setting in SPI control mode.

9.4.1 SPI timing

A7103A is very easy-to-use, only two steps to do radio control.

Step 1: Set wanted RF frequency by Register 0.
Step 2: Set features by Register 1.

Register 0 and 1 are both write-only. A7103A supports maximum 4Mbps SPI baud rate. To active SPI interface, SPI_STB pin must be set to high. To latch correct data, hold time and setup time between SPI_CLK and SPI_DATA must be satisfied. SPI_DATA is latched into the device at the rising edge of SPI_CLK. See below table for SPI timing characteristic.

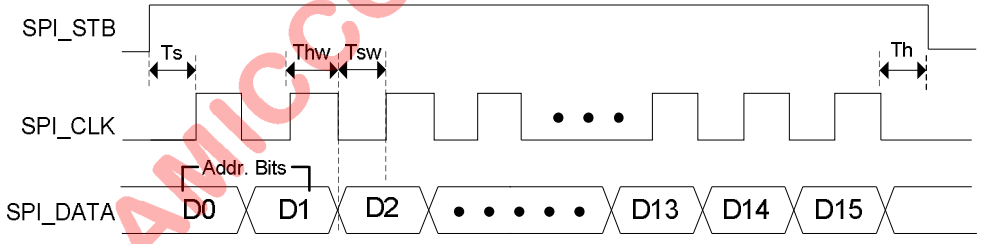


Fig 9.4.1.1 SPI timing chart

Parameter	Description	Min	Max	Unit
Fc	SPI Clock Frequency		4	MHz
Ts	SPI_STB Setup Time	50		ns
Thw	SPI_DATA Hold Time	50		ns
Tsw	SPI_DATA Setup Time	50		ns
Th	SPI_STB Hold Time	50		ns

Table 9.4.1.1 SPI timing characteristic

9.4.2 Register 0 (Address: 11)

Name	Write-only	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register 0		R1	R0	NB7	NB6	NB5	NB4	NB3	NB2	NB1	NB0	NA3	NA2	NA1	NA0	1	1
Reset value		1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1

← Write in direction (from D0 to D15, LSB first).

D1 and D0: Address bit. Register 0 = [11], Other settings are forbidden.

R[1:0]: Xtal reference frequency.

R [1:0]	Xtal (MHz)	R counter	Note
11	Reserved	Reserved	
10	12	15	PLL ref. freq = 800KHz, PLL step = RF step = 800KHz
01	13.5732 /13.56	16	PLL ref. freq = 848KHz, PLL step = RF step = 848KHz
00	16	20	PLL ref. freq = 800KHz, PLL step = RF step = 800KHz

NB, NA: Used to define wanted F_{RF} of PLL (see below table).

NA[3:0]: NA is odd (1 / 3 / 5 / 7) and complement.

NB[7:0]: NB is (5 ~ 40) and complement.

Formula	Example of 433.92 MHz	
N = 16NB + NA $F_{RF} = F_{XTAL}$ x N / 2R	NA = 15 = [1111b]	NA 1's complement = [0000b]
	NB = 63 = [0011-1111b]	NB 1's complement = [1100-0000b]
	N = 16 x 63 + 15 = 1023	
	R = 16 (F_{XTAL} =13.5732MHz)	
	F_{RF} = 13.5732 x 1023 / 2 / 16	F_{RF} = 433.92 MHz

Band 315MHz			Band 434MHz		
NA	NB	Example	NA	NB	Example
1	43	F_{RF} = 13.56 x (743) / 2 / 16 = 314.84 MHz	1	62	F_{RF} = 13.5732 x (1023) / 2 / 16 = 433.92 MHz
3	44		3	**63**	
5	45		5	64	
7	**46**		7	65	
9	47		9	66	
11			11		
13			13		
15			**15**		

9.4.3 Register 1 (Address: 01)

Name	Write-only	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register 1		EAGC	TXP1	TXP0	ULS	CKS	ECK	X	IFB1	IFB0	BANDb	FASK	CEb	RTX	CTLS	0	1
Reset value		0	1	1	1	0	1	1	1	0	1	1	1	1	1	0	1

← Write in direction (from D0 to D15, LSB first).

D1 and D0: Address bit. Register 0 = [01], Other settings are forbidden.

EAGC: Auto gain control (AGC) selection
[0]: Enable (default).
[1]: Disable.

TXP: TX output power control.
[11]: max. **[10]:** high. **[01]:** mid. **[00]:** min.

TXP [1:0]	TX power level	Band 315MHz (Typical)	Band 434MHz (Typical)
11	Max.	10 dBm	10 dBm
10	High	8 dBm	8 dBm
01	Mid.	5 dBm	5 dBm
00	Min.	2 dBm	2 dBm

ULS: ULS: RX Up/Low side band select. Shall be set to [1].

CKS: Reserved. Shall be set to [0].

ECK: Reserved. Shall be set to [1].

X: Crystal. Shall be set to [1].

IFB[1:0]: IF filter bandwidth selection.
[10]: mid. (ASK = 250KHz, FSK = 150KHz)

BANDb: RF band selection.
[0]: 434MHz.
[1]: 315MHz (default).

FASK: FSK ASK Select.
[0]: ASK.
[1]: FSK (default).

CEb: Chip Enable
[0]: Active mode.
[1]: Shut down mode (default).

RTX: RTX selection
[0]: TX mode.
[1]: RX mode (default).

CTLS: Control Mechanism Select.
[0]: CE control by Register D4 (CEb) and TRX by Register D3 (RTX), if so, pin 20 and pin 21 shall be tied to GND.
[1]: CE control by pin 20 and TRX control by pin 21 (default).

9.5 Start-up Sequence

CE pin is used to set A7103A from shut down mode to active mode, when CE > 1V , A7103A executes Xtal start-up and auto calibration. That means, VDD shall be stable (> 90% max VDD) before let CE go higher than 1V for successful calibration. Otherwise, VCO may not operate at properly frequency. For certain applications, if CE is connected to VDD directly, an extra RC delay at CE pin is necessary for proper start up sequence as shown below.

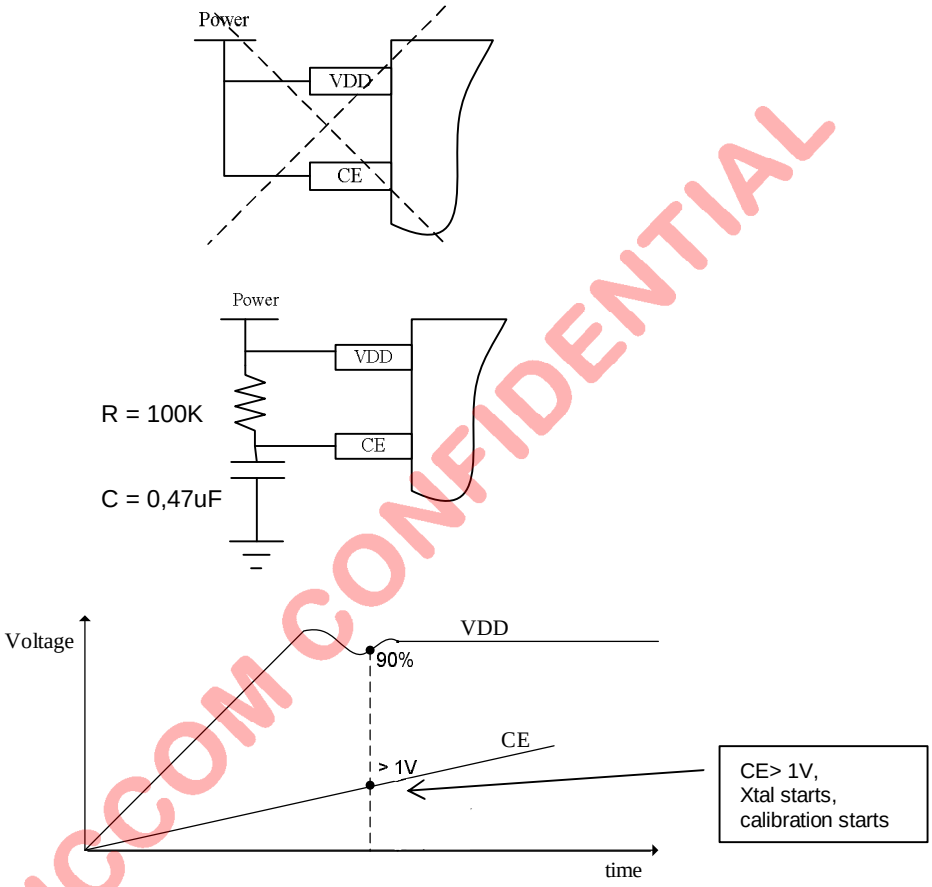
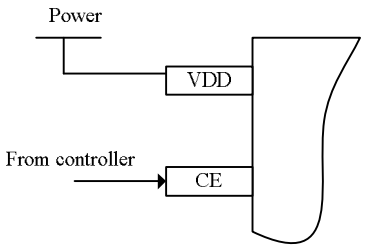


Fig 9.5.1. An extra RC delay on CE pin for correct start up sequence.

Hence, CE pin is recommended to be enabled by MCU. If so, RC delay on CE pin is not necessary, but, MCU shall also let CE pin go HIGH after VDD is stable (> 90% max VDD) as shown below.



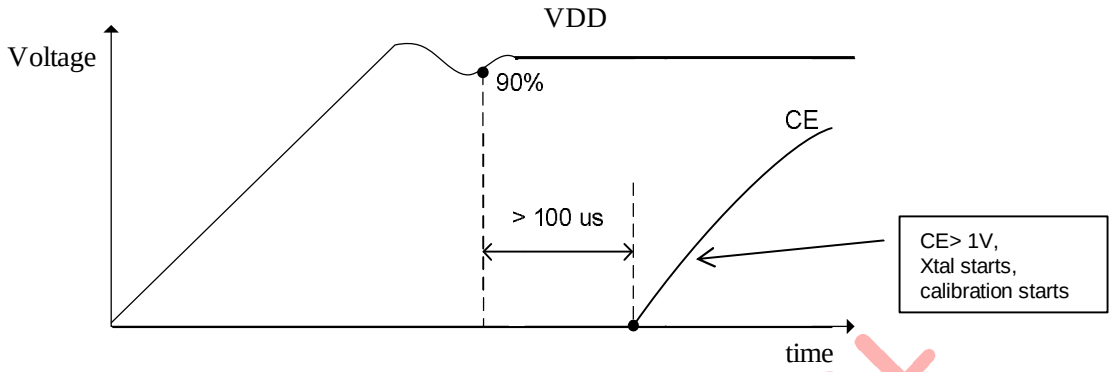


Fig 9.5.2. CE pin is controlled by MCU for a correct start up sequence.

When CE > 1V, Xtal oscillator and calibration procedure are active, in this device, RX settling time is longer than TX settling time. Figure 9.5.3 and Figure 9.5.4 illustrates A7103A's settling time when Ccomp is NC (Not Connected). If Ccomp is added, Xtal settling time becomes longer from 1ms to 4.5ms. See Table 9.5.1 for details.

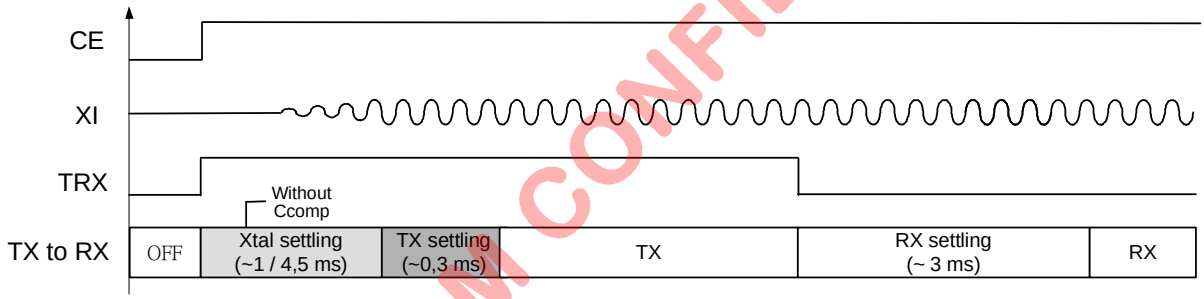


Fig 9.5.3 Settling time from shut down mode to TX mode.

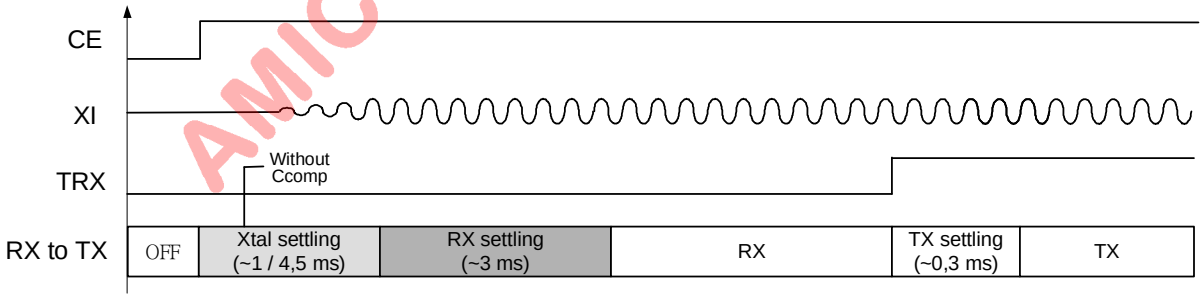
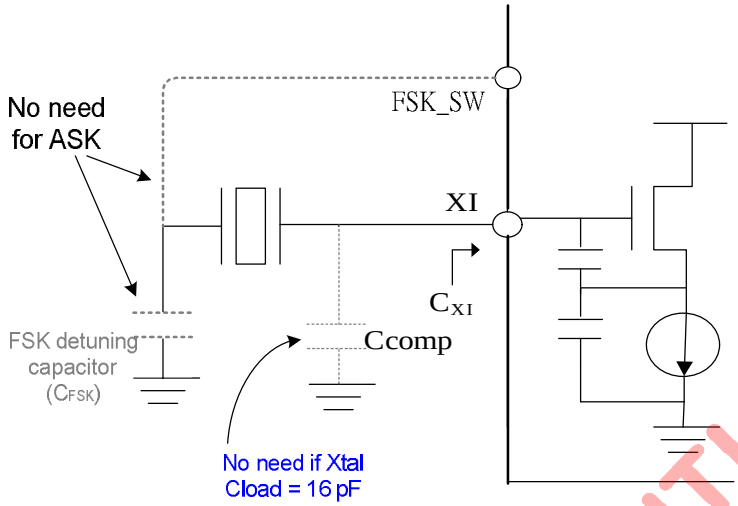


Fig 9.5.4 Settling time from shut down mode to RX mode.

A7103A's Xtal oscillator is Colpitts type with integrated feedback capacitors as shown in Figure 9.5.5. The input capacitance C_{XI} from XI pin is about 14 pF ~ 16 pF. Therefore, it is recommended to use a Xtal with 16 pF Cload because Xtal settling time is short. If Xtal Cload is larger than 16 pF, an external Ccomp shall be added at XI pin. Then, Xtal settling time becomes longer. Another case to add Ccomp is to fine tune $\mathbf{F_{RF}}$ for a proper frequency even though Xtal Cload =16 pF. Refer to Figure 9.5.5 and Table 9.5.1 for details.



Xtal Cload = 16pF may be slight changed under different PCB layout and PCB thickness.

Figure 9.5.5 Schematic of Xtal oscillator.

Settling Time (Typical)		
Xtal settling	without Ccomp	1 ms
	with Ccomp = 10pF when Xtal Cload = 20 pF	4.5 ms
TX settling time		0.3 ms
RX settling time		3 ms

Table 9.5.1 Typical settling time

Recommend Quartz Xtal Specification	
Center Frequency	13.5732MHz
Load Capacitance (Cload)	16 pF
Equivalent Series Resistance (ESR)	=<60 ohms
Shunt Capacitance (C0)	=<5pF
Stability	± 50 ppm

Table 9.5.2 Recommend Xtal spec

From Figure 9.5.5, A7103A's frequency deviation of FSK is defined by applying external capacitors (C_{FSK}) on FSK_SW pin. Fig. 9.5.6 is the equivalent circuit of detuning Xtal when TX_DATA=1 and TX_DATA = 0 respectively. Table 9.5.3 is a recommended C_{FSK} for ± 12,5KHz frequency deviation which is suitable for FSK data rate from 1K to 20Kbps.

Recommend C_{FSK}	Fdev	Note
75 pF	± 12,5KHz	1. Suitable for FSK data rate from 1K ~ 20Kbps 2. Recommend C_{comp} = 3pF in FSK, otherwise, C_{FSK} shall be away from TX path to avoid interference from TX signal, especially when TX power is larger than 5dBm.

Table 9.5.3 Recommend Fdev in FSK

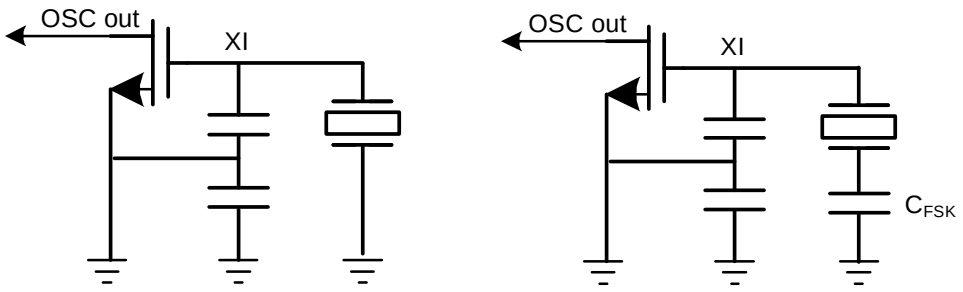


Figure 9.5.6 Equivalent circuit of Xtal oscillator during FSK modulation.

9.6 Preamble Format

A7103A needs the different preamble format between ASK and FSK for the best RX sensitivity. In ASK modulation, the lower data rate, A7103A needs the longer preamble to charge internal DC estimation circuit to make it. Figure 9.6.1 is an example of a packet and Table 9.6.1 gives an example of preamble format for ASK and FSK modulation.

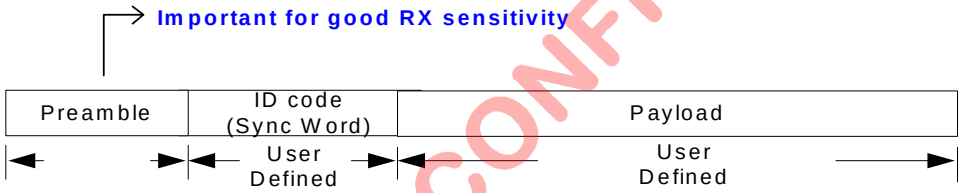


Figure 9.6.1 Packet Format

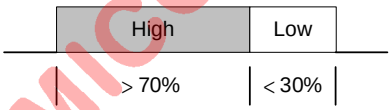
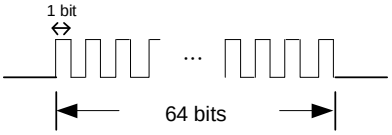
	ASK	FSK
Preamble Format	 Long high period + Short low period	 64 bits of alternate 0 and 1.
Data rate	9,6Kbps, High = 2,8 ms, Low = 1,2 ms 4,8Kbps, High = 2,8 ms, Low = 1,2 ms 2,4Kbps, High = 5,6 ms, Low = 2,4 ms	1K ~ 20Kbps

Table 9.6.1 Preamble Format

ID code (Sync Word):
If ID code (sync word) is used in a wireless system, its length is recommended to set 2~4 bytes by user definition.

Payload:
Payload is a carrier-information by user definition. Please noted, in ASK modulation, Do NOT apply data pattern in continuous low for over 40 ms. Otherwise, AGC circuit will operate abnormal.

9.7 RSSI

A7103A supports analog RSSI output on RSSI pin. The voltage is inverse proportional to the RF input power. The usable dynamic range is about -45 ~ -115 dBm. Due to AGC function, its transition point of RSSI is designed at – 70 dBm RF input power. Fig 9.7.1 shows a typical RSSI curve at 434MHz.

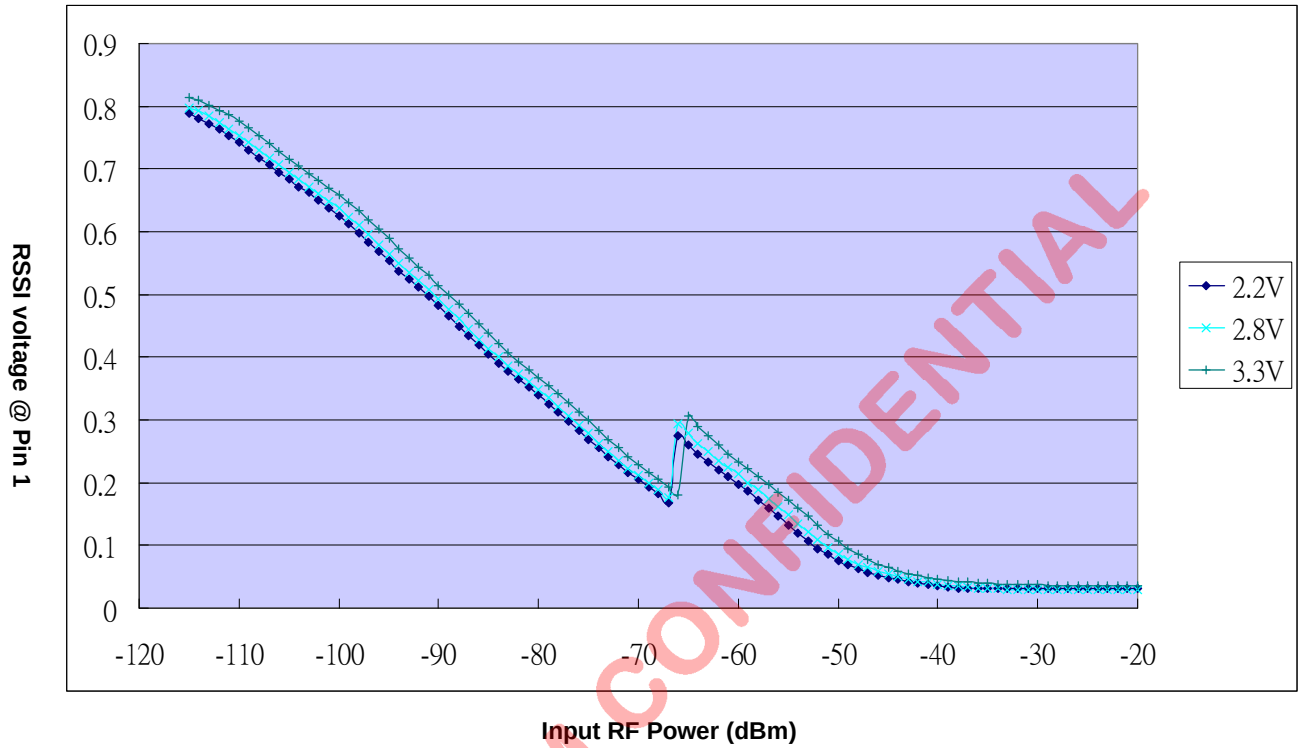


Figure 9.7.1 Typical RSSI curve at 434MHz

9.8 RX_DATA Duty Cycle and Sensitivity

In ASK modulation, the received data streaming is passing via RX_DATA pin to MCU or Decoder. Due to the internal mechanism, received data pattern, i.e. 01010101, may not be exactly 50/50 duty cycle. Table 9.8.1 shows the duty cycle of received data patterns (01010101...) is slightly related to the signal strength and data rate.

DataRate / TX Input(dBm)	5Kbps	10Kbps
-100	52/48	54/46
-90	52/48	52/48
-80	52/48	53/47
-70	52/48	53/47
-60	52/48	55/45
-50	52/48	55/45
-40	53/47	55/45
-30	54/46	56/44

Table 9.8.1 ASK duty cycle variation when VDD = 2,8V

Due to wide supply voltage range of this device, for RX sensitivity, BER performance is depending on supply voltage. BER test is measured by PN9 pattern with BER = 0.1% criteria. Below figures are FSK / ASK sensitivity at 433.92 MHz, 2,4Kbps respectively.

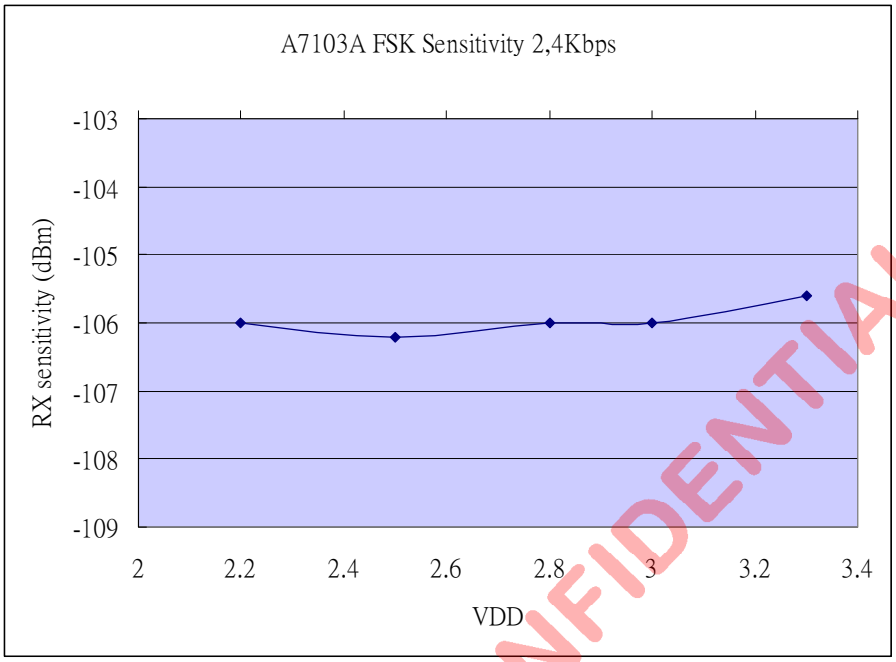


Figure 9.8.1 FSK Sensitivity @ 433.92MHz 2,4Kbps

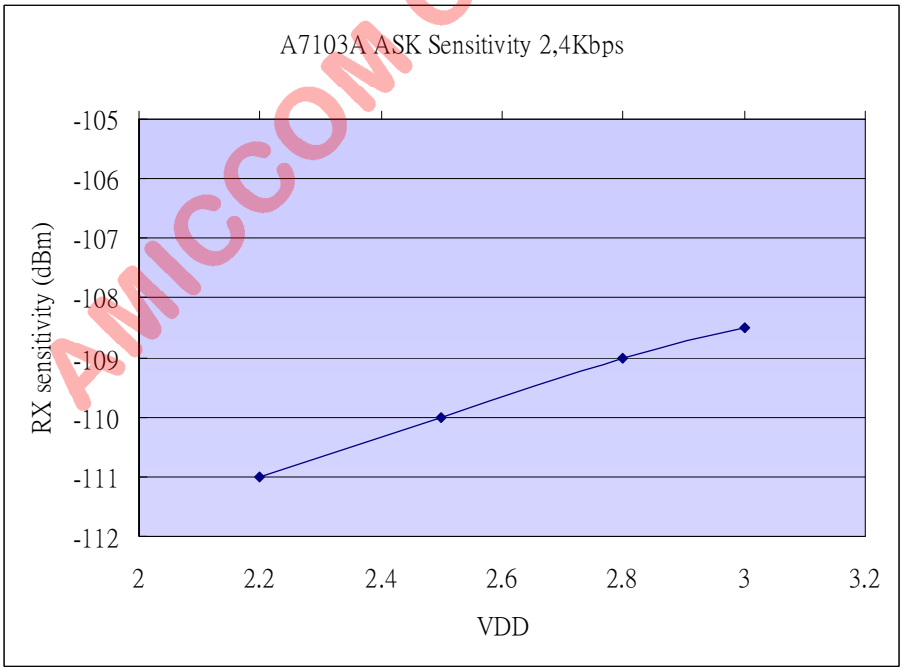


Figure 9.8.2 ASK Sensitivity @ 433.92MHz 2,4Kbps

9.9 TX Data Shaping

For minimizing TX transient power as well as occupied bandwidth, A7103A has built-in TX data shaping circuit as illustrated in Figure 9.9.1. Therefore, user has no need to add external RC data shaping on TX_DATA pin. TX modulated spectrum in ASK and FSK are shown in Figure 9.9.2 respectively.

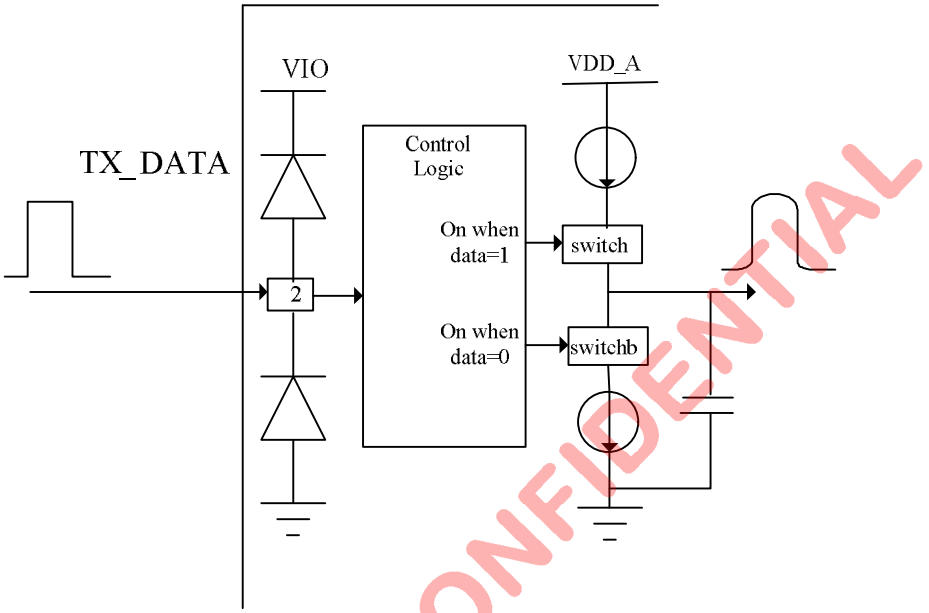
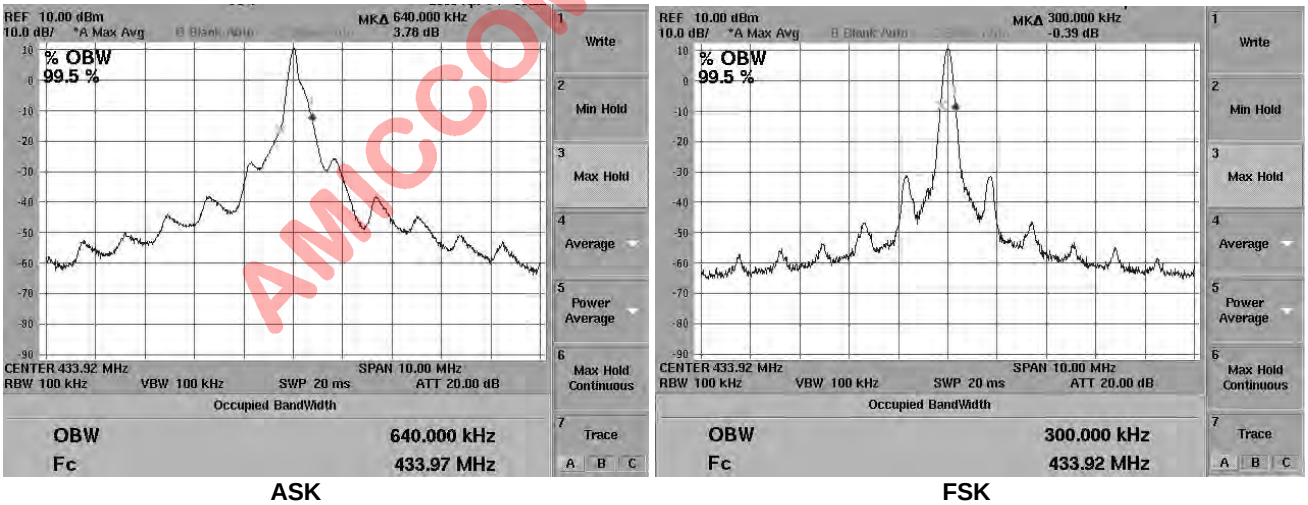


Figure 9.9.1 RC data shaping at TX_DATA pin `



ASK **FSK**

Figure 9.9.2 TX Spectrum (Spectrum Analyzer, RBW=VBW=100KHz, SPAN 10MHz)

9.10 TX Spurious Emission

Noisy VDD is a critical issue to induce A7103A a bad TX spurious emission. Inside A7103A, analog circuitry is powered by VDD_A pin and digital circuitry is powered by VDD_D pin. Please note to add low pass RC filter in front of VDD_A, VDD_D and VIO pin as shown below. For PA and LNA power supply, connect to VDD_A pin instead of VDD_D pin and use a suitable RC filter in front of VDD_D to isolate VDD noise while PA is switching. Hence, VDD RC filters lead a good result of TX spurious emission. Figure 9.10.1 illustrates R and C values used in AMICCOM's reference design. For different PCB design, R and C may be fine tuned to get optimized performance.

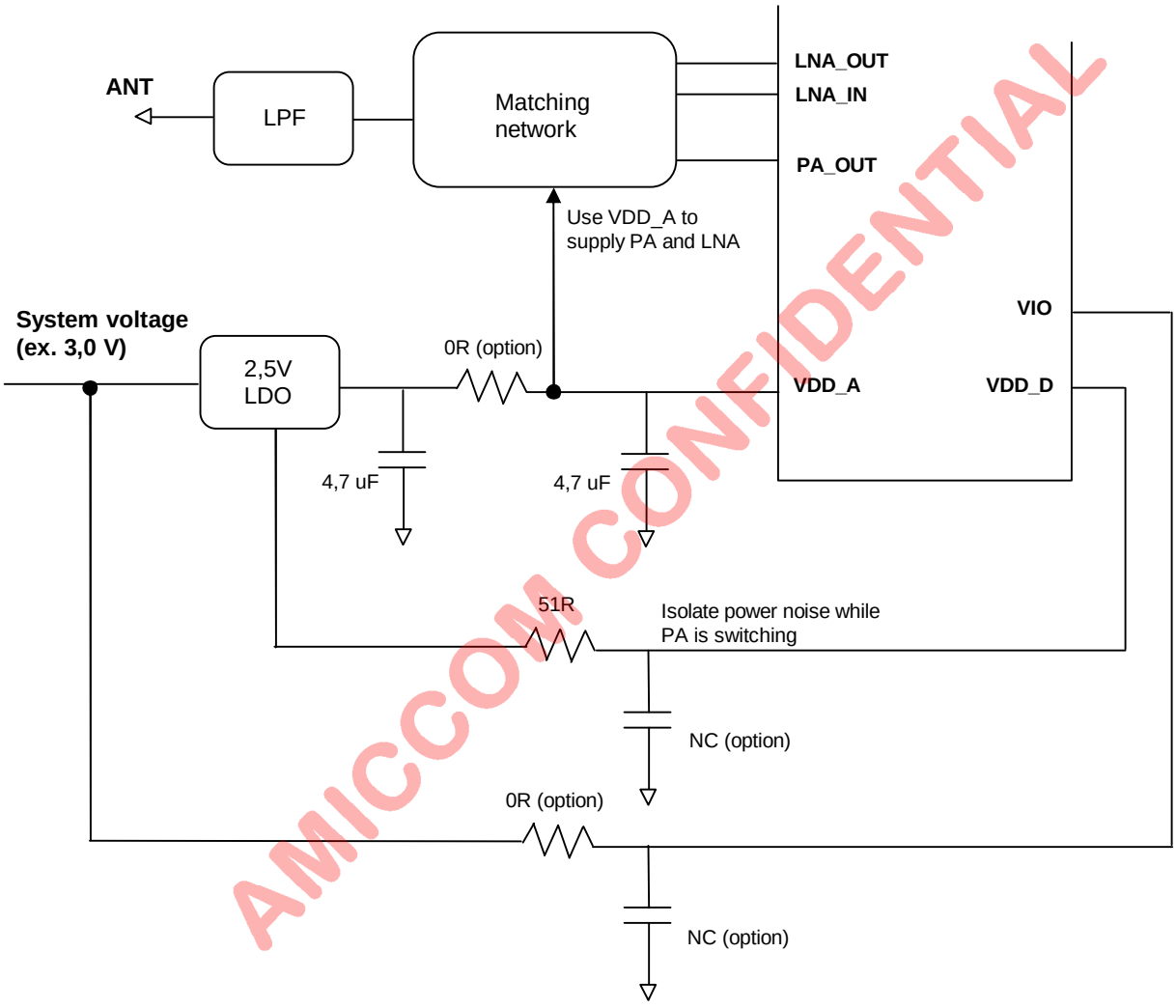


Figure 9.10.1 RC low pass filters on VDD_A, VDD_D

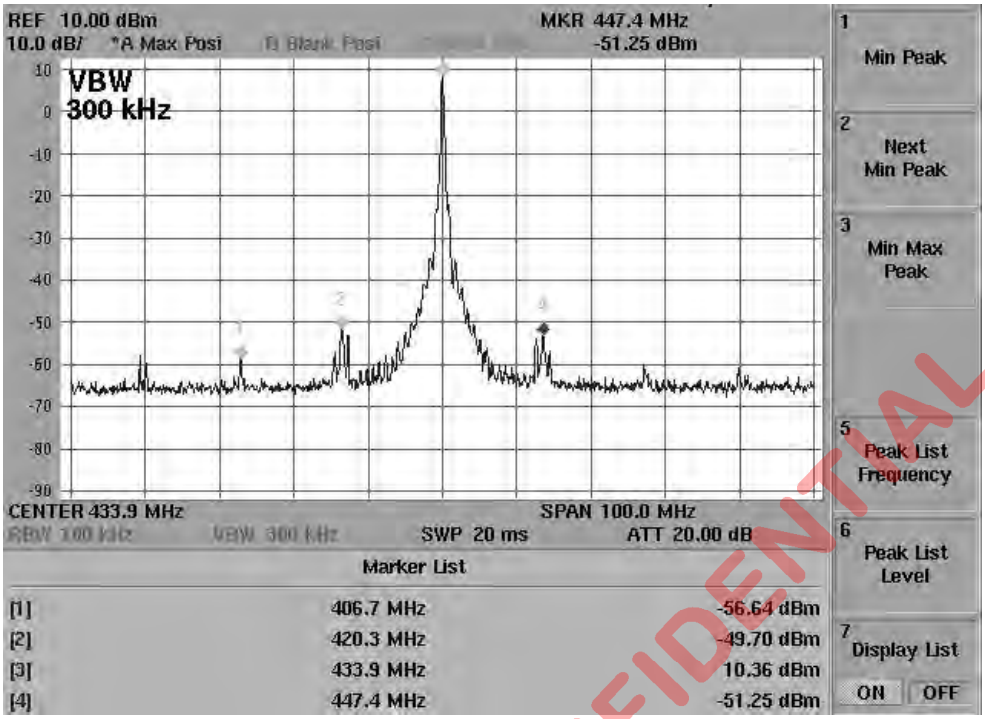


Figure 9.10.2 TX spectrum in ASK, Span 100MHz

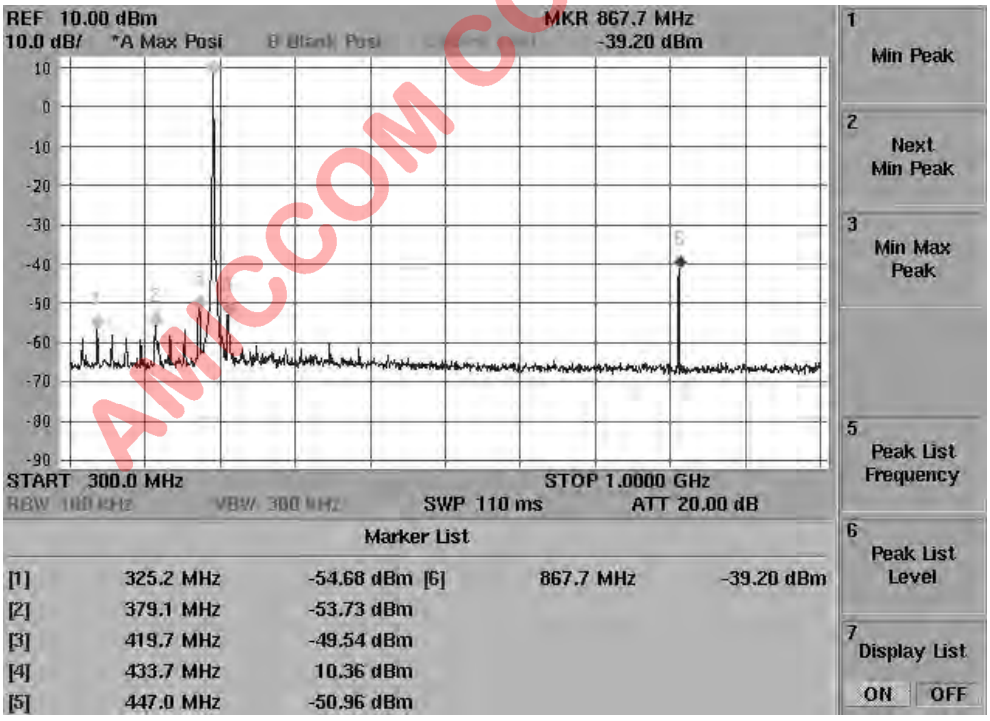


Figure 9.10.3 TX spectrum in ASK, Span 700MHz

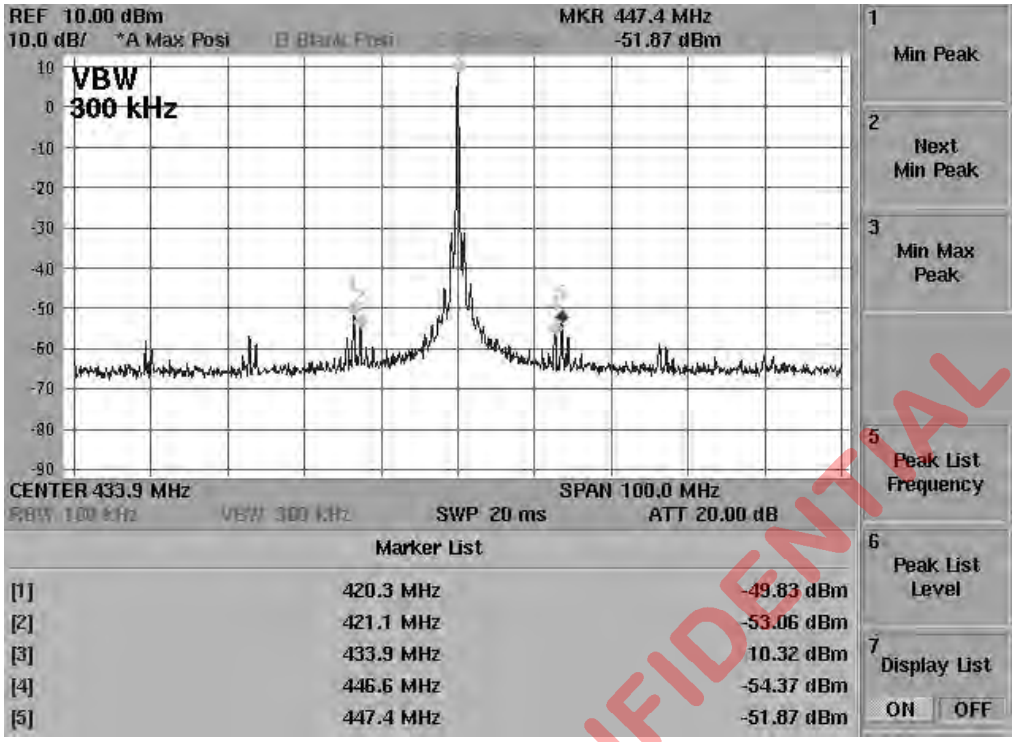


Figure 9.10.4 TX spectrum in FSK, Span 100MHz

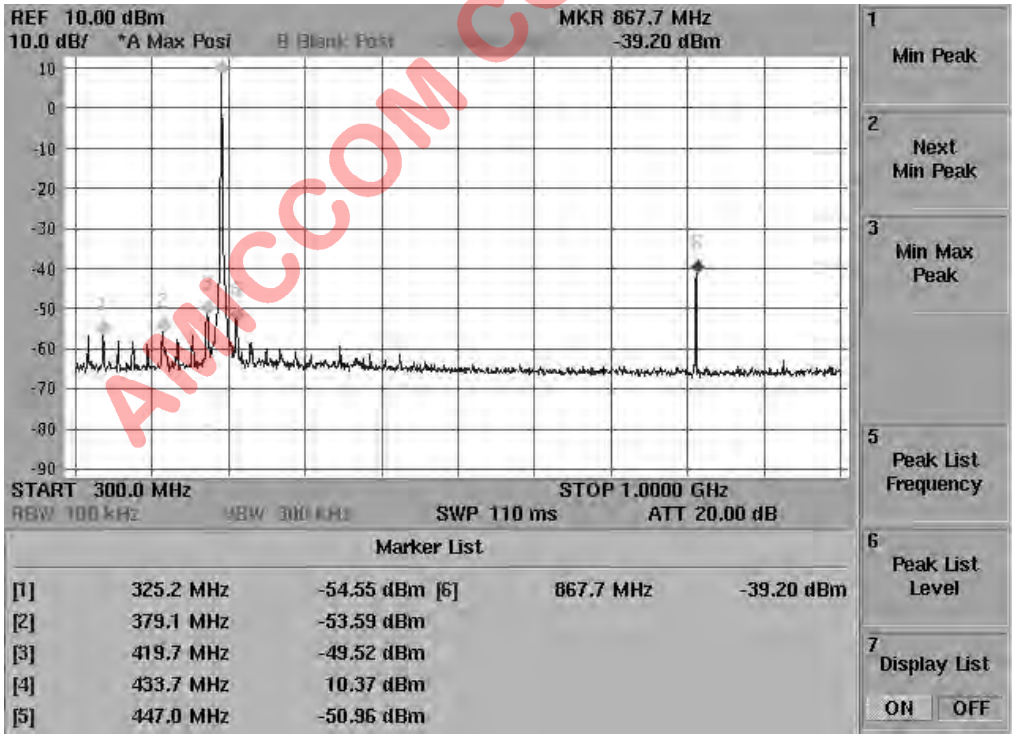


Figure 9.10.5 TX spectrum in FSK, Span 700MHz

9.11 Matching for sensitivity

According to AMICCOM's reference design, MD7103A-A41 that matching network is illustrated in Figure 9.11.1. The input impedance measured at 433.92MHz is about (31Ω-J32Ω). This shows return loss and RX sensitivity is.

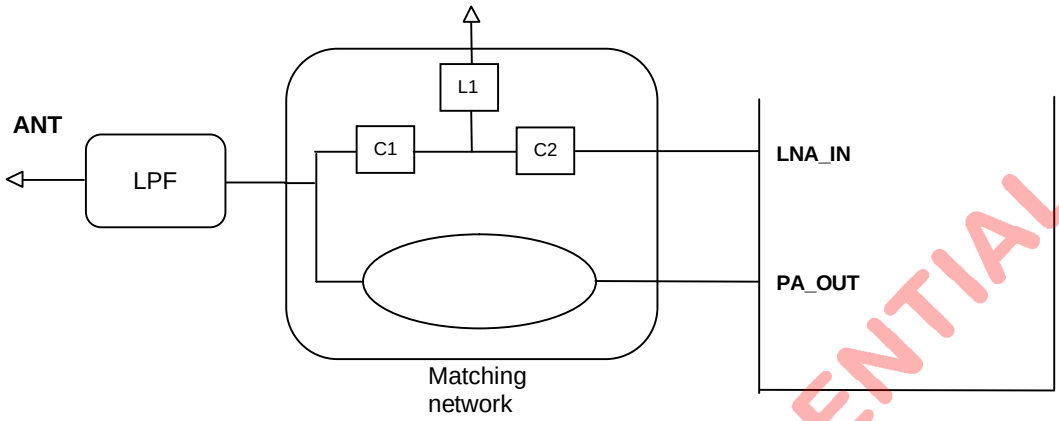


Figure 9.11.1 A typical matching network of LNA_IN

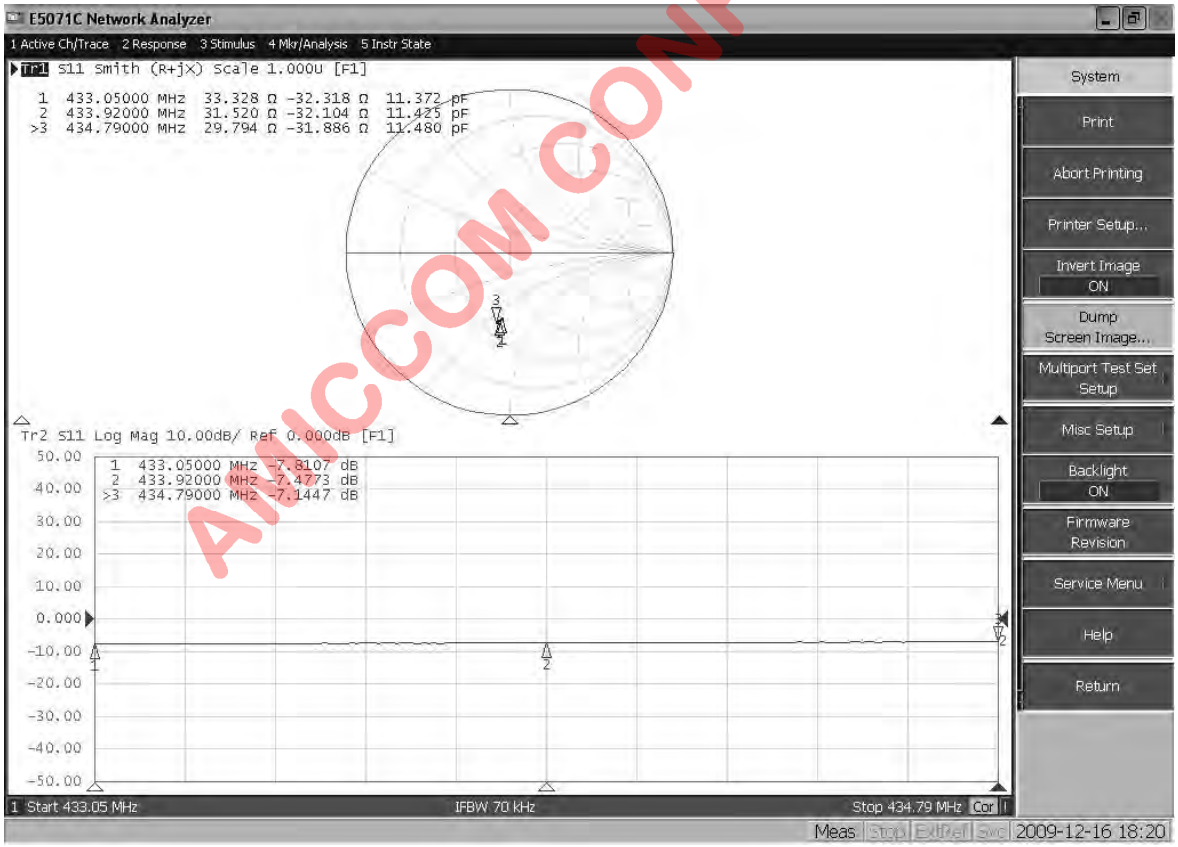


Figure 9.11.2 Input impedance of 433.92MHz when C1=1.2pF, L1=39nH , C2=100pF,.

9.12 Interference and Blocking Performance

A7103A has built-in image reject mixer and IF BW filter which provide good interference signal rejection. Below figures are set wanted signal is above 3 dBm of sensitivity level to get the carrier / interference ration. The blocking characteristics of ASK and FSK at 433.92MHz are illustrated in Fig 9.12.1 and Figure 9.12.2 respectively.

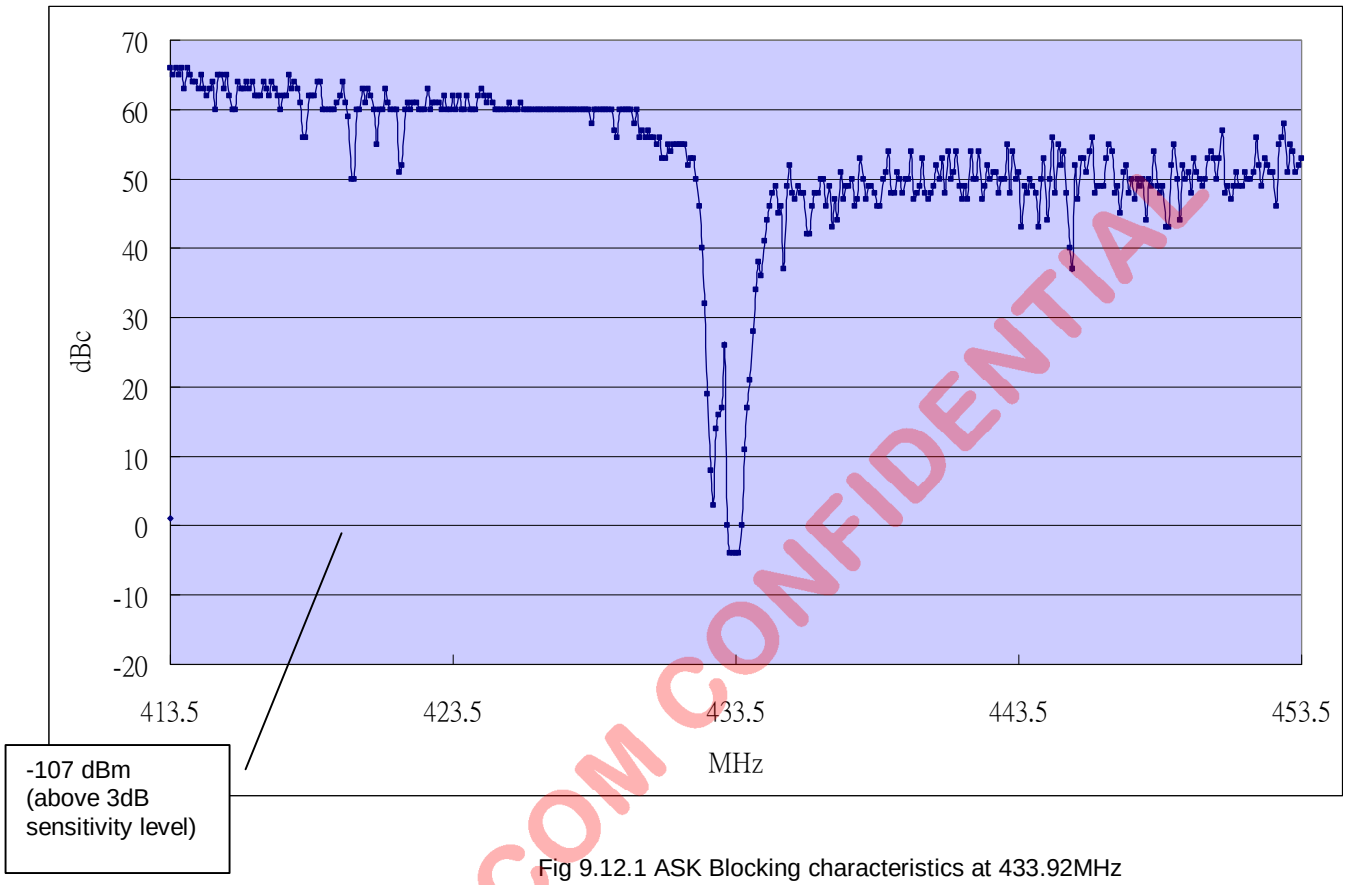


Fig 9.12.1 ASK Blocking characteristics at 433.92MHz

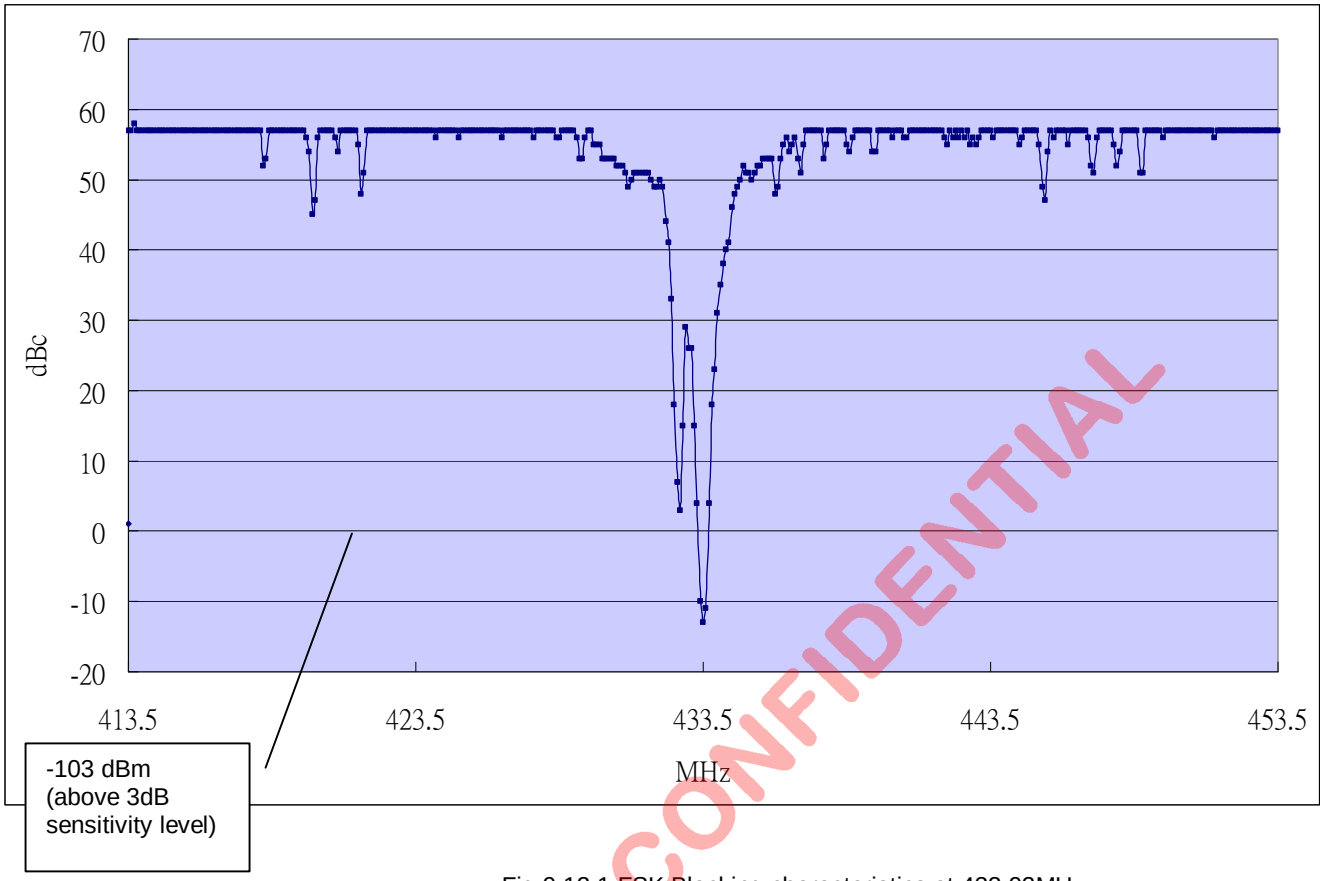
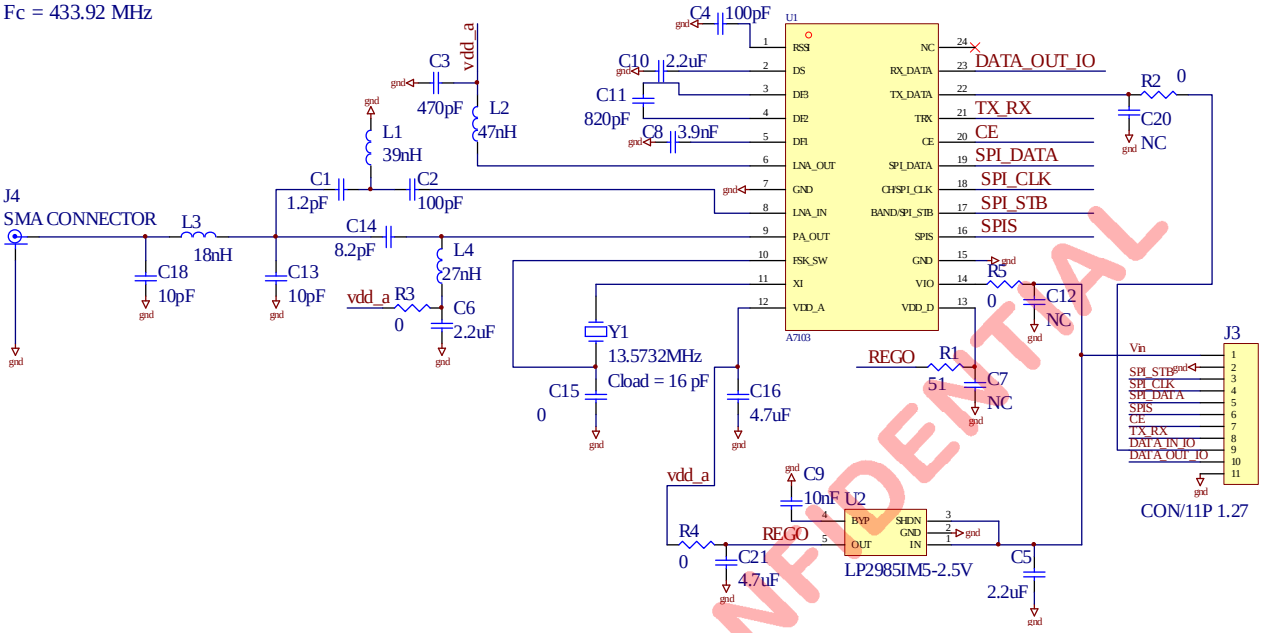


Fig 9.12.1 FSK Blocking characteristics at 433.92MHz

10. Application Circuit

10.1 SPI Control Mode for ASK (i.e. 433.92MHz)

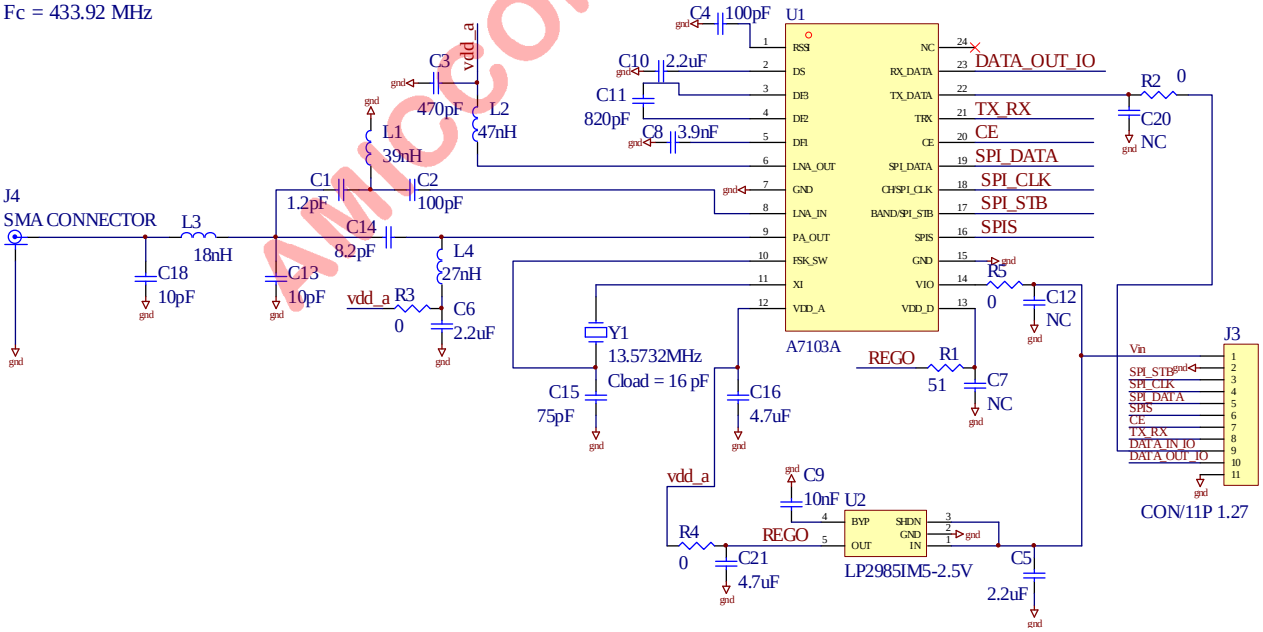
This Schematic is for ASK with Data Rate 2.4kbps
Fc = 433.92 MHz



Recommend, LDO = 2.5V and Xtal Cload = 16pF.

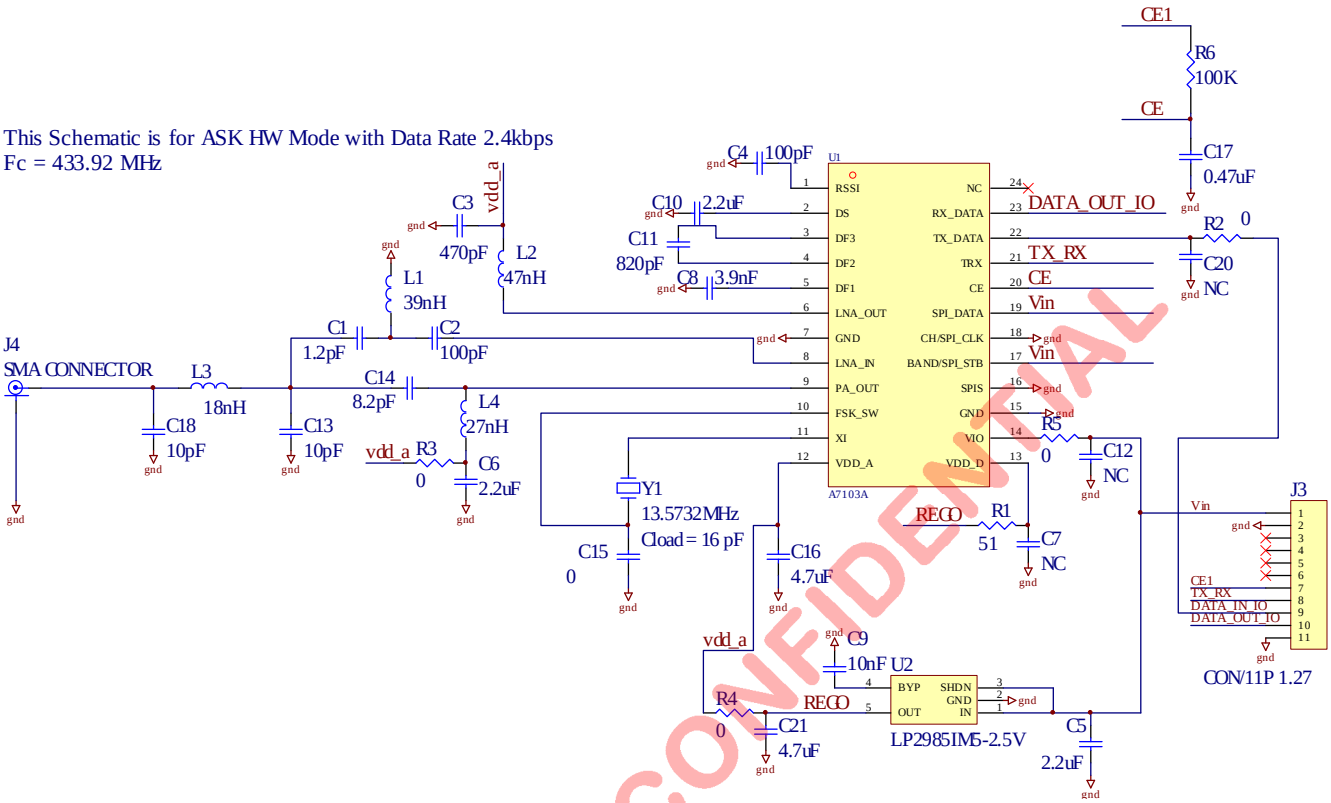
10.2 SPI Control Mode for FSK (i.e. 433.92MHz)

This Schematic is for FSK with Data Rate 2.4kbps
Fc = 433.92 MHz



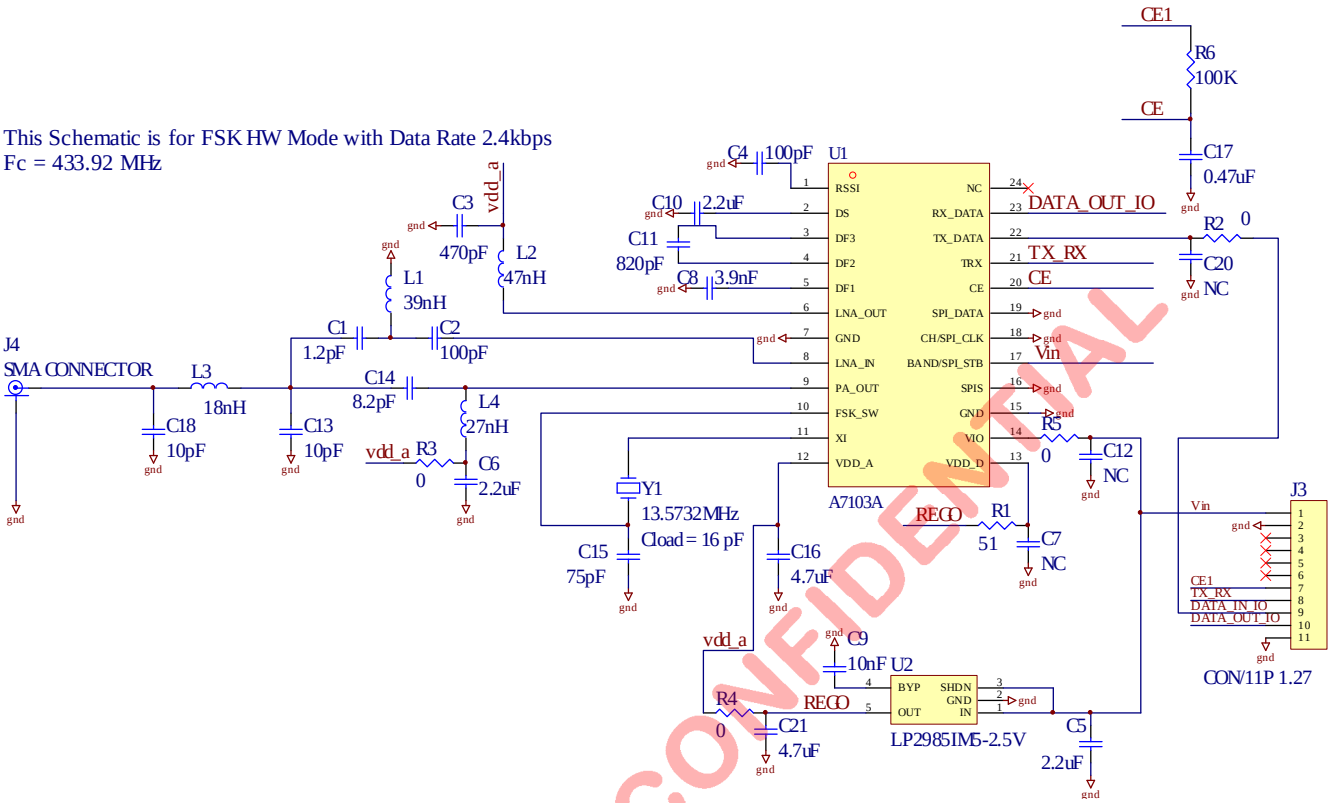
Recommend, LDO = 2.5V and Xtal Cload = 16pF.

10.3 HW Control Mode for ASK (i.e. 433.92MHz)



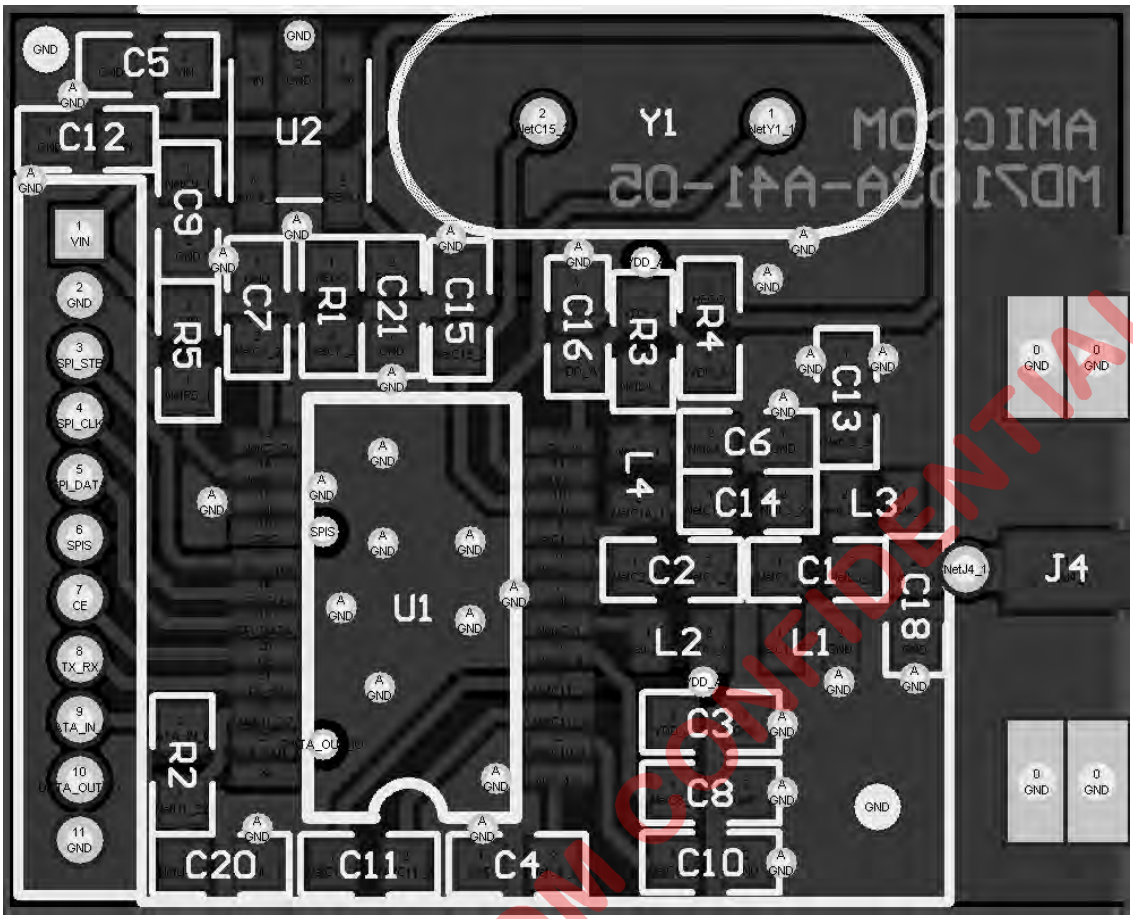
Recommend LDO = 2.5V and Xtal Cload = 16pF.

10.4 HW Control Mode for FSK (i.e. 433.92MHz)



Recommend LDO = 2.5V and Xtal Cload = 16pF.

10.5 Reference Layout of MD7103A-A41 (i.e. 433.92MHz)



Reference layout of MD7103A-A41 (433MHz band)

11. Abbreviations

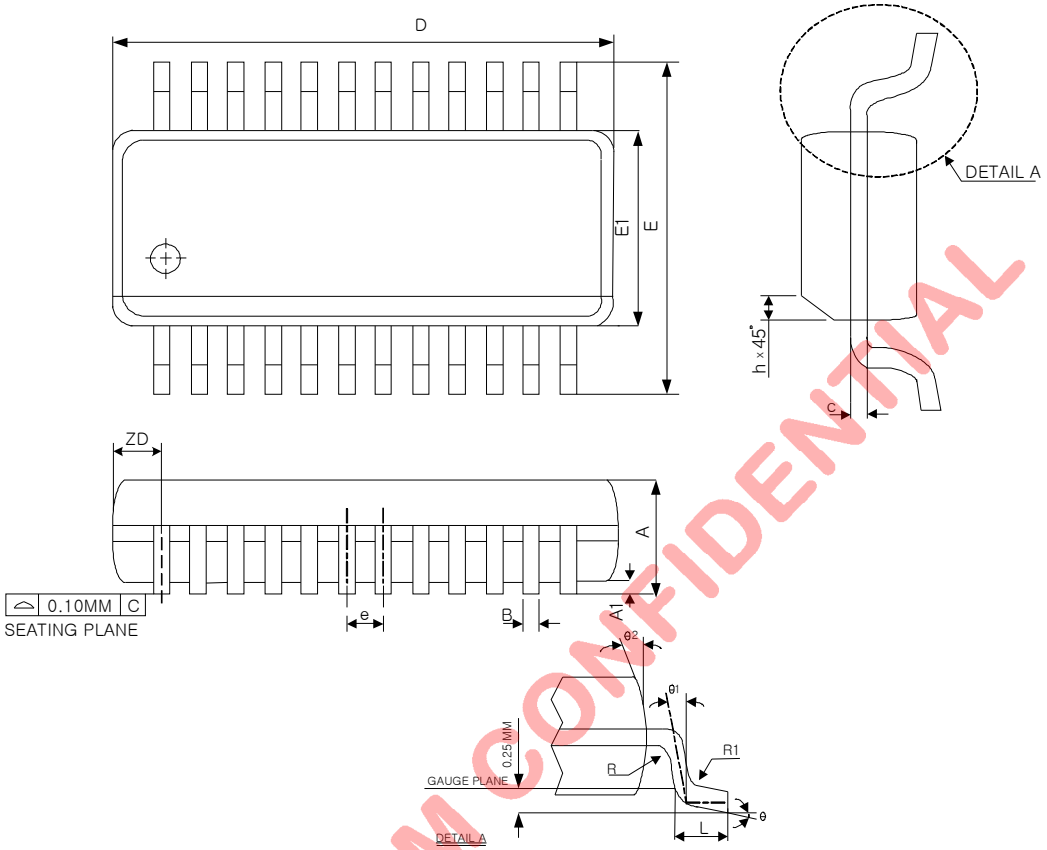
AIF	Auto IF
AGC	Automatic Gain Control
ASK	Amplitude Shift Keying
BER	Bit Error Rate
BW	Bandwidth
Fdev	Frequency Deviation
FSK	Frequency Shift Keying
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PLL	Phase Lock Loop
RX	Receiver
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
TX	Transmitter
VCO	Voltage Controlled Oscillator
Xtal	Crystal

12. Ordering Information

Part No.	Package	Units Per Reel / Tube
A71C03AUF/Q	SSOP 24L, Tape & Reel, Pb free, -40℃～85℃	3Kpcs
A71C03AUF	SSOP 24L, Tube, Pb free, -40℃～85℃	56pcs
A71C03AH	Die Form, Tray, Pb free, -40℃～85℃	250pcs

13. Package Information

SSOP24 Outline Dimensions



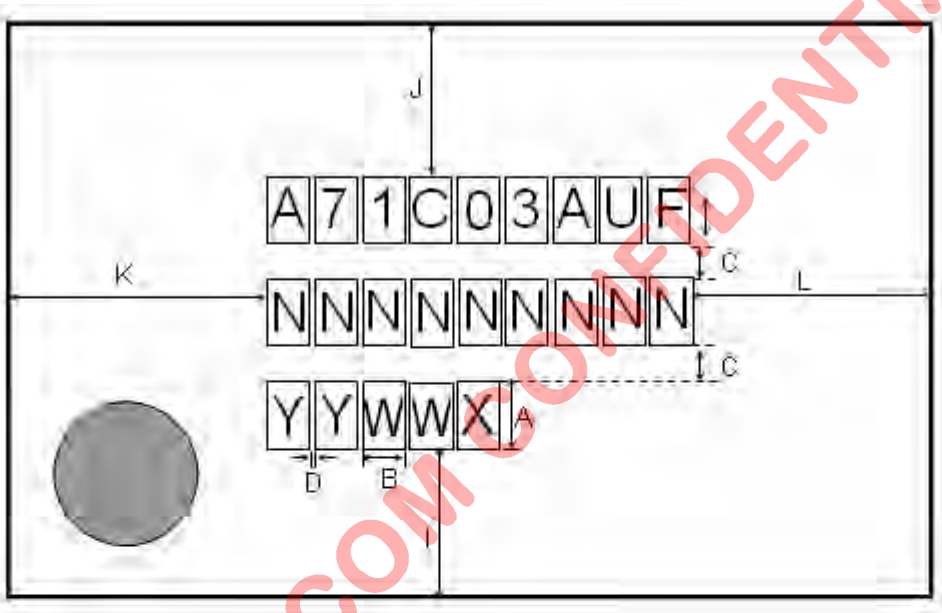
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NCM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	8.56	8.66	8.74	0.337	0.341	0.344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
ZD	0.838 REF			0.033 REF.		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEOEC	M0-137 (AF)					

14. Top Marking Information

A71C03AUF

- Part No. : **A71C03AUF**
- Pin Count : **24**
- Package Type : **SSOP**
- Dimension : **150mil**
- Mark Method : **Ink**
- Character Type : **Arial**
- Remark : **Pb Free**

Type



❖ CHARACTER SIZE : (Unit in mm)

A : 0.55
B : 0.36
C : 0.25
D : 0.03

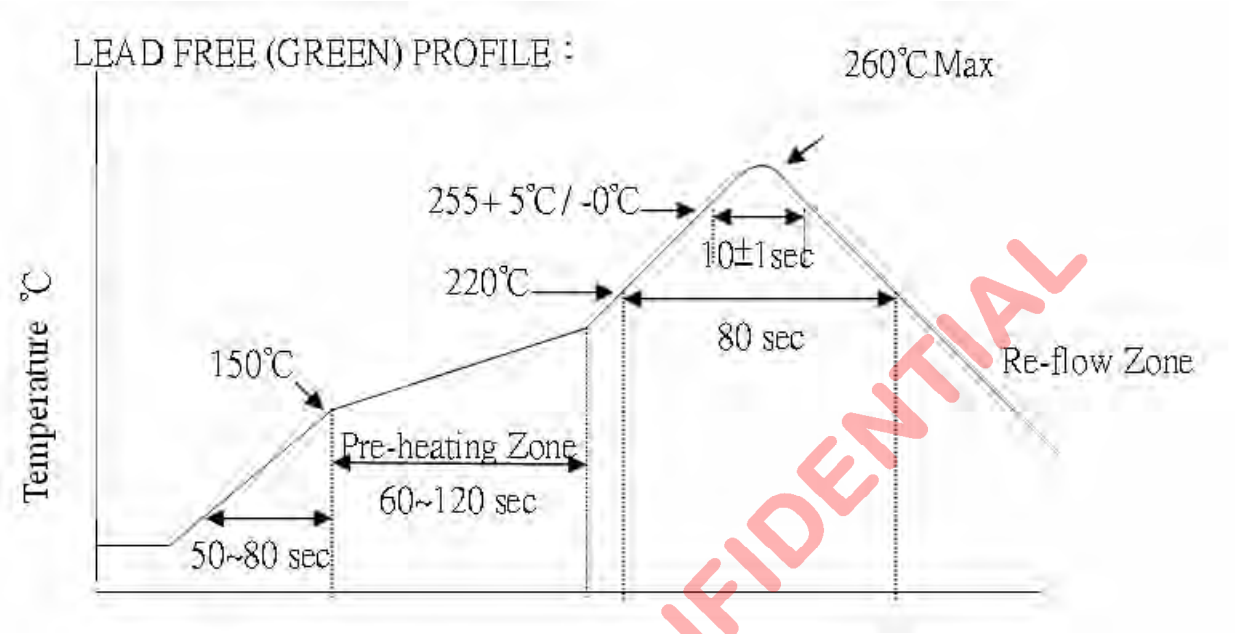
I=J
K=L

Y Y W W : DATECODE

X : PKG HOUSE ID

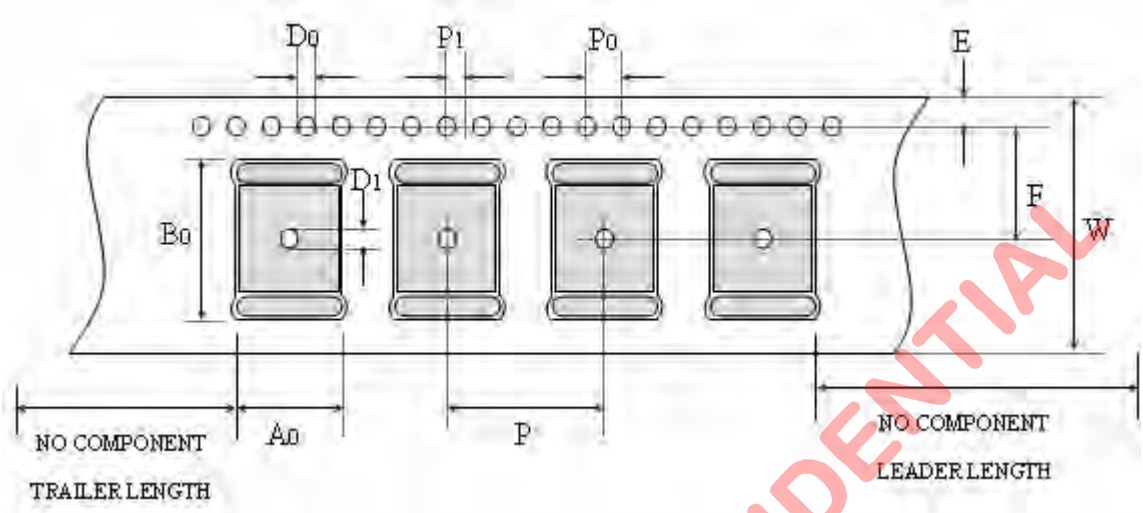
N N N N N N N N N : LOT NO. (max. 9 characters)

15. Reflow Profile



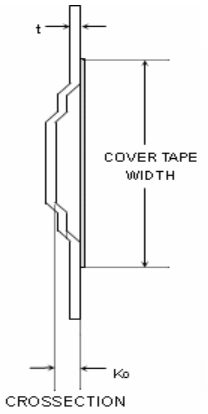
16. Tape Reel Information

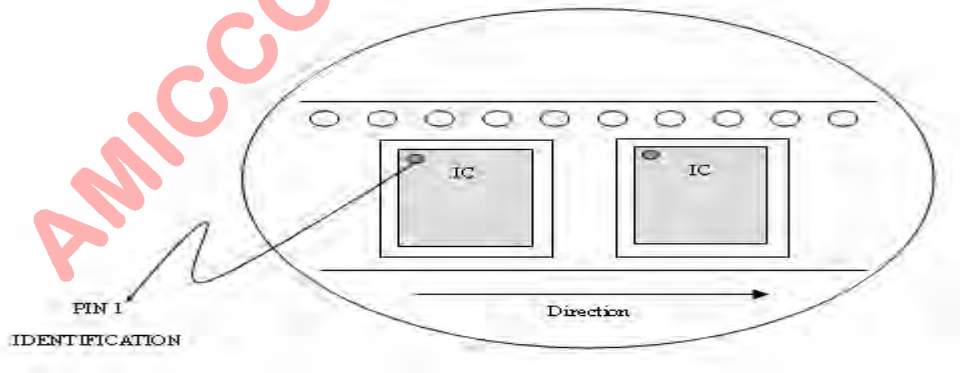
Cover / Carrier Tape Dimension



Unit: mm

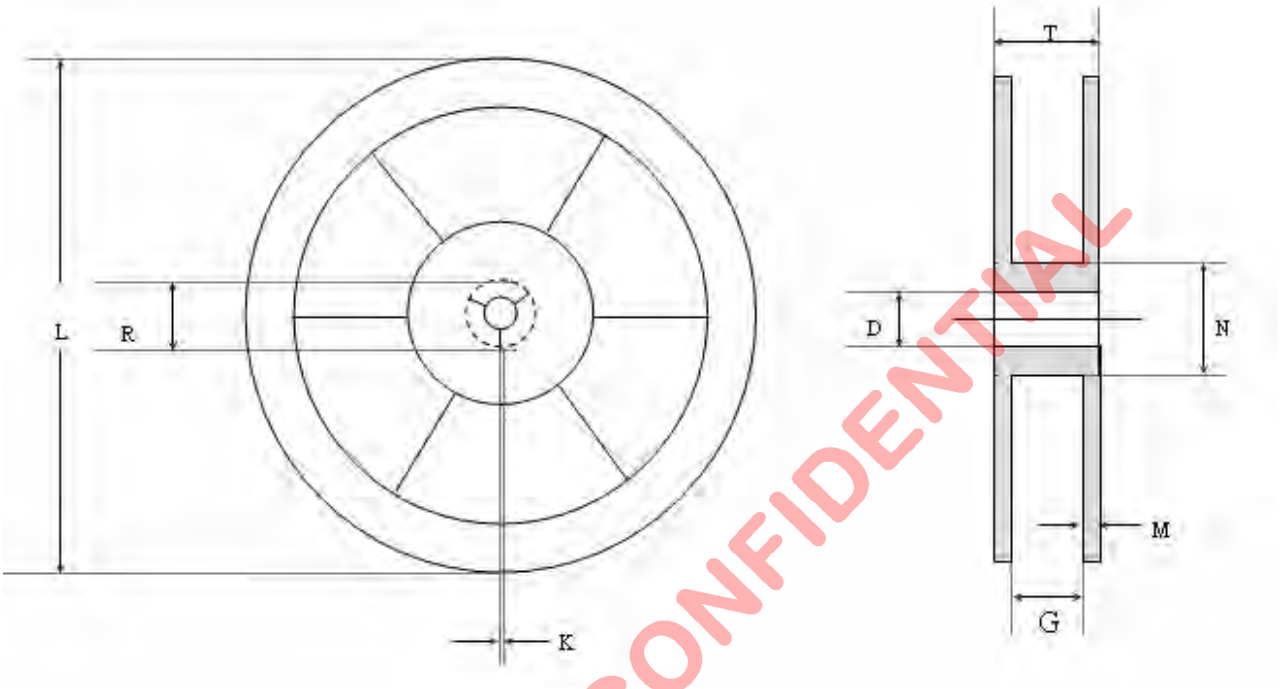
TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4*4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4*4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5*5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
QFN3*3 / DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16





TYPE	K0	t	COVER TAPE WIDTH
20 QFN (4X4)	1.1	0.3	9.2
24 QFN (4X4)	1.4	0.3	9.2
32 QFN (5X5)	1.1	0.3	9.2
QFN3*3 / DFN-10	0.75	0.25	8
20 SSOP	2.5	0.3	13.3
24 SSOP	2.1	0.3	13.3

REEL DIMENSIONS



Unit: mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) QFN(3X3) / DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330＋0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330＋0.00/-1.0	20.2

17 Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date.AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

RF ICs AMICCOM

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