

AS1119

144-LED Cross-Plexing Driver with 320mA Charge-Pump

General Description

The AS1119 is a compact LED driver for 144 (90) single LEDs. The devices can be programmed via an I²C compatible interface.

The AS1119 offers two blocks driving each 72 LEDs (3 blocks each 30LEDs) with 1/9 (1/6) cycle rate. The required lines to drive all 144 (90) LEDs are reduced to 18 by using the cross-plexing feature optimizing space on the PCB. Every block driving 72(30) LEDs can be analog dimmed from 1 to 30mA in 256 steps (8 bit).

Additionally each of the 144 (90) LEDs can be dimmed individually with 8-bit allowing 256 steps of linear dimming. To reduce CPU usage up to 6 frames can be stored with individual time delays between frames to play small animations automatically.

The AS1119 operates from 2.7V to 5.5V and includes a 320mA charge-pump to drive also white LEDs. The charge-pump operates in 2:3 and 1:2 mode.

The AS1119 features very low shutdown and operational current. The device is available in a ultrasmall 36-pin WL-CSP.

[Ordering Information](#) and [Content Guide](#) appear at end of *datasheet*.

Key Benefits & Features

The benefits and features of the AS1119, 144-LED Cross-Plexing Driver with 320mA Charge-Pump are listed below:

Figure 1:
Added Value of Using AS1119

Benefits	Features
<ul style="list-style-type: none"> • Excellent PCB real estate vs LED count 	<ul style="list-style-type: none"> • Up to 144LEDs as 2x 8x9 or 3x 5x6
<ul style="list-style-type: none"> • 16.7M full color matrix with white balance 	<ul style="list-style-type: none"> • 8bit PWM per LED and current control per matrix
<ul style="list-style-type: none"> • Reduces MCU load and increases battery lifetime 	<ul style="list-style-type: none"> • 6 frames of memory
<ul style="list-style-type: none"> • Extends battery lifetime while reducing BOM and increasing ease of use 	<ul style="list-style-type: none"> • Internal automatic charge pump

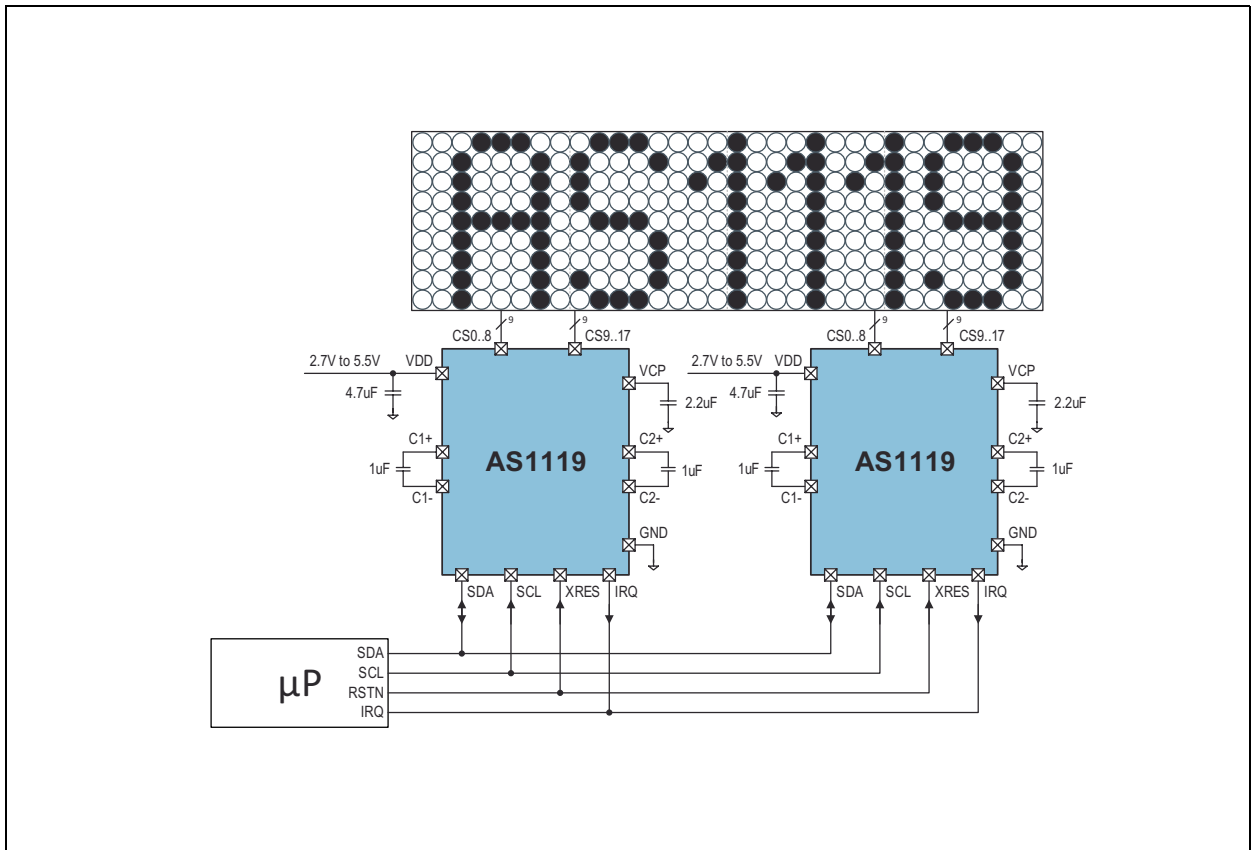
- 1MHz I²C-compatible interface
- Open and shorted LED error detection
- 144 LEDs in dot matrix
- Low-power shutdown current

- Individual 8-bit LED PWM control
- 8-bit analog brightness control
- (1:1), 2:3, 1:2 320mA charge pump
- 6 frames memory for animations
- System-clk synchronisation for multiple devices
- Supply voltage range: 2.7V to 5.5V
- Minimum PCB space required
- 36-pin WL-CSP package

Applications

The AS1119 is ideal for dot matrix displays in mobile phones, personal electronics and toys.

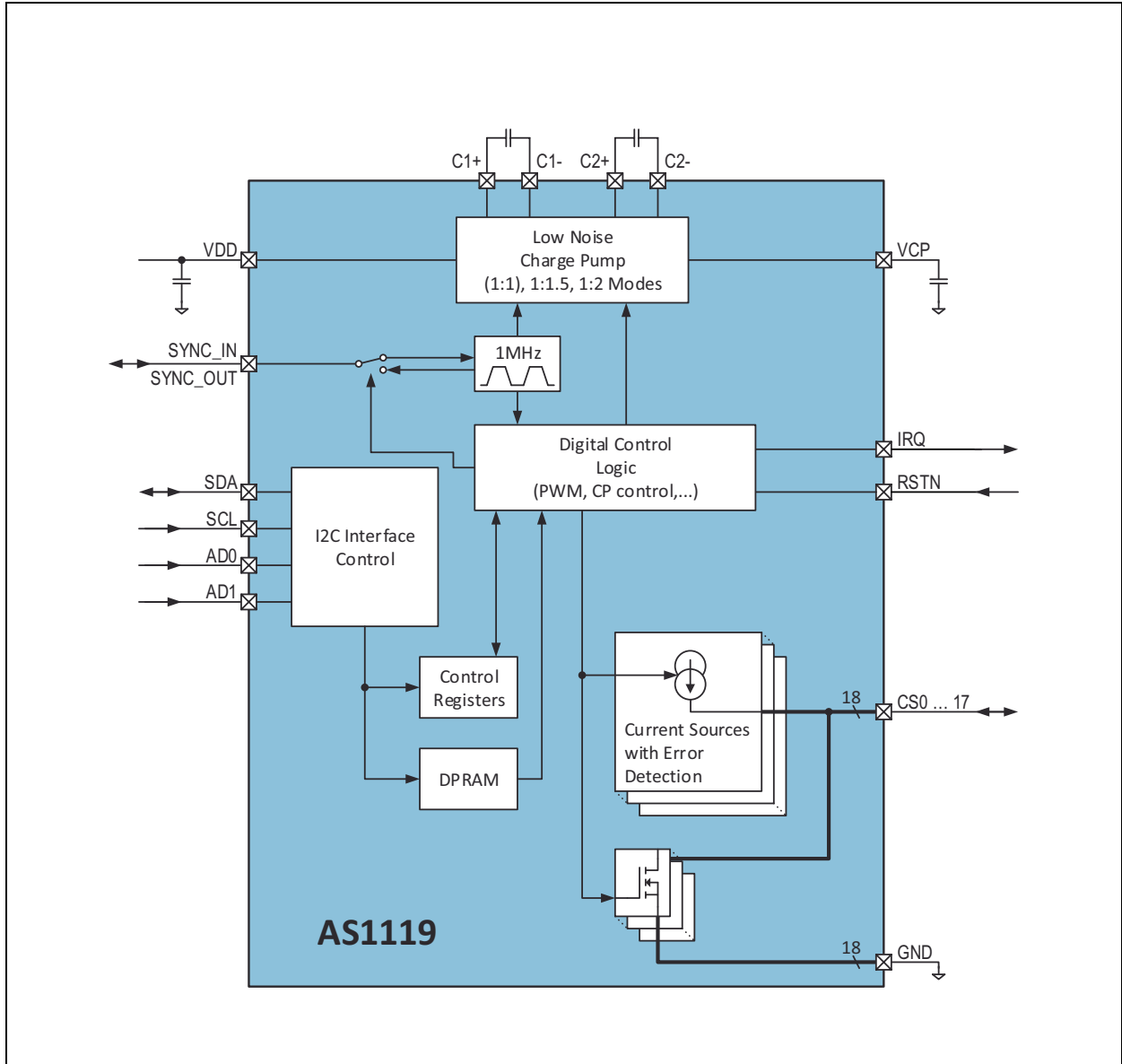
Figure 2:
Typical Application Diagram



Block Diagram

The functional blocks of this device are shown below:

Figure 3:
AS1119 Block Diagram



Pin Assignments

The AS1119 pin assignments are described below:

Figure 4:
Pin Diagram (Top View)

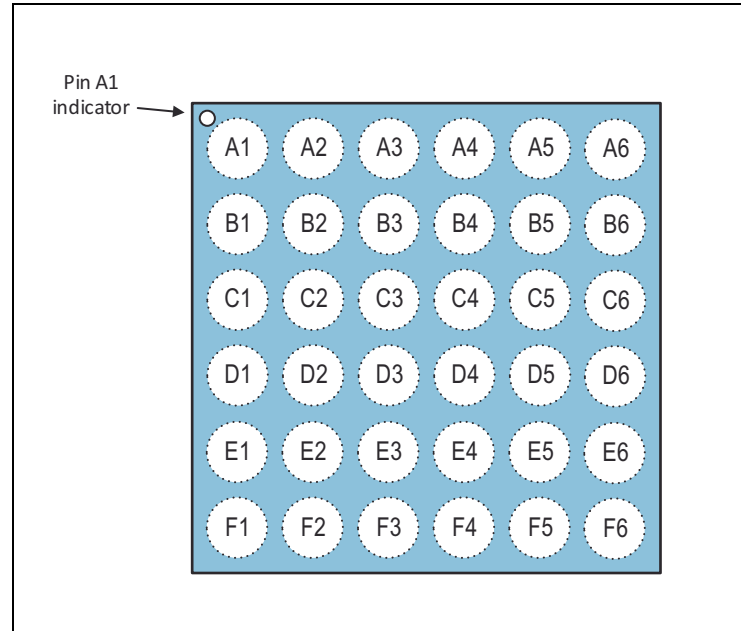


Figure 5:
Pin Description

Pin Name	Pin Number	Description
$V_{DD1}, V_{DD2}, V_{DD3}$	A6, E5, E1	Positive Supply Voltage. Connect to a +2.7V to +5.5V supply. Bypass this pin with 10 μ F capacitance to GND1, GND2, GND3.
VCP	F1	Charge-Pump Output Voltage. Connect a 2.2 μ F capacitor to GND3.
C1-, C1+	B1, C1	Flying Cap 1. Connect a 1 μ F capacitor.
C2-, C2+	A1, D1	Flying Cap 2. Connect a 1 μ F capacitor.
GND1	B5	Ground for VDD1. Used for CS0-CS8
GND2	F5	Ground for VDD2. Used for CS9-CS17
GND3	A2	Ground for VDD3. Used for Charge-Pump.
SDA	C6	Serial-Data I/O. Open drain digital I/O I ² C data pin.
SCL	D6	Serial-Clock Input.
AD0	C5	I²C Address for bit 0. Put to GND or VDD to set I ² C addresses.
AD1	D5	I²C Address for bit 1. Put to GND or VDD to set I ² C addresses.

Pin Name	Pin Number	Description	
RSTN	F6	Reset Input. Pull this pin to logic low to reset all control registers (set to default values) and to put the device into power-down. For normal operation pull this pin to VDD.	
SYNC_IN, SYNC_OUT	B6	Synchronization Clock Input or Output	
IRQ	E6	Interrupt Request. Open drain digital Output.	
CS0 - CS8	A5-A3, B4-B2, C4-C2	2 Matrices	Sinks and Sources for 72 LEDs each matrix.
CS9 - CS17	D4-D2, E4-E2, F4-F2		
CS0 - CS5	A5-A3, B4-B2	3 Matrices	Sinks and Sources for 30 LEDs each matrix.
CS6 - CS11	C4-C2, D4-D2		
CS12 - CS17	E4-E2, F4-F2		

Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comments
Electrical Parameters				
V _{DD} to GND	-0.3	7	V	
All other pins to GND	-0.3	7 or V _{DD} + 0.3	V	
Sink current		500	mA	
Segment current		100	mA	
Input current (latch-up immunity)	-100	100	mA	JEDEC 78
Electrostatic Discharge				
Electrostatic discharge HBM	±1.5		kV	MIL 883 E method 3015
Temperature Ranges and Storage Conditions				
Junction temperature		125	°C	
Storage temperature range	-55	125	°C	
Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> .
Relative humidity (non-condensing)	5	85	%	
Moisture sensitivity level	1			Represents a max. floor life time of unlimited

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

$V_{DD} = 2.7V$ to $5.5V$, $T_{AMB} = -40^{\circ}C$ to $85^{\circ}C$, typ. values are at $T_{AMB} = 25^{\circ}C$ (unless otherwise specified).

Figure 7:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{AMB}	Operating temperature range		-40		85	$^{\circ}C$
V_{DD}	Operating supply voltage		2.7		5.5	V
I_{DDSD}	Software shutdown supply current	All digital inputs at V_{DD} or GND, $V_{DD} = 5.5V$, $T_{AMB} = 25^{\circ}C$		7		μA
I_{DDFSD}	Full shutdown supply current	Pin RSTN = 0V, $T_{AMB} = 25^{\circ}C$		0.1	1	μA
I_{DD}	Operating supply current (all current sources turned off)	CP disabled @ $V_{DD} = 5.5V$		1.4		mA
		With CP in 2:3 mode @ $V_{DD} = 2.7V$		3		
		With CP in 1:2 mode @ $V_{DD} = 2.7V$		4		
I_{START}	Max. peak inrush current			1.5		A
	Max. DC current			700		mA
I_{DIGIT}	Digit drive sink current (drive capability of all sources of one digit ^{(1), (2)})	CP disabled			500	mA
		CP enabled	$V_{DD} < 3.3V$		160	
			$V_{DD} \geq 3.3V$		320	
I_{SEG}	Segment drive source current LED	$V_{OUT} = 1.8V$ to $V_{DD} - 400mV$	28	30	32	mA
ΔI_{SEG}	Segment drive current matching LED ⁽³⁾			2		%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DSSAT}	Saturation voltage	Current = 30mA, V _{DD} = 5V		100		mV
R _{DSON(N)}	Resistance for NMOS			0.5	1	Ω
f _{OSC}	Oscillator frequency		0.9	1	1.1	MHz
f _{REFRESH}	Display scan rate	2 time 9 × 8 matrixes	0.39	0.43	0.48	kHz

Note(s):

1. Not all sources are allowed to be fully ON at the same time.
2. guaranteed by design

$$3. I_{SEG} = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \times 100$$

Figure 8:
Logic Inputs/Outputs Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{IH} , I _{IL}	Logic input current	V _{IN} = 0V or V _{DD}	-1		1	μA
V _{IH}	Logic high input voltage		1.6			V
V _{IL}	Logic low input voltage				0.6	V
ΔV _I	Hysteresis voltage			0.1		V
V _{OL(SDA)}	SDA output low voltage	I _{SINK} = 3mA			0.4	V
V _{OL(IRQ)}	IRQ output low voltage	I _{SINK} = 3mA			0.4	V
V _{OL(SYNC_OUT)}	Sync clock output low voltage	I _{SINK} = 1mA			0.4	V
V _{OH(SYNC_OUT)}	Sync clock output high voltage	I _{SOURCE} = 1mA			V _{DD} - 0.4	V
	Open detection level threshold		V _{DD} - 0.4	V _{DD} - 0.1		V
	Short detection level threshold			0.9	1.2	V
	Capacitive load for each bus line	SCL frequency = 400kHz			400	pF
		SCL frequency = 1000kHz			100	

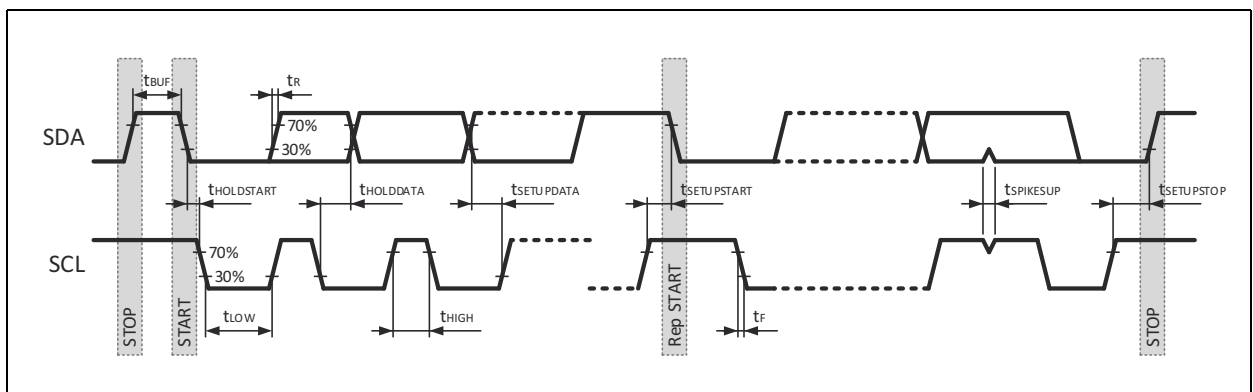
Figure 9:
I²C Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{SCL}	SCL frequency		100		1000	kHz
t _{BUF}	Bus free time between STOP and START conditions		1.3			µs
t _{HOLDSTART}	Hold time for repeated START condition		160			ns
t _{LOW}	SCL low period		50		75	ns
t _{HIGH}	SCL high period		50		75	ns
t _{SETUPSTART}	Setup time for repeated START condition		100			ns
t _{SETUPDATA}	Data setup time		10			ns
t _{HOLDDATA}	Data hold time				70	ns
t _{RISE(SCL)}	SCL rise time		10		40	ns
t _{RISE(SCL1)}	SCL rise time after repeated START condition and after an ACK bit		10		80	ns
t _{FALL(SCL)}	SCL fall time		10		40	ns
t _{RISE(SDA)}	SDA rise time		20		80	ns
t _{FALL(SDA)}	SDA fall time		20		80	ns
t _{SETUPSTOP}	STOP condition setup time		160			ns
t _{SPIKESUP}	Pulse width of spike suppressed			50		ns

Note(s):

1. The Min / Max values of the Timing Characteristics are guaranteed by design.

Figure 10:
Timing Diagram



Typical Operating Characteristics

Figure 11:
Segment Drive Current vs. Supply Voltage

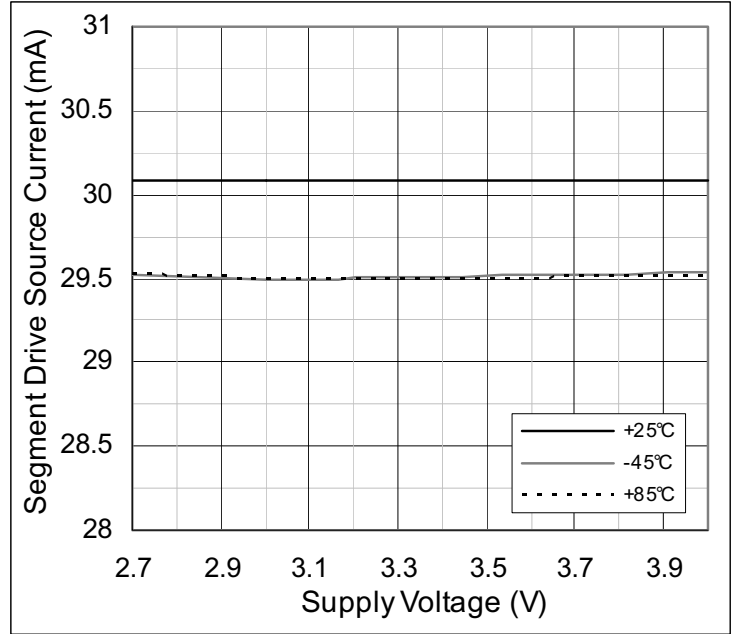


Figure 12:
Segment Drive Current vs. Temperature

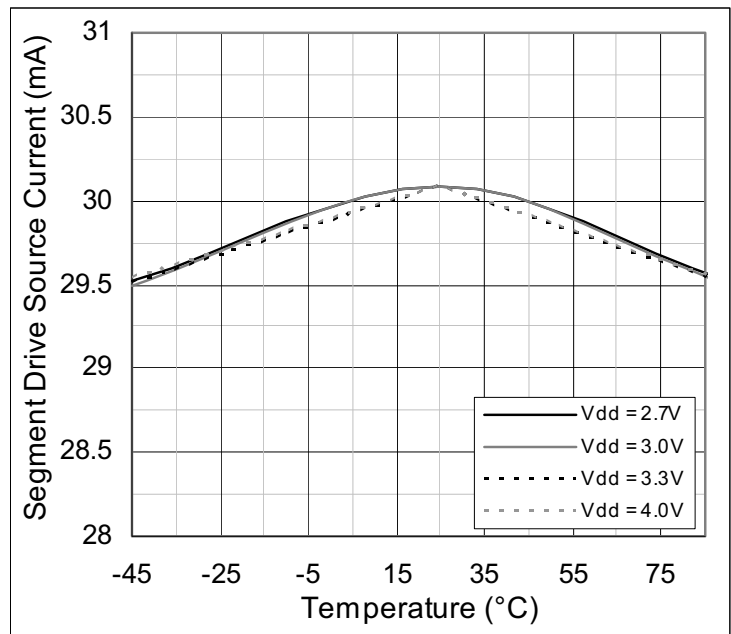


Figure 13:
Segment Drive Current vs. Output Voltage

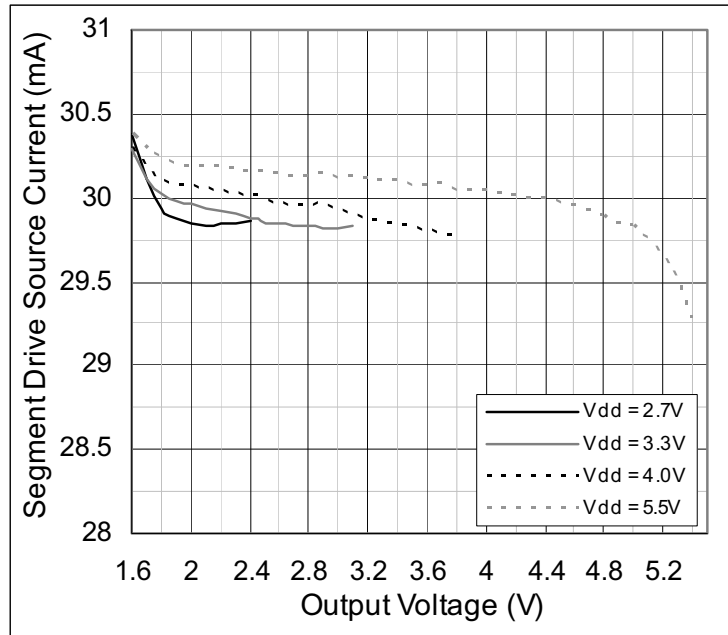


Figure 14:
R_{ONMOS} vs. Supply Voltage

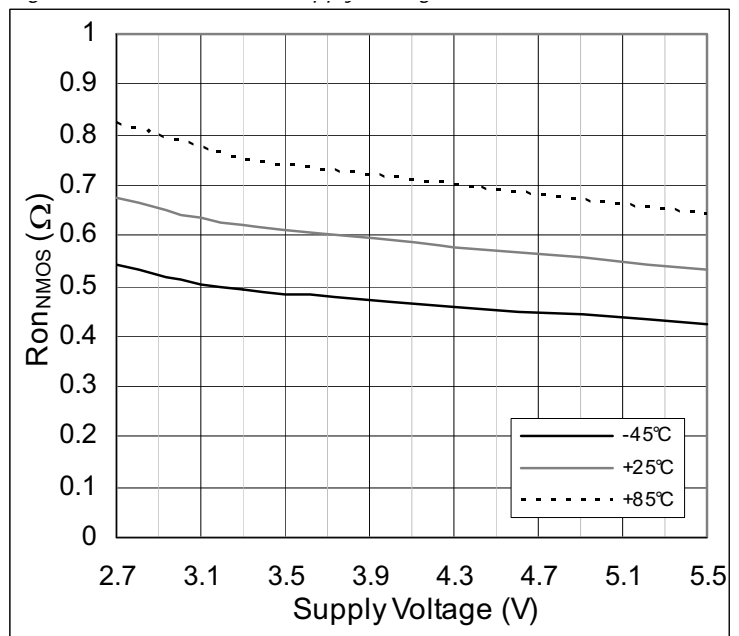


Figure 15: Open Detection Level vs. Supply Voltage

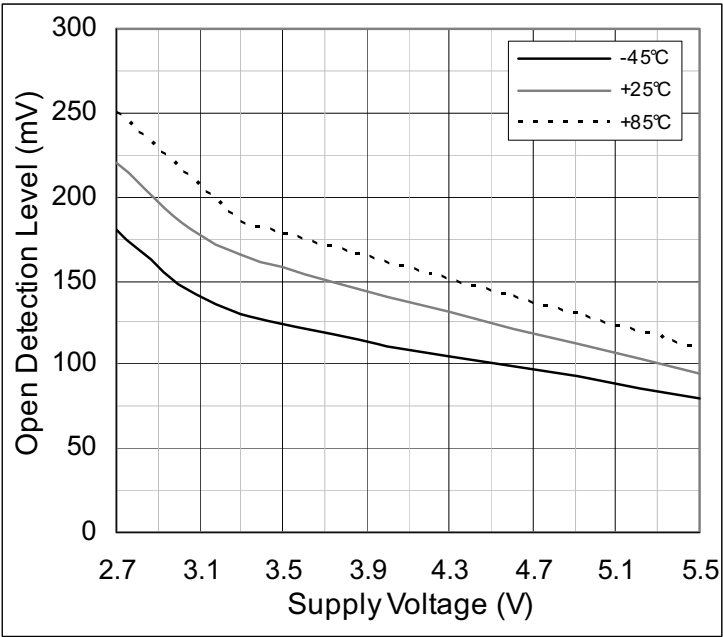


Figure 16: Short Detection Level vs. Supply Voltage

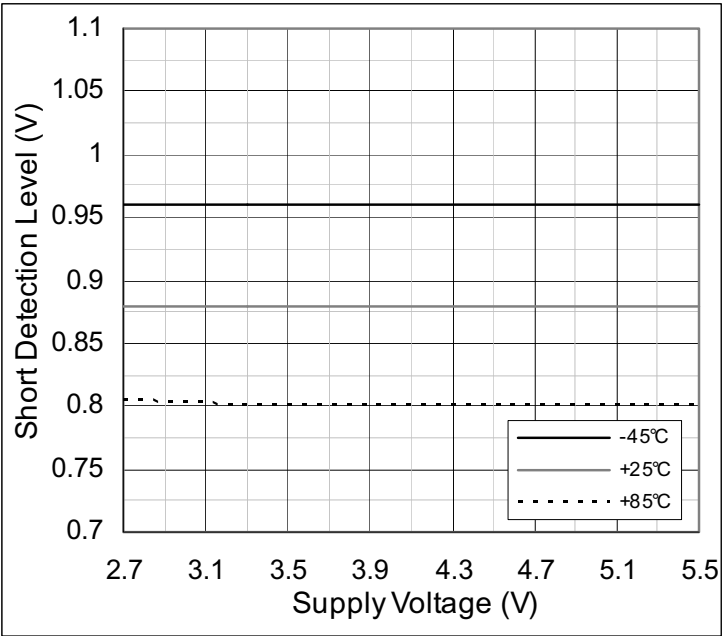


Figure 17:
Efficiency vs. Supply Voltage

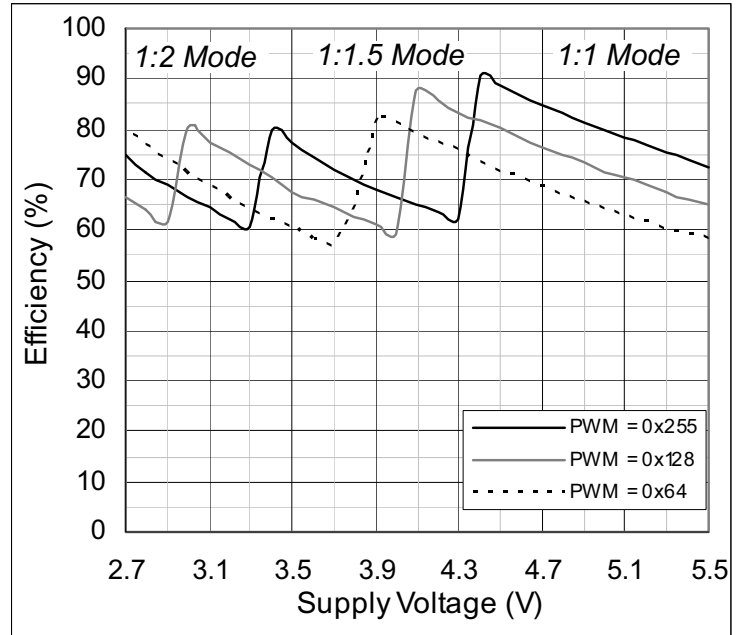


Figure 18:
Logic Input Voltage Levels

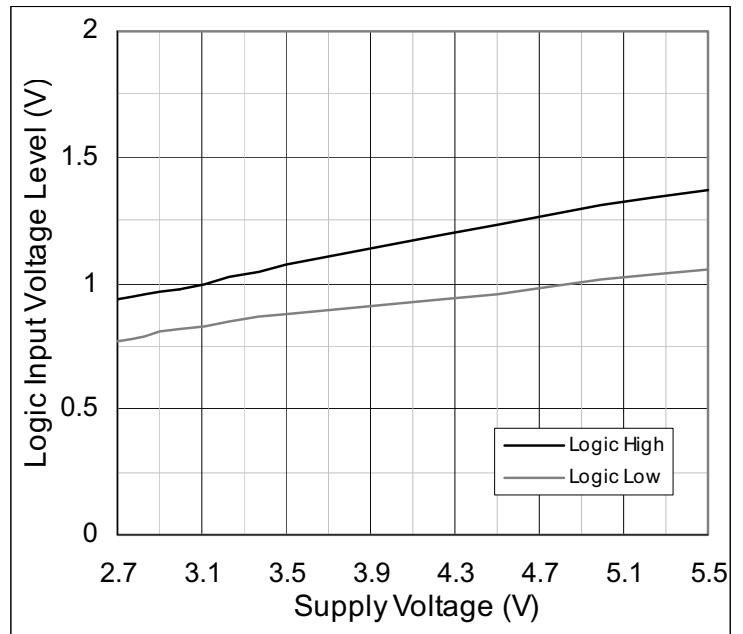
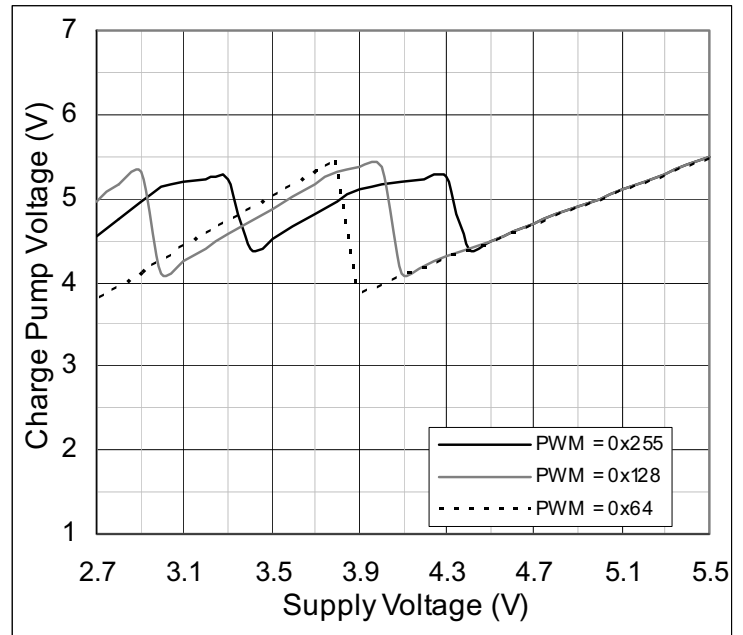


Figure 19:
Charge Pump Voltage vs. Supply Voltage



Detailed Description

I²C Interface

The AS1119 supports the I²C serial bus and data transmission protocol in fast mode at 1MHz. The AS1119 operates as a slave on the I²C bus. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. Connections to the bus are made via the open-drain I/O pins SCL and SDA.

Figure 20:
I²C Interface Initialization

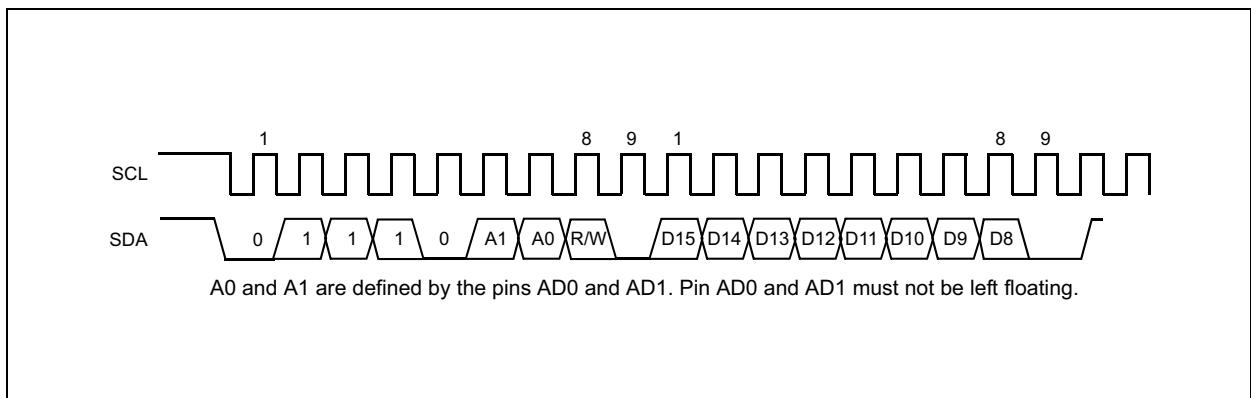
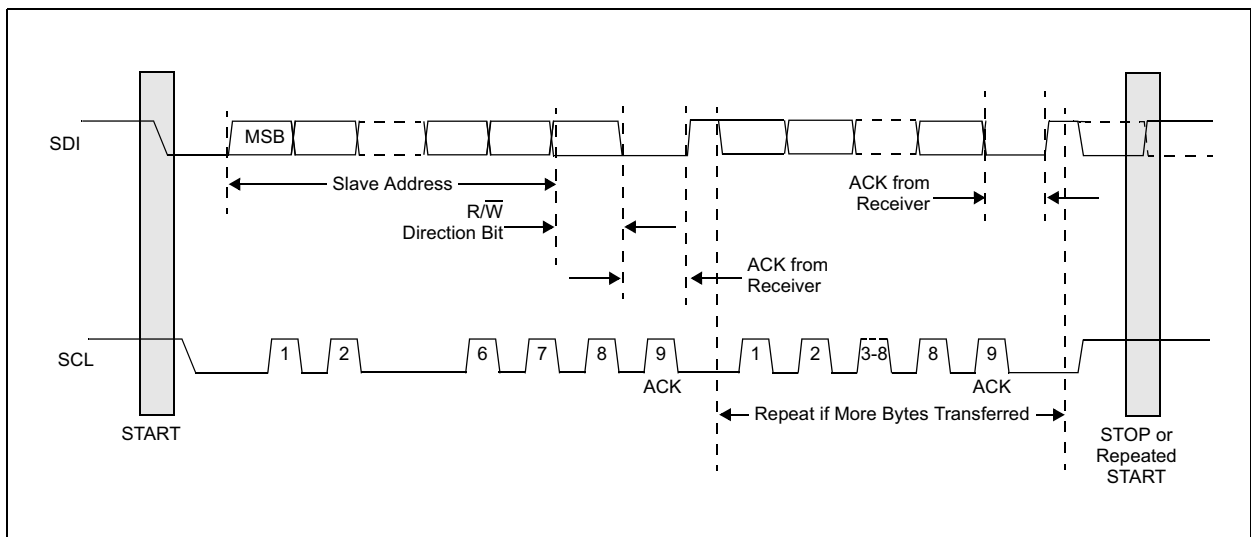


Figure 21:
Bus Protocol



The bus protocol (as shown in [Figure 21](#)) is defined as:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The bus conditions are defined as:

- **Bus Not Busy.** Data and clock lines remain HIGH.
- **Start Data Transfer.** A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
- **Stop Data Transfer.** A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.
- **Data Valid.** The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit. Within the I²C bus specifications a high-speed mode (3.4MHz clock rate) is defined.
- **Acknowledge.** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Ofcourse, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.
- **Figure 21** details how data transfer is accomplished on the I²C bus. Depending upon the state of the R/W bit, two types of data transfer are possible:
 - **Master Transmitter to Slave Receiver.** The first byte transmitted by the master is the slave address, followed by a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
 - **Slave Transmitter to Master Receiver.** The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

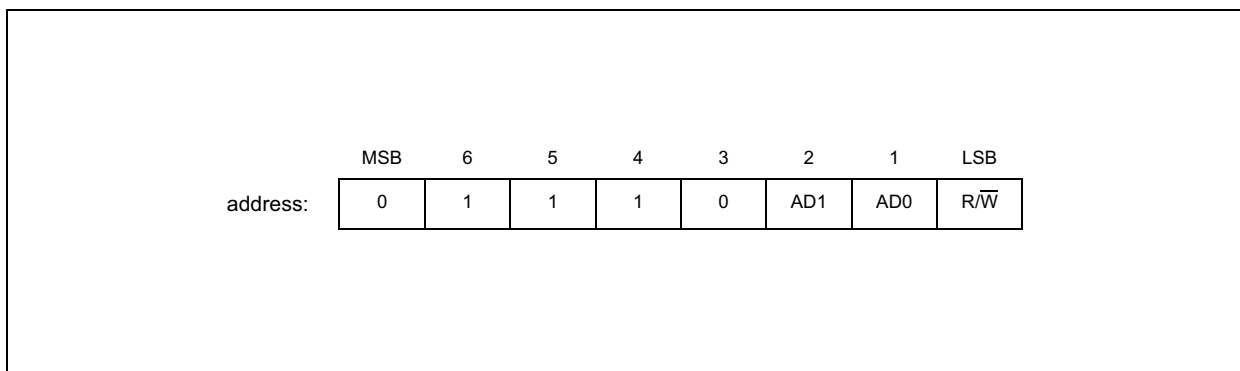
The AS1119 can operate in the following slave modes:

- Slave Receiver Mode.** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- Slave Transmitter Mode.** The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the AS1119 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

I²C Device Address Byte

The address byte (see Figure 22) is the first byte received following the START condition from the master device.

Figure 22:
I²C Device Address Byte



- The bit 1 and bit 2 of the address byte are the device select pins AD0 and AD1, which must be set to V_{DD} or to GND. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.
- The last bit of the address byte (R/W) define the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected.

Following the START condition, the AS1119 monitors the I²C bus, checking the device type identifier being transmitted. Upon receiving the address code, and the R/W bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The AS1119 operation, (see [Figure 21](#)) is determined by a command byte (see [Figure 23](#)).

Figure 23:
Command Byte

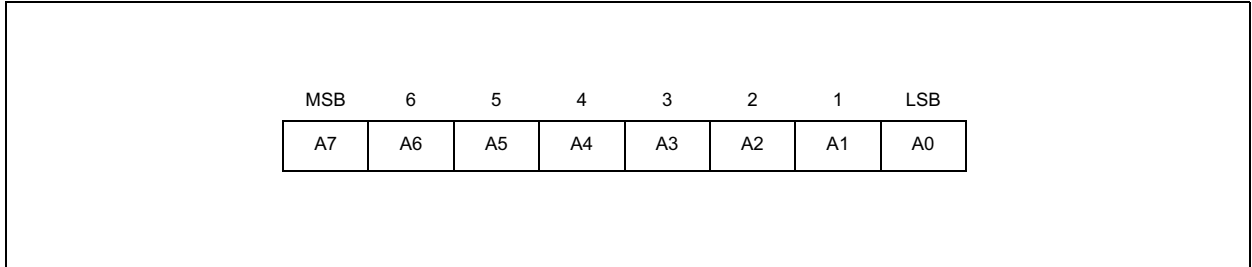


Figure 24:
Command and Single Data Byte Received by AS1119

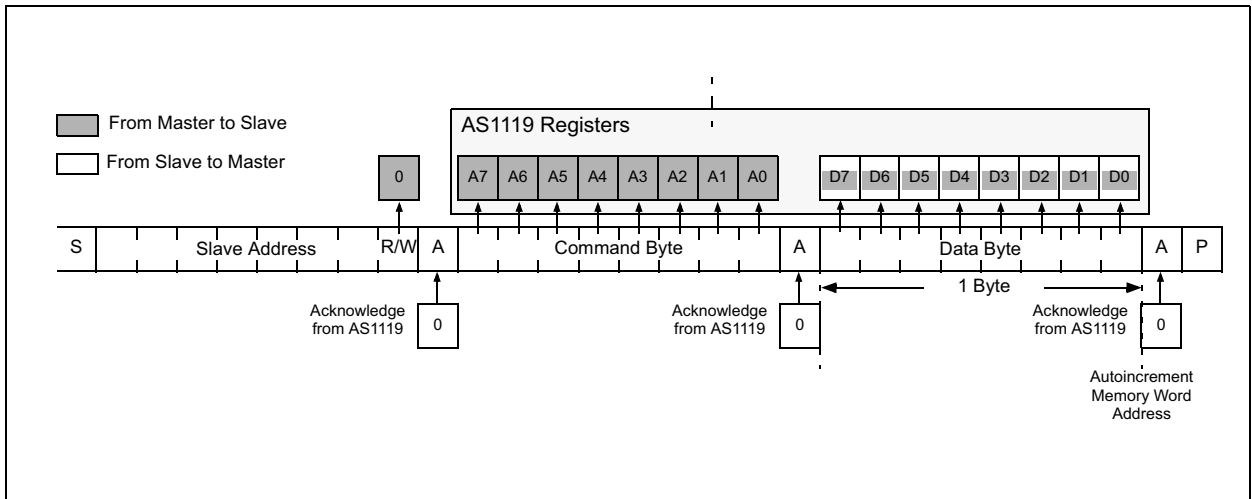


Figure 25:
Setting the Pointer to a Address Register to Select a Data Register for a Read Operation

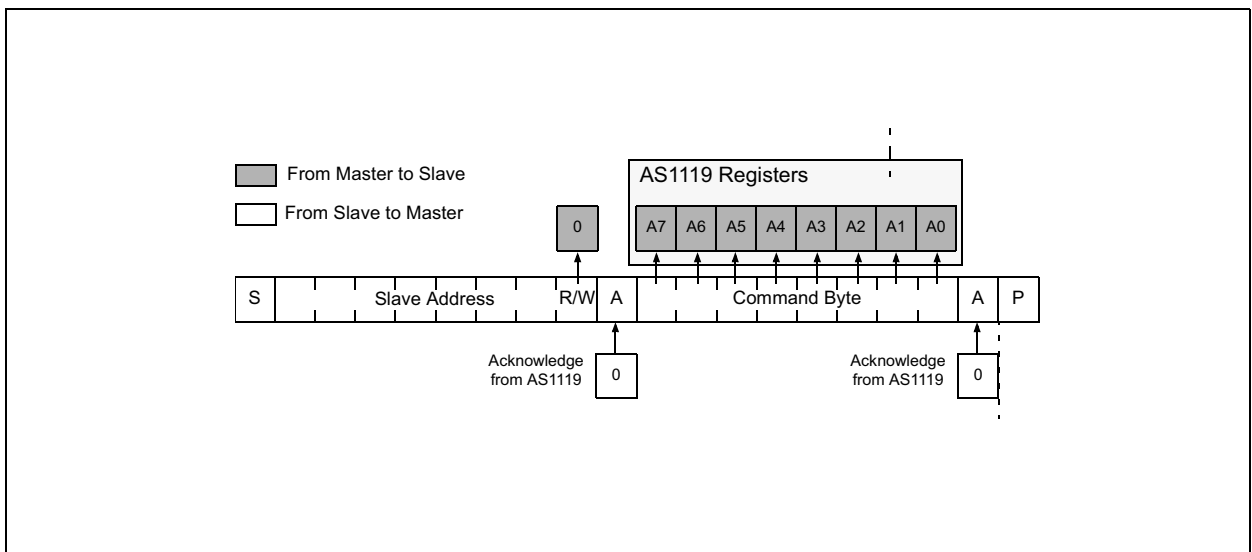
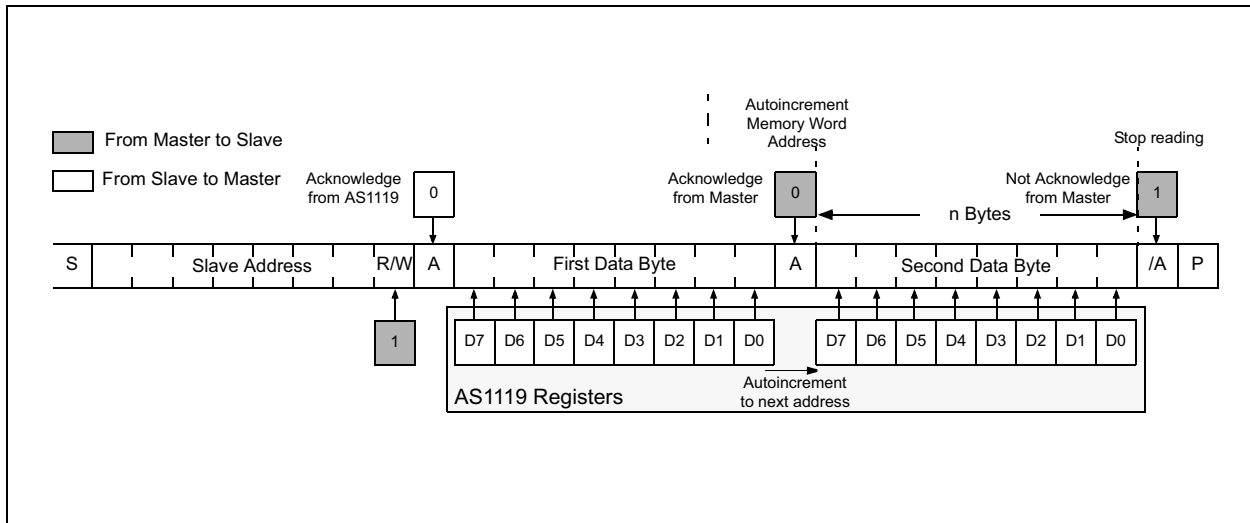


Figure 26:
Reading n Bytes from AS1119



Initial Power-Up

On initial power-up, the AS1119 registers are reset to their default values, the display is blanked, and the device goes into shutdown mode. At this time, all registers should be programmed for normal operation.

Note(s): The default settings enable only scanning of one digit; the internal decoder is disabled and the Intensity Control Register (see [Figure 32](#)) and (see [Figure 37](#)) is set to the minimum values.

Shutdown Mode

The AS1119 device features two different shutdown modes. A software shutdown via shutdown register (see [Shutdown Register \(0x0A\)](#)) and a hardware shutdown via the RSTN pin.

The software shutdown disables all LEDs and stops the internal operation of the logic. A shutdown mode via the RSTN pin additionally powers down the power-on-reset (PO) of the device. In this shutdown mode the AS1119 consumes only 100nA (typ.).



Register Description

Register Selection

Within this register the access to one of the RAM sections or to the Control selected this section is valid as long as an other section is selected.

Figure 27:
Register Selection Address Map

Register Section	Address									Data						
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2
NOP	253	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0
Data Frame 0										1	0	0	0	0	0	0
Data Frame 1										2	0	0	0	0	0	0
Data Frame 2										3	0	0	0	0	0	0
Data Frame 3										4	0	0	0	0	0	1
Data Frame 4										5	0	0	0	0	0	1
Data Frame 5										6	0	0	0	0	0	1
Control Register										11	0	0	0	0	1	0

Data Definition of Single Frames

One frame consists of 2 blocks (a 8 × 9 LED-matrix) or 3 blocks (a 5 × 6 LED-matrix). This configuration is set in the AS1119 config register (see [Figure 43](#)).

In the internal DPRAM of the device 6 frames can be stored. For each frame the following parameters have to be stored.

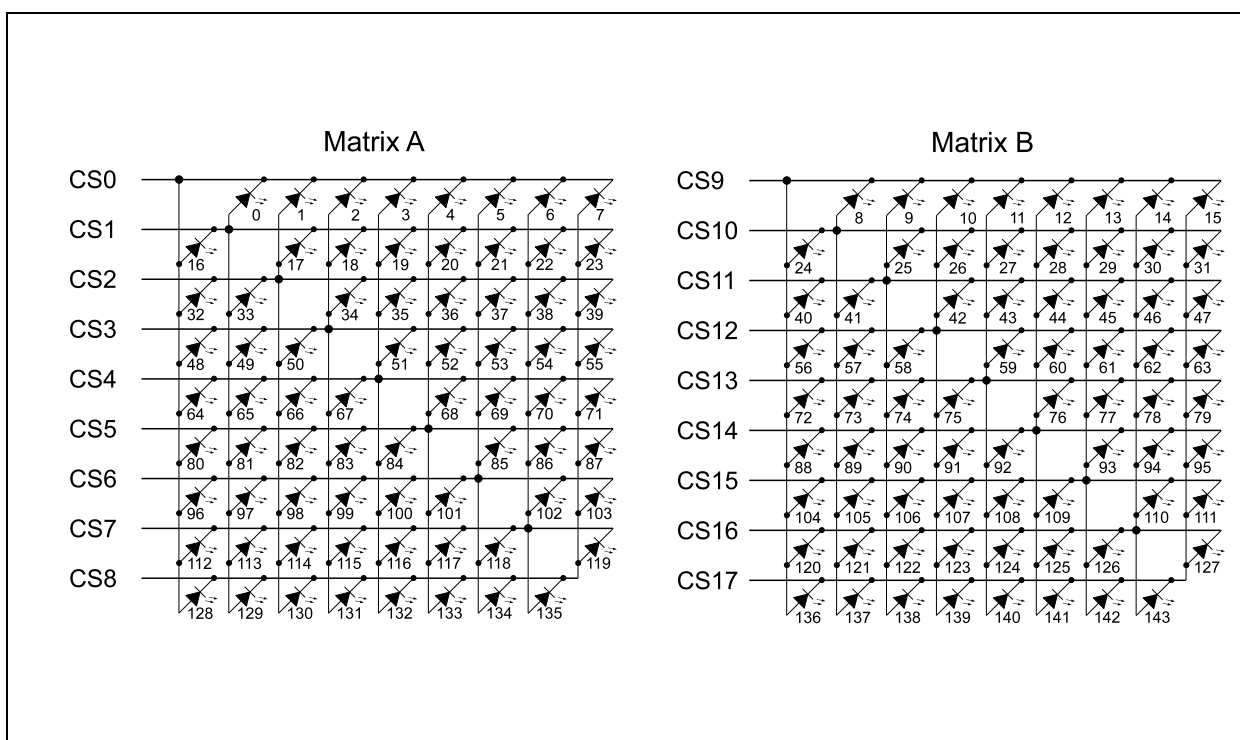
- LED is ON or OFF.
- LED is steady ON or blinking.
- The intensity of every single LED can be set via a 8 bits PWM.

Note(s): After power-up the data in the DPRAM is undefined (either '0' or '1').

2 Blocks with 8x9 LED Matrix

The AS1119 can be configured to control two separated blocks of LEDs matrixes. This must be set via the bit D0 in the AS1119 config register (see [Figure 43](#)).

Figure 28:
8x9 LED Matrix with Two Blocks



The address structure (as shown in [Figure 29](#)) within on frame is always the same independent which frame was selected via the register selection ([Register Selection Address Map](#)).

Figure 29:
Dataframe Address Structure for 2 Matrixes

		Addresses Within Frame (HEX code)					
Current Source		On / Off		Blink		Intensity	
Matrix A	Matrix B	Matrix A	Matrix B	Matrix A	Matrix B	Matrix A	Matrix B
CS0	CS9	0x00	0x01	0x12	0x13	0x24-0x2B	0x2C-0x33
CS1	CS10	0x02	0x03	0x14	0x15	0x34-0x3B	0x3C-0x43
CS2	CS11	0x04	0x05	0x16	0x17	0x44-0x4B	0x4C-0x53
CS3	CS12	0x06	0x07	0x18	0x19	0x54-0x5B	0x5C-0x63
CS4	CS13	0x08	0x09	0x1A	0x1B	0x64-0x6B	0x6C-0x73
CS5	CS14	0x0A	0x0B	0x1C	0x1D	0x74-0x7B	0x7C-0x83
CS6	CS15	0x0C	0x0D	0x1E	0x1F	0x84-0x8B	0x8C-0x93
CS7	CS16	0x0E	0x0F	0x20	0x21	0x94-0x9B	0x9C-0xA3
CS8	CS17	0x10	0x11	0x22	0x23	0xA4-0xAB	0xAC-0xB3

In [Figure 30](#) it's described which databit represents which LED in the matrix no LED is On. A '1' puts the LED On.

Figure 30:
LEDs ON/OFF Register Format for 2 Matrices Setup

Matrix	Current Source	Address									Data			
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4
A	CS0	0x00	0	0	0	0	0	0	0	0	LED7	LED6	LED5	LED4
B	CS9	0x01	0	0	0	0	0	0	0	1	LED15	LED14	LED13	LED12
A	CS1	0x02	0	0	0	0	0	0	1	0	LED23	LED22	LED21	LED20
B	CS10	0x03	0	0	0	0	0	0	1	1	LED31	LED30	LED29	LED28
A	CS2	0x04	0	0	0	0	0	1	0	0	LED39	LED38	LED37	LED36
B	CS11	0x05	0	0	0	0	0	1	0	1	LED47	LED46	LED45	LED44
A	CS3	0x06	0	0	0	0	0	1	1	0	LED55	LED54	LED53	LED52
B	CS12	0x07	0	0	0	0	0	1	1	1	LED63	LED62	LED61	LED60
A	CS4	0x08	0	0	0	0	1	0	0	0	LED71	LED70	LED69	LED68
B	CS13	0x09	0	0	0	0	1	0	0	1	LED79	LED78	LED77	LED76
A	CS5	0x0A	0	0	0	0	1	0	1	0	LED87	LED86	LED85	LED84
B	CS14	0x0B	0	0	0	0	1	0	1	1	LED95	LED94	LED93	LED92
A	CS6	0x0C	0	0	0	0	1	1	0	0	LED103	LED102	LED101	LED100
B	CS15	0x0D	0	0	0	0	1	1	0	1	LED111	LED110	LED109	LED108
A	CS7	0x0E	0	0	0	0	1	1	1	0	LED119	LED118	LED117	LED116



Matrix	Current Source	Address									Data			
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4
B	CS16	0x0F	0	0	0	0	1	1	1	1	LED127	LED126	LED125	LED124
A	CS8	0x10	0	0	0	1	0	0	0	0	LED135	LED134	LED133	LED132
B	CS17	0x11	0	0	0	1	0	0	0	1	LED143	LED142	LED141	LED140

In the blink register (see [Figure 31](#)) every single LED can be set to blink. The register (see [Display Option Register \(0x03\)](#)).

Figure 31:
LEDs Blink Register Format for 2 Matrixes Setup

Matrix	Current Source	Address									Data			
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4
A	CS0	0x12	0	0	0	1	0	0	1	0	LED7	LED6	LED5	LED4
B	CS9	0x13	0	0	0	1	0	0	1	1	LED15	LED14	LED13	LED12
A	CS1	0x14	0	0	0	1	0	1	0	0	LED23	LED22	LED21	LED20
B	CS10	0x15	0	0	0	1	0	1	0	1	LED31	LED30	LED29	LED28
A	CS2	0x16	0	0	0	1	0	1	1	0	LED39	LED38	LED37	LED36
B	CS11	0x17	0	0	0	1	0	1	1	1	LED47	LED46	LED45	LED44
A	CS3	0x18	0	0	0	1	1	0	0	0	LED55	LED54	LED53	LED52
B	CS12	0x19	0	0	0	1	1	0	0	1	LED63	LED62	LED61	LED60
A	CS4	0x1A	0	0	0	1	1	0	1	0	LED71	LED70	LED69	LED68

AS1119 – Register Description

Matrix	Current Source	Address									Data			
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4
B	CS13	0x1B	0	0	0	1	1	0	1	1	LED79	LED78	LED77	LED76
A	CS5	0x1C	0	0	0	1	1	1	0	0	LED87	LED86	LED85	LED84
B	CS14	0x1D	0	0	0	1	1	1	0	1	LED95	LED94	LED93	LED92
A	CS6	0x1E	0	0	0	1	1	1	1	0	LED103	LED102	LED101	LED100
B	CS15	0x1F	0	0	1	1	1	1	1	1	LED111	LED110	LED109	LED108
A	CS7	0x20	0	0	1	0	0	0	0	0	LED119	LED118	LED117	LED116
B	CS16	0x21	0	0	1	0	0	0	0	1	LED127	LED126	LED125	LED124
A	CS8	0x22	0	0	1	0	0	0	1	0	LED135	LED134	LED133	LED132
B	CS17	0x23	0	0	1	0	0	0	1	1	LED143	LED142	LED141	LED140

In the intensity register (see [Figure 32](#)) the brightness of every single LED c



Figure 32:
LEDs Intensity Register Format for 2 Matrices Setup

Matrix	Current Source		Address									D7	D6	D5
			HEX	A7	A6	A5	A4	A3	A2	A1	A0			
A	CS0	LED0	0x24	0	0	1	0	0	1	0	0	255 steps for		
		LED1	0x25	0	0	1	0	0	1	0	1			
		LED2	0x26	0	0	1	0	0	1	1	0			
		LED3	0x27	0	0	1	0	0	1	1	1			
		LED4	0x28	0	0	1	0	1	0	0	0			
		LED5	0x29	0	0	1	0	1	0	0	1			
		LED6	0x2A	0	0	1	0	1	0	1	0			
		LED7	0x2B	0	0	1	0	1	0	1	1			
B	CS9	LED8	0x2C	0	0	1	0	1	1	0	0			
		LED9	0x2D	0	0	1	0	1	1	0	1			
		LED10	0x2E	0	0	1	0	1	1	1	0			
		LED11	0x2F	0	0	1	0	1	1	1	1			
		LED12	0x30	0	0	1	1	0	0	0	0			
		LED13	0x31	0	0	1	1	0	0	0	1			
		LED14	0x32	0	0	1	1	0	0	1	0			
		LED15	0x33	0	0	1	1	0	0	1	1			

AS1119 – Register Description

Matrix	Current Source		Address									D7	D6	D5
			HEX	A7	A6	A5	A4	A3	A2	A1	A0			
A	CS1	LED16	0x34	0	0	1	1	0	1	0	0	255 steps fo		
		LED17	0x35	0	0	1	1	0	1	0	1			
		LED18	0x36	0	0	1	1	0	1	1	0			
		LED19	0x37	0	0	1	1	0	1	1	1			
		LED20	0x38	0	0	1	1	1	0	0	0			
		LED21	0x39	0	0	1	1	1	0	0	1			
		LED22	0x3A	0	0	1	1	1	0	1	0			
		LED23	0x3B	0	0	1	1	1	0	1	1			
B	CS10	LED24	0x3C	0	0	1	1	1	1	0	0			
		LED25	0x3D	0	0	1	1	1	1	0	1			
		LED26	0x3E	0	0	1	1	1	1	1	0			
		LED27	0x3F	0	0	1	1	1	1	1	1			
		LED28	0x40	0	1	0	0	0	0	0	0			
		LED29	0x41	0	1	0	0	0	0	0	1			
		LED30	0x42	0	1	0	0	0	0	1	0			
		LED31	0x43	0	1	0	0	0	0	1	1			



Matrix	Current Source		Address									D7	D6	D5
			HEX	A7	A6	A5	A4	A3	A2	A1	A0			
A	CS2	LED32	0x44	0	1	0	0	0	0	1	0	0	255 steps fo	
		LED33	0x45	0	1	0	0	0	0	1	0	1		
		LED34	0x46	0	1	0	0	0	0	1	1	0		
		LED35	0x47	0	1	0	0	0	0	1	1	1		
		LED36	0x48	0	1	0	0	0	1	0	0	0		
		LED37	0x49	0	1	0	0	0	1	0	0	1		
		LED38	0x4A	0	1	0	0	0	1	0	1	0		
		LED39	0x4B	0	1	0	0	0	1	0	1	1		
B	CS11	LED40	0x4C	0	1	0	0	0	1	1	0	0		
		LED41	0x4D	0	1	0	0	0	1	1	0	1		
		LED42	0x4E	0	1	0	0	0	1	1	1	0		
		LED43	0x4F	0	1	0	0	0	1	1	1	1		
		LED44	0x50	0	1	0	0	1	0	0	0	0		
		LED45	0x51	0	1	0	0	1	0	0	0	1		
		LED46	0x52	0	1	0	0	1	0	0	1	0		
		LED47	0x53	0	1	0	0	1	0	0	1	1		

AS1119 – Register Description

Matrix	Current Source		Address									D7	D6	D5
			HEX	A7	A6	A5	A4	A3	A2	A1	A0			
A	CS8	LED128	0xA4	1	0	1	0	0	1	0	0	255 steps fo		
		LED129	0xA5	1	0	1	0	0	1	0	1			
		LED130	0XA6	1	0	1	0	0	1	1	0			
		LED131	0XA7	1	0	1	0	0	1	1	1			
		LED132	0XA8	1	0	1	0	1	0	0	0			
		LED133	0XA9	1	0	1	0	1	0	0	1			
		LED134	0XAA	1	0	1	0	1	0	1	0			
		LED135	0XAB	1	0	1	0	1	0	1	1			
B	CS17	LED136	0XAC	1	0	1	0	1	1	0	0			
		LED137	0XAD	1	0	1	0	1	1	0	1			
		LED138	0XAE	1	0	1	0	1	1	1	0			
		LED139	0XAF	1	0	1	0	1	1	1	1			
		LED140	0XB0	1	0	1	1	0	0	0	0			
		LED141	0XB1	1	0	1	1	0	0	0	1			
		LED142	0XB2	1	0	1	1	0	0	1	0			
		LED143	0XB3	1	0	1	1	0	0	1	1			

3 Blocks with 5x6 LED Matrix

The AS1119 can be configured to control three separated blocks of LEDs matrixes. This must be set via the bit D0 in the AS1119 config register (see [AS1119 Config Register \(0x04\)](#)).

Figure 33:
5x6 LED Matrix with 3 Matrixes

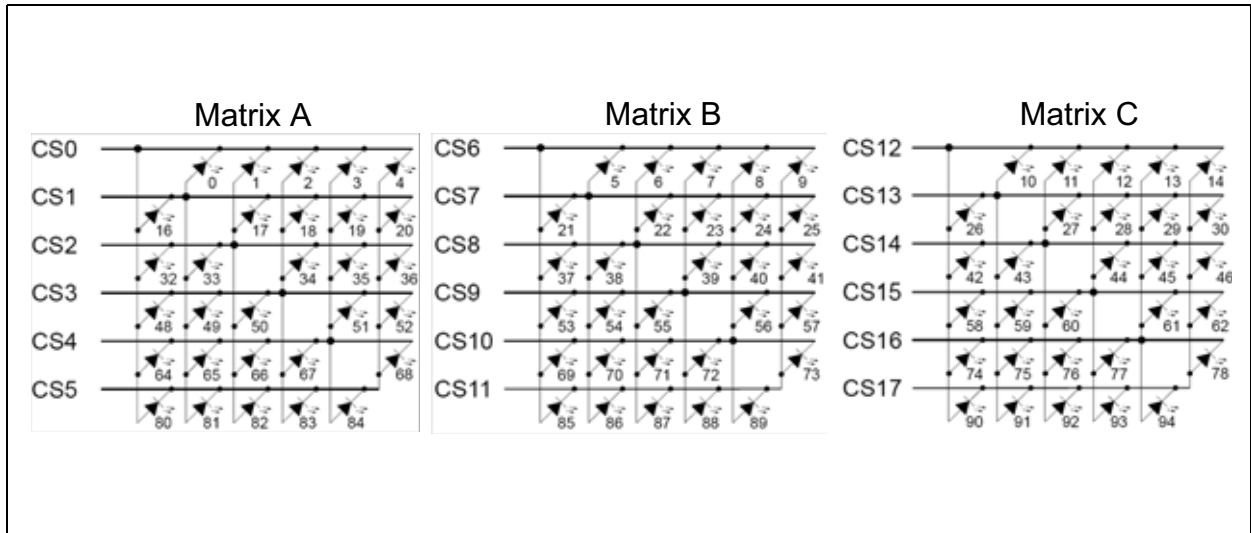


Figure 34:
Dataframe Address Structure for 3 Matrixes

			Addresses Within Frame (HEX code)									
Current Source			On / Off			Blink			Intensity			
Matrix			Matrix			Matrix			Matrix			
A	B	C	A	B	C	A	B	C	A	B	C	
CS0	CS6	CS12	0x00	0x01		0x12	0x13		0x24-0x2B		0x2C-0x33	
CS1	CS7	CS13	0x02	0x03		0x14	0x15		0x34-0x3B		0x3C-0x43	
CS2	CS8	CS14	0x04	0x05		0x16	0x17		0x44-0x4B		0x4C-0x53	
CS3	CS9	CS15	0x06	0x07		0x18	0x19		0x54-0x5B		0x5C-0x63	
CS4	CS10	CS16	0x08	0x09		0x1A	0x1B		0x64-0x6B		0x6C-0x73	
CS5	CS11	CS17	0x0A	0x0B		0x1C	0x1D		0x74-0x7B		0x7C-0x83	

In [Figure 35](#) it's described which databit represents which LED in the matrix. Per default all databits are '0', meaning no LED is on. A '1' puts the LED On.

Note(s): LED A01 is the first LED of the Current Source 0 in the Matrix A. LED B01 is the first LED of the Current Source 6 in the Matrix B. and so on.

Figure 35:
LEDs ON/OFF Register Format for 3 Matrices Setup

Current Source	Address									Data			
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4
CS0, CS6, CS12	0x00	0	0	0	0	0	0	0	0	LED7	LED6	LED5	LED4
	0x01	0	0	0	0	0	0	0	1	X	LED14	LED13	LED12
CS1, CS7, CS13	0x02	0	0	0	0	0	0	1	0	LED23	LED22	LED21	LED20
	0x03	0	0	0	0	0	0	1	1	X	LED30	LED29	LED28
CS2, CS8, CS14	0x04	0	0	0	0	0	1	0	0	LED39	LED38	LED37	LED36
	0x05	0	0	0	0	0	1	0	1	X	LED46	LED45	LED44
CS3, CS9, CS15	0x06	0	0	0	0	0	1	1	0	LED55	LED54	LED53	LED52
	0x07	0	0	0	0	0	1	1	1	X	LED62	LED61	LED60
CS4, CS10, CS16	0x08	0	0	0	0	1	0	0	0	LED71	LED70	LED69	LED68
	0x09	0	0	0	0	1	0	0	1	X	LED78	LED77	LED76
CS5, CS11, CS17	0x0A	0	0	0	0	1	0	1	0	LED87	LED86	LED85	LED84
	0x0B	0	0	0	0	1	0	1	1	X	LED94	LED93	LED92



In the blink register (see [Figure 36](#)) every single LED can be set to blink. The register (see [Display Option Register \(0x03\)](#)).

Figure 36:
LEDs Blink Register Format for 3 Matrices Setup

Current Source	Address									Data			
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4
CS0, CS6, CS12	0x12	0	0	0	0	0	0	0	0	LED7	LED6	LED5	LED4
	0x13	0	0	0	0	0	0	0	1	X	LED14	LED13	LED12
CS1, CS7, CS13	0x14	0	0	0	0	0	0	1	0	LED23	LED22	LED21	LED20
	0x15	0	0	0	0	0	0	1	1	X	LED30	LED29	LED28
CS2, CS8, CS14	0x16	0	0	0	0	0	1	0	0	LED39	LED38	LED37	LED36
	0x17	0	0	0	0	0	1	0	1	X	LED46	LED45	LED44
CS3, CS9, CS15	0x18	0	0	0	0	0	1	1	0	LED55	LED54	LED53	LED52
	0x19	0	0	0	0	0	1	1	1	X	LED62	LED61	LED60
CS4, CS10, CS16	0x1A	0	0	0	0	1	0	0	0	LED71	LED70	LED69	LED68
	0x1B	0	0	0	0	1	0	0	1	X	LED78	LED77	LED76
CS5, CS11, CS17	0x1C	0	0	0	0	1	0	1	0	LED87	LED86	LED85	LED84
	0x1D	0	0	0	0	1	0	1	1	X	LED94	LED93	LED92

In the intensity register (see [Figure 37](#)) the brightness of every single LED c

Figure 37:
LEDs Intensity Register Format for 3 Matrixes Setup

Matrix	Current Source		Address									D7	D6	D5
			HEX	A7	A6	A5	A4	A3	A2	A1	A0			
A	CS0	LED0	0x24	0	0	1	0	0	1	0	0	255 steps fo		
		LED1	0x25	0	0	1	0	0	1	0	1			
		LED2	0x26	0	0	1	0	0	1	1	0			
		LED3	0x27	0	0	1	0	0	1	1	1			
		LED4	0x28	0	0	1	0	1	0	0	0			
B	CS6	LED5	0x29	0	0	1	0	1	1	0	0			
		LED6	0x2A	0	0	1	0	1	1	0	1			
		LED7	0x2B	0	0	1	0	1	1	1	0			
		LED8	0x2C	0	0	1	0	1	1	1	1			
		LED9	0x2D	0	0	1	1	0	0	0	0			
C	CS12	LED10	0x2E	0	0	1	0	1	1	0	0			
		LED11	0x2F	0	0	1	0	1	1	0	1			
		LED12	0x30	0	0	1	0	1	1	1	0			
		LED13	0x31	0	0	1	0	1	1	1	1			
		LED14	0x32	0	0	1	1	0	0	0	0			



Matrix	Current Source		Address									D7	D6	D5
			HEX	A7	A6	A5	A4	A3	A2	A1	A0			
A	CS1	LED16	0x34	0	0	1	1	0	1	0	0	255 steps fo		
		LED17	0x35	0	0	1	1	0	1	0	1			
		LED18	0x36	0	0	1	1	0	1	1	0			
		LED19	0x37	0	0	1	1	0	1	1	1			
		LED20	0x38	0	0	1	1	0	0	0	0			
B	CS7	LED21	0x39	0	0	1	1	1	0	0	1			
		LED22	0x3A	0	0	1	1	1	0	1	0			
		LED23	0x3B	0	0	1	1	1	0	1	1			
		LED24	0x3C	0	0	1	1	1	1	0	0			
		LED25	0x3D	0	0	1	1	1	1	0	1			
C	CS13	LED26	0x3E	0	0	1	1	1	1	1	0			
		LED27	0x3F	0	0	1	1	1	1	1	1			
		LED28	0x40	0	1	0	0	0	0	0	0			
		LED29	0x41	0	1	0	0	0	0	0	1			
		LED30	0x42	0	1	0	0	0	0	1	0			



Matrix	Current Source		Address									D7	D6	D5
			HEX	A7	A6	A5	A4	A3	A2	A1	A0			
A	CS2	LED32	0x44	0	1	0	0	0	0	1	0	0	255 steps fo	
		LED33	0x45	0	1	0	0	0	0	1	0	1		
		LED34	0x46	0	1	0	0	0	0	1	1	0		
		LED35	0x47	0	1	0	0	0	0	1	1	1		
		LED36	0x48	0	1	0	0	0	1	0	0	0		
B	CS8	LED37	0x49	0	1	0	0	0	1	0	0	1		
		LED38	0x4A	0	1	0	0	0	1	0	1	0		
		LED39	0x4B	0	1	0	0	0	1	0	1	1		
		LED40	0x4C	0	1	0	0	0	1	1	0	0		
		LED41	0x4D	0	1	0	0	0	1	1	0	1		
C	CS14	LED42	0x4E	0	1	0	0	0	1	1	1	0		
		LED43	0x4F	0	1	0	0	0	1	1	1	1		
		LED44	0x50	0	1	0	1	0	0	0	0	0		
		LED45	0x51	0	1	0	1	0	0	0	0	1		
		LED46	0x52	0	1	0	1	0	0	0	1	0		
.....														



Matrix	Current Source		Address									D7	D6	D5
			HEX	A7	A6	A5	A4	A3	A2	A1	A0			
A	CS5	LED80	0xA4	1	0	1	0	0	1	0	0	255 steps fo		
		LED81	0xA5	1	0	1	0	0	1	0	1			
		LED82	0xA6	1	0	1	0	0	1	1	0			
		LED83	0xA7	1	0	1	0	0	1	1	1			
		LED84	0xA8	1	0	1	0	1	0	0	0			
B	CS11	LED85	0xA9	1	0	1	0	1	0	0	1			
		LED86	0xAA	1	0	1	0	1	0	1	0			
		LED87	0xAB	1	0	1	0	1	0	1	1			
		LED88	0xAC	1	0	1	0	1	1	0	0			
		LED89	0xAD	1	0	1	0	1	1	0	1			
C	CS17	LED90	0xAE	1	0	1	0	1	1	1	0			
		LED91	0xAF	1	0	1	0	1	1	1	1			
		LED92	0xB0	1	0	1	1	0	0	0	0			
		LED93	0xB1	1	0	1	1	0	0	0	1			
		LED94	0xB2	1	0	1	1	0	0	1	0			

Control-Registers

The AS1119 devices contain 13 control-registers which are listed in [Figure 38](#). All registers are selected using a 8-bit address word, and communication is done via the serial interface. Select the Control Register via the Register Selection (see [Figure 27](#)).

Figure 38:
Control Register Address Map

Register Name	HEX	Address								Register Data
		A7	A6	A5	A4	A3	A2	A1	A0	D7:D0
Frame address	0x00	0	0	0	0	0	0	0	0	(see Figure 39)
Frame play	0x01	0	0	0	0	0	0	0	1	(see Figure 40)
Frame time	0x02	0	0	0	0	0	0	1	0	(see Figure 41)
Display option	0x03	0	0	0	0	0	0	1	1	(see Figure 42)
AS1119 config	0x04	0	0	0	0	0	1	0	0	(see Figure 43)
Current source matrix A	0x05	0	0	0	0	0	1	0	1	(see Figure 44)
Current source matrix B	0x06	0	0	0	0	0	1	1	0	
Current source matrix C	0x07	0	0	0	0	0	1	1	1	
Chare pump config	0x08	0	0	0	0	1	0	0	0	(see Figure 45)
Open/short test	0x09	0	0	0	0	1	0	0	1	(see Figure 46)
Shutdown	0x0A	0	0	0	0	1	0	1	0	(see Figure 47)
I ² C Interface monitoring	0x0B	0	0	0	0	1	0	1	1	(see Figure 48)
Open/Short status	0x0C	0	0	0	0	1	1	0	0	(see Figure 49)
AS1119 status	0x0D	0	0	0	0	1	1	0	1	(see Figure 50)

Frame Address Register (0x00)

In this register it must be set if a picture or a movie is to display on the LED matrix. Also the start address of the movie or the picture which should be displayed must be set within this register. The default setting of this register is 0x00.

Figure 39:
Frame Address Register Format

0x00 Frame Address Register				
Bit	Bit Name	Default	Access	Bit Description
7	Play Movie	0	R/W	0: No movie 1: Play movie
6	Display Picture	0	R/W	0: No picture 1: Display picture
5:3	Start Address for movie	000	R/W	000: Frame 0 001: Frame 1 010: Frame 2 011: Frame 3 100: Frame 4 101: Frame 5
2:0	Address of Picture	000	R/W	000: Frame 0 001: Frame 1 010: Frame 2 011: Frame 3 100: Frame 4 101: Frame 5

Note(s):

1. If bit 6 and 7 are set to '1' the AS1119 will play the movie first and then the picture will be displayed.

Frame Play Register (0x01)

Within this register two movie play options can be set. Per default this register is set to 0x00.

- The number of frames which are displayed in one movie.
- The number of loops to play in a movie.

Figure 40:
Frame Play Register Format

0x01 Frame Play Register				
Bit	Bit Name	Default	Access	Bit Description
7:6	-	00	n/a	
5:3	Number of loops played in one movie	000	R/W	000: No loop 001: 1 loop 010: 2 loops 011: 3 loops 100: 4 loops 101: 5 loops 110: 6 loops 111: Play endless
2:0	Number of frames to played in a movie	000	R/W	000: 1 frame 001: 2 frames 010: 3 frames 011: 4 frames 100: 5 frames 101: 6 frames

Note(s):

1. To stop a movie in *play endless mode*, bits D5:D3 have to be set to a value between 000 to 110.

Frame Time Register (0x02)

Every single frame in a movie is displayed for a certain time before the next frame is displayed. This time can be set within this register with 4 bits. The stated values in Figure 41 are typical values. Per default this register is set to 0x00.

Figure 41:
Frame Time Register Format

0x02 Frame Time Register				
Bit	Bit Name	Default	Access	Bit Description
7:4	-	00	n/a	
3:0	Delay between frame change in a movie	000	R/W	0000: Play frame only one time 0001: 32.5ms 0010: 65ms 0011: 97.5ms 0100: 130ms 0101: 162.5ms 0110: 195ms 0111: 227.5ms 1000: 260ms 1001: 292.5ms 1010: 325ms 1011: 357.5ms 1100: 390ms 1101: 422.5ms 1110: 455ms 1111: 487.5ms

Display Option Register (0x03)

With the scan-limit it can be controlled how many digits are displayed in each matrix. When all 18 digits in the 2 matrix configuration are displayed, the display scan rate is 430Hz (typ.). If the number of digits to display is reduced, the update frequency is increased. Per default this register is set to 0x07.

Figure 42:
Display Option Register Format

0x03 Display Option Register						
Bit	Bit Name	Default	Access	Bit Description		
7	-	0	n/a			
6	Intensity setting	0	R/W	0: Use intensity setting of frame 0 for all other frames 1: Set the intensity of each frame independently		
5	Start with blink	0	R/W	0: Start blinking with LED On 1: Start blinking with LED Off		
4	Blink period	0	R/W	0: 1.5s 1: 3s		
3:0	Number of displayed current sources in one frame (scan-limit)	0111	R/W	2 Matrix setting		
				Matrix A	Matrix B	
				0000: CS0 0001: CS0 to CS1 0010: CS0 to CS2 0011: CS0 to CS3 0100: CS0 to CS4 0101: CS0 to CS5 0110: CS0 to CS6 0111: CS0 to CS7 1000: CS0 to CS8	0000: CS9 0001: CS9 to CS10 0010: CS9 to CS11 0011: CS9 to CS12 0100: CS9 to CS13 0101: CS9 to CS14 0110: CS9 to CS15 0111: CS9 to CS16 1000: CS9 to CS17	
				3 Matrixes setting		
				Matrix A	Matrix B	
				0000: CS0 0001: CS0 to CS1 0010: CS0 to CS2 0011: CS0 to CS3 0100: CS0 to CS4 0101: CS0 to CS5	0000: CS6 0001: CS6 to CS7 0010: CS6 to CS8 0011: CS6 to CS9 0100: CS6 to CS10 0101: CS6 to CS11	0000: CS12 0001: CS12 to CS13 0010: CS12 to CS14 0011: CS12 to CS15 0100: CS12 to CS16 0101: CS12 to CS17

AS1119 Config Register (0x04)

In this register the configuration of the charge pumps is set to 2 or 3 blocks. The direction of the SYNC_IN/SYNC_OUT pin (input or output) is also set. Per default this register is set to 0x00.

Figure 43:
AS1119 Config Register Format

0x04 AS1119 Config Register				
Bit	Bit Name	Default	Access	Bit Description
7:3	-	00000	n/a	
2:1	Sync	00	R/W	00: Internal oscillator is system-clk. No synchronisation on pin B6. Tie pin to high or low. 01: Internal oscillator is system-clk. System-clk is available on pin B6 for synchronization. (output) 10: Internal oscillator is disabled. Pin B6 is used as clk input for system-clk. 11: Do not use
0	Matrix configuration	0	R/W	0: 3 matrixes (a 5x6 LED-Matrix) 1: 2 matrixes (a 8x9 LED-Matrix)

Current Source Block A, B, C Registers (0x05, 0x06, 0x07)

Within this registers the current for every single LED in one block can be set from 0mA to 31mA in 255 steps (8 bits). Per default this register is set to 0x00.

Figure 44:
Current Source Register Format

Current Source Registers				
Bit	Bit Name	Default	Access	Bit Description
Address 0x05				
7:0	Analog Current Matrix A	0000000	R/W	00000000: 0mA 11111111: 31mA
Address 0x06				
7:0	Analog Current Matrix B	0000000	R/W	00000000: 0mA 11111111: 31mA
Address 0x07				
7:0	Analog Current Matrix C	0000000	R/W	00000000: 0mA 11111111: 31mA

Charge Pump Config Register (0x08)

In this register the characteristics of the Charge Pump can be set. By the use of the charge pump (bit 0) the supply voltage for the LEDs can be boosted to 1.5- or 2-times of the device supply (V_{DD}), if required. Additionally bit1 offers the option to check periodically if the LED supply can be reduced again during operation. This period is defined by bit 4:2.

Alternatively, the LED supply can be (re)set to V_{DD} by disabling the charge pump for a short time. In this case the period can be defined by user (application). Per default this register is set to 0x1E.

Figure 45:
AS1119 Charge Pump Config Register Format

0x08 Charge Pump Config Register				
Bit	Bit Name	Default	Access	Bit Description
7:5	-	000	n/a	
4:2	Timeframe for reduce supply test	111	R/W	000: 0.3s 001: 0.5s 010: 0.8s 011: 1.0s 100: 1.3s 101: 1.6s 110: 1.8s 111: 2.1s
1	Reduce supply option	1	R/W	0: Reduce supply option Off 1: Reduce supply option On
0	Charge Pump	0	R/W	0: Charge Pump disable 1: Charge Pump enable

Open/Short Test Register (0x09)

The AS1119 can detect open and shorted LEDs. To start this test the according bits have to be set. The result of the open/short test is written in the Open/Short startup register (see [Figure 46](#)). The default setting of this register is 0x00.

Figure 46:
Open/Short Test Register Format

0x09 Open/Short Test Register				
Bit	Bit Name	Default	Access	Bit Description
7:2	-	000000	n/a	
1	Full Matrix	0	R/W	0: All LED's are available in the matrixes 1: Not all LED's are available in the matrixes
0	Error detection	0	R/W	0: Start test 1: No test

The Open/Short test is only checking LEDs which are defined as ON in the Data Frame Registers [Figure 30](#) or [Figure 35](#). With the bit1 (Full Matrix) all LEDs of the matrixes will be defined as ON and will be tested independently from the content of the Data Frame Register. The function of bit1 is only available during the open/short test and not during normal operation.

Shutdown Register (0x0A)

The default setting of this register is 0x00. To get the AS1119 operational the bit D0 has to be set to '1'.

Figure 47:
Shutdown Register Format

0x0A Shutdown Register				
Bit	Bit Name	Default	Access	Bit Description
7:1	-	0000000	n/a	
0	shutdown	0	R/W	0: Shutdown 1: Normal operation

I²C Interface Monitoring Register (0x0B)

This register is used to monitor the activity on the I²C bus. If a deadlock situation occurs (e.g. the bus SDA pin is pulled to low and no communication is possible) the chip will reset the I²C interface and the master is able to start the communication again. The time window for the reset of the interface of the AS1119 can be set via 7 bits from 256µs to 33ms. The default setting of this register is 0xFF.

Figure 48:
I²C Interface Monitoring Register Format

0x0B I ² C Interface Monitoring Register				
Bit	Bit Name	Default	Access	Bit Description
7:2	Time out window	1111111	R/W	0 to 127 => 1 to 128 × 256µs 0000000: 256µs 1111111: 32.7ms
0	I ² C Monitor	1	R/W	0: I ² C monitoring Off 1: I ² C monitoring On

Open/Short Status Register (0x0C)

This is a read only register. Within this register the result of the open/short test can be read out. It's also stated if the test is completed or still running. The default setting of this register is 0x00.

Figure 49:
Open/Short Status Register Format

0x0C Open/Short Status Register				
Bit	Bit Name	Default	Access	Bit Description
7	-	0	n/a	
6	status	0	R	0: No test 1: Test ongoing
5	short test result Matrix C	0	R	0: No error detected 1: Short in Matrix C
4	short test result Matrix B	0	R	0: No error detected 1: Short in Matrix B
3	short test result Matrix A	0	R	0: No error detected 1: Short in Matrix A
2	open test result Matrix C	0	R	0: No error detected 1: Open in Matrix C

0x0C Open/Short Status Register				
Bit	Bit Name	Default	Access	Bit Description
1	open test result Matrix B	0	R	0: No error detected 1: Open in Matrix B
0	open test result Matrix A	0	R	0: No error detected 1: Open in Matrix A

AS1119 Status Register (0x0D)

This is a read only register. From this register the actual status of the AS1119 can be read out. The default setting of this register is 0x00. After a read command the bits 5:4 are set to '0' again automatically.

Figure 50:
AS1119 Status Register Format

0x0D AS1119 Status Register				
Bit	Bit Name	Default	Access	Bit Description
7	-	0	n/a	
6	Movie status		R	0: No movie is playing 1: One movie is playing
5:4	Interrupt	00	R	00: No Interrupt triggered 01: POR triggered an interrupt ⁽¹⁾ 10: I ² C monitor triggered an interrupt 11: Both (I ² C and POR) triggered an interrupt
3:0	actual displayed frame	000	R	000: Frame 0 001: Frame 1 010: Frame 2 011: Frame 3 100: Frame 4 101: Frame 5

Note(s):

1. The power-on reset is part of the start sequence, hence after start-up this bit is also set.

Package Drawings & Markings

Figure 51:
36-Pin WL-CSP

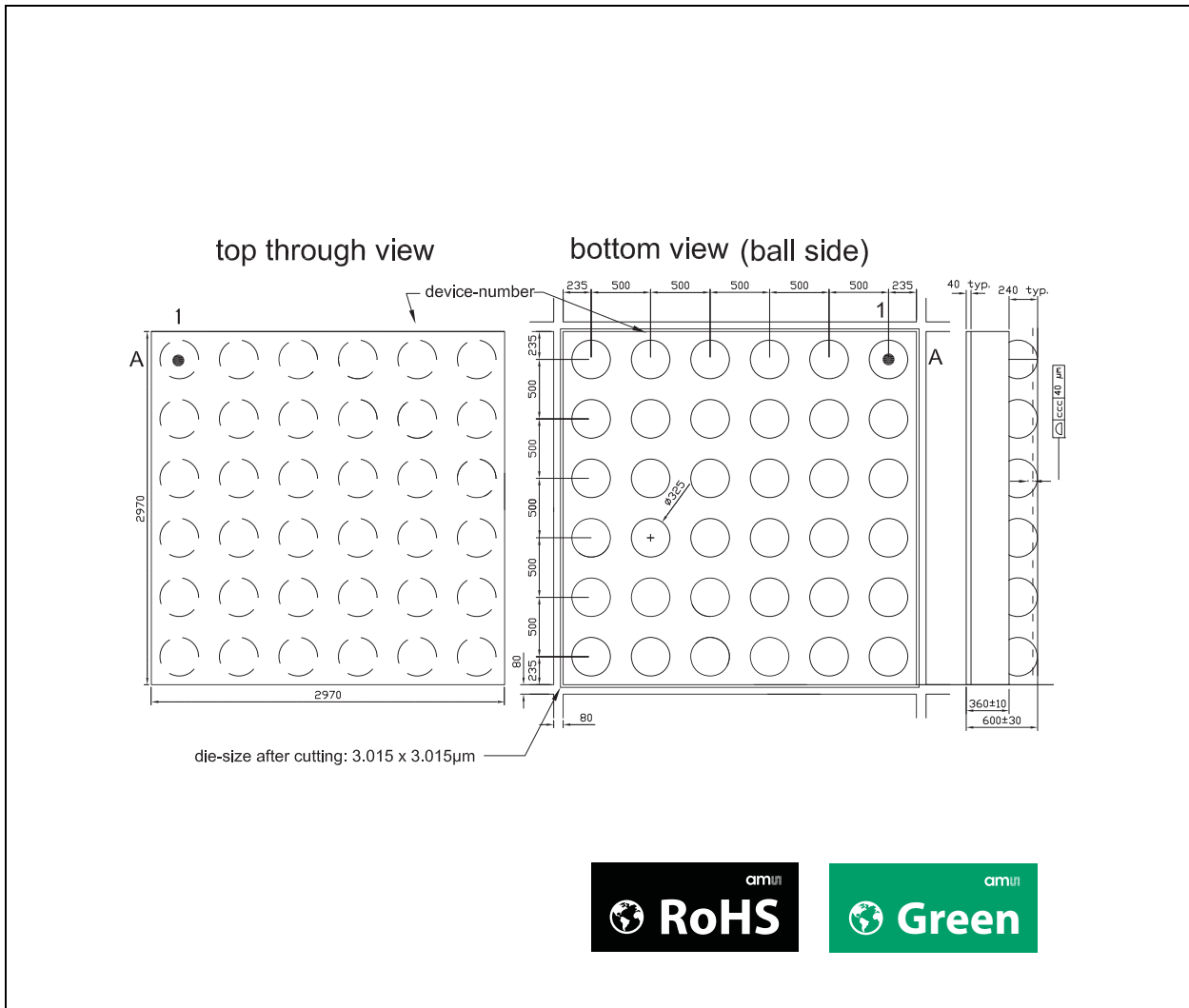


Figure 52:
36-Pin WL-CSP Marking

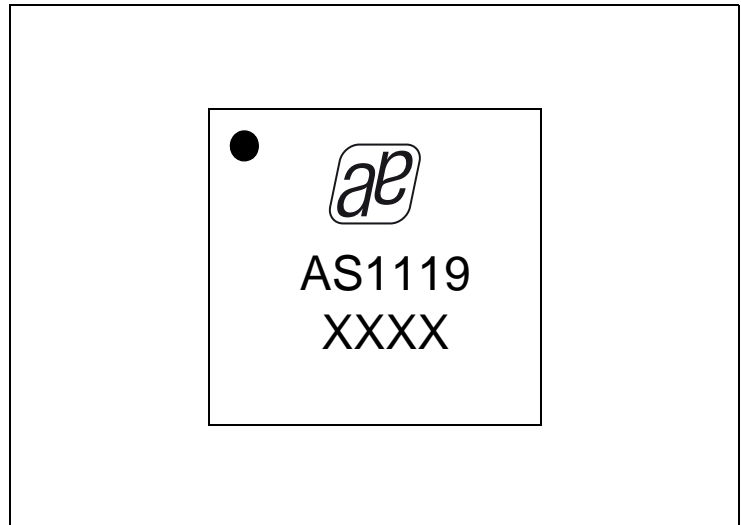


Figure 53:
Packaging Code

XXXX
Tracecode

Ordering & Contact Information

The devices are available as the standard products shown in Figure 54.

Figure 54:
Ordering Information

Ordering Code	Package	Marking	Description	Delivery Form	Delivery Quantity
AS1119-BWLT	36-Pin WL-CSP	AS1119	144-LED Cross-Plexing Driver with 320mA Charge-Pump	Tape & Reel	1000 pcs/reel

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 1.04 to current revision 2-00 (2016-Sep-21)	Page
Content of austriamicrosystems datasheet was converted to latest ams design	
Added Figure 1	1
Updated Figure 2	2
Updated Figure 3	3
Updated Figure 4	4
Updated Figure 10	9
Updated Figure 42	41
Updated Figure 52	49
Updated Figure 53	49

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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