austriamicrosystems AG

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ams AG

The technical content of this austriamicrosystems datasheet is still valid.

Contact information:

Headquarters:
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten, Austria
Tel: +43 (0) 3136 500 0
e-Mail: ams_sales@ams.com

Please visit our website at **www.ams.com**

AS1121

16-Channel LED Driver with Dot Correction and Greyscale PWM

1 General Description

The AS1121 is a 16-channel, constant current-sink LED driver. Each of the 16 channels can be individually adjusted by 4096-step greyscale PWM brightness control and 64-step constant-current sink (dot correction).

The dot correction circuitry adjusts the brightness variations between the AS1121 channels and other LED drivers. Greyscale control and dot correction circuitry are accessible via the SPI-compatible serial interface. A single external resistor sets the maximum current value of all 16 channels.

The open LED detection function indicates a broken or disconnected LED at one or more of the outputs. The overtemperature protection-flag indicates that the device is in an overtemperature condition.

An additional power-down pin puts the AS1121 into a 40nA standby-mode.

The AS1121 is available in a 32-pin TQFN 5x5 mm package.

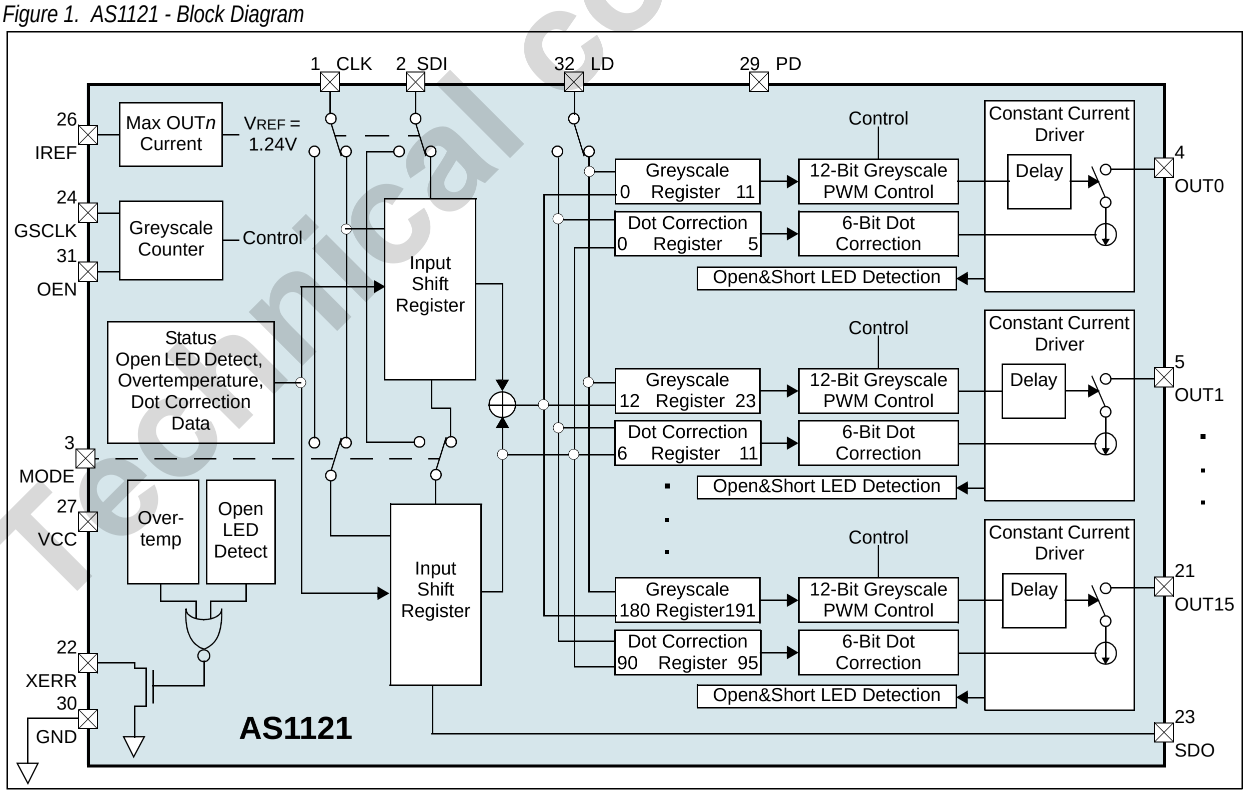
2 Key Features

- Greyscale PWM Control: 12-Bit (4096 Steps)
- Dot Correction: 6-Bit (64 Steps)
- Drive Capability (Constant-Current Sink): 0 to 40mA
- LED Power Supply Voltage: up to 30V
- Supply Voltage Range: 3.1V to 3.6V
- SPI-Compatible Serial Interface
- Output Delay for controlled Inrush Current (factory set, can be turned off)
- Factory set rise- and fall-time for EMI improvement
- PWM Clock Rate: up to 10 MHz
- Data Transfer Clock Rate: up to 30 MHz
- CMOS Level I/O
- Diagnostic Features
- 32-pin TQFN 5x5 mm Package

3 Applications

The device is ideal for mono-, multi-, and full-color LED displays, LED signboards, and display backlights.

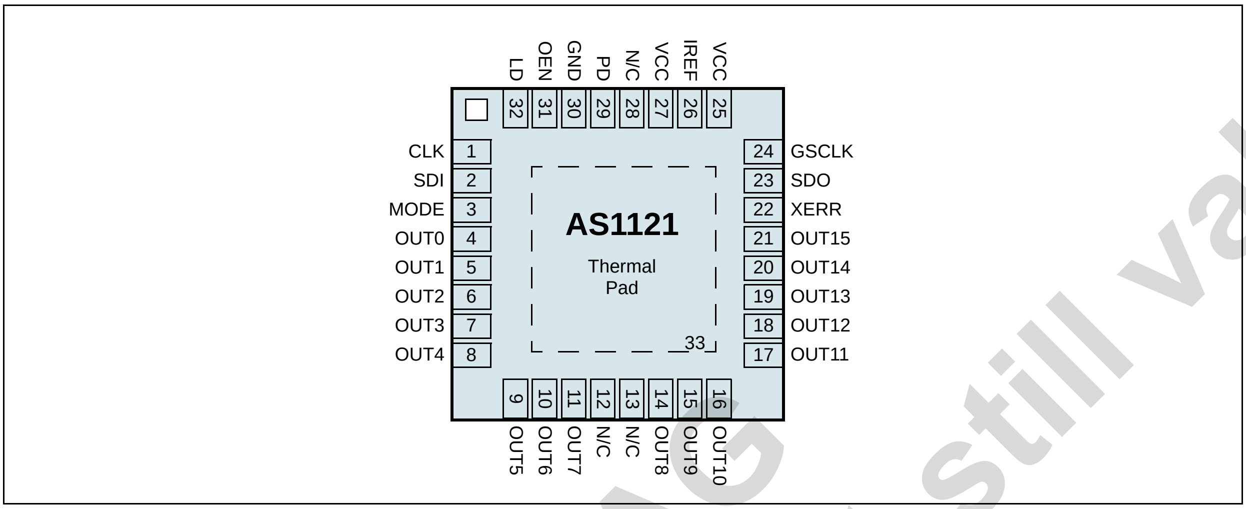
Figure 1. AS1121 - Block Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	CLK	Serial Data Shift Clock
2	SDI	Serial Data Input
3	MODE	Mode Select input with internal pulldown MODE = GND: Selects greyscale mode (see Setting Greyscale Brightness on page 14) MODE = VCC: Selects dor correction mode (see Setting Dot Correction on page 13)
4:11	OUT0:OUT7	Constant-Current Outputs 0:7
14:21	OUT8:OUT15	Constant-Current Outputs 8:15
22	XERR	Error Output 0 = LED open detection or overtemperature condition is detected. 1 = Normal operation.
23	SDO	Serial Data Output
24	GSCLK	Greyscale Clock. Reference clock for greyscale PWM control
26	IREF	Reference Current Terminal
25, 27	VCC	Power Supply Voltage
12,13,28	N/C	This pins must not be connected
29	PD	Power Down 0 = normal operation mode 1 = power down mode
30	GND	Ground
31	OEN	Blank Outputs 0 = OUT*n* outputs are controlled by the greyscale PWM control. 1 = OUT*n* outputs are forced off; the greyscale counter is reset.
32	LD	Data Latch. The internal connections are switched by pin MODE. For LD (MODE = GND), the greyscale register receives new data. For LD (MODE = VCC), the dot correction register receives new data.
33	Thermal Pad	Thermal Pad. This pin must be connected to GND to ensure normal operation.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
VCC to GND	-0.3	5	V	
All other pins to GND	-0.3	VCC + 0.3	V	
VSDO, VXERR to GND	-0.3	VCC + 0.3	V	
VOUT0 : VOUT15 to GND	-0.3	30	V	
Output Current		50	mA	
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic Discharge				
Electrostatic Discharge HBM	+/- 2		kV	Norm: MIL 883 E method 3015
Thermal Information				
Junction to ambient thermal resistance		37	°C/W	For more information about thermal metrics, see application note *AN01 Thermal Characteristics*.
Temperature Ranges and Storage Conditions				
Junction Temperature		+150	ºC	
Storage Temperature Range	-55	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	3			Represents a max. floor life time of 168h

6 Electrical Characteristics

V_{CC} = +3.1V to +3.6V, Typical values are at T_{AMB} = +25°C, V_{CC} = 3.3V (unless otherwise specified). All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods..

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{AMB}	Operating Temperature Range		-40		+85	°C
T_J	Operating Junction Temperature		-40		+125	°C
Input Supply						
V_{CC}	Supply Voltage		3.1		3.6	V
I_{CC}	Supply Current	All outputs off, R_{IREF} = 1kΩ		8.5	15	mA
		All outputs on, R_{IREF} = 1kΩ		15	20	
		All outputs off, R_{IREF} = 10kΩ		2	4	
		All outputs on, R_{IREF} = 10kΩ		3	5	
I	Input Current	V_{IN} = V_{CC} or GND; Pins OEN, GSCLK, CLK, SDI, LD, PD	-1		1	µA
		V_{IN} = V_{CC}; pin MODE			50	
		V_{IN} = GND; pin MODE	-1		1	
I_{PD}	Power Down Current			40		nA
Output						
V_{OUT}	Voltage Applied to Output (OUT0:OUT15)		1.5		30	V
I_{COC}	Constant Output Current	All outputs on, V_{OUT} = 1.5V, R_{IREF} = 1kΩ	36	40	44	mA
ΔI_{COC}	Constant Output Current Error	V_{OUT} = 1.5V, R_{IREF} = 1kΩ, OUT0:OUT15		±1		%
		V_{OUT} = 1.5V, R_{IREF} = 10kΩ, OUT0:OUT15		±1.5		
		Device to device, average current from OUT0:OUT15, R_{IREF} = 1kΩ		±1		
		Device to device, average current from OUT0:OUT15, R_{IREF} = 10kΩ		±1		
I_{LEAK}	Leakage Output Current	All outputs off, V_{OUT} = 30V, R_{IREF} = 1kΩ, OUT0:OUT15		20		nA
ΔI_{LNR}	Line Regulation	V_{OUT} = 1V, R_{IREF} = 1kΩ OUT0:OUT15		±1	±2.5	%/V
		V_{OUT} = 1V, R_{IREF} = 10kΩ OUT0:OUT15		±0.2	±2.5	
ΔI_{LDR}	Load Regulation	V_{OUT} = 1.5V to 4V, R_{IREF} = 1kΩ, OUT0:OUT15		±0.1	±0.4	%/V
		V_{OUT} = 1.5V to 4V, R_{IREF} = 10kΩ, OUT0:OUT15		±0.01	±0.4	
Logic Levels						
V_{IH}	High-Level Input Voltage		0.8 x V_{CC}		V_{CC}	V
V_{IL}	Low-Level Input Voltage		GND		0.2 x V_{CC}	V
V_{OH}	High-Level Output Voltage	I_{OH} = -1mA, SDO	V_{CC} -0.5			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1mA, SDO, XERR			0.5	V
I_{OH}	High-Level Output Current	V_{CC} = 5 V at SDO	-1.0			mA

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OL}	Low-Level Output Current	V_{CC} = 5 V at SDO, XERR	1.0			mA
V_{LOD}	LED Open Detection Threshold			0.3	0.4	V
V_{IREF}	Reference Voltage Output	R_{IREF} = 1kΩ	1.23	1.27	1.32	V
Thermal Protection						
T_{TWF}	Thermal Warn Flag Threshold			125		ºC
T_{TEF}	Thermal Error Flag Threshold			150		ºC

Timing Characteristics

V_{CC} = +3.1V to +3.6V, T_{AMB} = -40°C to +85ºC. Typical values are at T_{AMB} = +25°C, V_{CC} = 3.3V (unless otherwise specified).

Table 4. Output Tming Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{R0}	Rise Time	SDO		8		ns
t_{R1} [1]		OUT*n*, DC = $3F_{HEX}$, R_{IREF} = 1kΩ		25		
t_{F0}	Fall Time	SDO		8		ns
t_{F1} [1]		OUT*n*, DC = $3F_{HEX}$, R_{IREF} = 1kΩ		25		
t_{PD0}	Propagation Delay Time	CLK, SDO [2]		15		ns
t_{PD1}		OUT0, OUT1, OUT2, OUT3 [2], R_{IREF} = 1kΩ, turn ON delay				
t_{PD2}		OUT0, OUT1, OUT2, OUT3 [2], R_{IREF} = 1kΩ, turn OFF delay				
t_D	Average Output Delay Time (can be turend off on request)	OUT4, OUT5, OUT6, OUT7 [2]		25		ns
		OUT8, OUT9, OUT10, OUT11 [2]				
		OUT12, OUT13, OUT14, OUT15 [2]				

1. Value can be factory trimmed for EMI improvement
2. See Figure 24 on page 16.

Interface Characteristics

V_{CC} = +3.1V to +3.6V, T_{AMB} = -40°C to +85ºC. Typical values are at T_{AMB} = +25°C, V_{CC} = 3.3V (unless otherwise specified).

Table 5. Serial Interface Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	Data Shift Clock Frequency	CLK			30	MHz
f_{GSCLK}	Greyscale Clock Frequency	GSCLK			5	MHz
t_{WH0}/t_{WL0}	CLK Pulse Duration	CLK = 1/0 [1]	16			ns
t_{WH1}/t_{WL1}	GSCLK Pulse Duration	GSCLK = 1/0 [2]	tbd			ns
t_{WH2}	LD Pulse Duration	LD = 1 [1]	20			ns
t_{WH3}	OEN Pulse Duration	OEN = 1 [2]	20			ns

Table 5. Serial Interface Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tERR	Error Detection Duration	LD = 1, OEN = 0 [3]		1000		ns
tSU0	Setup Time	SDI, CLK [4]	12			ns
tSU1		CLK, LD [3]	12			
tSU2		MODE, CLK [5]	12			
tSU3		MODE, LD [4]	12			
tSU4		OEN, GSCLK [2]	12			
tH0	Hold Time	CLK, SDI [3]	12			ns
tH1		LD, CLK [1]	12			
tH2		CLK, MODE [4]	12			
tH3		LD, MODE [4]	12			
tH4		OEN, GSCLK [2]	12			

1. See Figure 20 on page 13.
2. See Figure 24 on page 16.
3. See Figure 18 on page 11
4. See Figure 22 on page 14.
5. See Figure 17 on page 10.

7 Typical Operating Characteristics

TAMB = +25°C, VCC = 3.3V (unless otherwise specified)

Figure 3. Constant Output Current vs. Output Voltage

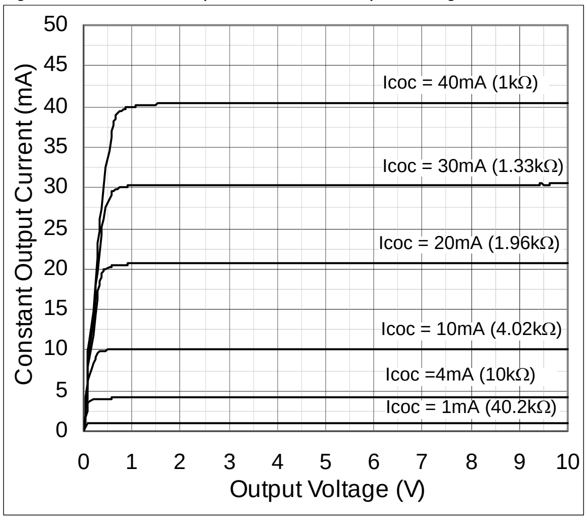


Figure 4. Constant Output Current vs. Output Voltage

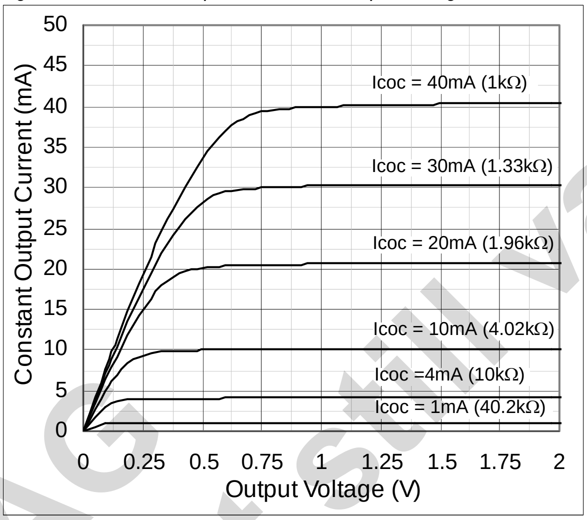


Figure 5. Constant Output Current vs. VOUT; RIREF = 1kΩ

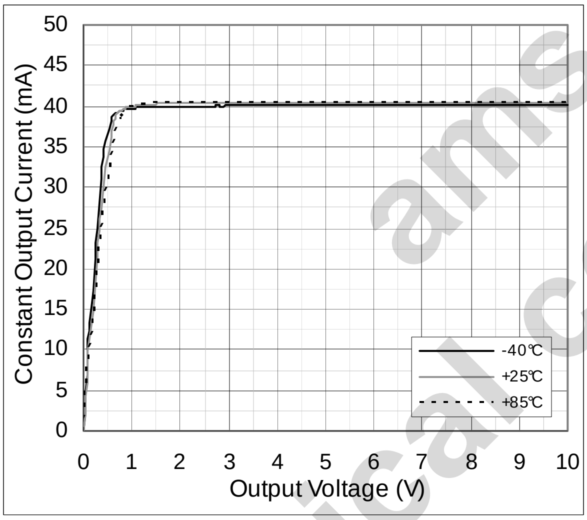


Figure 6. Constant Output Current vs. VOUT; RIREF = 1kΩ

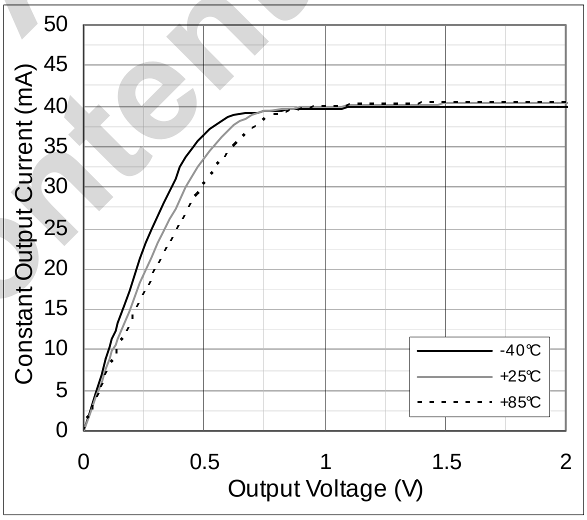


Figure 7. ICOC vs. Temp.; RIREF = 1kΩ, VOUT = 1.5V

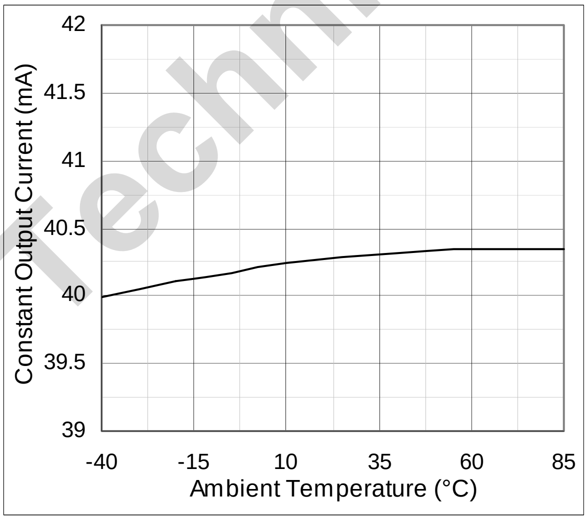


Figure 8. ICOC vs. Temp.; RIREF = 10kΩ, VOUT = 1.5V

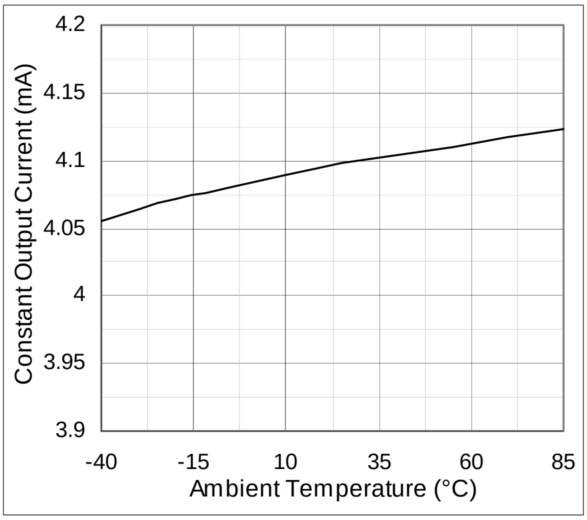


Figure 9. ICOC vs. RIREF; VOUT = 1.5V

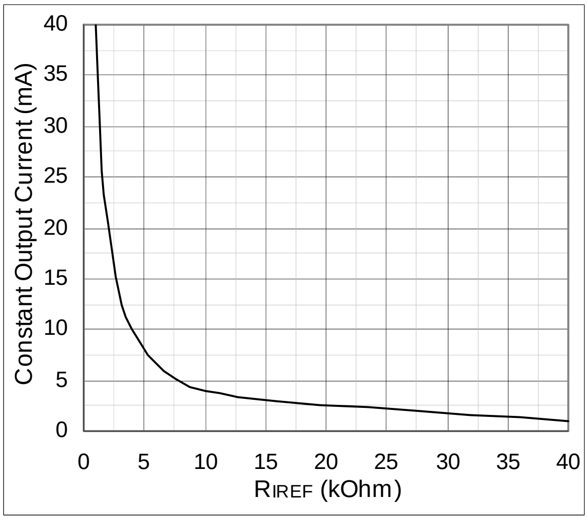


Figure 10. ICOC vs. Dot Correction; VOUT = 1.5V

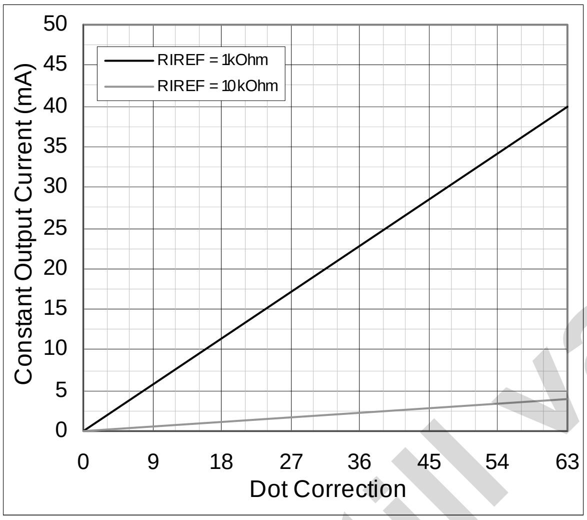


Figure 11. Supply Current vs. Temp.; RIREF = 1kΩ, VOUT = 1.5V

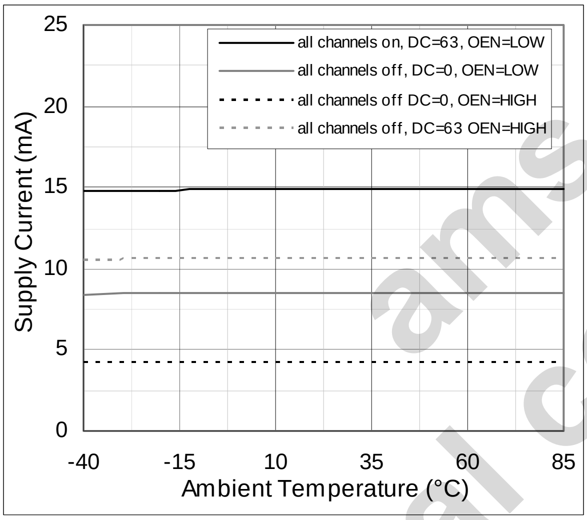


Figure 12. ΔICOC vs. Constant Output Current average

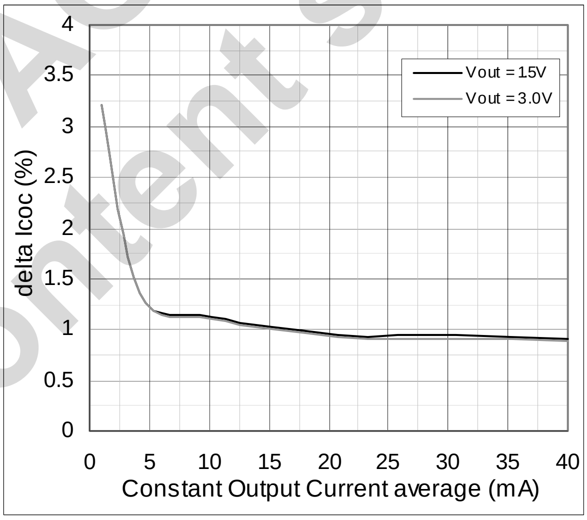


Figure 13. ΔICOC vs. Temp.; RIREF = 1kΩ

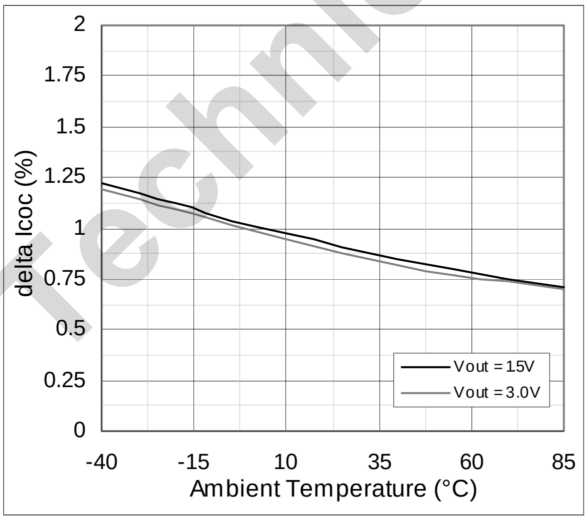


Figure 14. ΔICOC vs. Temp.; RIREF = 10kΩ

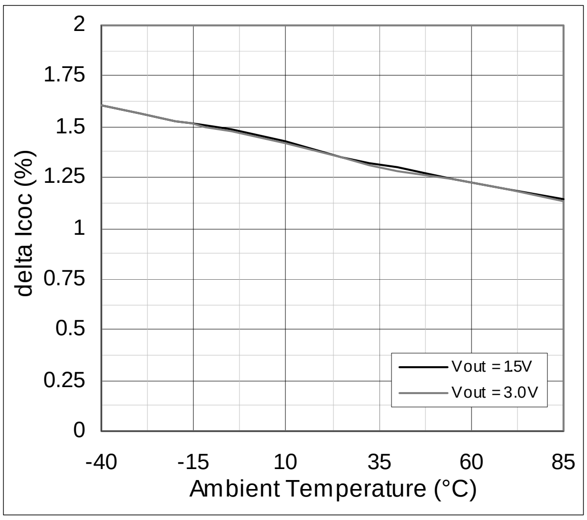


Figure 15. LED Open Detection Threshold vs. Temperature

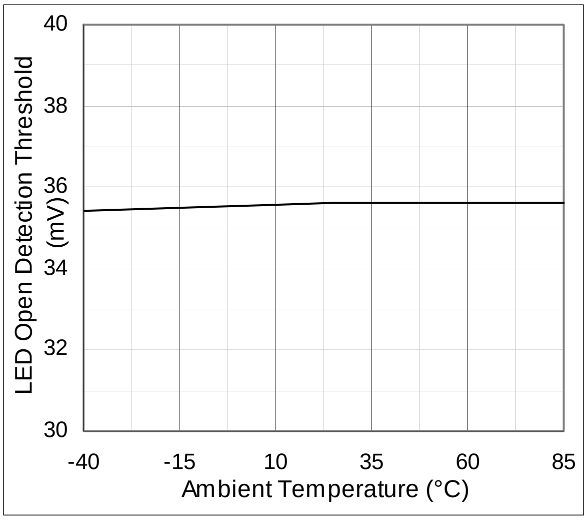
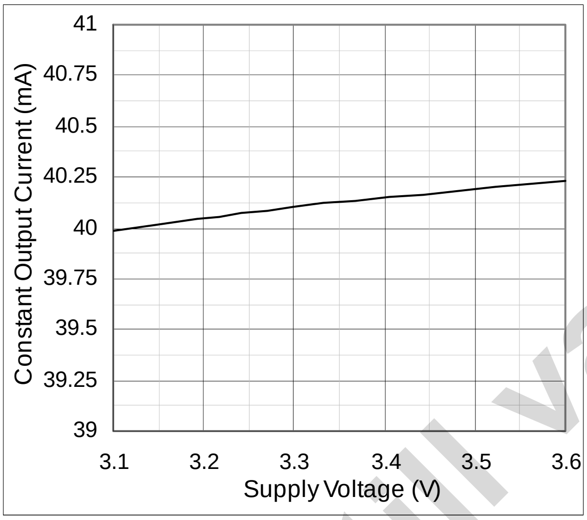


Figure 16. ICOC vs. Supply Voltage; RIREF = 1kΩ



8 Detailed Description

Serial Interface

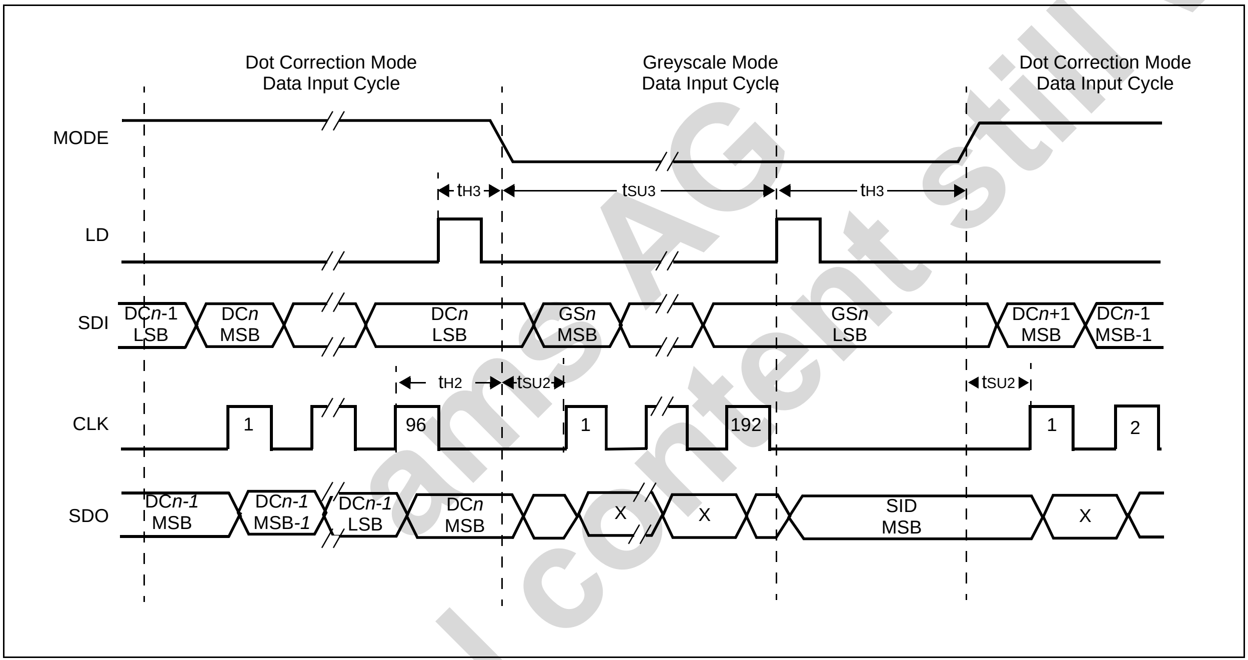
The AS1121 features a versatile 3-pin (CLK, SDI, and SDO) serial interface, which can be connected to microcontrollers or digital signal processors in various configurations.

The rising edge of the CLK signal shifts data from pin SDI to the internal register. After all data is clocked in, the serial data is latched into the internal registers at the rising edge of the LD signal.

Note: All data is clocked in with the MSB first.

Multiple AS1121 devices can be cascaded by connecting the SDO pin of one device with pin SDI of the next device (see Figure 25 on page 17). The SDO pin can also be connected to the microcontroller to receive status information from the AS1121. The serial data format is 96-bit or 192-bit wide, depending on mode of the device (see LD on page 2).

Figure 17. Serial Data Input Timing Diagram



Error Information Output

The open-drain output pin XERR indicates if the device is in one of the two error conditions: overtemperature flag or open LED detect. During normal operation, the internal transistor connected to pin XERR is turned off and the voltage on XERR is pulled up to VCC through an external pullup resistor.

If an overtemperature or open LED condition is detected, the internal transistor is switched on, and XERR is pulled to GND. Because XERR is an open-drain output, multiple AS1121 devices can be ORed together and pulled up to VCC with a single pullup resistor (see Figure 25 on page 17). This reduces the number of signals needed to report a system error.

To differentiate the overtemperature flag from the open LED detect flag from pin XERR, the open LED detect flag can be masked out by setting OEN = 1 (see Table 6).

Table 6. XERR Truth Table

Error Condition			Error Information			Selected Mode			Status
	Temp.	OUT*n* Voltage	Thermal Error Flag	Thermal Warning Flag	Open LED Detect	OEN	Mode	XERR	
Open	$T_J < T_{TEF}$	OUT*n* > V_{LOD}	0	Don't Care	0	0	0	1	normal
		OUT*n* < V_{LOD}	0	Don't Care	1	0	0	0	open error
	$T_J > T_{TEF}$	OUT*n* > V_{LOD}	1	Don't Care	0	0	0	0	temp. error
		OUT*n* < V_{LOD}	1	Don't Care	1	0	0	0	open & temp. error
Temp	$T_J > T_{TEF}$	Don't Care	0	Don't Care	Don't Care	1	0	1	normal
	$T_J < T_{TEF}$	Don't Care	1	Don't Care	Don't Care	1	0	0	temp error
	$T_J > T_{TWF}$	Don't Care	Don't Care	0	Don't Care	1	1	1	normal
	$T_J < T_{TWF}$	Don't Care	Don't Care	1	Don't Care	1	1	0	temp. warn

Overtemperature Error/Warning Flags

The AS1121 provides a overtemperature circuit to indicate that the device is in an overtemperature condition. If the device junction temperature (T_J) exceeds the threshold temperature (150°C typ), the overtemperature circuit trips and pulls XERR to ground. The overtemperature flag status can be read out from the AS1121 status register.

To prevent an overtemperature condition the AS1121 offers an temperature warning flag at 125°C typical. This flag can be used to take precautions (e.g. start an external cooling) against a overtemperature condition.

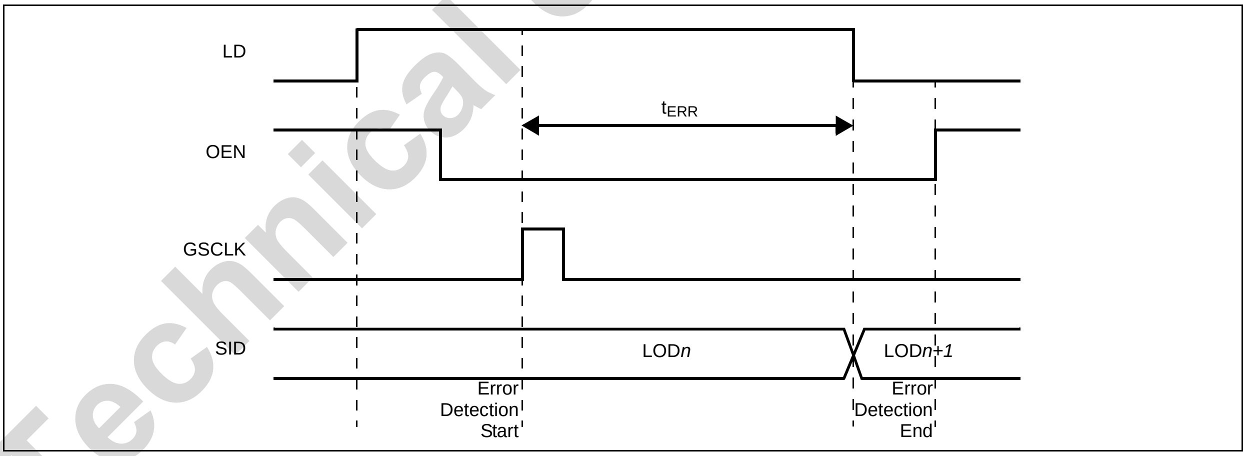
Open LED Detection

The AS1121 integrated open LED detection circuit reports an error if any of the 16 LEDs is open or disconnected from the circuit. The open LED detection circuit trips when the error detection is activated and the voltage at OUT*n* is less than V_{LOD}.

Note: The voltage at each OUT*n* is sampled 1 µs after being switched on. Please refer to Figure 18 on page 11.

The open LED detection circuit also pulls XERR to GND when tripped. The open LED status of each channel can also be read out from the AS1121 status information data (SID) during a greyscale data input cycle.

Figure 18. Error Detection Timing (GS=FFFF$_{HEX}$, DC=3F$_{HEX}$)



Note: The rising edge of LD latches new data into the internal registers depending on the logic level of the pin MODE. If the pin MODE is tied GND, the greyscale registers are updated. If the pin MODE is tied to V_{CC}, the dot correction registers are updated.

OUTn Enable

All OUTn channels can be collectively switched off with one signal. When OEN is set to 1, all OUTn channels are disabled, regardless of the device logic operations. The greyscale counter is also reset when OEN is set to 1.

When OEN is set to 0, all OUTn channels are in normal operation.

Table 7. Pin OEN Truth Table

OEN	OUT0:OUT15
0	Normal Operation
1	Disabled

Setting Maximum Channel Current

The maximum output current per channel is programmed by a single resistor, RIREF, which is placed between pin IREF and GND. The voltage on pin IREF is set by an internal band gap VIREF (1.27V typ). The maximum channel current is equivalent to the current flowing through RIREF multiplied by a factor of 31.5. The maximum output current is calculated as:

$$I_{MAX} = \frac{V_{IREF}}{R_{IREF}} \times 31.5 \qquad \text{(EQ 1)}$$

Where:

VIREF = 1.27V;
RIREF = User-selected external resistor.

Power Dissipation

To ensure proper operation of the device, the total power dissipation of the AS1121 must be below the power dissipation rating of the device package. Total power dissipation is calculated as:

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{MAX} \times n \times \frac{DCn}{63} \; d_{PWM}) \qquad \text{(EQ 2)}$$

Where:

VCC is the device supply voltage;
ICC is the device supply current;
VOUT is the device OUTn voltage when driving LED current;
IMAX is the LED current adjusted by RIREF;
DCn is the maximum dot correction value for OUTn;
n is the number of OUTn driving LED at the same time;
dPWM is the duty cycle defined by pin OEN or the greyscale PWM value.

Operating Modes

The AS1121 operates in two modes (see Table 8). Greyscale operating mode (see Figure 22 on page 14) and the shift registers are in reset state at power-up.

Table 8. Operating Modes

Mode	Input Shift Register	Operating Mode
0	192-bit	Greyscale PWM Mode
1	96-bit	Dot Correction Data Input Mode

Setting Dot Correction

The AS1121 can perform independent fine-adjustments to the output current of each channel, i.e., dot correction. Dot correction is used to adjust brightness deviations of LEDs connected to the output channels (OUT0:OUT15).

The device powers up with the following default seetings: DC = 63 and GS = 4095.

The 16 channels can be individually programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0 to 100% of the maximum output current (I_{MAX}). The output current for each OUT*n* channel can be calculated as:

$$I_{OUTn} = I_{MAX} \times \frac{DCn}{63} \qquad \text{(EQ 3)}$$

Where:

I_{MAX} is the maximum programmable output current for each output;
DC*n* is the programmed dot correction value for output (DC*n* = 0 to 63);
n = 0 to 15

Dot correction data are simultaneously entered for all channels. The complete dot correction data format consists of 16 x 6-bit words, which forms a 96-bit serial data packet (see Figure 19). Channel data is put on one by one, and the data is clocked in with the MSB first.

Figure 19. Dot Correction Data Packet Format

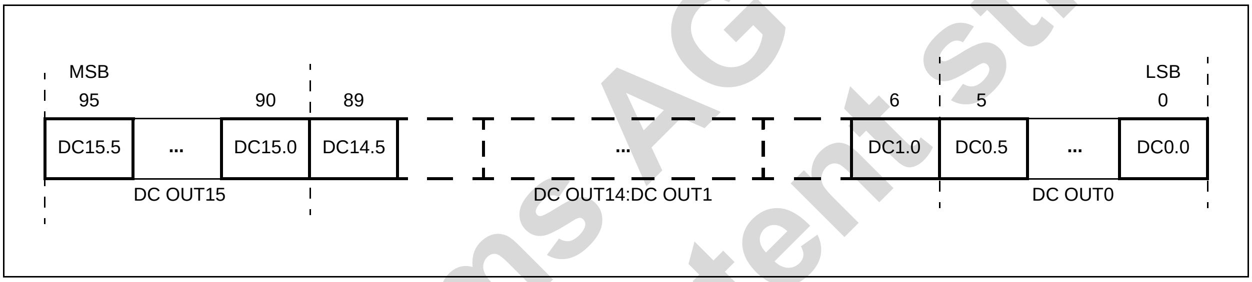
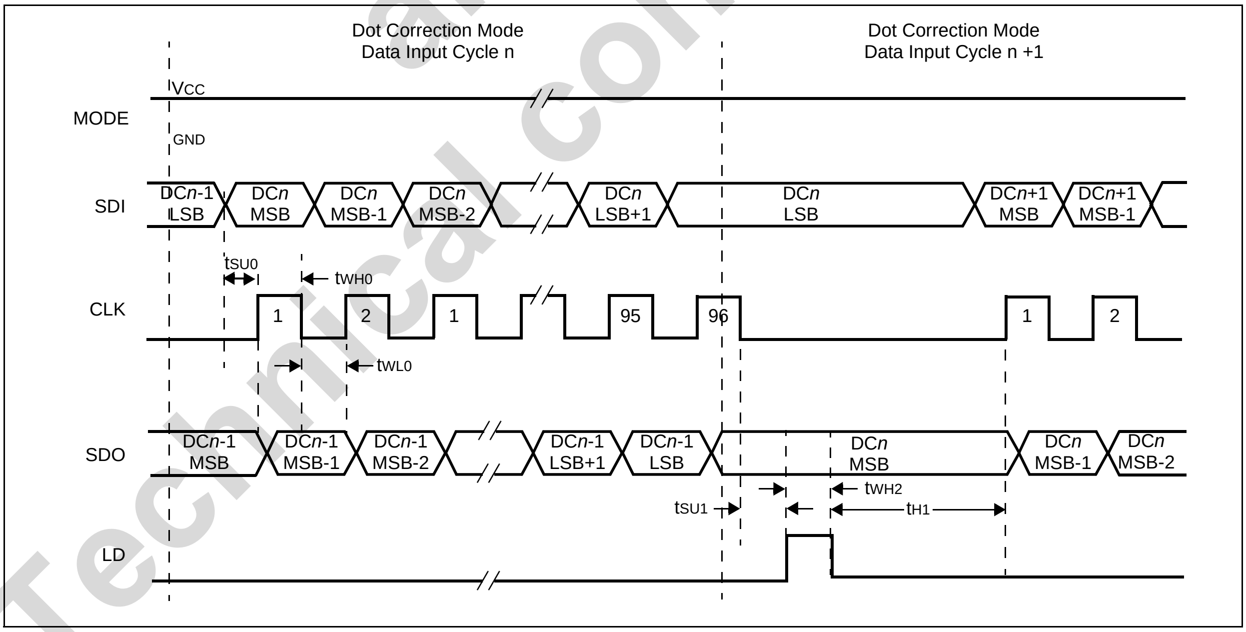


Figure 20. Dot Correction Data Input Timing Diagram



Setting Greyscale Brightness

The brightness of each channel output can be adjusted using a 12 bits-per-channel PWM control scheme which results in 4096 brightness steps, from 0% to 100% brightness. The brightness level for each output is calculated as:

$$\%Brightness = \frac{GSn}{4095} \times 100 \qquad \text{(EQ 4)}$$

Where:

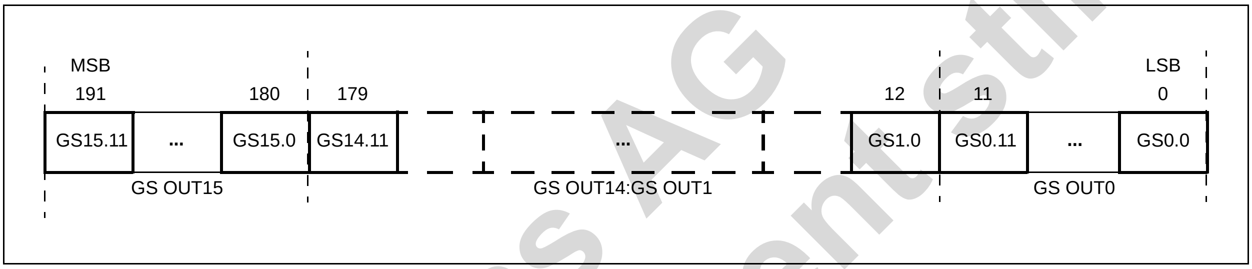
GS*n* is the programmed greyscale value for OUT*n* (GS*n* = 0 to 4095);
n = 0 to 15 greyscale data for all outputs.

The device powers up with the following default seetings: GS = 4095 and DC = 63.

The input shift register shifts greyscale data into the greyscale register for all channels simultaneously. The complete greyscale data format consists of 16 x 12 bit words, which forms a 192-bit wide data packet (see Figure 21).

Note: The data packet must be clocked in with the MSB first.

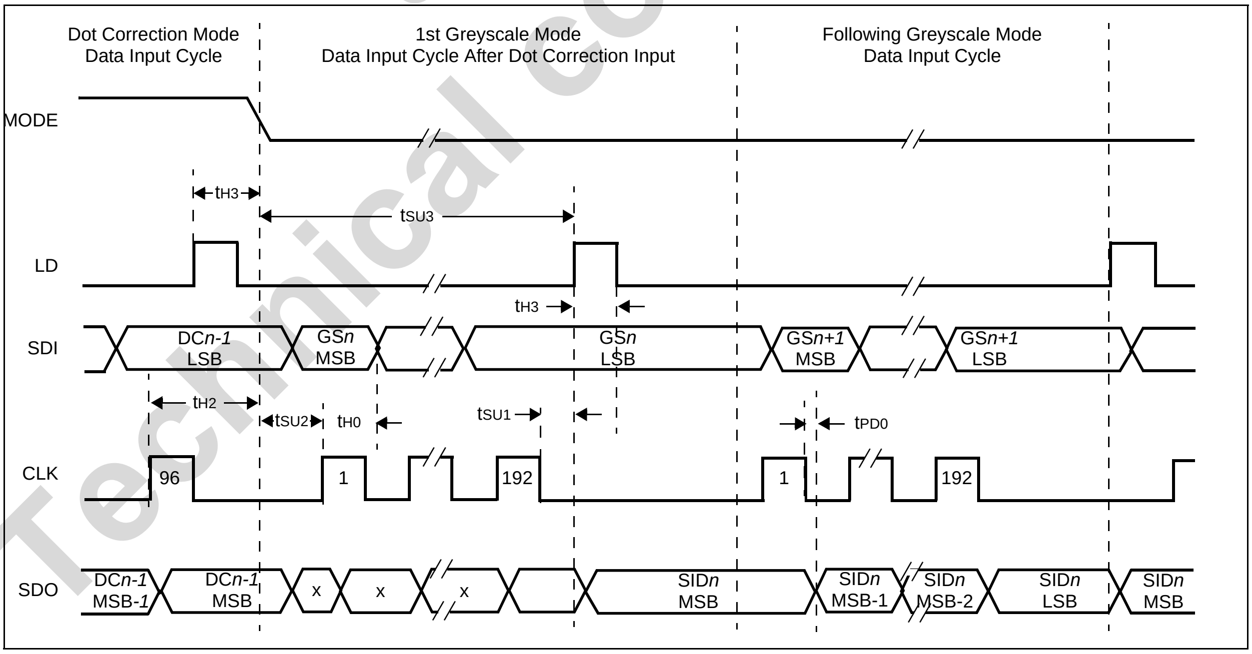
Figure 21. Greyscale Data Packet Format



When pin MODE is tied to GND, the AS1121 enters greyscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, the rising edge of the LD signal latches the data into the greyscale register (see Figure 22).

All greyscale data in the input shift register is replaced with status information data (SID) after latching into the greyscale register.

Figure 22. Greyscale Data Input Timing Diagram

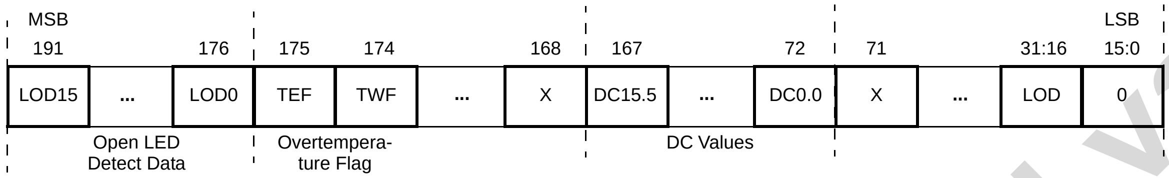


Status Information Data (SID)

The AS1121 contains an integrated status information register, which can be accessed in greyscale mode (MODE = GND). Once the LD signal latches the data into the greyscale register, the input shift register data is replaced with status information data (see Figure 23).

Open LED and overtemperature flags as well as the dot-correction registers can be read out at pin SDO. The status information data packet is 192 bits wide. Bits 191:176 and 31:16 contain the open LED detection status of each channel (either 191:176 or 31:16 can be used for readout). Bit 175 contains the thermal error flag status. Bits 167:72 contain the data of the dot-correction register. Bit 15:0 contains the LED shorted flags. The remaining bits are reserved. The complete status information data packet is shown in Figure 23.

Figure 23. Status Information Data Packet Format



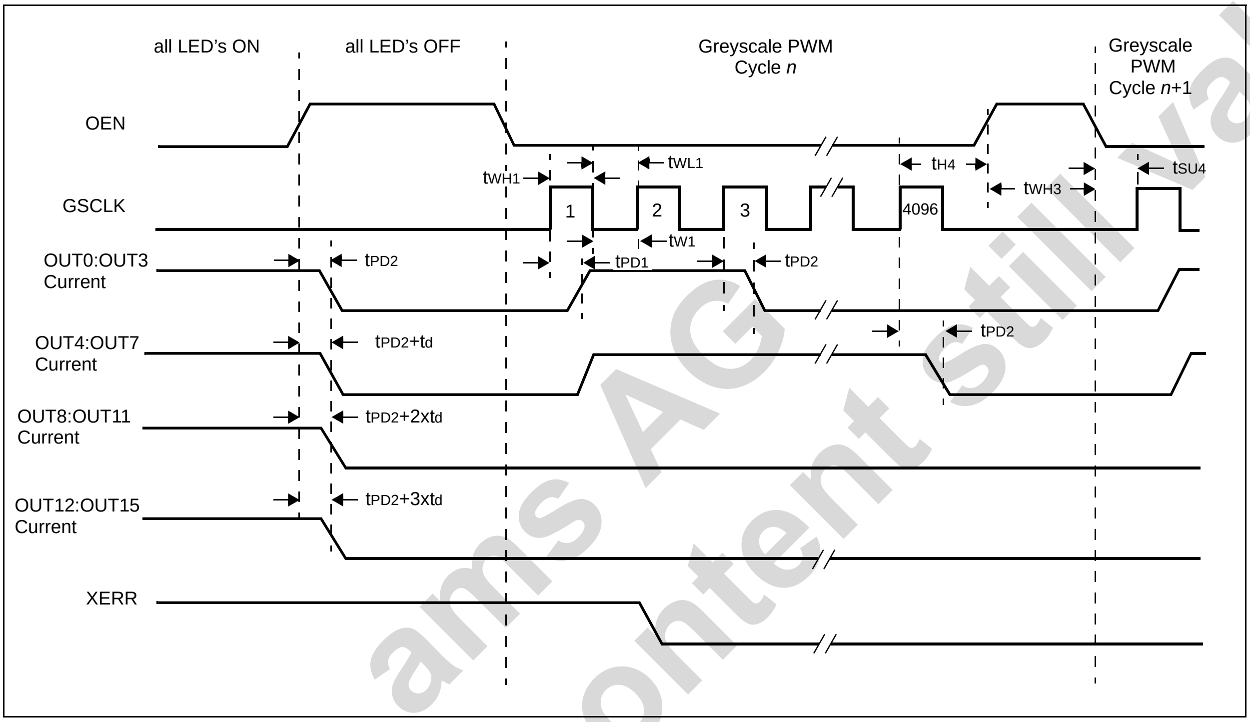
Bit #	Description	Bit #	Description
191:176	reserved	167:72	Dot Correction Readback (16 x 6 Bit)
175	Temperature Error Flag (TEF, 150ºC, typ)	71:32	reserved
174	Temperature Warning Flag (TWF, 125ºC, typ)	31:16	LED Open Detection (Optional, same as bits 176:191), LOD
173:168	reserved	15:0	reserved

Greyscale PWM Operation

The falling edge of the OEN signal initiates a greyscale PWM cycle. The first GSCLK pulse after the falling edge of OEN increments the greyscale counter by one and switches on any OUT*n* whose greyscale value does not equal zero. Each subsequent rising edge of GSCLK increments the greyscale counter by one.

The AS1121 compares the greyscale value of each OUT*n* channel with the greyscale counter value. All OUT*n* whose greyscale values equal the counter values are switched off. A OEN = 1 signal after 4096 GSCLK pulses resets the greyscale counter to zero and completes a greyscale PWM cycle (see Figure 24).

Figure 24. Greyscale PWM Cycle Timing Diagram



Output Delay

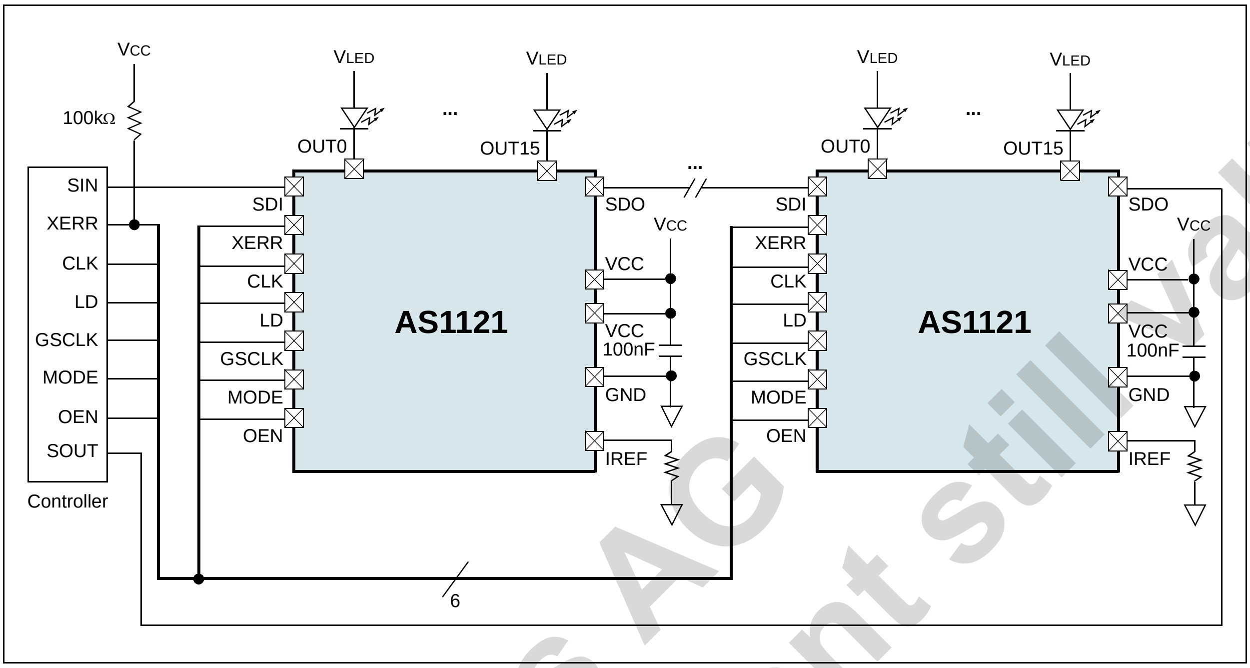
To minimize the ripple on the inrush current, the outputs are delayed and are not switching at the same time. The 16 channels of the AS1121 are combined in groups of 4. The channels within the groups OUT0:OUT3, OUT4:OUT7, OUT8:OUT11, OUT12:OUT15 are switching at the same time. Between the 4 groups a delay of t_d = 25ns (typ.) is implemented. On request this delay can be turned off (see Ordering Information on page 20).

To increase the EMI performance the rising and falling edges of the OUTn signals are symmetrical (t_R = t_F = 25ns). The rise- and fall-times are factory set and can be changed on request. For further information and requests, please contact us mailto:sales@austriamicrosystems.com.

Serial Data Transfer Rate

Figure 25 shows a cascaded arrangement AS1121 devices connected to a controller, building a basic module of an LED display system.

Figure 25. Cascaded Configuration



The maximum number of cascading AS1121 devices depends on the application system and is in the range of 40 devices. The minimum frequency needed can be calculated by the following equations:

$$f_{GSCLK} = 4096 \times f_{UPDATE} \quad \text{(EQ 5)}$$

Where:

f_{GSCLK} is the minimum frequency needed for GSCLK;

f_{UPDATE} is the update rate of whole cascaded system.

$$f_{CLK} = 193 \times f_{UPDATE} \times n \quad \text{(EQ 6)}$$

Where:

f_{CLK} is the minimum frequency needed for CLK and SIN;

f_{UPDATE} is the update rate of whole cascaded system;

n is the number of cascaded of AS1121 devices.

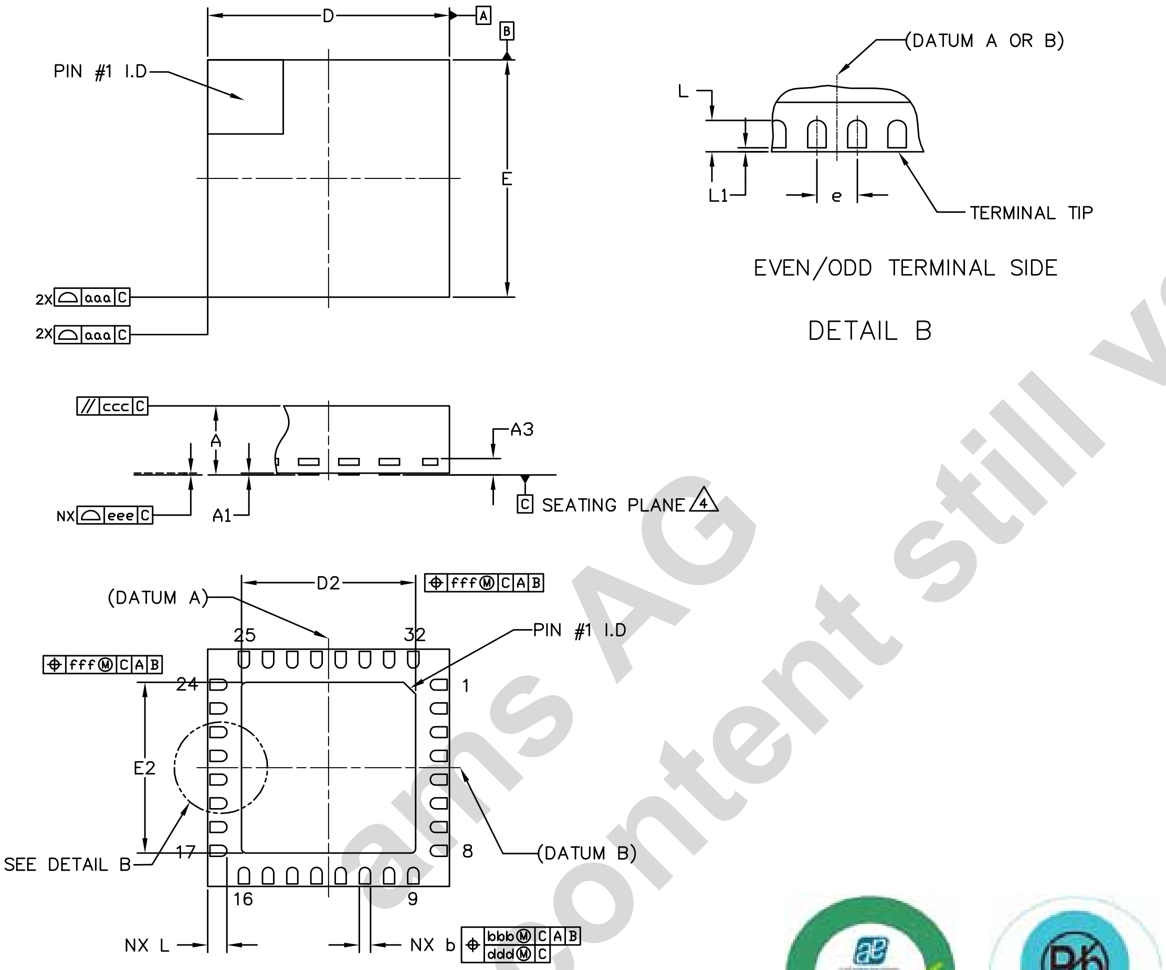
9 Package Drawings and Markings

Figure 26. 32-pin TQFN 5x5 mm Marking

Figure 27. Packaging Code YYWWIZZ

YY	WW	I	ZZ
last two digits of the current year	manufacturing week	plant identifier	free choice / traceability code

Figure 28. 32-pin TQFN 5x5 mm Package



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	–	0.20 REF	–
L	0.30	0.35	0.40
L1	0	–	0.15
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D2	3.50	3.60	3.70
E2	3.50	3.60	3.70
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
fff	–	0.10	–
N		32	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. N IS THE TOTAL NUMBER OF TERMINALS.

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DRAWN RH8	DATE 2010.10.29	REV. N/C	ASSEMBLY ENGINEERING TITLE SAWN QFN, PULL BACK, 5x5x0.9mm 32 LEAD, 3.60mm SQ. ePAD	REFERENCE DOCUMENT JEDEC MO – 220 LATEST REVISION
CHECKED GBO	DATE 2010.10.29		DRAWING NO. QRK	UNIT
APPROVED MKR	DATE 2010.10.29	SHEET 1 OF 1	DIMENSION AND TOLERANCE	SCALE NOT IN SCALE

10 Ordering Information

The device is available as the standard products shown in Table 9.

Table 9. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1121-BQFT	AS1121	16-Channel LED Driver with Dot Correction and Greyscale PWM	Tape and Reel	32-pin TQFN 5x5 mm
AS1121B-BQFT*	AS1121B	16-Channel LED Driver with Dot Correction and Greyscale PWM without Output Delay	Tape and Reel	32-pin TQFN 5x5 mm

*) on request

Note: All products are RoHS compliant and austriamicrosystems green.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical Support is found at http://www.austriamicrosystems.com/Technical-Support

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or find your local distributor at http://www.austriamicrosystems.com/distributor

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Contact Information

Headquarters

austriamicrosystems AG
Tobelbaderstrasse 30
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

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