AS1371

400mA, Low Input Voltage, Low Quiescent Current LDO

1 General Description

The AS1371 low input voltage, positive voltage regulator is designed to deliver up to 400mA while consuming typically only 15µA of quiescent current. The device operates from input voltages of 1.2V to 3.6V, and is available in fixed output voltages between 0.6V and 3.3V (programmable in 50mV steps).

Operation at the full 400mA load current is dependent upon the maximum power dissipation available from package and environment.

The low input voltage and ultra-low dropout voltage (20mV @ 100mA load and 80mV @ 400mA load) supports single primary cell operation in small applications, when operated with minimum input-to-output voltage differentials. In addition, the regulator provides a power management life extension by operating from pre-existing 1.8V and 2.5V outputs to provide low output voltages for new generation portable processor cores.

The device features stable output voltage with ceramic capacitors down to a value of 1µF, strict output voltage regulation tolerances (±1%), and good line- and load-regulation.

The AS1371 is available in a 6-pin 2x2 TDFN package and is qualified for -40°C to +85°C operation.

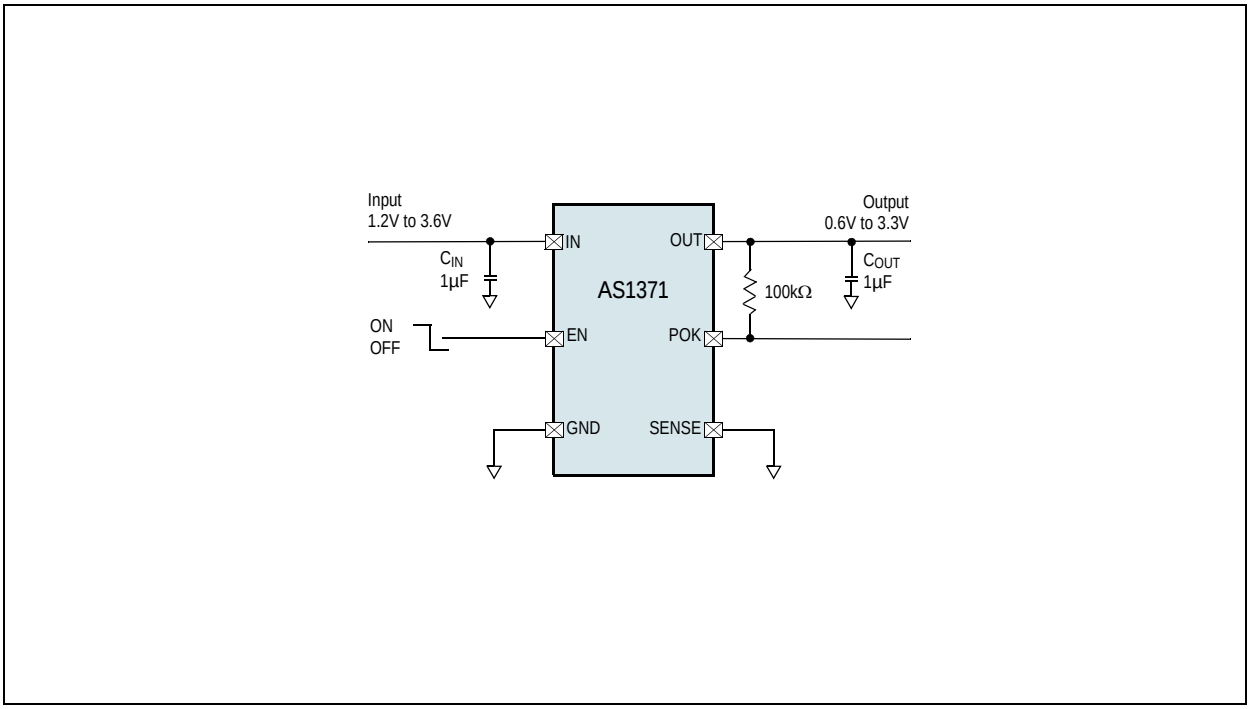
2 Key Features

- Ultra-Low Dropout Voltage: 20mV @ 100mA load
- Operating Input Voltage Range: 1.2V to 3.6V
- Output Voltages: 0.6V to 3.3V in 50mV steps
- Max. Output Current: 400mA
- Output Voltage Accuracy: ±1%
- Low Shutdown Current: 10nA
- Low Quiescent Current: 50µA @ max load
- Integrated Overtemperature/Overcurrent Protection
- Under-Voltage Lockout Feature
- Chip Enable Input
- Power-OK and Low Battery Detection
- Sense Input Option
- Minimal External Components Required
- Operating Temperature Range: -40°C to +85°C
- 6-pin 2x2 TDFN Package

3 Applications

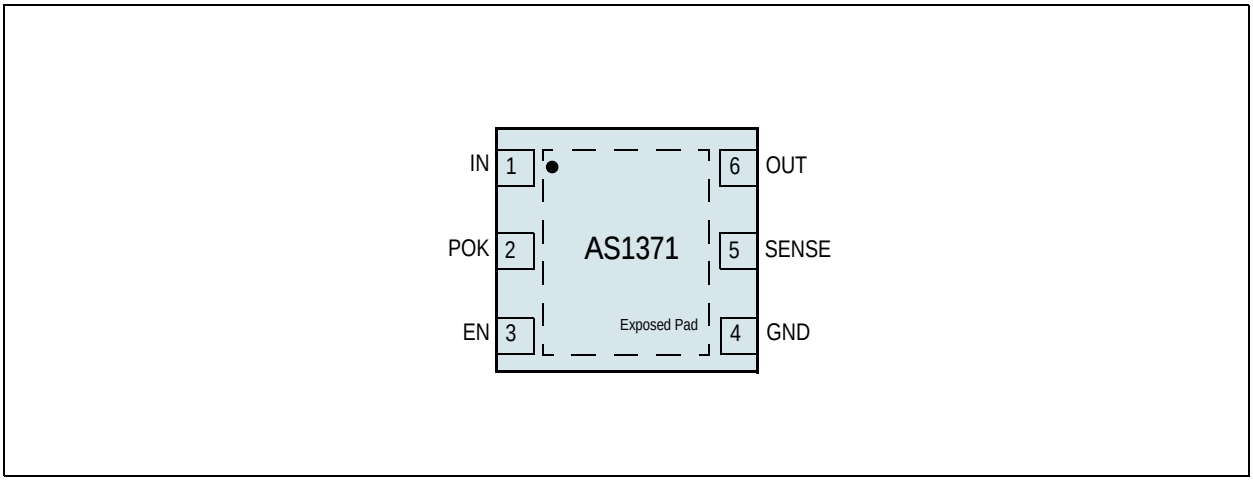
The devices are ideal for powering cordless and mobile phones, MP3 players, CD and DVD players, PDAs, hand-held computers, digital cameras, and any other hand-held and/or battery-powered device.

Figure 1. AS1371 - Typical Application Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	IN	LDO Input. Input voltage range: 1.2V to 3.6V. Bypass with 1µF to GND.
2	POK	Power-OK Output. Active-low, open-drain output indicates an out-of-regulation condition. Connect a 100kΩ pull-up resistor to pin OUT for logic levels. Leave this pin unconnected if the Power-OK feature is not used.
3	EN	Active-High Enable Input. A logic low reduces the supply current to < 1µA. Connect to pin IN for normal operation.
4	GND	Ground. This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.
5	SENSE	Sense Input. Represents the input for the Power-OK behavior. If connected to GND the POK output is related to OUT.
6	OUT	LDO Output. Bypass with 1µF to GND.
Exposed Pad	GND	Exposed Pad. This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation. Internally it is connected GND.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Electrical Parameters				
IN and EN to GND	-0.3	+5.0	V	
POK and OUT to GND	-0.3	V_{IN} + 0.3	V	
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic Discharge				
Electrostatic Discharge HBM		±1000	V	Norm: MIL 883 E method 3015
Temperature Ranges and Storage Conditions				
Thermal Resistance θ_{JA}	+78.6		ºC/W	Junction-to-ambient thermal resistance is very dependent on application and board-layout. In situations where high maximum power dissipation exists, special attention must be paid to thermal dissipation during board design.
Junction Temperature		+125	ºC	
Storage Temperature Range	-55	+125	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	1			Represents a maximum floor life time of unlimited

6 Electrical Characteristics

V_{IN} = V_{OUT} (Nominal) + 0.5V, EN = IN, C_{IN} = C_{OUT} = 1µF, T_{AMB} = -40°C to +85ºC (unless otherwise specified).
Typical Values are at T_{AMB} = +25ºC.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{AMB}	Operating Temperature Range		-40		+85	°C
V_{IN}	Input Voltage		1.2		3.6	V
V_{OUT}	Output Voltage	Available in 50mV steps, see Ordering Information on page 16	0.6		3.3	V
	Output Voltage Accuracy	T_{AMB} = +25ºC, I_{OUT} = 1mA, V_{OUT} > 1V	-2		+2	%
		T_{AMB} = -40 to +85ºC, I_{OUT} = 1mA, V_{OUT} > 1V	-3.5		+3.5	
I_{OUT}	Maximum Output Current		400			mA
I_{LIM}	Current Limit			650		mA
I_Q	Quiescent Current	I_{OUT} = 0mA		15	20	µA
		I_{OUT} = 400mA		50		
V_{IN}-V_{OUT}	Dropout Voltage[1]	I_{OUT} = 100mA		20	50	mV
		I_{OUT} = 400mA		80		
ΔV_{LNR}	Line Regulation	I_{OUT} = 1mA	-15	0	+15	mV
ΔV_{LDR}	Load Regulation	I_{OUT} = 1mA to 400mA		0.003		%/mA
	Output Voltage Noise	f = 10Hz to 100kHz, I_{OUT} = 10mA		100		μV_{RMS}
PSRR	Output Voltage AC Power-Supply Rejection Ratio	f = 10kHz, I_{OUT} = 10mA		50		dB
C_{OUT}	Output Capacitor	Load Capacitor Range	0.47	1		µF
		ESR Load			500	mΩ
Shutdown[2]						
t_{ON}	Exit Delay from Shutdown[3,4]			90	150	µs
I_{OFF}	Enable Supply Current	EN = GND, T_{AMB} = +25ºC		0.01	1	µA
		EN = GND, T_{AMB} = +85ºC		0.04		
V_{IH}	Enable Input Threshold		1.0			V
V_{IL}					0.4	
I_{EN}	Enable Input Bias Current	EN = IN or GND, T_{AMB} = +25ºC		0.03	100	nA
		EN = IN or GND, T_{AMB} = +85ºC		0.2		
Power-OK Output						
V_{POK}	Power-OK Voltage Threshold[5]	SENSE = GND, $V_{POKFALLING}$	90	94	97	% V_{OUT}
		SENSE = GND, Hysteresis		1		
V_{SENSE}	Power-OK Sense Voltage Threshold	V_{OUT} = 1.05V, V_{SENSE} falling	650	800	950	mV
		Hysteresis		50		
V_{OL}	POK Output Voltage Low	I_{SINK} = 100µA			0.4	V

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{POK}	POK Output Leakage Current	$0 \leq V_{POK} \leq 3.6V$, T_{AMB} = +25ºC, V_{OUT} in regulation			1	µA
Thermal Protection						
T_{SHDN}	Thermal Shutdown Temperature			150		ºC
ΔT_{SHDN}	Thermal Shutdown Hysteresis			15		ºC

1. Dropout voltage = V_{IN} - V_{OUT} when V_{OUT} is 100mV < V_{OUT} for V_{IN} = $V_{OUT(NOM)}$ +0.5V (applies only to output voltages ≥ 1.3V).
2. The rise and fall time of the shutdown signal must not exceed 1ms.
3. The delay time is defined as time required to set V_{OUT} to 95% of its final nominal value.
4. Guaranteed by design.
5. The functionality is proven by production test, limits are guaranteed by design.

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

7 Typical Operating Characteristics

VOUT = 1.8V, VIN = *2.3V,* IOUT = 1mA, TAMB = +25°C (unless otherwise specified).

Figure 3. Output Voltage vs. Temperature

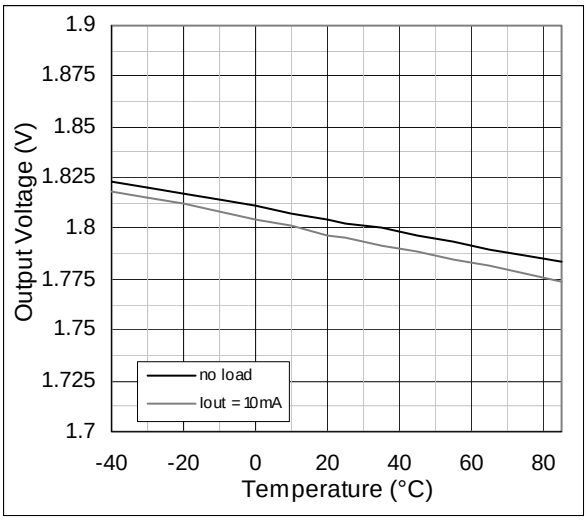


Figure 4. Line Regulation, VOUT vs. VIN

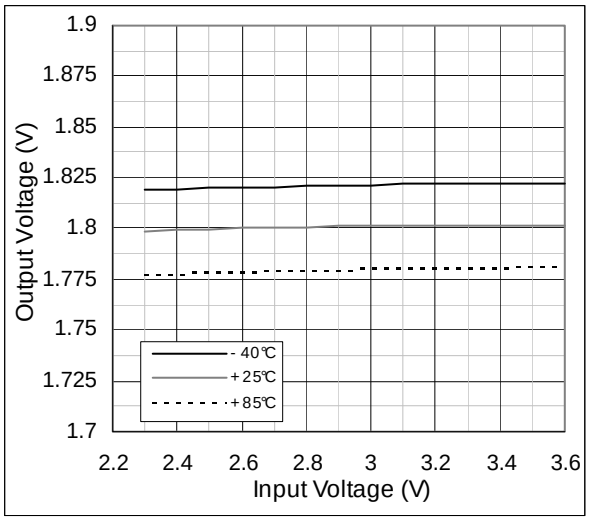


Figure 5. Load Regulation, VOUT vs. IOUT

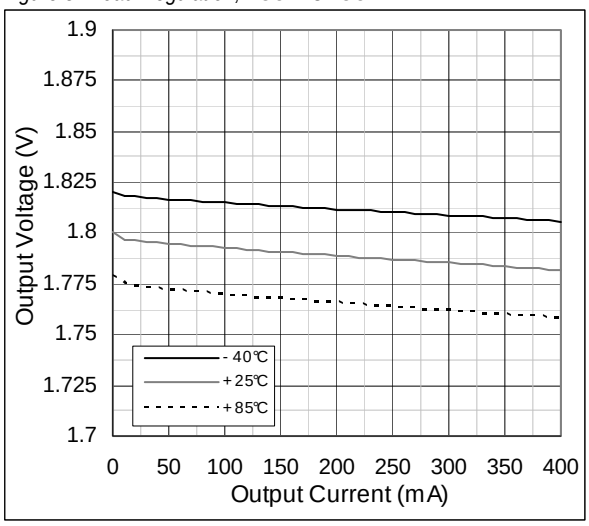


Figure 6. Quiescent Current vs. Input Voltage

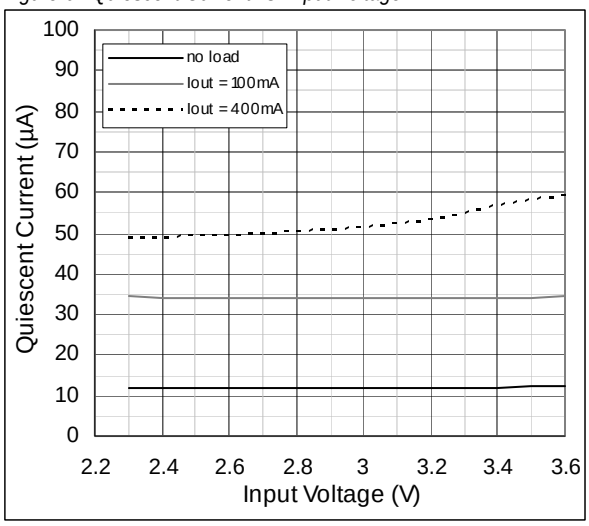


Figure 7. POK Voltage Threshold vs. Temperature

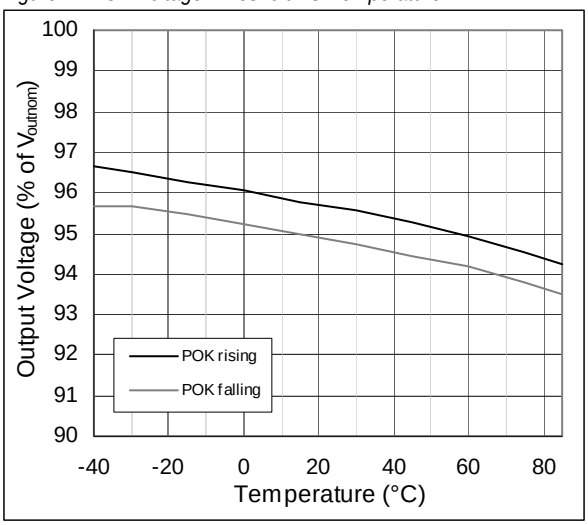


Figure 8. Dropout Voltage vs. Output Current

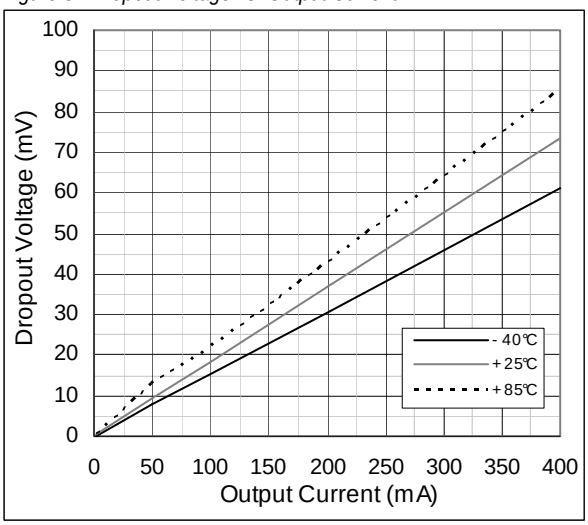


Figure 9. Line Transient Response; V_{IN} = 2.3V to 2.8V, No load

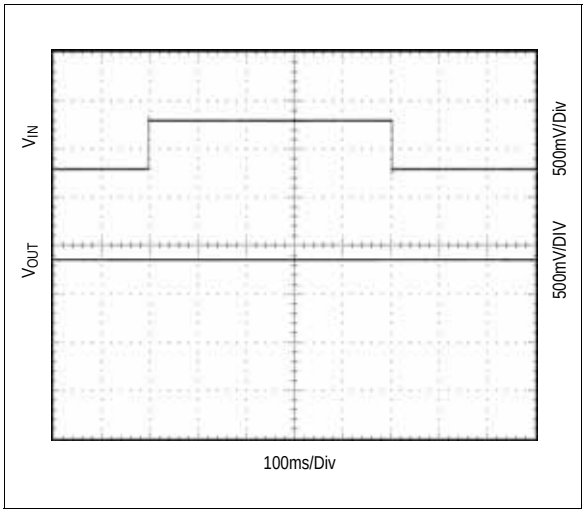


Figure 10. Load Transient Response; I_{OUT} = 0mA to 100mA

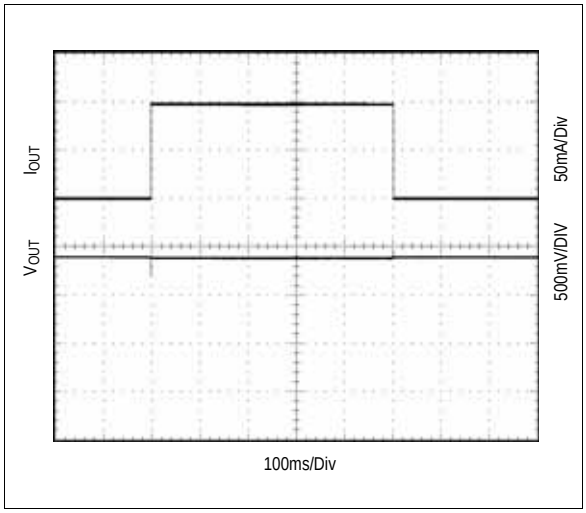


Figure 11. Turn ON

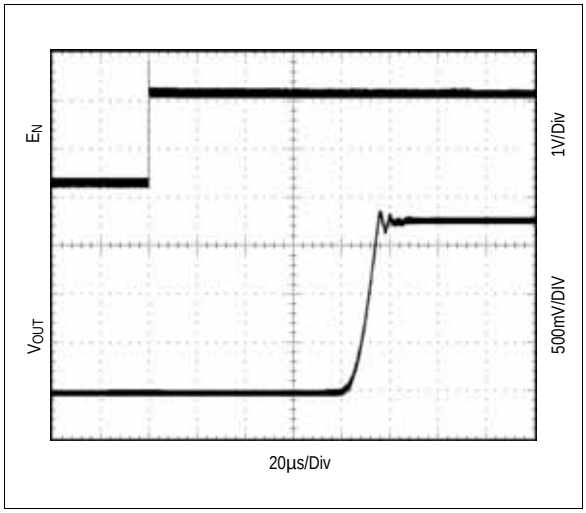
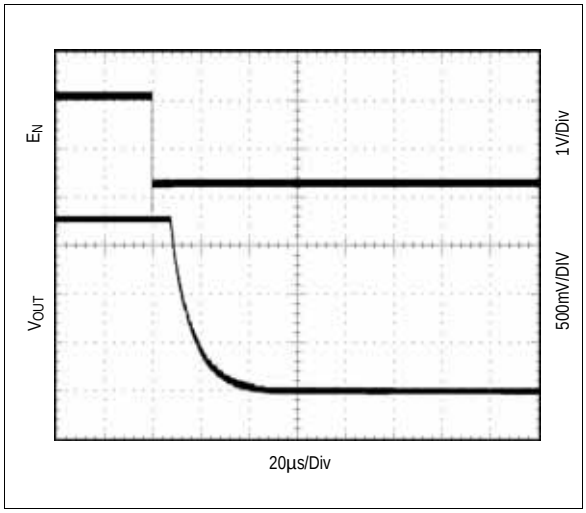


Figure 12. Turn OFF



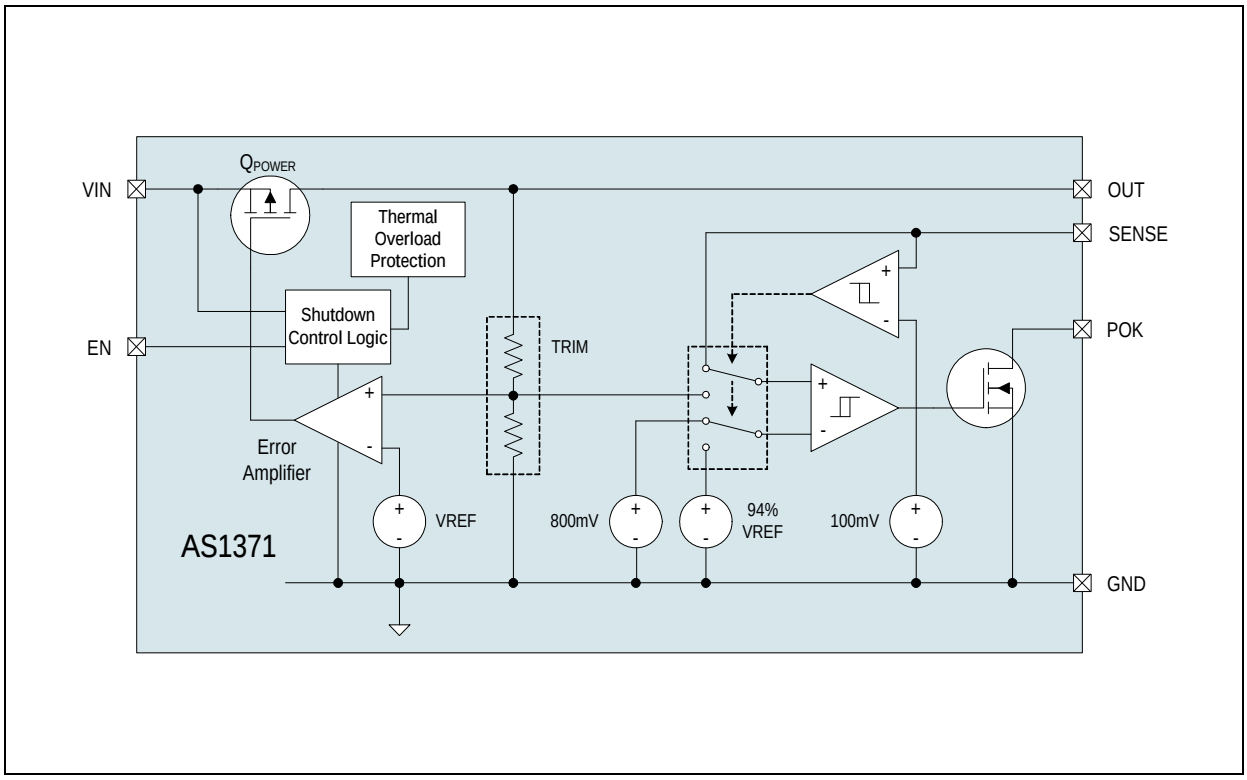
8 Detailed Description

The AS1371 is a low-dropout, low-quiescent-current linear regulator intended for LDO regulator applications where output current load requirements range from no load to 400mA. All devices come with fixed output voltage from 0.6V to 3.3V. See Ordering Information on page 16.

The AS1371 also features a Power-OK output to indicate when the output is within 10% (max) of final value when the Enable pin is grounded. When the Enable pin is raised above ground, the POK comparator inputs are switched to change the functionality. The comparator reference is now 800mV and the Enable pin becomes an uncommitted comparator input. See Power-OK and Low-Battery-Detect Functionality (page 9) for setting resistor values when monitoring other voltages (i.e. VOUT). Shutdown current for the whole regulator is typically 10nA. The device features integrated short-circuit and over current protection. Under-Voltage lockout prevents erratic operation when the input voltage is slowly decaying (e.g. in a battery powered application). Thermal Protection shuts down the device when die temperature reaches 150°C. This is a useful protection when the device is under sustained short circuit conditions.

Figure 13 shows the block diagram of the AS1371. It identifies the basics of a series linear regulator employing a P-Channel MOSFET as the control element. A stable voltage reference (REF in Figure 13) is compared with an attenuated sample of the output voltage. Any difference between the two voltages (reference and sample) creates an output from the error amplifier that drives the series control element to reduce the difference to a minimum. The error amplifier incorporates additional buffering to drive the relatively large gate capacitance of the series pass P-channel MOSFET, especially under transient conditions, when additional drive current is required. Input supply variations are absorbed by the series element, and output voltage variations with loading are absorbed by the low output impedance of the regulator.

Figure 13. AS1371 - Block Diagram



8.1 Output Voltages

Standard products are factory-set with output voltages from 0.6V to 3.3V. A two-digit suffix of the part number identifies the nominal output (see Ordering Information on page 16). Non-standard devices are available.

For more information contact: http://www.austriamicrosystems.com/contact

8.2 Power-OK and Low-Battery-Detect Functionality

The AS1371's power-ok or low-battery-detect circuitry is built around an N-channel MOSFET. The circuitry monitors the voltage on pin SENSE and if the voltage goes out of regulation (e.g. during dropout, current limit or thermal shutdown) the pin POK goes low. The pin SENSE can be connected to a resistive-divider to monitor a particular definable voltage and compare it with an internal voltage reference. If the SENSE pin is connected to GND an internal resistive-divider is activated and connected to the output. Therefore, the Power-OK functionality can be realized with no additional external components.

The Power-OK feature is not active during shutdown and provides a power-on-reset function that can operate down to V_{IN} = 1.2V. A capacitor to GND may be added to generate a power-on-reset delay. To obtain a logic-level output, connect a pull-up resistor from pin POK to pin OUT. Larger values for this resistor will help to minimize current consumption; a 100kΩ resistor is perfect for most applications (see Figure 1 on page 1).

For the circuit shown in the left of Figure 14 on page 9, the input bias current into SENSE is very low, permitting large-value resistor-divider networks while maintaining accuracy. Place the resistor-divider network as close to the device as possible. Use a defined resistor for R_2 and then calculate R_1 as:

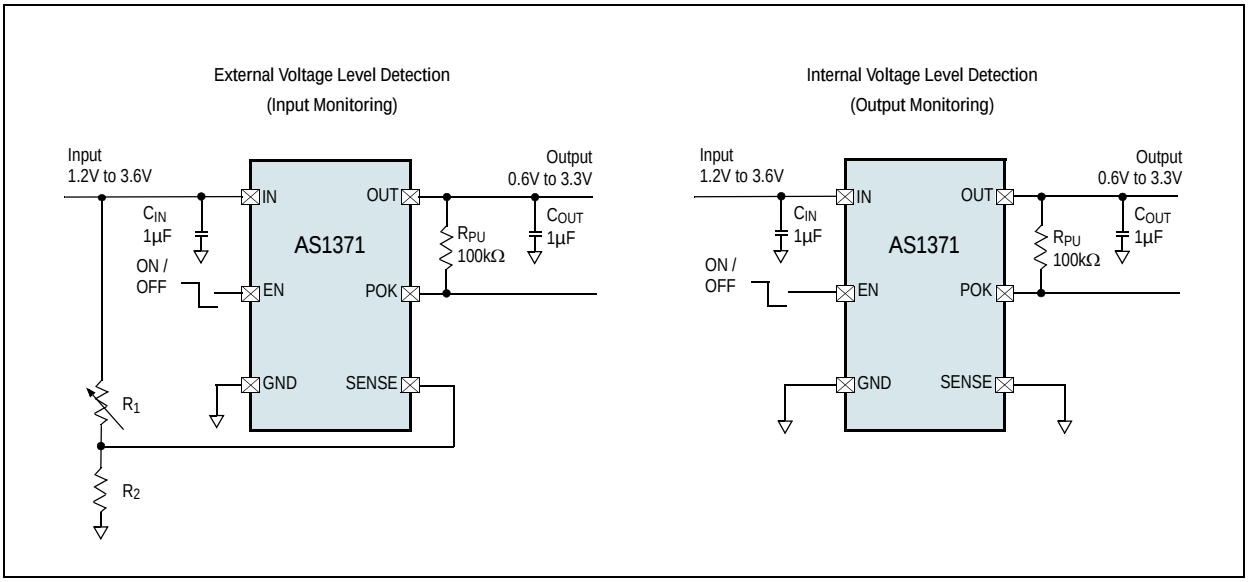
$$R_1 = R_2 \times \left(\frac{V_{IN}}{V_{SENSE}} - 1 \right) \quad \textit{(EQ 1)}$$

Where:

V_{SENSE} = 800mV ± 150mV.

In case of the SENSE pin is connected to GND, an internal resistor-divider network is activated and compares the output voltage with a 94% (typ.) voltage threshold. For this particular Power-OK application, no external resistive components are necessary.

Figure 14. Application Diagrams



8.3 Current Limiting

The AS1371 include current limiting circuitry to protect against short-circuit conditions. The circuitry monitors and controls the gate voltage of the P-channel MOSFET, limiting the output current to 400mA. The P-channel MOSFET output can be shorted to ground for an indefinite period of time without damaging the device.

8.4 Thermal-Overload Protection

The devices are protected against thermal runaway conditions by the integrated thermal sensor circuitry. Thermal shutdown is an effective instrument to prevent die overheating since the power transistor is the principle heat source in the device.

If the junction temperature exceeds 150ºC with 15ºC hysteresis, the thermal sensor starts the shutdown logic, at which point the P-channel MOSFET is switched off. After the device temperature has dropped by approximately 15ºC, the thermal sensor will turn the P-channel MOSFET on again. Note that this will be exhibited as a pulsed output under continuous thermal-overload conditions.

9 Application Information

9.1 Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different currents and, in particular at the regulator maximum one. From this is obtained the MOSFET maximum series resistance over temperature etc. More generally:

$$V_{DROPOUT} = I_{LOAD} \times R_{SERIES} \quad \textit{(EQ 2)}$$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful “end of life” of the battery before replacement or re-charge is required.

Figure 15. Graphical Representation of Dropout Voltage

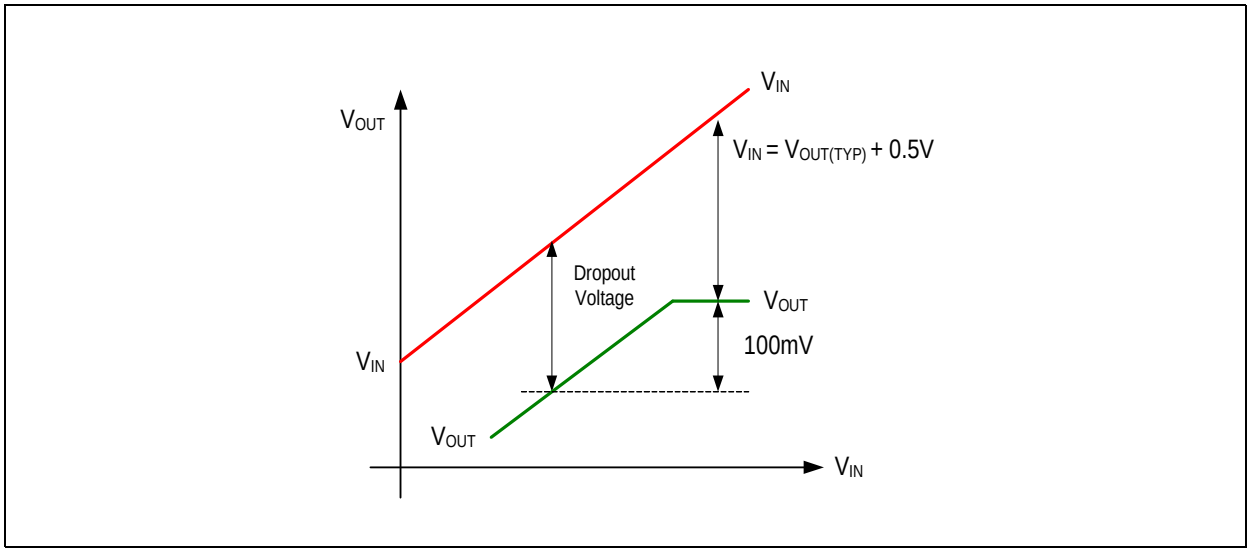


Figure 15 shows the variation of VOUT as VIN is varied for a certain load current. The practical value of dropout is the differential voltage (VOUT-VIN) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

9.2 Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

$$\textit{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN}(I_Q + I_{LOAD})} \times 100\ \% \quad \textit{(EQ 3)}$$

Where:
I_Q = Quiescent current of LDO

9.3 Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier, and is calculated as:

$$PD_{(MAX)}(Seriespass) = I_{LOAD(MAX)}(V_{IN(MAX)} - V_{OUT(MIN)})\ \textit{Watts} \quad \textit{(EQ 4)}$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD_{(MAX)}(Bias) = V_{IN(MAX)} I_Q\ \textit{Watts} \quad \textit{(EQ 5)}$$

Total LDO power dissipation is calculated as:

$$PD_{(MAX)}(Total) = PD_{(MAX)}(Seriespass) + PD_{(MAX)}(Bias)\ \textit{Watts} \quad \textit{(EQ 6)}$$

9.4 Junction Temperature

Under all operating conditions, the maximum junction temperature should not be allowed to exceed 125ºC (unless the data sheet specifically allows). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case (θ_{JC}ºC/W fixed by the IC manufacturer), and adjustment of the case to ambient heat path (θ_{CA}ºC/W) by manipulation of the PCB copper area adjacent to the IC position.

Figure 16. Package Physical Arrangements

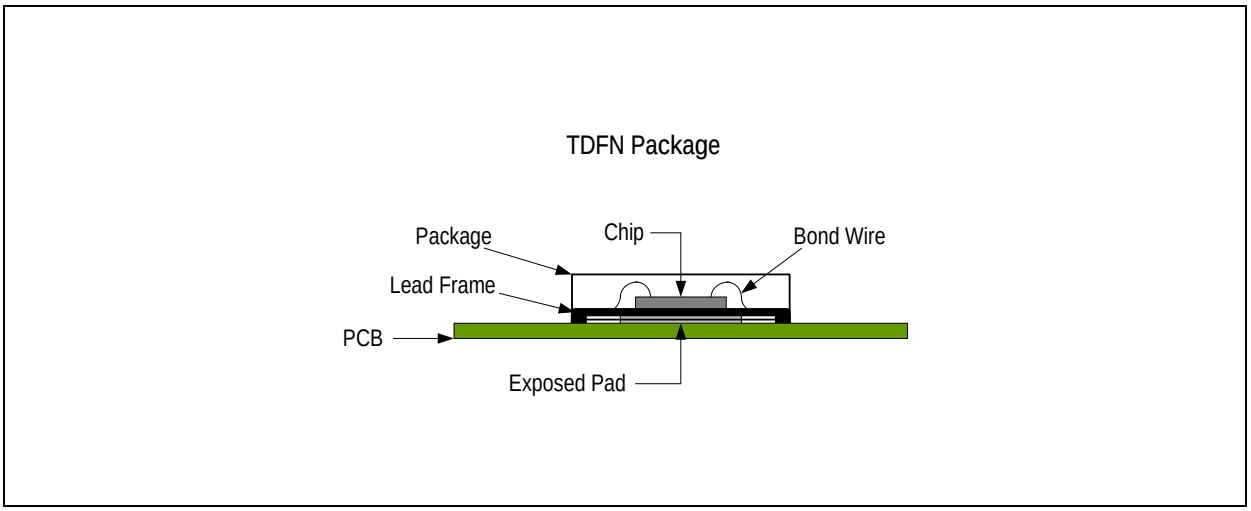
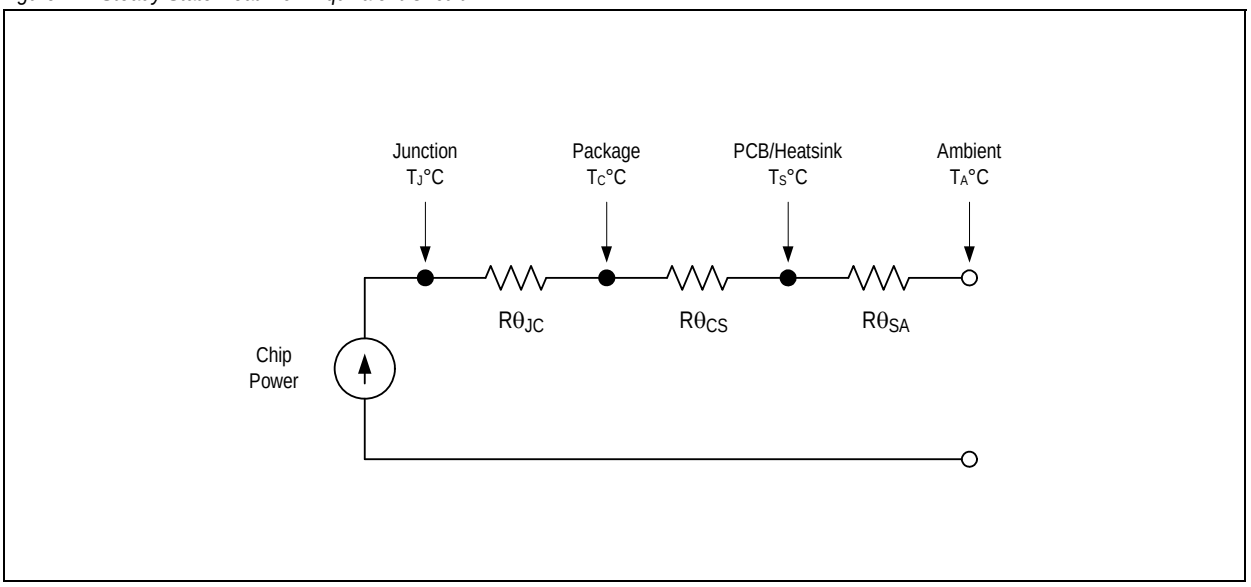


Figure 17. Steady State Heat Flow Equivalent Circuit



Total Thermal Path Resistance:

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA} \quad \textit{(EQ 7)}$$

Junction Temperature (T_JºC) is determined by:

$$T_J = (PD_{(MAX)} \times R\theta_{JA}) + T_{AMB}\ ºC \quad \textit{(EQ 8)}$$

9.5 Explanation of Steady State Specifications

9.5.1 Line Regulation

Line regulation is defined as the change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier. More generally:

$$\textit{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \textit{ and is a pure number} \qquad \textit{(EQ 9)}$$

In practise, line regulation is referred to the regulator output voltage in terms of % / VOUT. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \textit{ \% / V} \qquad \textit{(EQ 10)}$$

9.5.2 Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \textit{ and is units of ohms (}\Omega\textit{)} \qquad \textit{(EQ 11)}$$

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \frac{100}{\Delta V_{OUT}} \textit{ \% / mA} \qquad \textit{(EQ 12)}$$

9.5.3 Setting Accuracy

Accuracy of the final output voltage is determined by the accuracy of the ratio of R1 and R2, the reference accuracy and the input offset voltage of the error amplifier. When the regulator is supplied pre-trimmed, the output voltage accuracy is fully defined in the output voltage specification.

When the regulator has a SET or SENSE terminal, the output voltage may be adjusted externally. In this case, the tolerance of the external resistor network must be incorporated into the final accuracy calculation. Generally:

$$V_{OUT} = (V_{SET} \pm \Delta V_{SET})\left(1 + \frac{R1 \pm \Delta R1}{R2 \pm \Delta R2}\right) \qquad \textit{(EQ 13)}$$

The reference tolerance is given both at 25ºC and over the full operating temperature range.

9.5.4 Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

Total % Accuracy = Setting % Accuracy + Load Regulation % + Line Regulation % *(EQ 14)*

9.6 Explanation of Dynamic Specifications

9.6.1 Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions. Generally:

$$\textit{PSSR} = 20Log\frac{\delta V_{OUT}}{\delta V_{IN}} \textit{ dB using lower case } \delta \textit{ to indicate AC values} \qquad \textit{(EQ 15)}$$

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally.

9.6.2 Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a limit statement in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations in temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below T_{AMB} = -10ºC. With X7R or X5R capacitors, a 1µF capacitor should be sufficient at all operating temperatures.

Larger output capacitor values (10µF) help to reduce noise and improve load transient-response, stability and power-supply rejection.

9.6.3 Input Capacitor

An input capacitor at V_{IN} is required for stability. It is recommended that a 1.0µF capacitor be connected between the AS1371 power supply input pin V_{IN} and ground (capacitance value may be increased without limit subject to ESR limits). This capacitor must be located at a distance of not more than 1cm from the V_{IN} pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

9.6.4 Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems.

9.6.5 Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This “propagation time” is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times R_{ESR} \quad \textit{Units are Volts, Amps, Ohms.} \qquad \textit{(EQ 16)}$$

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approx. linear in time and sums with the ESR contribution to make a total transient variation at the output of:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times \left(R_{ESR} + \frac{T}{C_{LOAD}} \right) \quad \textit{Units are Volts, Seconds, Farads, Ohms.} \qquad \textit{(EQ 17)}$$

Where:
C_{LOAD} is output capacitor
T = Propagation delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for t < “propagation time”, so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance 50mA load current step produces 50mV output drop if the LDO response is 1usec and the load cap is 1µF.

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

9.6.6 Turn On Time

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the enable pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at V_{IN} is stable and within the regulator min and max limits. Shutdown reduces the quiescent current to very low, mostly leakage values (<1µA).

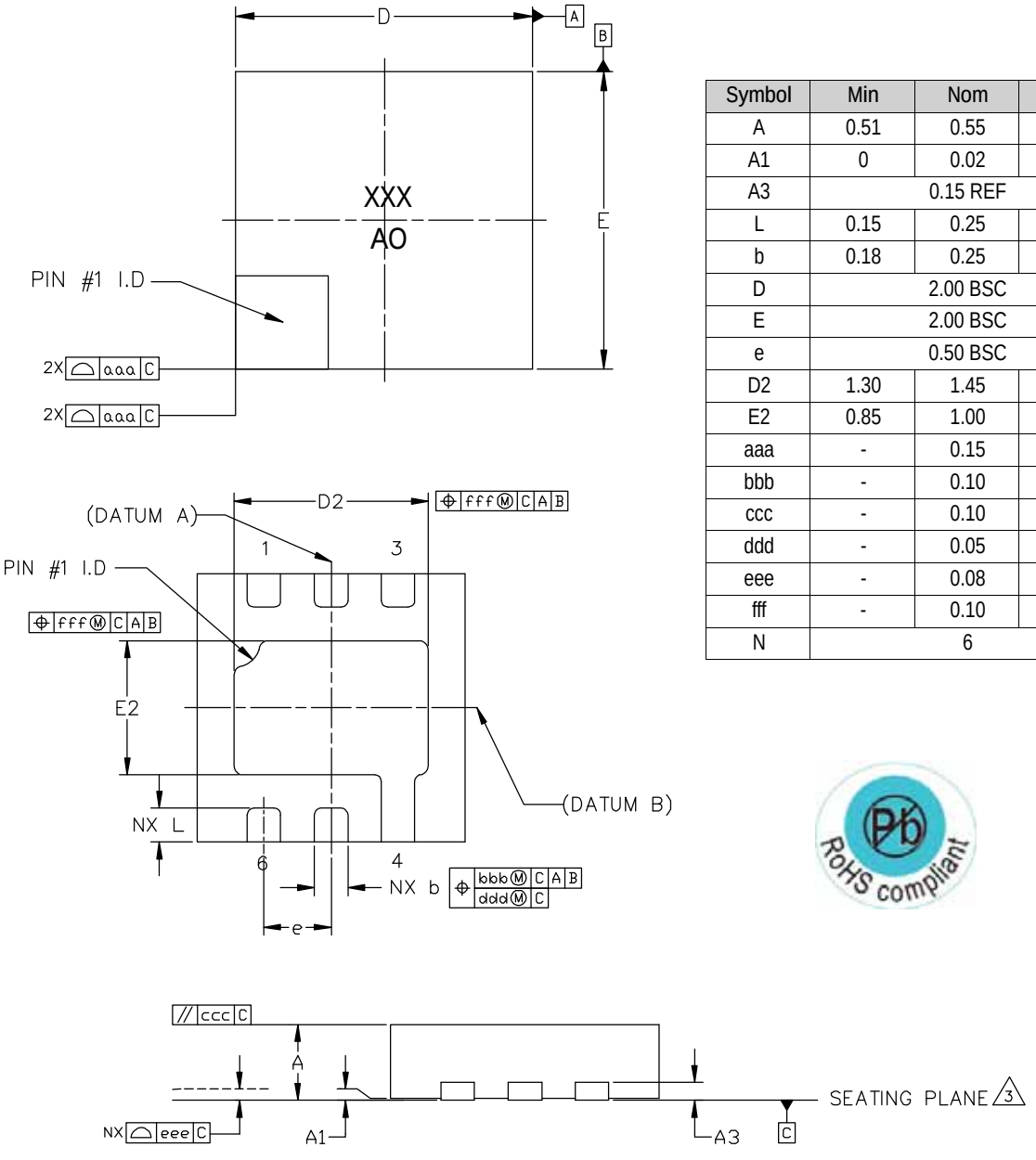
9.6.7 Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a 150ºC threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of 20ºC prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

10 Package Drawings and Markings

The device is available in a 6-pin 2x2 TDFN package.

Figure 18. Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.51	0.55	0.60
A1	0	0.02	0.05
A3		0.15 REF	
L	0.15	0.25	0.35
b	0.18	0.25	0.30
D		2.00 BSC	
E		2.00 BSC	
e		0.50 BSC	
D2	1.30	1.45	1.10
E2	0.85	1.00	
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		6	

Notes:

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Revision History

Revision	Date	Owner	Description
1.5		afe	
1.6	02 Jan, 2012		Changes made across the document

Note: Typos may not be explicitly mentioned under revision history.

11 Ordering Information

The device is available as the standard products listed in Table 4.

Table 4. Ordering Information

Ordering Code	Marking	Output	Description	Delivery Form	Package
AS1371-BTDT-105	AO	1.05V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-12[1]	AM	1.2V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-15[1]	AN	1.5V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-18[1]	AT	1.8V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-20[1]	AP	2.0V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-25[1]	AQ	2.5V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-30[1]	AR	3.0V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-SAMPLE[1]	AS	V_{OUT}[2]	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN

1. Available on request.
2. Non-standard devices from 0.6V to 3.3V are available in 50mV steps.

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