AS1500/AS1501/AS1502/AS1503

DataSheet

Digital Potentiometer

1 General Description

The AS1500 is a digital potentiometer with 256 programmable steps. The values of the resistor can be controlled via 3 wire serial interface capable to handle programming rates up to 10MHz.

The AS1500 is available in four different resistor values. The AS1500 incorporates a 10kΩ, the AS1501 a 20kΩ, the AS1502 a 50kΩ and the AS1503 a 100kΩ fixed resistor. The wiper contact taps the fixed resistor at points determined by the 8-bit digital code word. The resistance between the wiper and the endpoint of the resistor is linear. The switching action is performed in a way that no glitches occur.

The AS150x is available in an 8-pin SOIC package. All parts are guaranteed to operate over the extended industrial temperature range of –40º to +125º.

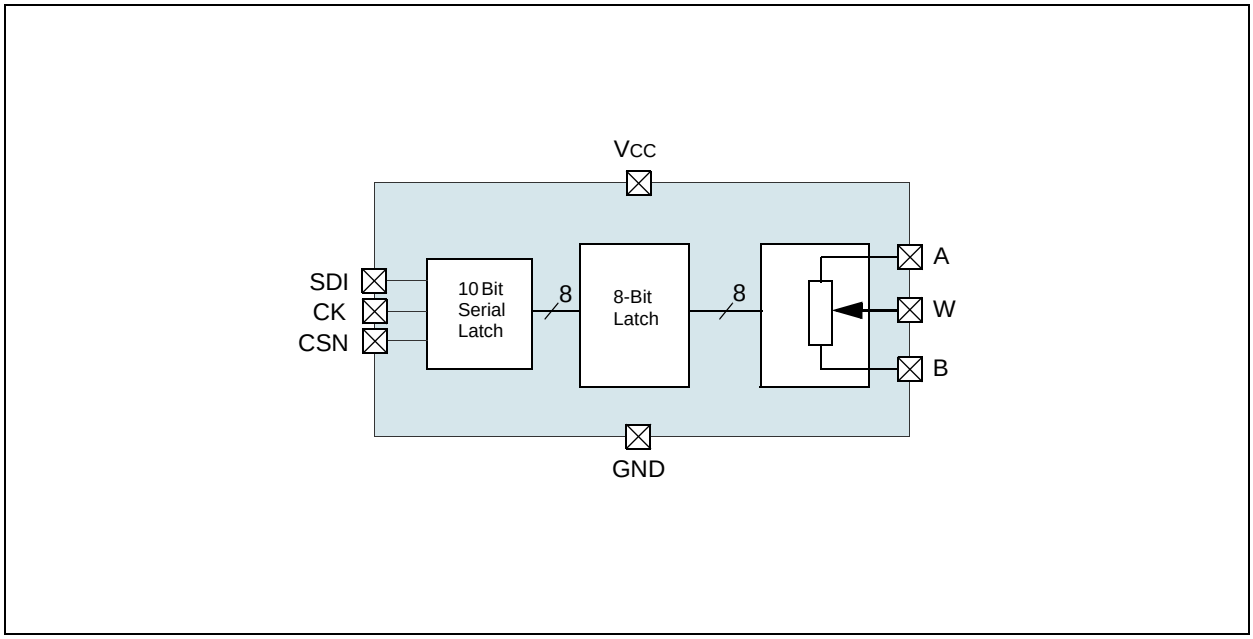
2 Key Features

- 256 - Taps
- Available in four Resistance values
  - AS1500 resistance 10kΩ
  - AS1501 resistance 20kΩ
  - AS1502 resistance 50kΩ
  - AS1503 resistance 100kΩ
- Standby current - Less than 1 µA
- 3-Wire Serial Data Interface
- 10 MHz Update Data Loading Rate
- 2.7 V to 5.5 V Single-Supply Operation
- Temperature Range –40º to +125º
- 8-pin SOIC Package

3 Applications

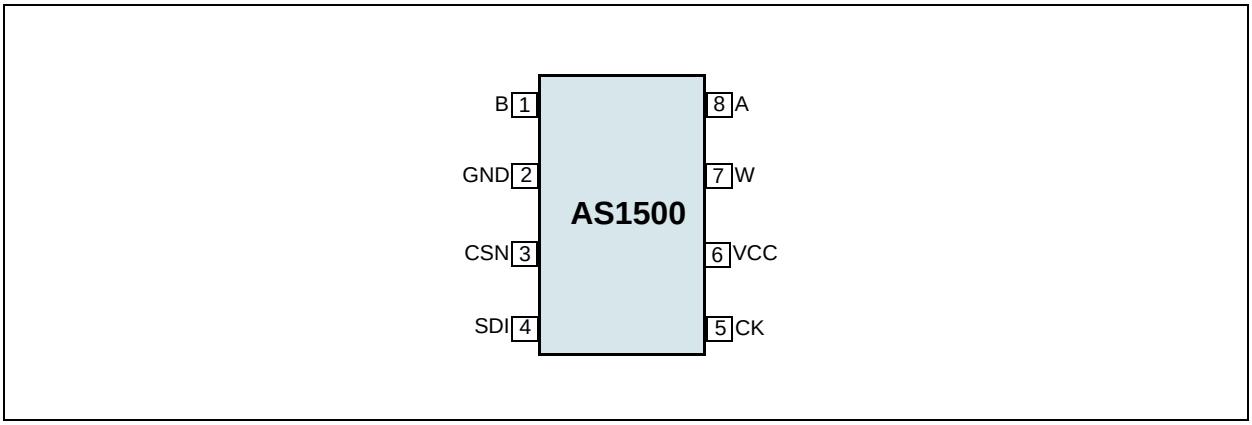
The AS1500 is ideal for volume controls in TV sets and audio systems, and applications that require line impedance matching, programmable filters or power supply adjustment. The AS1500 can also be designed in as a replacement for mechanical potentiometers.

Figure 1. Application Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Description

Pin Name	Pin Number	Description
B	1	**Terminal B** RDAC
GND	2	**Ground**
CSN	3	**Chip Select Input**, Active Low. When CSN returns high, data in the serial input register is loaded into the DAC register.
SDI	4	**Serial Data Input**
CK	5	**Serial Clock Input**, Positive Edge Triggered.
VCC	6	**Positive power supply**, specified for operation at both 3V and 5V.
W	7	**Wiper RDAC**
A	8	**Terminal A RDAC**

5 Absolute Maximum Ratings

(TA = 25º C, unless otherwise noted)

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VCC to GND	-0.3	+7	V	
VA, VB, VW to GND	0	VCC	V	
AX – BX, AX – WX, BX – WX	±20		mA	
Digital Input and Output Voltage to GND	0	+7	V	
Operating Temperature Range	-40	+125	ºC	
Maximum Junction Temperature (TJ max)		+150	ºC	
Storage Temperature	-65	+150	ºC	
Package body temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Package Power Dissipation				(TJ max - TA) / θJA
ESD		1	kV	HBM MIL-Std883E 3015.7methods.

6 Electrical Characteristics

AS1500 / AS1501 – SPECIFICATIONS

V_{CC} = 3V±10% or 5V±10%, $V_A = V_{CC}$, V_B = 0V, –40ºC ≤ T_A ≤ +125ºC unless otherwise noted.

Table 3. Electrical Characteristics – 10k and 20k Versions

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
DC Characteristics Rheostat Mode						
R_{AB}	Nominal Resistance[2]	T_A = 25ºC, V_{CC} = 5V, AS1500, Version: 50kΩ	8	10	12	kΩ
		T_A = 25ºC, V_{CC} = 5V, AS1501, Version: 100kΩ	16	20	24	kΩ
$\Delta R_{AB}/\Delta T$	Resistance Tempco[3]	$V_{AB} = V_{CC}$, Wiper = No Connect		500		ppm/ºC
R_W	Wiper Resistance	V_{CC} = 5V	20	100	200	Ω
R-DNL	Resistor Differential NL[4]	R_{WB}, V_{CC} = 5V, V_A = No Connect	-1	±1/4	+1	LSB
R-INL	Resistor Integral NL	R_{WB}, V_{CC} = 5V, V_A = No Connect	-2	±1/2	+2	LSB
DC Characteristics Potentiometer Divider						
N	Resolution			8		Bits
INL	Integral Nonlinearity	V_{CC} = 5.5V T_A = 25ºC	-2	±1/2	+2	LSB
		V_{CC} = 2.7V T_A = 25ºC	-2	±1/2	+2	LSB
DNL	Differential Nonlinearity	V_{CC} = 5.5V T_A = 25ºC	-1	±1/4	+1	LSB
		V_{CC} = 2.7V T_A = 25ºC	-1	±1/4	+1	LSB
$\Delta V_W/\Delta T$	Voltage Divider Tempco	Code = 80_H		15		ppm/ºC
V_{WFSE}	Full-Scale Error	Code = FF_H, V_{CC} = 5.5V	-4	-2.8	0	LSB
V_{WFSE}	Zero-Scale Error	Code = 00_H, V_{CC} = 5.5V	0	1.3	2	LSB
Resistor Terminals						
$V_{A, B, W}$	Voltage Range[5]		0		V_{CC}	V
$C_{A, B}$	Capacitance[6] Ax, Bx	f =1MHz, Measured to GND, Code = 80_H		75		pF
C_W	Capacitance Wx	f =1MHz, Measured to GND, Code = 80_H		120		pF
Digital Inputs and Outputs						
V_{IH}	Input Logic High	V_{CC} = 5V	2.4			V
V_{IL}	Input Logic Low	V_{CC} = 5V			0.8	V
V_{IH}	Input Logic High	V_{CC} = 3V	2.1			V
V_{IL}	Input Logic Low	V_{CC} = 3V			0.6	V
I_{IH}, I_{IL}	Input Current	V_{IN} = 5V or 0V, V_{CC} = 5V			±1	µA
C_{IL}	Input Capacitance			5		pF
Power Supplies						
V_{CC}	Power Supply Range		2.7		5.5	V
I_{DD}	Supply Current (CMOS)	$V_{IH} = V_{CC}$ or V_{IL} = 0V, V_{CC} = 5.5V		0.1	1	µA
I_{DD}	Supply Current (TTL)[7]	V_{IH} = 2.4V or 0.8V, V_{CC} = 5.5V		0.9	4	mA

Table 3. Electrical Characteristics – 10k and 20k Versions

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Units
P_{DISS}	Power Dissipation (CMOS)[8]	V_{IH} = V_{CC} or V_{IL} = 0V, V_{CC} = 5.5V				27.5	µW
PSSR	Power Supply Suppression Ratio	V_{CC} = 5V+0.5V_P sine wave @ 1kHz	AS1500, Version: 10kΩ		-54	-25	dB
			AS1501, Version: 20kΩ		-52	-25	dB
Dynamic Characteristics[9]							
BW_10k	Bandwidth –3dB	R_{WB} = 10kΩ, V_{CC} = 5V			1000		kHz
BW_20k	Bandwidth –3dB	R_{WB} = 20kΩ, V_{CC} = 5V			500		kHz
THD_W	Total Harmonic Distortion	V_A = 1V_{RMS} + 2V_{DC}, V_B = 2V_{DC}, f = 1kHz			0.003		%
t_S_10k	VW Settling Time	R_{WB} = 5kΩ, V_A = V_{CC}, V_B = 0V, ±1% Error Band			2		µs
t_S_20k		R_{WB} = 10kΩ, V_A = V_{CC}, V_B = 0V, ±1% Error Band			4		µs
e_{NWB}_10k	Resistor Noise Voltage	R_{WB} = 5kΩ, f =1kHz			9		nV/ √ Hz
e_{NWB}_20k		R_{WB} = 10kΩ, f =1kHz			13		nV/ √ Hz

1. Typicals represent average readings at 25ºC and V_{CC} = 5V.
2. Wiper is not connected. I_{AB} = 350µA for the 10kΩ version and 175µA for the 20kΩ version.
3. All Tempcos are guaranteed by design and not subject to production test.
4. Terminal A is not connected. I_W = 350µA for the 10kΩ version and 175µA for the 20kΩ version.
5. Resistor terminals A, B, W have no limitations on polarity with respect to each other.
6. All capacitances are guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5V bias on the measured terminal. The remaining resistor terminals are left open circuit.
7. Worst-case supply current consumed when input logic level at 2.4V, standard characteristic of CMOS logic.
8. P_{DISS} is calculated from (I_{DD}×V_{CC}). CMOS logic level inputs result in minimum power dissipation.
9. All dynamic characteristics are guaranteed by design and not subject to production test. All dynamic characteristics use V_{CC}=5V.

AS1502 / AS1503 – SPECIFICATIONS

V_{CC} = 3V±10% or 5V±10%, V_A = V_{CC}, V_B = 0V, –40ºC ≤ T_A ≤ +125ºC unless otherwise noted.

Table 4. Electrical Characteristics – 50k and 100k Versions

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
DC Characteristics Rheostat Mode						
R_{AB}	Nominal Resistance[2]	T_A = 25ºC, V_{CC} = 5V, AS1502, Version: 50kΩ	40	50	60	kΩ
		T_A = 25ºC, V_{CC} = 5V, AS1503, Version: 100kΩ	80	100	120	kΩ
$\Delta R_{AB}/\Delta T$	Resistance Tempco[3]	V_{AB} = V_{CC}, Wiper = No Connect		500		ppm/ºC
R_W	Wiper Resistance	V_{CC} = 5V	20	100	200	Ω
R-DNL	Resistor Differential NL[4]	R_{WB}, V_{CC} = 5V, V_A = No Connect	-1	±1/4	+1	LSB
R-INL	Resistor Integral NL	R_{WB}, V_{CC} = 5V, V_A = No Connect	-2	±1/2	+2	LSB

Table 4. Electrical Characteristics – 50k and 100k Versions

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Units
DC Characteristics Potentiometer Divider							
N	Resolution				8		Bits
INL	Integral Nonlinearity	V_{CC} = 5.5V T_A = 25ºC		-4	±1	+4	LSB
		V_{CC} = 2.7V T_A = 25ºC		-4	±1	+4	LSB
DNL	Differential Nonlinearity	V_{CC} = 5.5V T_A = 25ºC		-1	±1/4	+1	LSB
		V_{CC} = 2.7V T_A = 25ºC		-1	±1/4	+1	LSB
$\Delta V_W / \Delta T$	Voltage Divider Tempco	Code = 80_H			15		ppm/ºC
V_{WFSE}	Full-Scale Error	Code = FF_H, V_{CC}= 5.5V		-1	-0.25	0	LSB
V_{WFSE}	Zero-Scale Error	Code = 00_H, V_{CC} = 5.5V		0	0.1	1	LSB
Resistor Terminals							
$V_{A, B, W}$	Voltage Range[5]			0		V_{CC}	V
$C_{A, B}$	Capacitance[6] Ax, Bx	f =1MHz, Measured to GND, Code = 80_H			15		pF
C_W	Capacitance Wx	f =1MHz, Measured to GND, Code = 80_H			80		pF
Digital Inputs and Outputs							
V_{IH}	Input Logic High	V_{CC} = 5V		2.4			V
V_{IL}	Input Logic Low	V_{CC} = 5V				0.8	V
V_{IH}	Input Logic High	V_{CC} = 3V		2.1			V
V_{IL}	Input Logic Low	V_{CC} = 3V				0.6	V
I_{IH}, I_{IL}	Input Current	V_{IN} = 5V or 0V, V_{CC} = 5V				±1	µA
C_{IL}	Input Capacitance				5		pF
Power Supplies							
V_{CC}	Power Supply Range			2.7		5.5	V
I_{DD}	Supply Current (CMOS)	V_{IH} = V_{CC} or V_{IL} = 0V, V_{CC} = 5.5V			0.1	1	µA
I_{DD}	Supply Current (TTL)[7]	V_{IH} = 2.4V or 0.8V, V_{CC} = 5.5V			0.9	4	mA
P_{DISS}	Power Dissipation (CMOS)[8]	V_{IH} = V_{CC} or V_{IL} = 0V, V_{CC} = 5.5V				27.5	µW
PSSR	Power Supply Suppression Ratio	V_{CC} = 5V+0.5V_P sine wave @ 1kHz	AS1502, Version: 50kΩ		-43		dB
			AS1503, Version: 100kΩ		-52		dB
Dynamic Characteristics[9]							
BW_50k	Bandwidth –3dB	R_{WB} = 50kΩ, V_{CC} = 5V			220		kHz
BW_100k	Bandwidth –3dB	R_{WB} = 100kΩ, V_{CC} = 5V			110		kHz
THD_W	Total Harmonic Distortion	V_A = 1V_{RMS} + 2V_{DC}, V_B = 2V_{DC}, f = 1kHz			0.003		%

Table 4. Electrical Characteristics – 50k and 100k Versions

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
t_{S}_50k	VW Settling Time	R_{WB} = 50kΩ, V_A = Vcc, V_B = 0V, ±1% Error Band		9		µs
t_{S}_100k		R_{WB} = 100kΩ, V_A = Vcc, V_B = 0V, ±1% Error Band		18		µs
e_{NWB}_50k	Resistor Noise Voltage	R_{WB} = 50kΩ, f =1kHz		20		nV/ √ Hz
e_{NWB}_100k		R_{WB} = 100kΩ, f =1kHz		29		nV/ √ Hz

1. Typicals represent average readings at 25ºC and Vcc = 5V.
2. Wiper is not connected. I_{AB} = 70µA for the 50kΩ version and 35µA for the 100kΩ version.
3. All Tempcos are guaranteed by design and not subject to production test.
4. Terminal A is not connected. I_W = 70µA for the 50kΩ version and 35µA for the 100kΩ version.
5. Resistor terminals A, B, W have no limitations on polarity with respect to each other.
6. All capacitances are guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5V bias on the measured terminal. The remaining resistor terminals are left open circuit.
7. Worst-case supply current consumed when input logic level at 2.4V, standard characteristic of CMOS logic.
8. P_{DISS} is calculated from (I_{DD}×Vcc). CMOS logic level inputs result in minimum power dissipation.
9. All dynamic characteristics are guaranteed by design and not subject to production test. All dynamic characteristics use Vcc=5V.

AS150x – SPECIFICATIONS

Vcc = 3V±10% or 5V±10%, V_A = Vcc, V_B = 0V, –40ºC ≤ T_A ≤ +125ºC unless otherwise noted.

Table 5. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Switching Characteristics[2 3]						
t_{CH}, t_{CL}	Input Clock Pulsewidth	Clock Level High or Low	50			ns
t_{DS}	Data Setup Time		5			ns
t_{DH}	Data Hold Time		5			ns
t_{CSS}	CSN Setup Time		10			ns
t_{CSWH}	CSN High Pulsewidth		10			ns
t_{CSWL}	CSN Low Pulsewidth				100	ms
t_{CSH}	CK Fall to CSN Rise Hold Time		0			ns
t_{CS1}	CSN Rise to Clock Rise Setup		10			ns

1. Typicals represent average readings at 25ºC and Vcc=5V.
2. Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5V bias on the measured terminal. The remaining resistor terminals are left open circuit.
3. See timing diagram for location of measured values. All input control voltages are specified with tR = tF = 1ns (10% to 90% of Vcc) and timed from a voltage level of 1.6V. Switching characteristics are measured using Vcc=3V or 5V. To avoid false clocking, a minimum input logic slew rate of 1V/µs should be maintained.

7 Detailed Description

Serial-Programming

Programming of the AS150x is done via the 3 wire serial interface. The three input signals are serial data input (SDI), clock(CK) and chip select (CSN). A programming sequence consists of 10-bit, where the last eight bit contain the code word for the resistor value. The first two bits A1 and A0 have to be low to program the resistor value (see Table 6). Otherwise the resistor value is not affected. The data is shifted into the internal 10 Bit register with the rising edge of the CK signal. With the rising edge of the CSN signal the data become valid and the resistance is updated (see Figure 3). A detailed block diagram is shown in Figure 4.

Table 6. Serial data format (10 bits)

A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	MSB				Data			LSB

Figure 3. Timing Diagram

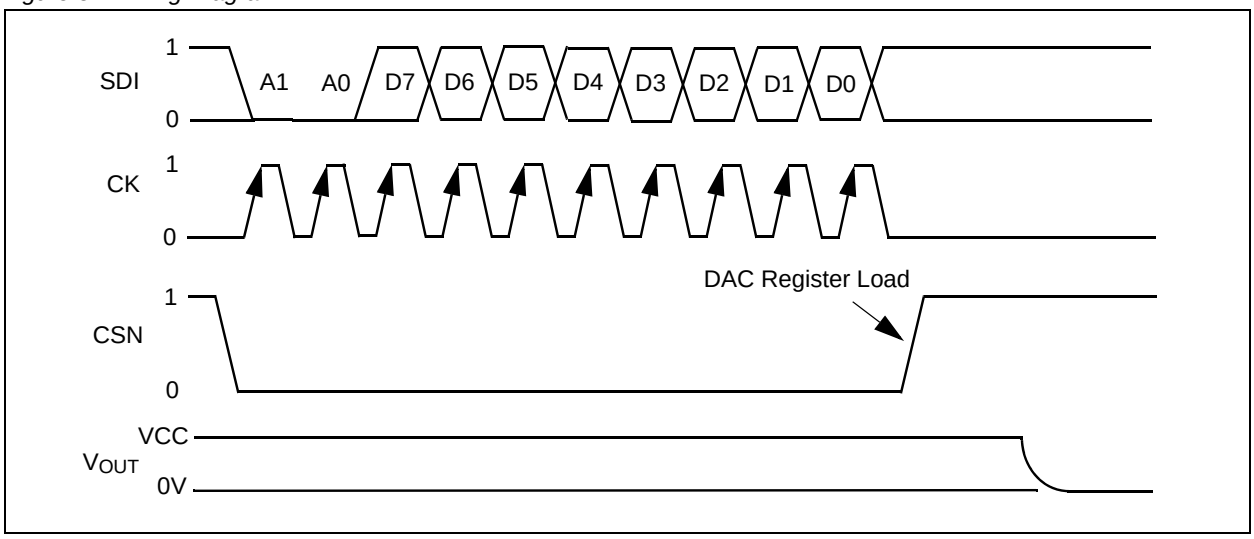
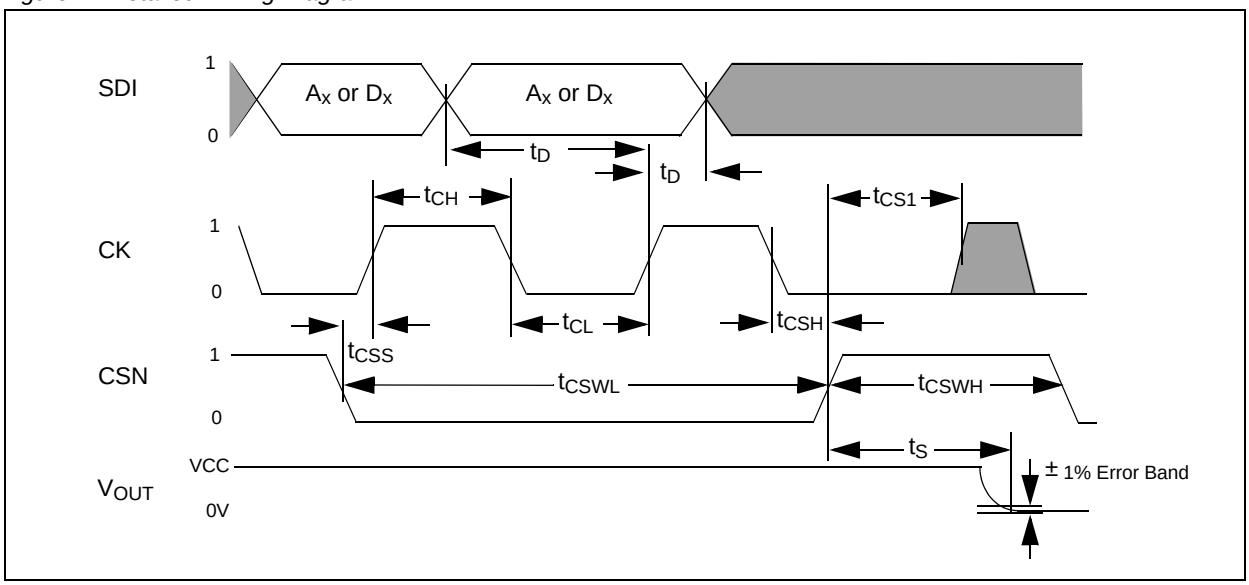


Figure 4. Detailed Timing Diagram



Rheostat Operation

The digital potentiometer family AS150x offers nominal resistor values of 10kΩ, 20kΩ, 50kΩ and 100kΩ. The resistor has 256 contact points where the wiper can access the resistor. The 8-bit code word determines the position of the wiper and is decoded through an internal logic. The lowest code 00h is related to the terminal B. The resistance is then only determined by the wiper resistance (100Ω). The resistance for the next code 01h is the nominal resistor RAB (10kΩ, 20kΩ, 50kΩ or 100kΩ) divided through 256 plus the wiper resistor. In case of AS1501 (10kΩ) the total resistance is 39Ω+100Ω=139Ω. Accordingly the resistor for code 02h is 78Ω+100Ω=178Ω. The last code 255h does not connect to terminal A directly (see Figure 5). So the maximum value is 10000Ω - 39Ω +100Ω = 10061Ω. The general formula for the calculation of the resistance R_{WB} is:

$$R_{WB}(Dx) = (Dx)/256 \bullet R_{AB} + R_W \qquad \text{(EQ 1)}$$

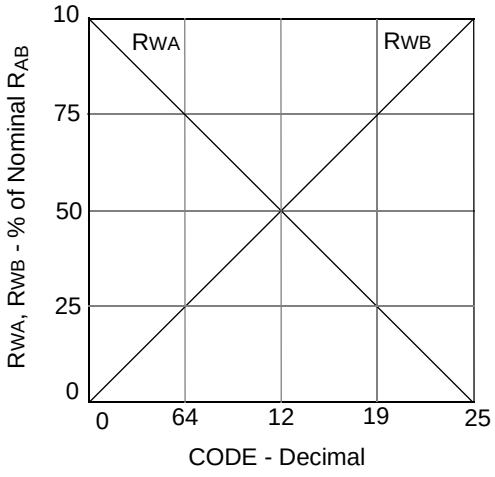
where R_{AB} is the nominal resistance between terminal A and B, R_W is the wiper resistance and D_X is the 8-Bit Code word. In Table 7 the resistor values between the wiper and terminal B for AS1500 are given for specific codes D_X. In the zero-scale condition the wiper resistance of 100Ω remains present.

Table 7. RDAC-Codes WB

D_X (Dec)	R_{WB} (Ω)	Output State
255	10061	Full Scale
128	5100	Midscale
1	139	1 LSB
0	100	Zero-Scale (Wiper Contact Resistance)

The maximum current through the wiper and terminal B is 5mA. If the current exceeds this limit the internal switches can degrade or even be damaged. As a mechanical potentiometer the resistances R_{WA} and R_{WB} are totally symmetrical. The relation between them is shown in Figure 5.

Figure 5. R_{WA} and R_{WB} versa code



The resistance R_{WA} is the complimentary resistor to R_{WB} and can be controlled digitally as well. R_{WA} starts at the maximum value of the nominal resistance and is reduced with increasing 8-Bit code words. The formula to calculate R_{WA} is given below:

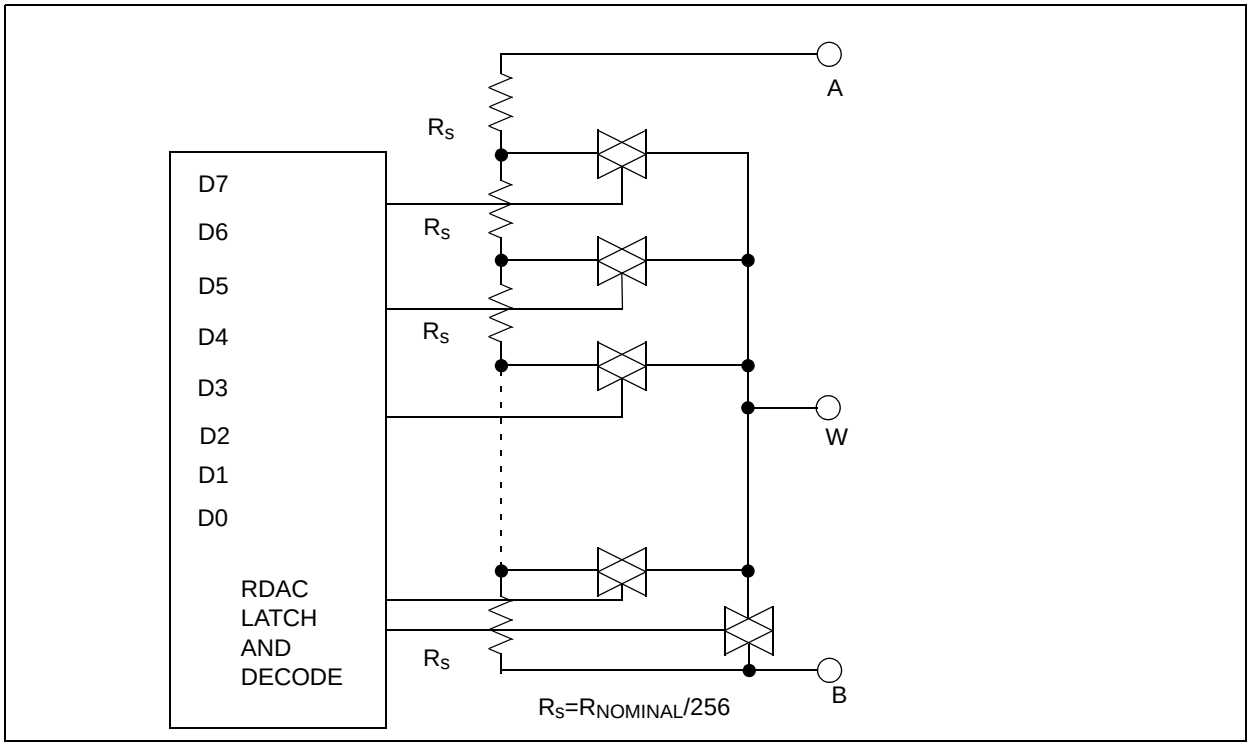
$$R_{WA}(Dx) = (256 - Dx)/256 \bullet R_{AB} + R_W \qquad (EQ\ 2)$$

where R_{AB} is the nominal resistance between terminal A and B, R_W is the wiper resistance and Dx is the 8-Bit Code word. In Table 8 the resistor values between the wiper and terminal B for AS1500 are given for specific codes Dx.

Table 8. RDAC-Codes WA

D_X (Dec)	R_{WA} (Ω)	Output State
255	89	Full Scale
128	5050	Midscale
1	10011	1 LSB
0	10050	Zero-Scale

Figure 6. Equivalent RDAC Circuit



Voltage Output Operation

The AS150x family can easily used in an voltage output mode, where the output voltage is proportional to an applied voltage to a given terminal. When 5V are applied to terminal A and B is set to ground the ouput voltage at the wiper starts at zero volts up to 1LSB less then 5V. One LSB of voltage corresponds to the voltage applied at terminal AB divided through 256 steps of possible wiper settings. The formula is given by

$$V_W(Dx) = (Dx)/256 \bullet V_{AB} + V_B \qquad (EQ\ 3)$$

where V_{AB} is the voltage applied between terminal A and B, VW is the voltage at the wiper, Dx is the 8-Bit Code word and V_B is the voltage at terminal B. The temperature drift is significant better than in Rheostat mode, since the temperature coefficient is determined by the internal resistor ratio. Therefore the temperature drift is only 15ppm/°C.

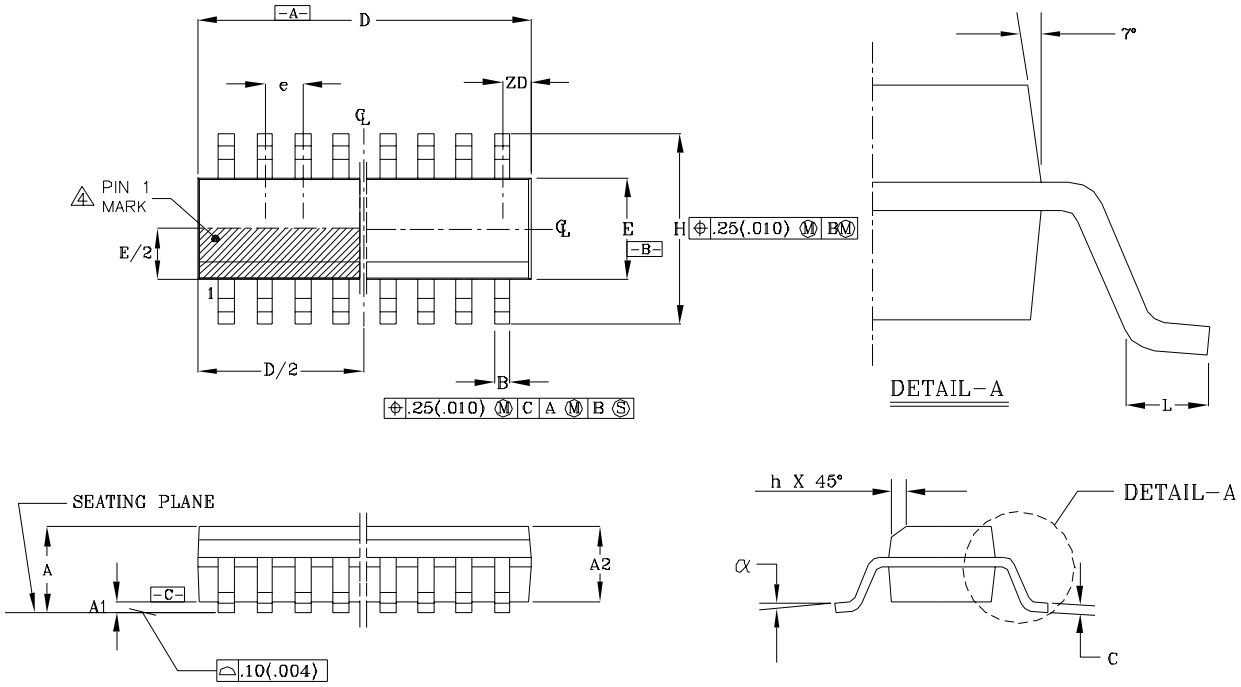
Applications

The digital potentiometer can replace in many applications the analog trimming potentiometer. The digital potentiometer is not sensitive to vibrations and shocks. It has an extremely small form-factor and can be adjusted very fast (e.g. AS1500 has an update rate of 600kHz). Furthermore the temperature drift, resolution and noise are significant better and cannot be achieved with a mechanical trimming potentiometer. Due to the programmability the resistor settings can be stored in the system memory, so that after a power down the exact settings can be recalled easily.

All analog signals must remain within 0 to V_{CC} range. For standard potentiometer applications the wiper output can be used directly. In the case of a low impedance load, a buffer shall be used.

8 Package Drawings and Markings

Figure 7. 8-pin SOIC Package



Notes:

1. Lead coplanarity should be 0 to 0.10mm (.004”) max.
2. Package surface finishing:
   (2.1) Top: matte (charmilles #18-30).
   (2.2) All sides: matte (charmilles #18-30).
   (2.3) Bottom: smooth or matte (charmilles #18-30).
3. All dimensions exclusive of mold flash, and end flash from the package body shall not exceed 0.24mm (0.10”) per side (D).
4. Details of pin #1 identifier are optional but must be located within the zone indicated.

Symbol	Min	Max
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27BSC	
H	5.80	6.20
h	0.25	0.50
L	.041	1.27
A	1.52	1.72
	0º	8º
ZD	0.53REF	
A2	1.37	1.57

9 Ordering Information

Table 9.

Model	Resistor	Delivery Form	Package	Description
AS1500	10kΩ	Tubes	8-pin SOIC	8-bit Digital Potentiometer
AS1501	20kΩ	Tubes	8-pin SOIC	8-bit Digital Potentiometer
AS1502	50kΩ	Tubes	8-pin SOIC	8-bit Digital Potentiometer
AS1503	100kΩ	Tubes	8-pin SOIC	8-bit Digital Potentiometer
AS1500-T	10kΩ	T&R	8-pin SOIC	8-bit Digital Potentiometer
AS1501-T	20kΩ	T&R	8-pin SOIC	8-bit Digital Potentiometer
AS1502-T	50kΩ	T&R	8-pin SOIC	8-bit Digital Potentiometer
AS1503-T	100kΩ	T&R	8-pin SOIC	8-bit Digital Potentiometer

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