AS3560

Class-G Stereo Headphone Amplifier

1 General Description

The AS3560 is a Class-G stereo headphone amplifier optimized for usage within portable devices. The Class-G supply rail adaptation is implemented by an integrated DCDC buck converter that takes its input directly from the battery. The continuous adaption of supply rails is done according to the input signal swing and load conditions. This architecture implements significant power savings compared to traditional Class-AB amplifiers.

An I2C control interface is implemented for a 32-step volume control.

The integrated charge pump generates a symetric negative supply for true ground output signal levels without the need of output coupling capacitors.

A supervisory circuit is included for overtemperature and short-circuit protection.

Differential inputs together with output ground sensing guarantees very low noise sensitivity.

2 Key Features

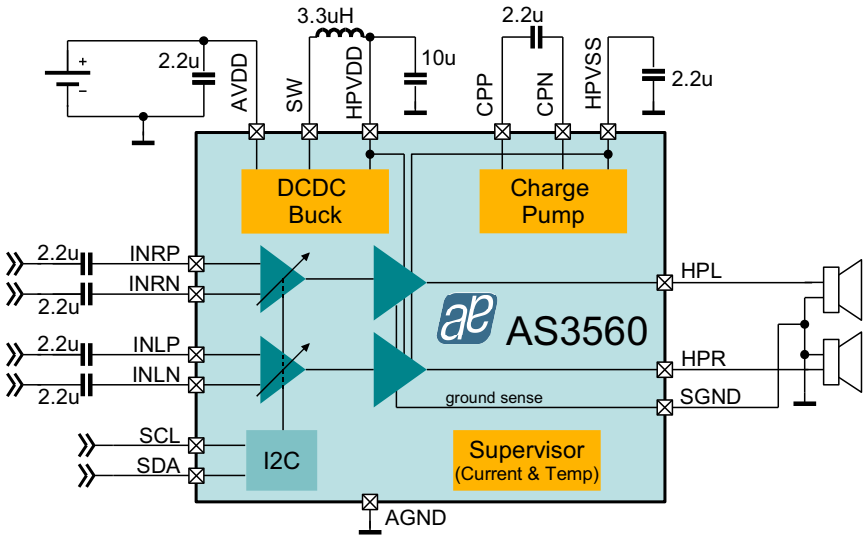
- G-Class amplifier with integrated DCDC buck converter
  - 2x30mW, 0.02% THD @16Ω
  - >100dB SNR @1V_{rms}
- Charge pump for true ground output without coupling capacitors
- Direct battery connection with wide supply range: 2.3V to 5.5V
- Low power consumption optimized for battery operation
  - 1 mA quiescent current with both channels enabled
  - <5 µA shutdown current
- Fully Differential Inputs reduce system noise
  - Also configurable as Single-Ended Inputs
- SGND pin for ground sensing and ground feedback minimizes sensitivity to interference
- I2C control interface
  - volume control with 32 gain steps, -59 to +4dB, <-80dB mute
  - Channel independent enable control

  Current and Temperature Supervisor
- Package: 0.4 mm Pitch WL-CSP (1.615x1.615mm)

3 Applications

- Mobile Phones
- Portable Navigation DevicesMedia Devices
- Media Devices

Figure 1. AS3560 Block Diagram



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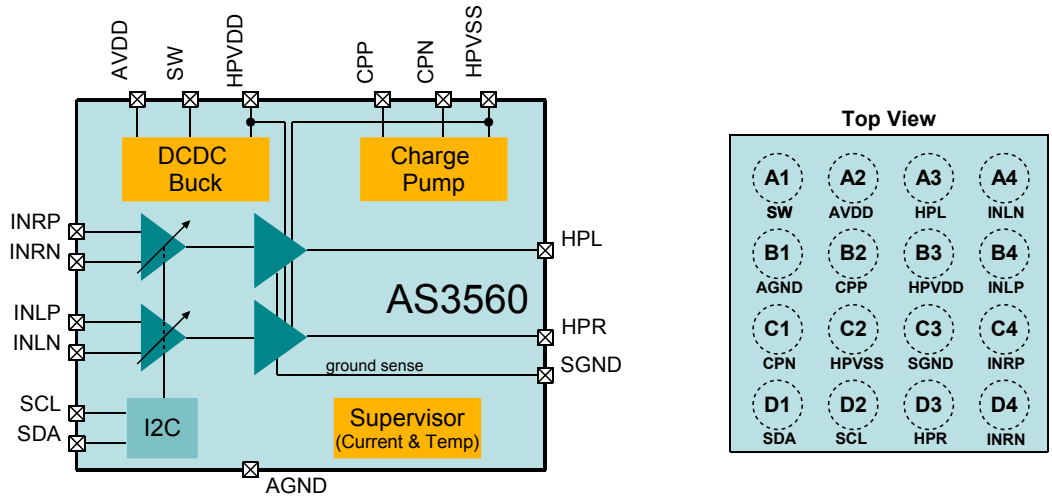
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
SW	A1	Buck converter switching node
AVDD	A2	Primary power supply for device
HPL	A3	Left channel headphone amplifier output
INLN	A4	Inverting left input for differential signals; connect to left input signal through 2.2µF capacitor for single-ended input applications
AGND	B1	Main Ground for headphone amplifiers, DC/DC converter, and charge pump
CPP	B2	Charge pump positive flying cap; connect to 2.2µF flying capacitor
HPVDD	B3	Power supply for headphone amplifier (DC/DC output node)
INLP	B4	Non-inverting left input for differential signals; connect to ground through 2.2µF capacitor for single-ended input applications
CPN	C1	Charge pump negative flying cap; connect to 2.2µF flying capacitor
HPVSS	C2	Charge pump output; connect 2.2µF capacitor to GND
SGND	C3	Ground sense; connect to headphone jack ground
INRP	C4	Non-Inverting right input for differential signals; connect to right input signal through 2.2µF capacitor for single-ended input applications
SDA	D1	I²C Data; 1.8V logic compliant
SCL	D2	I²C Clock; 1.8V logic compliant
HPR	D3	Right channel headphone amplifier output
INRN	D4	Inverting right input for differential signals; connect to ground through 2.2µF capacitor for single-ended input applications

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Operating Conditions on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Supply voltage, AVDD	-0.3	5.5	V	for 1 ms peaks
Amplifier supply voltage, HPVDD	-0.3	2.0	V	
SGND	-0.3	0.3	V	
Differential Input voltage	HPVSS -0.3V	HPVDD +0.3V	V	
Input voltage at SCL, SDA	-0.3	7.0	V	
Breakdown voltage at amplifier outputs	HPVSS -0.5	HPVDD +0.5	V	
Input current (latchup immunity)		±200	mA	
Continuous Power Dissipation				
Continuous power dissipation		TBD	mW	P_T [1]
Continuous power dissipation derating factor		TBD	mW/ºC	P_{DERATE} [2]
Electrostatic Discharge				
ESD HBM		±2	KV	Norm: MIL 883 E Method 3015
ESD MM		±100	V	Norm: JEDEC JESD 22-C101C
ESD CDM	-4	±500	V	Norm: JEDEC JESD 22-A115-A level A
Temperature Range and Storage Conditions				
Junction Temperature		+150	ºC	internally limited (overtemperature protection) auto shutdown at 140 ºC
Storage Temperature Range	-55	+125	ºC	
Body Temperature during Soldering		+260	ºC	according to IPC/JEDEC J-STD-020C

1. Depending on actual PCB layout and PCB used
2. P_{DERATE} derating factor changes the total continuous power dissipation (P_T) if the ambient temperature is not 70°C.
   Therefore for e.g. TAMB=85°C calculate P_T at 85ºC = P_T - P_{DERATE} * (85ºC - 70ºC)

6 Electrical Characteristics

AVDD=3.6V, T_A=25 ºC, Rload = 15 + 32 Ω (headphone + external protection resistor), unless otherwise specified.

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General Operating Conditions						
AVDD	Supply Voltage		2.3		4.8	V
	Rail Voltages HPVDD, HPVSS (Buck and CP output)		0.8	0.9	1.0	V
			1.15	1.25	1.35	V
			1.7	1.8	1.9	V
I_{DD}	Quiescent Current	both channels enabled, no audio signal		1.1	1.5	mA
I_{SD}	Shutdown Current	SW shutdown		1	5	uA
I_S	Supply Current	Output: 2x100µW @ 3dB Crest Factor		2.0	3.5	mA
		Output: 2x500µW @ 3dB Crest Factor		3.1	5.5	mA
		Output: 2x1mW @ 3dB Crest Factor		4.0	7.5	mA
T_A	Operating Temperature Range		-30	25	+85	ºC
t_{WAKEUP}	Wakeup Time			10	15	ms
Input Interfaces						
V_{IL}	Low-level input voltage (SCL, SDA)	AVDD 2.9V to 4.5V			0.6	V
V_{IH}	High-level input voltage (SCL, SDA)	AVDD 2.9V to 4.5V	1.2			V
V_{HYST}	Hysteresis (SCL, SDA)		50	100	200	mV
Z_{IN}	Input Impedance Line Inputs	Differential	20			kΩ
		Single Ended	10			kΩ
HPA Output						
V_{OUT}	Output Voltage	Rload=16Ω, THD+N=1%, L+R in phase	0.7			V_{rms}
		Rload=32Ω, THD+N=1%, L+R in phase	1.0			V_{rms}
	Output DC Offset	Both channels enabled			500	µV
Z_{OUT}	Output Impedance	In HiZ mode	<40 KHz	10		kΩ
			6 MHz	500		Ω
			36 MHz	75		Ω
	Voltage applied to Output; HPR, HPL	when SWS = 0, HiZ_L = HiZ_R = 1, device in HI-Z mode	-1.8		1.8	V
C_{LOAD}	Capacitive Load	ext. cap, 15Ω series resistor	0.8	5	100	nF
		ext cap, directly connected			100	pF
$Z_{OOT,SD}$	Output impedance in shutdown	SWS = 1		8		kΩ
	Voltage applied to Output; HPR, HPL	when SWS = 1, device disabled	-0.3		3.6	V
Audio Parameters						
THD+N	Total Harmonic Distortion + Noise	700mV_{rms}, 1KHz		0.01	0.02	%
PSRR	Power Supply Rejection Ratio	Gain 0dB @217 Hz	90			dB
SNR	Signal-to-Noise Ratio	1V_{rms}, 1KHz	100	105		dB
	Channel Separation	>16Ω (Headset)	60			dB
		>10kΩ (Lineout)	80			dB

Table 3. Operating Conditions (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_N	Output Noise	Gain 0dB, A-weighted		5.3	9	μV_{rms}
Other Parameters						
	Thermal Shutdown	Threshold		140		°C
		Hysteresis		30		

7 Detailed Operating Characteristics

T_A = 25ºC, AVDD (V_{DD}) = 3.6 V, GAIN = 0 dB, C_{HPVDD} = 10 uF, C_{HPVSS} = 2.2 µF, C_{INPUT} = C_{FLYING} = 2.2 µF.

TBD

Figure 3. THD+N versus output power for RL=47Ω

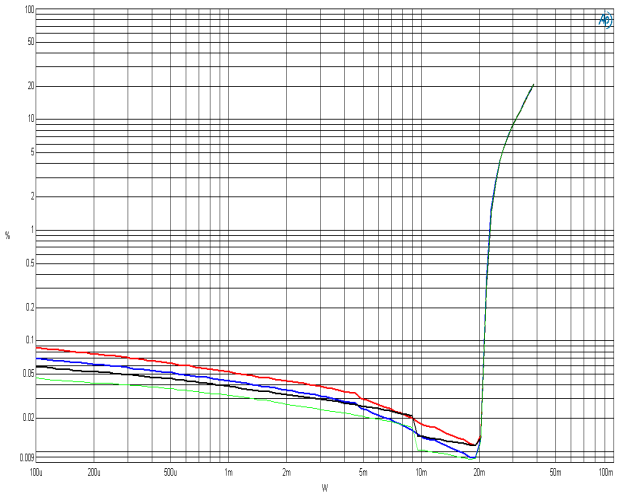


Figure 4. Output Noise Level

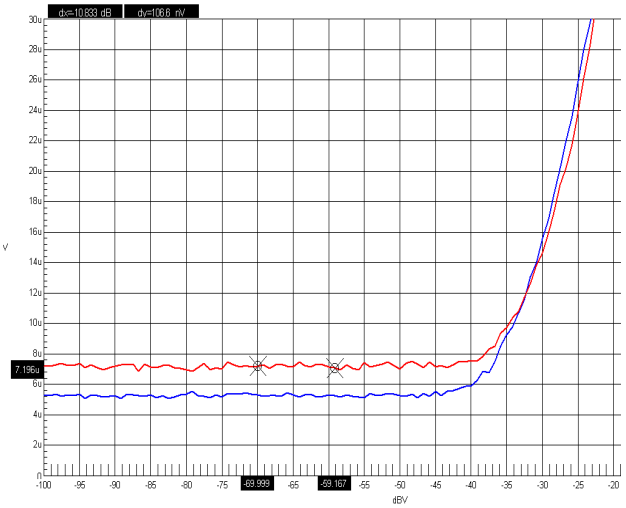


Figure 5. PSRR versus frequency (200mVpkpk supply ripple)

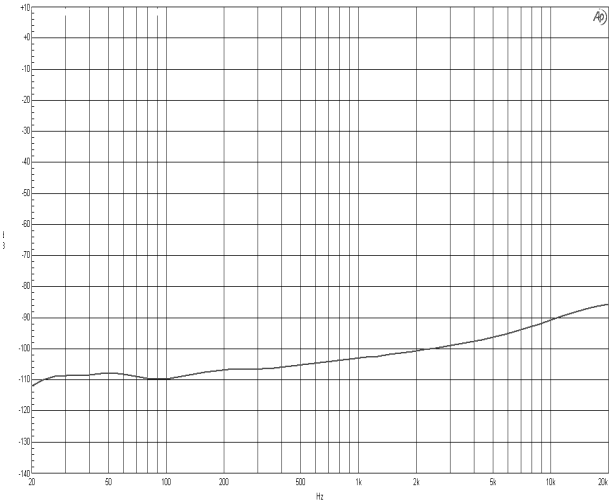


Figure 6. Crosstalk versus frequency (700 mVrms, RL=32Ω

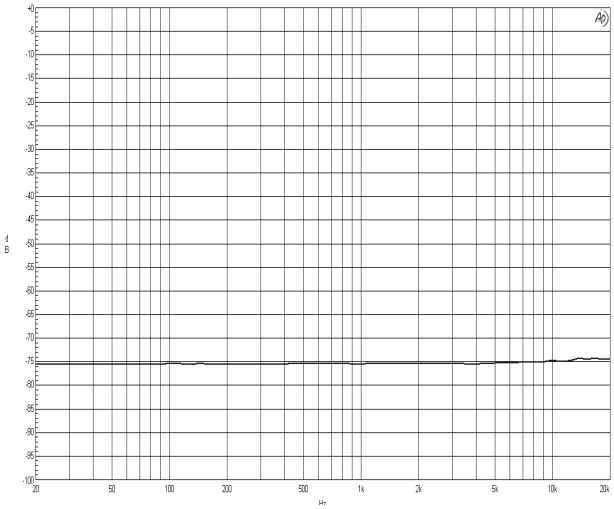


Figure 7. IDD versus output power

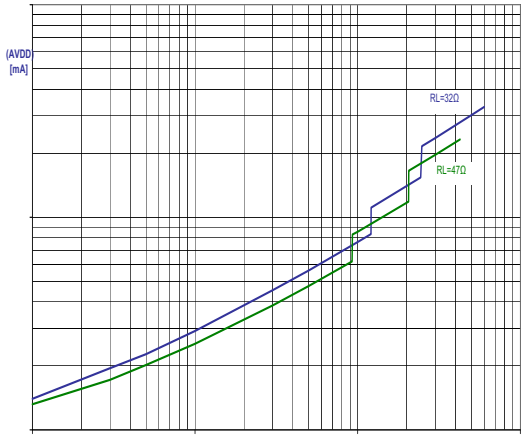


Figure 8. Total power consumption versus output power

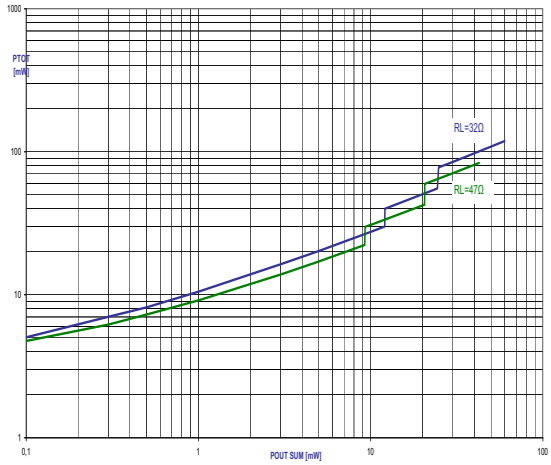


Figure 9. HPVDD/HPVSS attack for neg rise

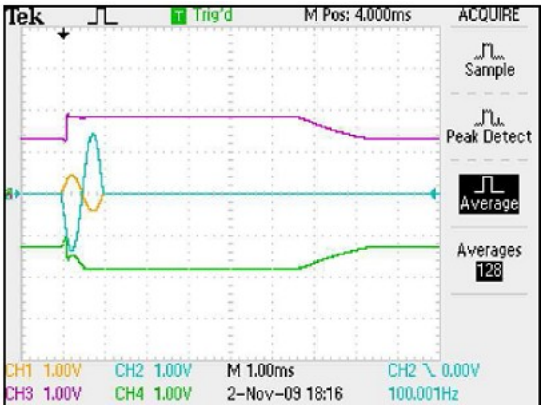
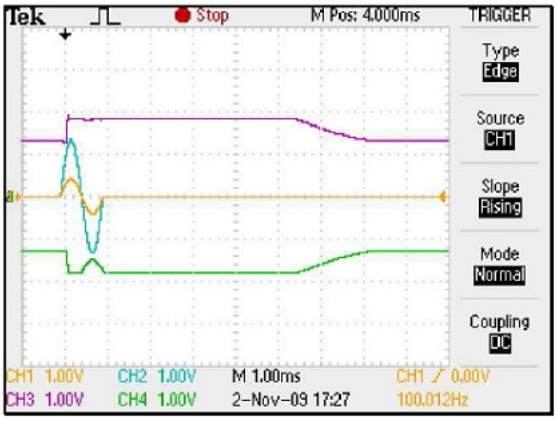


Figure 10. HPVDD/HPVSS attack for pos rise



8 Detailed Description

8.1 I2C Control Interface

An I2C slave interface is implemented for read/write access of the internal registers. SCL is the corresponding clock input pin and SDA the data input pin.

Access is done in 7-bit addressing mode, addresses for read and write are defined by

C0h = 11000000b ... write

C1h = 11000001b ... read

Figure 11. I2C block diagram

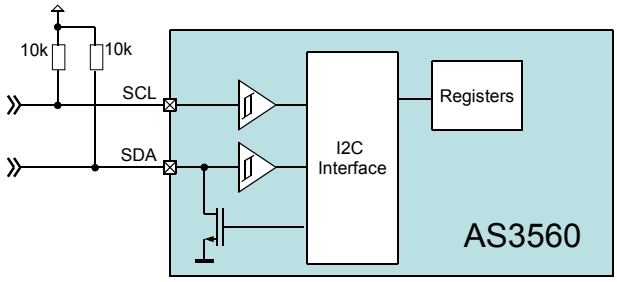


Figure 12. I2C Timing Definition

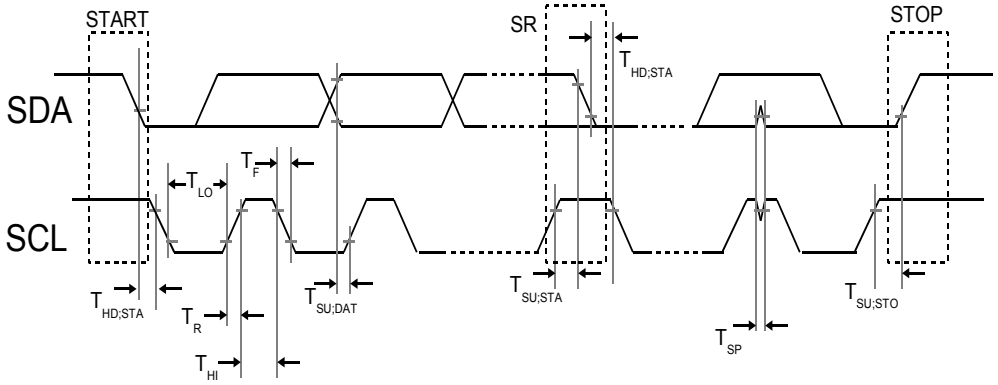


Table 4. I2C Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{SP}	Spike Insensitivity		50	100		ns
T_{HI}	High Clock Time	400 KHz clock speed	330			ns
T_{LO}	Low Clock Time		660			ns
T_{SU}		SDA has to change Tsetup before rising edge of SCLK	30			ns
T_{HD}		no hold time needed for SDA relative to rising edge of CSCL	-40			ns
$T_{HD;STA}$	Within start condition, after low going SDA, SCL has to stay constant for the specified hold time		300			ns
$T_{SU;STO}$	After high going edgle of SCL, SDA has to stay constant for the specified setup time before STOP or repeated start condition is applied		100			ns
$T_{SU;STA}$			100			ns

9 Register Definition

9.1 Register Overview

Register	Description
ENABLE Register (1h)	
Volume Register (2h)	
HiZ Register (3h)	
Info Register (4h)	

9.2 Detailed Register Descriptions

Table 5. ENABLE Register (1h)

Bit	Bit Name	Default	Access	Bit Description
Bit 7	HP_EN_L	0	RW	0 … Disable Headphone Left; 1 … Enable Headphone Left Channel
Bit 6	HP_EN_R	0	RW	0 … Disable Headphone Right;1 … Enable Headphone Right Channel
Bit 5	-	-	-	-
Bit 4	-	-	-	-
Bit 3	-	-	-	-
Bit 2	-	-	-	-
Bit 1	Thermal	0	S_RC	0 … Normal Operation;1 … Thermal Shutown
Bit 0	SWS	1	RW	0 … Normal Operation;1 … Software ShutDown

Table 6. Volume Register (2h)

Bit	Bit Name	Default	Access	Bit Description	
Bit 7	Mute_L	1	RW	0 … Unmuted Left Channel;1 … Mute Left Channel	
Bit 6	Mute_R	1	RW	0 … Unmuted Right Channel;1 … Mute Right Channel	
Bit[5:1]	Vol[4:0]	0	RW	0d … -59 dB; 1d … -55 dB; 2d … -51 dB; 3d … -47 dB; 4d … -43 dB; 5d … -39 dB; 6d … -35 dB; 7d … -31 dB; 8d … -27 dB; 9d … -25 dB; 10d … -23 dB; 11d … -21 dB; 12d … -19 dB; 13d … -17 dB; 14d … -15 dB; 15d … -13 dB;	16d … -11 dB; 17d … -10 dB; 18d … -9 dB; 19d … -8 dB; 20d … -7 dB; 21d … -6 dB; 22d … -5 dB; 23d … -4 dB; 24d … -3 dB; 25d … -2 dB; 26d … -1 dB; 27d … 0 dB; 28d … 1 dB; 29d … 2 dB; 30d … 3 dB; 31d … 4 dB
Bit 0	-	-	-	-	

Table 7. HiZ Register (3h)

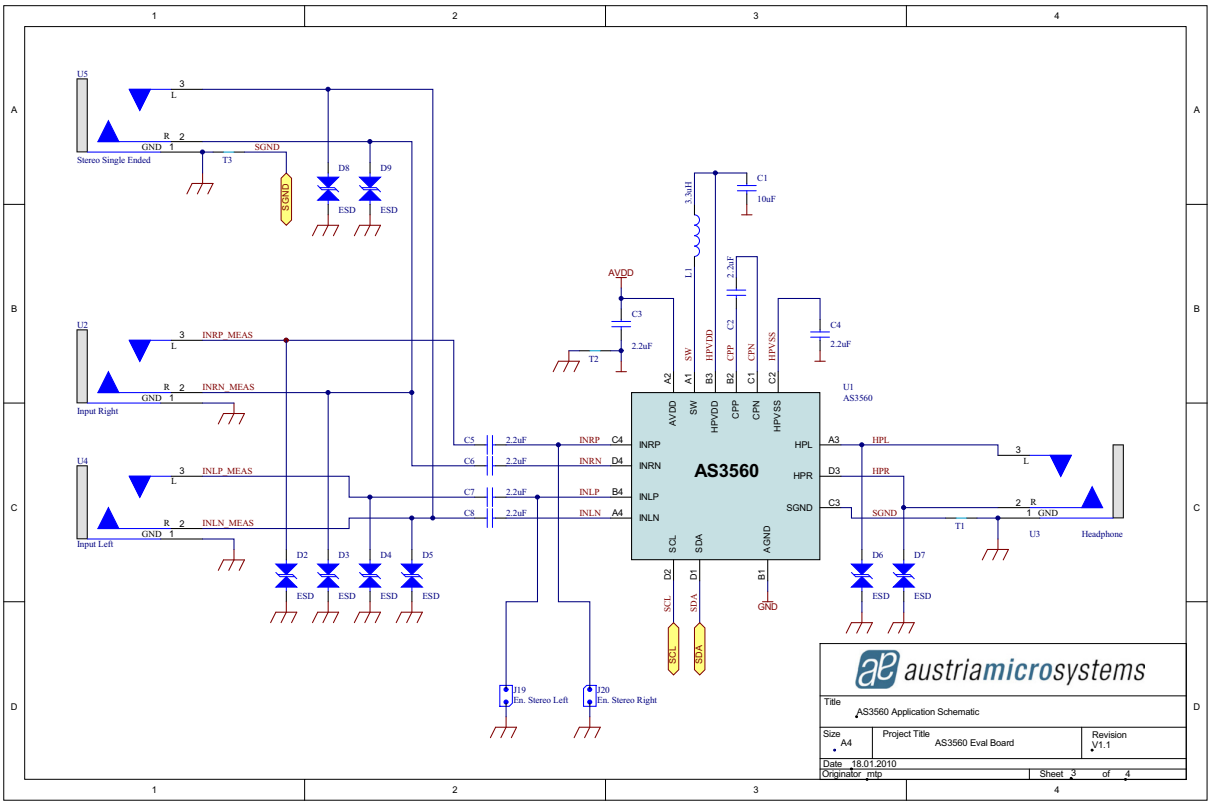
Bit	Bit Name	Default	Access	Bit Description
Bit 7	-	-	-	-
Bit 6	-	-	-	-
Bit 5	-	-	-	-
Bit 4	-	-	-	-
Bit 3	-	-	-	-
Bit 2	-	-	-	-
Bit 1	HiZ_L	0	RW	0 … Normal Operation;1 … High Impedance on HPH_Output Left
Bit 0	HiZ_R	0	RW	0 … Normal Operation;1 … High Impedance on HPH_Output Right

Table 8. Info Register (4h)

Bit	Bit Name	Default	Access	Bit Description
Bit 7	Supplier Bit [1:0]	RO	1	11b … Default Supplier ID; else … unused
Bit 6			1	
Bit 5	-	-	-	-
Bit 4	-	-	-	-
Bit 3	Version Bit [3:0]	RO	0	0 … First Version; else … unused
Bit 2			0	
Bit 1			0	
Bit 0			0	

10 Application Information

Figure 13. AS3560 application board



10.1 GND Connections

The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than ±0.3V to SGND. AGND is a power ground. Connect supply decoupling capacitors for AVDD, HPVDD, and HPVSS to AGND.

10.2 External Elements

1 x 3.3 uH Coil (SW-HPVDD)

7 x 2.2 uH ±10% X5R (AVDD, CPP-CPN, HPVSS, INRP, INRN, INLP, INLN)

1 x 10 uH ±10% X5R (HPVDD)

10.3 Software Shutdown

Set software shutdown by writing a logic 1 in ENABLE Register (1h), bit 0 (SWS bit). Software shutdown places the device in the lowest power state. See Operating Conditions for values. Engaging software shutdown turns off the buck regulator and charge pump and disables the amplifier outputs. Write a logic 0 to the SWS bit to reactivate the device.

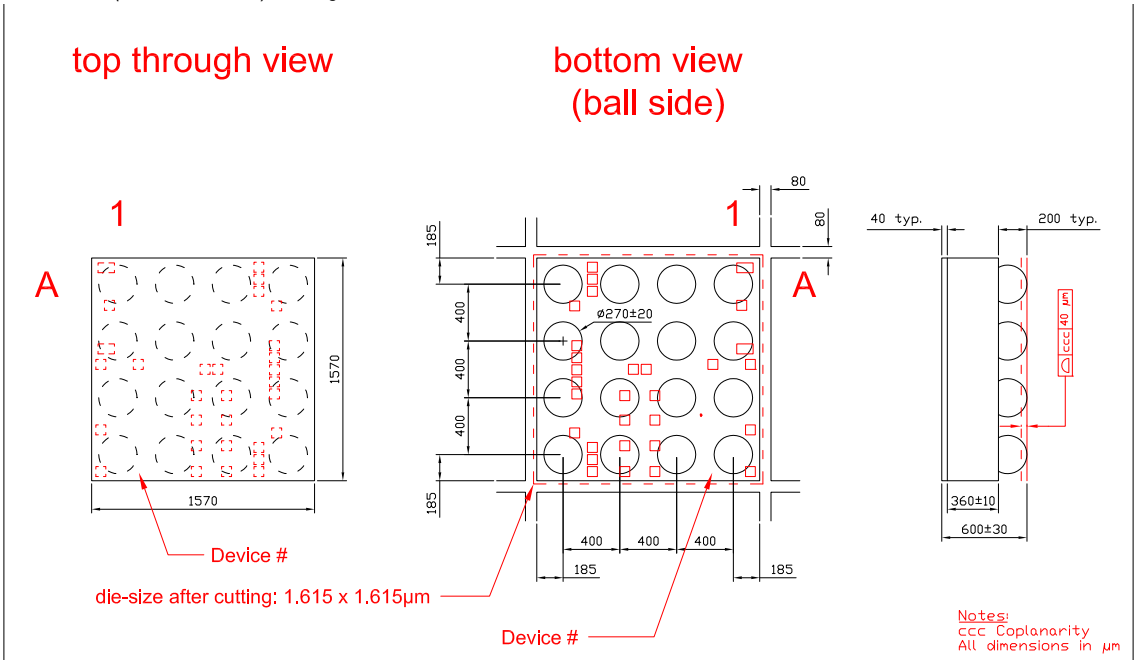
Note: When the device is in SWS mode all registers will maintain their values. The HP_EN_L and HP_EN_R bits can be reset because a full word must be used when writing just one bit to the register.

Note that I2C read and write access is still possible in shutdown mode.

11 Package Drawings and Markings

The devices are available in a WL-CSP (1.615x1.615mm) package.

Figure 14. WL-CSP (1.615x1.615mm) Package



Notes:

1. All dimensions are in micrometers, angle is in degrees.

Revision History

Revision	Date	Owner	Description
0.01	Sep 10th, 2009	pkm	Initial draft template
0.02	Sep 23rd, 2009	wsg	revised draft
0.04	Sep 29th, 2009	wsg	after first review
0.06	Feb 9th, 2010	wsg	update on detailed operating characteristics

Note: Typos may not be explicitly mentioned under revision history.

12 Ordering Information

The devices are available as the standard products shown in Table 9.

Table 9. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS3560BWLT		Tape&Reel	WL-CSP

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
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