AS3691

4 Precision 400mA Current Sources for RGB and Single Color LEDs

General Description

The AS3691 (AS3691A and AS3691B) features four high precision current sinks to drive up to four LED strings. Each of the current sinks can sustain up to 15V and drive up to 400mA. Every channel can be controlled independently by PWM inputs.

To ensure best efficiency AS3691 is able to regulate any external LED power supply (DC-DC converter) to its perfect needs (patented feedback function).

The full scale current is set by external resistor.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of the AS3691 4 Precision 400mA Current Sources for RGB and Single Color LEDs, are listed below:

Figure 1:
Added Value of Using AS3691

Benefits	Features
• Fully flexible current outputs / no SW effort	• 4 × up to 0.4A constant current outputs • Programmable with external resistors • 4 independent PWM inputs
• Perfect color uniformity	• Absolute current accuracy ±0.5%
• Unique DC-DC feedback function	• 'Automatic Supply Regulation' (1) to reduce power dissipation

• Maximum number of LEDs per channel	• Very wide output voltage current source voltage compliance
	  • Down to 0.41V
	  • Up to 15V (2)

• On-chip safety features	• Integrated overtemperature protection

• Easy integration due to several package types including thermal enhanced eP-TSSOP	• Package options:
	  • QFN24 (4 × 4mm)
	  • eP-TSSOP

Note(s):

1. **ams** system patent
2. 15V is sufficient for most applications as the AS3691 does not switch off the LED current completely

Applications

- General Lighting
- Backlighting
- RGB Backlighting for LCD TV/Monitors with White Color Balancing

Application Diagrams

Figure 2:
Application Diagram of AS3691 for Single Color Lighting

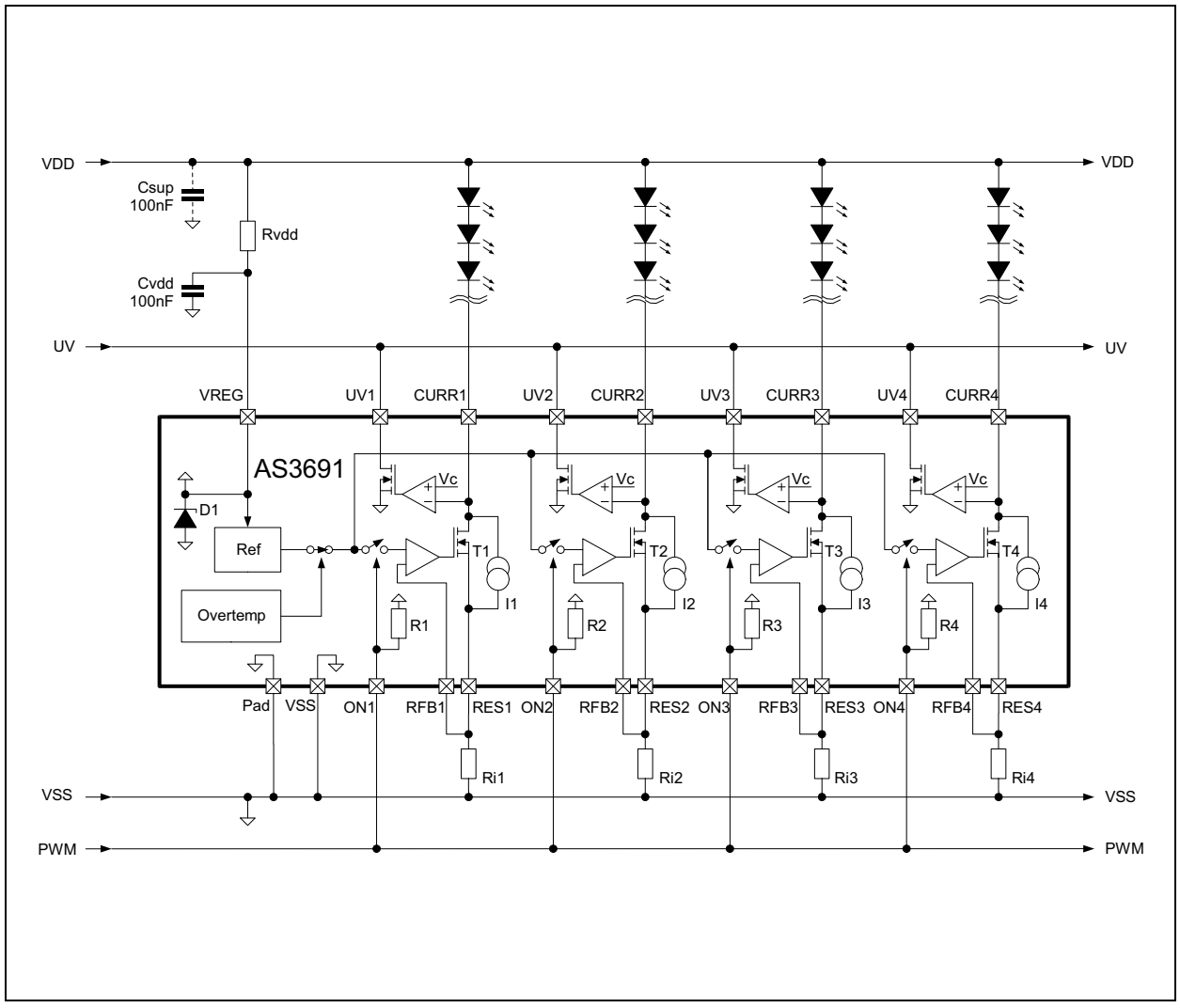
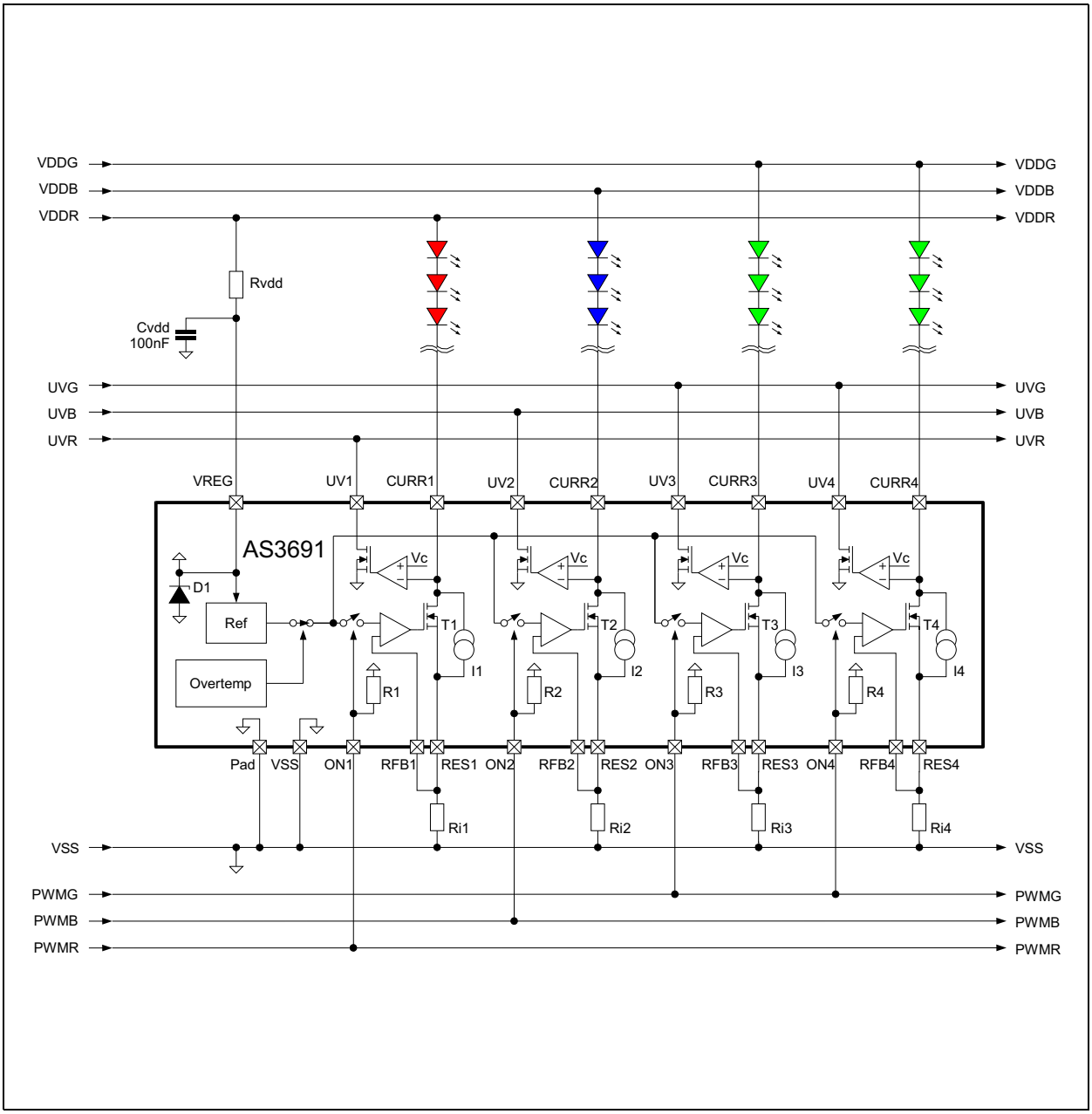
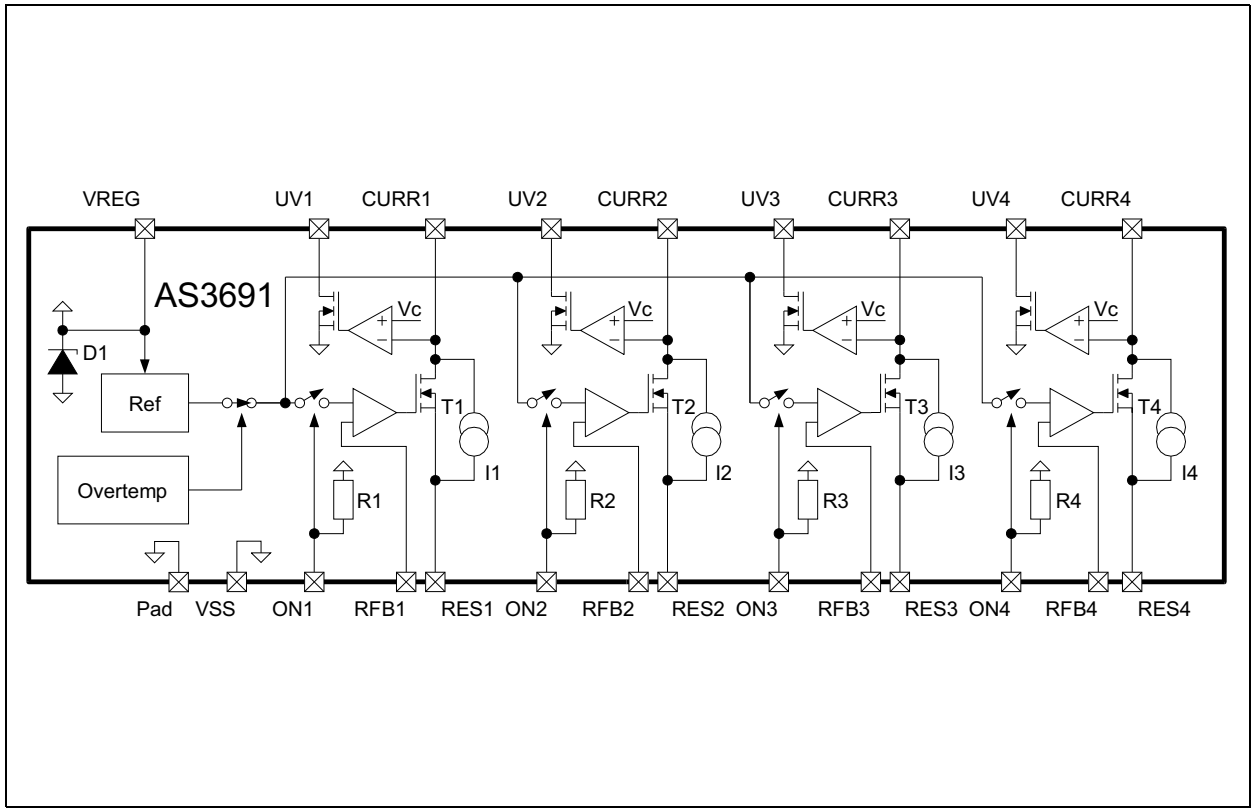


Figure 3:
Application Diagram of AS3691 for RGB Lighting



Pin Assignments

Figure 4:
Pin Usage



Pin Descriptions

Figure 5:
Pin Descriptions

Pin Number QFN Package	Pin Number eP-TSSOP Package	Pin Name	Type	Description
1	10	CURR1	AI/O	Current source 1 output
2	11	RFB1	AI	Connect to current set resistor R1 directly at resistor itself
3	12	nc	nc	Leave open
4	13	RFB4	AI	Connect to current set resistor R4 directly at resistor itself
5	14	CURR4	AI/O	Current source 4 output
6	15	RES4	AI/O	Connect to current set resistor R4

Pin Number QFN Package	Pin Number eP-TSSOP Package	Pin Name	Type	Description
7	16	ON4	DI	Current source CURR4 control; internal pullup resistor to VREG (can be left open, if CURR4 is always switched ON) High … 100% current Low … 5% current
8	17	UV4	AO	Automatic supply regulation for CURR4; if not used, leave open
9	18	TEST	AI	Digital test input; Leave open or connect to VSS; internal pulldown to VSS
10	19	UV3	AO	Automatic supply regulation for CURR3; if not used, leave open
11	20	ON3	DI	Current source CURR3 control; internal pullup resistor to VREG (can be left open, if CURR3 is always switched ON) High … 100% current Low … 5% current
12	21	RES3	AI/O	Connect to current set resistor R3
13	22	CURR3	AI/O	Current source 3 output
14	23	RFB3	AI	Connect to current set resistor R3 directly at resistor itself
15	24	VREG	S	Shunt regulator supply; connect to Rvdd and Cvdd
16	1	RFB2	AI	Connect to current set resistor R2 directly at resistor itself
17	2	CURR2	AI/O	Current source 2 output
18	3	RES2	AI/O	Connect to current set resistor R2
19	4	ON2	DI	Current source CURR2 control; internal pullup resistor to VREG (can be left open, if CURR2 is always switched ON) High … 100% current Low … 5% current
20	5	UV2	AO	Automatic supply regulation for CURR2; if not used, leave open
21	6	VSS	S	VSS supply connection
22	7	UV1	AO	Automatic supply regulation for CURR1; if not used, leave open

Pin Number QFN Package	Pin Number eP-TSSOP Package	Pin Name	Type	Description
23	8	ON1	DI	Current source CURR1 control; internal pullup resistor to VREG (can be left open, if CURR1 is always switched ON) High … 100% current Low … 5% current
24	9	RES1	AI/O	Connect to current set resistor R1
Pad	Pad	VSS	S	VSS supply connection; add as many vias to ground plane as possible

The abbreviations used in Figure 5 are explained below:

AI/O: Analog Input/Output

AI: Analog Input

AO: Analog Output

DI: Digital Input

S: Supply

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{DDMAX}	Supply for LEDs	-0.3	> 17	V	See notes (1)
V_{INVREG}	VREG Supply Voltage	-0.3	7.0	V	Applicable for pin VREG
V_{IN5V}	5V Pins	-0.3	V_{REG} + 0.3V	V	Applicable for 5V pins (2)
V_{IN15V}	15V Pins	-0.3	17	V	Applicable for CURR1, CURR2, CURR3 and CURR4
I_{IN}	Input Pin Current	-25	+25	mA	At 25°C, Norm: JEDEC 17
T_{STRG}	Storage Temperature Range	-55	125	°C	
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor lifetime of 168h
ESD_{HBM}	Electrostatic Discharge	±2000		V	Norm: MIL 883 E Method 3015
PT	Total Power Dissipation		2.0	W	At 50°C, no airflow for QFN24 on two layer FR4-Cu PCB (3)
P_{DERATE}	PT Derating Factor		23	mW/°C	See notes (3)
T_{BODY}	Body Temperature during Soldering		260	°C	According to IPC/JEDEC J-STD- 020C

Note(s):

1. As the AS3691 is not directly connected to this supply. Only the parameters V_{INVREG}, V_{IN5V} and V_{IN15V} have to be guaranteed by the application.
2. All pins except CURR1, CURR2, CURR3 and CURR4.
3. Depending on actual PCB layout and especially number of vias below the exposed pad – see Layout Recommendations; can be improved e.g. with Al-PCB or airflow.

Electrical Characteristics

Figure 7:
Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDD	Main Supply			Not Limited	V	Supply is not directly connected to the AS3691 – see Shunt Regulator
VDD_{TOL}	Main Supply Voltage Tolerance	-20		+20	%	Applies only for supply VREG is connected via Rvdd
$VREG_{INT}$	Supply (shunt regulated by AS3691)	5.0	5.2	5.4	V	If internally (shunt-)regulated by D1
$VREG_{EXT}$		4.5	4.75	5.0	V	If externally supplied
IVREG	Supply Current			2.5	mA	Excluding current through shunt regulator (D1) – see Shunt Regulator
T_{AMB}	Ambient Temperature	-20	25	85	°C	

Figure 8:
Analog Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CURR}	Current Source CURR1 to CURR4 Voltage Compliance	0.9		15.0	V	at 400mA; total power dissipation limit PT must not be exceeded
		0.41		15.0	V	at 100 mA
I_{CURR}	Current Source Range	10		400 (1)	mA	ONx = high ICURRx = 250mV / Rix (x = 1 to 4)
$I_{CURR, TOL}$	Current Source Tolerance	-0.5		+0.5	%	@25°C $T_{JUNCTION}$, excluding variation of external resistors; V(CURRx) ≤ 4.0V
		-1.5		+1.5	%	-20°C to 100°C (2) $T_{JUNCTION}$, -20°C to 85°C T_{AMB}, excluding variation of external resistors; V(CURRx) ≤ 4.0V
V_C	Automatic Supply Regulation Compare Voltage		1.0		V	See Automatic Supply Regulation
$V_{C,GAIN}$	Automatic Supply Regulation Gain		2.0		mA/V	Voltage to current ratio; output current range typ 0 to 200µA

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{1-4}	Parallel Current			1.0	mA	V(CURRx) ≤ 15V
				0.1	mA	V(CURRx) ≤ 5.0V
T_{OVTEMP}	Overtemperature Limit		140		°C	Maximum junction temperature

Note(s):

1. To obtain higher currents connect more than one current source in parallel.
2. Accuracy at 100°C guaranteed by design and verified by laboratory characterization.

Figure 9:
Digital Input Pin Characteristics for Pins ON1, ON2, ON3 and ON4

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{IH}	High Level Input Voltage	2.3		VREG	V	
V_{IL}	Low Level Input Voltage	0.0		0.9	V	
R_{PU}	Pullup Resistor		70		kΩ	Internal pullup resistor R1 to R4 to VREG
f_{ON}	Input Frequency Range	0		20	kHz	This defines the actual input frequency seen on the input ON1 to ON4; the basic frequency to generate the PWM signal is not limited by this parameter

Typical Operating Characteristics

Figure 10:
Output Current vs. Voltage on Current Source – High Current Range

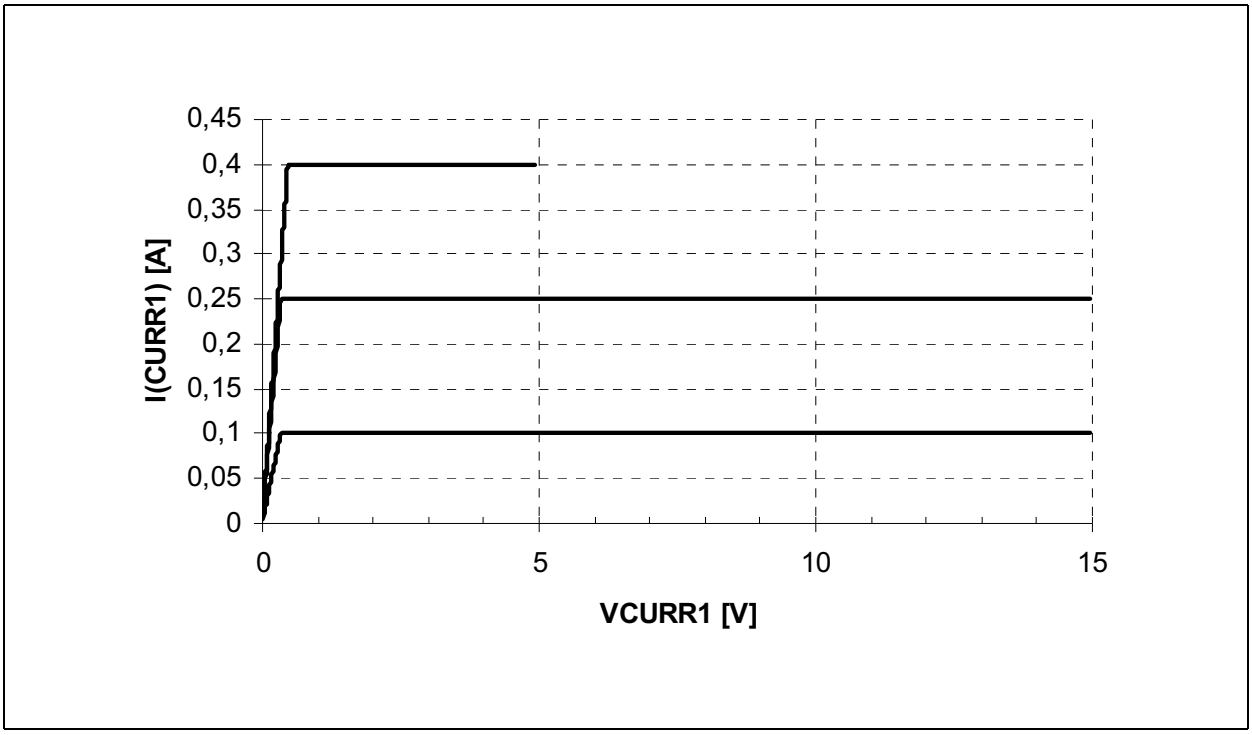


Figure 11:
Output Current vs. Voltage on Current Source – Low Current Range

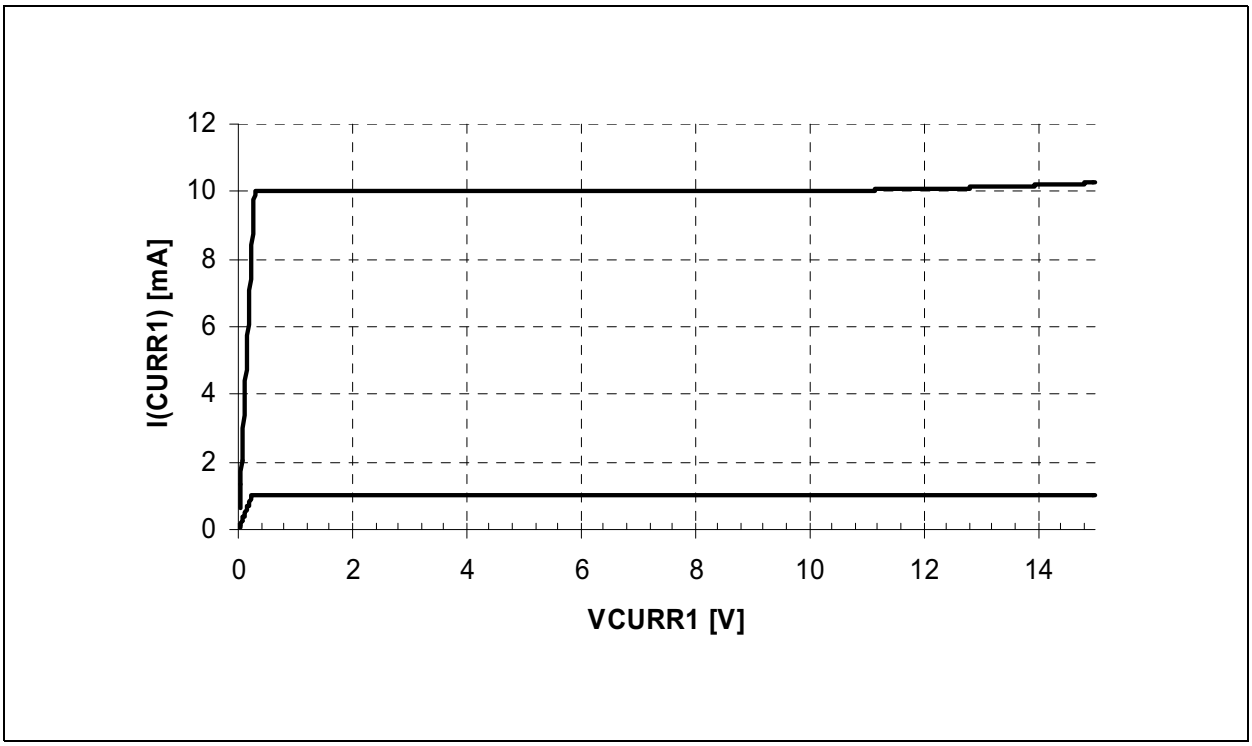
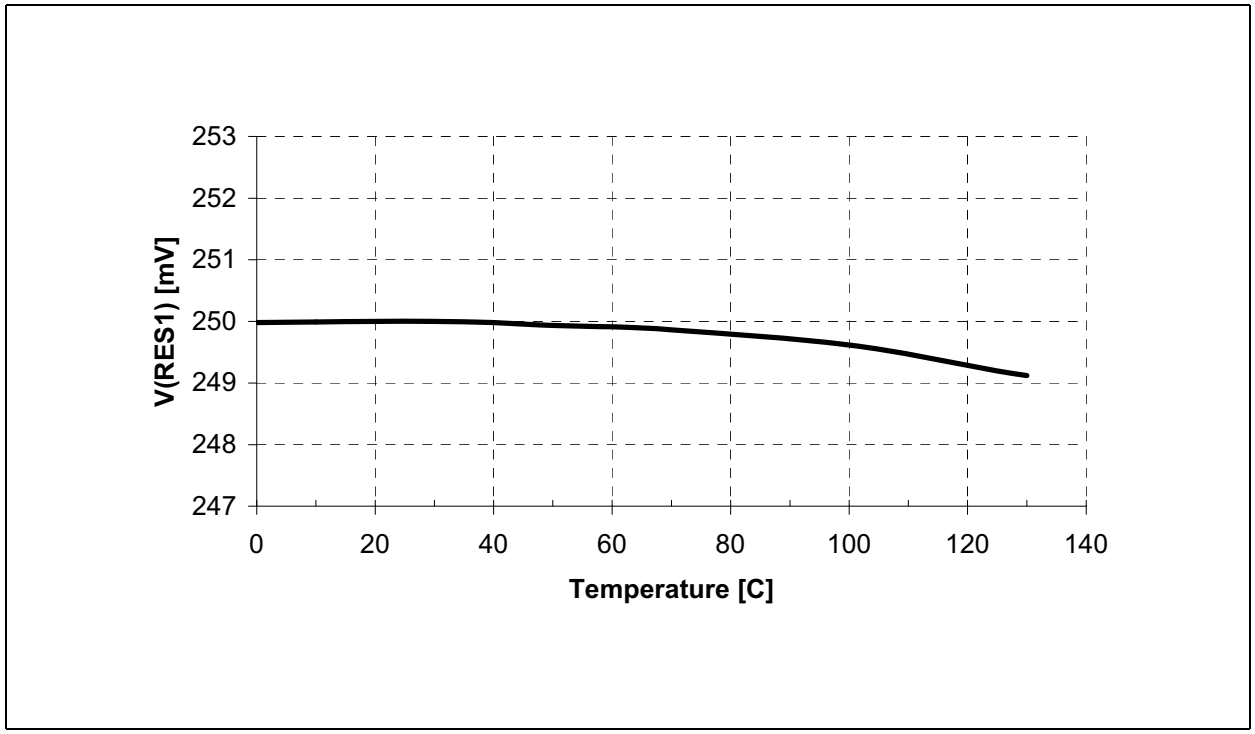


Figure 12:
Internal Voltage Reference vs. Temperature, V(CURR1) = 2.0V, Ri1 = 250Ω



$$ICURR_1 = \frac{V(RES1)}{Ri_1} \quad \text{(EQ1)}$$

Figure 13:
Output Current vs. Temperature, V(CURR1) = 2.0V, Ri1 = 2.5Ω (temperature coefficient of Ri1 = -200ppm/°C)

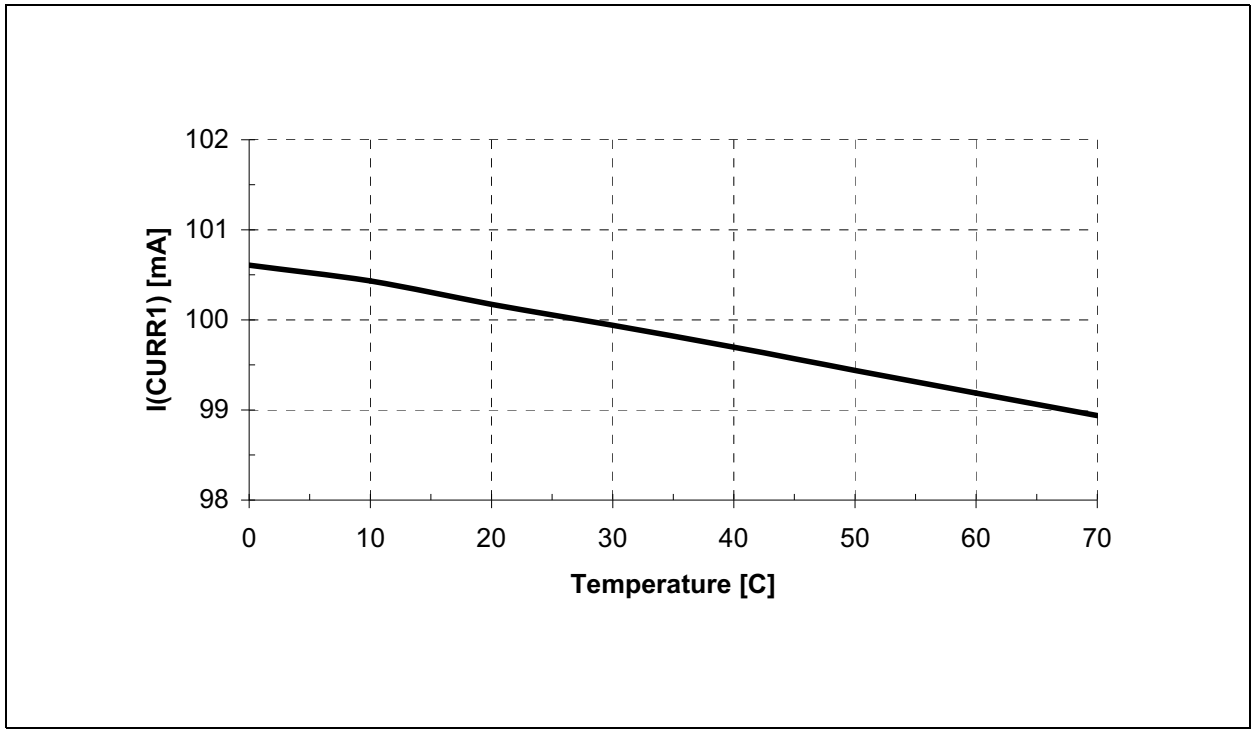


Figure 14:
Cross Coupling of PWM on CURR1 to CURR2; I(CURR1) = 100mA to 4mA, I(CURR2) = 100mA; AS3691A

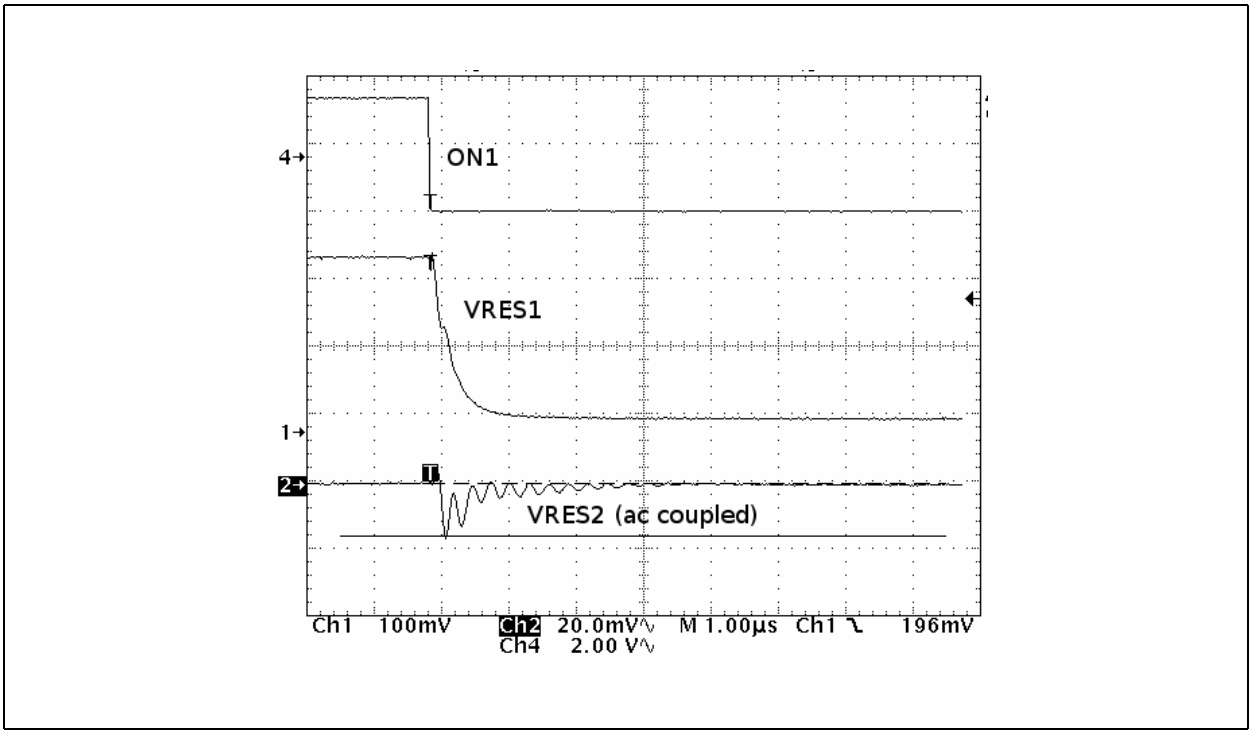


Figure 15:
PWM Performance of Current Source CURR1, I(CURR1) Changed Between 400mA (ON1=1) and 20mA (ON1=0); AS3691A

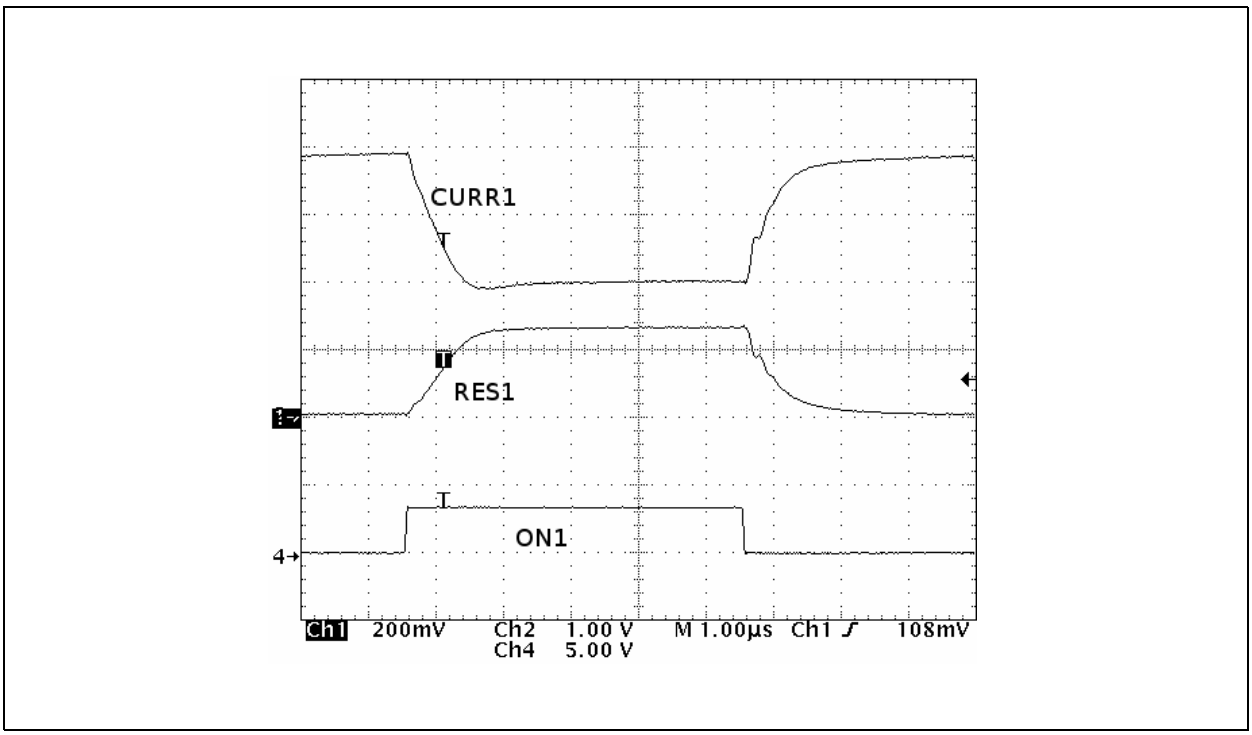


Figure 16:
Shunt Regulator Voltage VREG vs. Supply VDD with Rfb=1kΩ

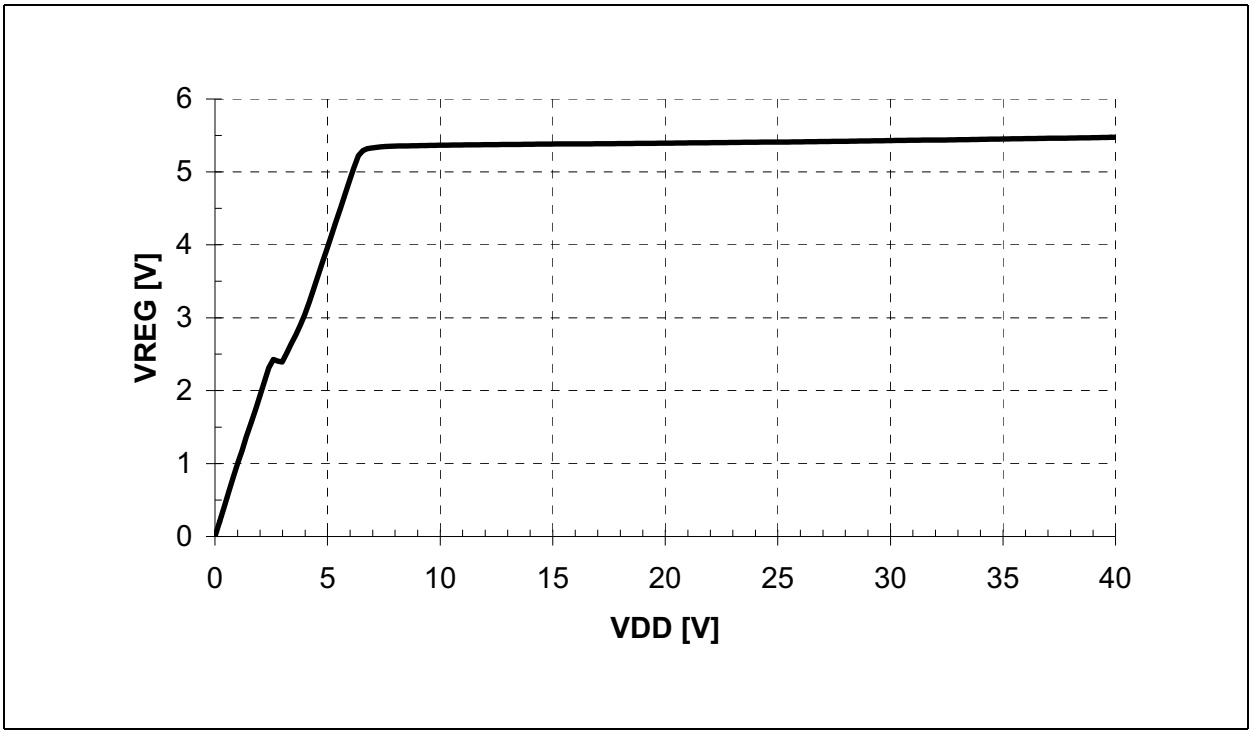
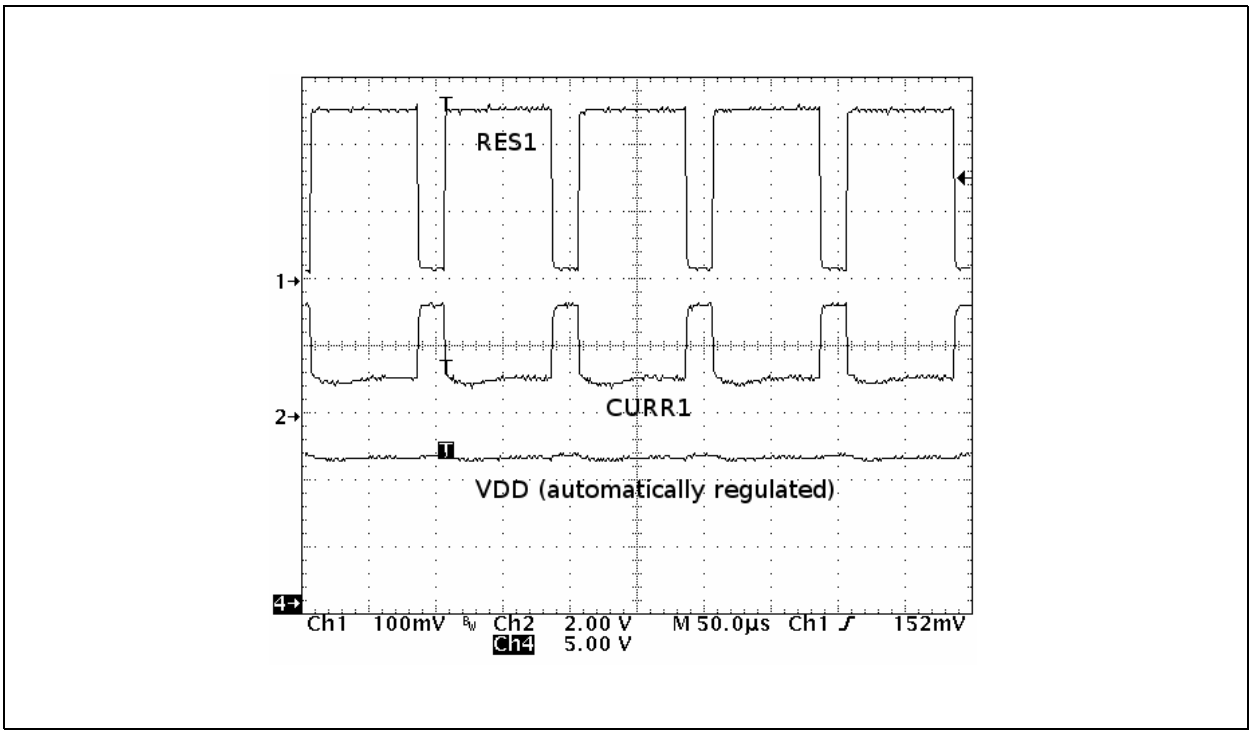
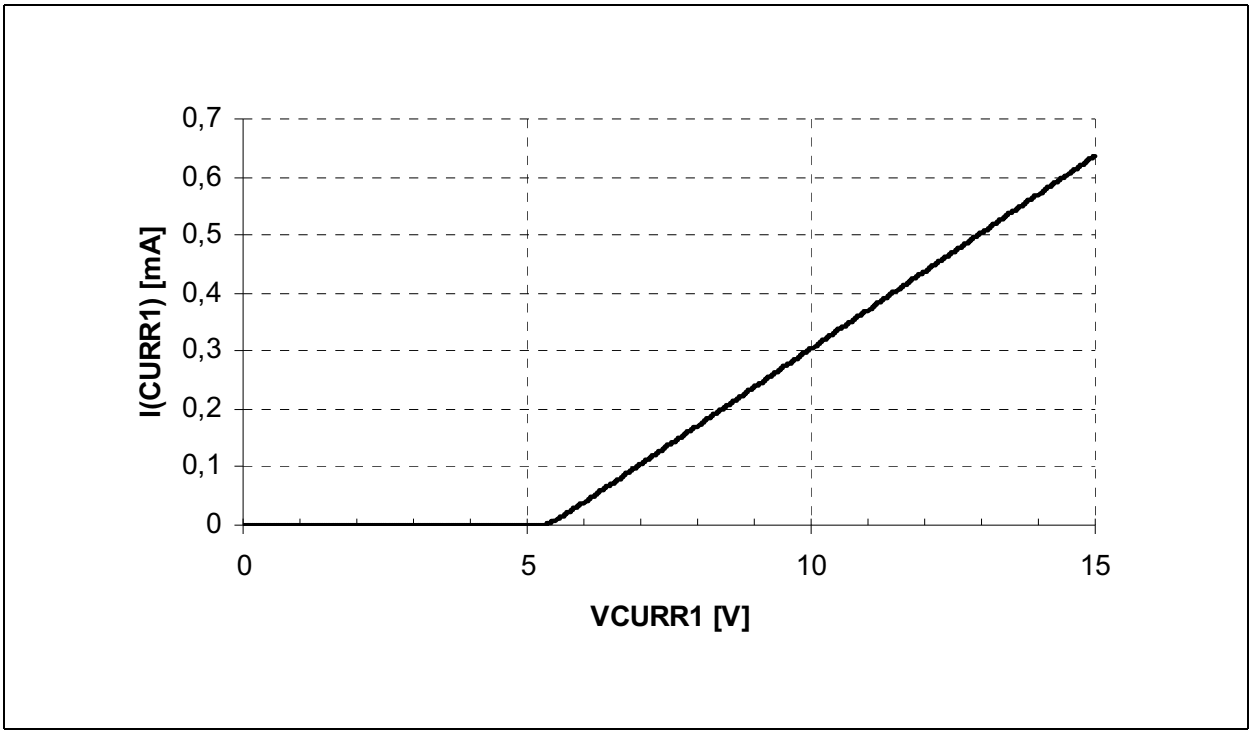


Figure 17:
Automatic Supply Regulation Dynamic Performance Using DC-DC Converter in Regulation Loop



Automatic Supply Regulation Dynamic Performance Using DC-DC Converter in Regulation Loop:
R1 = 47kΩ, R2 = 10kΩ, R3 = 5kΩ, R4 = 500Ω, C1 = 1uF, I(CURR1) = 400mA/20mA (Ri1=0.625Ω)
3 OSRAM Golden Dragon in series as load between CURR1 and VDD
Input signal on pin ON1: PWM signal with f=10kHz, 80% duty cycle

Figure 18:
Parallel Current I1 to I4 (for measurement of I1 remove current set resistor R1)



Detailed Description

The AS3691 includes four high precision current sources (sinks). Each current source is set by an external resistor. For internal power supply an internal shunt regulator is used. Optionally an additional 5V device can be supplied as well with this shunt regulator.

The current sources are individually controlled by four ON inputs. If the inputs ON are high or left open, then the current is set as follows:

(EQ2) $$ICURR_{1-4} = \frac{250mV}{Ri_{1-4}}$$

Setting the input ON to low the current is

(EQ3) $$ICURR_{1-4} = \frac{10.0mV}{Ri_{1-4}}$$ for part numbers starting with AS3691A

The current is not zero to avoid high voltage jumps on the LEDs and supplies and therefore reduce EMI.

(EQ4) $$ICURR_{1-4} = \frac{0.0mV}{Ri_{1-4}} + I_{1-4} = I_{1-4}$$ for part numbers starting with AS3691B; I1-4 is the parallel current (see Figure 17).

Shunt Regulator

The supply of the AS3691 is generated from the high voltage supply. To obtain a 5V regulated supply, a series resistor Rvdd is used together with an internal zener diode (shunt regulator principle). An external capacitor Cvdd is used to filter the supply on the pin VREG.

The external resistor Rvdd has to be chosen according to the following formula:

(EQ5) $$Rvdd = \frac{VDD_{MIN} - \mathrm{VVREGINT_{MAX}}}{IVREG_{MAX}}$$

VDD_{MIN} is the minimum voltage of the supply, where Rvdd is connected.

This ensures enough supply current ($IVREG_{MAX}$) for the AS3691 under minimum supply voltage VDD_{MIN}.

If a stable 5V supply within the operating conditions limits of $VREG_{EXT}$ is already existing in the system it is possible to supply the AS3691 directly. In this case remove the resistor Rvdd and connected this supply directly to VREG.

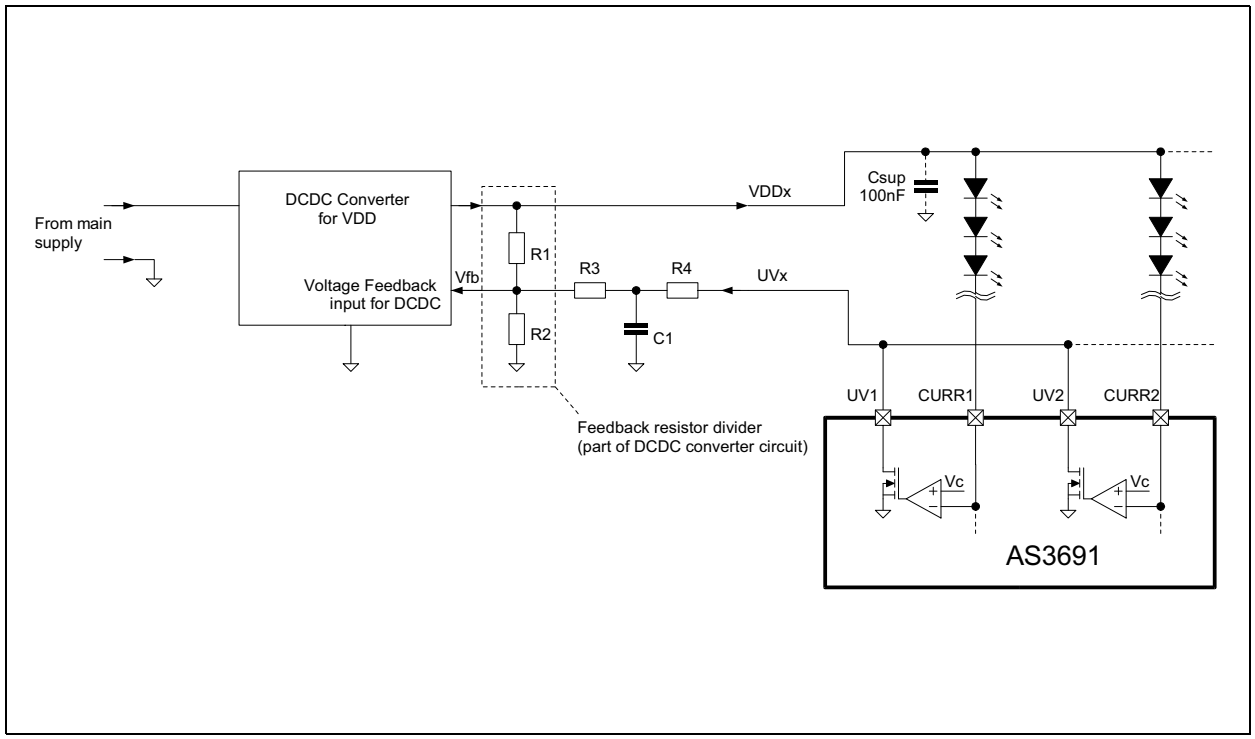
Overtemperature Protection

If the junction temperature inside the AS3691 rises above T_{OVTEMP}, the current sources are switched OFF.

Automatic Supply Regulation

The purpose of the automatic supply regulation is to minimize the voltage supply to reduce the voltage across the current sources of the AS3691 (CURR1-CURR4 to VSS) and therefore reduce the power dissipation of the AS3691 and the complete system. The AS3691 automatically controls the minimum required supply voltage for the different led strings to support very power efficient systems for lighting using the following circuit (any off-the-shelf DC-DC converter or ldo with adjustable output voltage can be used):

Figure 19:
Automatic Supply Regulation Circuit



The function of this circuit is as follows:

All channels, which are connected to the supply VDDx should have their respective UV pin connected together to UVx (see Figure 19 and Typical Application Schematic). If any of these current sources has a too low voltage, it gradually pulls the wire UVx low. (The analog gain between the current source CURRx and output UVx is defined by the parameter $V_{C,GAIN}$.)

Therefore the feedback pin Vfb of the DC-DC converter is pulled low and the DC-DC converter compensates this by increasing the voltage on VDDx to obtain the same feedback voltage as before.

To stabilize this regulation loop, the low pass filter build by C1 and R4 is used (this should be the dominant pole for the regulation loop).

The minimum output voltage $VDDx_{min}$ can be set accurately by the resistors R1 and R2. The maximum output voltage $VDDx_{max}$ is set by R1, R2, R3 and R4 (Vref is the internal voltage reference of the DC-DC converter; usually Vref = Vfb):

(EQ6) $$VDDx_{MIN} = Vref \cdot \frac{R_1 + R_2}{R_2}$$

(EQ7) $$VDDx_{MAX} = Vref \cdot \frac{R_1 + R_2 \parallel (R_3 + R_4)}{R_2 \parallel (R_3 + R_4)}$$

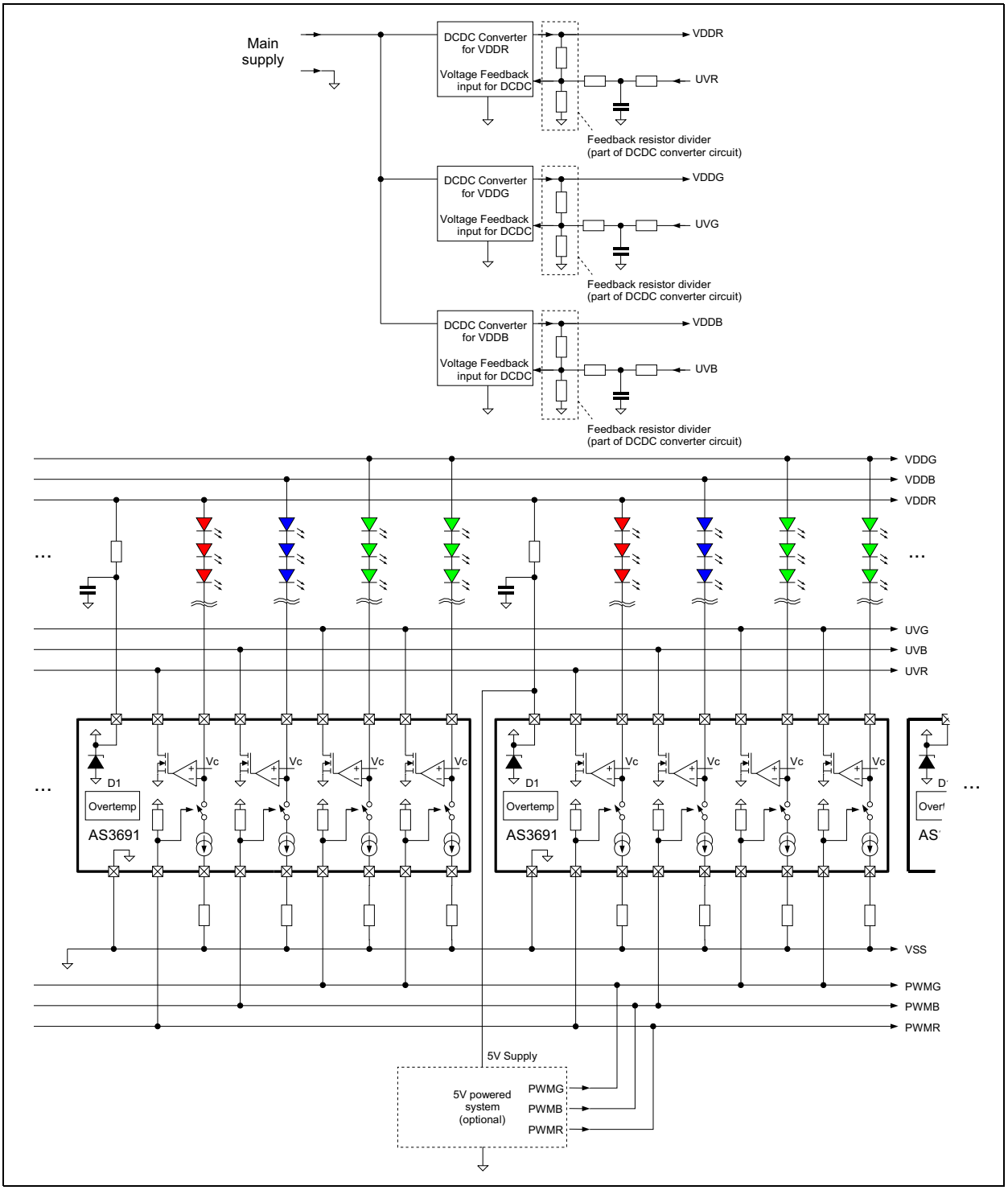
Therefore even if a led string is broken (then UVx is forced to 0V) or some LEDs are shorted, the supply always stays within the limits $VDDx_{MIN}$ and $VDDx_{MAX}$.

Application Information

Typical Application Schematic

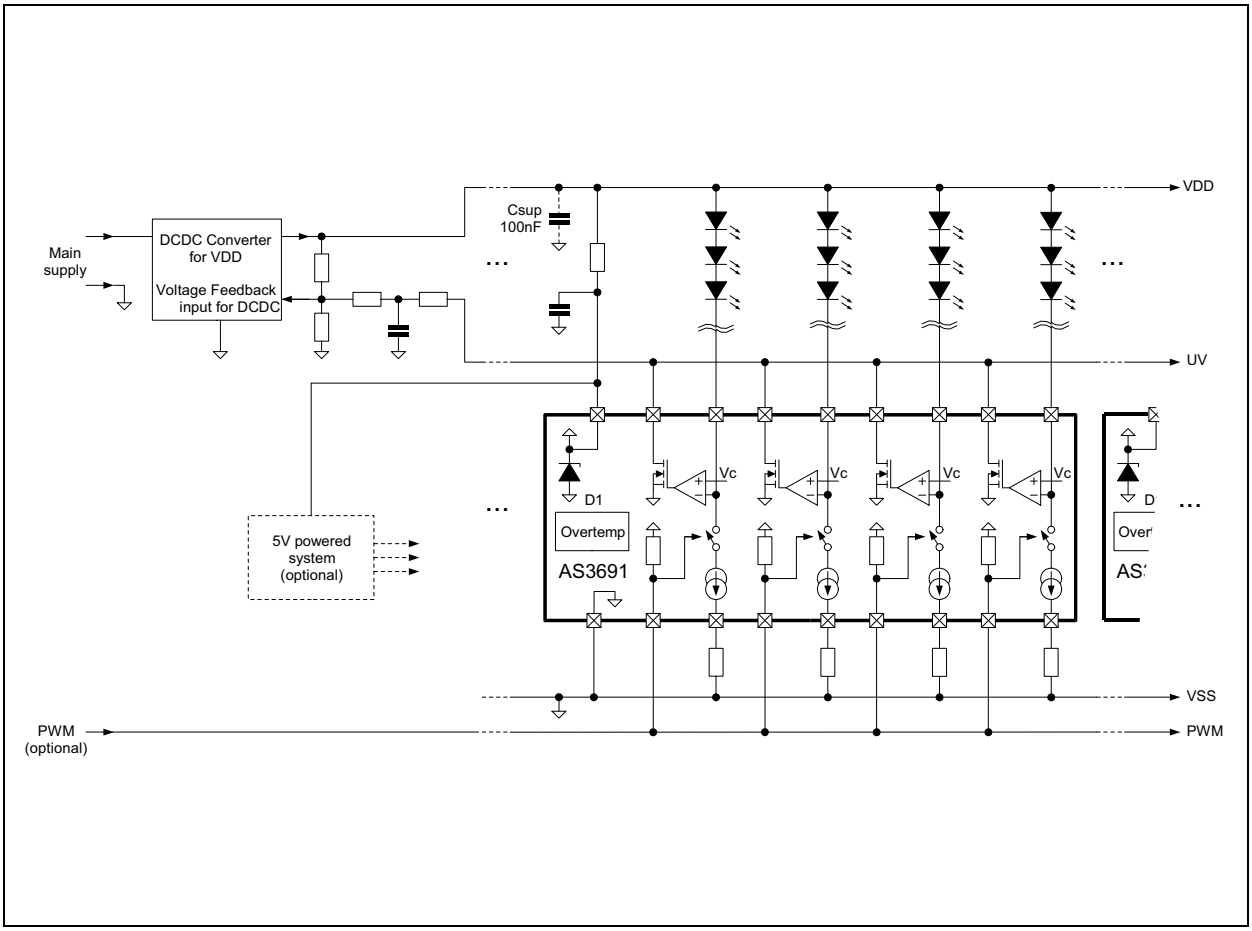
For RGB LEDs (and a white color balancing circuit) use the following application schematic including automatic supply regulation (feedback paths UVR, UVG, UVB):

Figure 20:
Typical AS3691 System for RGB (Back-Lighting); Several AS3691 Can Be Cascaded



A typical AS3691 for single color LEDs can be done as follows using automatic supply regulation (feedback path UV):

Figure 21:
Typical AS3691 System for Single Color LEDs and Supply Regulation Loop; Several AS3691 Can Be Cascaded



Note(s): Csup (100nF) is only required, if there are long wires (>0.3m) between the DC-DC converter and the AS3691. The wire length between the Csup capacitor and the CURRx pin on AS3691 should not exceed 0.3m. If this cannot be guaranteed, add additional capacitors of 100nF to the pins CURRx.

Design Example

Assume a single color LEDs application (4 times 3 LEDs in series, each 100mA with Uf ranging from Uf_{min} = 3.2V to Uf_{max} = 3.8V) with a fixed supply. First choose the external current set resistor with the following formula:

(EQ8) $$Ri_{1-4} = \frac{250mV}{ICURR_{1-4}}$$

So for a current of 100mA, use a resistor of 2.5Ω; 1/8W rated resistors are suitable (even up to 400mA).

Then calculate the required voltage of the power supply. The minimum voltage on the current sink for guaranteed operation is 0.41V (V_{CURR} @100mA) and the maximum forward voltage of the LEDs is assumed to be Uf_{max} = 3.8V. Therefore
3 * 3.8V + 0.41V = 11.81V.

As this is the required minimum voltage of the power supply, add all the tolerances on top. Assumed ±10% supply tolerance results in a power supply with nominal 13V (to have at least 11.81V in worst case).

Using the following formula to calculate the external shunt resistor:

(EQ9) $$Rvdd = \frac{VDD_{MIN} - VREGINT_{MAX}}{IVREG_{MAX}} = \frac{VDD_{MIN} - 5.4V}{2.5mA}$$

VDD_{MIN} is the minimum voltage of the power supply, where Rvdd is connected obtains 2564Ω. The nearest lower(!) available value is 2.4kΩ. For Cvdd use:

(EQ10) $$Cvdd = 100nF$$

Csup (100nF) is only required, if there are long connections between the DC-DC converter and the AS3691 (>0.3m). The wire length between the Csup capacitor and the CURRx pin on AS3691 should not exceed 0.3m. If this cannot be guaranteed, add additional capacitors of 100nF to the pins CURRx.

Then calculate the maximum power dissipation inside the AS3691. The worst case is maximum voltage supply (13V + 10%) together with LEDs with minimum forward voltage Uf_{min}:

For these conditions the maximum voltage on any current source (CURR1 to CURR4) is:

(EQ11) $$VCURR_{MAX} = (1 + VDD_{TOL})VDD - nU_{fmin}$$

Not using automatic supply regulation

In our example 14.3V – 9.6V = 4.7V. The maximum power dissipation inside the AS3691 is now (assuming 4 identical strings):

(EQ12) $$P_{MAX} = 4VCURR_{MAX}ICURR$$

In our example 1.88W. As

(EQ13) $$T_{MAX} = \frac{PT - P_{MAX}}{P_{DERATE}} + 50°C$$

Note(s):

For PT and PDERATE see Absolute Maximum Ratings.

- The system can be operated safely up to an ambient temperature of 55°C assuming worst case power supplies and worst case LEDs.
- If the internal junction temperature of the AS3691 rises too high, the AS3691 will switch OFF the current sources for protection (it will never damage the AS3691).

Using Automatic Supply Regulation

For the identical system using the automatic supply regulation, the supply is regulated to minimize the power dissipation of the system. Therefore the tolerance of the VDD supply and also the variation in forward voltages of the LEDs can be ignored (only the difference in one lot of LEDs is still important, as the four strings are connected in parallel to the power supply). Assume a difference of ΔUf = 0.2V of forward voltage of the LEDs in one lot, then calculate the maximum voltage on the current source of the AS3691 (CURR1 to CURR4) with

(EQ14) $$VCURR_{MAX} = n\Delta U_f + V_C$$

Using automatic supply regulation ΔUf variation of LED forward voltage in one lot (for one application) V_C is internal set voltage (1.0V) to be 1.6V. Using the identical formulas as above, P_{MAX} now is 0.64W and T_{MAX} is 110°C.

Therefore using automatic supply regulation, the ambient temperature can be up to 110°C under identical conditions.

Layout Recommendations

See **ams** 'AN3691_TECH_Module Description'[1] as a layout example for the AS3691.

Layout Checklist

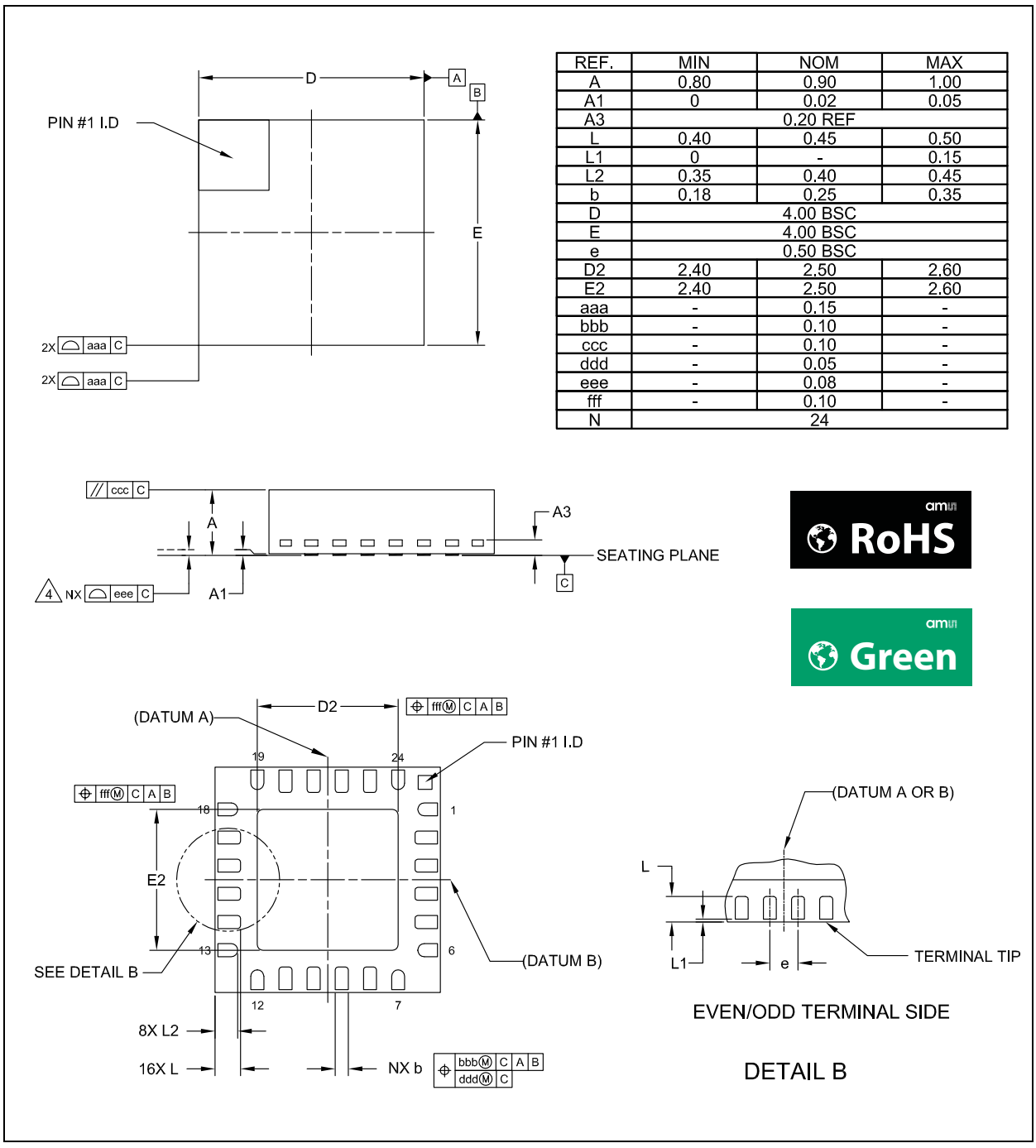
1. Use the bottom layer as ground plane and minimize the number and the length of connections within this layer.
2. Do as many vias as possible on the exposed pad (for thermal performance) to the ground plane.
3. Connect RFBx and RESx together at the current set resistor Rix (see above recommended layout).
4. The ground connections of the current set resistors should be as close to the AS3691 as possible.
5. The ground connection of the capacitor Cvdd should be as close as possible to the AS3691.
6. Minimize Area build by 'Csup VSS connection – Csup Supply Connection – LEDs – CURRx – Csup VSS connection' (to minimize inductance in this path).

1. Please contact **ams** for more information.

Package Drawings & Markings

QFN Package

Figure 22:
QFN 24 – 4 × 4mm Package Drawings



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
L	0.40	0.45	0.50
L1	0	-	0.15
L2	0.35	0.40	0.45
b	0.18	0.25	0.35
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
D2	2.40	2.50	2.60
E2	2.40	2.50	2.60
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		24	

Note(s):

1. Dimensioning and tolerancing conform to ASME Y14. 5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.
6. N is the total number of terminals.

Figure 23:
QFN Marking Diagram

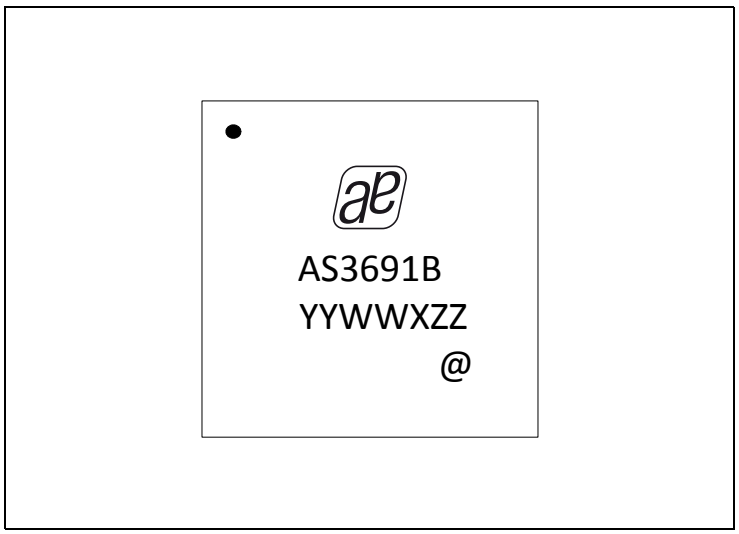
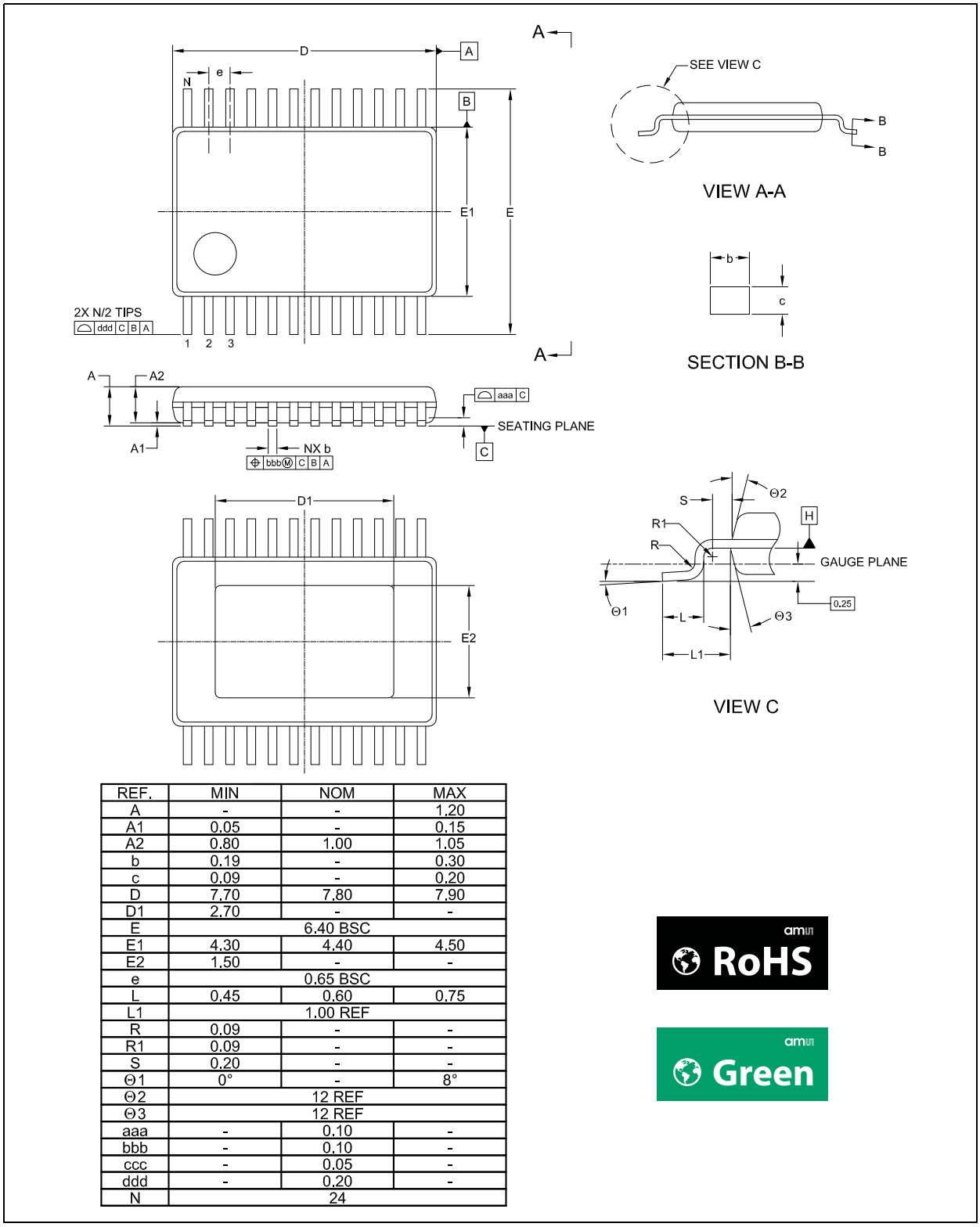


Figure 24:
QFN Package Code

YY	WW	X	ZZ	@
Manufacturing year	Manufacturing week	Plant's identifier	Letters of free choice	Sublot Identifier

eP-TSSOP Package

Figure 25:
eP-TSSOP Package Drawings



REF.	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	7.70	7.80	7.90
D1	2.70	-	-
E	6.40 BSC		
E1	4.30	4.40	4.50
E2	1.50	-	-
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
Θ1	0°	-	8°
Θ2	12 REF		
Θ3	12 REF		
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N	24		

Note(s):

1. Dimensioning and tolerancing conform to ASME Y14. 5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. N is the total number of terminals.

Figure 26:
eP-TSSOP Marking

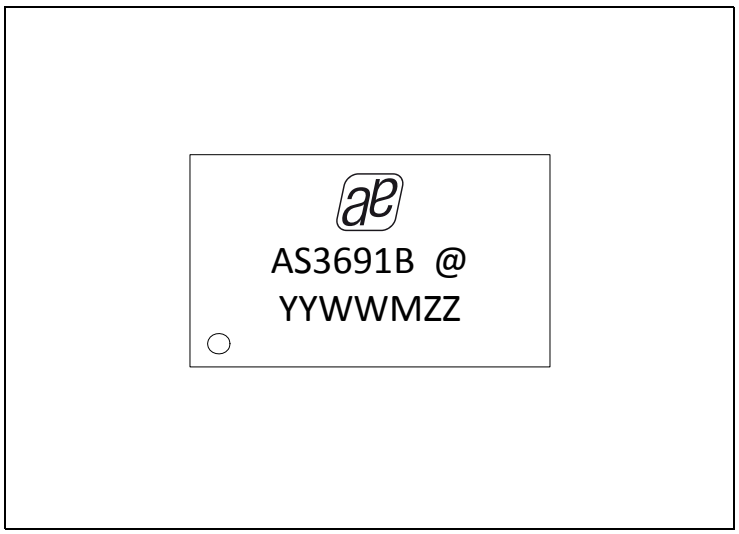


Figure 27:
eP-TSSOP Package Code

YY	WW	M	ZZ	@
Manufacturing year	Manufacturing week	Plant's identifier	Letters of free choice	Sublot Identifier

Ordering & Contact Information

Figure 28:
Ordering Information

Ordering Code	Marking	Package	Delivery Form	Delivery Quantity
AS3691A-ZQFT	AS3691A	QFN24	Trays in Dry Pack	4900 pcs/tray
AS3691B-ZQFT	AS3691B	QFN24	Trays in Dry Pack	4900 pcs/tray
AS3691B-ZQFP	AS3691B	QFN24	Tape and Reel in Dry Pack	6000 pcs/reel
AS3691B-ZTSP	AS3691B	eP-TSSOP24	Tape and Reel in Dry Pack	4500 pcs/reel

Description:

AS3691V-ZPPD

V … AS3691 version, either A or B

AS3691A: 10mV on VRESx (x = 1 to 4) if ONx = 0
(see Detailed Description)

AS3691B: 0mV on VRESx (x = 1 to 4) if ONx = 0
(see Detailed Description)

Z … Temperature range -20°C to 85°C

PP … Package;
QF for QFN, TS for enhanced Power TSSOP

D … Delivery form;
P for Tape & Reel in Dry Pack,
T for Trays in Dry Pack

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Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 2.3 (2007-Oct-30) to current revision 2-07 (2016-Jan-21)	Page
2.3 (2007-Oct-30) to 2-04 (2015-Dec-18)	
Content of austriamicrosystems datasheet was converted to latest **ams** design	
Added benefits to Figure 1	1
Updated Figure Absolute Maximum Ratings	7
Updated Ordering & Contact Information	29
2-04 (2015-Dec-18) to 2-05 (2015-Dec-22)	
Updated QFN Package section	23
Updated eP-TSSOP Package section	25
2-05 (2015-Dec-22) to 2-06 (2016-Jan-18)	
Updated Ordering & Contact Information	27
2-06 (2016-Jan-18) to 2-07 (2016-Jan-21)	
Updated Figure 1	1

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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