AS3977

Multi-Channel Narrowband FSK Transmitter

1 General Description

The AS3977 is a low-power fully integrated ETSI, FCC and ARIB compliant FSK transmitter capable of operating at any ISM frequency in the range of 300 to 928 MHz. It is based on a sigma-delta controlled fractional-N synthesizer phase locked loop (PLL) with fully integrated voltage controlled oscillator (VCO). The power amplifier (PA) output is programmable and can deliver power ranging from –20dBm up to +10dBm. An on-chip low drop-out (LDO) regulator is available in case an accurate output power independent of voltage supply variation is required. The output signal can be shaped using a programmable Gaussian filter to minimize the occupied bandwidth and adjacent channel power. The maximum data rate can be up to 100 kb/s – depending on the required filtering. The FSK frequency deviation is programmable up to a maximum of 64 kHz.

The crystal oscillator can handle a wide range of frequencies. For narrow-band applications, a temperature sensor with digital read-out is included that allows compensation of the crystal frequency drift due to temperature variation.

The AS3977 is connected to an external microcontroller via a bi-directional digital interface. The device operates at very low current consumption with a power supply range from 2.0V to 3.6V and can be powered down when not in use.

The device is fabricated in austriamicroystems advanced 0.35µm SiGe-BiCMOS technology.

2 Key Features

- Fully integrated UHF transmitter
- Compliant to ETSI EN 300-220, FCC CFR47 part 15 and ARIB STD-T67
- Multi-channel with narrow bandwidth
- 300 – 928 MHz operating frequency range (ISM)
- Filtered FSK
- Data rate up to 100 kb/s
- FSK deviation programmable up to 64kHz
- Extremely low power consumption

Main Characteristics

- 2.0 – 3.6V power supply
- Power down current consumption 100 nA (3V, 25ºC)
- Output power up to +10dBm
- Occupied bandwidth 6 kHz (4.8 kb/s, FFSK, ARIB)
- -40 to 85ºC temperature range

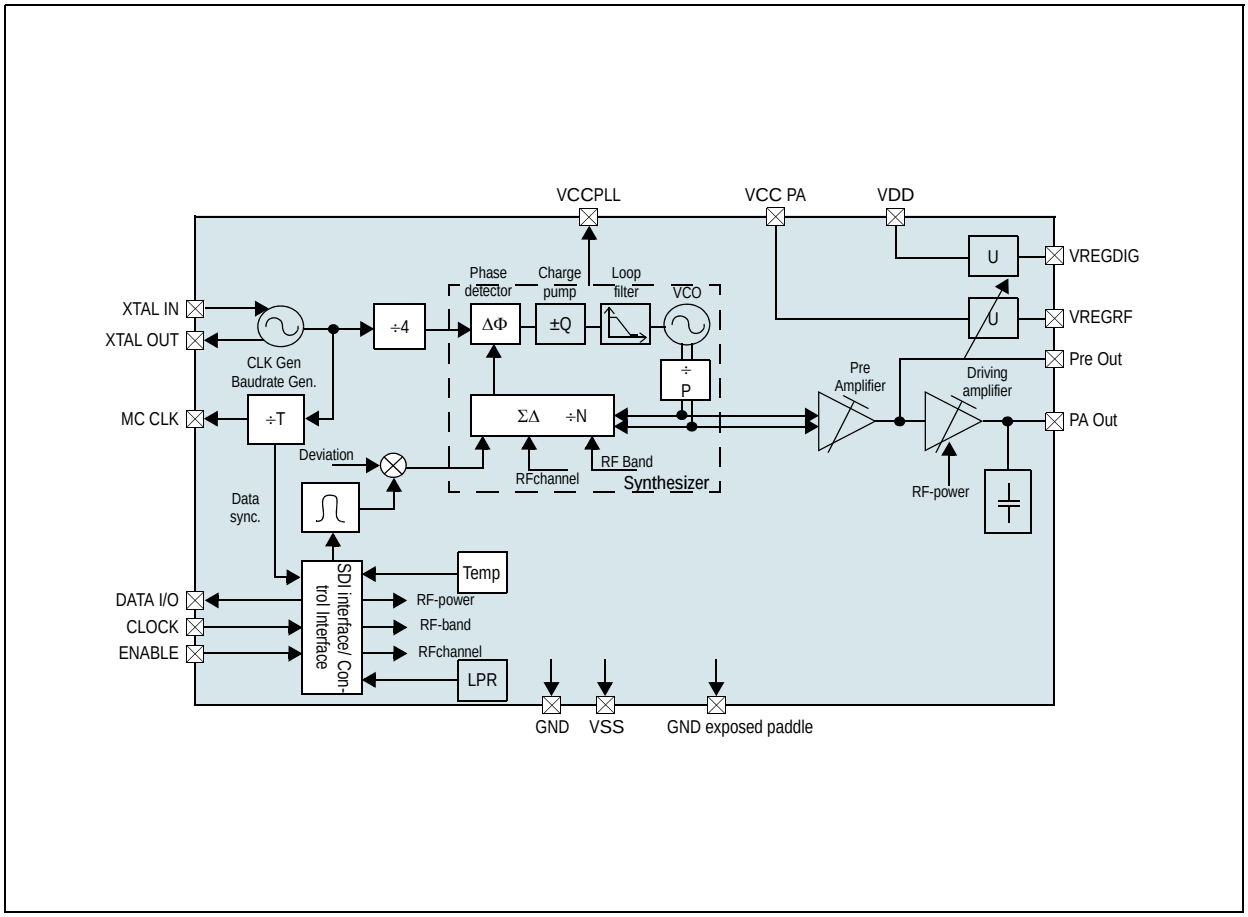
Additional Features

- Sigma-Delta controlled fractional-N synthesizer
- Resolution of synthesizer < 100Hz
- Fully integrated PLL
- Fully integrated voltage controlled oscillator (VCO)
- 4kV ESD protection (1.5kV for the Analog pins)
- 12 – 20 MHz crystal oscillator
- On-chip temperature sensor with digital readout for AFC purposes
- Fast frequency hopping with predefined channel selection
- Microcontroller clock output to save addition crystal
- Constant output power over battery life time
- Integrated Manchester coder
- Digital lock detector
- Low drop-out regulator
- Bi-directional serial interface
- Low Power Down Mode current consumption

3 Applications

The AS3977 is suitable for Remote keyless entry systems, Short range radio data transmission, Domestic and consumer remote control units, Cordless alarm systems, Remote metering, and Low power telemetry.

Figure 1. AS3977 Block Diagram



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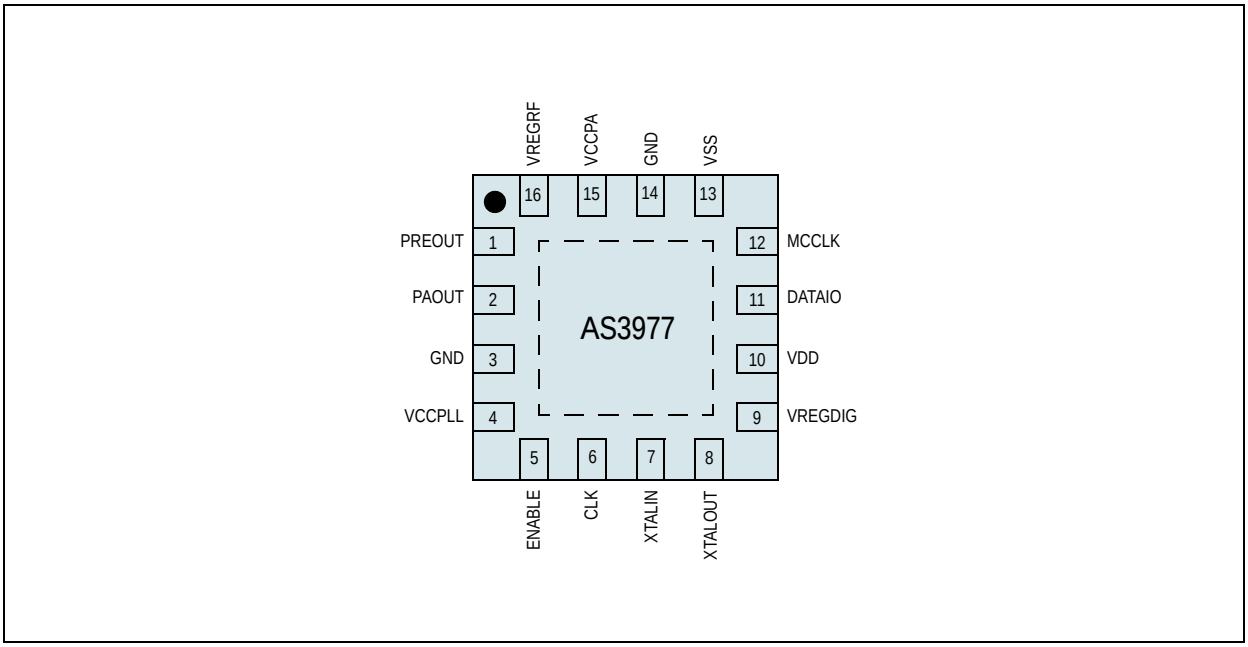
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

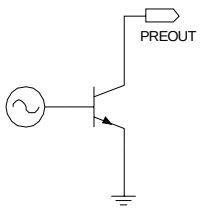
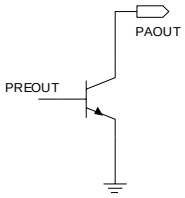
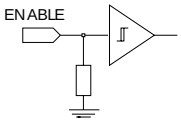
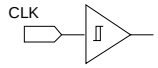
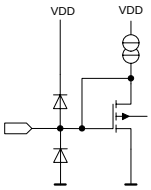
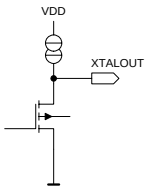
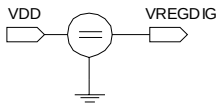
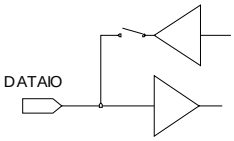
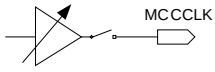
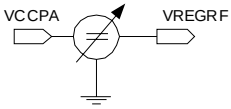
Pin Name	Pin Number	Type	Description
PREOUT	1		Open Collector preamplifier output, need a feeding coil connected to VREGRF or VDD and is the input for the Power amplifier
PAOUT	2		Open Collector power amplifier output, need a feeding coil connected to VREGRF or VDD
RESERVED	3		Must be connected to GND
VCCPLL	4	Positive Power Pin	Positive supplies of VCO, for optimum performance, add decoupling capacitors on this Pin.
ENABLE	5		Digital CMOS level input, internal Pull down resistor > 60k

Table 1. Pin Descriptions

Pin Name	Pin Number	Type	Description
CLK	6		SDI clock
XTALIN	7		XTAL oscillator input, DC Level approximately 1 Volt, needs an DC Blocker in case of external clock
XTALOUT	8		XTAL oscillator output, DC Level approximately 1 Volt
VREGDIG	9		Voltage regulator2 (VRegDig) output, requires a capacitor with nominal 100 nF.
VDD	10	Positive Power Pin	Positive supply of digital part and voltage regulator2 (VRegDig)
DATAIO	11		Digital CMOS level input Pin, SDI data input / output
MCCLK	12		Micro controller clock output Digital output with variable driver strength
VSS	13	GND Pin	Negative supply of digital part
Reserved	14		Must be connected to GND
VCCPA	15	Positive Power Pin	Positive supply of PA and voltage regulator
VREGRF	16		Voltage regulator output to feed the RF Amplifier. For optimum performance a capacitor with nominal 1µF and 100 nF is recommended.
GND	17	GND Power Pin	Negative supply of analogue part (exposed paddle)

5 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” (see Table 3) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Min	Max	Units	Comments
Positive supply voltage (V_{SUP})		-0.5	5.0	V	Voltage on all supply Pins VCCPA,VCCPLL,V_{DD}
Negative supply voltage (GND, V_{SS})		0	0	V	
Input current (latch-up immunity) (I_{SCR})		-40	40	mA	Norm: Jedec 17
ESD for Digital Pins	ESD_{DHBM}	±4		kV	Norm MIL 883 E method 3015 (Human Body Model)
	ESD_{DMM}	±200		V	Norm: EIJA IC-121 (Machine Model)
ESD for Analog Pins	ESD_{AHBM}	±1.5		kV	Norm MIL 883 E method 3015 (Human Body Model)
	ESD_{AMM}	±100		V	Norm: EIJA IC-121 (Machine Model)
ESD for RF Pins	ESD_{RFHBM}	±1.5		kV	Norm MIL 883 E method 3015 (Human Body Model)
	ESD_{RFMM}	±100		V	Norm: EIJA IC-121 (Machine Model)
Total power dissipation (all supplies and outputs)			200	mW	
Storage temperature, (T_{STRG})		-55	125	ºC	
Package body temperature (T_{BODY})			260	ºC	Norm: IPC/JEDEC J-STD-020C. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/ JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”.
Humidity non-condensing		5	85	%	

6 Electrical Characteristics

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SUP}	Positive supply voltage analog	Voltage on all supply VCCPA,VCCPLL,VDD	2.0		3.6	V
GND	Negative supply voltage analog		0		0	V
VSS	Negative supply voltage digital		0		0	V
A-D	Difference of supplies	VCC-VDD, GND-VSS	-0.1		0.1	V
TAMB	Ambient Temperature		-40		85	ºC

Table 4. Block Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OUT315}	Output Frequency Range		300		320	MHz
f_{OUT434}			425		450	
f_{OUT868}			865		870	
f_{OUT915}			902		928	
P_{OUT}	Output Power	Depends on Power Setting				
$f_{FSKdata}$	FSK Data Rate	Internal Manchester Coding	1		100	kbit/s
			0.5		50	
315MHz Frequency Band Section, FCC part 15 is applicable						
ΔFSK_1	FSK Deviation	programmable (8bit) Resolution of FSK Deviation (see Table 5)	0		±64	kHz
P_{SPE1}	Spurious Emissions (max. –19.6dBm radiated fundamental power)[1]	216-960MHz			-49	dBm
		at frequencies > 960Mhz			-41	
		at harmonics			-40	
	Phase noise @ 50 kHz	Charge pump setting: I_{CHP}=50µA; V_{SUP}=2.0..3.6V, TAMB=-40..85ºC		-86		dBc/Hz
	Phase noise @ 250 kHz			-92		
	Phase noise @ 1 MHz			-102		
434MHz Frequency Band Section, EN 300 220 and/or ARIB STD-T67 are applicable						
ΔFSK_2	FSK Deviation	Small deviation (ARIB), programmable (8bit) Resolution of FSK Deviation (see Table 5)	±1.25		±4	kHz
			0		±64	
	Phase noise @ 50 kHz	Charge pump setting: I_{CHP}=50µA; V_{SUP}=2.0…3.6V, TAMB=-40…85ºC		-86	-83	dBc/Hz
	Phase noise @ 250 kHz			-94		
	Phase noise @ 1 MHz			-102		
P_{ACP2}	Adjacent Channel Power	ARIB, f_{REF}=4MHz, I_{CHP}=50µA			-40	dBc
OBW_2	Occupied Bandwidth	Channel spacing 12.5 kHz, FSK data rate 4.8 kbit/s (ARIB) FSK Deviation ±1.8 KHz			8.5	
		GF Setting (see Gaussian Filter Clock Setting on page 38) Channel spacing 25 kHz, FSK data rate 9.6 kbit/s (ARIB) FSK Deviation ±3.0 KHz	8.5		16	kHz

Table 4. Block Specification (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
P_{SPE2}	Spurious Emissions excluding Harmonics[1]	47-74MHz 87.5-118MHz 174-230MHz 470-862MHz (EN 300 220)			-54	dBm
	Spurious Emissions and Harmonics[1]	at other frequencies < 1GHz at ≥ 1GHz (EN 300 220)			-36 -30	dBm
		ARIB			-29	
f_{ERROR}	Output Frequency Error	With ideal crystal, V_{SUP}=2.0…3.6V, TAMB=-40…85ºC			±1	ppm
868MHz Frequency Band Section, EN 300 220 is applicable						
ΔFSK_3	FSK Deviation	programmable (8bit) Resolution of FSK Deviation (see Table 5)	0		±64	kHz
P_{SPE3}	Spurious Emissions excluding Harmonics[1]	47-74MHz 87.5-118MHz 174-230MHz 470-862MHz (@-10dBm radiated power)			-54	dBm
	Spurious Emissions and Harmonics[1]	at other frequencies < 1GHz at frequencies ≥ 1GHz			-36 -30	dBm
	Phase noise @ 50 kHz	Charge pump setting: I_{CHP}=50µA; V_{SUP}=2.0…3.6V, TAMB=-40…85ºC			-78	dBc/Hz
	Phase noise @ 250 kHz				-85	
	Phase noise @ 1 MHz				-89	
915MHz Frequency Band Section, FCC part 15 is applicable						
ΔFSK_4	FSK Deviation	programmable (8bit) Resolution of FSK Deviation (see Table 5)	0		±64	kHz
P_{SPE4}	Spurious Emissions (max. –1dBm radiated fundamental power)[1]	216-960MHz at frequencies > 960MHz and harmonics			-49 -41	dBm

1. These parameters will not be tested.

Table 5. Resolution of FSK Deviation

Symbol	Parameter	Conditions	Equation for Min. Resolution	Units
315MHz and 434MHz Frequency Band Section				
ΔFSK_{res1}	Resolution of FSK Deviation[1]	For detailed information, See FSK Deviation Setting and Frequency Trimming on page 37	$\Delta F = (INT <8> +1). \frac{f_{REF}}{2^{16}}$	Hz
868MHz and 915MHz Frequency Band Section				
ΔFSK_{res2}	Resolution of FSK Deviation[1]	For detailed information, See FSK Deviation Setting and Frequency Trimming on page 37	$\Delta F = (INT <8> +1). \frac{f_{REF}}{2^{15}}$	Hz

1. INT<8> refer to Register Settings

Table 6. Reference Frequency Generator and Micro Controller Clock Driver

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Crystal Oscillator						

Table 6. (Continued)Reference Frequency Generator and Micro Controller Clock Driver

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{XOSC}	Crystal Oscillator Frequency		12	16	20	MHz
t_{XOSC}	Crystal Oscillator Start up time	V_{SUP}=2.0…3.6V, TAMB=-40…85ºC crystal series resistance ≤ 100Ω			1.5	ms
R_{XOSC}	Crystal Oscillator Oscillation Margin Level	f_{XOSC}=13.56MHz, C_L=12pF	1500			Ω
$\Delta f/f_0$	Frequency Stability vs. Temperature[1]	AS3977 Only			±1	ppm
Micro Controller Clock Driver						
f_{MCCLK}	Clock output frequency	depending on configuration register settings and crystal			4	MHz
V_{MCL}	Low level output voltage	V_{SUP}=3V, at nominal high level output current			0.1*V_{SUP}	V
V_{MCH}	High level output voltage	V_{SUP}=3V, at nominal high level output current	0.9*V_{SUP}			V
C_{LMCC}	Capacitive load				20	pF
t_{RMCC}	Rise time				62.5	ns
t_{FMCC}	Fall time				62.5	ns
I_{MCH}	High level output current				1	mA
I_{MCL}	Low level output current				1	mA

1. These parameters will not be tested.

Table 7. Phase Locked Loop

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{REF}	Comparison Frequency	depending on f_{XOSC} (reference divider division ratio = 4)	3.0	4.0	5.0	MHz
Δf_O	Output Frequency Resolution	f_{OUT315} / f_{OUT434}	46	61	77	Hz
		f_{OUT868} / f_{OUT915}	92	122	153	
t_{SYNTH}	Synthesizer Start up Time			500		µs
t_{LOCK}	Synthesizer Lock Time	Δf=600kHz, f_{ERROR} @ t_{LOCK}=10kHz		50	200	µs

Table 8. Loop Filter Bandwidth

Symbol	Parameter		Conditions	Min	Typ	Max	Units
Filter Bandwidth at 315 MHz							
f_{BW}	Charge pump setting: I_{CHP}	@ 12.5 µA	Reference Frequency = 4MHz VSUP = 3.0 V; TAMB = 25ºC		55		kHz
		@ 25 µA			85		
		@ 37.5µA			115		
		@ 50 µA			170		
Filter Bandwidth at 433 MHz							

Table 8. (Continued)Loop Filter Bandwidth

Symbol	Parameter		Conditions	Min	Typ	Max	Units
f_{BW}	Charge pump setting: I_{CHP}	@ 12.5 µA	Reference Frequency = 4MHz VSUP = 3.0 V; TAMB = 25ºC		50		kHz
		@ 25 µA			70		
		@ 37.5µA			90		
		@ 50 µA			120		
Filter Bandwidth at 868 MHz							
f_{BW}	Charge pump setting: I_{CHP}	@ 12.5 µA	Reference Frequency = 4MHz VSUP = 3.0 V; TAMB = 25ºC		50		kHz
		@ 25 µA			70		
		@ 37.5µA			90		
		@ 50 µA			120		

Table 9. Power Amplifier (300 - 320 MHz and 425 - 450 MHz Bands)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POUT	Min. Output Power @ 50Ω	VSUP=3V, @ 25ºC, Power depending on power setting with or without the use of the internal voltage regulator, external matching network included		-20		dBm
POUT	Max. Output Power @ 50Ω	VSUP=3V, @ 25ºC, Power depending on power setting with or without the use of the internal voltage regulator, external matching network included		8		dBm
POUT	Output Power Variation@ 50Ω[1] (300 – 320MHz)	VSUP=3V, @ 25ºC, Power depending on register setting with or without the use of the internal voltage regulator, external matching network included, strong AB operation mode	-2.5		+2.5	dBm
POUT	Output Power Variation@ 50Ω[1] (425 – 450MHz)	VSUP=3V, @ 25ºC, Power depending on register setting with or without the use of the internal voltage regulator, external matching network included, strong AB operation mode	-2.0		+2.0	dBm
POUT	Output Power Variation vs. VDD and Temperature @ 50Ω	VSUP=2.2…3.6V, TAMB=-40…85ºC, With the use of the internal voltage regulator, external matching network included, strong AB operation mode	-2.8	+0.6 / -1.5	1.0	dB
POUT	Output Power Variation vs. Temperature @ 50Ω	VSUP=3V, TAMB=-40..85ºC, Without the use of the internal voltage regulator, external matching network included, strong AB operation mode		+1.5 / -2.0		dB
POUT	Max Output Power @ 50Ω	VSUP=3.6V, @ 25ºC, Power depending on power setting without the use of the internal voltage regulator, external matching network included		10		dBm

1. Limits by production test measurement uncertainties

Table 10. Power Amplifier (865 - 870 MHz and 902 - 928 MHz Bands)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POUT	Min Output Power @ 50Ω	VSUP=3V, @ 25ºC, Power depending on power setting with or without the use of the internal voltage regulator, external matching network included		-20		dBm
POUT	Max Output Power @ 50Ω	VSUP=3V, @ 25ºC, Power depending on power setting with or without the use of the internal voltage regulator, external matching network included		4		dBm
POUT	Output Power Variation @ 50Ω[1]	VSUP=3V, @ 25ºC, Power depending on register setting with or without the use of the internal voltage regulator, external matching network included, strong AB operation mode[2]	-3.5		+3.5	dBm
POUT	Output Power Variation vs. VDD and Temperature @ 50Ω	VSUP=2.2…3.6V, TAMB= -40…85ºC, With the use of the internal voltage regulator, external matching network included, strong AB operation mode[2]		+2.0 / -3.0		dB
POUT	Output Power Variation vs. Temperature @ 50Ω	VSUP=3V, TAMB=-40…85ºC, Without the use of the internal voltage regulator, external matching network included, strong AB operation mode[2]		+2.0 / -3.0		dB

1. Limits by production test measurement uncertainties
2. Power line matching needs to be adjusted to VDD to ensure strong AB operation mode

Table 11. Antenna Tuning Circuit

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{Atmin}	Minimum Antenna tuning Capacitor	ATCPH <3:0> = 0000		0.11		pF
C_{Atmax}	Maximum Antenna tuning Capacitor	ATCPH <3:0> = 1111		1.51		pF

Table 12. Low Power Reset (Bit LT)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{LPR}	Low Power Detection Threshold Voltage	Decreasing Supply Voltage	1.85	1.95	2.05	V
V_{LPR}	Low Power Release Threshold Voltage	Rising Supply Voltage		2.05		V

Table 13. Low Supply Voltage Detector (Bit LS)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{LS}	Low Supply Detection Threshold Voltage	Decreasing Supply Voltage	2.0	2.1	2.2	V
V_{LS}	Low Supply Release Threshold Voltage	Rising Supply Voltage		2.17		

Table 14. Temperature Sensor

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ERR_{TS}	Absolute Error	T_{AMB} = -40…85ºC	-5		+5	ºC
ERR_{TSL}	Absolute Error (limited temperature range)	T_{AMB} = -20…65ºC		±2		ºC
	Conversion Factor	T_{AMB} = -40…85ºC		0.19		ºC/bit
OR_{TS}	Output Resolution			10		bit
CR_{TS}	Conversion Rate	$f_{TS} = f_{CRYSTAL}/12$ after startup time of 256 / f_{TS}			$f_{TS}/1354$	samples/s

Table 15. Voltage Regulator for Power Amplifier

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VREGRF	Output Voltage for supply Power Amplifier	Adjustable, nominal value	1.7		2.0	V
D_VREGRF	Regulator Tolerance		-0.15		0.1	V

Table 16. Current Consumption

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{PDWN}	Power Down Mode	V_{SUP}=3V @ 25ºC			100	250	nA
		V_{SUP}=2.0…3.6V, T_{AMB}=-40…85ºC			1000	5000	
I_{CLKEN}	Clock Enable Mode	V_{SUP}=3V @ 25ºC, C_{load}≤20pF, f_{CLK}=20MHz			1	1.25	mA
		V_{SUP}=2.0…3.6V, T_{AMB}=-40..85ºC, Cload≤20pF, f_{CLK}=20MHz			1.25	1.6	
I_{Temp_sens}	Temperature sensor Current	V_{SUP}=2.0..3.6V, T_{AMB}=-40..85ºC			0.25		mA
I_{PLLEN}	PLL Enable Mode	V_{SUP}=2.0…3.6V, T_{AMB}=-40…85ºC			5.6		mA
$ITX8dBm_{315}$	Transmit Mode @ 8dBm output power, 315 MHz band @ 50Ω including matching network, strong AB operation	V_{SUP}=3V @ 25ºC	without the use of the internal regulator[1]		13.5	16.5	mA
		V_{SUP}=2.0…3.6V, T_{AMB}=-40…85ºC			15.5	19	mA
		V_{SUP}=3V @ 25ºC	with the use of the internal regulator		14.0	17.0	mA
		V_{SUP}=2.2…3.6V, T_{AMB}=-40…85ºC			16.0	19.5	mA
$ITX8dBm_{433}$	Transmit Mode @ 8dBm output power, 433 MHz band @ 50Ω including matching network, strong AB operation	V_{SUP}=3V @ 25ºC	without the use of the internal regulator		12.5	15.5	mA
		V_{SUP}=2.0…3.6V, T_{AMB}=-40…85ºC			14.5	18	mA
		V_{SUP}=3V @ 25ºC	with the use of the internal regulator		13.0	16.0	mA
		V_{SUP}=2.2…3.6V, T_{AMB}=-40…85ºC			15	18.5	mA

Table 16. Current Consumption

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$ITX4dBm_{868}$	Transmit Mode @ 4dBm output power, 868 MHz and 906MHz band @ 50Ω including matching network, strong AB operation	V_{SUP}=3V @ 25ºC	without the use of the internal regulator		14.5	17.5	mA
		V_{SUP}=2.0…3.6V, T_{AMB}=-40…85ºC			16.5	19.0	mA
		V_{SUP}=3V @ 25ºC	with the use of the internal regulator		15.0	18.0	mA
		V_{SUP}=2.2…3.6V, T_{AMB}=-40…85ºC			17.0	19.5	mA

1. Power line matching needs to be adjusted to VDD to ensure strong AB operation mode

Table 17. DC/AC Characteristics for Digital Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS Input						
V_{IH}	High Level Input Voltage		0.7 * V_{SUP}		V_{SUP} + 0.1	V
V_{IL}	Low Level Input Voltage		V_{GND} -0.1		0.3 * V_{SUP}	V
I_{IL}	Low Level Input Leakage Current	no internal pull up/down			±1	µA
I_{IH}	High Level Input Leakage Current	no internal pull up/down			±1	µA
I_{IHPD}	High Level Input Leakage Current with internal pull down	V_{SUP}=3.6V, V_{IN}=3.6V	15		60	µA
CMOS Output **Note:** The following specification is valid for the DATAIO standard CMOS output. The MCCLK output can be programmed to different driver strengths according MCCDS register.						
V_{OH}	High level output voltage	V_{SUP}=3V, at nominal high level output current	V_{SUP}-0.5			V
V_{OL}	Low level output voltage	V_{SUP}=3V, at nominal low level output current			V_{SS}+0.4	V
C_L	Capacitive load				20	pF
t_R	Rise time				50	ns
t_F	Fall time				50	ns
I_{OH}	High level output current				1	mA
I_{OL}	Low level output current				1	mA

7 Timing Characteristics

Be aware that the Power Down Mode can be entered by setting ENABLE low for more than 2^{16} XTAL cycles (Power Down Timer).

Figure 3. Write Data

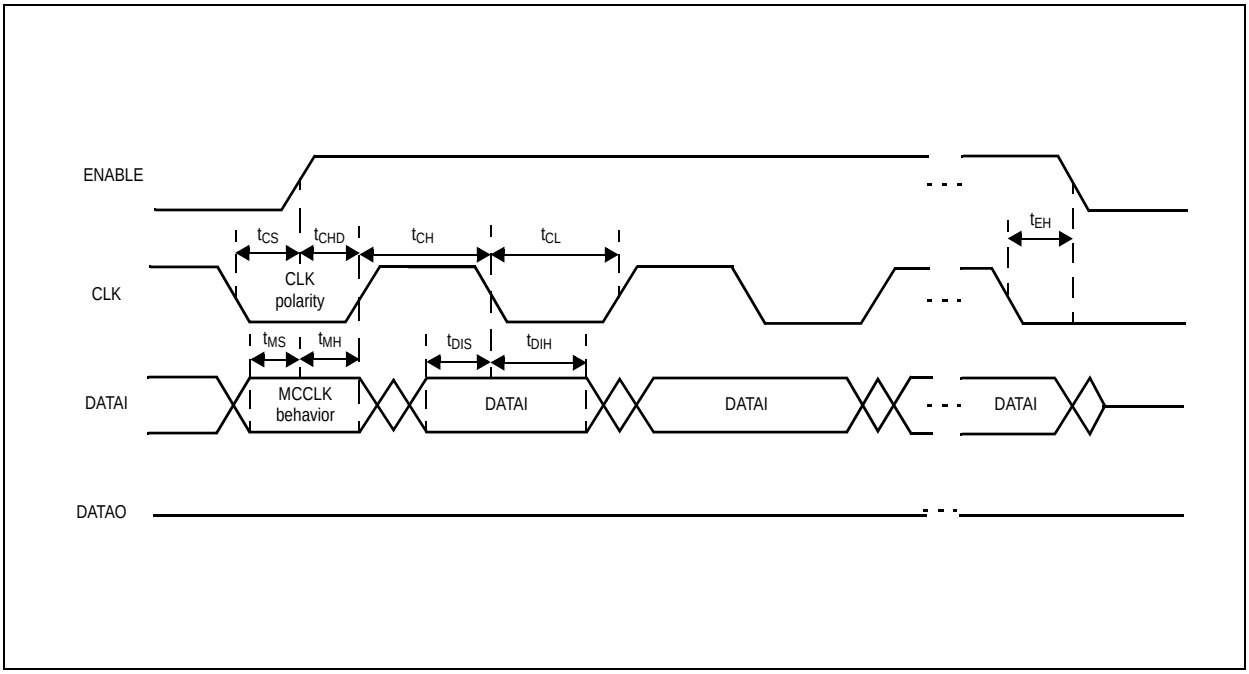
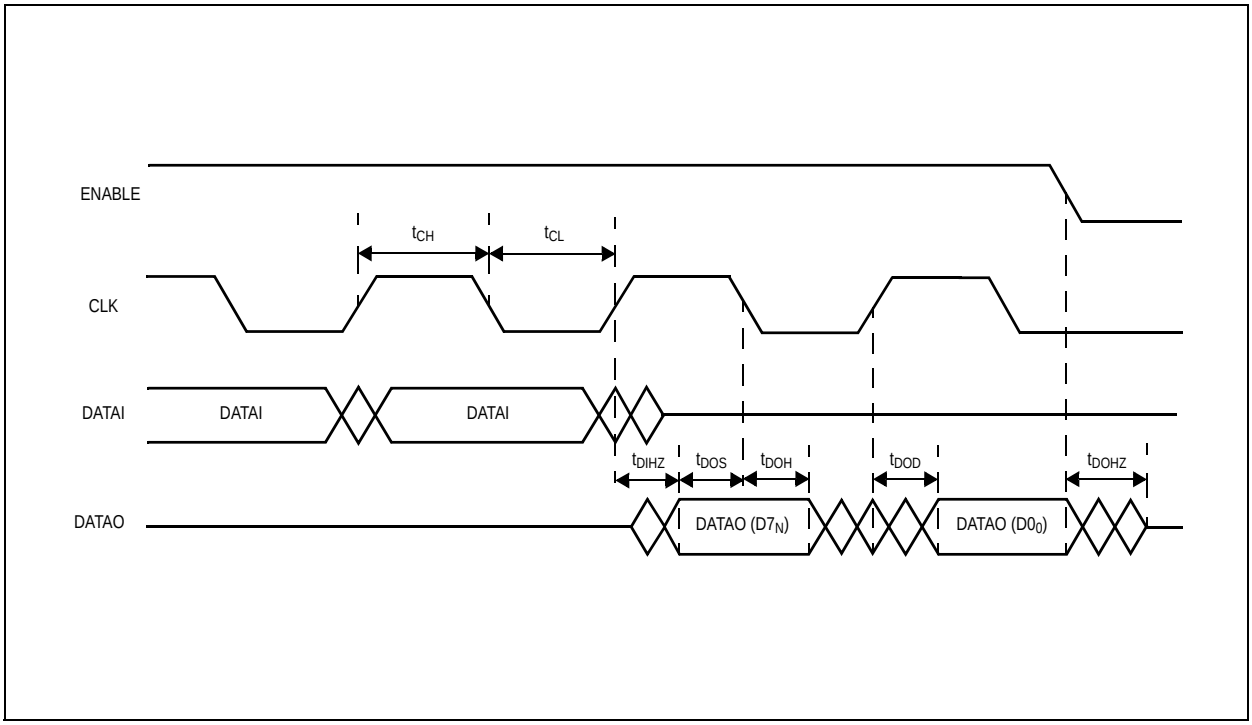


Figure 4. Read Data



7.1 Timing Parameters

Table 18. Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
General						
BR_{SDI}	Bit rate				2	Mbps
t_{CH}	Clock high time		250			ns
t_{CL}	Clock low time		250			ns
Write timing						
t_{DIS}	Data in setup time		20			ns
t_{DIH}	Data in hold time		10			ns
t_{EH}	Enable hold time		20			ns
Read timing						
t_{DIHZ}	Data in to high impedance delay	time for the µC to release the DATAIO bus			45	ns
t_{DOS}	Data out setup time		130			ns
t_{DOH}	Data out hold time		135			ns
t_{DOD}	Data out delay				80	ns
t_{DOHZ}	Data out to high impedance delay	time for the SDI to release the DATAIO bus			80	ns
Timing parameters when leaving the Power Down Mode (for determination of CLK polarity and MCCLK behavior)						
t_{CS}	Clock setup time (CLK polarity)	Setup time of CLK with respect to ENABLE rising edge	20			ns
t_{CHD}	Clock hold time (CLK polarity)	Hold time of CLK with respect to ENABLE rising edge	20			ns
t_{MS}	Data in setup time (MCCLK behavior)	DATAIO setup time with respect to ENABLE rising edge	20			ns
t_{MH}	Data in hold time (MCCLK behavior)	DATAIO hold time with respect to ENABLE rising edge	20			ns

8 Detailed System Description

The AS3977 is based on a fully integrated sigma-delta controlled fractional-N synthesizer phase locked loop (PLL) and a power amplifier (PA). A reference frequency generator including a crystal oscillator provides the comparison frequency of the PLL and a high-precision clock output. A programmable Gaussian filter enables to minimize the occupied bandwidth and adjacent channel power. A temperature sensor with digital read-out is included that allows compensation of the crystal frequency drift due to temperature variation. An on-chip low drop out regulator (LDO) is available in case an accurate output power independent of supply voltage variation is required. A second LDO for the digital supply voltage helps to minimize interference between the analog and digital part and decreases the current consumption of the digital part. A PROM enables the compensation of process variation. The AS3977 is controlled by an external microcontroller via a bi-directional serial digital interface (SDI).

8.1 Reference Frequency Generator

The reference frequency generator consists of a crystal oscillator and frequency divider. The crystal oscillator can be driven externally in case an external clock frequency is supplied.

8.2 Phase Locked Loop

The PLL is of standard charge pump type. The phase frequency detector is designed such that dead zone problems are avoided. The charge pump current is programmable. All loop filter components are on-chip, the bandwidth is programmable through the charge pump current. The differential based voltage controlled oscillator (VCO) has integrated inductors and varactors. The VCO operates at a center frequency around 1.8GHz. To cover the specified frequency range over process variation, the sufficiently wide overall tuning range is split into 16 overlapping frequency bands. At start up of the PLL, an automatic range select circuit (ARS) selects the proper frequency band. The VCO output frequency is divided by 2, 4, and 6, which enables to cover output frequencies in the range of 850 – 928 MHZ, 425 – 450 MHz and 300 – 320 MHz, respectively. A lock detector enables to monitor the PLL lock status.

8.3 Gaussian Filter and Digital Modulator

The programmable sigma-delta modulator controls the output frequency of the PLL. The order of the modulator is programmable (MASH2 or MASH3). In combination with the programmable Gaussian filter for the data signal, the modulator performs the FSK modulation with programmable deviation, whereby the Gaussian Filter enables to minimize the occupied bandwidth and the adjacent channel power.

8.4 Power Amplifier

The power amplifier is single ended and consists of a preamplifier and an output stage, both with open collector. The necessary external chokes can be connected to a LDO in case an accurate output power independent of supply voltage variation is required. The output power is programmable up to 10dBm.

8.5 Temperature Sensor

The AS3977 includes a temperature sensor to measure the absolute temperature inside the chip. The analog value is converted to a digital value and can then be read out by the microcontroller in order to control the output frequency and/or the transmission power. The value of the chip temperature in degree can be obtained using following formula:

$$Temperature = TS < 9...0 > * 0.19 - 50 \qquad (EQ\ 1)$$

The temperature sensor can be used to compensate the crystal drift over temperature.

Note: AS3977 has the same temperature than the crystal only at start up and the temperature will increase immediately thereafter due to self heating.

Temperature sensor must be used only in the Clock Enable Mode as a stand alone block. It is mandatory to be used with the PLL and Power Amplifier switched off.

8.6 Low Power Reset

The low power reset (LPR) disables the power amplifier, if the supply voltage falls below the low power threshold.

8.7 Low Drop Out Regulators

In order to avoid stability issues, external capacitors are required. (see Table 1)

8.8 SDI / Control Interface

This interface enables a serial and synchronous communication between external microcontroller and AS3977. Data can be written to and read out from AS3977. Additionally, it facilitates the transmission of TX-data. The rising edge on the SDI enable signal (transition to the active state), while the device is in Power Down Mode has various effects on the circuit:

- It wakes up the crystal oscillator (this takes maximum 1.5 ms with the specified Crystal parameters)
- It sets the transfer and sampling edge of the AS3977 SDI data signal.
- It activates the Micro Controller clock output depending on the register setting and the value of the data signal.

Thus, the wakeup event through the SDI interface determines the basic communication between AS3977 and the microcontroller. In addition it takes some time to have a stable crystal oscillator clock available. Therefore all functions that require a stable crystal oscillator clock are not immediately available after the wakeup.

8.9 Baud Rate Generator

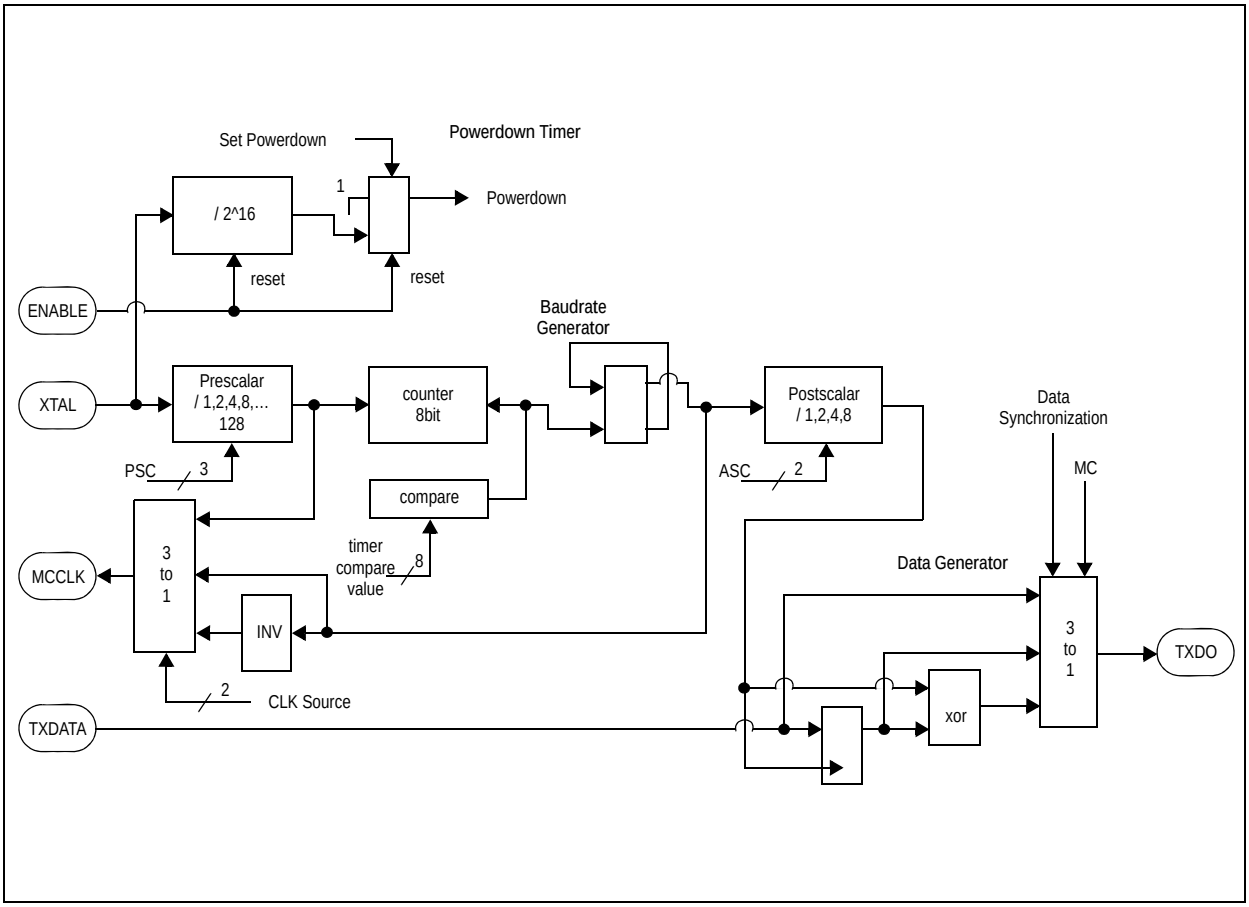
This module generates two clocks; one used for the microcontroller (MCCLK) and one as baud rate clock with 50% duty cycle. The baud rate clock is used by the microcontroller to properly synchronize the provided data during transmission with the internal Manchester coder.

The baud rate generator maintains the behavior of MCCLK and keeps it properly synchronized to the TX data clock. For example, a missing synchronization can occur when clock settings are changed by an asynchronous event like SDI programming or when a new transmission starts.

The Baud rate generator offers different types of data outputs: one fully asynchronous, one synchronous and one synchronous but Manchester coded. By means of AS3977 command control Byte, any of the three different output data types can be selected.

9 Application Information

Figure 5. Functional Description Diagram of Timers and Data Synchronization



The Prescaler divides the XTAL frequency by $f_{OUT}=2^{-PSC<2:0>}*f_{IN}$

The Compare timer divides by $f_{OUT}=f_{IN}/(TCV+1)$ and the Postscaler divides the input frequency by $f_{OUT}=2^{-ASC<1:0>}*f_{IN}$ which leads into a data frequency of:

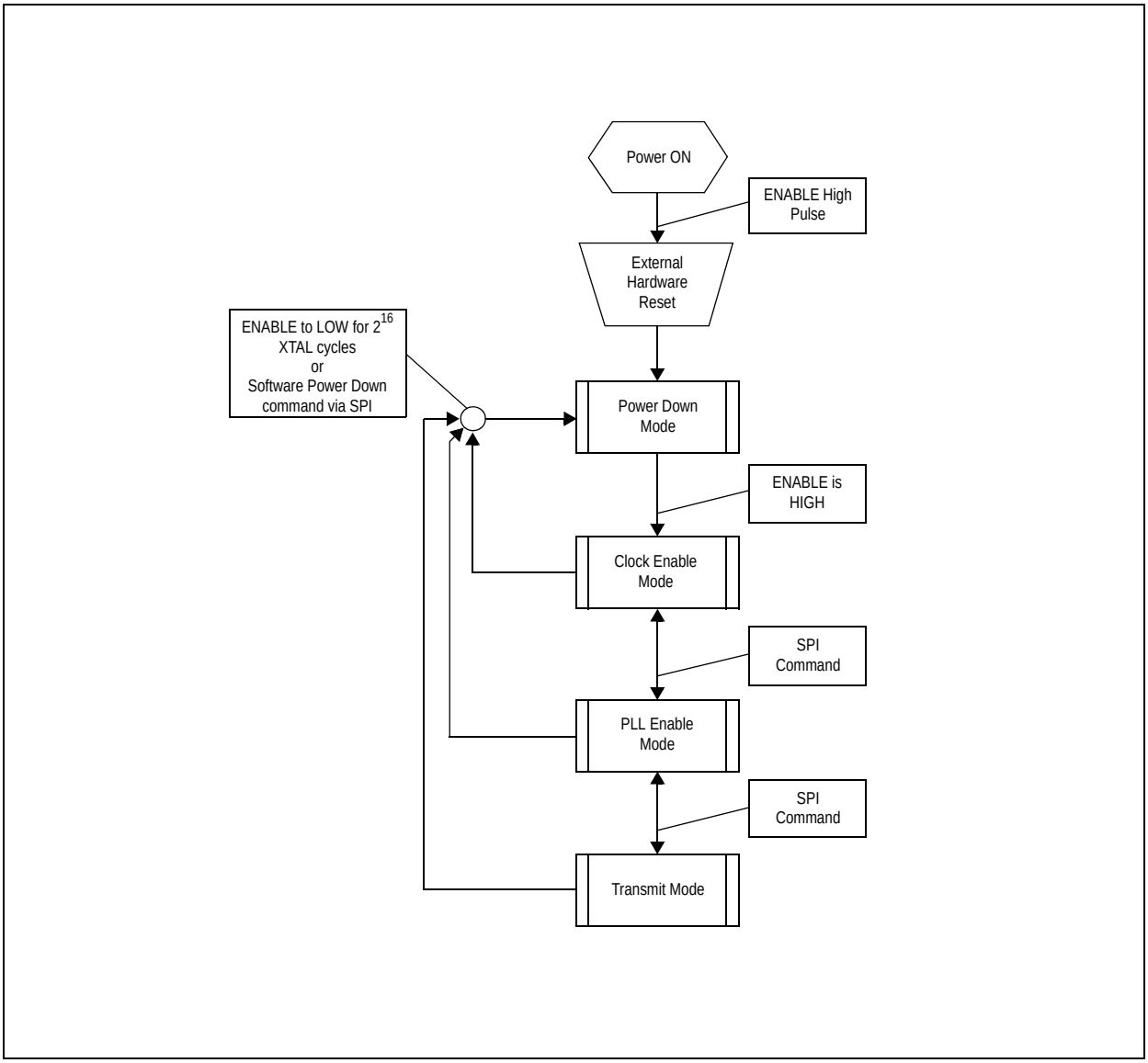
$$f_{OUT}=2^{-(PSC<2:0>+ASC<1:0>+1)} * f_{IN} / (TCV+1) \quad \text{(EQ 2)}$$

9.1 Operation Modes

All modes are controlled by the SDI interface.

- Power Down Mode
  The AS3977 is connected to the power supply and can be switched to power down mode. The current consumption is limited by the leakage current.
- Clock Enable Mode
  In this mode, only the reference frequency generator is switched on and a clock signal is supplied via the clock output.
- PLL Enable Mode
  The PLL is switched on and locked at the selected output frequency. The power amplifier is in power down mode. This mode enables OOK-ASK modulation by switching the PA on and off.
- Transmit Mode
  The PLL is switched on and locked at the selected output frequency. The power amplifier is in power on mode. This is the FSK mode for transmitting data.

Figure 6. Operation Mode Relations



9.2 Transmitter Control Interface

The AS3977 is controlled by an external micro controller (µC) via. a bi-directional communication interface (serial digital interface, SDI). The SDI enables data to be read from and written to internal control registers without the necessity of an internal clock signal. Analog de-bouncing of clock and data input is implemented in order to improve the overall system reliability.

The SDI-control interface includes a state machine, which expects a command control word as first byte and in reference to this byte, the interface is configured as write, read, or transmit operation. This method enables an effective and easy control of basic transmitter functions. Four preset independent output frequencies and two preset independent output power levels and modulation types can be selected using the control-command byte, thus enabling fast channel hopping and/or fast changes to the output power level and modulation type. The selection of the active output frequency and/or power level and modulation type is done using the so-called command byte.

As an additional feature, the AS3977 provides a configurable clock signal derived from the crystal frequency. The purpose of this clock signal is to provide a µC clock and to enable data synchronization.

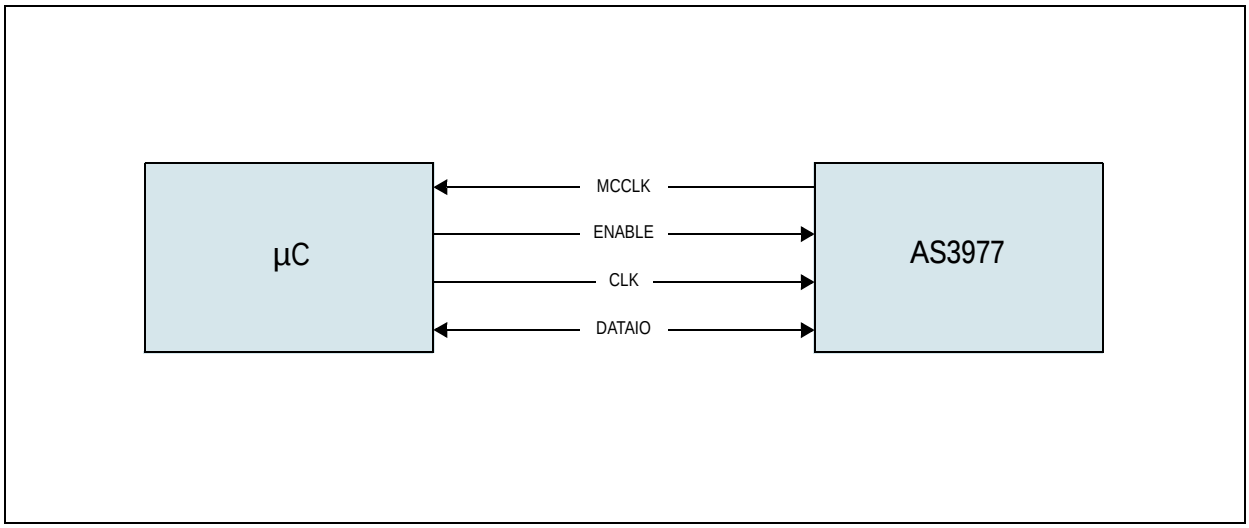
A timer is included to power down (Power Down Mode) the transmitter after a certain time, which is defined as 2^{16} multiplied with the crystal oscillator- Period.

9.2.1 Configuration Diagram

The interface has one clock signal for the external µC and the SDI input clock. As the MCCLK line can be used to clock the SDI Interface as well as must have a high impedance pin during the clocking phase of the microcontroller, the Pin must be bi-directional. The pad behavior is selected by configuration bits and by setting the SDI DATA-IO Line of the SDI interface when leaving PD. Possible configurations between the interface and the µC are done using 4 wires as shown in Figure 7.

MCCLK is simply connected to the micro controller and can be used to clock a timer or interrupt logic.

Figure 7. Configuration Diagram



A connection using a set of three wires is required to implement the SDI protocol.

- ENABLE signal is used to activate the interface and to wake up the whole IC. In addition, the rising edge of the ENABLE after power down mode is used to set the starting point of the communication protocol.
- CLK represents the SDI clock and both edges can be used for data transfer, dependable on the configuration after wake-up.
- DATAIO is a bi-directional signal that goes from microcontroller to the Interface during write and transmit-commands, while it is in the other direction when the interface is sending data read from the micro controller.

The interface supports the following functionality for the micro controller clock output (MCCLK).

- MCCLK can be inactive (MCCLK level not defined), always active after start-up (MCCLK is clocking) or clocking only during transmit.
- It is possible to configure and to maintain MCCLK settings (even when leaving PD).
- Maximum frequency is specified to f_{XOSC} (by using the prescaler output with a division ratio of 1, PSC=0).
- Minimum frequency is f_{XOSC} / 65280 (by using the baud rate generator output with prescaler division ratio of 128 and timer counter value of 255).

The rising edge of ENABLE after a Power Down Mode selects the transfer edge of the SDI-CLK by sampling the SDI clock value itself. This configuration will be valid until the next PD. Each bit must be transferred and sampled according to the configured edges. For example, if at the first rising edge of SDI enable SDI clock is LOW, then each bit is transferred from the microcontroller on the rising edge of SDI clock and it is sampled from AS3977 on falling edge of the SDI clock. This is valid for read as well as for write commands.

During the first byte of the WRITE command communication (command and address), the SDI master drives each new data bit on the transfer active edge and the SDI slave samples it on the next opposite edge. This protocol will be valid until the last data bit has been written to the external registers. Data' are transferred to the registers byte by byte after sampling of the last bit.

It is not necessary to enter the PD mode for reset the Interface. The rising edge of SDI-ENABLE signal starts the communication.

When the command is READ, a direction change on the SDI data wire will be done. This change has to be performed synchronously on SDI master and slave side, however, the master always provide the SDI clock. After sampling the last addressed bit, the SDI slave pin becomes active on the following SDI clock edge and the first readable bit read is transferred from SDI slave to the master.

In any case, the SDI master has to reset the SDI interface on the last bit of the data in order to stop the communication by applying an Enable LOW pulse (duration: min > 1 SDI CLK cycle, max: < $1/f_{crystal} * 2^{16}$).

9.2.2 Power On Reset

For stable start up of the AS3977 and to avoid unwanted crystal oscillation, it is strongly recommended to perform a power on reset (Hardware Reset Method). This can be performed as described in Table 19 and must be carried out every time when the supply voltage is less than the minimum allowed value (see Operating Conditions on page 8).

Table 19. Power On Reset

Step	Hardware Reset Method
1	Apply Power to the AS3977
2	Apply Enable high pulse (Low-High-Low transition)
3	Power on reset complete after xtal start up + 2^{16} xtal cycles

9.2.3 Writing of Data to Addressable Registers

When the Power Down Mode is left, the level of CLK at the rising edge of ENABLE determines the sampling edge of CLK. If CLK is low, when ENABLE rises, DATAI is sampled at the falling edge of CLK (see Figure 8 and Figure 9), if CLK is high when ENABLE rises, DATAI is sampled at the rising edge of CLK.

An Enable LOW pulse indicates the end of the WRITE command after register has been written.

Figure 8 illustrates a write command in which the initialization of DATAIO take over condition is done at the falling edge of CLK signal.

Figure 8. Writing of a Single Byte (falling edge sampling)

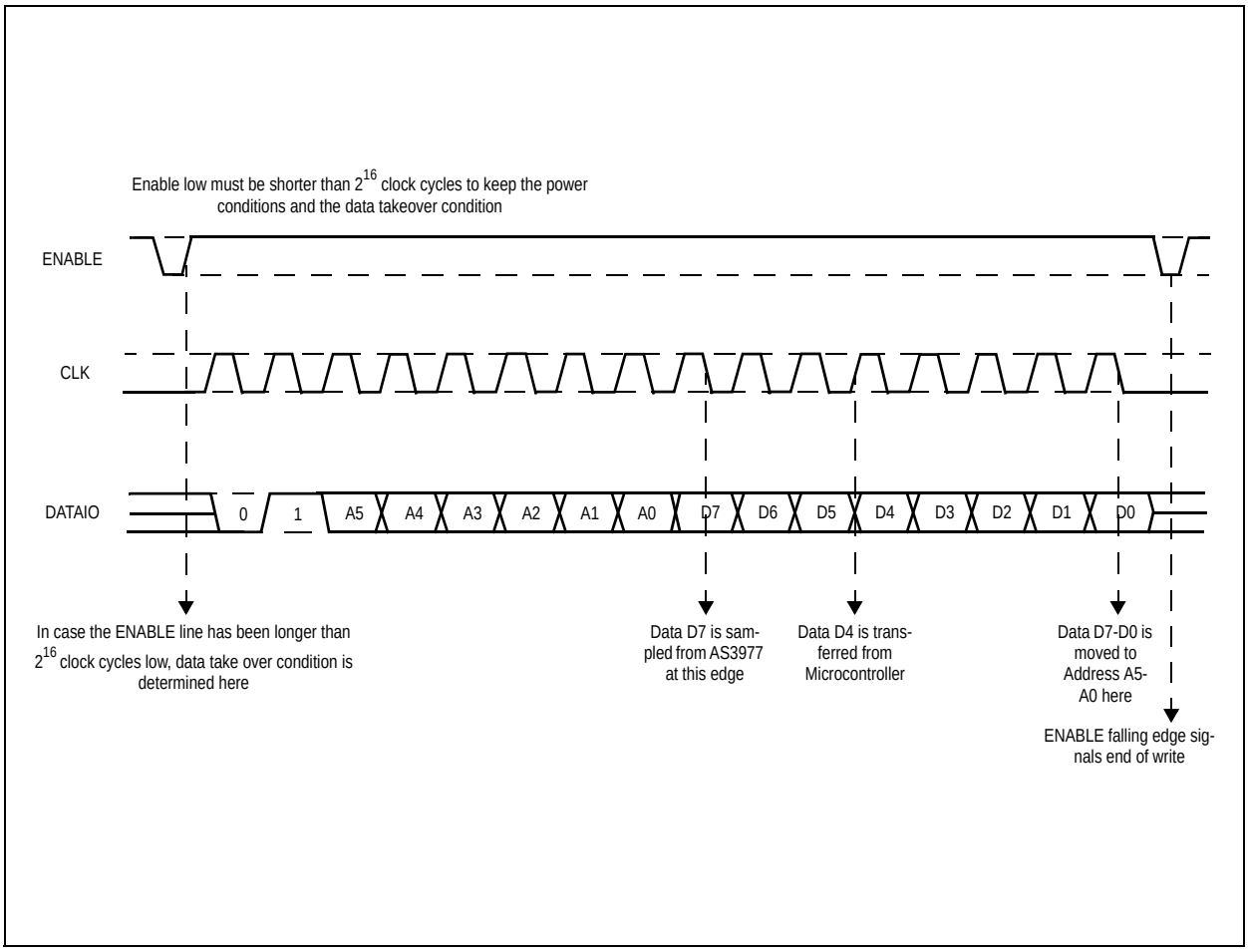
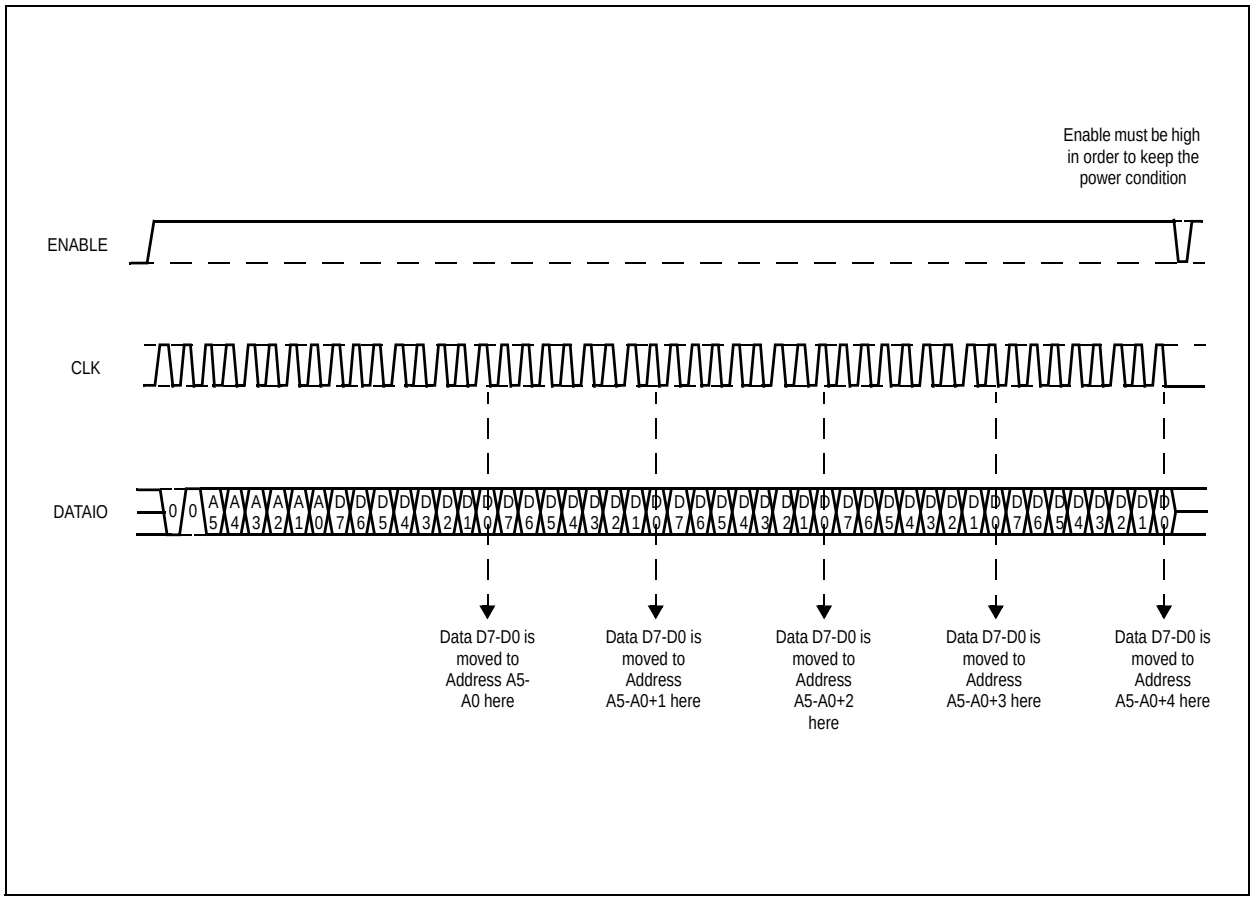


Figure 9. Writing of Data with Auto-Incrementing Address



9.2.4 Reading of Data from Addressable Registers

By leaving the Power Down Mode through a rising edge of ENABLE, the level of CLK determines the sampling edge of CLK. If CLK is low, DATAI is sampled at the falling edge of CLK (see Figure 10 and Figure 11), if CLK is high when ENABLE rises, DATAI is sampled at the rising edge of CLK. Consequently, data to be read from the microcontroller are driven by the slave (AS3977) at the transfer edge and sampled by the master (µC) at the sampling edge of CLK. An Enable LOW pulse has to be performed after register data has been transferred in order to indicate the end of the READ command and prepare the Interface to the next command control Byte.

The command control Byte for a read command consists of a command code and an address. The Command code has to be provided from least significant bit (LSB) to most significant bit (MSB), e.g. for a read it is <C0, C1> = “01”. After the command code, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SDI slave to the master, always from the MSB to the LSB. To transfer bytes from consecutive addresses, SDI master has to keep the SDI enable signal high and the SDI clock has to be active as long as data need to be read from the slave.

Each bit of the command and address sections of the frame have to be driven by the SDI master on the SDI clock transfer edge and the SDI slave samples it on the next SDI clock edge. Each bit of the data section of the frame has to be driven by the SDI slave on the SDI clock transfer edge and the SDI master on the next SDI clock edge samples it. These edges are selected on the first access after PD and they cannot be changed until next PD.

If the read access is interrupted (by de-asserting the SDI enable signal), data provided to the master is consistent to given address, but it is only the register content from MSB to LSB. If more SDI clock cycles are provided, data remains consistent and each data byte belongs to given or incremented address.

In the following figures (Figure 10 and Figure 11), two examples for a read command (without and with address self-increment) are given. The initialization base for this timing diagram is a “LOW” on the CLK line during Initialization.

Figure 10. Reading of a Single Byte (falling edge sampling)

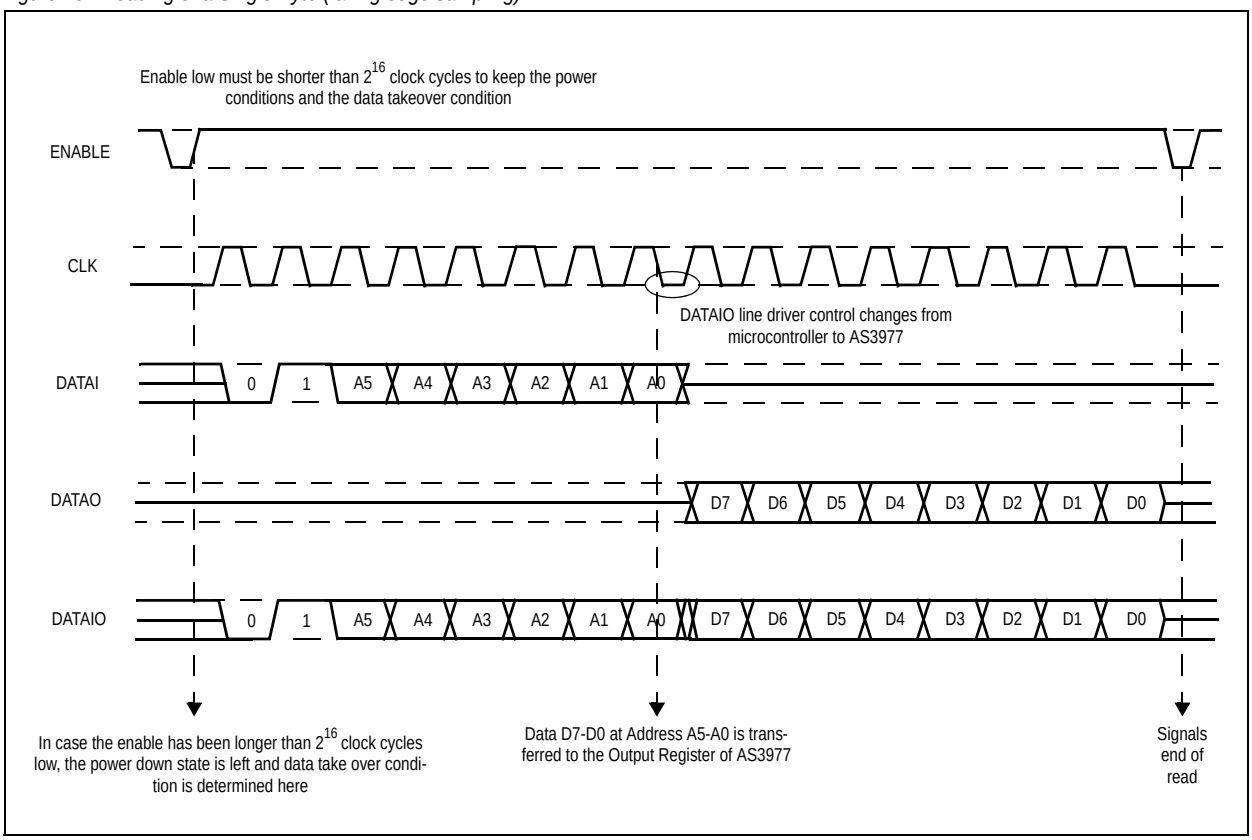
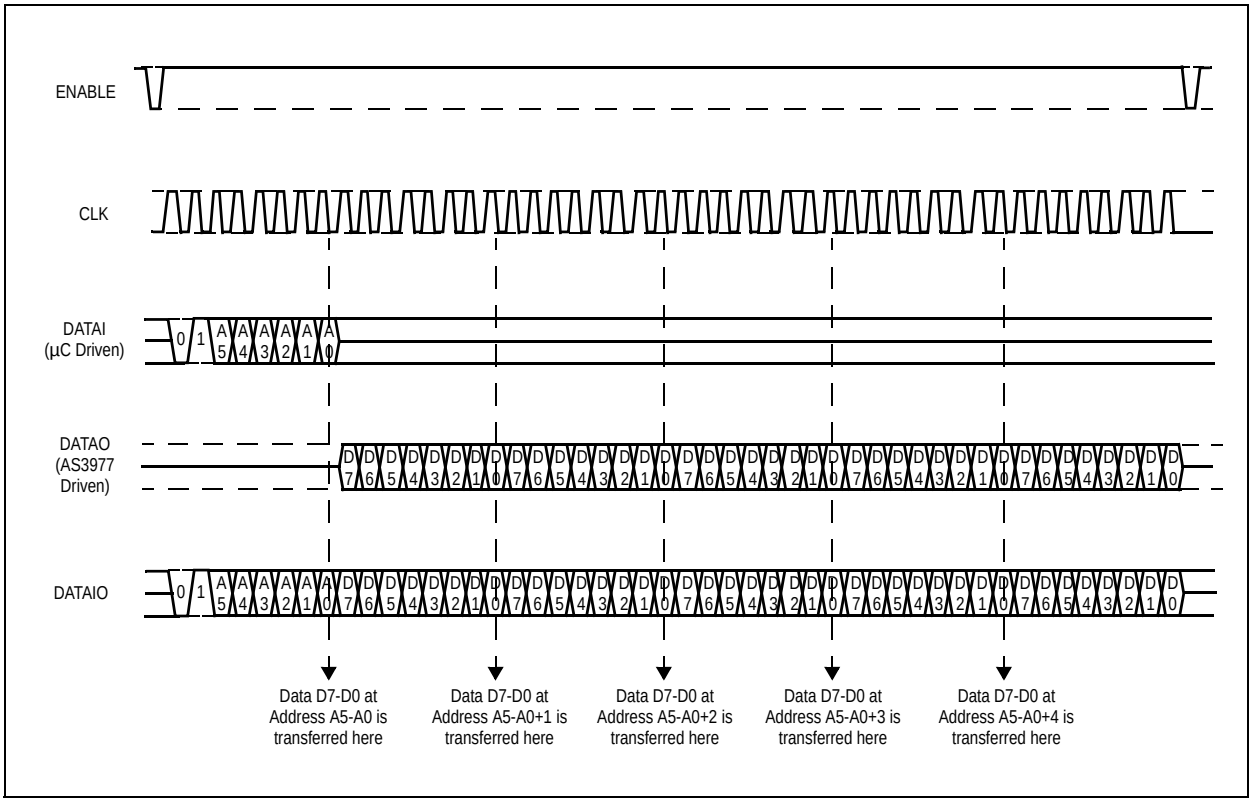


Figure 11. Reading of Data with Auto-Incrementing Address



9.2.5 Transmitting Data

Command code has to be provided from LSB to MSB and for transmit it is <C0, C1> = “11”. After the command code, further configuration has to be provided from the MSB to the LSB. Then a bit-stream, the data to be sent, can be transferred from the SDI master by keeping SDI enable signal to high. No SDI clock is required for data synchronization or the input bit stream.

Each bit of the command and address sections of the frame have to be driven by the SDI master on the SDI clock transfer edge and the SDI slave on the next SDI clock edge samples it.

The transmission starts as follows:

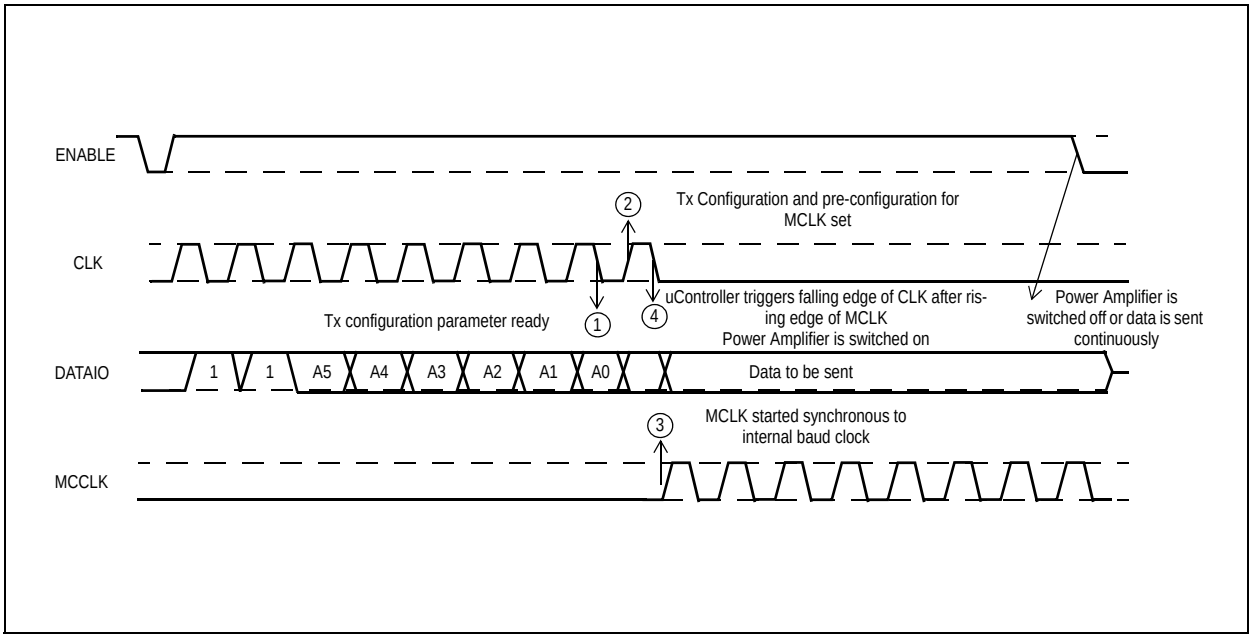
After the last configuration bit has been sampled, the micro controller has to provide an additional SDI clock edge to activate the output amplifier. This allows the SDI state machine to switch to the TX status and to activate MCCLK. Then, together with the first TX data bit, the next SDI clock sampling edge provided by the master starts the transmission itself and powers on the analog output driver.

In case, the MCCLK output is properly configured, the transmission will be stopped by the microcontroller by setting the clock to a high impedance state and the MCCLK output of the Transceiver became active and takes over the communication of the Interface.

The power amplifier is switched on (if not already on) at the subsequent sampling edge of CLK after receiving the transmit command byte. This allows to delay the PAON signal, e.g. to enable locking of the PLL in case a channel hop has to be performed.

The following figure (Figure 12) shows an example (sampling falling edge) of the transmit command with MCCLK active during TX. It is important to note in this mode the sequence of events labelled 1-4 in the diagram, which lead to transmission. This mode allows the baud clock to be synchronized to the external data. In such a case, the synchronization (A5=1) bit should be set within the transmitter configuration.

Figure 12. Transmit Command with MCCLK Active During Tx (falling edge sampling)



9.3 Transmitter Control States

9.3.1 Power Down State

When the Power Down Mode is entered, the crystal oscillator ends running and two very important bits of the registers are set to their inactive values:

1. Lock transmit: which is set (1) during PD to forbid any transmission.

2. Setpd: it is reset (0) to avoid a locked Power Down Mode.

When the circuit is in Power Down Mode, the crystal oscillator and all the other analog/digital circuits are OFF. The transmitter interface is the only supplied circuit and it is sensitive to SDI signals. The current consumption is limited by the leakage current. The configuration registers do not alter as long as the minimum supply requirements are met. The state can only be left by the rising edge of ENABLE. The state can be entered either by setting the *set power down* bit (SETPD) via. SDI communication or by setting ENABLE low for more than 2^{16} XTAL cycles (Power Down Timer). When the Power Down Mode is left (by the rising edge of ENABLE), the crystal oscillator is activated.

Software Power Down Method.

Step	Software Power Down Method
1	Set power Down Bit =1 and put ENABLE to LOW level
2	Power on reset complete with next xtal cycle

Lock Transmit Bit. When the Power Down Mode is left, the lock transmit bit (LT) is set high. The power amplifier can not be switched on as long as the bit is set to high.

State	ENABLE	LT	Description
Power Down Mode	↑	1	LT is set to High
All other states	↑	LT_{-1}	LT is unchanged except the Supply voltage drops down below the threshold level

9.3.2 Active Edge of CLK

When the Power Down Mode is left, the level of CLK at the rising edge of ENABLE determines the active edge of CLK (CLK polarity). Once the CLK polarity is set, it stays unchanged until the next Power Down Mode is re-entered.

State	ENABLE	CLK	Description
Power Down Mode	↑	0	DATAIO is sampled at the falling edge of CLK
Power Down Mode	↑	1	DATAIO is sampled at the rising edge of CLK
All other states	↑	X	CLK behavior is unchanged

9.3.3 Active State

The Active state is entered at the rising edge of ENABLE, which as well resets the Power Down timer. Possible previous states are Power Down Mode, Transmit state. DATAIO is set to SDI data input and the Interface expects a command control byte to configure the state-machine. The SDI state can be left by programming another state or by setting ENABLE low for more than 2^{16} XTAL cycles (Power Down timer).

9.3.4 Transmit State

The state is entered upon command. The transmit command byte defines in combination with the configuration registers the transmit configuration. The power amplifier (PA) will be activated on the subsequent sampling edge of CLK after receiving the command byte only if the *lock transmit bit* has been reset (0) by a previous SDI command. Here (only here) the baud rate and data generator counters are reset, i.e. if Transmit was interrupted by a SDI communication and is re-entered again (with active PA), the baud rate generator is kept synchronized with the previous transmitted string. DATAIO is set to TX data input. If during transmit a low power reset (LPR) occurs, the lock transmit bit is set high and hence the power amplifier is switched off.

The state can be left at the falling edge of ENABLE, or increasing the Supply Voltage above the threshold and setting the register bit (LT) to zero. The control of the power amplifier is determined by the command byte (bit A4 and A5).

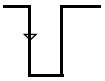
Table 20. PA Control Modes

State	LT	A4	A5	ENABLE	Description
All States	1	X	X	X	PAON low
Transmit	0	X	X	1	PAON high on the subsequent sampling edge of CLK after receiving the command byte
Transmit	0	0	0	↓	PAON low at the falling edge of ENABLE
Transmit	0	0	1	↓	PAON low at the falling edge of ENABLE but synchronized with baud rate, DATAIO is latched
Transmit	0	1	X	↓	PAON stays high, DATAIO is latched

9.4 ENABLE Signal Functionality

Figure 21 summarizes the function of ENABLE in combination with the SDI state and the logical level of CLK and DATAIO.

Table 21. ENABLE Signal Functionality

State	ENABLE	CLK	DATAIO	Description
Power Down Mode	↑	X	X	resets the SDI and state machine activates the crystal oscillator (PD is set to low) sets the lock transmit bit
		0	X	indicates data are sampled at the falling edge of CLK
		1	X	indicates data are sampled at the rising edge of CLK
		X	0	activates MCCLK, $f_{MCCLK}=f_{XOSC}/16$
		X	1	MCCLK configuration is unchanged
All	↑	X	X	resets the Power Down Timer resets the SDI Interface (re-)enters the Active state
Active, Transmit	↓	X	X	activates the Power Down Timer; after 2^{16} crystal clock cycles the IC reaches the Power Down Mode
Active, Transmit		X	X	indicates the end of Read/Write (duration: min > 1 SDI CLK cycle, max: < $1/f_{crystal} * 2^{16}$)
All	0	X	X	disables CLK and DATAIO sets DATAIO to high impedance
Transmit	↓	X	X	switches off the PA (if enabled) latches DATAIO (if enabled)

9.5 Communication and Command Byte Structure

A frame consists of a command byte including address/configuration and a following bit stream that can either represent an integer number of bytes or a random sequence of bits when the command is transmit. Command is encoded in the 2 first bits, while address is given on 6 bits. In case if the command is neither read nor write, these bits are used to configure the transmission and they will be stored until the next configuration.

The first byte of every SDI sequence is the command byte.

Function Code		Register Address or Transmission Configuration					
C0	C1	A5	A4	A3	A2	A1	A0

The function code defines the command to be performed.

C0	C1	Command		
0	0	Write data to register at address <A5…A0>		
0	1	Read data from register at address <A5…A0>		
1	0	Not defined		
1	1	Transmit data. A0…A5 defines the transmit configuration:		
		Bit	Function	Value, Description
		<A1, A0>	Frequency Selection	0 (00): selects frequency setting 1 1 (00): selects frequency setting 2 2 (10): selects frequency setting 3 3 (11): selects frequency setting 4
		A2	Power level / modulation type selection	0: selects power level / modulation type 1 1: selects power level / modulation type 2
		A3	Manchester coding	0: off 1: on
		A4	PA mode	0: PA off at the falling edge of ENABLE (synchronized with baud rate if A5 high) 1: DATAIO is latched at the falling edge of ENABLE (i.e. TX data are kept constant, PA stays on)
		A5	Data Synchronization	0: off 1: on

9.6 Transmitter Configuration Register

All configuration registers are readable and writable. The registers are arranged as addressable bytes. The first byte (A<7:0>) is addressed by 0, the consecutive bytes (A<15:8>, B<7:0>, etc.) are addressed by 1,2, etc. The configuration register settings (except the registers with default setting when entering or leaving the Power down mode), do not alter during Power down mode as long as the minimum supply requirements are met.

Table 22. Configuration Registers

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	reserved					CPSC <1:0>		CPSEC	DIVR <2:0>			ARSDRS <1:0>		ARSRST	BSEL <1:0>	
B	FRAC1<10:0>											reserved	PN9INT	reserved	SD3	reserved
C	PLLON	INT1<9:0>										FRAC1<15:11>				
D	FRAC2<15:0>															
E	FRAC3<5:0>							INT2<9:0>								
F	INT3<5:0>							FRAC3<15:6>								
G	FRAC4<11:0>												INT3<9:6>			
H	reserved		INT4<9:0>										FRAC4<15:12>			
I	DF<7:0>								GFCS<7:0>							
J	PREOP1 <0>	PAOP1 <1:0>		RPAOV1		ATCPH<3:0>				reserved		reserved			REGEN	GFBP
K	PREOP2<4:0>					PAOP2 <1:0>		RPAOV2 <1:0>		LS	LT	FSK1	PREOP1<4:1>			
L	PSC <0>	CLKS<1:0>		MCCDS <2:0>				MCCS <1:0>		reserved						FSK2
M	reserved				ASC<1:0>			TCV<7:0>							PSC<2:1>	
N	reserved							SETPD	reserved						TSRST	TSON
O	reserved					LD		TS<9:0>								

Default settings given are recommendations according to application note (not set at power up).

Table 23. Configuration Registers Description

Register	Name	Default Value	Description
Synthesizer section			
A<1:0>	SEL<1:0>	application dependent	Frequency band selection 0 (00): 315MHz frequency band 1 (01): 434 MHz and ARIB frequency band 2 (10): 868MHz frequency band 3 (11): 915MHz frequency band
A<2>	ARSRST	0	Automatic range select reset, active high

Table 23. Configuration Registers Description

Register	Name	Default Value	Description
A<4:3>	ARSDRS <1:0>	11	Automatic range select division ratio setting 0 (00): f_{REF}/64 1 (01): f_{REF}/128 2 (10): f_{REF}/256 3 (11): f_{REF}/512
A<7:5>	DIVR <2:0>	010	Reference divider division ratio setting must be set to Binary 010
A<8>	CPSEC	0	Charge pump sections setting 0: One section active 1: Two sections active
A<10:9>	CPCS <1:0>	application dependent	Charge pump current setting 0 (00): 12.5 µA/Section 1 (01): 25.0 µA/Section 2 (10): 37.5 µA/Section 3 (11): 50.0 µA/Section
A<11:15>		00000	reserved Bits: set to Binary 00000 for normal mode of operation
B<0>		0	0: normal mode of operation 1: reserved for test purposes only
B<1>	SD3	1	ΣΔ order selection 0: MASH2 1: MASH3
B<2>		0	0: reserved Bit; set to zero
B<3>	PN9INT	0	0: normal mode 1: reserved for test purposes only
B<4>		0	0: normal mode 1: reserved for test purposes only
B<15:5>	FRAC1 <15:0>	application dependent	Synthesizer fractional setting 1
C<4:0>			
C<14:5>	INT1<9:0>	application dependent	Synthesizer integer setting 1
C<15>	PLLON	1	0: Phase locked loop off 1: Phase locked loop on
D<15:0>	FRAC2 <15:0>	application dependent	Synthesizer fractional setting 2
E<9:0>	INT2<9:0>	application dependent	Synthesizer integer setting 2
E<15:10>	FRAC3 <15:0>	application dependent	Synthesizer fractional setting 3
F<9:0>			
F<15:10>	INT3<9:0>	application dependent	Synthesizer integer setting 3
G<3:0>			
G<15:4>	FRAC4 <15:0>	application dependent	Synthesizer fractional setting 4
H<3:0>			
H<13:4>	INT4<9:0>	application dependent	Synthesizer integer setting 4
H<15:14>		00	reserved Bits: set to Binary 00 for normal mode of operation

Table 23. Configuration Registers Description

Register	Name	Default Value	Description
Modulation and Power Amplifier section			
I<7:0>	GFCS <7:0>	application dependent	Gaussian filter clock setting
I<15:8>	DF<7:0>	application dependent	FSK deviation setting
J<0>	GFBP	0	Gaussian filter bypass 0: not bypassed 1: bypassed
J<1>	REGEN	1	0: Turn off the VDD RF Regulator 1: Turn on the VDD RF Regulator
J<5:2>	-	0000	reserved Bits: set to Binary 0000 for normal mode of operation
J<6>	reserved	0	reserved Bit should be set to 0
J<10:7>	ATCPH <3:0>	0000	Antenna tuning circuit phase shift setting 0 (0000): minimum capacitor : : 15 (1111): maximum capacitor
J<12:11>	RPAOV1 <1:0>	11	PA voltage regulator setting 1 0 (00): VREG=1.7V 1 (01): VREG=1.8V 2 (10): VREG=1.9V 3 (11): VREG=2.0V
J<14:13>	PAOP1 <1:0>	application dependent	Power amplifier power level setting 1 0 (00): maximum power : 3 (11): minimum power
J<15>	PREOP1 <4:0>	application dependent	Preamplifier power level setting 1 0 (00000): power off 1 (00001): minimum power : 31 (11111): maximum power
K<3:0>			
K<4>	FSK1	0	Modulation type selection 1 0: FSK 1: reserved for test purposes only
K<5>	LT	0	Lock transmit, active=high
K<6>	LS	0	Low power supply indicator, active=high
K<8:7>	RPAOV2 <1:0>	11	PA voltage regulator setting 2 0 (00): VREG=1.7V 1 (01): VREG=1.8V 2 (10): VREG=1.9V 3 (11): VREG=2.0V
K<10:9>	PAOP2 <1:0>	application dependent	Power amplifier power level setting 2 0 (00): maximum power : 3 (11): minimum power

Table 23. Configuration Registers Description

Register	Name	Default Value	Description
K<15:11>	PREOP2 <4:0>	application dependent	Preamplifier power level setting 2 0 (00000): power off 0 (00001): minimum power : 31 (11111): maximum power
L<0>	FSK2	0	Modulation type selection 2 0: FSK 1: reserved for test purposes only
L<7:1>	-	0000000	reserved Bits: set to Binary 0000000 for normal mode of operation
Baud Rate Generator, Data Generator and Digital Test Multiplexer section			
L<9:8>	MCCS <1:0>	11	Micro controller clock output 0 (00): reserved 1 (01): reserved 2 (10): Micro controller clock is on during transmit (MCCLK is output) 3 (11): Micro controller clock is always on (MCCLK is output)
L<12:10>	MCCDS <2:0>	application dependent	Clock output driver driving strength setting 0 (000): 4mA (maximum) driving strength … 7 (111): 1mA (minimum) driving strength
L<14:13>	CLKS<1:0>	application dependent	MCCLK source selection 0 (00): MCCLK connected to pre scaler output 1 (01): MCCLK connected to baud rate generator output 2 (10): MCCLK connected to baud rate generator output but inverted 3 (11): not used
L<15> M<1:0>	PSC<2:0>	application dependent	Micro controller clock pre scaler division ratio $f_{OUT}=2^{-PSC<2:0>}*f_{IN}$
M<9:2>	TCV<7:0>	application dependent	Baud rate generator counter value
M<11:10>	ASC<1:0>	application dependent	Baud rate generator after scaler division ratio $f_{OUT}=2^{-ASC<1:0>}*f_{IN}$
M<15:12>	reserved	0010	reserved Bits: set to Binary 0010 for normal mode of operation
Temperature Sensor section			
N<0>	TSON	0	0: Temperature sensor off 1: Temperature sensor on
N<1>	TSNRST	1	Reset of temperature sensor, active=low
N<7:2>	-	0000000	reserved Bits: set to Binary 0000000 for normal mode of operation
Power Down Control (see Power On Reset on page 22)			
N<8>	SETPD	0	Set power down, active=high (see Power On Reset on page 22)

Table 23. Configuration Registers Description

Register	Name	Default Value	Description
N<15:9>	-	0000000	reserved Bits: set to Binary 0000000 for normal mode of operation
Temperature Sensor and Lock Detector Output (read only)			
O<9:0>	TS<9:0>	-	Temperature sensor output
O<10>	LD	-	Lock detector output
O<15:11>	-	-	reserved

9.7 Special Bits

The following paragraphs provide a brief description of special bits used for Transmitter Interface functionality.

9.7.1 LT (Lock Transmit)

The Lock Transmit bit will be set each time the circuit goes in Power Down Mode. When the bit is set, the power amplifier of the AS3977 cannot be activated. TX commands will be anyway accepted but without any “external” and visible effect.

A low has to be written before starting any RF-Transmission. The first write command can be responsible for a wake up event of the circuit and to release Power Down Mode, which will lead to the inactive state. This signal will be activated whenever the power supply is dramatically under the threshold for safe workings of analog circuits during transmit operations. If the supply voltage is under the threshold during transmit, the read back value is “1” and this can indicate a non finished transmission.

9.7.2 LS (Low Power Supply Voltage)

Low power Supply voltage (LS) is a read/write bit, which indicates that the power amplifier supply voltage level (VCCPA) is below a certain threshold voltage (see Table 13). After an increase of the power supply voltage above the threshold level (plus a hysteresis), this bit has to be reset to zero via SPI. The bit condition has no influence on the operation of the IC. LS and LT monitor the VCCPA supply (they are only working if Voltage is applied to VCCPA). As they are working with the same VREF generator that will be supplied from VCCPA, an overlap of the threshold levels will never occur. LS is an indicator whereby LT switches off the PA hard coded.

9.7.3 MCCS, CLKS and PSC

These bits are used to set the micro controller clock functionality and to control the associated MCCLK bi-directional and multi-functional pad.

MCCS stands for Micro Controller Clock output Selection and it declares how the MCCLK pad will be used. Depending on the level of DATAIO by leaving the Power Down Mode, this setting can be left unchanged from the last written value (DATAIO=1) or it can be set to the default value (DATAIO=0). Default MCCS value is “11” then the MCCLK pad is used as output and the clock is always active.

CLKS stands for Clock Selection and it is used to select as MCCLK pre-scaler or baud rate output. Default value is the pre-scaler output.

PSC stands for Pre-scaler and it is the two’s exponent for first crystal oscillator division ratio. Default value is “100” that means a division ratio of $2^4 = 16$.

By leaving the Power Down Mode and if DATAIO is sampled LOW, these bits are set to their default values and then as soon as the crystal oscillator is on, the MCCLK will be active and with a frequency that is 1/16 of the crystal oscillator working frequency.

9.7.4 SETPD (Set Power Down)

This bit is used to force the circuit to go in Power Down Mode (see Software Power Down Method on page 26). When the circuit is in Power Down Mode, this bit is reset to ZERO to avoid a dead lock condition. The Power Down Mode can be reached by writing a ONE to this bit whenever a fast transition to the Power Down Mode is needed.

9.8 Output Frequency Setting

The output frequency f_{RF} is given by:

$$f_{RF} = P \cdot f_{REF} \cdot (M \cdot N + AC + FRAC) \quad \text{(EQ 3)}$$

Where:

P is the Predivider division ratio
f_{REF} is the Reference frequency
M is the Prescaler modulus
N is the N-counter division ratio
AC is the A-counter offset, AC determines together with FRAC the actual A-counter setting
FRAC is the Fractional part

Predivider Division Ratio P and Pre Scaler Modulus M. The frequency band selection determines the value of the predivider division ratio P and the setting of the pre scaler modulus M. The setting of these values for the different frequency bands is given in Table 24.

Table 24. P and M Values for Frequency Bands

Frequency Band	P	M	BSEL<1:0>	Note
315 MHz	1	4	0 (00)	300 – 320 MHz
433 MHz	1	5	1 (01)	425 – 450 MHz
868 MHz	2	5	2 (10)	865 – 870 MHz
915 MHz	2	5	3 (11)	902 – 928 MHz

The reference frequency should be in the range of 3 to 5, 75 MHz and can be calculated by:

$$f_{REF} = \frac{f_{XTAL}}{divider} \quad \text{(EQ 4)}$$

The recommended setting of the divider is 4.

The next step is to calculate the Division ratio:

$$DR = \frac{f_{RF}}{P \cdot f_{REF}} = DR_{INT} + DR_{FRAC} \quad \text{(EQ 5)}$$

This division ration can be split into a part before the comma, called integer part and a part after the comma, also called fractional part DR_{FRAC}

The N-counter value of the Fractional N Synthesizer can be calculated with the formula:

$$N = \text{whole numbered part of } \frac{(DR_{INT} - 3)}{M} \quad \text{(EQ 6)}$$

The A-Counter is the rest of this Division and can be calculated by:

$$AC = (DR_{INT} - 3) - N \times M \quad \text{(EQ 7)}$$

In case, the Value of the A-counter is zero, the value of the A-counter has to be increased by M and the value of N has to be decreased by one

$$AC = M$$
$$N = N - 1 \quad \text{(EQ 8)}$$

In case, the N-counter is in the range from 10 to 25 and the value of the A-counter is less than N-counter-7:

$$INT<3:0> = N - 10$$
$$INT<7:4> = AC - 1 \quad \text{(EQ 9)}$$

Note: In case, no solution can be found for the wanted center frequency, it may help to modify the reference frequency or INT<8>

9.8.1 Implementation

Starting from the equation,

$$f_{RF} = P \cdot f_{REF} \cdot (M \cdot N + AC + FRAC) \quad \text{(EQ 10)}$$

The equation now rewritten by taking configuration registers and implementation details into account:

(EQ 11)

$$f_{RF} = P\frac{f_{XTAL}}{DIVR<2:0>+2}\left((INT<9>+4)(INT<3:0>+INT<8>\cdot 6+10)+INT<7:4>+1+(INT<8>+1)\left(3+\frac{FRAC<15:0>}{2^{16}}\right)\right)$$

Reference frequency f_{REF} (DIVR<2:0>)

The reference frequency f_{REF} is determined by the crystal frequency f_{XTAL} and the reference divider division ratio setting DIVR<2:0> and can be calculated with the help of:

(EQ 12)

$$f_{REF} = \frac{f_{XTAL}}{DIVR<2:0>+2}$$

The value of f_{REF} should be in the range of 3 MHz to 5, 75 MHz to achieve an optimum on noise performance and current consumption

$$DIVR<2:0> = \frac{f_{XTAL}}{f_{REF}} - 2 \quad \text{(EQ 13)}$$

9.8.1.1 M-counter and Value of INT<9>

The value of the M-counter is given by:

$$M = (INT<9>+4) \quad \text{(EQ 14)}$$

The Bit INT<9> can be calculated as,

INT < 9 > = M - 4

9.8.1.2 N-counter and Value of INT<3:0>

$$N = (INT<3:0>+INT<8>.6+10) \quad \text{(EQ 15)}$$

Taken the default value of INT<8>=0 into account, the value of the INT3<..0> can be calculated by:

INT < 3:0 > = N-10

9.8.1.3 A- Counter and Value of INT<7:4>

$$AC = INT<7:4>+1+(INT<8>+1) \times 3 \quad \text{(EQ 16)}$$

Taken the default value of INT<8>=0 into account, the value of the INT<7:40> can be calculated by:

INT < 7:4 > = AC-1

9.8.1.4 Fractional Part and Values of FRAC<15:0>

(EQ 17)

$$DR_{FRAC} = (INT<8>+1)\left(\frac{FRAC<15:0>}{2^{16}}\right)$$

Taken the default value of INT<8>=0 into account, multiplying the Fractional part with 2^{16} gives the register values for the Fractional and synthesizer value and can be calculated by:

FRAC < 15:0 >= DR_{FRAC} x 2^{16}

Example:

Wanted frequency 425 MHz by 16 MHz crystal frequency.

The values of P and M can be taken from table

P=1→ Defined with the BSEL Bit's BSEL<1:0>= Hex "2"

M=5 → INT<9>= 5-4 = 1

The Setting of DIVR<2:0> = 2 results in a reference frequency divider of 4.

The Division ratio will now be:

$$DR = \frac{f_{RF}}{P \cdot f_{REF}} = \frac{433,92_R}{1.4} = 108,48 = DR_{INT} + DR_{FRAC} \qquad \textit{(EQ 18)}$$

And can be split into the values:

$$N = \textit{whole numbered part of } \frac{(DR_{INT} - 3)}{M} = \frac{(108 - 3)}{5} = 21 \qquad \textit{(EQ 19)}$$

As the Rest is zero, we have to set AC=M and N to decrease by one.

N=20

INT < 3:0 >= N-10 = 20-10=10 = Hex „A"

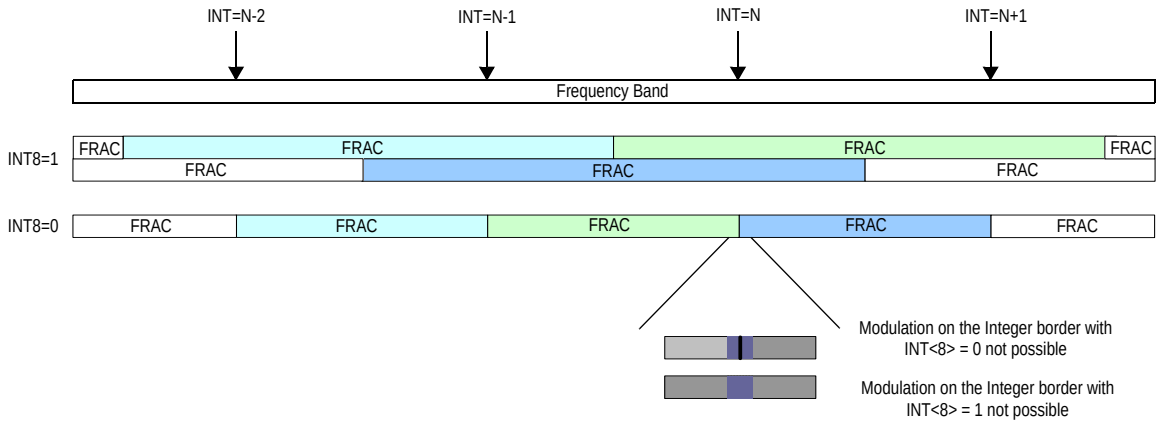
AC=5

INT < 7:4 >= AC-1= 5-1=4 Hex „4"

FRAC < 15:0 >= DR_{FRAC} x 2^{16} = 0,48 x 65536 = 31457 =Hex "7AE1"

9.8.2 Optional Frequency Calculation with Overlapping Fractional Bands by Using the Bit INT<8>

Bit INT<8>. The bit INT<8> is a multiplier to the output of the ΣΔ-modulator. Set this Bit to high stretches the fractional-N region by two and results in overlapping frequency bands with a bandwidth of 2*f_{REF} and an overlap ratio of 50% in order to allow frequency modulation and/or frequency trimming independently on the required output frequency and selected crystal. Note that setting INT<8> high increases the PLL in-band noise by approximately 3dB. Therefore it is recommended to use this option only if the required frequency band did not fit to the crystal reference.



Steps for INT<8>=1

Calculate the Division ratio

$$DR = \frac{f_{RF}}{P \cdot f_{REF}} = DR_{INT} + DR_{FRAC} \quad \text{(EQ 20)}$$

1. If the fractional part is larger than 0.5

$$FRAC\ <15:0> = DR_{FRAC} \cdot 2^{15}$$

$$N = \text{whole numbered part of } \frac{(DR_{INT} - 6)}{M} \quad \text{(EQ 21)}$$

The A-Counter is the rest of the Division and can be calculated by:

$$AC = (DR_{INT} - 6) - N \times M \quad \text{(EQ 22)}$$

2. If the fractional part is less than 0.5

$$FRAC\ <15:0> = (DR_{FRAC} + 1) \cdot 2^{15}$$

$$N = \text{whole numbered part of } \frac{DR_{INT} - 7}{M} \quad \text{(EQ 23)}$$

The A-Counter is the rest of the Division and can be calculated by:

$$AC = (DR_{INT} - 7) - N \times M \quad \text{(EQ 24)}$$

In case, the value of the A-counter is zero, the value of the A-counter has to be increased by M and the value of N has to be decreased by one

$$AC = AC + M$$
$$N = N - 1 \quad \text{(EQ 25)}$$

In case, the N-counter is in the range from 16 to 31 and the value of the A-counter is less than N-counter-14:

$$INT\ <3:0> = N - 16$$
$$INT\ <7:4> = AC - 1 \quad \text{(EQ 26)}$$

Note: In case, no solution can be found for the wanted center frequency, it may help to modify the reference frequency or INT<8>.

9.8.3 FSK Deviation Setting and Frequency Trimming

The frequency resolution Δf is determined by the reference frequency f_{REF}, the selected frequency band and the setting of INT<8> and can be calculated with following equation:

$$\Delta f = P \cdot (INT\ <8> + 1) \cdot \frac{f_{REF}}{2^{16}} \quad \text{(EQ 27)}$$

9.8.3.1 FSK Deviation Setting

The FSK deviation DF is given by the frequency resolution Δf and the setting of DF<7:0> and can be calculated with the help of:

$$DF = \Delta f \cdot DF\ <5:0> \,.\, DM \quad \text{(EQ 28)}$$

The deviation multiplier DM is determined by the setting of DF<7:6> according to the following table:

DF<7:6>	DM
0 (00)	1
1 (01)	2
2 (10)	4
3 (11)	16

Frequency Trimming. Frequency trimming (e.g. in case a characterized crystal is used) can be done with the help of the (nominal) frequency resolution Δf and without recalculating all the frequency settings. If the crystal error is known, the resulting error ε_{RF} in the output frequency is also known. The ratio $\frac{|\varepsilon_{RF}|}{\Delta f}$ can then be used to correct the error. In case the crystal error is positive, $\frac{|\varepsilon_{RF}|}{\Delta f}$ has to be subtracted from, in case the crystal error is negative it has to be added to FRAC<15:0>.

A similar procedure can be performed to calibrate for initial frequency errors. Note that in both cases the resulting value for FRAC<15:0> has to fulfil the conditions FRAC<15:0> - DF ≥ 0H and FRAC<15:0> + DF ≤ FFFFH.

9.8.3.2 Gaussian Filter Clock Setting

The setting of GFCS<7:0> determines the clock frequency f_{GF} of the Gaussian filter according to

(EQ 29)

$$f_{GF} = \frac{f_{REF}}{GFCS<7:0> + 1}$$

Ideally, f_{GF} should be set to be 30*f_{Mod} (f_{Mod} ...modulation frequency).

9.9 Baud Rate Generator

The main functionality of the module is to generate clocks with programmed periods. The first action is to change the parameters followed by starting a transmission.

- Changing PSC, TCV, ASC and CLKS parameters
  As soon as the crystal oscillator clock is active, pre scaler and after scaler timer configuration parameters are continuously updated from the SDI registers. To avoid spurious emissions, these synchronized values cannot be immediately used for new clock generation because the circuit has to take care about current and new clock phase difference. Then, as soon as the phase difference between them is zero, an enable signal is generated and new values are stored to the final registers that will be used for the normal functionality of the circuit. At this point the new clock will start without spurious periods.
- Starting a transmission
  A typical situation is as follows – After start up and configuration, the circuit goes in Power Down Mode. Then a wake up event occurs on the SDI interface and the internal crystal oscillator starts running (after a setup time). The wake up event is typically a rising edge on the SDI enable input that samples the SDI data e.g. to the LOW value and this resets the MCCLK frequency to be 1/16 of the oscillator frequency and makes the clock always active. At this point the micro-controller starts its activity and it can decide to reprogram MCCLK frequency to the desired value and to the desired behavior. The decision between current and new value will be done synchronously to eliminate any possible spurious period on MCCLK (mainly if it is used). In any case it can be maintained the new setting between different Power Down Modes or it can be reset to the default value on the first access to the SDI interface when the circuit is in Power Down Mode.

9.10 Reference Design PREOUT and PAOUT Connection

For all RF Specification, refer to the Reference Design. The PAOUT pin is Power Line matched to 50Ω load wherein a power of 8dBm@315MHz/433MHz and 4dBm@868MHz/915MHz is spent typically.

9.10.1 Matching Circuit and PREOUT and PAOUT Connections to the Supply Voltage

Figure 13 shows the Power Line Matching and Transformation Network used on the Reference Design. Table 25 gives the values for several settings, varying the operation frequency and the Supply Voltage source. Supply blocking capacitors are not shown in the schematic (see Figure 13).

Figure 13. Schematic

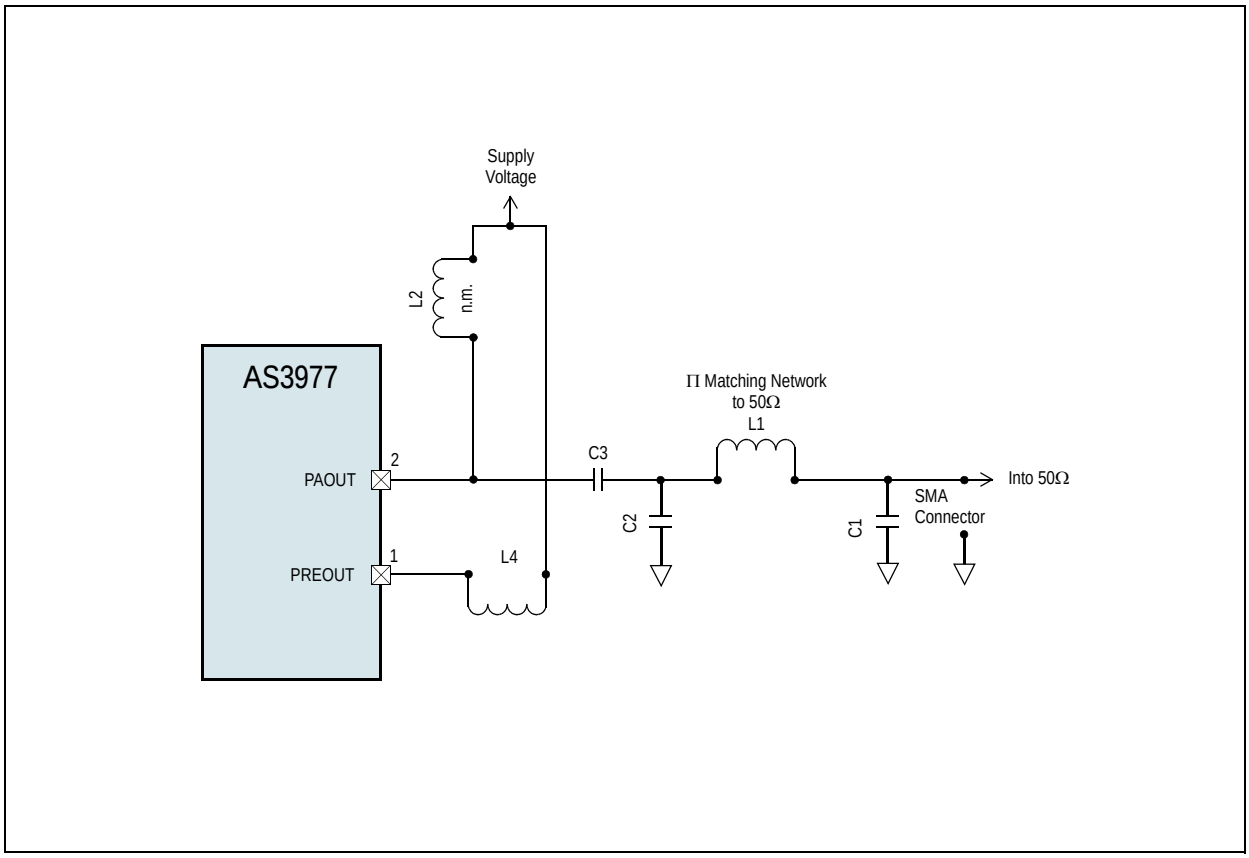


Table 25. Part List of the Reference Design Components

Supply voltage 2V regulated Source is VREGRF (pin 16)			Supply voltage 3V Source is Power Supply		
315 MHz			315 MHz		
Component	Value	Type	Component	Value	Type
L4	47 nH	Murata-LQW18AN47NG00	L4	43 nH	Murata-LQW18AN43NG00
L2	62 nH	Murata-LQW18AN62NG00	L2	62 nH	Murata-LQW18AN62NG00
C3	10 pF	Murata-GRM1885C1H100JA01	C3	100 pF	Murata-GRM1885C1H101JA01
C2	2.7 pF	Murata-GRM1885C1H2R7CZ01	C2	3.3 pF	Murata-GRM1885C1H3R3CZ01
L1	56 nH	Murata-LQW18AN56NG00	L1	82 nH	Murata-LQW18AN82NG00
C1	0.5 pF	Murata-GRM1885C1HR50CZ01	C1	4.7 pF	Murata-GRM1885C1H4R7CZ01
433 MHz			433 MHz		
L4	24 nH	Murata-LQW18AN24NG00	L4	24 nH	Murata-LQW18AN24NG00
L2	33 nH	Murata-LQW18AN33NG00	L2	33 nH	Murata-LQW18AN33NG00
C3	10 pF	Murata-GRM1885C1H100JA01	C3	100 pF	Murata-GRM1885C1H101JA01
C2	2.2 pF	Murata-GRM1885C1H2R2CZ01	C2	3.9 pF	Murata-GRM1885C1H3R9CZ01
L1	43 nH	Murata-LQW18AN43NG00	L1	43 nH	Murata-LQW18AN43NG00
C1	2.7 pF	Murata-GRM1885C1H2R7CZ01	C1	6.8 pF	Murata-GRM1885C1H6R8CZ01

Table 25. Part List of the Reference Design Components

Supply voltage 2V regulated Source is VREGRF (pin 16)			Supply voltage 3V Source is Power Supply		
868/915 MHz			868/915 MHz		
L4	8.2 nH	Toko-LL1608-FS	L4	8.2 nH	Toko-LL1608-FS
L2	8.2 nH	Toko-LL1608-FS	L2	8.2 nH	Toko-LL1608-FS
C3	10 pF	Murata-GRM1885C1H100JA01	C3	10 pF	Murata-GRM1885C1H100JA01
C2	1.0 pF	Murata-GRM1885C1H1R0CZ01	C2	1.0 pF	Murata-GRM1885C1H1R0CZ01
L1	10 nH	Murata-LQW18AN10NG00	L1	10 nH	Murata-LQW18AN10NG00
C1	2.2 pF	Murata-GRM1885C1H2R2CZ01	C1	2.2 pF	Murata-GRM1885C1H2R2CZ01

10 Measurement Results

Figure 14. Output spectrum with 7.5MHz span, Frequency=433.92MHz, POUT=8dBm (0.3dBm added due to cable attenuation), Span=7.5MHz

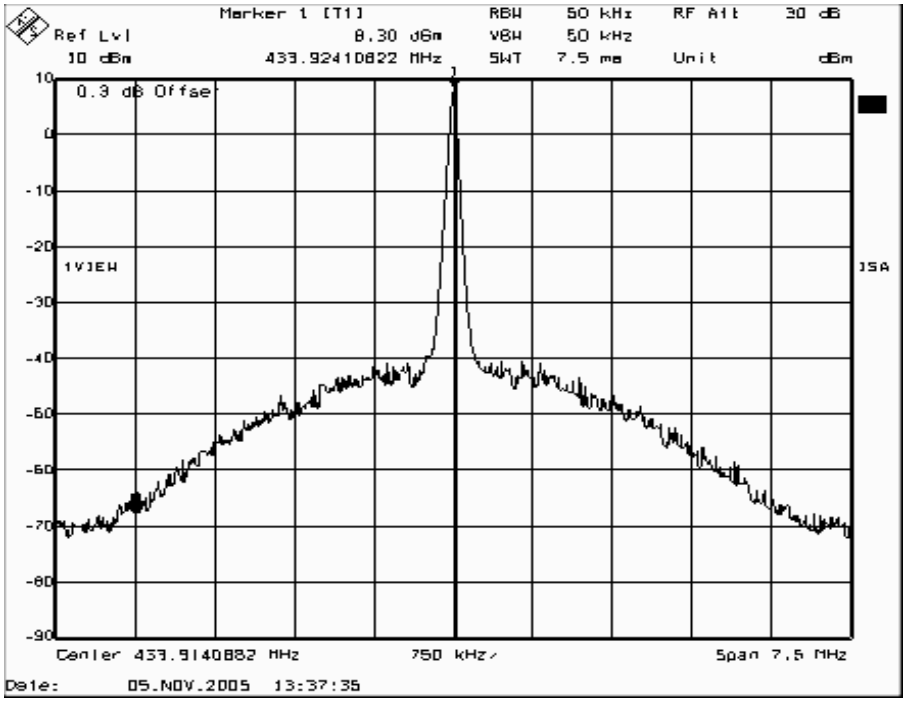


Figure 15. Phase-noise: - 88.5dBc, POUT=8dBm

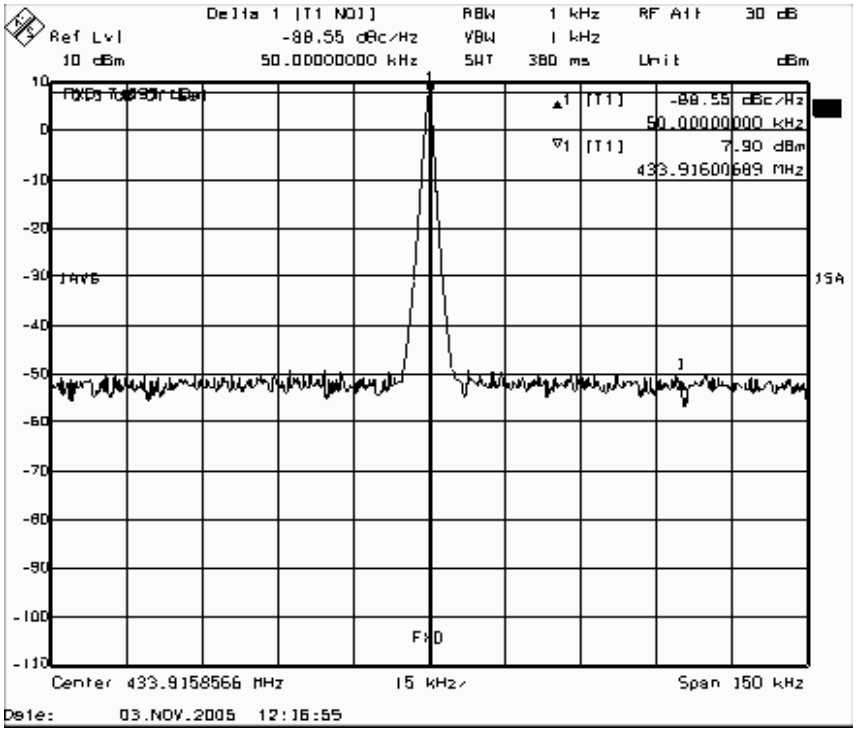


Figure 16. Modulated signal with bypass gaussian filter, Freq Mod: 5kHz, Deviation: 10kHz

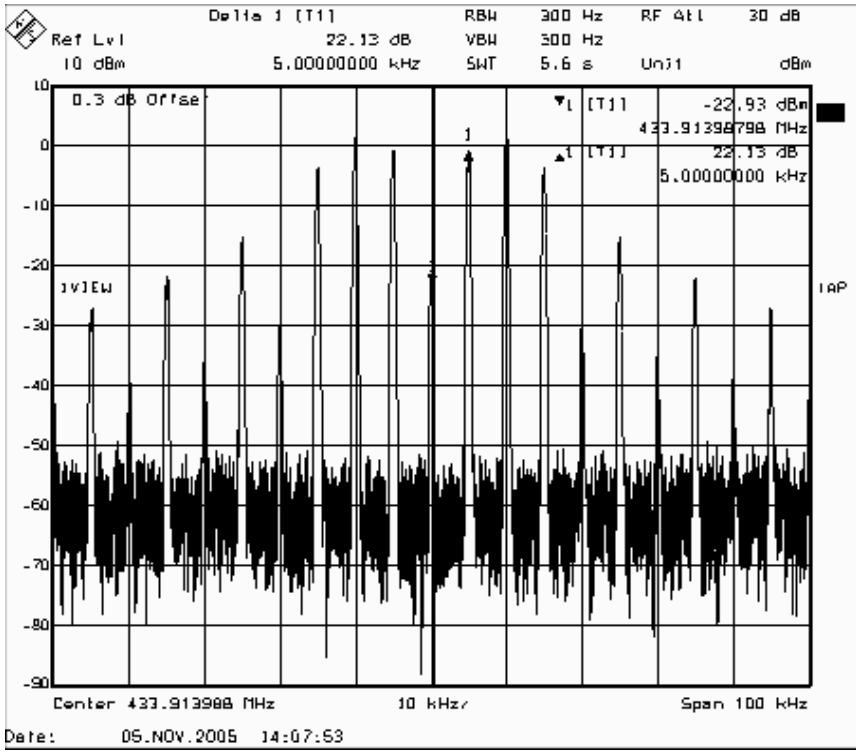


Figure 17. Modulated signal with gaussian filter, Freq Mod: 5kHz, Deviation: 10kHz

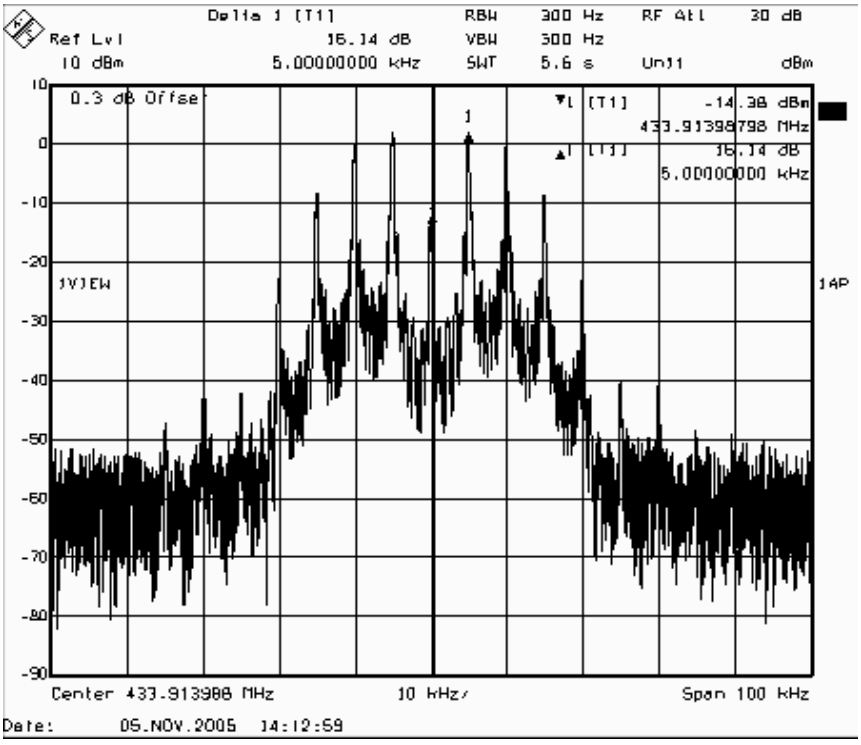


Figure 18. Occupied bandwidth with bypass gaussian filter, Occupied bandwidth: 49.7kHz, Freq Mod: 5kHz, Deviation: 10kHz

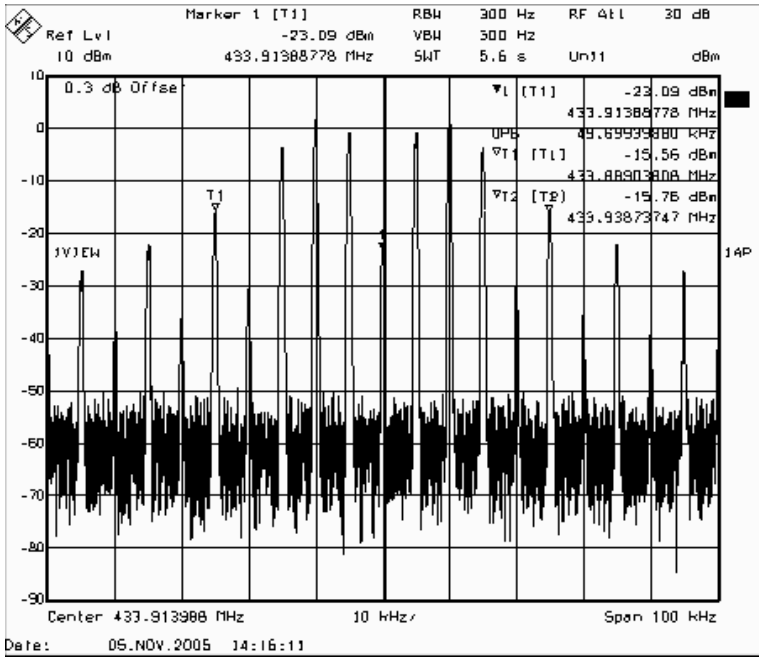
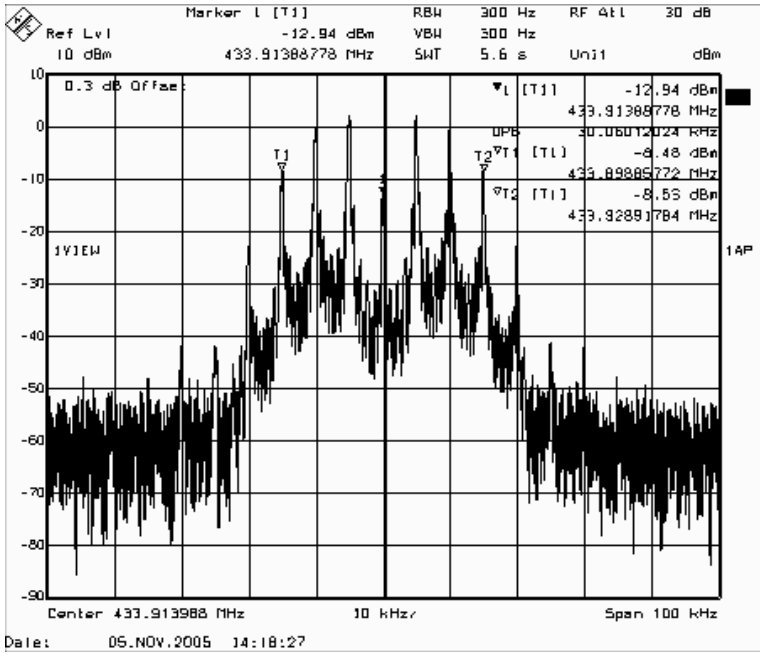


Figure 19. Occupied bandwidth with gaussian filter, Occupied bandwidth: 30kHz, Freq Mod: 5kHz, Deviation: 10kHz



10.0.1 Applicable Radio Standards

- ARIB STD-T67 (Telemeter, Telecontrol and Data-Transmission Radio Equipment)
- ETSI EN 300 220
- FCC CFR 47 Part 15

11 Package Drawings and Markings

The device is available in a 16-Lead QFN (4x4mm) package.

Figure 20. Package Drawings

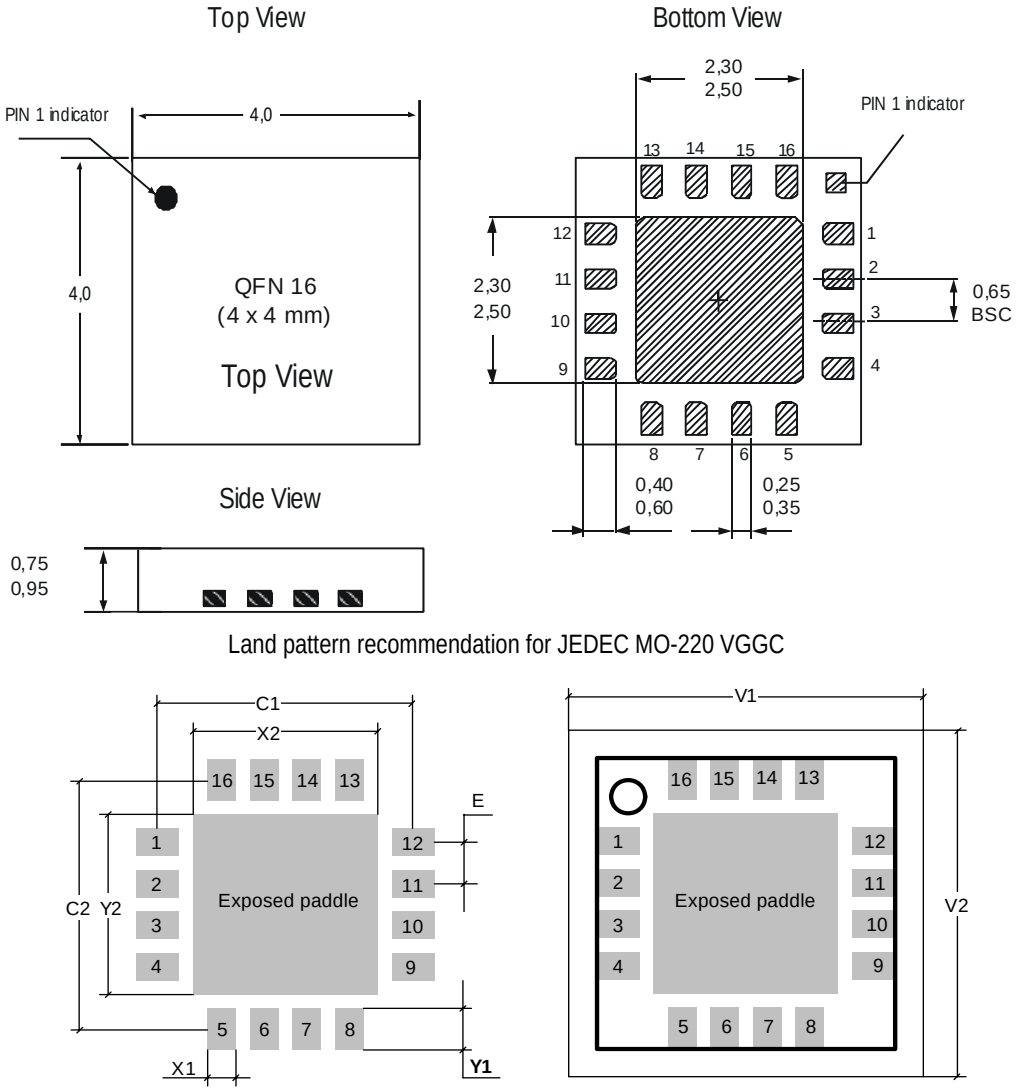


Table 26. Package Dimensions

Symbol	mm
Pitch E	0.65
Pad X1	0.35
Pad Y1	0.9
Pad Space C1	3.9
Pad space C2	3.9
Tab pad X2	2.4
Tab pad Y2	2.4
Courtyard V1	5.3
Courtyard V2	5.3

Revision History

Revision	Date	Owner	Description
3.4	Apr 01, 2008		
3.5	Dec 15, 2008	kfr/tjs	Added block diagram Operation Mode Relations (page 20) Updated Ordering Information (page 46)
3.6	Apr 16, 2010		Updated Ordering Information (page 46)

Note: Typos may not be explicitly mentioned under revision history.

12 Ordering Information

The devices are available as the standard products shown in Table 27.

Table 27. Ordering Information

Device ID	Part Number	Description	Delivery Form[1]	Package
AS3977-TPD	AS3977B-BQFS		Tray	QFN16 4x4
	AS3977B-BQFT		Tape and Reel	QFN16 4x4

1. Dry Pack sensitivity Level =3 according IPC/JEDEC J-STD-033A.

Where:
T=Temperature range:
B=-40...85 degree
P=Package Type:
QF=QFN
D=Delivery Form
S=Tray in DryPack
T=Tape and Reel

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

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