

AS5013

Low Power Integrated Hall IC for Human Interface Applications

General Description

The AS5013 is a complete Hall Sensor IC for smart navigation key applications to meet the low power requirements and host SW integration challenges for products such as cell phones and smart handheld devices.

Due to the on chip processing engine, system designers are not tasked with integrating complex SW algorithms on their host processor thus leading to rapid development cycles.

The AS5013 single-chip IC includes 5 integrated Hall sensing elements for detecting up to ± 2 mm lateral displacement, high resolution ADC, XY coordinate and motion detection engine combined with a smart power management controller.

The X and Y positions coordinates and magnetic field information for each Hall sensor element is transmitted over a 2-wire I²C compliant interface to the host processor.

The AS5013 is available in a small 16-pin 4mmx4mmx0.55mm QFN package and specified over an operating temperature of -20°C to 80°C

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5013, Low Power Integrated Hall IC for Human Interface Applications are listed below:

Figure 1:
Added Value of Using AS5013

| Benefits | Features |
|---|---|
| <ul style="list-style-type: none"> Lateral magnet movement radius up to 2mm | <ul style="list-style-type: none"> 8-bit resolution in X and Y direction |
| <ul style="list-style-type: none"> Fast and simple interface integration | <ul style="list-style-type: none"> High-speed I²C interface |
| <ul style="list-style-type: none"> Automatic low-power-mode | <ul style="list-style-type: none"> 3μA current consumption in stand by |
| <ul style="list-style-type: none"> Low operating voltage supply | <ul style="list-style-type: none"> 2.7V to 3.6V operating voltage - Down to 1.7V peripheral supply voltage |
| <ul style="list-style-type: none"> Contactless push-button possible | <ul style="list-style-type: none"> 12-bit raw hall output |
| <ul style="list-style-type: none"> Small package, lower cost | <ul style="list-style-type: none"> QFN4x4 package |
| <ul style="list-style-type: none"> Push button and Motion detection | <ul style="list-style-type: none"> Various interrupt modes available |
| <ul style="list-style-type: none"> Insensitive to external magnetic stray fields | |

Applications

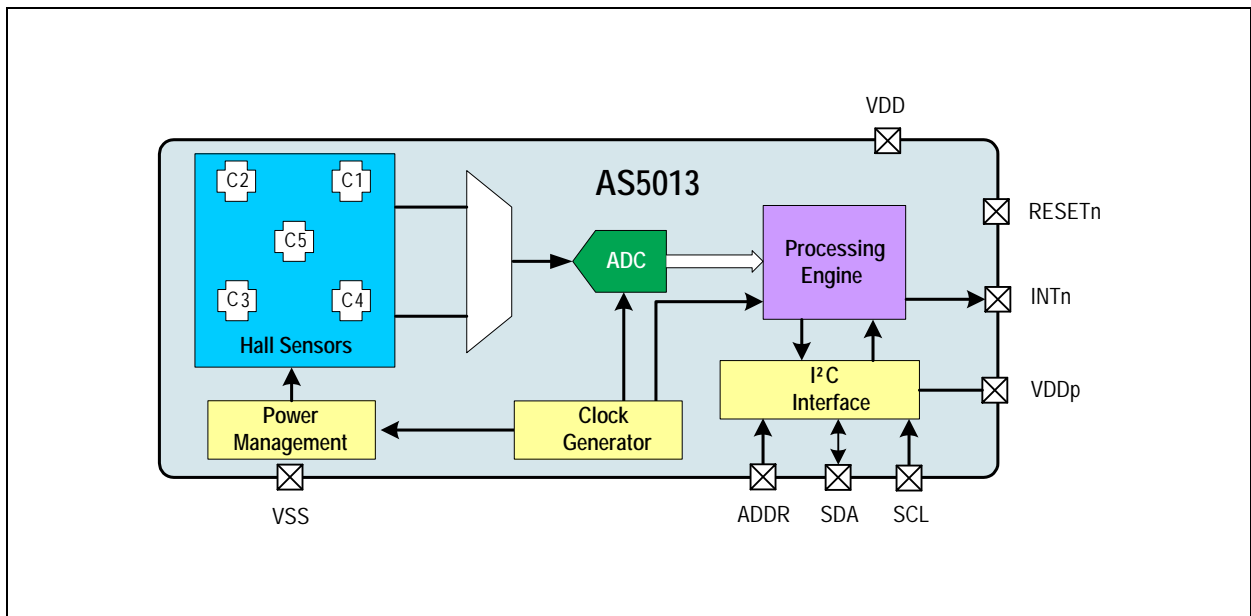
The AS5013 is ideal for small form-factor manual input devices in battery operated equipment, such as

- Mobile phones
- MP3 players
- PDAs
- GPS receivers
- Gaming consoles

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS5013 Block Diagram



Pin Assignments

Figure 3:
Pin Diagram (Top View)

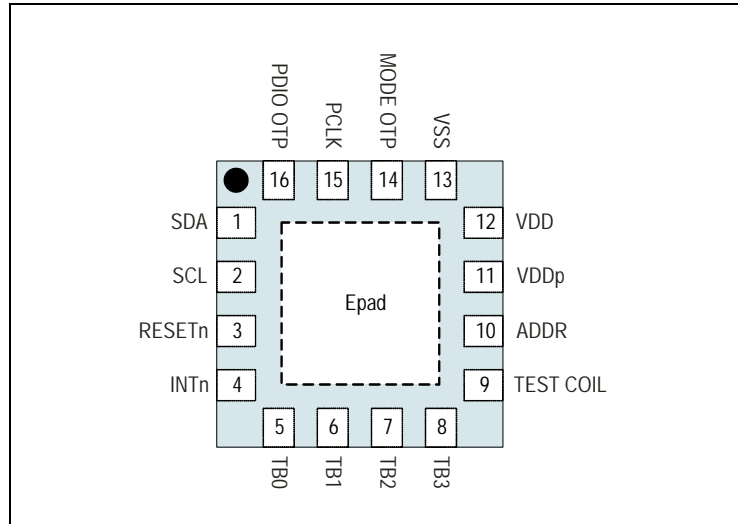


Figure 4:
Pin Descriptions

| Pin Number | Pin Name | Pin Type | ESD | Description |
|------------|-----------|--|-----|---|
| 1 | SDA | Digital I/O /Open drain | 2kV | I ² C data line, open drain |
| 2 | SCL | Digital input | 2kV | I ² C clock line |
| 3 | RESETrn | | 2kV | General reset input 0: Reset 1: Normal mode |
| 4 | INTn | Digital output open drain | 2kV | Interrupt line, open drain, active low |
| 5 | TB0 | Analog I/O | 2kV | Test pin, leave unconnected |
| 6 | TB1 | | 2kV | |
| 7 | TB2 | | 2kV | |
| 8 | TB3 | | 2kV | |
| 9 | TEST COIL | Special | 2kV | Test pin, leave unconnected or connect to VSS |
| 10 | ADDR | Digital input with Schmitt trigger functionality | 2kV | I ² C address selection input. Read in at each reset |

| Pin Number | Pin Name | Pin Type | ESD | Description |
|------------|--------------|-------------|-----|--|
| 11 | VDDp | Supply pad | 2kV | 1.7 ~ 3.6V IO power supply |
| 12 | VDD | | 2kV | 2.7 ~ 3.6V core power supply |
| 13 | VSS | | 2kV | Power supply ground |
| 14 | MODE OTP | Digital I/O | 2kV | Test pin, leave unconnected |
| 15 | PCLK | | 2kV | |
| 16 | PDIO OTP | | 2kV | |
| EPAD | Exposure Pad | - | - | Internally not connected. Leave open or connect to VSS |

Absolute Maximum Ratings

Stresses beyond those listed in [Figure 5](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Operating Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Comments |
|--|----------------------------------|------|---------------|-------|---|
| Electrical Parameters | | | | | |
| VDD | DC supply voltage | -0.3 | 5 | V | |
| VDDp | Peripheral supply voltage | -0.3 | 5 VDD +0.3 | V | |
| Vin | Input pin voltage | -0.3 | VDDp +0.3 | V | |
| | | - | 3.6 | V | |
| I _{scr} | Input current (latchup immunity) | ±100 | | mA | JEDEC 78 |
| Electrostatic Discharge | | | | | |
| ESD | Electrostatic discharge | ±2 | | kV | MIL 883 E method 3015, direct pad contact |
| θ _{JA} | Package thermal resistance | - | 32 | K/W | Velocity=0, Multi Layer PCB; JEDEC Standard Testboard |
| Temperature Ranges and Storage Conditions | | | | | |
| T _{strg} | Storage temperature | -55 | 125 | °C | |
| T _{body} | Package body temperature | | 260 | °C | IPC/JEDEC J-STD-020 ⁽¹⁾ |
| RH _{NC} | Humidity non-condensing | 5 | 85 | % | |
| MSL | Moisture Sensitive Level | 3 | | | Represents a maximum floor life time of 168h |

Note(s):

- The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*. The lead finish for Pb-free leaded packages is matte tin (100% Sn).

Electrical Characteristics

Operating Conditions

 $T_{AMB} = -20^{\circ}\text{C}$ to 80°C , $VDD = 3.3\text{V}$, $RESE\text{Tn} = \text{HIGH}$

Figure 6:
Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------|---|--|-----------------|-----|------|--------------------|
| VDD | Core supply voltage | | 2.7 | | 3.6 | V |
| VDDp | Peripheral supply voltage | Input: RESE\text{Tn} Open drain outputs: SCL, SDA, INTn. External I ² C pull up resistor to be connected to VDDp. | 1.7 | | VDD | V |
| IDD _s | Maximal average current consumption on VDD, Pulsed peaks = IDD _f depends on the sampling time ts[ms] | $T_{AMB} = -20^{\circ}\text{C}$ to 50°C | 3+3760/ts [ms] | | | μA |
| | | $T_{AMB} = 50^{\circ}\text{C}$ to 80°C | 10+3760/ts [ms] | | | |
| IDD _i | Current consumption on core supply, Idle mode, no readout (ts = infinite) | $T_{AMB} = -20^{\circ}\text{C}$ to 50°C | | | 3 | μA |
| | | $T_{AMB} = 50^{\circ}\text{C}$ to 80°C | | | 10 | |
| IDD _f | Current consumption on core supply, Idle mode, continuous readout (ts=450 μs) | Continuous current pin VDD Maximum sampling ts = 450 μs | | | 10 | mA |
| T _{pua} | Power up time analog | Step on VDD to Data_Ready | | | 1000 | μs |
| T _{conv} | Conversion time | Read X/Y coordinate I ² C Y_ res_int ACK bit of to Data_ Ready | | | 450 | μs |
| t _{p,w} | Nominal wakeup time | | 20 | | 320 | ms |
| dx dy | Lateral movement radius | The range depends on the magnet and the distance to the surface, dx ² +dy ² <= 4mm | | | 2 | mm |
| d | Type of magnet | Cylindrical; axial magnetized | 2 | | 3 | mm |
| RH | Hall array diameter | | | 2.2 | | mm |
| B _Z | Magnetic field strength | Vertical magnetic field at magnet center; measured at chip surface | 30 | | 120 | mT |
| T _{AMB} | Ambient temperature range | | -20 | | 80 | $^{\circ}\text{C}$ |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|-----------------------------------|--|-------------------------|-----|-----|----------|
| | Resolution of XY displacement | Over 2*dx and 2*dy axis | | 8 | | bit |
| | Noise (RMS) | C1..C5 channel data (result from two measurement – positive and negative current spinning) | | | 100 | μT |
| PSSR | Power Supply Rejection Ratio | VDD=3.3V; Temp = 25°C dVDD= 100 mVpp at 10.30kHz | | | 0.2 | %/100 mV |
| | IC package | | QFN16 4mmx4mmx0.55mm | | | |
| | Power supply filtering capacitors | Ceramic capacitor VDD - VSS | 100 | | | nF |
| | | Ceramic capacitor VDDp - VSS | 100 | | | nF |

Digital IO pads DC/AC Characteristics

Figure 7:
DC/AC Characteristics

| Symbol | Parameter | Conditions | Min | Max | Units |
|---------------------------------------|--------------------------|-------------|-------------|-------------|-------|
| Inputs: SCL, SDA | | | | | |
| V _{IH} | High level input voltage | IIC | 0.7 * VDDp | | V |
| V _{IL} | Low level input voltage | IIC | | 0.3 * VDDp | V |
| I _{LEAK} | Input leakage current | VDDp = 3.6V | | 1 | μA |
| Inputs: ADDR, RESETn (JEDEC76) | | | | | |
| V _{IH} | High level input voltage | JEDEC | 0.65 * VDDp | | V |
| V _{IL} | Low level input voltage | JEDEC | | 0.35 * VDDp | V |
| I _{LEAK} | Input leakage current | VDDp = 3.6V | | 1 | μA |

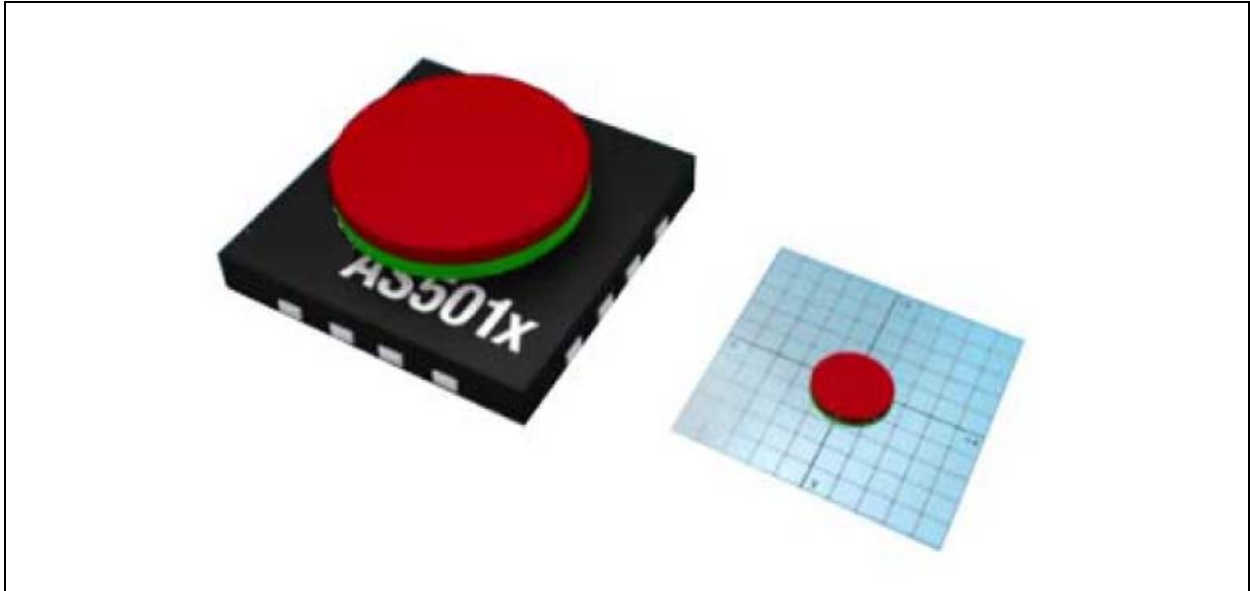
| Symbol | Parameter | Conditions | Min | Max | Units |
|--------------------------------|-----------------------------|--|---------------------------|------------|------------------------------|
| Outputs: SDA | | | | | |
| V_{OH} | High level output voltage | High level output voltage | Open drain | | Leakage current 1 μ A |
| V_{OL1} | Low level output voltage | -6mA; VDDP > 2V; Fast mode | | VSS + 0.4 | V |
| V_{OL3} | | -6mA; VDDP \leq 2V; Fast mode | | VDDP*0.2 | V |
| V_{OL1} | | -3mA; VDDP > 2V; High speed | | VSS + 0.4 | V |
| V_{OL3} | | -3mA; VDDP \leq 2V; high speed | | VDDP*0.2 | V |
| C_L | | Capacitive load | Standard mode (100kHz) | | 400 |
| | Fast mode (400kHz) | | | 400 | pF |
| | High speed mode (3.4MHz) | | | 100 | pF |
| Outputs: INTn (JEDEC76) | | | | | |
| V_{OH} | High level output voltage | High level output voltage | Open drain | | Leakage current 1 μ A |
| V_{OL} | Low level output voltage | -100 μ A | | VSS + 0.2 | V |
| V_{OL} | | -2mA | | VSS + 0.45 | V |
| C_L | Capacitive load | Standard mode (100kHz) | | 30 | pF |

Detailed Description

The benefits of the AS5013 device are as follows:

- Complete system-on-chip
- High reliability due to non-contact sensing
- Low power consumption

Figure 8:
Typical Arrangement of AS5013 and Axial Magnet



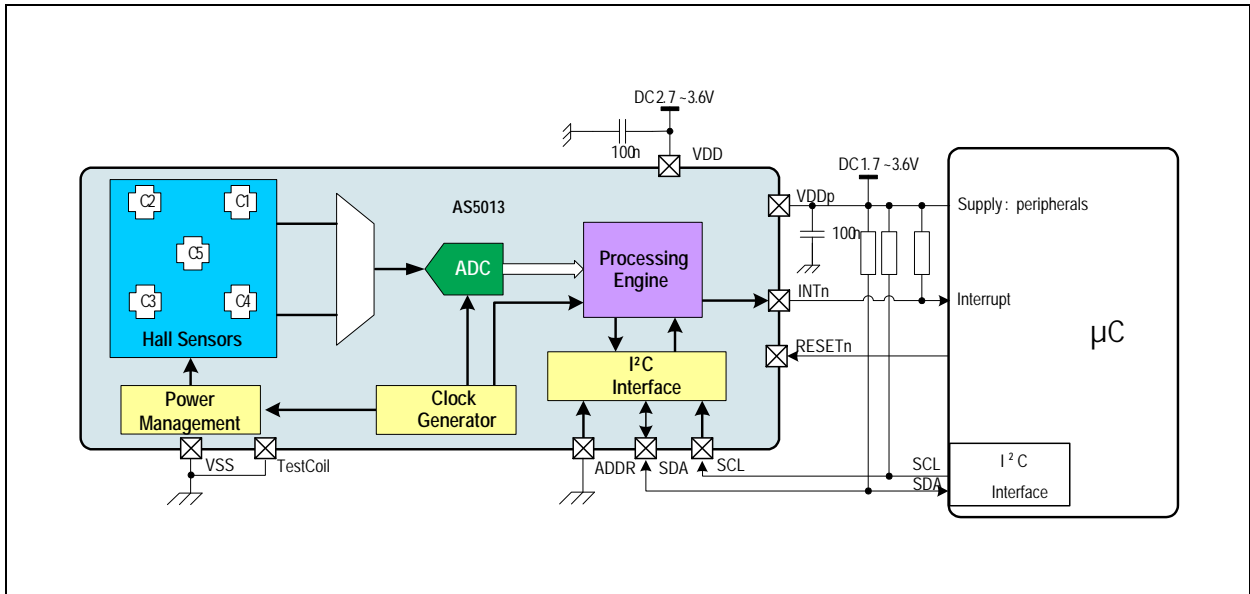
Operating the AS5013

Typical Application

The AS5013 requires only a few external components in order to operate immediately when connected to the host microcontroller.

Only 4 wires are needed for a simple application using a single power supply: two wires for power and two wires for the I²C communication. A fifth connection can be added in order to send an interrupt to the host CPU when the magnet is moving away from the center and to inform that a new valid coordinate can be read.

Figure 9:
Electrical Connection of AS5013 with Microcontroller

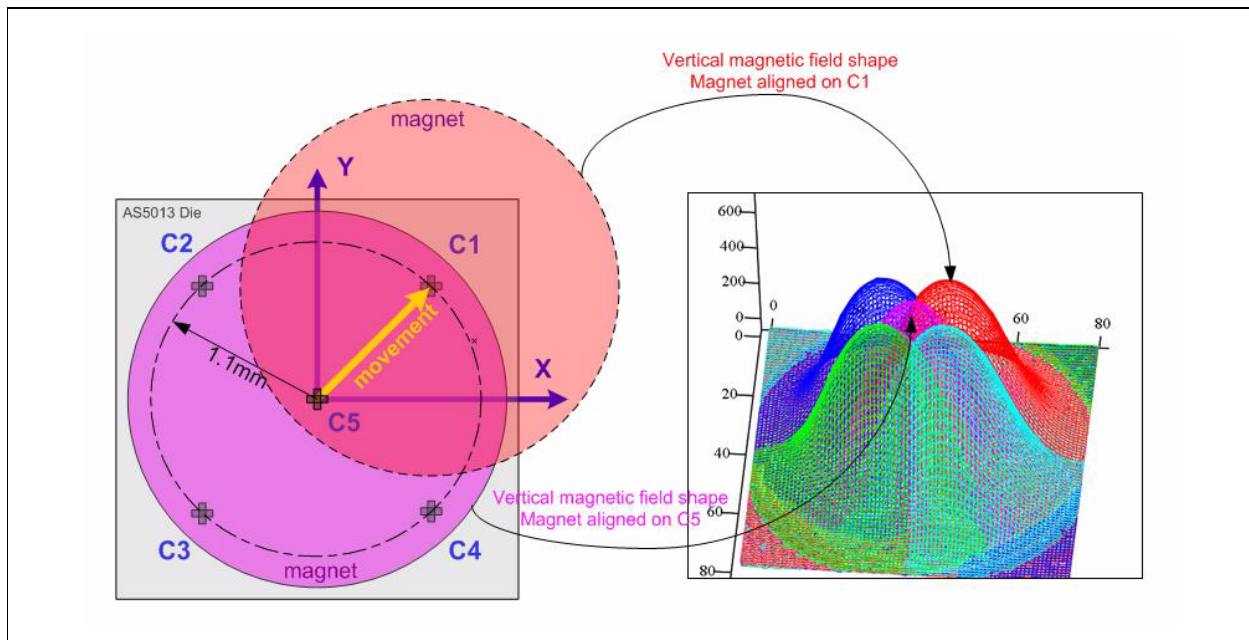


XY Coordinates Interpretation

The movement of the magnet over the Hall elements causes response which is geometrically distributed like a bell-shaped curve.

The maximum magnet travel is a circle of 2mm radius around the center of the AS5013. The Hall elements C1..C4 are placed on a circle centered on the middle of the package. The Hall element C5, placed exactly in the middle is used for better linearity response with magnet displacement larger than ±1.0mm.

Figure 10:
Hall Element Placement and Magnetic Field when the Magnet Is Centered Over Each Hall Element



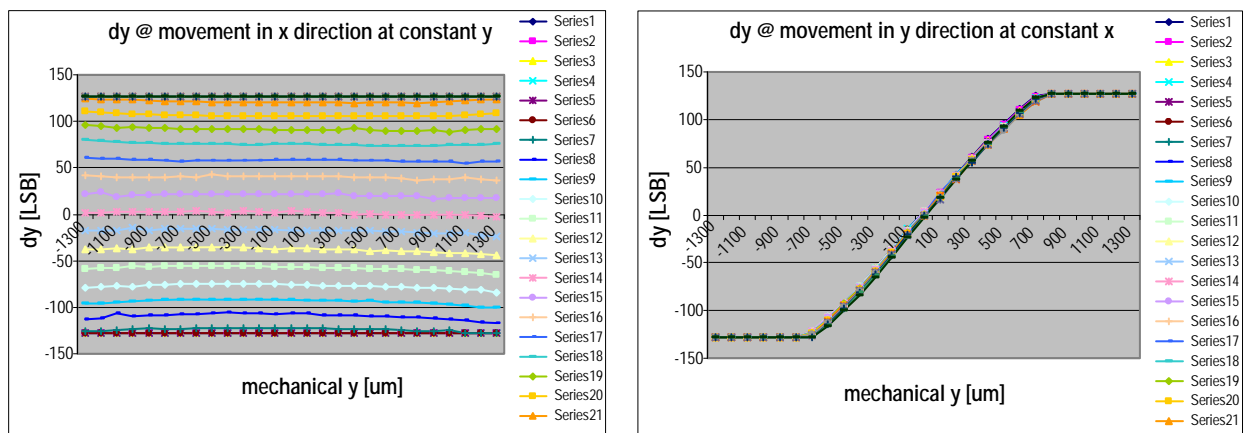
Transfer Function

AS5013 has the possibility to adjust the transfer function for the used magnet and a specific range to optimize the linearity and resolution. The value will be provided from ams and has to be written in the algorithm related registers M_ctrl [0x2B], J_ctrl [0x2C], T_ctrl [0x2D] during the initialization phase.

Please contact **ams** for parameter settings.

Below is the optimal setup for a range of ± 0.6 mm to obtain the best dynamic range from XY registers -128~+127 with one given magnet airgap, with d2x0.8mm axial magnet.

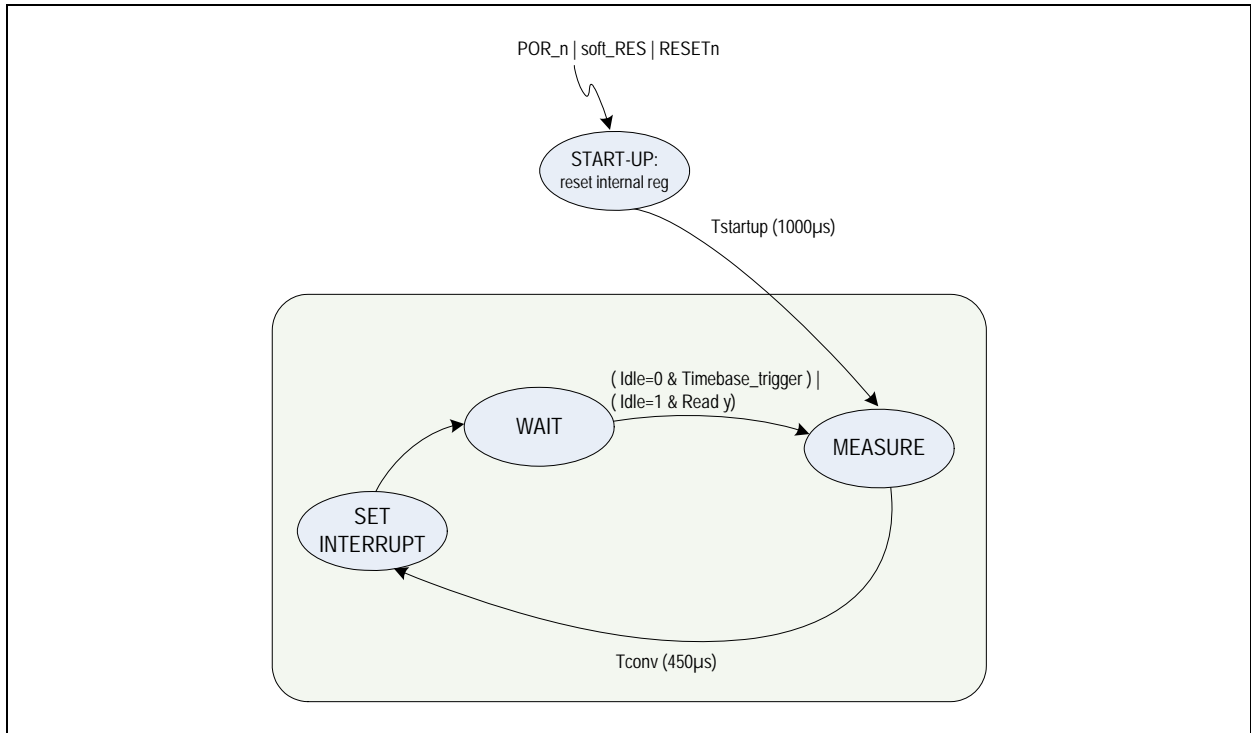
Figure 11:
Example of Transfer Function Y_displacement vs. Y_register, Optimized for 0.6mm Travel Radius



Power Modes

The AS5013 can operate in two different power modes, depending on the power consumption requirements of the whole system.

Figure 12:
Readout Cycle Depending on Power Mode (idle bit)



START-UP

After power up and after applying a soft reset (Reg 0Fh [1]) or hardware reset (RESETh input, LOW pulse >100ns), AS5013 enters the START-UP state. During this state the internal registers are loaded with their reset values. After min. Tstartup = 1000µs, the AS5013 will perform one measurement and switches automatically into the WAIT state.

MEASURE

The Hall element data are measured, x/y coordinates are calculated and available in registers 10h and 11h after Tconv = 450µs max.

SET INTERRUPT

The INTn output is set, depending on the interrupt mode configured in the control register Reg 0Fh [2] and Reg 0Fh [3]

WAIT

The module is now in waiting status. A new measurement will occur depending on the power mode (Reg 0Fh [7] Idle = 0 or 1) and the Timebase Reg 0Fh [6:4]

I²C Interface

The AS5013 supports the 2-wire high-speed I²C protocol in device mode, according to the NXP specification UM10204.

The host MCU (master) has to initiate the data transfers. The 7-bit device address of the AS5013 depends on the state at the pin ADDR.

ADDR = 0 → Slave address = '100 0000' (40h)

ADDR = 1 → Slave address = '100 0001' (41h)

For other I²C addresses, please contact **ams**.

Supported modes (slave mode):

- Random/Sequential Read
- Byte/Page Write
- Standard Mode: 0 to 100kHz clock frequency
- Fast Mode: 0 to 400kHz clock frequency
- High Speed: 0 to 3.4MHz clock frequency

The SDA signal is bidirectional and is used to read and write the serial data. The SCL signal is the clock generated by the host MCU, to synchronize the SDA data in read and write mode. The maximum I²C clock frequency is 3.4MHz, data are triggered on the rising edge of SCL.

Figure 13:
I²C Timing Diagram for FS-Mode

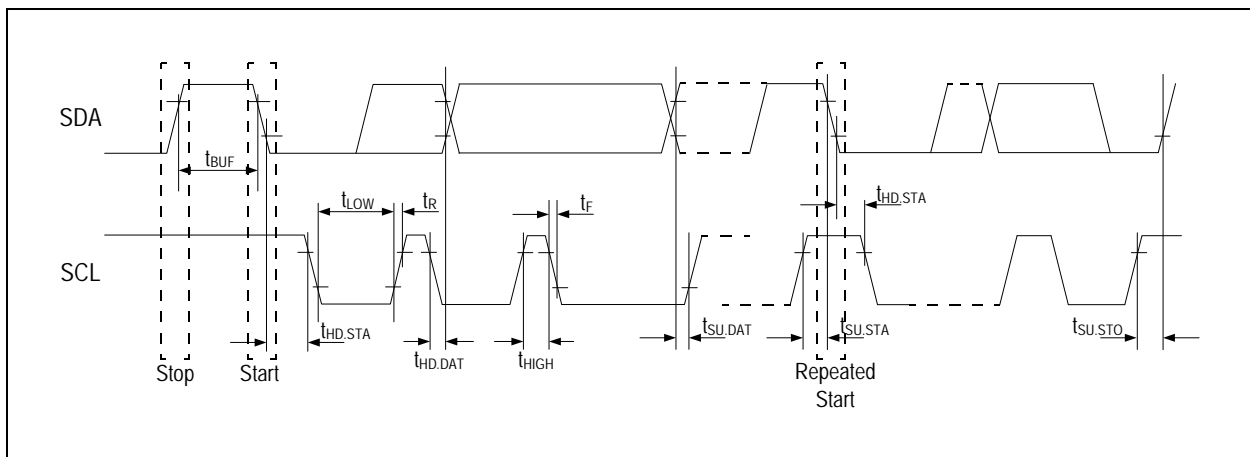
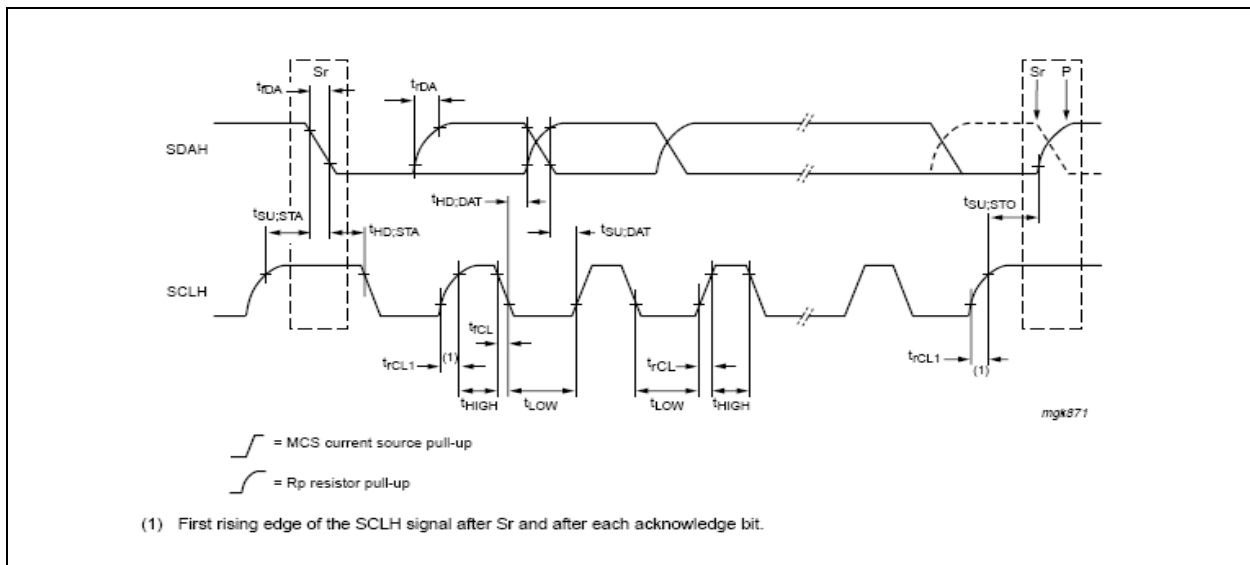


Figure 14:
Timing Diagram for HS-Mode



I²C Electrical Specification

Standard-mode, Fast-mode, High speed-mode

Figure 15:
I²C Electrical Specification

| Symbol | Parameter | Condition | Min | Max | Units |
|------------------|---|--|---------|---------------------------|-------|
| V _{IL} | LOW-level input voltage | | -0.5 | 0.3VDDp | V |
| V _{IH} | HIGH-level input voltage | | 0.7VDDp | VDDp + 0.5 ⁽¹⁾ | V |
| V _{hys} | Hysteresis of Schmitt Trigger inputs | VDDp < 2V | 0.1VDDp | | V |
| V _{OL} | LOW-level output voltage (open-drain or open-collector) at 3mA sink current | VDDp < 2V | - | 0.2VDDp | V |
| I _{OL} | LOW-level output current | V _{OL} = 0.4V | - | - | mA |
| I _{CS} | Pull-up current of SCLH current source | SCLH output levels between 0.3VDDp and 0.7VDDp | 3 | 12 | mA |
| t _{SP} | Pulse width of spikes that must be suppressed by the input filter | In HS-mode | - | 10 ⁽²⁾ | ns |
| | | In Fast-mode | | 50 ⁽²⁾ | ns |
| I _i | Input current at each I/O Pin | Input voltage between 0.1VDDp and 0.9VDDp | | 10 ⁽³⁾ | μA |

| Symbol | Parameter | Condition | Min | Max | Units |
|-----------|---|-----------|-----|-----|-------|
| C_B | Total capacitive load for each bus line | | - | 400 | pF |
| $C_{I/O}$ | I/O capacitance (SDA, SCL) | | - | 10 | pF |

Note(s):

1. Maximum $V_{IH} = V_{DDpmax} + 0.5V$ or $5.5V$, which ever is lower.
2. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50ns in Fast-mode and 10ns in HS-mode.
3. I/O pins of Fast-mode and Fast-mode plus devices must not obstruct the SDA and SCL lines if V_{DDp} is switched off.

Figure 16:
I²C Timing

| Symbol | Parameter | Condition | Fast-Mode | | HS-Mode $C_B=100pF$ | | HS-Mode $C_B=400pF^{(1)}$ | | Unit |
|--------------|--|-----------|-----------|-----|------------------------|------|------------------------------|------|------|
| | | | Min | Max | Min | Max | Min | Max | |
| f_{SCLK} | SCL clock Frequency | | - | 400 | - | 3400 | - | 1700 | kHz |
| t_{BUF} | Bus Free Time; time between STOP and START Condition | | 500 | - | 500 | - | 500 | - | ns |
| $t_{HD;STA}$ | Hold Time; (Repeated) START Condition ⁽²⁾ | | 600 | - | 160 | - | 160 | - | ns |
| t_{LOW} | LOW Period of SCL Clock | | 1300 | - | 160 | - | 320 | - | ns |
| t_{HIGH} | HIGH Period of SCL Clock | | 600 | - | 60 | - | 120 | - | ns |
| $t_{SU;STA}$ | Setup Time for a Repeated START condition | | 600 | - | 160 | - | 160 | - | ns |
| $t_{HD;DAT}$ | Data Hold Time ⁽³⁾ | | 0 | 900 | 0 | 70 | 0 | 150 | ns |
| $t_{SU;DAT}$ | Data Setup Time ⁽⁴⁾ | | 100 | - | 10 | - | 10 | - | ns |

| Symbol | Parameter | Condition | Fast-Mode | | HS-Mode $C_B=100\text{pF}$ | | HS-Mode $C_B=400\text{pF}^{(1)}$ | | Unit |
|--------------|--|--|-------------|-----|-------------------------------|-----|-------------------------------------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| t_{rCL} | Rise time of SCLH signal | External pull-up source of 3mA | - | - | 10 | 40 | 20 | 80 | ns |
| t_{rCL1} | Rise time of SCLH signal after repeated START condition and after an acknowledge bit | External pull-up source of 3mA | - | - | 10 | 80 | 20 | 160 | ns |
| t_R | Rise Time of SDA and SCL Signals | | $20+0.1C_B$ | 120 | - | - | - | - | ns |
| t_F | Fall time of SDA and SCL signals | | $20+0.1C_B$ | 120 | - | - | - | - | ns |
| $t_{SU;STO}$ | Setup Time for STOP Condition | | 600 | - | 160 | - | 160 | - | ns |
| V_{nL} | Noise margin at LOW level | For each connected device (including hysteresis) | 0.1VDDp | - | 0.1 VDDp | - | 0.1 VDDp | - | V |
| V_{nH} | Noise margin at HIGH level | | 0.2VDDp | - | 0.2 VDDp | - | 0.2 VDDp | - | V |

Note(s):

- For bus line loads C_B between 100pF and 400 pF the timing parameters must be linearly interpolated.
- After this time the first clock is generated.
- A device must internally provide a minimum hold time (300ns for Fast-mode, 80ns / max 150ns for High-speed mode) for the SDA signal (referred to the V_{IHmin} of the SCL) to bridge the undefined region of the falling edge of SCL.
- A fast-mode device can be used in standard-mode system, but the requirement $t_{SU;DAT} = 250\text{ns}$ must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{Rmax} + t_{SU;DAT} = 1000 + 250 = 1250\text{ns}$ before the SCL line is released.

I²C Modes

The AS5013 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus.

The AS5013 operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and the input SCL. Clock stretching is not included.

Automatic Increment of Address Pointer

The AS5013 slave automatically increments the address pointer after each byte transferred. The increase of the address pointer is independent from the address being valid or not.

Invalid Addresses

If the user sets the address pointer to an invalid address, the address byte is not acknowledged. Nevertheless a read or write cycle is possible. The address pointer is increased after each byte.

Reading

When reading from a wrong address, the AS5013 slave data returns all zero. The address pointer is increased after each byte. Sequential read over the whole address range is possible including address overflow.

Writing

A write to a wrong address is not acknowledged by the AS5013 slave, although the address pointer is increased. When the address pointer points to a valid address again, a successful write access is acknowledged. Page write over the whole address range is possible including address overflow.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as start or stop signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy:

Both data and clock lines remain HIGH.

Start Data Transfer:

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer:

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid:

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a

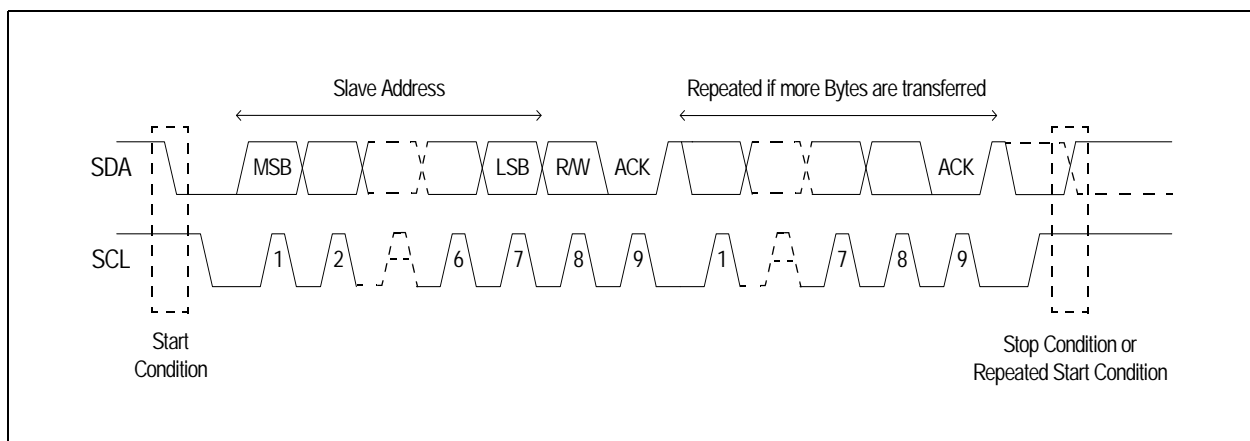
START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge:

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of READ access to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 17:
Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



Depending upon the state of the R/W bit, two types of data transfer are possible:

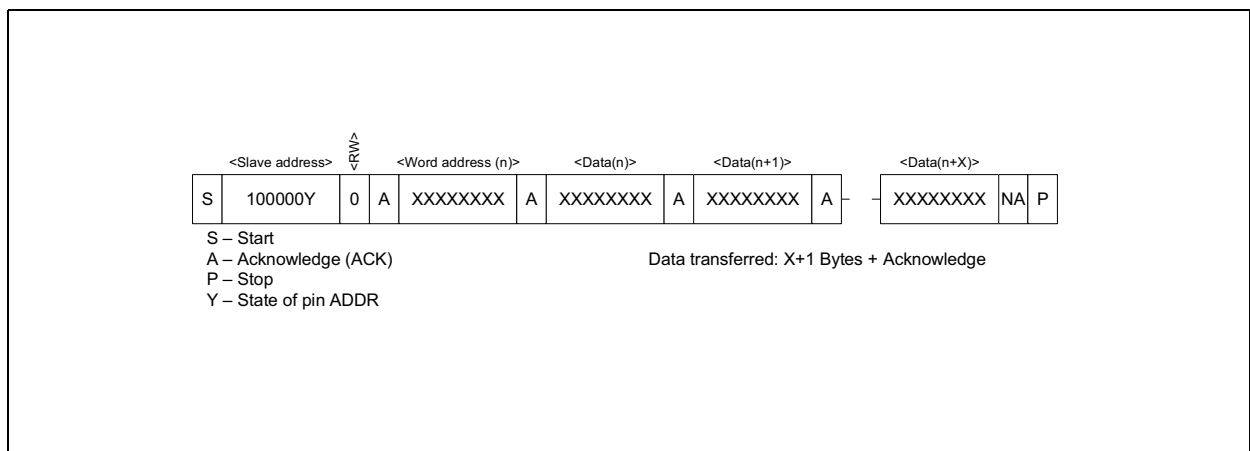
- Data transfer from a master transmitter to a slave receiver:** The first byte transmitted by the master is the slave address, followed by R/W = 0. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. If the slave does not understand the command or data it sends a “not acknowledge”. Data is transferred with the most significant bit (MSB) first.
- Data transfer from a slave transmitter to a master receiver:** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and

the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS5013 can operate in the following two modes:

- Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. Each byte is followed by an acknowledge bit (or by a not acknowledge depending on the address-pointer pointing to a valid position). START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 18). The slave address byte is the first byte received after the START condition. The slave address byte contains the 7-bit AS5013 address, which is stored in the OTP memory. The 7-bit slave address is followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA. After the AS5013 acknowledges the slave address + write bit, the master transmits a register address to the AS5013. This sets the address pointer on the AS5013. If the address is a valid readable address the AS5013 answers by sending an acknowledge. If the address-pointer points to an invalid position a “not acknowledge” is sent. The master may then transmit zero or more bytes of data. In case of the address pointer pointing to an invalid address the received data are not stored. The address pointer will increment after each byte transferred independent from the address being valid. If the address-pointer reaches a valid position again, the AS5013 answers with an acknowledge and stores the data. The master generates a STOP condition to terminate the data write.

Figure 18:
Data Write - Slave Receiver Mode



- Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on

SDA by the AS5013 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS5013 address. The default address is 40h. The 7-bit slave address is followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS5013 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS5013 must receive a “not acknowledge” to end a read.

Figure 19:
Data Read (from Current Pointer Location) - Slave Transmitter Mode

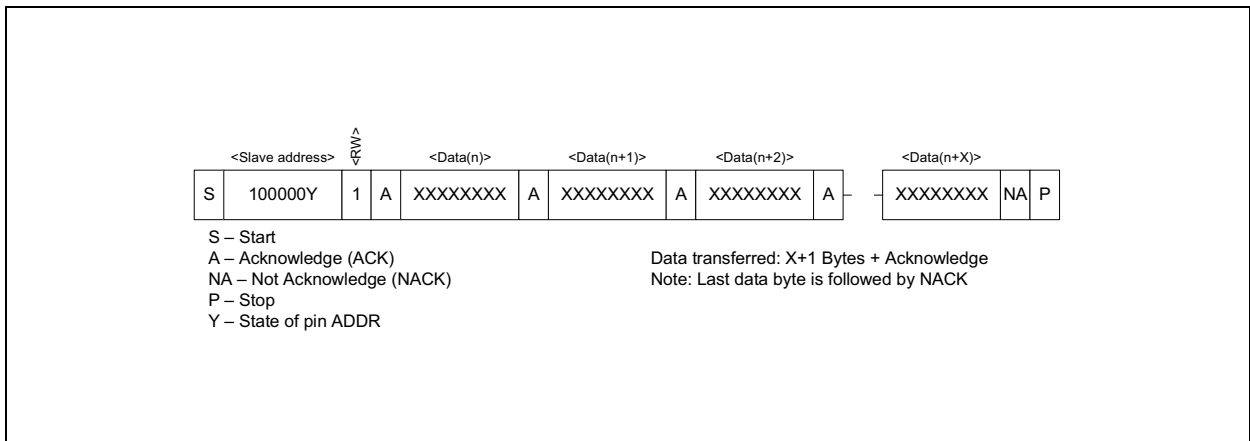
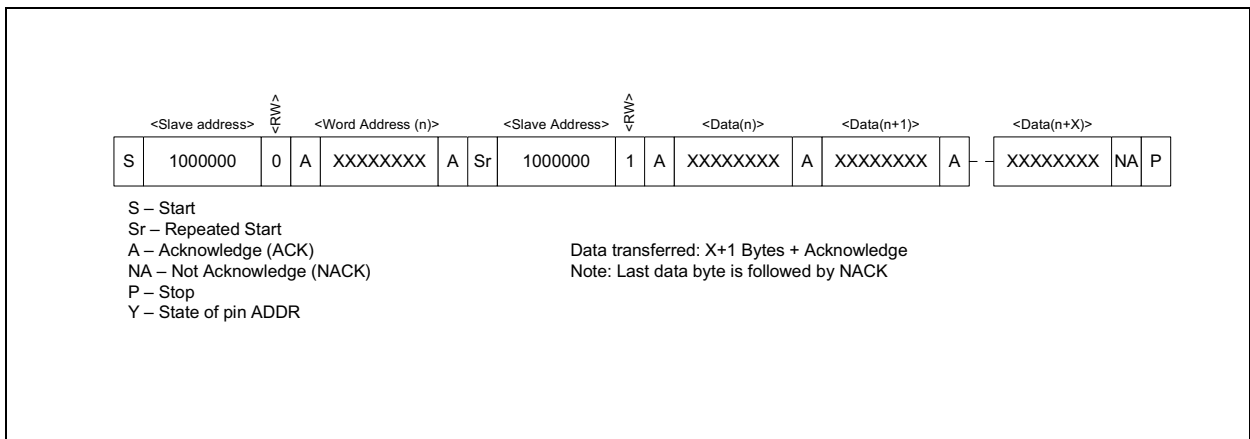


Figure 20:
Data Read (from New Pointer Location) - Slave Transmitter Mode



High Speed Mode

The AS5013 is capable to work in HS-mode.

For switching to HS-mode the Master has to send the sequence: START, MASTER CODE, NACK. This sequence is sent in FS-mode. As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge. After a device receives the master code it has to switch from FS-settings to HS-settings within $t_{SU.STA}$ which is 160ns for HS-mode. The device stays in HS-mode as long as it does not receive a STOP command. After receiving a STOP command it has to switch back from HS-settings to FS-settings, which has to be completed within the minimum bus free time t_{BUF} which is 500ns.

When switching to HS-mode the slave has to:

- Adapt the SDAH and SCLH input filters according to the spike suppression requirement required in HS-mode. In HS-mode spikes up to 10ns, in FS-mode spikes up to 50ns have to be suppressed.
- Adapt the setup and hold times according to the HS-mode requirement. In HS-mode an internal hold time for SDA for START/STOP detection of 80ns (max. 150ns), in FS-mode an internal hold time of 160ns (max. 250ns) has to be provided.
- Adapt the slope control for SDAH output stage.

Figure 21:
Data Transfer Format in HS-Mode

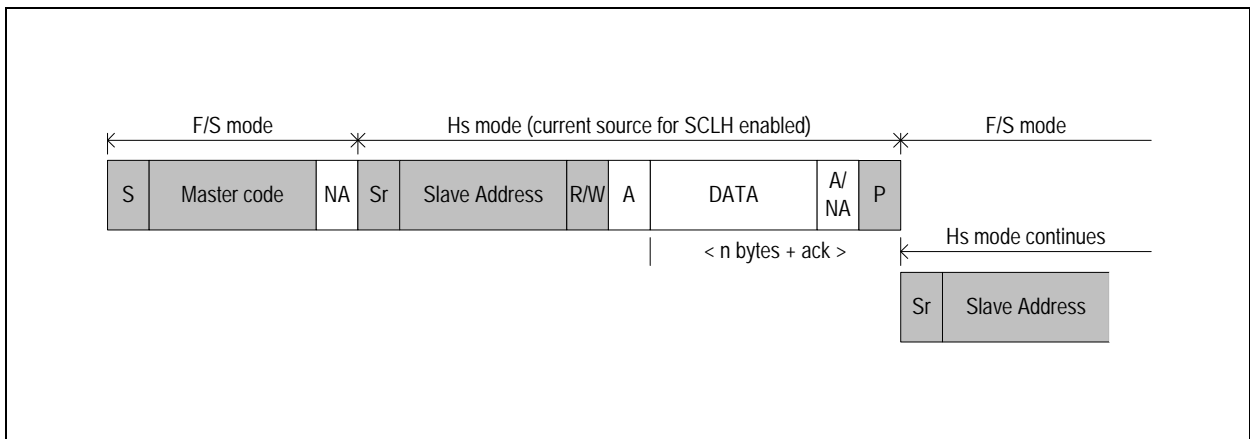
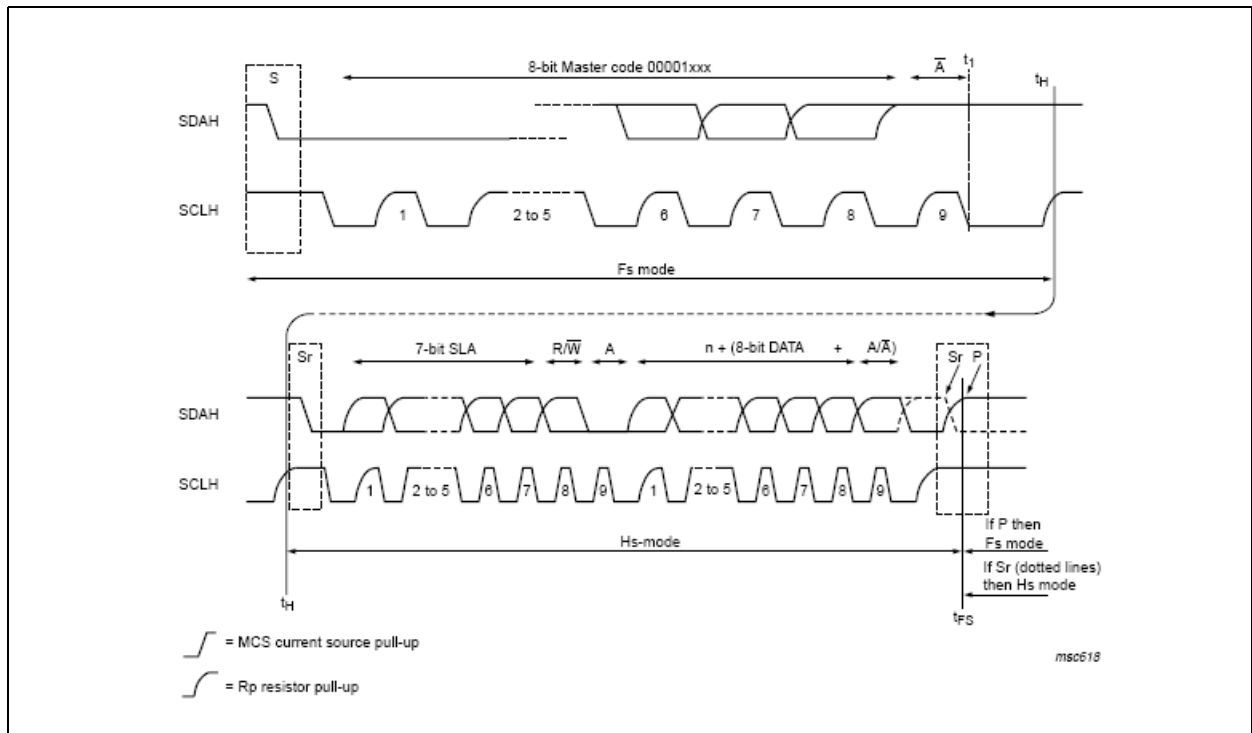


Figure 22:
A Complete HS-Mode Transfer



Automatic Increment of Address Pointer

The AS5013 slave automatically increments the address pointer after each byte transferred. The increase of the address pointer is independent from the address being valid or not.

Invalid Addresses

If the user sets the address pointer to an invalid address, the address byte is not acknowledged. Nevertheless a read or write cycle is possible. The address pointer is increased after each byte.

Reading:

When reading from a wrong address, the AS5013 slave returns all zero. The address pointer is increased after each byte. Sequential read over the whole address range is possible including address overflow.

Writing:

A write to a wrong address is not acknowledged by the AS5013 slave, although the address pointer is increased. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

SDA, SCL Input Filters

Input filters for SDA and SCL inputs are included to suppress noise spikes of less than 50ns. Furthermore, the SDA line is delayed by 120ns to provide an internal hold time for Start/Stop detection to bridge the undefined region of the falling edge of SCL. The delay needs to be smaller than $t_{HD,STA}$ 260ns.

I²C Registers

Figure 23:
Control Register 1 (0Fh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------|------------------|------------------|------------------|-------------|--------------|----------|------------|
| Idle | Time base bit[2] | Time base bit[1] | Time base bit[0] | INT_disable | INT_function | Soft_rst | Data_valid |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |
| Reset value: 1111 0000 | | | | | | | |

| Bit | Bit Description |
|-----|---|
| 7 | 0= Low Power Mode The measurements are triggered with an internal low power oscillator – the user can select between 8 different timings by setting the low power timebase (Control Register 1 [6:4]) |
| | 1=Idle Mode (default) A new measurement cycle is started after the I ² C ACK bit following the read out of the Y_res_int register 11h. The readout rate and thus the power consumption is externally controlled by the host MCU. |
| 6:4 | Configure the time base of the automatic wakeup in Low Power Mode (see Figure 24). |
| 3 | 0=Interrupt output INTn is enabled (default) |
| | 1=Interrupt output INTn is disabled and is fixed to Hi-Z |
| 2 | 0=Interrupt output INTn is active '0' after each measurement (default): <ul style="list-style-type: none"> - Automatically triggered in Low Power mode, depending on the time base chosen - 450µs after Y readout in Idle mode The interrupt is cleared by the I ² C ACK bit after reading the Y_res_int 11h. In block read mode, the several other bytes could be transferred before the interrupt is cleared. |
| | 1=Interrupt output INTn is active '0' when the movement of the magnet exceeds the Dead Zone area. (see Figure 25). The Dead Zone area is set by registers Xp (Reg 12h), Xn (Reg 13h), Yp (Reg 14h), Yn (Reg 15h). The interrupt is cleared by the I ² C ACK bit after reading the Y_res_int register 11h, and will be active '0' at the next measurement if the magnet is still in the Detection Area. In block read mode, several other bytes could be transferred before the interrupt is cleared when the Y_res_int register is read. It is recommended to use this mode with the Low Power mode (Idle = 0), in order to wake up automatically a system when the magnet has been moved away from the center. The polling time is set by the Low Power time base bit [6:4]. |
| 1 | 0=Normal mode (default) |
| | 1=Reset mode. All the internal registers are loaded with their reset value. The Control Register 1 is loaded as well with the value 1111 0000, then the Soft_rst bit goes back to 0 (Normal mode) once the internal reset sequence is finished. |

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|-------|-------|-------|-------|-------|-------|-------|
| 0 | | | | | | | |
| 0=Conversion of new coordinates ongoing, no valid coordinate is present in the X and Y_res_int registers. Reading those registers at that moment can give wrong values. | | | | | | | |
| 1=New coordinate values are ready in X and Y_res_int registers. | | | | | | | |

Note(s):

- The values in Control Register 1, X_register and Y_res_int register are frozen when the I²C address pointer is set to 0Fh, 10h or 11h. This ensures that the Data_valid bit, X and Y values are taken at the same time. In order to get updated values from those registers, set the address pointer to any other address.

Figure 24:
Configuration

| Low Power Time Base CONFIG_REG1 0Fh [6:4] | $\Delta t_{\text{timebase}}$ (ms) | Average Core Current IDD (μA) @T _{AMB} = 25°C |
|---|--------------------------------------|--|
| 000b | 20 | 190 |
| 001b | 40 | 97 |
| 010b | 80 | 50 |
| 011b | 100 | 40 |
| 100b | 140 | 30 |
| 101b | 200 | 22 |
| 110b | 260 | 17 |
| 111b (default) | 320 | 15 |

Figure 25:
Dead Zone Representation with INT_function=1

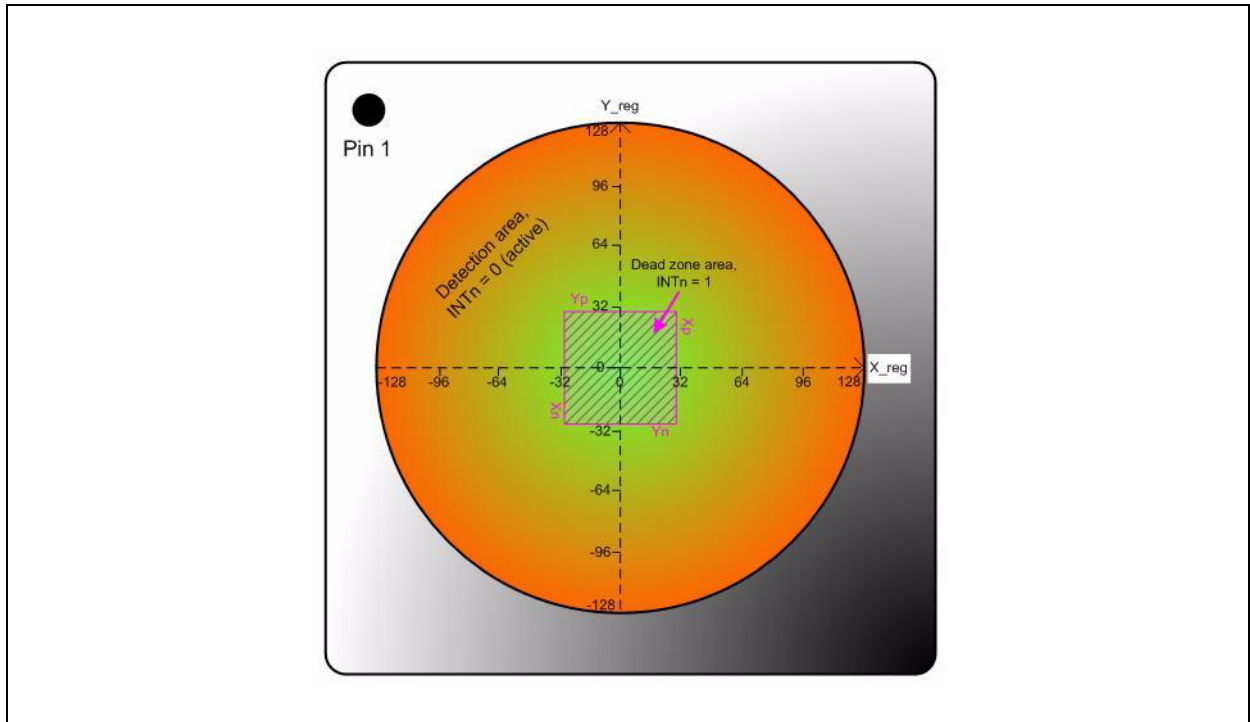


Figure 26:
X Register (10h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------|-------|-------|-------|-------|-------|-------|-------|
| X[7] | X[6] | X[5] | X[4] | X[3] | X[2] | X[1] | X[0] |
| R | R | R | R | R | R | R | R |
| Reset value: 0000 0000 | | | | | | | |

| Bit | Bit Description |
|-----|---|
| 7:0 | X coordinate, Two's complement format (signed -128 ~ +127). |

Figure 27:
Y_res_int Register (11h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------|-------|-------|-------|-------|-------|-------|-------|
| Y[7] | Y[6] | Y[5] | Y[4] | Y[3] | Y[2] | Y[1] | Y[0] |
| R | R | R | R | R | R | R | R |
| Reset value: 0000 0000 | | | | | | | |

| Bit | Bit Description |
|-----|---|
| 7:0 | Y coordinate, Two's complement format (signed -128 ~ +127). Reading this register will reset the INTn output to Hi-Z after the ACK bit of Y_res_int register readback. |

Figure 28:
Xp Register (12h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------------------|-------|-------|-------|-------|-------|-------|-------|
| Xp[7] | Xp[6] | Xp[5] | Xp[4] | Xp[3] | Xp[2] | Xp[1] | Xp[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: 0000 0101 (5d) | | | | | | | |

| Bit | Bit Description |
|-----|---|
| 7:0 | Xp range value, Two's complement (signed: -128 ~ +127). Determines the LEFT threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (See Figure 23). |

Figure 29:
Xn Register (13h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Xn[7] | Xn[6] | Xn[5] | Xn[4] | Xn[3] | Xn[2] | Xn[1] | Xn[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: 1111 1011 (-5d) | | | | | | | |

| Bit | Bit Description |
|-----|--|
| 7:0 | Xn range value, Two's complement (signed: -128 ~ +127). Determines the RIGHT threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (See Figure 23). |

Figure 30:
Yp Register (14h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------------------|-------|-------|-------|-------|-------|-------|-------|
| Yp[7] | Yp[6] | Yp[5] | Yp[4] | Yp[3] | Yp[2] | Yp[1] | Yp[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: 0000 0101 (5d) | | | | | | | |

| Bit | Bit Description |
|-----|--|
| 7:0 | Yp range value, Two's complement (signed: -128 ~ +127). Determines the TOP threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (See Figure 23). |

Figure 31:
Yn Register (15h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Yn[7] | Yn[6] | Yn[5] | Yn[4] | Yn[3] | Yn[2] | Yn[1] | Yn[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: 1111 1011 (-5d) | | | | | | | |

| Bit | Bit Description |
|-----|---|
| 7:0 | Yn range value, Two's complement (signed: -128 ~ +127). Determines the BOTTOM threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (See Figure 23). |

Figure 32:
M_ctrl Register (2Bh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| M_ctrl[7] | M_ctrl[6] | M_ctrl[5] | M_ctrl[4] | M_ctrl[3] | M_ctrl[2] | M_ctrl[1] | M_ctrl[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: 0000 0000 (00h) | | | | | | | |

| Bit | Bit Description |
|-----|---|
| 7:0 | Middle Hall element C5 control register to improve the linearity of XY outputs for the whole mechanical XY displacement of the magnet. Use the default value for d=2*0.8mm standard axial magnet. For more information on how to configure this parameter, please contact ams . |

Figure 33:
J_ctrl Register (2Ch)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| J_ctrl[7] | J_ctrl[6] | J_ctrl[5] | J_ctrl[4] | J_ctrl[3] | J_ctrl[2] | J_ctrl[1] | J_ctrl[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: 0000 0110 (06h) | | | | | | | |

| Bit | Bit Description |
|-----|---|
| 7:0 | Sector dependent attenuation of the outer Hall elements C1..C4 in order to improve the linearity of XY outputs for the whole mechanical XY displacement of the magnet. Use the default value for d=2*0.8mm standard axial magnet. For more information on how to configure this parameter, please contact ams . |

Figure 34:
T_ctrl Register (2Dh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| T_ctrl[7] | T_ctrl[6] | T_ctrl[5] | T_ctrl[4] | T_ctrl[3] | T_ctrl[2] | T_ctrl[1] | T_ctrl[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: 0000 1001 (09h) | | | | | | | |

| Bit | Bit Description |
|-----|---|
| 7:0 | Scaling control register. This register controls the scaling factor of the XY coordinates to fit to the 8-bit X and Y_res_int register (full dynamic range). The following table includes scaling factors referenced to the default setting T_ctrl = 9 (100% scaling). |

| T_ctrl | Scaling Factor % |
|--------|------------------|
| 31 | 31.3 |
| 30 | 32.2 |
| 29 | 33.4 |
| 28 | 34.6 |
| 27 | 35.7 |
| 26 | 37.1 |
| 25 | 38.5 |
| 24 | 40.0 |
| 23 | 41.6 |
| 22 | 43.6 |
| 21 | 45.5 |
| 20 | 47.7 |
| 19 | 50.0 |
| 18 | 52.5 |
| 17 | 55.5 |
| 16 | 58.8 |
| 15 | 62.5 |
| 14 | 66.6 |
| 13 | 71.5 |

| T_ctrl | Scaling Factor % |
|--------|------------------|
| 47 | 117.6 |
| 7 | 125.0 |
| 45 | 133.4 |
| 6 | 142.8 |
| 43 | 153.9 |
| 5 | 166.6 |
| 41 | 181.8 |
| 4 | 200.0 |
| 79 | 210.5 |
| 39 | 222.3 |
| 77 | 235.4 |
| 3 | 250.0 |
| 75 | 266.6 |
| 37 | 285.7 |
| 73 | 307.6 |
| 2 | 333.4 |
| 71 | 363.7 |
| 35 | 400.0 |
| 69 | 444.5 |

| T_ctrl | Scaling Factor % |
|--------|------------------|
| 12 | 77.0 |
| 11 | 83.4 |
| 10 | 90.8 |
| 9 | 100.0 |
| 8 | 111.1 |

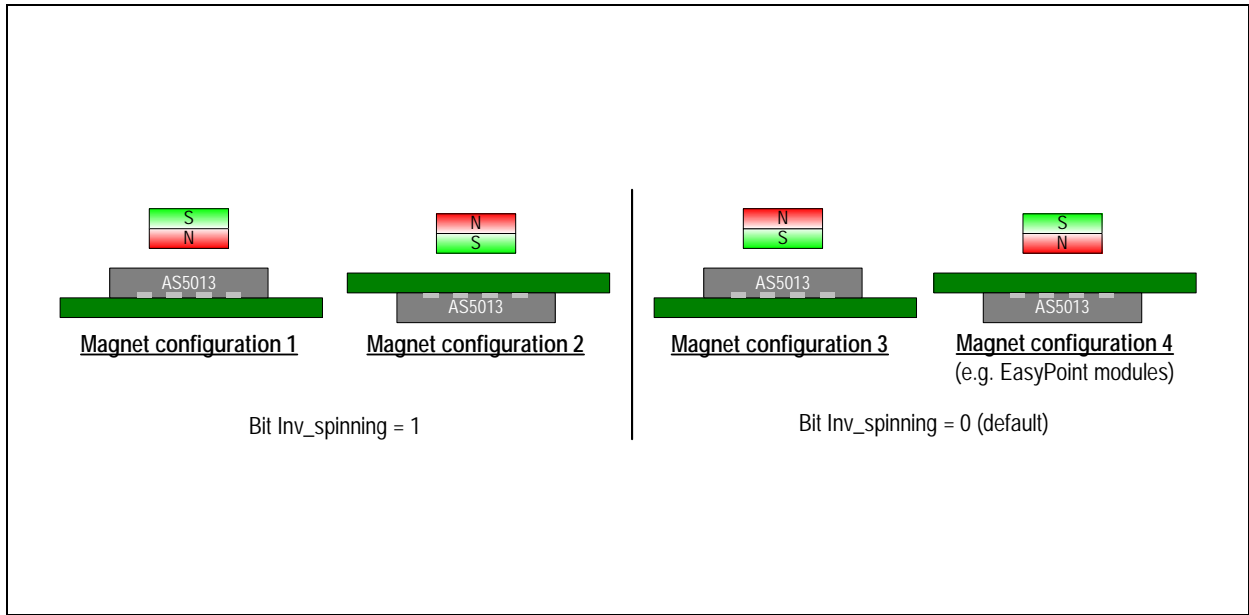
| T_ctrl | Scaling Factor % |
|--------|------------------|
| 1 | 500.0 |
| 67 | 571.5 |

Figure 35:
Control Register 2 (2Eh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------|-------|-------|------------|-------------------|----------------|--------------|-------|
| Test | Test | Test | ext_clk_en | use_static_offset | EN_offset_comp | inv_spinning | Test |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: 1000 0100 | | | | | | | |

| Bit | Bit Description |
|-----|--|
| 7 | Test bit. Must configured '1'. |
| 6:4 | Test bit. Must configured '000'. |
| 3 | Test bit. Must configured '0'. |
| 2 | Test bit. Must configured '1'. |
| 1 | Magnet Polarity bit. Must be set after power up, depending on how the magnet is placed Figure 36 |
| 0 | Test bit. Must configured '0'. |

Figure 36:
Magnet Configuration



Note: In order to know the polarity of the magnet without any testing device, please refer to [Registers Initialization](#)

Hall Element Direct Read Registers (16h to 29h)

Each Hall element C1..C5 can be read independently, after each interrupt (data ready).

One hall element value consists of two 12-bit signed-registers: Cx_neg and Cx_pos. For each conversion cycle (i.e. after a readout or Y_res in idle mode, or at each time-based conversion cycle in Low Power mode), each Hall element is read twice: With normal spin (result Cx_pos) and then with inverted spin (result Cx_neg) in order to remove any Hall voltage offset from the Hall elements.

The formula to read any Hall element Cx:

$$(EQ1) \quad Cx = (Cx_pos - Cx_neg) / 2$$

Where

$$Cx_pos = (Cx_pos[11:8] \ll 8) | Cx_pos[7:0]$$

$$Cx_neg = (Cx_neg[11:8] \ll 8) | Cx_neg[7:0]$$

Figure 37:
Hall Element Direct Read Registers (2Ah)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | AGC5 | AGC4 | AGC3 | AGC2 | AGC1 | AGC0 |
| R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: 0010 0000 | | | | | | | |

The AGC register controls the sensitivity of each Hall element C1...C5, in order to stay in the larger dynamic range of the 12-bit ADC of the AS5013. In order to determine the best value to be set during the AS5013 initialization, place your magnet on the 0,0 position (centered on C5 Hall element), and increase the AGC value to obtain the nearest value to 2867 (= 70% of 4096).

It is possible that this value cannot be reached with small magnets or with large airgaps. In that case set AGC to 3Fh, which is the maximum sensitivity.

Power ON

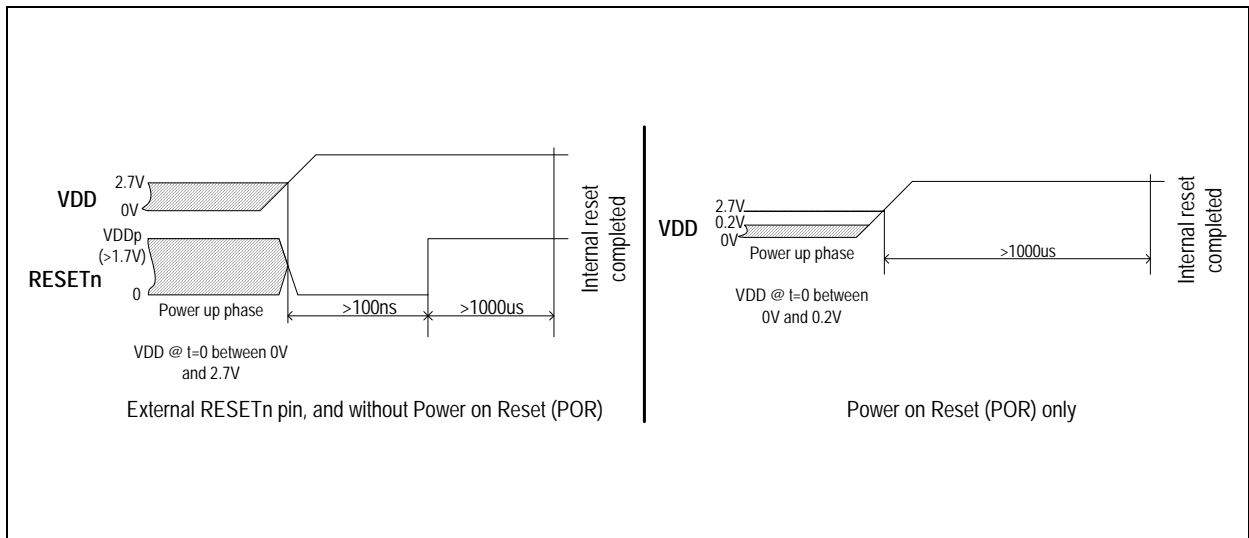
The AS5013 has a Power ON Reset (POR) cell to monitor the VDD voltage at startup and reset all the internal registers.

After the internal reset is completed, the POR cell is disabled in order to save current during normal operation.

If VDD drops below 2.7V down to 0.2V, the POR cell will not be enabled back, and the registers will not be correctly reseted or can get random values.

Note: It is highly recommended to control the external RESETn signal by applying a LOW pulse of >100ns once VDD reached 2.7V and VDDp reached 1.7V.

Figure 38:
Power-Up Sequence



Registers Initialization

After Power Up, the following sequence must be performed:

1. VDD and VDDp Power up, and reached their nominal values (VDD>2.7V, VDDp>1.7V).
2. RESETn LOW during >100ns
3. Delay 1000µs
4. Loop check register [0Fh] until the value F0h or F1h is present (reset finished, registers to their default values)
5. Optional: Write value 86h into register [2Eh] → Invert magnet polarity. See Control Register 2 (2Eh) on page 22.
6. Configure register [2Bh] → Configure M_ctrl middle Hall element control
7. Configure register [2Ch] → Configure J_ctrl attenuation factor
8. Configure register [2Dh] → Configure T_ctrl scaling factor
9. Configure the wanted Power Mode into register [0Fh] (Idle mode or Low Power Mode with Timebase configuration)
10. X Y coordinates are ready to be read.

Note: In order to detect if the magnet polarity is correct, read the C5 middle Hall element when the magnet is centered.

$$C5 = (C5_pos - C5_neg) / 2$$

$$\text{With: } C5_pos = (c5_pos[11:8] \ll 8) | c5_pos[7:0]$$

$$C5_neg = (c5_neg[11:8] \ll 8) | c5_neg[7:0]$$

C5 must always be positive.

If C5 is negative, then invert the bit inv_spinning in the Control Register 2 (2Eh). C5 will become positive.

Registers Table

The following registers / functions are accessible over the serial I²C interface.

Figure 39:
Registers

| Register | Number of Bits | Access | Address | Format | Reset Value | Bit | Description |
|---------------------------|----------------|--------|---------|--------|-------------|-------|---|
| IC Identification | | | | | | | |
| ID Code | 8 | R | 0C | | 0Ch | <7:0> | 8-bit Manufacture ID Code |
| ID Version | 8 | R | 0D | | 0Dh | <7:0> | 8-bit Component ID Version |
| Silicon Revision | 8 | R | 0E | | 00h | <7:0> | 8-bit Silicon Revision |
| Control_register_1 | | | | | | | |
| Idle | 1 | R/W | 0Fh | | 1b | <7> | 1: Idle mode 0: Low Power mode |
| Low_power_timebase | 3 | R/W | 0Fh | | 111b | <6:4> | Low Power readout time base register |
| INT_disable | 1 | R/W | 0Fh | | 0b | <3> | Disables the interrupt functionality. 1: Interrupt disabled 0: Interrupt enabled |
| INT_function | 1 | R/W | 0Fh | | 0b | <2> | Interrupt control register 0: Interrupt goes low with every new calculated x/y coordinates 1: Interrupt pin goes low in when new x/y coordinates are calculated and the magnet has exited the xp, xn, yp, yn threshold values |
| soft_rst | 1 | R/W | 0Fh | | 0b | <1> | Soft Reset 0: Normal mode 1: All registers return to their respective reset value |

| Register | Number of Bits | Access | Address | Format | Reset Value | Bit | Description |
|--------------------------------|----------------|--------|---------|-------------|--------------|----------------|--|
| data_valid | 1 | R | 0Fh | | 0b | <0> | Data valid indicator 0: X/Y calculation ongoing 1: X/Y calculation finished, coordinates ready |
| X/Y Coordinate Register | | | | | | | |
| x | 8 | R | 10h | two's comp. | 00h | <7:0> | Result |
| y_res_int | 8 | R | 11h | two's comp. | 00h | <7:0> | Result, resets the interrupt flag at the value ACK |
| Range Settings | | | | | | | |
| xp | 8 | R/W | 12h | two's comp. | 5h (5 dec) | <7:0> | Wake up threshold @ positive X-direction |
| xn | 8 | R/W | 13h | two's comp. | FBh (-5 dec) | <7:0> | Wake up threshold @ negative X-direction |
| yp | 8 | R/W | 14h | two's comp. | 5h (5 dec) | <7:0> | Wake up threshold @ positive Y-direction |
| yn | 8 | R/W | 15h | two's comp. | FBh (-5 dec) | <7:0> | Wake up threshold @ negative Y-direction |
| Channel Voltages (3) | | | | | | | |
| c4_neg <11:8> | 4 | R | 16h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 4, negative current spinning Sign extended to 8-bit |
| c4_neg <7:0> | 8 | R | 17h | two's comp. | 00h | <7:0> | Voltage @ channel 4, negative current spinning |
| c4_pos <11:8> | 4 | R | 18h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 4, positive current spinning Sign extended to 8-bit |
| c4_pos <7:0> | 8 | R | 19h | two's comp. | 00h | <7:0> | Voltage @ channel 4, positive current spinning |

| Register | Number of Bits | Access | Address | Format | Reset Value | Bit | Description |
|------------------|----------------|--------|---------|-------------|-------------|----------------|--|
| c3_neg <11:8> | 4 | R | 1Ah | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 3, negative current spinning Sign extended to 8-bit |
| c3_neg <7:0> | 8 | R | 1Bh | two's comp. | 00h | <7:0> | Voltage @ channel 3, negative current spinning |
| c3_pos <11:8> | 4 | R | 1Ch | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 3, positive current spinning Sign extended to 8-bit |
| c3_pos <7:0> | 8 | R | 1Dh | two's comp. | 00h | <7:0> | Voltage @ channel 3, positive current spinning |
| c2_neg <11:8> | 4 | R | 1Eh | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 2, negative current spinning Sign extended to 8-bit |
| c2_neg <7:0> | 8 | R | 1Fh | two's comp. | 00h | <7:0> | Voltage @ channel 2, negative current spinning |
| c2_pos <11:8> | 4 | R | 20h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 2, positive current spinning Sign extended to 8-bit |
| c2_pos <7:0> | 8 | R | 21h | two's comp. | 00h | <7:0> | Voltage @ channel 2, positive current spinning |
| c1_neg <11:8> | 4 | R | 22h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 1, negative current spinning Sign extended to 8-bit |
| c1_neg <7:0> | 8 | R | 23h | two's comp. | 00h | <7:0> | Voltage @ channel 1, negative current spinning |

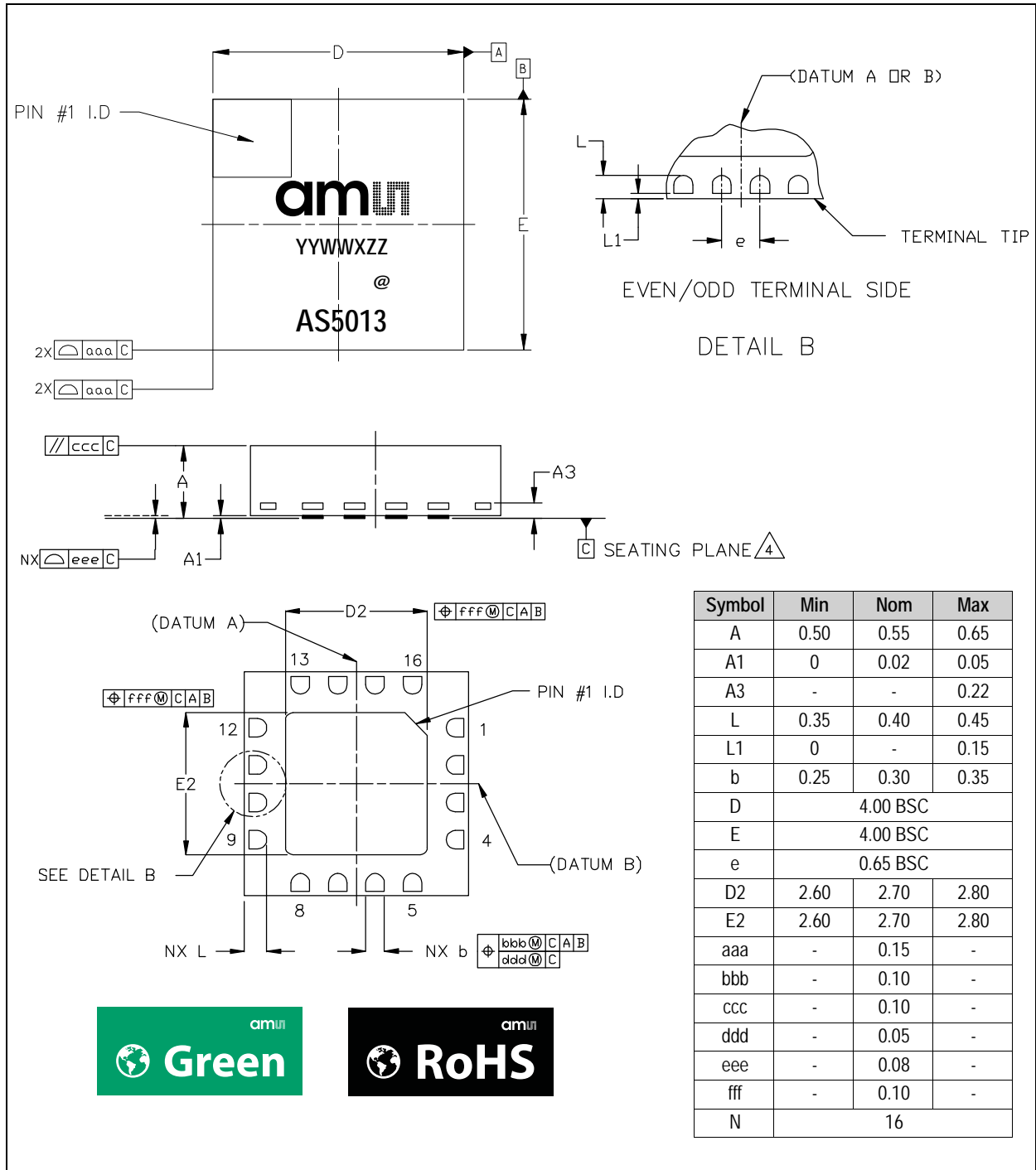
| Register | Number of Bits | Access | Address | Format | Reset Value | Bit | Description |
|---------------------------|----------------|--------|---------|-------------|-------------|----------------|--|
| c1_pos <11:8> | 4 | R | 24h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 1, positive current spinning Sign extended to 8-bit |
| c1_pos <7:0> | 8 | R | 25h | two's comp. | 00h | <7:0> | Voltage @ channel 1, positive current spinning |
| | | | | | | | |
| c5_neg <11:8> | 4 | R | 26h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 5, negative current spinning Sign extended to 8-bit |
| c5_neg <7:0> | 8 | R | 27h | two's comp. | 00h | <7:0> | Voltage @ channel 5, negative current spinning |
| c5_pos <11:8> | 4 | R | 28h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 5, positive current spinning Sign extended to 8-bit |
| c5_pos <7:0> | 8 | R | 29h | two's comp. | 00h | <7:0> | Voltage @ channel 5, positive current spinning |
| Hall Bias Currents | | | | | | | |
| AGC | 8 | RW | 2Ah | | 00b 20h | <7:6> <5:0> | Not implemented (read 00b) 6-bit AGC value (if an AGC algorithm implemented in the μ C) |

| Register | Number of Bits | Access | Address | Format | Reset Value | Bit | Description |
|---|----------------|--------|---------|--------|-------------|-------|---|
| Control Register for the Algorithm | | | | | | | |
| M_ctrl | 8 | R/W | 2Bh | | 00h | <7:0> | Control register for the middle Hall element C5. If the register is zero the middle Hall element is not used for the XY calculation |
| J_ctrl | 8 | R/W | 2Ch | | 06h | <7:0> | Control register for the sector dependent attenuation of the outer Hall elements |
| T_ctrl | 8 | R/W | 2Dh | | 09h | <7:0> | Scale input to fit to the 8-bit result register |
| Control_register_2 | | | | | | | |
| Test | 1 | R/W | 2Eh | | 1b | <7> | Test only, must be '1' |
| Test | 1 | R/W | 2Eh | | 0b | <6> | Test only, must be '0' |
| Test | 1 | R/W | 2Eh | | 0b | <5> | Test only, must be '0' |
| ext_clk_en | 1 | R/W | 2Eh | | 0b | <4> | Test only, must be '0' |
| use_static_offset | 1 | R/W | 2Eh | | 0b | <3> | Test only, must be '0' |
| EN_offset_comp | 1 | R/W | 2Eh | | 1b | <2> | Test only, must be '1' |
| inv_spinning | 1 | R/W | 2Eh | | 0b | <1> | Invert the channel voltage. Set to invert the magnet polarity |
| pptrim_en | 1 | R/W | 2Eh | | 0b | <0> | Factory only, must be '0' |

Package Drawings & Markings

The device is available in a 16-pin QFN (4mmx4mmx0.55mm) package.

Figure 40:
Drawings and Dimensions



Note(s):

1. Dimensioning & tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.
6. N is the total number of terminals.

Figure 41:
Package Marking

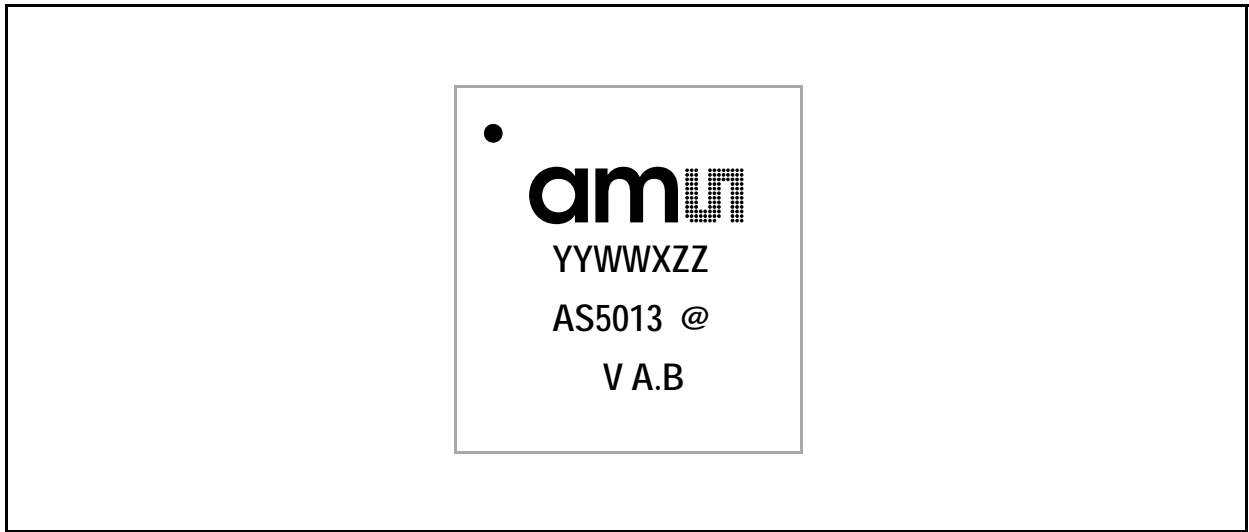
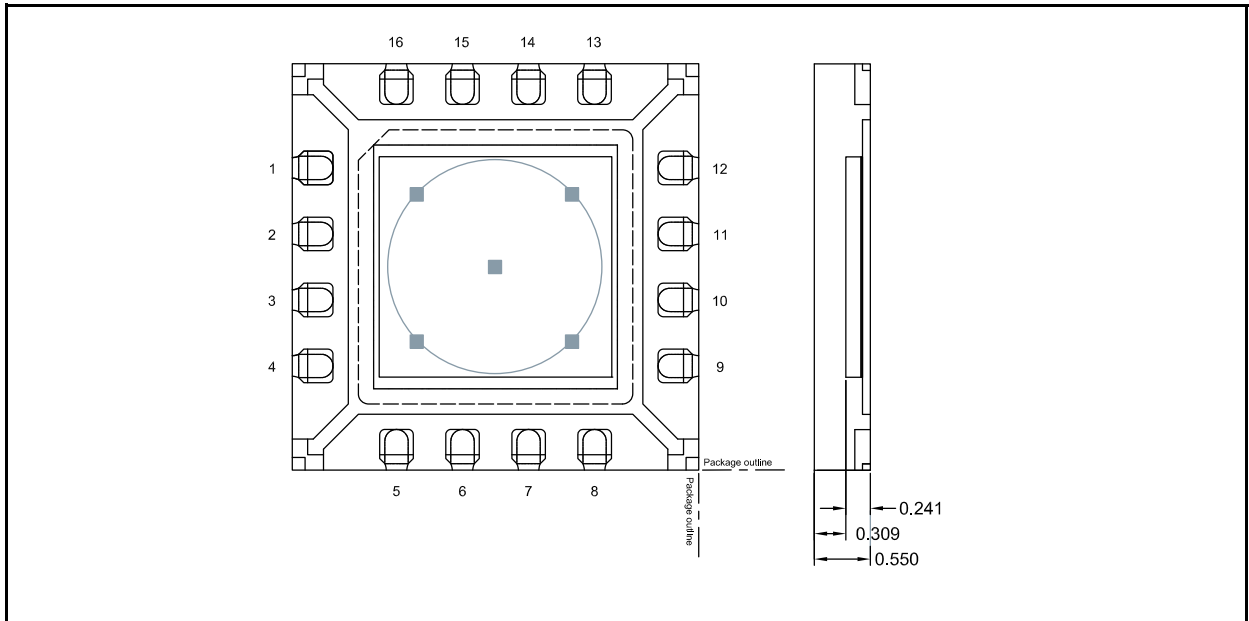


Figure 42:
Package Code: YYWWXZZ@

| YY | WW | X | ZZ | @ |
|-------------------------------------|--------------------|---------------------------|----------------------------|-------------------|
| Last two digits of the current year | Manufacturing Week | Assembly plant identifier | Assembly traceability code | Sublot identifier |

Mechanical Data

Figure 43:
Die Placement and Hall Array Position

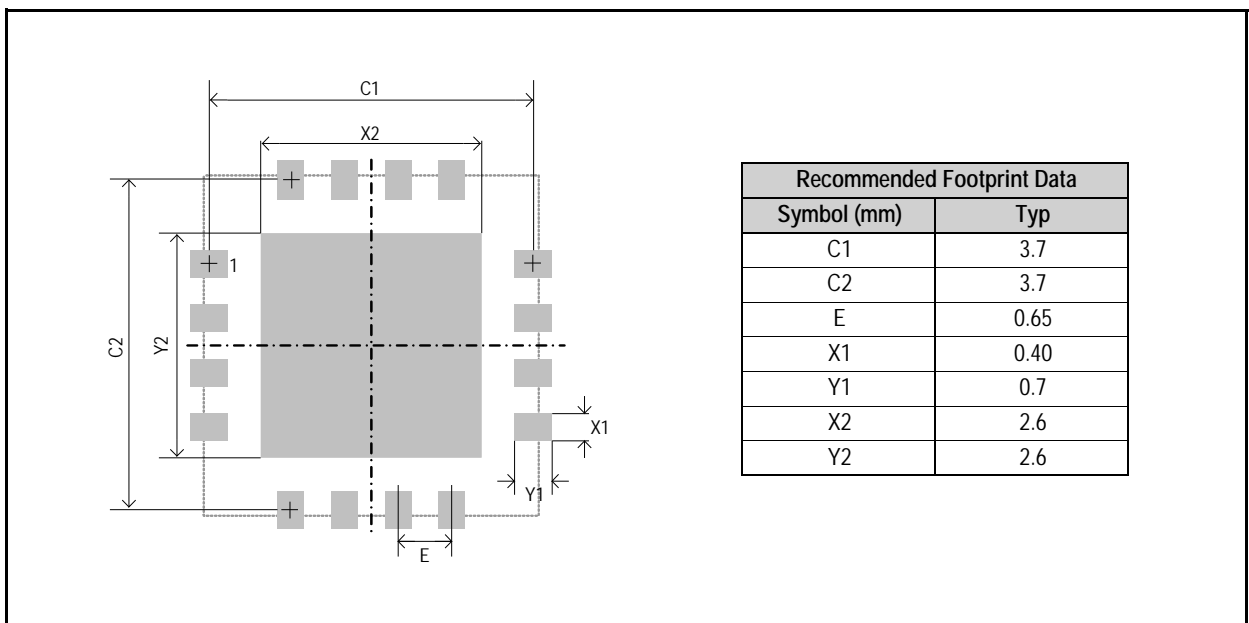


Note(s):

1. All dimensions in mm.
2. The Hall array center is located in the center of the IC package. Hall array radius is 1.1mm.
3. Die thickness is 150µm nominal.
4. Adhesive thickness 15µm nominal.
5. Leadframe thickness 76µm nominal.

Recommended Footprint

Figure 44:
Footprint



Recommended Mounting

The typical mounting configuration of the AS5013 with the mechanics is on both sides of the PCB:

- Mechanics + Magnet on the top side
- AS5013 IC on the bottom side

A thickness of 0.3mm to 1.0mm for the PCB is recommended.

A dome switch for push button function can be added as well.

Figure 45:
AS5013 Mounting Example for Low Profile Joystick

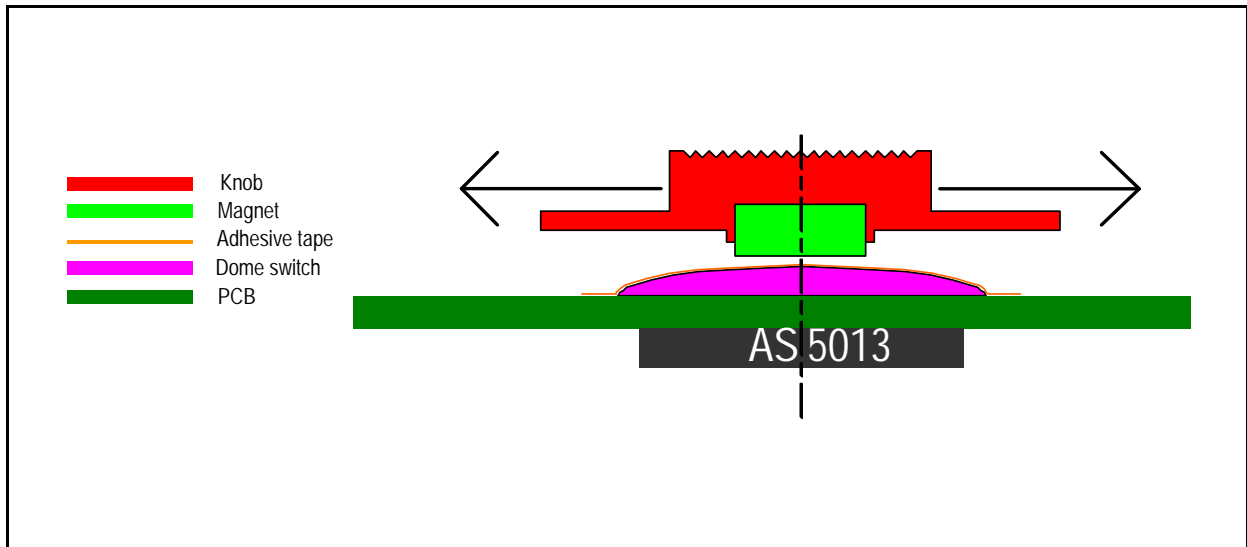
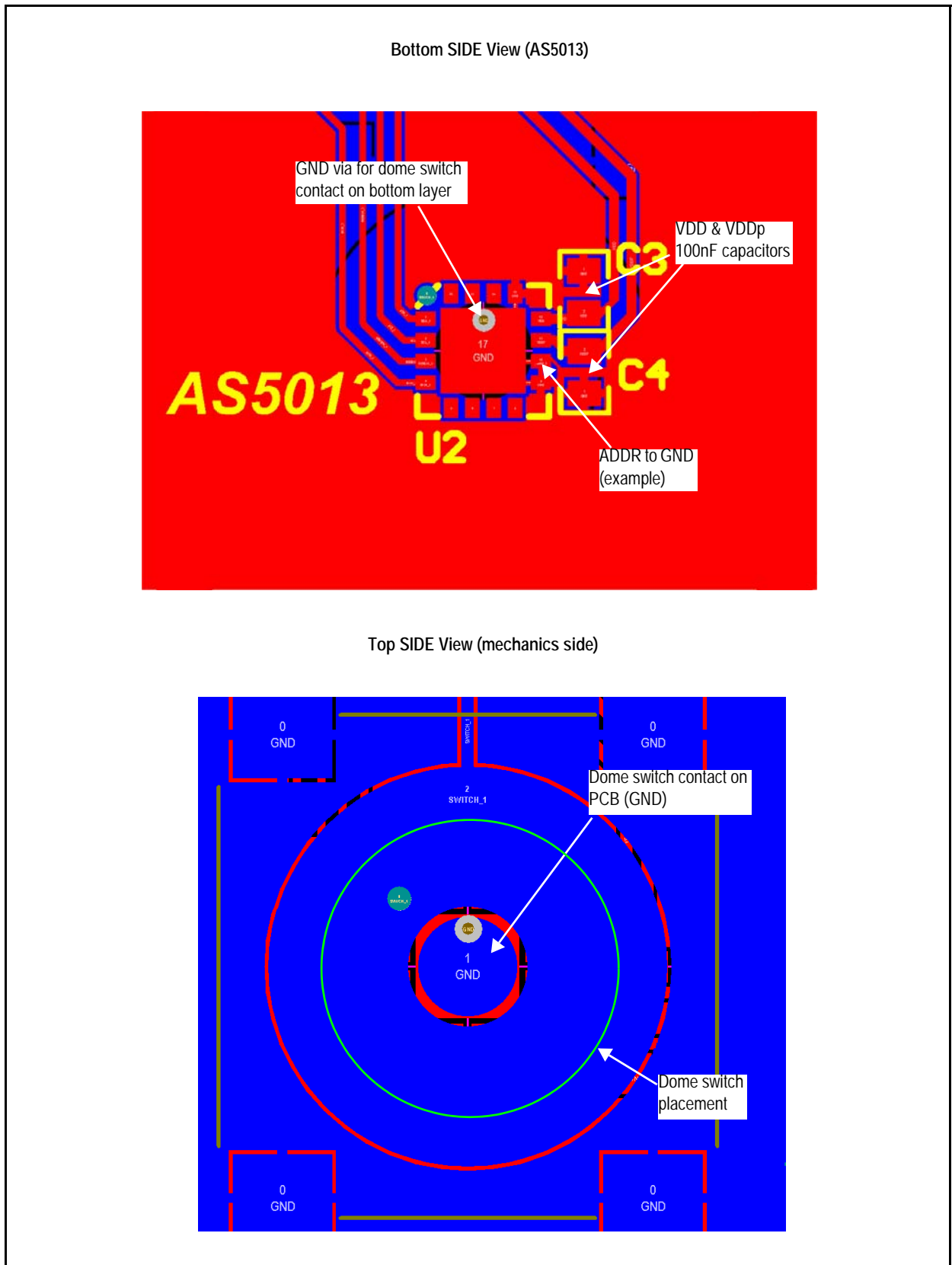


Figure 46:
Layout Example for Low Profile Joystick



Ordering & Contact Information The devices are available as the standard products shown in [Figure 47](#).

Figure 47:
Ordering Information

| Ordering Code | Package | Marking | Delivery Form |
|---------------|--------------------------------|---------|---------------|
| AS5013-IQFT | 16-pin QFN (4mmx4mmx0.55mm) | AS5013 | Tape & Reel |

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| Document Status | Product Status | Definition |
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Revision Information

| Changes from 1.15 to current revision 2-00 (2021-Apr-19) | Page |
|--|------|
| Content was updated to latest ams design | |
| Added section "Mechanical Data" | 42 |

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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