

AS5040

10-Bit 360° Programmable Magnetic Rotary Encoder

General Description

The AS5040 is a contactless magnetic rotary encoder for accurate angular measurement over a full turn of 360°. It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip, is required. The magnet may be placed above or below the IC.

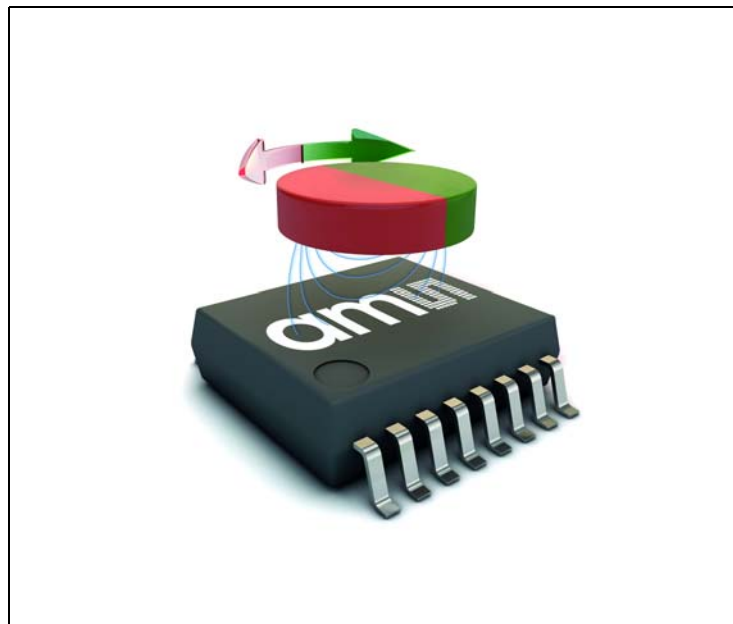
The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of $0.35^\circ = 1024$ positions per revolution. This digital data is available as a serial bit stream and as a PWM signal.

Furthermore, a user-programmable incremental output is available, making the chip suitable for replacement of various optical encoders.

An internal voltage regulator allows the AS5040 to operate at either 3.3V or 5V supplies.

[Ordering Information](#) and [Content Guide](#) appear at end of datasheet.

Figure 1:
Typical Arrangement of AS5040 and Magnet



Key Benefits & Features

The benefits and features of AS5040, 10-Bit 360° Programmable Magnetic Rotary Encoder are listed below:

Figure 2:
Added Value of Using AS5040

Benefits	Features
<ul style="list-style-type: none"> • Highest reliability and durability 	<ul style="list-style-type: none"> • Contactless high resolution rotational position encoding over a full turn of 360 degrees
<ul style="list-style-type: none"> • Simple programming 	<ul style="list-style-type: none"> • Simple user-programmable resolution, pole pairs and zero position
<ul style="list-style-type: none"> • Multiple interfaces 	<ul style="list-style-type: none"> • Serial communication interface (SSI) • 10-bit pulse width modulated (PWM) output • Quadrature A/B and Index output signal • Step/Direction and Index output signal • 3-Phase commutation for brushless DC motors
<ul style="list-style-type: none"> • Ideal for motor applications 	<ul style="list-style-type: none"> • Rational speeds up to 30000rpm
<ul style="list-style-type: none"> • Failure diagnostics 	<ul style="list-style-type: none"> • Failure detection mode for magnet placement monitoring and loss of power supply
<ul style="list-style-type: none"> • Easy setup 	<ul style="list-style-type: none"> • Serial read-out of multiple interconnected devices using daisy chain mode
<ul style="list-style-type: none"> • Great flexibility at a huge application area 	<ul style="list-style-type: none"> • Push button functionality detects movement of magnet in Z-axis
<ul style="list-style-type: none"> • Fully automotive qualified 	<ul style="list-style-type: none"> • AEC-Q100, grade 1
<ul style="list-style-type: none"> • Small form factor 	<ul style="list-style-type: none"> • SSOP 16 (5.3mm x 6.2mm)
<ul style="list-style-type: none"> • Robust environmental tolerance 	<ul style="list-style-type: none"> • Wide temperature range: -40°C to 125°C

Applications

AS5040 is ideal for:

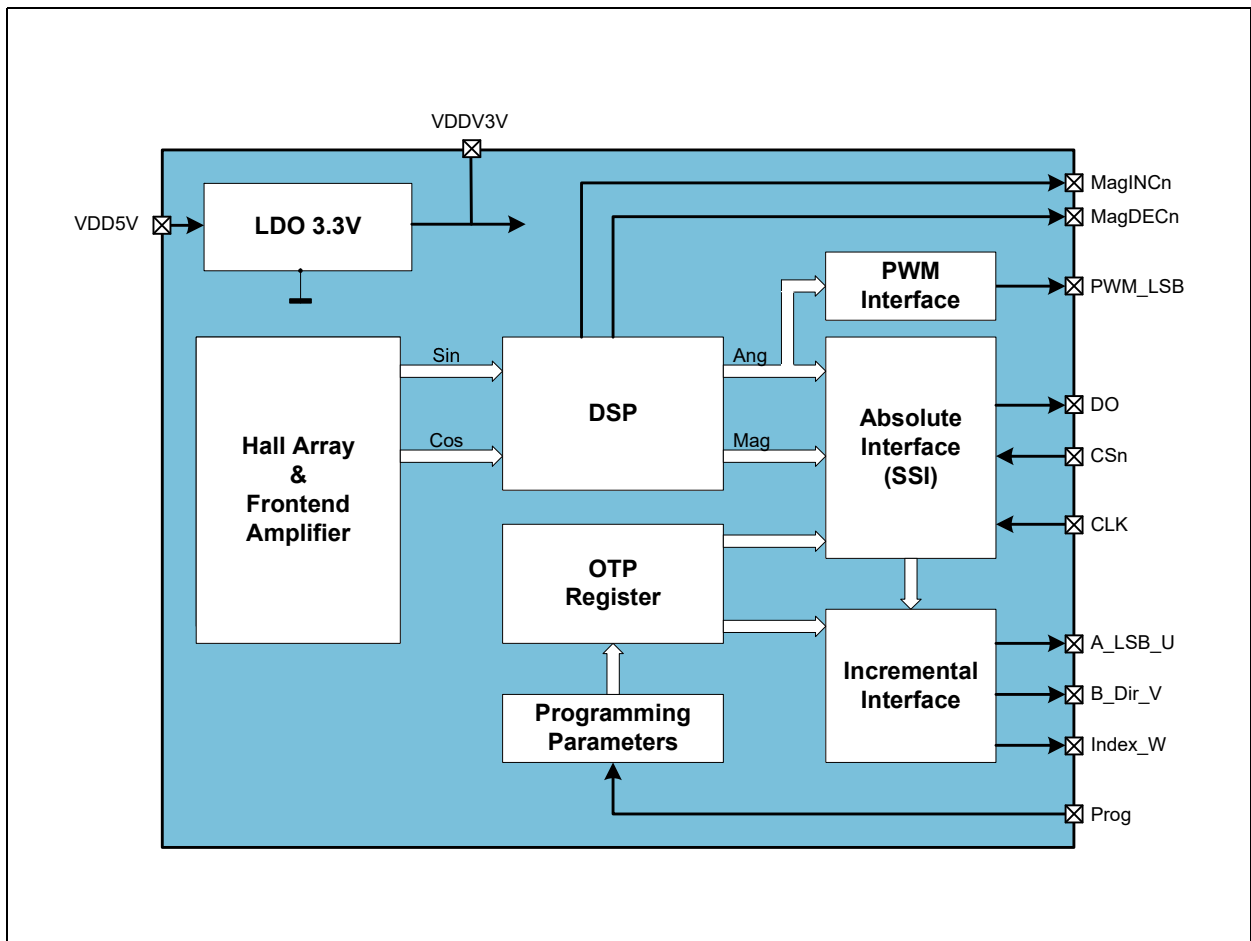
- Industrial applications:
 - Contactless rotary position sensing
 - Robotics
 - Brushless DC motor commutation
 - Power tools
- Automotive applications:
 - Steering wheel position sensing
 - Gas pedal position sensing
 - Transmission gearbox encoder
 - Headlight position control
 - Power seat position indicator

- Office equipment: Printers, scanners, copiers
- Replacement of optical encoders
- Front panel rotary switches
- Replacement of potentiometers

Block Diagram

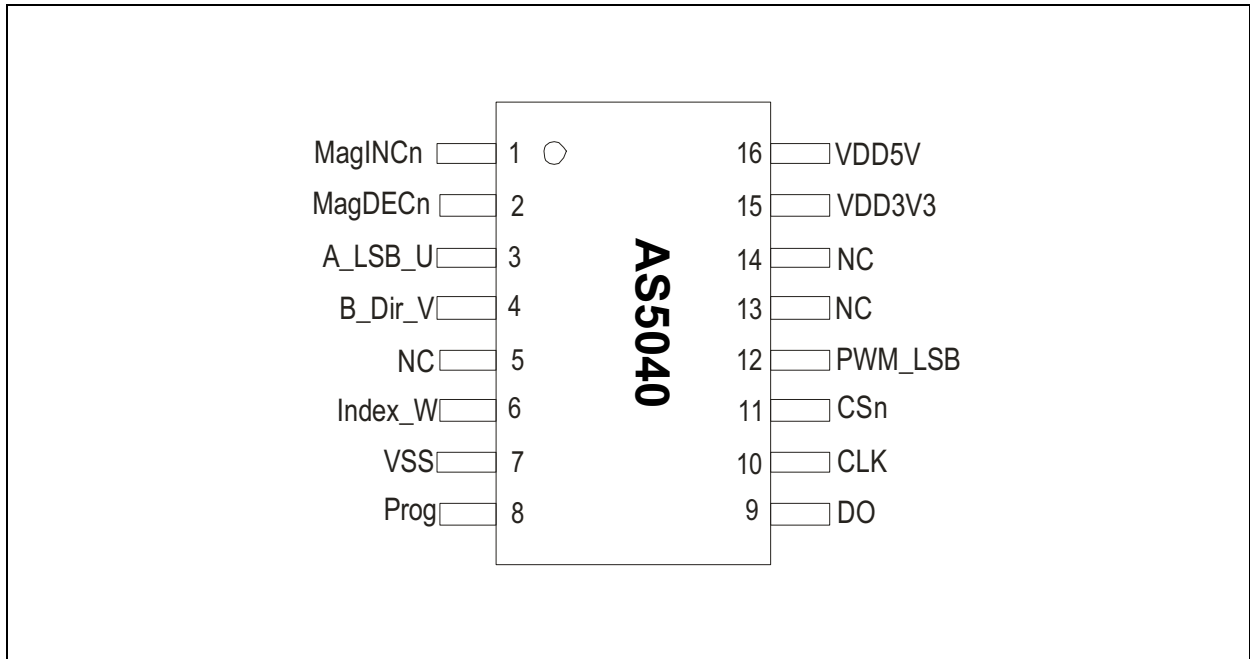
The functional blocks of this device are shown below:

Figure 3:
AS5040 Block Diagram



Pin Assignment

Figure 4:
Pin Configuration SSOP16



Pin Description

Figure 6 shows the description of each pin of the standard SSOP16 package (Shrink Small Outline Package, 16 leads, body size: 5.3mm x 6.2mm; see Figure 4).

Pins 7, 15 and 16 are supply pins, pins 5, 13 and 14 are for internal use and must not be connected.

Pins 1 and 2 are the magnetic field change indicators, MagINCn and MagDECn (magnetic field strength increase or decrease through variation of the distance between the magnet and the device). These outputs can be used to detect the valid magnetic field range. Furthermore those indicators can also be used for contact-less push-button functionality.

Pins 3, 4 and 6 are the incremental pulse output pins. The functionality of these pins can be configured through programming the one-time programmable (OTP) register.

Figure 5:
Pin Assignment for the Different Incremental Output Modes

Output Mode	Pin 3	Pin 4	Pin 6	Pin 12
1.x: Quadrature	A	B	Index	PWM
2.x: Step/Direction	LSB	Direction	Index	PWM
3.x: Commutation	U	V	W	LSB

Mode 1.x: Quadrature A/B Output

Represents the default quadrature A/B signal mode.

Mode 2.x: Step / Direction Output

Configures pin 3 to deliver up to 512 pulses (up to 1024 state changes) per revolution. It is equivalent to the LSB (least significant bit) of the absolute position value. Pin 4 provides the information of the rotational direction.

Both modes (mode 1.x and mode 2.x) provide an index signal (1 pulse/revolution) with an adjustable width of one LSB or three LSB's.

Mode 3.x: Brushless DC Motor Commutation Mode

In addition to the absolute encoder output over the SSI interface, this mode provides commutation signals for brushless DC motors with either one pole pair or two pole pair rotors. The commutation signals are usually provided by 3 discrete Hall switches, which are no longer required, as the AS5040 can fulfill two tasks in parallel: absolute encoder + BLDC motor commutation.

In this mode, pin 12 provides the LSB output instead of the PWM (Pulse-Width-Modulation) signal.

Pin 8 (Prog) is also used to program the different incremental interface modes, the incremental resolution and the zero position into the [OTP](#).

This pin is also used as digital input to shift serial data through the device in [Daisy Chain configuration](#).

Pin 11 Chip Select (CS_n; active low) selects a device within a network of AS5040 encoders and initiates serial data transfer. A logic high at CS_n puts the data output pin (DO) to tri-state and terminates serial data transfer. This pin is also used for [Alignment Mode](#) and [Programming the AS5040](#).

Pin 12 allows a single wire output of the 10-bit absolute position value. The value is encoded into a pulse width modulated signal with 1µs pulse width per step (1µs to 1024µs over a full turn). By using an external low pass filter, the digital PWM signal is converted into an analog voltage, allowing a direct replacement of potentiometers.

Figure 6:
Pin Description SSOP16

Pin	Symbol	Type	Description
1	MagINCn	DO_OD	Magnet Field Magn itude INC rease; active low, indicates a distance reduction between the magnet and the device surface.
2	MagDECn	DO_OD	Magnet Field Magn itude DEC rease; active low, indicates a distance increase between the device and the magnet.

Pin	Symbol	Type	Description
3	A_LSB_U	DO	<i>Mode1.x:</i> Quadrature A channel <i>Mode2.x:</i> Least Significant Bit <i>Mode3.x:</i> U signal (phase1)
4	B_Dir_V	DO	<i>Mode1.x:</i> Quadrature B channel quarter period shift to channel A. <i>Mode2.x:</i> Direction of Rotation <i>Mode3.x:</i> V signal (phase2)
5	NC	-	Must be left unconnected
6	Index_W	DO	<i>Mode1.x and Mode2.x:</i> Index signal indicates the absolute zero position <i>Mode3.x:</i> W signal (phase3)
7	VSS	S	Negative Supply Voltage (GND)
8	Prog	DI_PD	OTP Programming Input and Data Input for Daisy Chain mode. Internal pull-down resistor (~74kΩ). May be connected to VSS if programming is not used
9	DO	DO_T	Data Output of Synchronous Serial Interface
10	CLK	DI, ST	Clock Input of Synchronous Serial Interface; Schmitt-Trigger input
11	CSn	DI_PU, ST	Chip Select , active low; Schmitt-Trigger input, internal pull-up resistor (~50kΩ) connect to VSS in incremental mode (see 0)
12	PWM_LSB	DO	Pulse Width Modulation of approx. 1kHz; LSB in <i>Mode3.x</i>
13	NC	-	Must be left unconnected
14	NC	-	Must be left unconnected
15	VDD3V3	S	3V-Regulator Output (see Figure 39)
16	VDD5V	S	Positive Supply Voltage 5 V

Abbreviations for Pin Types in [Figure 6](#):

DO_OD	: Digital output open drain
DO	: Digital output
DI_PD	: Digital input pull-down
DI_PU	: Digital input pull-up
S	: Supply pin
DI	: Digital input
DO_T	: Digital output /tri-state
ST	: Schmitt-Trigger input

Absolute Maximum Ratings

Stresses beyond those listed in [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in [Operating Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
VDD5V	DC supply voltage at pin VDD5V	-0.3	7	V	
VDD3V3	DC supply voltage at pin VDD3V3	-0.3	5	V	
V _{in}	Input pin voltage	-0.3	VDD5V +0.3	V	Pins MagINCn, MagDECn, CLK, CSn
		-0.3	7.5		Pin Prog
I _{scr}	Input current (latchup immunity)	-100	100	mA	JEDEC 78
ESD	Electrostatic discharge	±2		kV	MIL 883 method 3015
T _{strg}	Storage temperature	-65	150	°C	Min – 67°F, Max 257°F
T _{Body}	Body temperature (Lead free package)		260	°C	t=20s to 40s, IPC/JEDEC J-Std-020 Lead finish 100% Sn “matte tin”
RH _{NC}	Relative humidity (non condensing)	5	85	%	
MSL	Moisture sensitivity level	3			Maximum floor life time of 168h

Electrical Characteristics

Operating Conditions

Figure 8:
Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{amb}	Ambient temperature	-40		125	°C	-40°F to 257°F
I_{supp}	Supply current		16	21	mA	
VDD5V VDD3V3	External supply voltage at pin VDD5V Internal regulator output voltage at pin VDD3V3	4.5 3.0	5.0 3.3	5.5 3.6	V V	5V operation
VDD5V VDD3V3	External supply voltage at pin VDD5V, VDD3V3	3.0 3.0	3.3 3.3	3.6 3.6	V V	3.3V operation (pins VDD5V and VDD3V3 connected)

DC Characteristics for Digital Inputs and Outputs

CMOS Schmitt-Trigger Inputs: CLK, CSn (CSn = Internal Pull-Up)

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C ,
 $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Figure 9:
CMOS Schmitt-Trigger Inputs: CLK, CSn (CSn = Internal Pull-Up)

Symbol	Parameter	Min	Max	Unit	Note
V_{IH}	High level input voltage	$0.7 * V_{DD5V}$		V	Normal operation
V_{IL}	Low level input voltage		$0.3 * V_{DD5V}$	V	
$V_{I_{on}} - V_{I_{off}}$	Schmitt trigger hysteresis	1		V	
I_{LEAK}	Input leakage current	-1	1	μA	CLK only
I_{iL}	Pull-up low level input current	-30	-100		CSn only, VDD5V: 5.0V

CMOS / Program Input: Prog

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Figure 10:
CMOS / Program Input: Prog

Symbol	Parameter	Min	Max	Unit	Note
V_{IH}	High level input voltage	$0.7 * V_{DD5V}$	5	V	
V_{PROG}	High level input voltage	See Programming Conditions		V	During programming
V_{IL}	Low level input voltage		$0.3 * V_{DD5V}$	V	
I_{iL}	Pull-down high level input current		100	μA	$V_{DD5V}: 5.5\text{V}$

CMOS Output Open Drain: MagINCn, MagDECn

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Figure 11:
CMOS Output Open Drain: MagINCn, MagDECn

Symbol	Parameter	Min	Max	Unit	Note
V_{OL}	Low level output voltage		$V_{SS}+0.4$	V	
I_O	Output current		4 2	mA	$V_{DD5V}: 4.5\text{V}$ $V_{DD5V}: 3\text{V}$
I_{OZ}	Open drain leakage current		1	μA	

CMOS Output: A, B, Index, PWM

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Figure 12:
CMOS Output: A, B, Index, PWM

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	High level output voltage	$V_{DD5V}-0.5$		V	
V_{OL}	Low level output voltage		$V_{SS}+0.4$	V	
I_O	Output current		4 2	mA	$V_{DD5V}: 4.5\text{V}$ $V_{DD5V}: 3\text{V}$

Tristate CMOS Output: DO

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Figure 13:
Tristate CMOS Output: DO

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	High level output voltage	$V_{DD5V}-0.5$		V	
V_{OL}	Low level output voltage		$V_{SS}+0.4$	V	
I_O	Output current		4 2	mA	$V_{DD5V}: 4.5\text{V}$ $V_{DD5V}: 3\text{V}$
I_{OZ}	Tri-state leakage current		1	μA	

Magnetic Input Specification

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $VDD5V = 3.0\text{V}$ to 3.6V (3V operation) $VDD5V = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Two-pole cylindrical diametrically magnetized source:

Figure 14:
Magnetic Input Specification

Symbol	Parameter	Min	Typ	Max	Unit	Note
d_{mag}	Diameter	4	6		mm	Recommended magnet: \varnothing 6mm x 2.5mm for cylindrical magnets
t_{mag}	Thickness	2.5			mm	
B_{pk}	Magnetic input field amplitude	45		75	mT	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm
B_{off}	Magnetic offset			± 10	mT	Constant magnetic stray field
	Field non-linearity			5	%	Including offset gradient
f_{mag_abs}	Input frequency (rotational speed of magnet)			10	Hz	Absolute mode: 600 rpm @ readout of 1024 positions (see Figure 36)
f_{mag_inc}				500	Hz	Incremental mode: no missing pulses at rotational speeds of up to 30000 rpm (see Figure 36)
Disp	Displacement radius			0.25	mm	Max. X-Y offset between defined IC package center and magnet axis (see Figure 41)
				0.485		Max. X-Y offset between chip center and magnet axis.
	Chip placement tolerance			± 0.235	mm	Placement tolerance of chip within IC package (see Figure 43)
	Recommended magnet material and temperature drift		-0.12		%K	NdFeB (Neodymium Iron Boron)
			-0.035			SmCo (Samarium Cobalt)

Electrical System Specifications

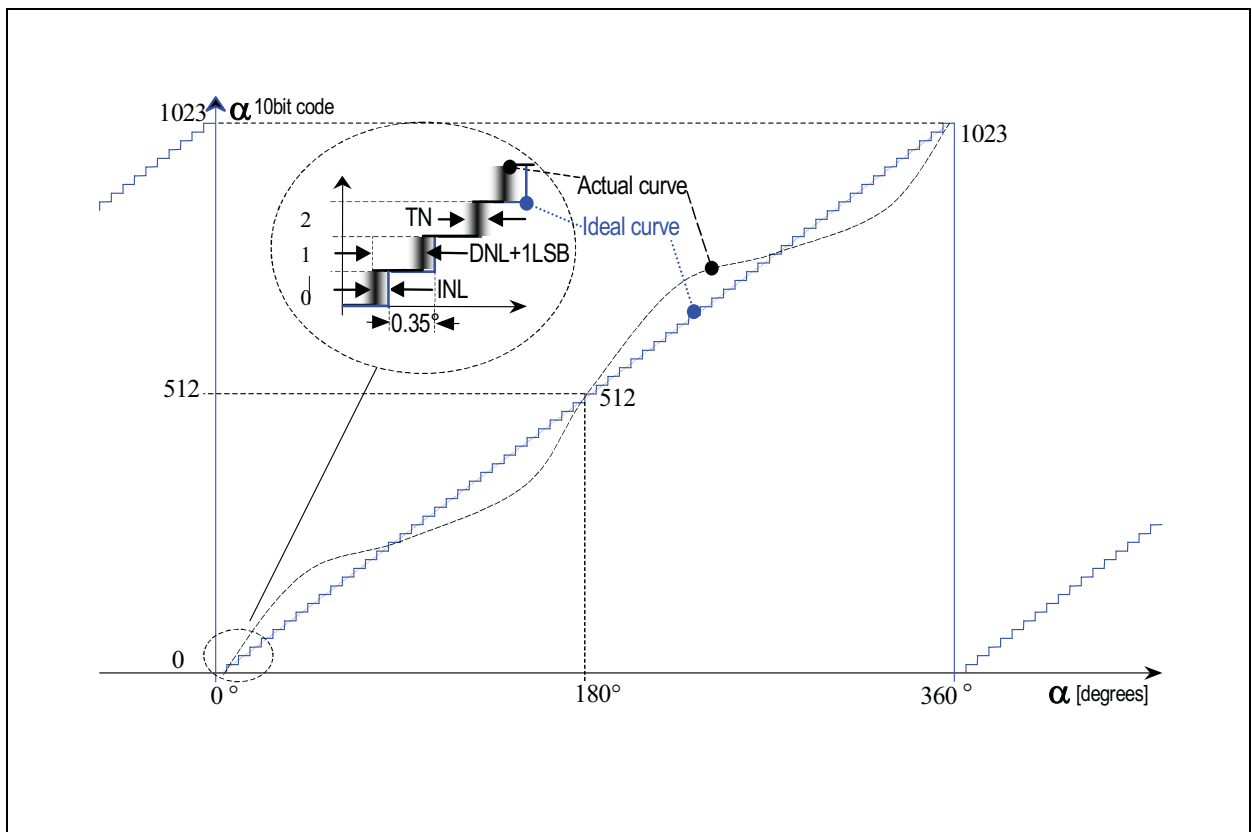
Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Figure 15:
Electrical System Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
RES	Resolution			10	bit	0.352deg
LSB	7-bit 8-bit 9-bit 10-bit		2.813 1.406 0.703 0.352		deg	Adjustable resolution only available for incremental output modes; Least significant bit, minimum step
INL_{opt}	Integral non-linearity (optimum)			± 0.5	deg	Maximum error with respect to the best line fit. Verified at optimum magnet placement, $T_{amb} = 25^{\circ}\text{C}$.
INL_{temp}	Integral non-linearity (optimum)			± 0.9	deg	Maximum error with respect to the best line fit. Verified at optimum magnet placement, $T_{amb} = -40^{\circ}\text{C}$ to 125°C
INL	Integral non-linearity			± 1.4	deg	Best line fit = $(Err_{max} - Err_{min}) / 2$ Over displacement tolerance with 6mm diameter magnet, $T_{amb} = -40^{\circ}\text{C}$ to 125°C
DNL	Differential non-linearity			± 0.176	deg	10-bit, no missing codes
TN	Transition noise			0.12	Deg RMS	RMS equivalent to 1 sigma
Hyst	Hysteresis		0.704		deg	Incremental modes only
V_{on}	Power-on-reset threshold ON voltage; 300mV typ. hysteresis	1.37	2.2	2.9	V	DC supply voltage 3.3V (VDD3V3)
V_{off}	Power-on-reset threshold OFF voltage; 300mV typ. hysteresis	1.08	1.9	2.6	V	DC supply voltage 3.3V (VDD3V3)
t_{PwrUp}	Power-up time			50	ms	Until offset compensation finished
t_{delay}	System propagation delay absolute output			48	μs	Includes delay of ADC and DSP
	System propagation delay incremental output			192	μs	Calculation over two samples

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_s	Sampling rate for absolute output	9.90	10.42	10.94	kHz	Internal sampling rate, $T_{amb} = 25^\circ\text{C}$
		9.38	10.42	11.46		Internal sampling rate, $T_{amb} = -40^\circ\text{C}$ to 125°C
CLK	Read-out frequency			1	MHz	Max. clock frequency to read out serial data

Figure 16:
Integral and Differential Non-Linearity Example (Exaggerated Curve)



Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.

Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next.

Transition Noise (TN) is the repeatability of an indicated position.

Timing Characteristics

Synchronous Serial Interface (SSI)

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Figure 17:
Synchronous Serial Interface (SSI)

Symbol	Parameter	Min	Typ	Max	Unit	Note
$t_{DO\ active}$	Data output activated (logic high)			100	ns	Time between falling edge of CSn and data output activated
$t_{CLK\ FE}$	First data shifted to output register	500			ns	Time between falling edge of CSn and first falling edge of CLK
$T_{CLK/2}$	Start of data output	500			ns	Rising edge of CLK shifts out one bit at a time
$t_{DO\ valid}$	Data output valid	357		413	ns	Time between rising edge of CLK and data output valid
$t_{DO\ tristate}$	Data output tristate			100	ns	After the last bit DO changes back to "tristate"
t_{CSn}	Pulse width of CSn	500			ns	CSn = high; To initiate read-out of next angular position
f_{CLK}	Read-out frequency	>0		1	MHz	Clock frequency to read out serial data

Pulse Width Modulation Output

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Figure 18:
Pulse Width Modulation Output

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{PWM}	PWM frequency	0.927	0.976	1.024	kHz	Signal period = $1025\mu\text{s} \pm 5\%$ at $T_{amb} = 25^{\circ}\text{C}$
		0.878	0.976	1.074		$=1025\mu\text{s} \pm 10\%$ at $T_{amb} = -40^{\circ}\text{C}$ to 125°C
PW_{MIN}	Minimum pulse width	0.90	1	1.10	μs	Position 0d; angle 0 degree
PW_{MAX}	Maximum pulse width	922	1024	1126	μs	Position 1023d; angle 359.65 degree

Incremental Outputs

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted.

Figure 19:
Incremental Outputs

Symbol	Parameter	Min	Typ	Max	Unit	Note
$t_{\text{Incremental outputs valid}}$	Incremental outputs valid after power-up			500	ns	Time between first falling edge of CS_n after power-up and valid incremental outputs
$t_{\text{Dir valid}}$	Directional indication valid			500	ns	Time between rising or falling edge of LSB output and valid directional indication

Programming Conditions

(operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C , $V_{DD5V} = 3.0\text{V}$ to 3.6V (3V operation) $V_{DD5V} = 4.5\text{V}$ to 5.5V (5V operation) unless otherwise noted).

Figure 20:
Programming Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
$t_{\text{Prog enable}}$	Programming enable time	2			μs	Time between rising edge at Prog pin and rising edge of CSn
$t_{\text{Data in}}$	Write data start	2			μs	
$t_{\text{Data in valid}}$	Write data valid	250			ns	Write data at the rising edge of CLK_{PROG}
$t_{\text{Load PROG}}$	Load programming data	3			μs	
t_{PrgR}	Rise time of V_{PROG} before CLK_{PROG}	0			μs	
t_{PrgH}	Hold time of V_{PROG} after CLK_{PROG}	0		5	μs	
CLK_{PROG}	Write data – programming CLK_{PROG}			250	kHz	
t_{PROG}	CLK pulse width	1.8	2	2.2	μs	During programming; 16 clock cycles
$t_{\text{PROG finished}}$	Hold time of V_{prog} after programming	2			μs	Programmed data is available after next power-on
V_{PROG}	Programming voltage	7.3	7.4	7.5	V	Must be switched OFF after zapping
V_{ProgOff}	Programming voltage OFF level	0		1	V	Line must be discharged to this level
I_{PROG}	Programming current			130	mA	During programming
$\text{CLK}_{\text{Aread}}$	Analog read CLK			100	kHz	Analog readback mode
$V_{\text{programmed}}$	Programmed zener voltage (log.1)			100	mV	$V_{\text{Ref}} - V_{\text{PROG}}$ during analog readback mode (see Analog Readback Mode)
$V_{\text{unprogrammed}}$	Unprogrammed zener voltage (log. 0)	1			V	

Functional Description

The AS5040 is manufactured in a CMOS standard process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip.

The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5040 provides accurate high-resolution absolute angular position information. For this purpose a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs MagINCn and MagDECn that indicate movements of the used magnet towards or away from the device's surface.

A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information (see [Figure 40](#)).

The AS5040 senses the orientation of the magnetic field and calculates a 10-bit binary code. This code can be accessed via a Synchronous Serial Interface (SSI). In addition, an absolute angular representation is given by a Pulse Width Modulated signal at pin 12 (PWM).

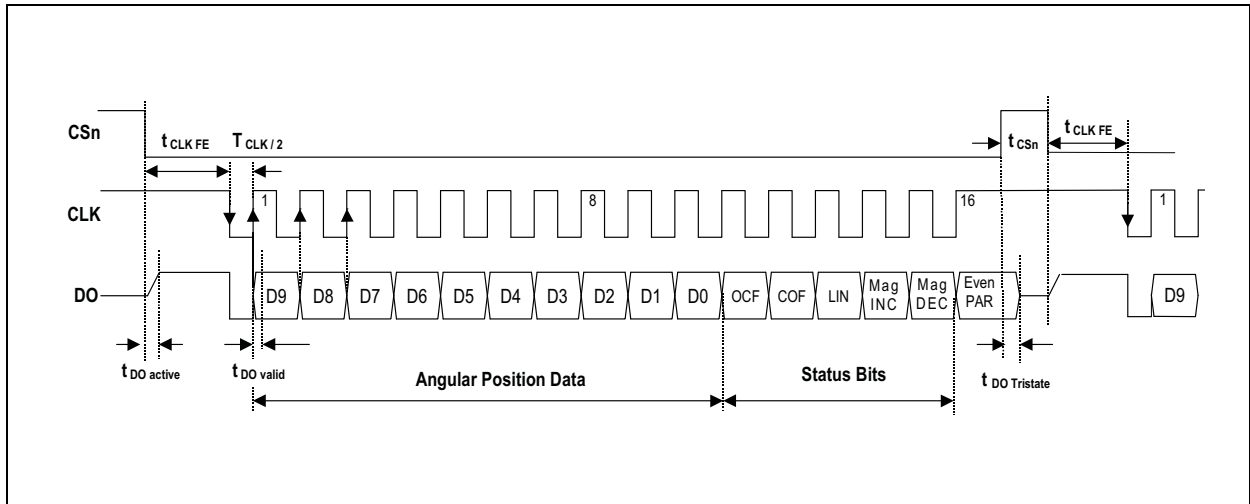
Besides the absolute angular position information the device simultaneously provides incremental output signals. The various incremental output modes can be selected by programming the OTP mode register bits (see [Figure 36](#)). As long as no programming voltage is applied to pin Prog, the new setting may be overwritten at any time and will be reset to default when power is turned OFF. To make the setting permanent, the OTP register must be programmed (see [Figure 34](#)). The default setting is a quadrature A/B mode including the Index signal with a pulse width of 1 LSB. The Index signal is logic high at the user programmable zero position.

The AS5040 is tolerant to magnet misalignment and magnetic stray fields due to differential measurement technique and Hall sensor conditioning circuitry.

10-Bit Absolute Angular Position Output

Synchronous Serial Interface (SSI)

Figure 21: Synchronous Serial Interface with Absolute Angular Position Data



If CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out will be initiated.

- After a minimum time t_{CLKFE} , data is latched into the output shift register with the first falling edge of CLK.
- Each subsequent rising CLK edge shifts out one bit of data.
- The serial word contains 16 bits, the first 10 bits are the angular information D[9:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase/decrease).
- A subsequent measurement is initiated by a log. "high" pulse at CSn with a minimum duration of t_{CSn} .

Data Content

D9:D0 absolute angular position data (MSB is clocked out first)

OCF (Offset Compensation Finished), logic high indicates the finished Offset Compensation Algorithm. For fast startup, this bit may be polled by the external microcontroller. As soon as this bit is set, the AS5040 has completed the startup and the data is valid (see [Figure 23](#))

COF (CORDIC Overflow), logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D9:D0 is invalid. The absolute output maintains the last valid angular value.

This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

LIN (Linearity Alarm), logic high indicates that the input field generates a critical output linearity. When this bit is set, the data at D9:D0 may still be used, but can contain invalid data. This warning may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

MagINCn, (Magnitude Increase) becomes HIGH, when the magnet is pushed towards the IC, thus the magnetic field strength is increasing.

MagDECn, (Magnitude Decrease) becomes HIGH, when the magnet is pulled away from the IC, thus the magnetic field strength is decreasing.

Both signals HIGH indicate a magnetic field that is out of the allowed range (see [Figure 22](#)).

Figure 22:
Magnetic Magnitude Variation Indicator

Mag INCn	Mag DECn	Description
0	0	No distance change; Magnetic input field OK (in range, 45mT to 75mT)
0	1	Distance increase: Pull-function. This state is dynamic, it is only active while the magnet is moving away from the chip in Z-axis
1	0	Distance decrease: Push- function. This state is dynamic, it is only active while the magnet is moving towards the chip in Z.-axis.
1	1	Magnetic Input Field invalid – out of range: <45mT or >75mT (or missing magnet)

Note(s):

1. Pins 1 and 2 (MagINCn, MagDECn) are open drain outputs and require external pull-up resistors. If the magnetic field is in range, both outputs are turned OFF.

The two pins may also be combined with a single pull-up resistor. In this case, the signal is high when the magnetic field is in range. It is low in all other cases (see [Figure 22](#)).

Even Parity bit for transmission error detection of bits 1 to 15 (D9 to D0, OCF, COF, LIN, MagINCn, MagDECn).

The absolute angular output is always set to a resolution of 10-bit. Placing the magnet above the chip, angular values increase in clockwise direction by default.

Data D9:D0 is valid, when the status bits have the following configurations:

Figure 23:
Status Bit Outputs

OCF	COF	LIN	Mag INCn	Mag DECn	Parity
1	0	0	0	0	Even checksum of bits 1:15
			0	1	
			1	0	

The absolute angular position is sampled at a rate of 10kHz (0.1ms). This allows reading of all 1024 positions per 360 degrees within 0.1 seconds = 9.76Hz (~10Hz) without skipping any position. Multiplying 10Hz by 60, results the corresponding maximum rotational speed of 600rpm.

Readout of every second angular position allows for rotational speeds of up to 1200rpm.

Consequently, increasing the rotational speed reduces the number of absolute angular positions per revolution (see [Figure 46](#)). Regardless of the rotational speed or the number of positions to be read out, the absolute angular value is always given at the highest resolution of 10-bit.

The incremental outputs are not affected by rotational speed restrictions due to the implemented interpolator. The incremental output signals may be used for high-speed applications with rotational speeds of up to 30000 rpm without missing pulses.

Daisy Chain Mode

The Daisy Chain mode allows connection of several AS5040's in series, while still keeping just one digital input for data transfer (see "Data IN" in [Figure 24](#) below). This mode is accomplished by connecting the data output (DO; pin 9) to the data input (Prog; pin 8) of the subsequent device. An RC filter must be implemented between each PROG pin of device n and DO pin of device n+1, to prevent the encoders to enter the alignment mode, in case of ESD discharge, long cables, or not conform signal levels or shape. Using the values $R=100R$ and $C=1nF$ allow a max. CLK frequency of 1 MHz on the whole chain. The serial data of all connected devices is read from the DO pin of the first device in the chain. The Prog pin of the last device in the chain should be connected to VSS. The length of the serial bit stream increases with every connected device, it is

$n * (16+1)$ bits:

e.g. 34-bit for two devices, 51-bit for three devices, etc...

The last data bit of the first device (Parity) is followed by a logic low bit and the first data bit of the second device (D9), etc... (see [Figure 25](#)).

Programming Daisy Chained Devices

In Daisy Chain mode, the Prog pin is connected directly to the DO pin of the subsequent device in the chain (see [Figure 24](#)). During programming (see [Programming the AS5040](#)), a programming voltage of 7.5V must be applied to pin Prog. This voltage level exceeds the limits for pin DO, so one of the following precautions must be made during programming:

- Open the connection DO -> Prog during programming or
- Add a Schottky diode between DO and Prog (Anode = DO, Cathode = Prog)

Due to the parallel connection of CLK and CSn, all connected devices may be programmed simultaneously.

Figure 24:
Daisy Chain Hardware Configuration

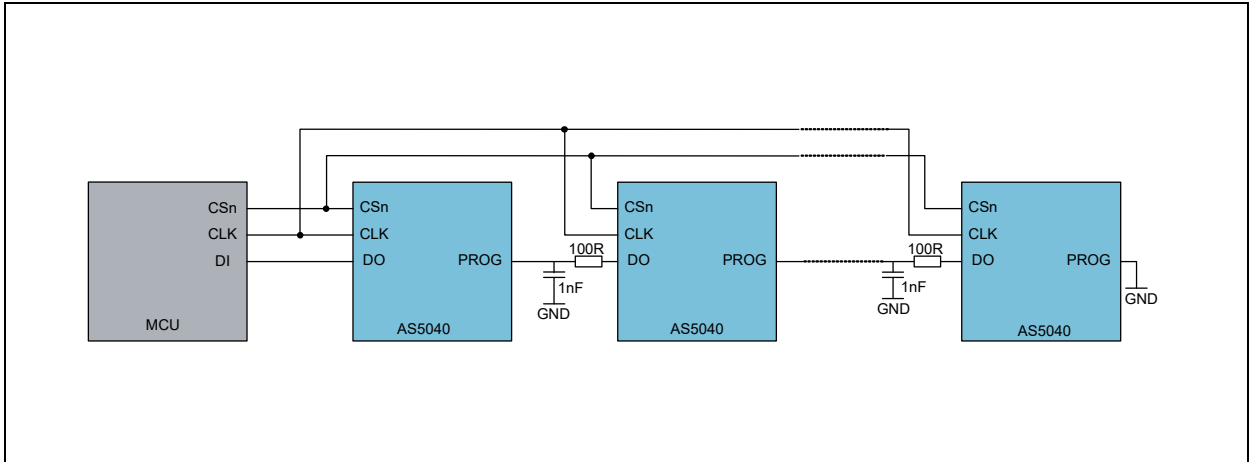
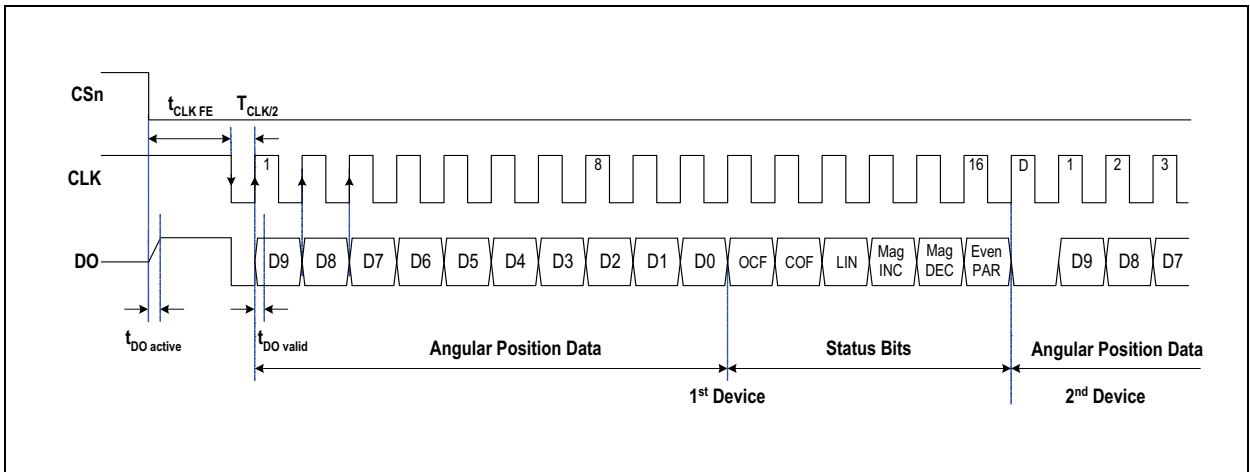


Figure 25:
Daisy Chain Mode Data Transfer



Incremental Outputs

Three different incremental output modes are possible with quadrature A/B being the default mode.

Figure 26 shows the two-channel quadrature as well as the step/direction incremental signal (LSB) and the direction bit in clockwise (CW) and counter-clockwise (CCW) direction.

Quadrature A/B Output (Quad A/B Mode)

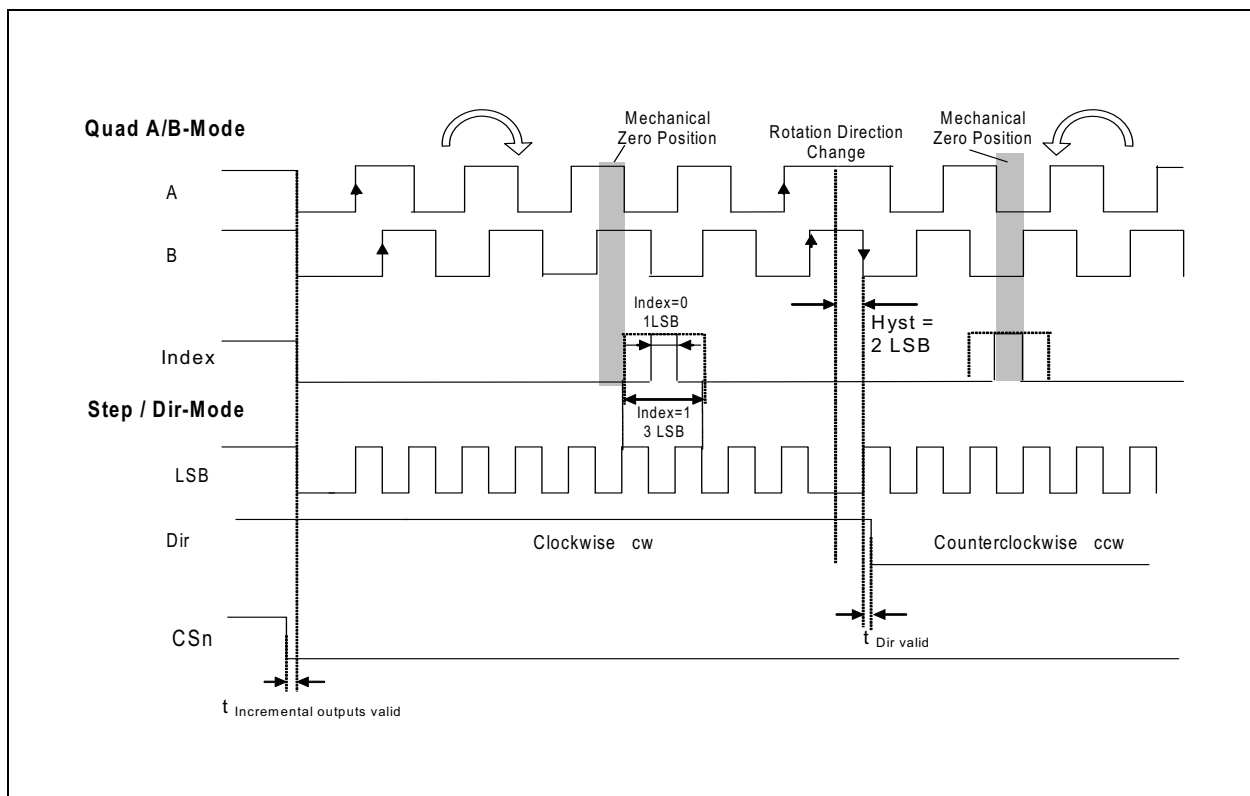
The phase shift between channel A and B indicates the direction of the magnet movement. Channel A leads channel B at a clockwise rotation of the magnet (top view) by 90 electrical degrees. Channel B leads channel A at a counter-clockwise rotation.

LSB Output (Step/Direction Mode)

Output LSB reflects the LSB (least significant bit) of the programmed incremental resolution (OTP Register Bit Div0, Div1). Output Dir provides information about the rotational direction of the magnet, which may be placed above or below the device (1=clockwise; 0=counter clockwise; top view). Dir is updated with every LSB change.

In both modes (quad A/B, step/direction) the resolution and the index output are user programmable. The index pulse indicates the zero position and is by default one angular step (1LSB) wide. However, it can be set to three LSBs by programming the Index-bit of the OTP register accordingly (see Figure 36).

Figure 26: Incremental Output Modes



Incremental Power-Up Lock Option

After power-up, the incremental outputs can optionally be locked or unlocked, depending on the status of the CSn pin:

CSn = low at power-up:

CSn has an internal pull-up resistor and must be externally pulled low ($R_{ext} \leq 5k\Omega$). If CSn is low at power-up, the incremental outputs (A, B, Index) will be high until the internal offset compensation is finished.

This unique state (A=B=Index = high) may be used as an indicator for the external controller to shorten the waiting time at power-up. Instead of waiting for the specified maximum power up-time (0), the controller can start requesting data from the AS5040 as soon as the state (A=B=Index = high) is cleared.

CSn = high or open at power-up:

In this mode, the incremental outputs (A, B, Index) will remain at logic high state, until CSn goes low or a low pulse is applied at CSn. This mode allows intentional disabling of the incremental outputs until for example the system microcontroller is ready to receive data.

Incremental Output Hysteresis

To avoid flickering incremental outputs at a stationary magnet position, a hysteresis is introduced.

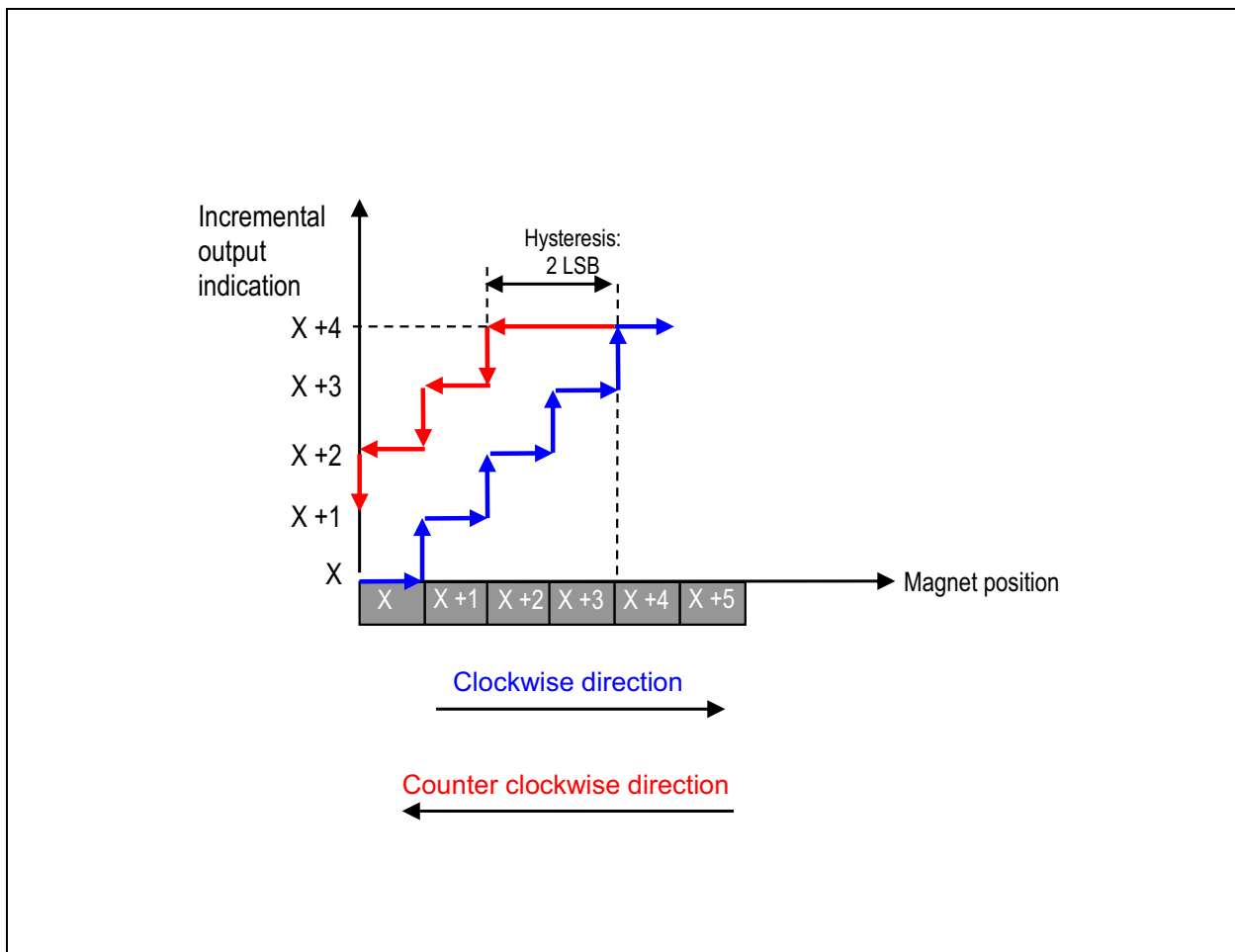
In case of a rotational direction change, the incremental outputs have a hysteresis of 2 LSB.

Regardless of the programmed incremental resolution, the hysteresis of 2 LSB always corresponds to the highest resolution of 10-bit. In absolute terms, the hysteresis is set to 0.704 degrees for all resolutions.

For constant rotational directions, every magnet position change is indicated at the incremental outputs (see Figure 27). If for example the magnet turns clockwise from position “x+3” to “x+4”, the incremental output would also indicate this position accordingly.

A change of the magnet’s rotational direction back to position “x+3” means, that the incremental output still remains unchanged for the duration of 2 LSB, until position “x+2” is reached. Following this direction, the incremental outputs will again be updated with every change of the magnet position.

Figure 27:
Hysteresis Window for Incremental Outputs



Pulse Width Modulation (PWM) Output

The AS5040 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle.

$$(EQ1) \quad \text{Position} = \frac{t_{\text{on}} \times 1025}{t_{\text{on}} + t_{\text{off}}} - 1$$

The PWM frequency is internally trimmed to an accuracy of ±5% (±10% over full temperature range). This tolerance can be canceled by measuring the complete duty cycle as shown above.

Figure 28:
PWM Output Signal

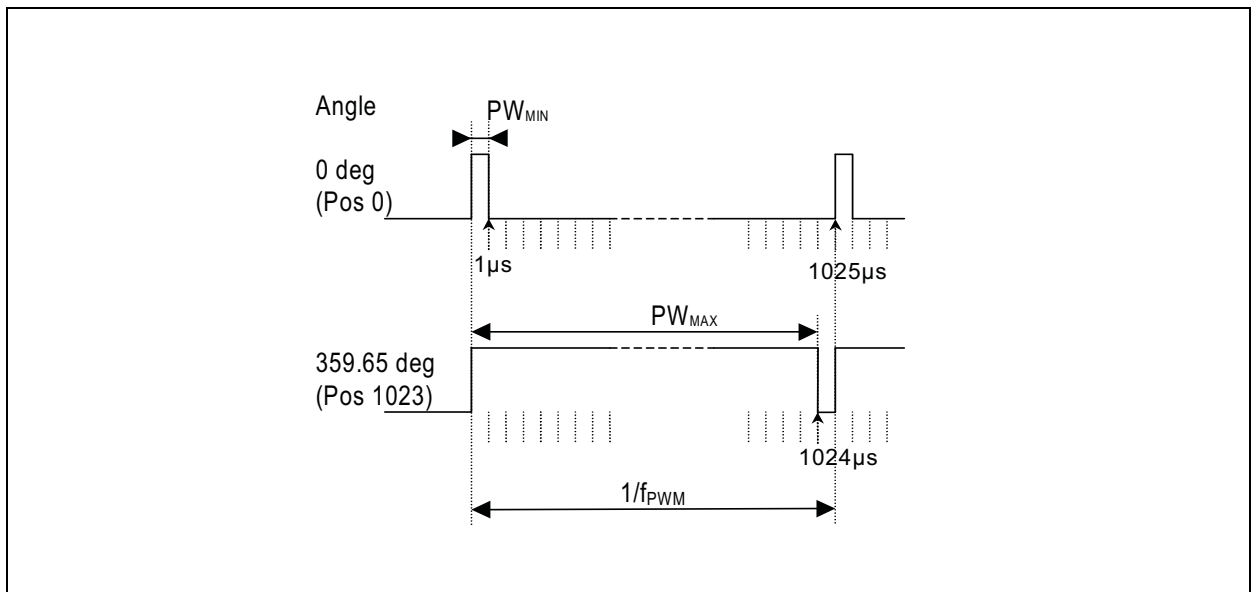


Figure 29:
PWM Signal Parameters

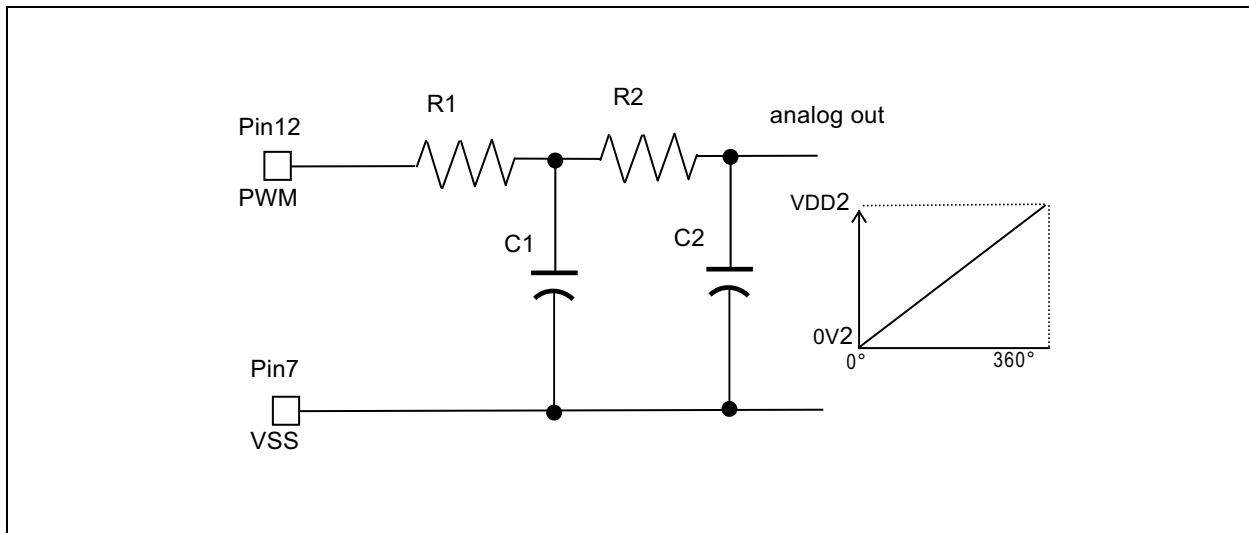
Parameter	Symbol	Typ	Unit	Note
PWM frequency	f _{PWM}	0.9756	kHz	Signal period: 1025 μs
MIN pulse width	PW _{MIN}	1	μs	<ul style="list-style-type: none"> Position 0d Angle 0 deg
MAX pulse width	PW _{MAX}	1024	μs	<ul style="list-style-type: none"> Position 1023d Angle 359.65 deg

Analog Output

An analog output can be generated by averaging the PWM signal, using an external active or passive low pass filter. The analog output voltage is proportional to the angle:
 $0^\circ = 0V$; $360^\circ = VDD5V$.

Using this method, the AS5040 can be used as direct replacement of potentiometers.

Figure 30:
Simple Passive 2nd Order RC Low Pass Filter



(EQ2) $R1, R2 \geq 4K7$ $C1, C2 \geq 1\mu F/6V$

R1 should be $\geq 4k7$ to avoid loading of the PWM output. Larger values of R_x and C_x will provide better filtering and less ripple, but will also slow down the response time.

Brushless DC Motor Commutation Mode

Brushless DC motors require angular information for stator commutation. The AS5040 provides U-V-W commutation signals for one and two pole pair motors. In addition to the three-phase output signals, the step (LSB) output at pin 12 allows high accuracy speed measurement. Two resolutions (9 or 10-bit) can be selected by programming Div0 according to [Figure 36](#).

Mode 3.0 (3.1) is used for brush-less DC motors with one-pole pair rotors. The three phases (U, V, W) are 120 degrees apart, each phase is 180 degrees ON and 180 degrees OFF.

Mode 3.2 (3.3) is used for motors with two pole pairs requiring a higher pulse count to ensure a proper current commutation. In this case the pulse width is 256 positions, equal to 90 degrees. The precise physical angle at which the U, V and W signals change state (“Angle” in [Figure 31](#) and [Figure 32](#)) is calculated by multiplying each transition position by the angular value of 1 count:

$$(EQ3) \text{ Angle [deg]} = \text{Position} \times (360 \text{ degree} / 1024)$$

Figure 31:
U, V and W-Signals for BLDC Motor Commutation (Div1=0, Div0=0)

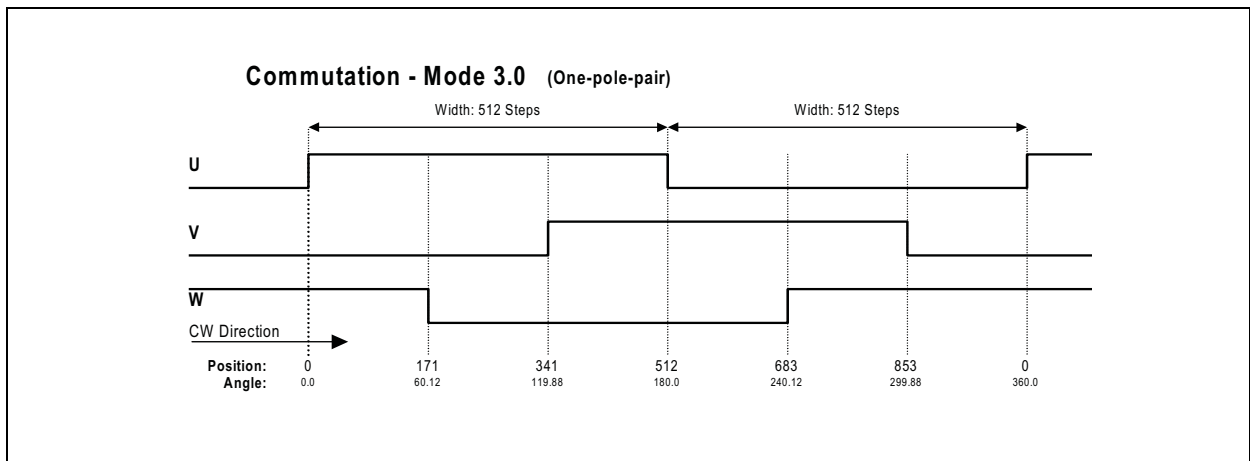
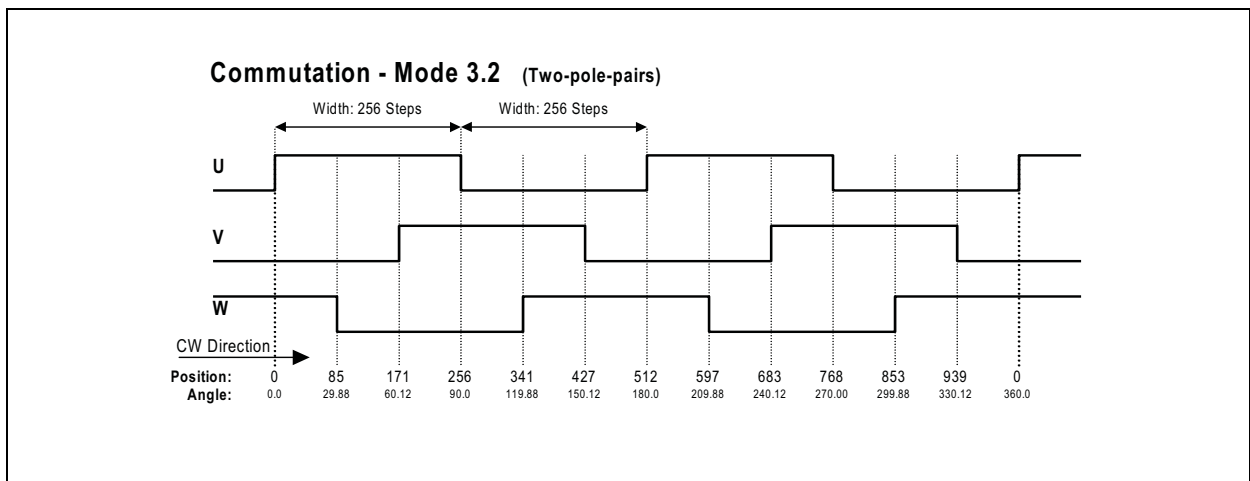


Figure 32:
U, V and W-Signals for 2-Pole BLDC Motor Commutation (Div1=1; Div0=0)



Programming the AS5040

After power-on, programming the AS5040 is enabled with the rising edge of CSn with Prog = high and CLK = low. 16-bit configuration data must be serially shifted into the OTP register via the Prog-pin. The first “CCW” bit is followed by the zero position data (MSB first) and the incremental mode setting as shown in Table 6. Data must be valid at the rising edge of CLK (see [Figure 33](#)).

After writing data into the OTP register it can be permanently programmed by rising the Prog pin to the programming voltage V_{PROG} . 16 CLK pulses (t_{PROG}) must be applied to program the fuses ([Figure 34](#)). To exit the programming mode, the chip must be reset by a power-on-reset. The programmed data is available after the next power-up.

Note(s): During the programming process, the transitions in the programming current may cause high voltage spikes generated by the inductance of the connection cable. To avoid these spikes and possible damage to the IC, the connection wires, especially the signals Prog and VSS must be kept as short as possible. The maximum wire length between the V_{PROG} switching transistor and pin Prog (see [Figure 35](#)) should not exceed 50mm (2 inches). To suppress eventual voltage spikes, a 10nF ceramic capacitor should be connected close to pins Prog and VSS. This capacitor is only required for programming, it is not required for normal operation.

The clock timing t_{CLK} must be selected at a proper rate to ensure that the signal Prog is stable at the rising edge of CLK (see [Figure 33](#)). Additionally, the programming supply voltage should be buffered with a 10 μ F capacitor mounted close to the switching transistor. This capacitor aids in providing peak currents during programming.

The specified programming voltage at pin Prog is 7.3 – 7.5V (see section 0). To compensate for the voltage drop across the V_{PROG} switching transistor, the applied programming voltage may be set slightly higher (7.5 - 8.0V, see [Figure 35](#)).

OTP Register Contents:

CCW	Counter Clockwise Bit <ul style="list-style-type: none"> • ccw=0 – angular value increases in clockwise direction • ccw=1 – angular value increases in counterclockwise direction
Z [9:0]	Programmable Zero / Index Position
Indx	Index Pulse Width Selection: 1LSB / 3LSB
Div1, Div0	Divider Setting of Incremental Output
Md1, Md0	Incremental Output Mode Selection

OTP Default Setting

The AS5040 can also be operated without programming. The default, un-programmed setting is shown in Figure 36 (Mode 0.0):

- CCW:0 = Clockwise operation
- Z9 to Z0: 00 = No programmed zero position
- Indx: 0 = Index bit width = 1LSB
- Div0, Div1: 00 = Incremental resolution = 10-bit
- Md0, MD1: 00 = Incremental mode = quadrature

Figure 33: Programming Access – Write Data (section of Figure 34)

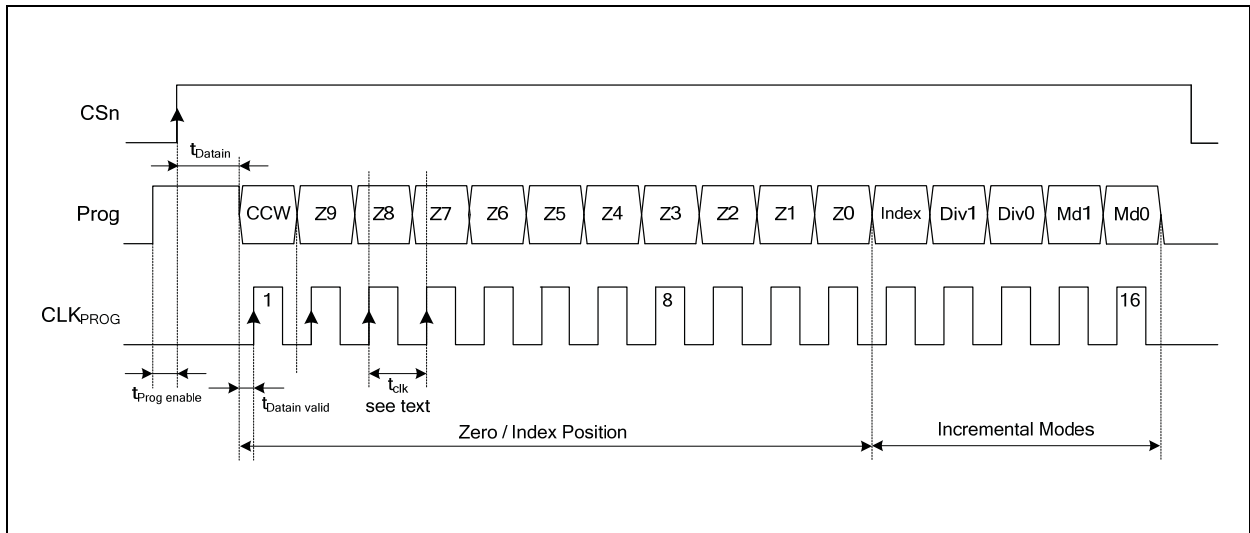


Figure 34: Complete Programming Sequence

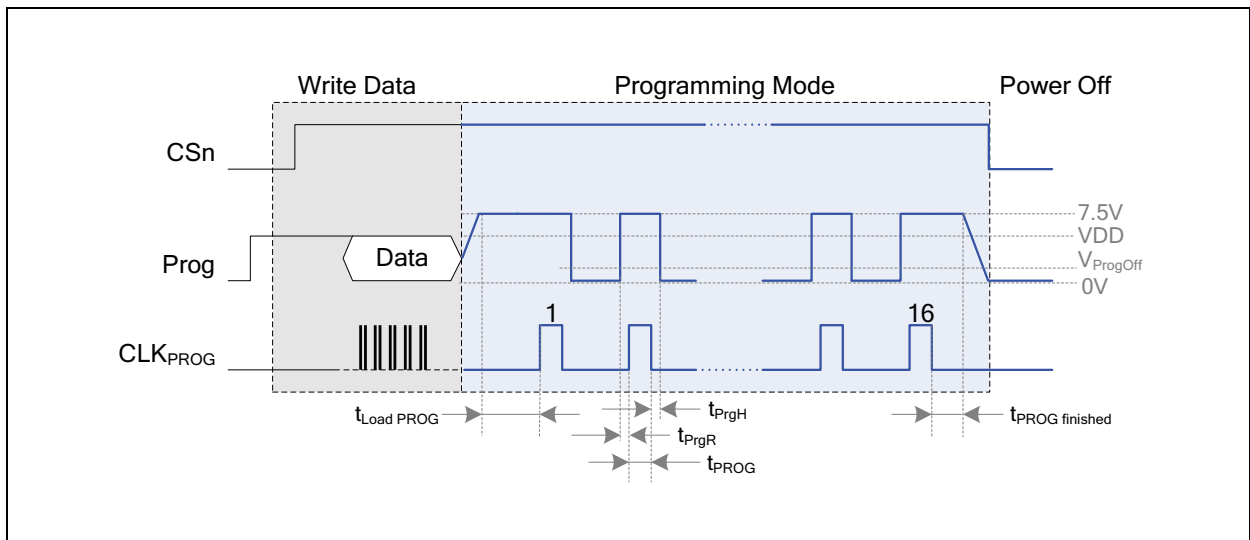
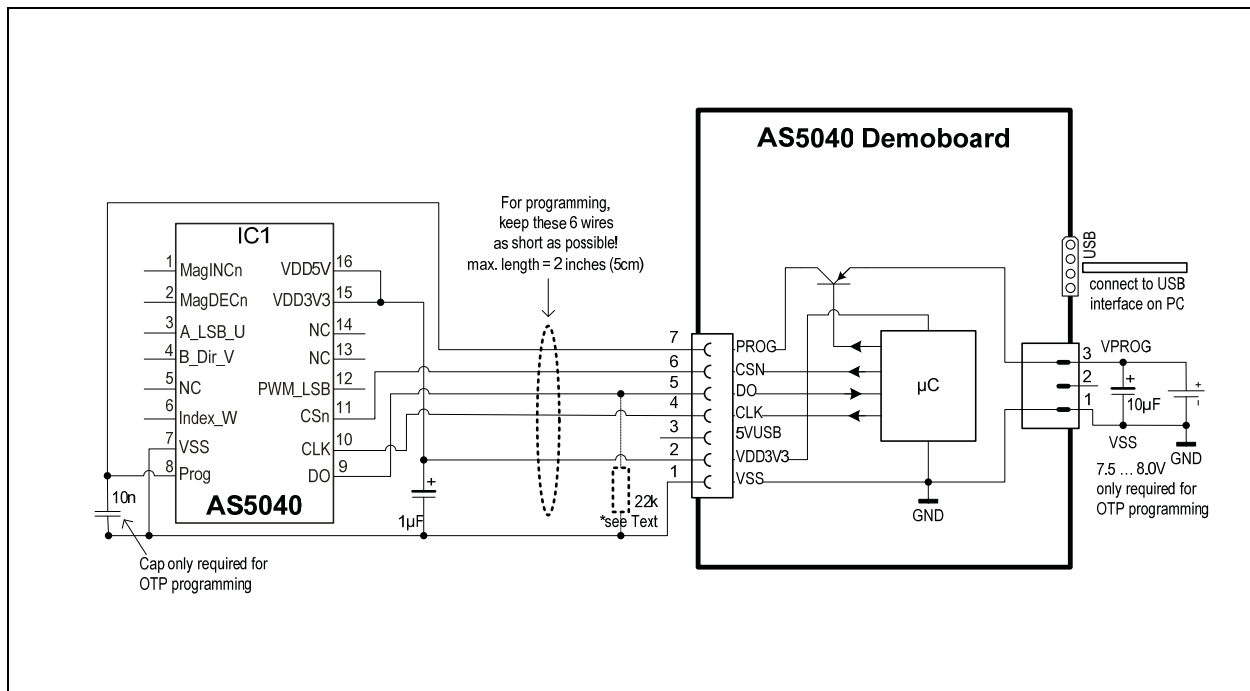


Figure 35:
OTP Programming Connection of AS5040 (shown with AS5040 demoboard)



Incremental Mode Programming

Three different incremental output modes are available.

Mode: Md1=0 / Md0=1 sets the AS5040 in quadrature mode.

Mode: Md1=1 / Md0=0 sets the AS5040 in step / direction mode (see [Figure 5](#)).

In both modes, the incremental resolution may be reduced from 10-bit down to 9, 8 or 7-bit using the divider OTP bits Div1 and Div0. (see [Figure 36](#) below).

Mode: Md1=1 / Md0=1 sets the AS5040 in brushless DC motor commutation mode with an additional LSB incremental signal at pin 12 (PWM_LSB).

To allow programming of all bits, the default factory setting is all bits = 0. This mode is equal to mode 0:0 (quadrature A/B, 1LSB index width, 256ppr).

The absolute angular output value, by default, increases with clockwise rotation of the magnet (top view).

Setting the CCW-bit (see [Figure 33](#)) allows reversing the indicated direction, e.g. when the magnet is placed underneath the IC:

CCW = 0 – angular value increases clockwise;

CCW = 1 – angular value increases counterclockwise.

By default, the zero / index position pulse is one LSB wide. It can be increased to a three LSB wide pulse by setting the Index-bit of the OTP register.

Further programming options (commutation modes) are available for brushless DC motor-control.

Md1 = Md0 = 1 changes the incremental output pins 3, 4 and 6 to a 3-phase commutation signal. Div1 defines the number of pulses per revolution for either a two-pole (Div1=0) or four-pole (Div1=1) rotor.

In addition, the LSB is available at pin 12 (the LSB signal replaces the PWM signal), which allows for high rotational speed measurement of up to 30000 rpm.

Figure 36:
One Time Programmable (OTP) Register Options

Mode	OTP-Mode-Register-Bit					Pin #			
	Md1	Md0	Div1	Div0	Index	3	4	6	12
Default (Mode0.0)	0	0	0 ⁽¹⁾	0 ⁽¹⁾	0 ⁽¹⁾	A	B	1LSB	PWM 10 bit
quadAB-Mode1.0	0	1	0	0	0			1LSB	
quadAB-Mode1.1	0	1	0	0	1			3LSBs	
quadAB-Mode1.2	0	1	0	1	0			1LSB	
quadAB-Mode1.3	0	1	0	1	1			3LSBs	
quadAB-Mode1.4	0	1	1	0	0			1LSB	
quadAB-Mode1.5	0	1	1	0	1			3LSBs	
quadAB-Mode1.6	0	1	1	1	0			1LSB	
quadAB-Mode1.7	0	1	1	1	1			3LSBs	

Mode	OTP-Mode-Register-Bit					Pin #			
	Md1	Md0	Div1	Div0	Index	3	4	6	12
Step/Dir-Mode2.0	1	0	0	0	0	LSB	Dir	1LSB	PWM 10-bit
Step/Dir-Mode2.1	1	0	0	0	1			3LSBs	
Step/Dir-Mode2.2	1	0	0	1	0			1LSB	
Step/Dir-Mode2.3	1	0	0	1	1			3LSBs	
Step/Dir-Mode2.4	1	0	1	0	0			1LSB	
Step/Dir-Mode2.5	1	0	1	0	1			3LSBs	
Step/Dir-Mode2.6	1	0	1	1	0			1LSB	
Step/Dir-Mode2.7	1	0	1	1	1			3LSBs	
Commutation-Mode3.0	1	1	0	0	0	U(0°)	V(120°)	W(240°)	LSB
Commutation-Mode3.1	1	1	0	1	0				
Commutation-Mode3.2	1	1	1	0	0	U'(0°, 180°)	V'(60°, 240°)	W'(120°, 300°)	LSB
Commutation-Mode3.3	1	1	1	1	0				

Note(s):

1. Div1, Div0 and Index cannot be programmed in Mode 0:0

Zero Position Programming

Zero position programming is an OTP option that simplifies assembly of a system, as the magnet does not need to be manually adjusted to the mechanical zero position. Once the assembly is completed, the mechanical and electrical zero positions can be matched by software. Any position within a full turn can be defined as the permanent new zero/index position.

For zero position programming, the magnet is turned to the mechanical zero position (e.g. the “OFF”-position of a rotary switch) and the actual angular value is read.

This value is written into the OTP register bits Z9:Z0 (see [Figure 33](#)) and programmed as described in [Programming the AS5040](#).

This new absolute zero position is also the new Index pulse position for incremental output modes.

Note(s): The zero position value may also be modified before programming, e.g. to program an electrical zero position that is 180° (half turn) from the mechanical zero position, just add 512 to the value read at the mechanical zero position and program the new value into the OTP register.

Repeated OTP Programming

Although a single AS5040 OTP register bit can be programmed only once (from 0 to 1), it is possible to program other, unprogrammed bits in subsequent programming cycles. However, a bit that has already been programmed should not be programmed twice. Therefore it is recommended that bits that are already programmed are set to “0” during a programming cycle.

Non-Permanent Programming

It is also possible to re-configure the AS5040 in a non-permanent way by overwriting the OTP register. This procedure is essentially a “Write Data” sequence (see [Figure 33](#)) without a subsequent OTP programming cycle. The “Write Data” sequence may be applied at any time during normal operation. This configuration remains set while the power supply voltage is above the power-on reset level (see 0). See Application Note AN5000-20 for further information.

Analog Readback Mode

Non-volatile programming (OTP) uses on-chip zener diodes, which become permanently low resistive when subjected to a specified reverse current.

The quality of the programming process depends on the amount of current that is applied during the programming process (up to 130mA).

This current must be provided by an external voltage source. If this voltage source cannot provide adequate power, the zener diodes may not be programmed properly.

In order to verify the quality of the programmed bits, an analog level can be read for each zener diode, giving an indication whether this particular bit was properly programmed or not.

To put the AS5040 in analog readback mode, a digital sequence must be applied to pins CSn, Prog and CLK as shown in Figure 37. The digital level for this pin depends on the supply configuration (3.3V or 5V; see 3.3V / 5V Operation).

The second rising edge on CSn (OutpEN) changes pin Prog to a digital output and the log. high signal at pin Prog must be removed to avoid collision of outputs (grey area in Figure 37).

The following falling slope of CSn changes pin Prog to an analog output, providing a reference voltage V_{ref} , that must be saved as a reference for the calculation of the subsequent programmed and unprogrammed OTP bits. Following this step, each rising slope of CLK outputs one bit of data in the reverse order as during programming (see Figure 37):

Md0-MD1-Div0,Div1-Indx-Z0...Z9, ccw)

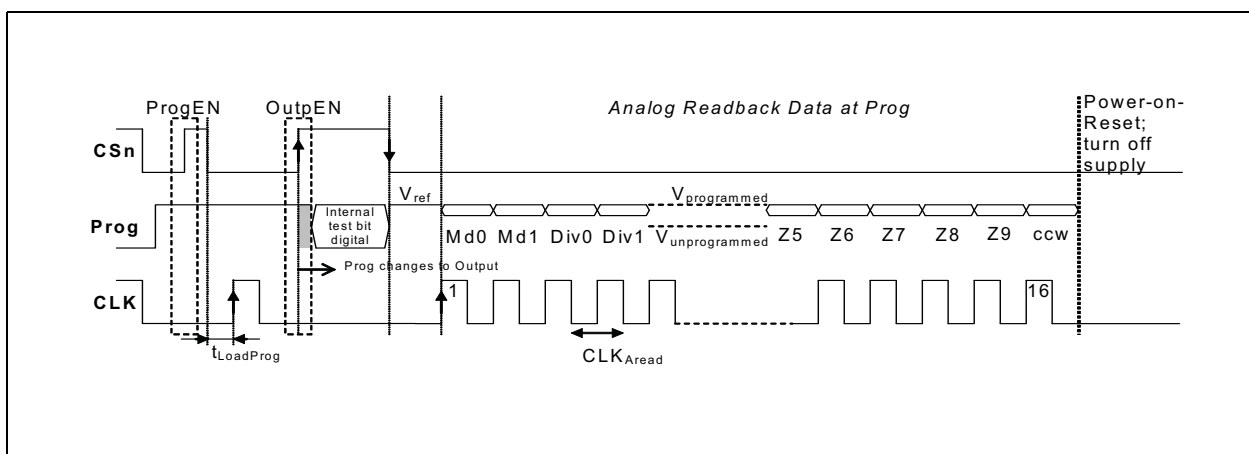
During analog readback, the capacitor at pin Prog (see Figure 35) should be removed to allow a fast readout rate. If the capacitor is not removed the analog voltage will take longer to stabilize due to the additional capacitance.

The measured analog voltage for each bit must be subtracted from the previously measured V_{ref} , and the resulting value gives an indication on the quality of the programmed bit: a reading of $<100\text{mV}$ indicates a properly programmed bit and a reading of $>1\text{V}$ indicates a properly unprogrammed bit.

A reading between 100mV and 1V indicates a faulty bit, which may result in an undefined digital value, when the OTP is read at power-up.

Following the 16th clock (after reading bit "ccw"), the chip must be reset by disconnecting the power supply.

Figure 37: OTP Register Analog Read



Alignment Mode

The alignment mode simplifies centering the magnet over the chip to gain maximum accuracy and XY-alignment tolerance.

This electrical centering method allows a wider XY-alignment tolerance (0.485mm radius) than mechanical centering (0.25mm radius) as it eliminates the placement tolerance of the die within the IC package ($\pm 0.235\text{mm}$).

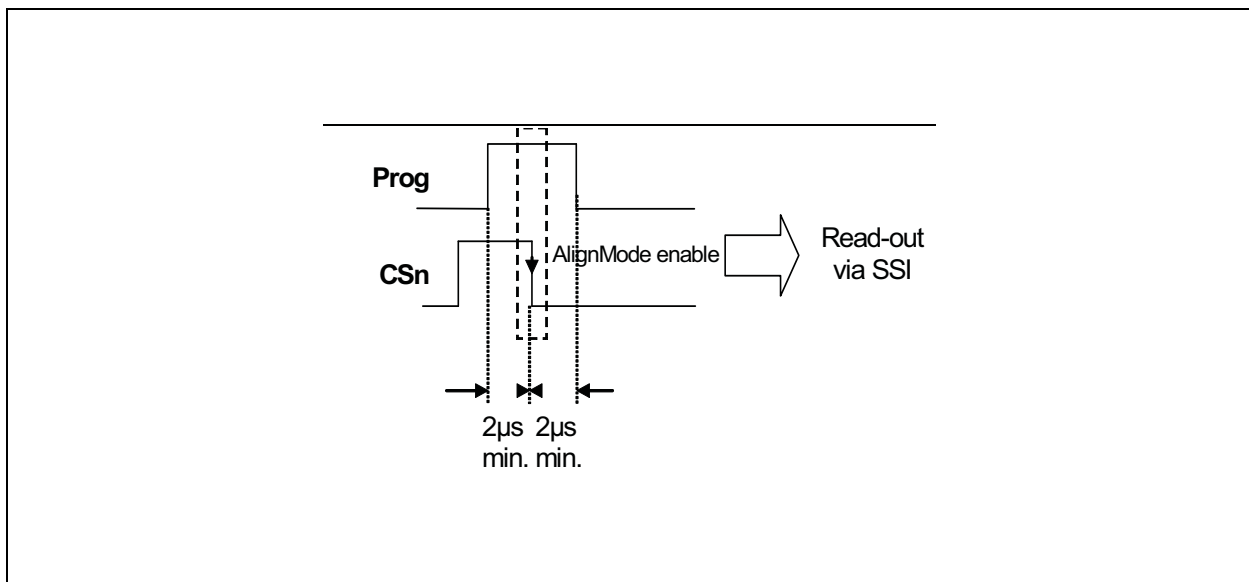
Alignment mode can be enabled with the falling edge of CSn while Prog = logic high (Figure 38). The Data bits D9-D0 of the SSI change to a 10-bit displacement amplitude output. A high value indicates large X or Y displacement, but also higher absolute magnetic field strength. The magnet is properly aligned, when the difference between highest and lowest value over one full turn is at a minimum.

Under normal conditions, a properly aligned magnet will result in a reading of less than 32 over a full turn. The MagINCn and MagDECn indicators will be = 1 when the alignment mode reading is < 32 . At the same time, both hardware pins MagINCn (#1) and MagDECn (#2) will be pulled to VSS. A properly aligned magnet will therefore produce a MagINCn = MagDECn = 1 signal throughout a full 360° turn of the magnet.

Stronger magnets or short gaps between magnet and IC may show values larger than 32. These magnets are still properly aligned as long as the difference between highest and lowest value over one full turn is at a minimum.

The alignment mode can be reset to normal operation mode by a power-on-reset (disconnect / re-connect power supply).

Figure 38:
Enabling the Alignment Mode



3.3V / 5V Operation

The AS5040 operates either at 3.3V \pm 10% or at 5V \pm 10%. This is made possible by an internal 3.3V Low-Dropout (LDO) voltage regulator. The internal supply voltage is always taken from the output of the LDO, meaning that the internal blocks are always operating at 3.3V.

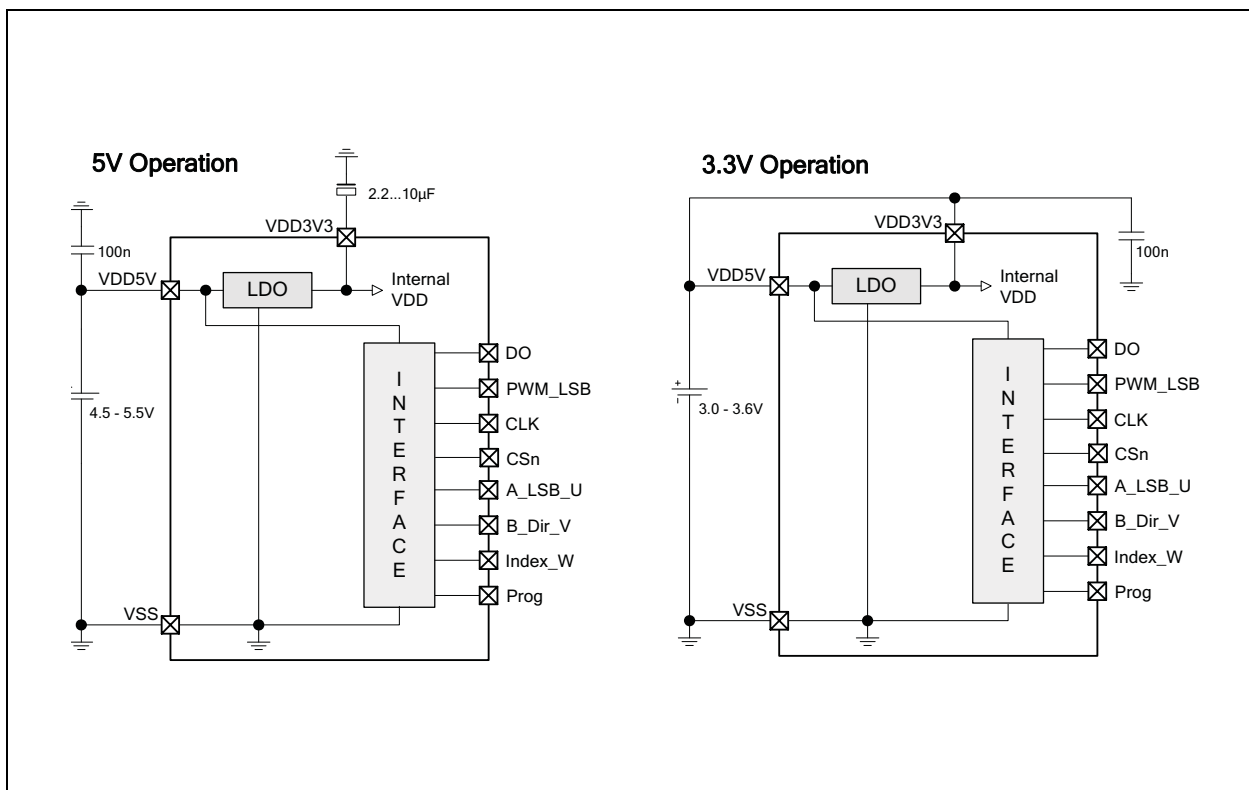
For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 39).

For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 2.2...10 μ F capacitor, which is supposed to be placed close to the supply pin (see Figure 39).

The VDD3V3 output is intended for internal use only. It must not be loaded with an external load.

The output voltage of the digital interface I/O's corresponds to the voltage at pin VDD5V, as the I/O buffers are supplied from this pin (see Figure 39).

Figure 39:
Connections for 5V / 3.3V Supply Voltages



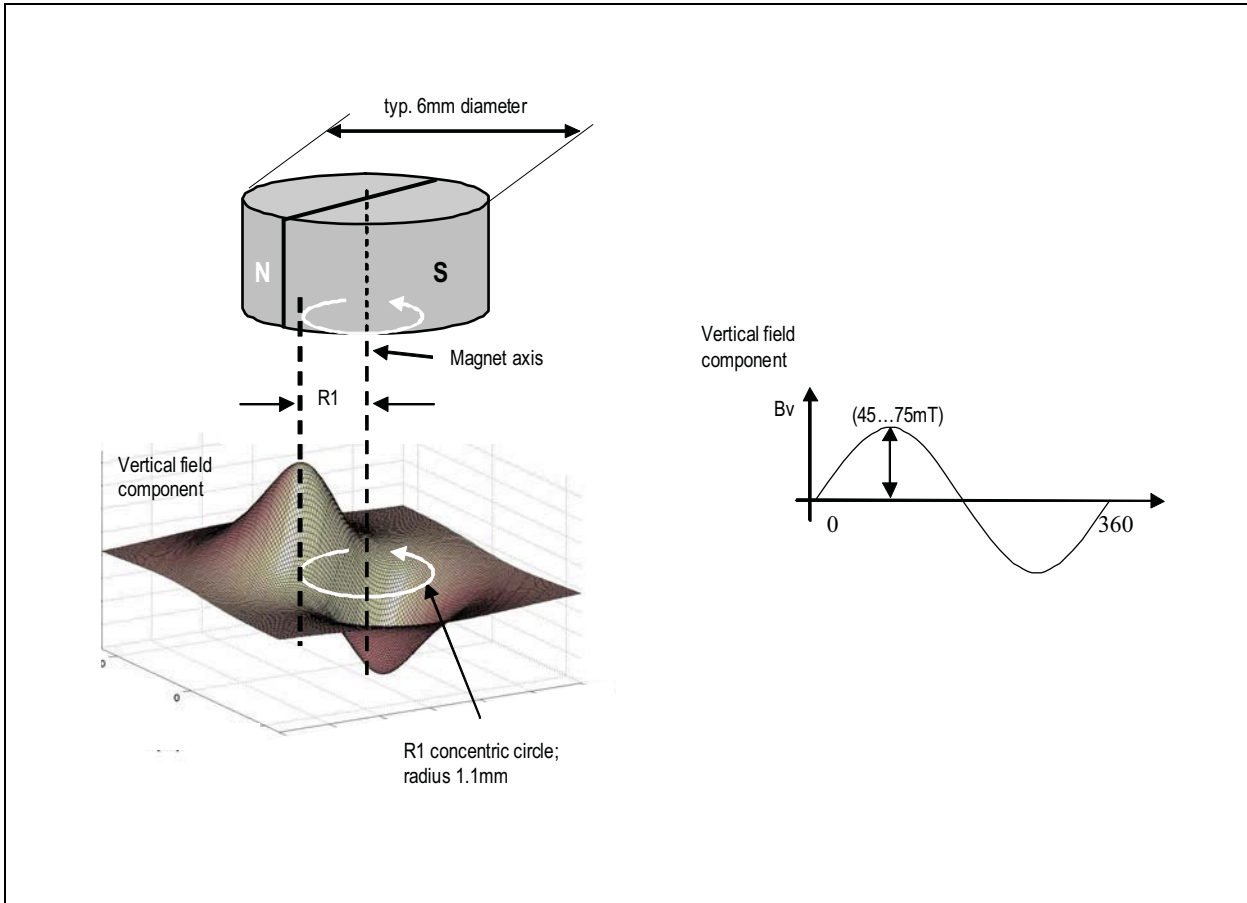
A buffer capacitor of 100nF is recommended in both cases close to pin VDD5V. Note that pin VDD3V3 must always be buffered by a capacitor. It must not be left floating, as this may cause an instable internal 3.3V supply voltage which may lead to larger than normal jitter of the measured angle.

Choosing the Proper Magnet

Typically the magnet should be 6mm in diameter and $\geq 2.5\text{mm}$ in height. Magnetic materials such as rare earth AlNiCo, SmCo5 or NdFeB are recommended.

The magnet's field strength perpendicular to the die surface should be verified using a gauss-meter. The magnetic field B_v at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of $\pm 45\text{mT}$ to $\pm 75\text{mT}$. (see Figure 40).

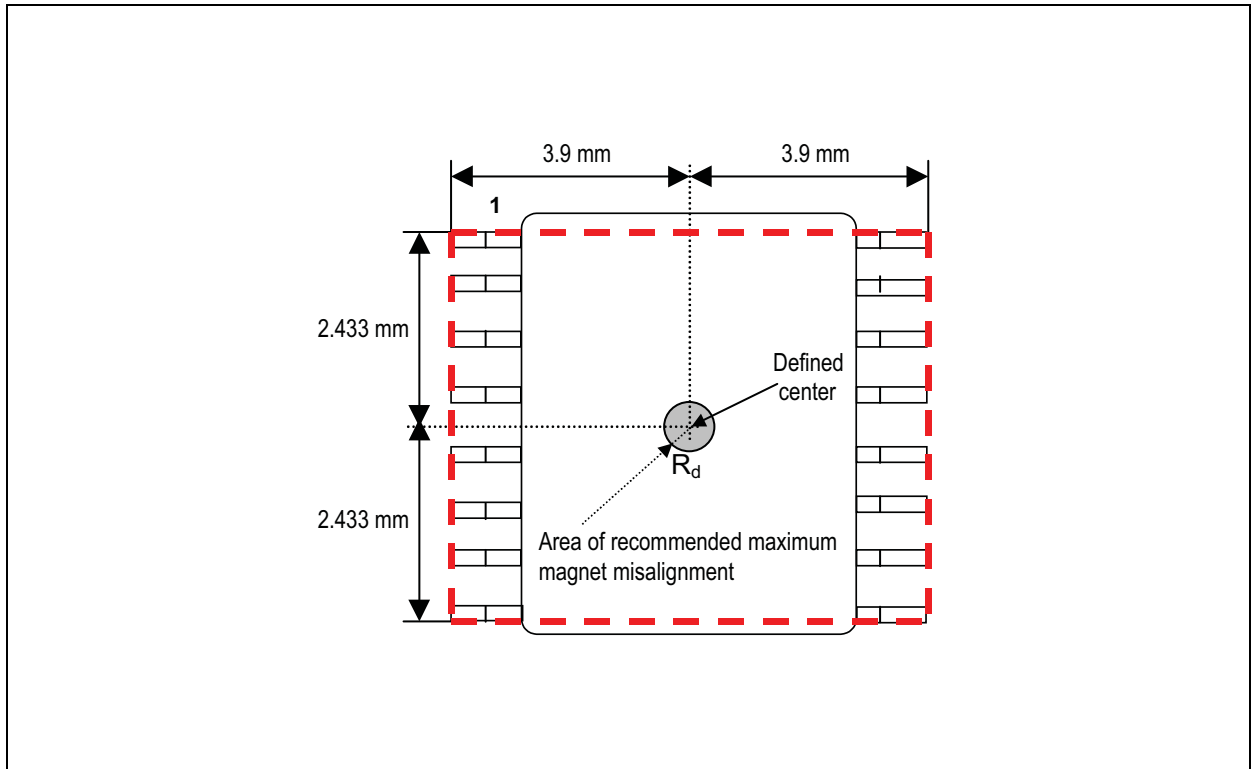
Figure 40:
Typical Magnet and Magnetic Field Distribution



Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the IC package as shown in Figure 41:

Figure 41:
Defined IC Center and Magnet Displacement Radius



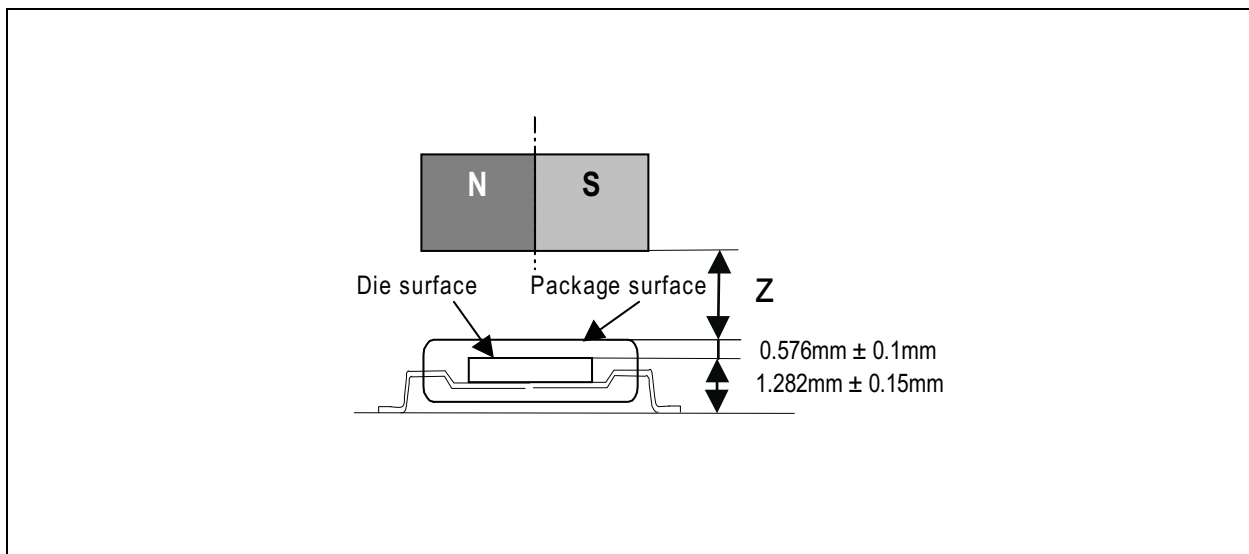
Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm from the defined center of the IC with reference to the edge of pin #1 (see [Figure 41](#)). This radius includes the placement tolerance of the chip within the SSOP-16 package ($\pm 0.235\text{mm}$). The displacement radius R_d is 0.485mm with reference to the center of the chip (see [Alignment Mode](#))

The vertical distance should be chosen such that the magnetic field on the die surface is within the specified limits (see [Figure 40](#)). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.8mm with the recommended magnet (6mm x 2.5mm). Larger gaps are possible, as long as the required magnetic field strength stays within the defined limits.

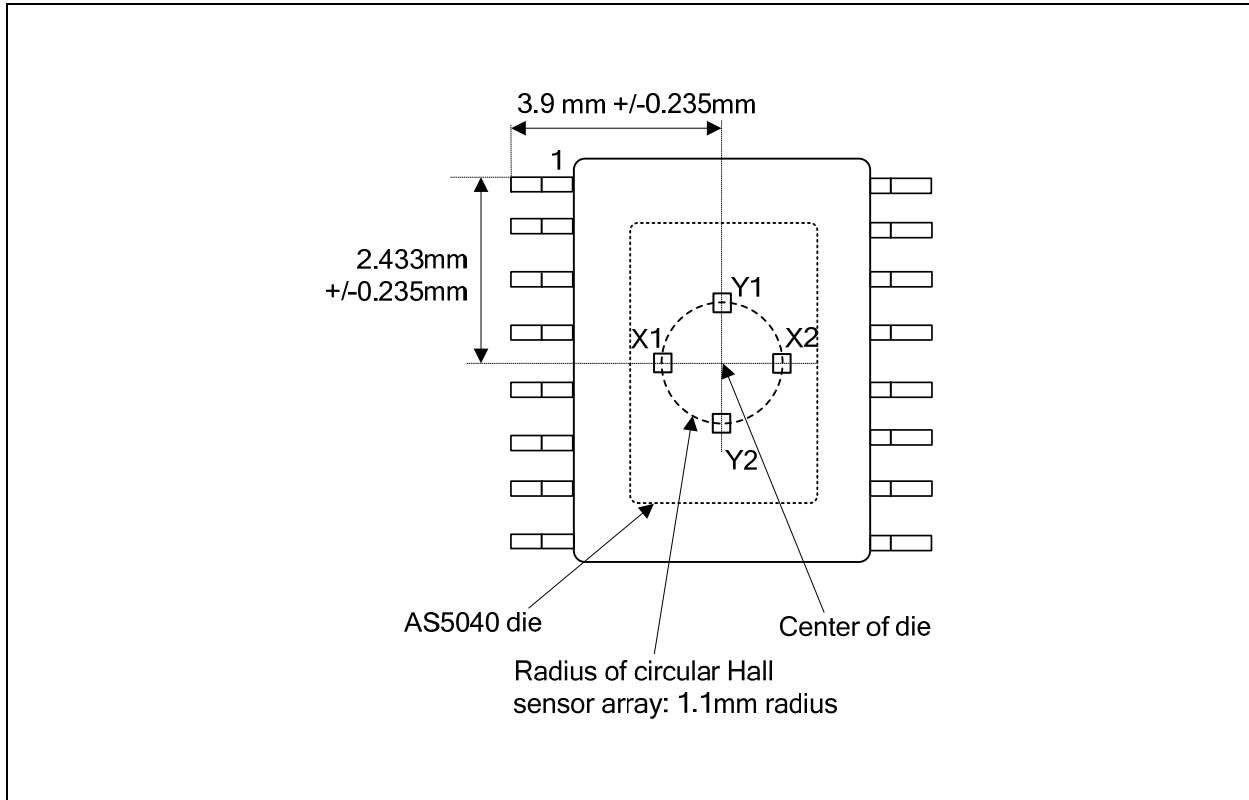
A magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by MagINCn (pin 1) and MagDECn (pin 2), see [Figure 22](#).

Figure 42:
Vertical Placement of the Magnet



Simulation Modelling

Figure 43:
Arrangement of Hall Sensor Array on Chip (principle)



With reference to [Figure 43](#), a diametrically magnetized permanent magnet is placed above or below the surface of the AS5040. The chip uses an array of Hall sensors to sample the vertical vector of a magnetic field distributed across the device package surface. The area of magnetic sensitivity is a circular locus of 1.1mm radius with respect to the center of the die. The Hall sensors in the area of magnetic sensitivity are grouped and configured such that orthogonally related components of the magnetic fields are sampled differentially.

The differential signal Y1-Y2 will give a sine vector of the magnetic field. The differential signal X1-X2 will give an orthogonally related cosine vector of the magnetic field.

The angular displacement (θ) of the magnetic source with reference to the Hall sensor array may then be modelled by:

$$(EQ4) \quad \theta = \arctan\left(\frac{Y1 - Y2}{X1 - X2}\right) \pm 0.5^\circ$$

The $\pm 0.5^\circ$ angular error assumes a magnet optimally aligned over the center of the die and is a result of gain mismatch errors of the AS5040. Placement tolerances of the die within the package are ± 0.235 mm in X and Y direction, using a reference point of the edge of pin #1 ([Figure 43](#)).

In order to neglect the influence of external disturbing magnetic fields, a robust differential sampling and ratiometric calculation algorithm has been implemented. The differential sampling of the sine and cosine vectors removes any common mode error due to DC components introduced by the magnetic source itself or external disturbing magnetic fields. A ratiometric division of the sine and cosine vectors removes the need for an accurate absolute magnitude of the magnetic field and thus accurate Z-axis alignment of the magnetic source.

The recommended differential input range of the magnetic field strength ($B_{(X1-X2)}, B_{(Y1-Y2)}$) is $\pm 75\text{mT}$ at the surface of the die. In addition to this range, an additional offset of $\pm 5\text{mT}$, caused by unwanted external stray fields is allowed.

The chip will continue to operate, but with degraded output linearity, if the signal field strength is outside the recommended range. Too strong magnetic fields will introduce errors due to saturation effects in the internal preamplifiers. Too weak magnetic fields will introduce errors due to noise becoming more dominant.

Failure Diagnostics

The AS5040 also offers several diagnostic and failure detection features:

Magnetic Field Strength Diagnosis

By software: the MagINCn and MagDECn status bits will both be high when the magnetic field is out of range.

By hardware: Pins #1 (MagINCn) and #2 (MagDECn) are open-drain outputs and will both be turned ON (= low with external pull-up resistor) when the magnetic field is out of range. If only one of the outputs is low, the magnet is either moving towards the chip (MagINCn) or away from the chip (MagDECn).

Power Supply Failure Detection

By software: If the power supply to the AS5040 is interrupted, the digital data read by the SSI will be all "0"s. Data is only valid, when bit OCF is high, hence a data stream with all "0"s is invalid. To ensure adequate low levels in the failure case, a pull-down resistor (~10kΩ) should be added between pin DO and VSS at the receiving side.

By hardware: The MagINCn and MagDECn pins are open drain outputs and require external pull-up resistors. In normal operation, these pins are high ohmic and the outputs are high (see [Figure 22](#)). In a failure case, either when the magnetic field is out of range or the power supply is missing, these outputs will become low. To ensure adequate low levels in case of a broken power supply to the AS5040, the pull-up resistors (>10kΩ) from each pin must be connected to the positive supply at pin 16 (VDD5V).

By hardware: PWM output: The PWM output is a constant stream of pulses with 1kHz repetition frequency. In case of power loss, these pulses are missing.

By hardware: Incremental outputs: In normal operation, pins A(#3), B(#4) and Index (#6) will never be high at the same time, as Index is only high when A=B=low. However, after a power-on-reset, if VDD is powered up or restarts after a power supply interruption, all three outputs will remain in high state until pin CSn is pulled low. If CSn is already tied to VSS during power-up, the incremental outputs will all be high until the internal offset compensation is finished (within t_{PwrUp}).

Angular Output Tolerances

Accuracy

Accuracy is defined as the error between measured angle and actual angle. It is influenced by several factors:

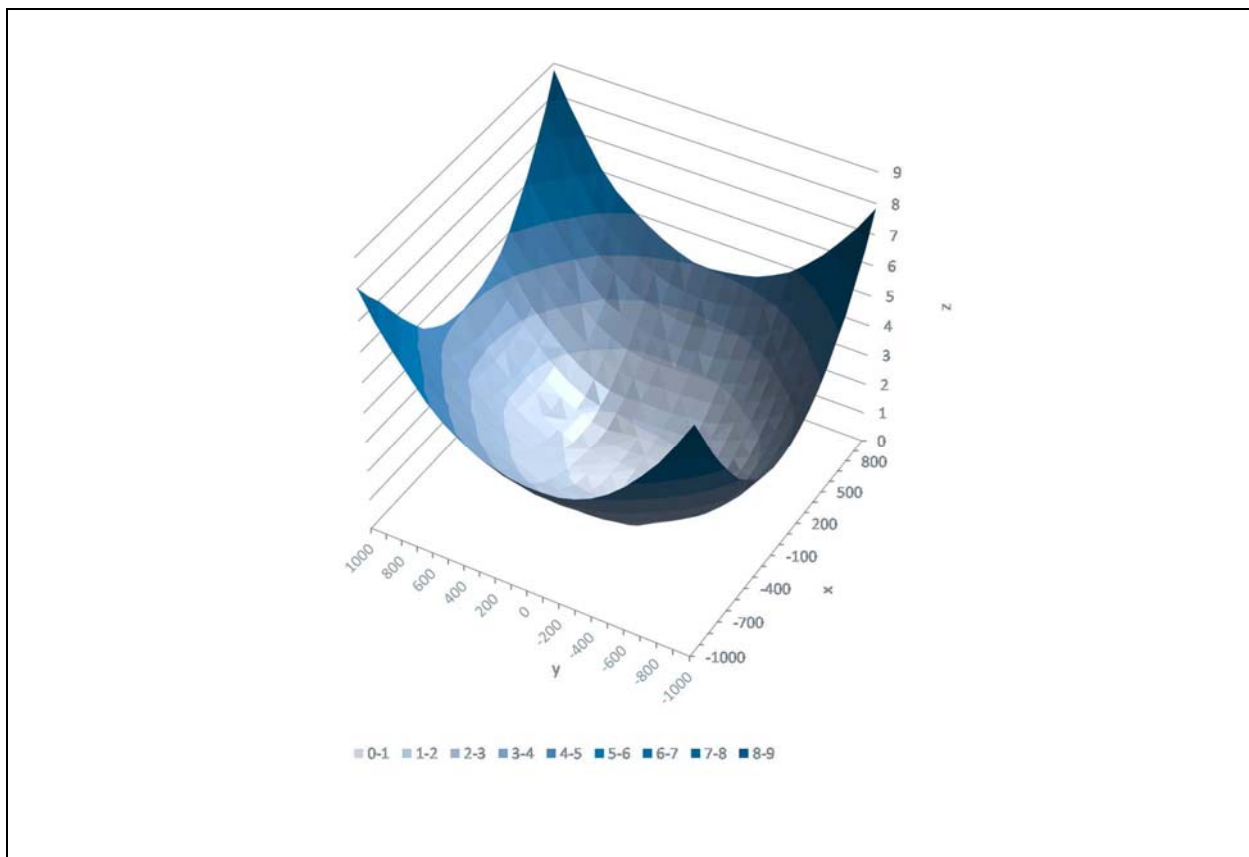
- The non-linearity of the analog-digital converters,
- Internal gain and mismatch errors,
- Non-linearity due to misalignment of the magnet

As a sum of all these errors, the accuracy with centered magnet = $(Err_{max} - Err_{min})/2$ is specified as better than ± 0.5 degrees @ 25°C (see [Figure 45](#)).

Misalignment of the magnet further reduces the accuracy. [Figure 44](#) shows an example of a 3D-graph displaying nonlinearity over XY-misalignment. The center of the square XY-area corresponds to a centered magnet (see dot in the center of the graph). The X- and Y- axis extends to a misalignment of ± 1 mm in both directions. The total misalignment area of the graph covers a square of 2x2 mm (79x79mil) with a step size of 100 μ m.

For each misalignment step, the measurement as shown in [Figure 45](#) is repeated and the accuracy $(Err_{max} - Err_{min})/2$ (e.g. 0.25° in [Figure 45](#)) is entered as the Z-axis in the 3D-graph.

Figure 44:
Example of Linearity Error Over XY Misalignment

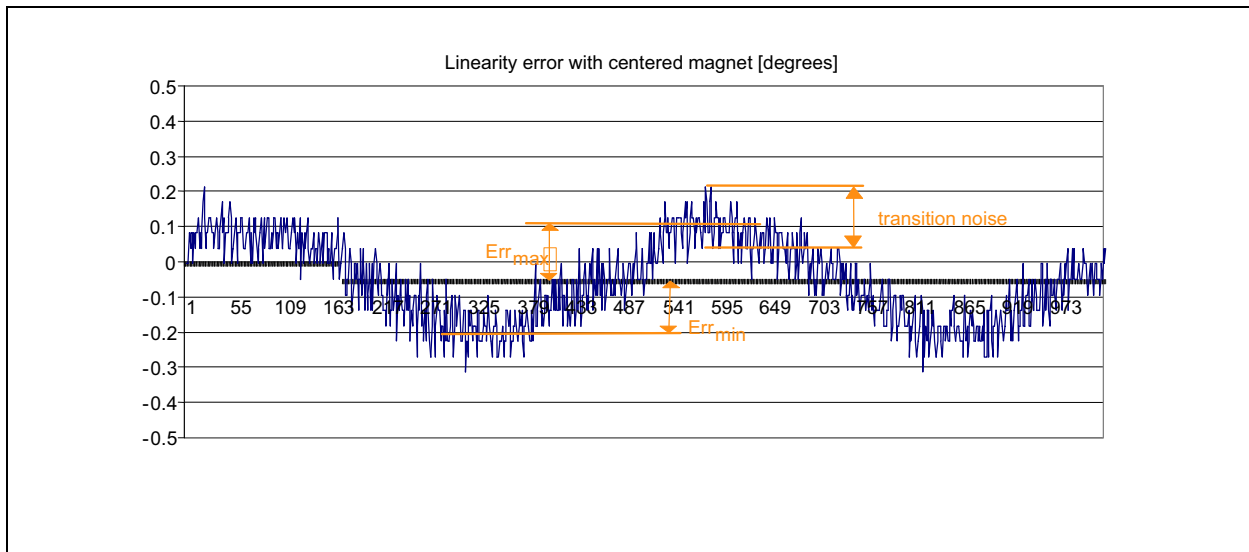


The maximum non-linearity error on this example is better than ± 1 degree (inner circle) over a misalignment radius of ~ 0.7 mm. For volume production, the placement tolerance of the IC within the package (± 0.235 mm) must also be taken into account.

The total nonlinearity error over process tolerances, temperature and a misalignment circle radius of 0.25mm is specified better than ± 1.4 degrees.

The magnet used for this measurement was a cylindrical NdFeB (Bomatec® BMN-35H) magnet with 6mm diameter and 2.5mm in height.

Figure 45:
Example of Linearity Error Over 360°



Transition Noise

Transition noise is defined as the jitter in the transition between two steps.

Due to the nature of the measurement principle (Hall sensors + Preamplifier + ADC), there is always a certain degree of noise involved.

This transition noise voltage results in an angular transition noise at the outputs. It is specified as 0.12 degrees rms (1 sigma)¹

This is the repeatability of an indicated angle at a given mechanical position.

1. Statistically, 1 sigma represents 68.27% of readings, 3 sigma represents 99.73% of readings.

The transition noise has different implications on the type of output that is used:

- **Absolute Output; SSI Interface:** The transition noise of the absolute output can be reduced by the user by applying an averaging of readings.
- **PWM Interface:** If the PWM interface is used as an analog output by adding a low pass filter, the transition noise can be reduced by lowering the cutoff frequency of the filter. If the PWM interface is used as a digital interface with a counter at the receiving side, the transition noise may again be reduced by averaging of readings.
- **Incremental Mode:** In incremental mode, the transition noise influences the period, width and phase shift of the output signals A, B and Index. However, the algorithm used to generate the incremental outputs guarantees no missing or additional pulses even at high speeds (up to 30.000 rpm and higher).

High Speed Operation

Sampling Rate

The AS5040 samples the angular value at a rate of 10.42k samples per second. Consequently, the incremental, as well as the absolute outputs are updated each 96µs. At a stationary position of the magnet, this sampling rate creates no additional error.

Absolute Mode with Serial Communication

With the given sampling rate of 10.4 kHz, the number of samples (n) per turn for a magnet rotating at high speed can be calculated by:

$$(EQ5) \quad n = \frac{60}{\text{rpm} \cdot 96\mu\text{s}}$$

In practice, there is no upper speed limit. The only restriction is that there will be fewer samples per revolution as the speed increases.

Regardless of the rotational speed, the absolute angular value is always sampled at the highest resolution of 10-bit.

Likewise, for a given number of samples per revolution (n), the maximum speed can be calculated by:

$$(EQ6) \quad \text{rpm} = \frac{60}{n \cdot 96\mu\text{s}}$$

In absolute mode with serial communication, 610 rpm is the maximum speed, where 1024 readings per revolution can be obtained.

In incremental mode, the maximum error caused by the sampling rate of the ADCs is 0/+96µs. It has a peak of 1LSB = 0.35° at 610rpm. At higher speeds this error is reduced again due to interpolation and the output delay remains at 192µs as the DSP requires two sampling periods (2x96µs) to synthesize and redistribute any missing pulses.

Absolute Mode with PWM

The principle is the same as with the serial communication. The PWM output is refreshed with a rate of 1.025ms, the number of samples (n) per turn for a magnet rotating at high speed can be calculated by:

$$(EQ7) \quad n = \frac{60}{\text{rpm} \times 1.025\text{ms}}$$

In absolute mode with PWM output, 57rpm is the maximum speed, where 1024 readings per revolution can be obtained.

Incremental Mode

Incremental encoders are usually required to produce no missing pulses up to several thousand rpm’s.

Therefore, the AS5040 has a built-in interpolator, which ensures that there are no missing pulses at the incremental outputs for rotational speeds of up to 30000 rpm, even at the highest resolution of 10 bits (512 pulses per revolution).

Figure 46:
Speed Performance

Absolute Output Mode	Incremental Output Mode
610rpm = 1024 samples / turn	No missing pulses @ 10-bit resolution (512ppr): max. speed = 30000 rpm
1220rpm = 512 samples / turn	
2441rpm = 256 samples / turn	
etc...	

Propagation Delays

The propagation delay is the delay between the time that the sample is taken until it is converted and available as angular data. This delay is 48µs for the absolute interface and 192µs for the incremental interface.

Using the SSI interface for absolute data transmission, an additional delay must be considered, caused by the asynchronous sampling ($t = 0...1/f_s$) and the time it takes the external control unit to read and process the data.

Angular Error Caused by Propagation Delay

A rotating magnet will therefore cause an angular error caused by the output delay. This error increases linearly with speed:

$$(EQ8) \quad e_{\text{sampling}} = \text{rpm} \times 6 \times \text{prop-delay}$$

Where:

e_{sampling} = angular error [°]

rpm = rotating speed [rpm]

prop delay = propagation delay [seconds]

Note(s): Since the propagation delay is known, it can be automatically compensated by the control unit processing the data from the AS5040, thus reducing the angular error caused by speed.

Internal Timing Tolerance

The AS5040 does not require an external ceramic resonator or quartz. All internal clock timings for the AS5040 are generated by an on-chip RC oscillator. This oscillator is factory trimmed to $\pm 5\%$ accuracy at room temperature ($\pm 10\%$ over full temperature range). This tolerance influences the ADC sampling rate and the pulse width of the PWM output:

- Absolute Output; SSI Interface:
A new angular value is updated every 100 μs (typ)
- Incremental outputs:
the incremental outputs are updated every 100 μs (typ.)
- PWM output:
A new angular value is updated every 100 μs (typ.).
The PWM pulse timings T_{on} and T_{off} also have the same tolerance as the internal oscillator.
If only the PWM pulse width T_{on} is used to measure the angle, the resulting value also has this timing tolerance. However, this tolerance can be canceled by measuring both T_{on} and T_{off} and calculating the angle from the duty cycle (see [Incremental Outputs](#)):

$$(EQ9) \quad \text{Position} = \frac{t_{\text{on}} \cdot 1025}{(t_{\text{on}} + t_{\text{off}})} - 1$$

Temperature

Magnetic Temperature Coefficient

One of the major benefits of the AS5040 compared to linear Hall sensors is that it is much less sensitive to temperature. While linear Hall sensors require a compensation of the magnet's temperature coefficients, the AS5040 automatically compensates for the varying magnetic field strength over temperature. The magnet's temperature drift does not need to be considered, as the AS5040 operates with magnetic field strengths from $\pm 45\text{mT}$ to $\pm 75\text{mT}$.

Example:

A NdFeB magnet has a field strength of 75mT @ -40°C and a temperature coefficient of -0.12% per Kelvin.

The temperature change is from -40° to $+125^\circ = 165\text{K}$.

The magnetic field change is: $165 \times -0.12\% = -19.8\%$, which corresponds to 75mT at -40°C and 60mT at 125°C .

The AS5040 can compensate for this temperature related field strength change automatically, no user adjustment is required.

Accuracy Over Temperature

The influence of temperature in the absolute accuracy is very low. While the accuracy is $\leq \pm 0.5^\circ$ at room temperature, it may increase to $\leq \pm 0.9^\circ$ due to increasing noise at high temperatures.

Timing Tolerance Over Temperature

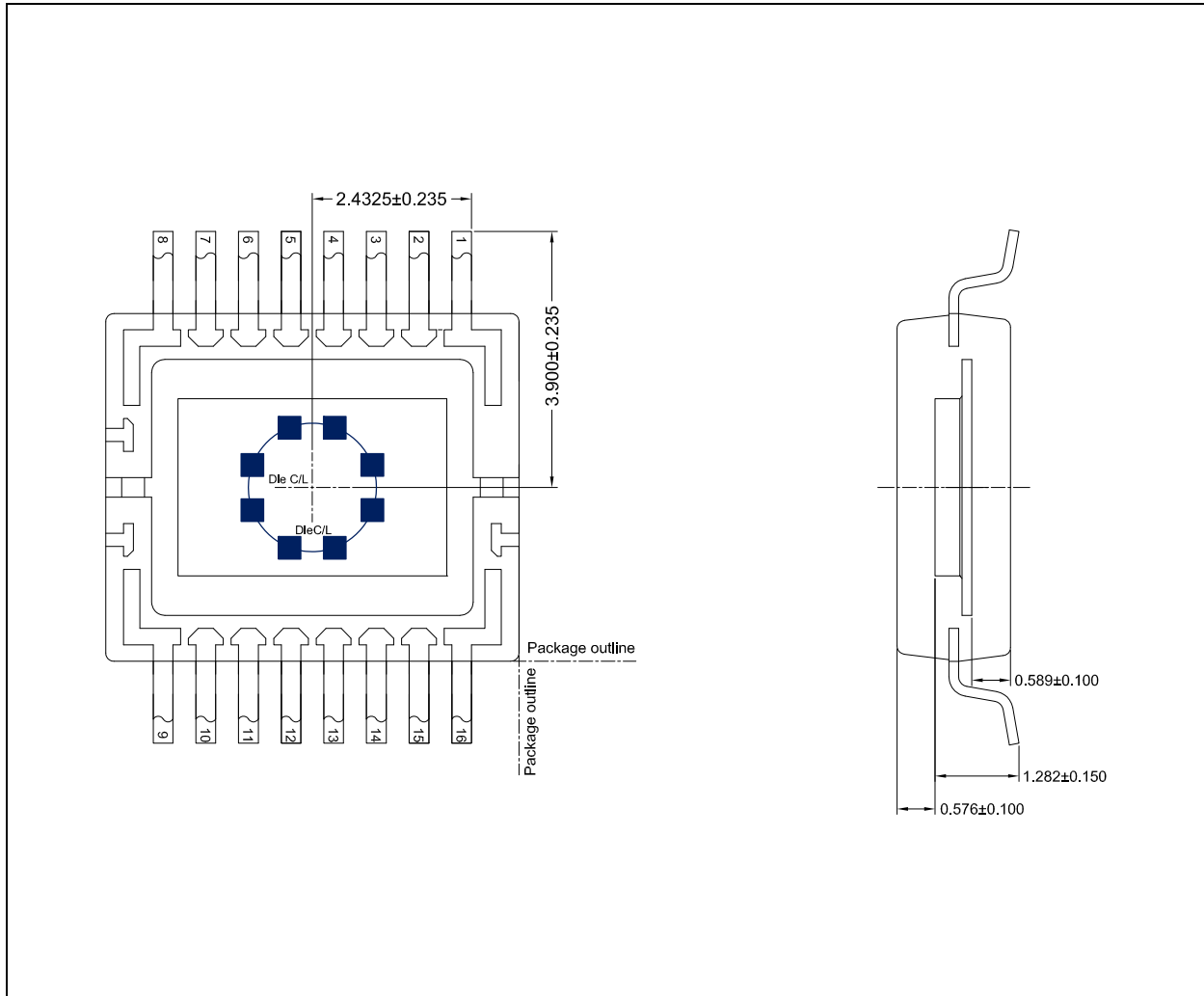
The internal RC oscillator is factory trimmed to $\pm 5\%$. Over temperature, this tolerance may increase to $\pm 10\%$. Generally, the timing tolerance has no influence in the accuracy or resolution of the system, as it is used mainly for internal clock generation.

The only concern to the user is the width of the PWM output pulse, which relates directly to the timing tolerance of the internal oscillator. This influence, however, can be canceled by measuring the complete PWM duty cycle (see [Internal Timing Tolerance](#)).

Mechanical Data

The internal Hall elements are located in the center of the package on a circle with a radius of 1 mm.

Figure 47:
Hall Element Positions

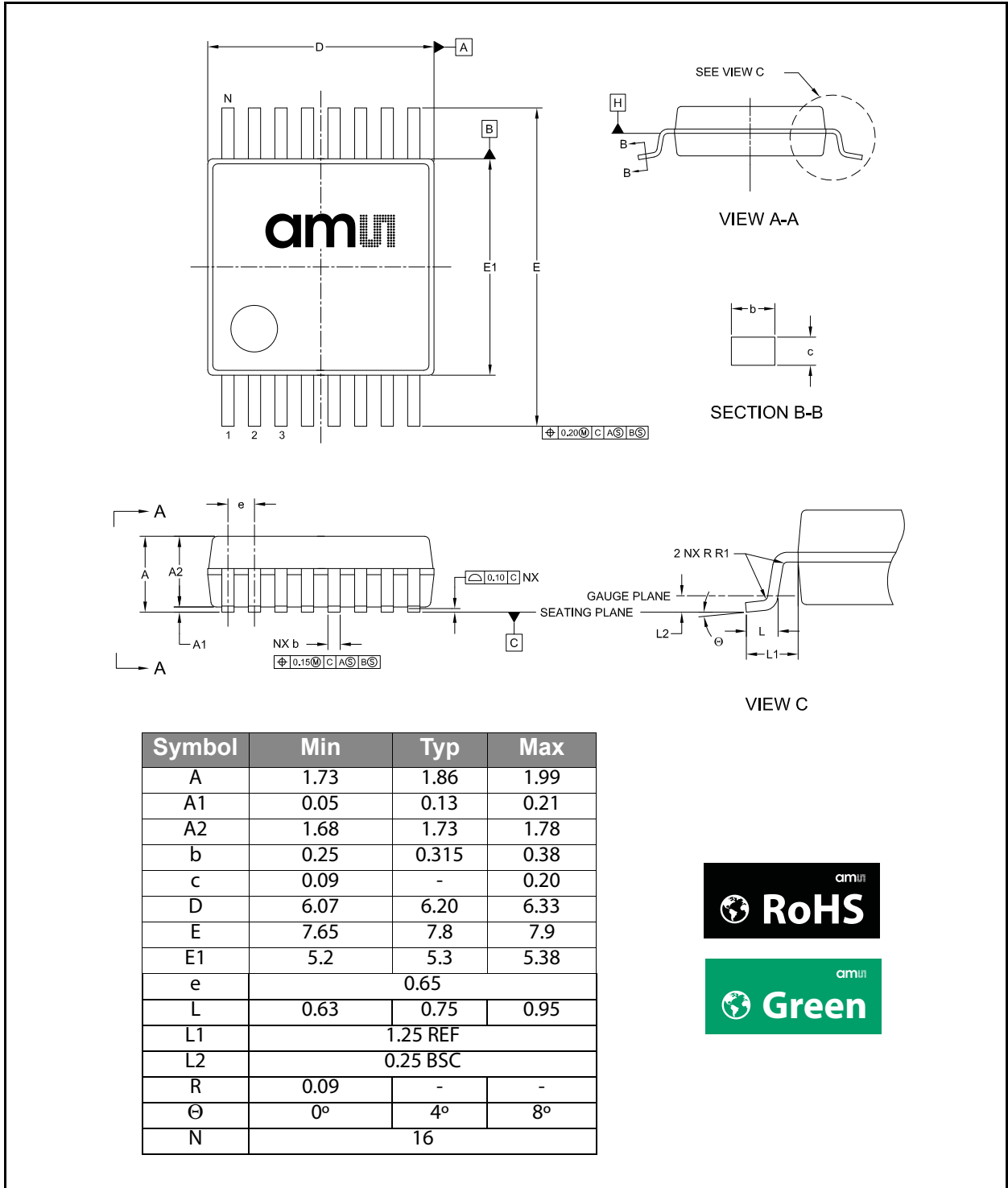


Note(s):

1. All dimensions in mm.
2. Die thickness 38µm nom.
3. Adhesive thickness 30 ± 15µm.
4. Leadframe downset 200 ± 38µm.
5. Leadframe thickness 152±8 µm.

Package Drawings & Markings

Figure 48:
16-Lead Shrink Small Outline Package SSOP-16

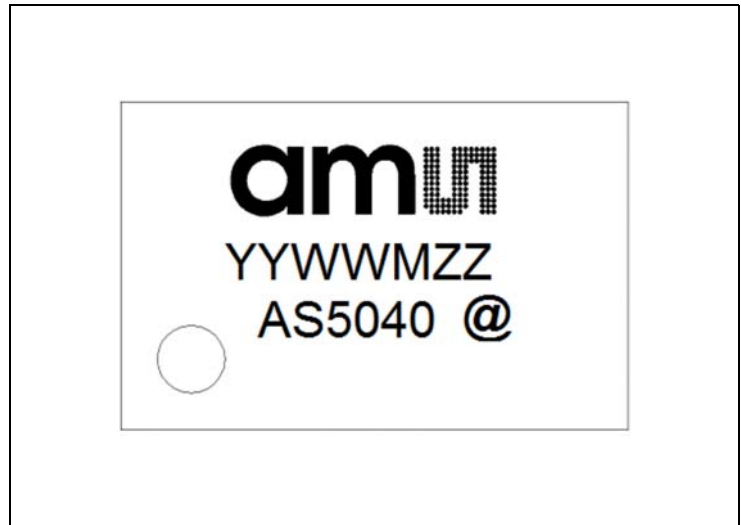


Note(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles in degrees.
3. N is the total number of terminals.



**Figure 49:
Package Marking**



**Figure 50:
Packaging Code**

YY	WW	M	ZZ	@
Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Free choice/ traceability code	Sublot identifier

JEDEC Package Outline Standard:
MO - 150 AC

Thermal Resistance $R_{th(j-a)}$:
typ. 151 K/W in still air, soldered on PCB

IC's marked with a white dot or the letters "ES" denote Engineering Samples

Recommended PCB Footprint

Figure 51:
Recommended PCB Footprint

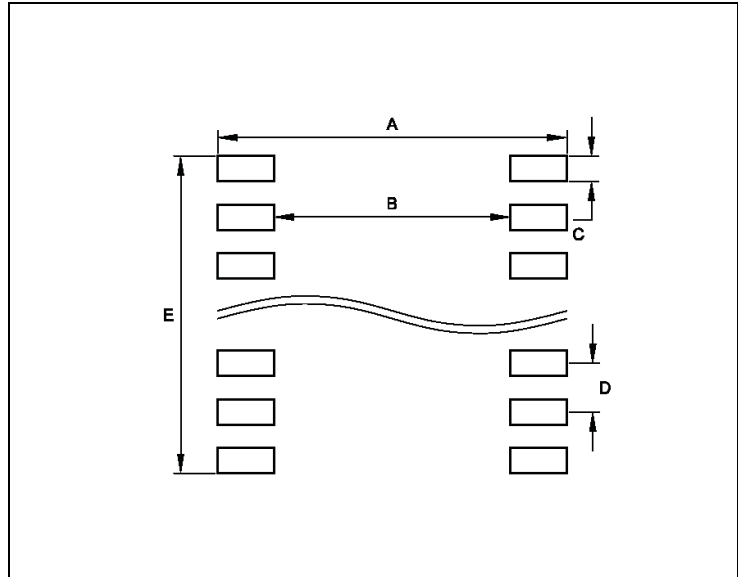


Figure 52:
Recommended Footprint Data

Recommended Footprint Data		
	mm	inch
A	9.02	0.355
B	6.16	0.242
C	0.46	0.018
D	0.65	0.025
E	5.01	0.197

Ordering & Contact Information

Figure 53:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS5040-ASSM	SSOP-16	AS5040	Tape & Reel	500 pcs/reel
AS5040-ASST	SSOP-16	AS5040	Tape & Reel	2000 pcs/reel

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Document Status	Product Status	Definition
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Updated Figure 27	25
2-13 (2020-Sep-14) to 2-14 (2020-Nov-25)	
Updated Figure 7	7

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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