AS5055A

Low Power 12-Bit Magnetic Position Sensor

General Description

The AS5055A is a single-chip magnetic position sensor with low voltage and low power features.

It includes an integrated Hall element array, a high resolution ADC and a smart power management controller.

The angle position, alarm bits and magnetic field information are transmitted over a 3-wire or 4-wire SPI interface to the microcontroller.

The AS5055A is available in a compact QFN 16-pin 4x4x0.85 mm package and specified over an operating temperature of -40ºC to 85ºC.

For further understanding in regards to the contents of the datasheet, please refer to the Reference Guide located at the end of the document.

Key Benefits & Features

The benefits and features of AS5055A, Low Power 12-Bit Magnetic Position Sensor are listed below:

Figure 1:
Added Value of Using AS5055A

Benefits	Features
Precise and reliable absolute angle measurement	12-bit absolute angle position indication
Very low power consumption	3µA current consumption in low power mode
High reliability sensing	Immune to external magnetic stray fields
Synchronisation between microcontroller and sensor	Interrupt pin displays availability of new data
Ideal for small and compact designs	QFN-16 4x4 package
Industry-standard interface	3- or 4-wire SPI interface

Applications

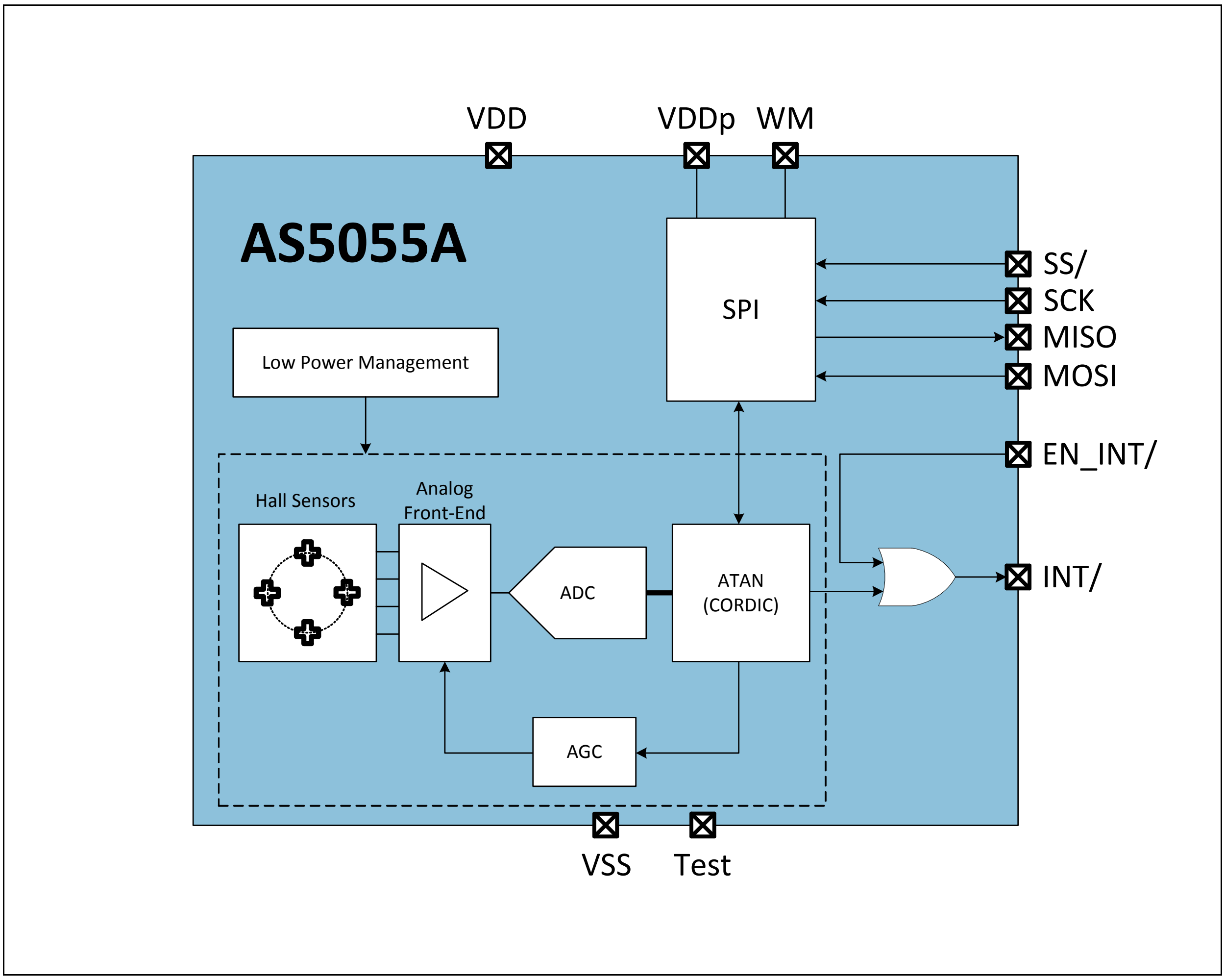
This sensor is optimized for a broad range of demanding applications including:

- Servo motor control
- Battery operated systems
- Robotics

Block Diagram

The functional blocks of this sensor are shown below:

Figure 2:
AS5055A Block Diagram



Pin Assignment

The AS5055A pin assignments are shown below.

Figure 3:
Pin Diagram

Pin Assignments (Top View):
Package drawing is not to scale.

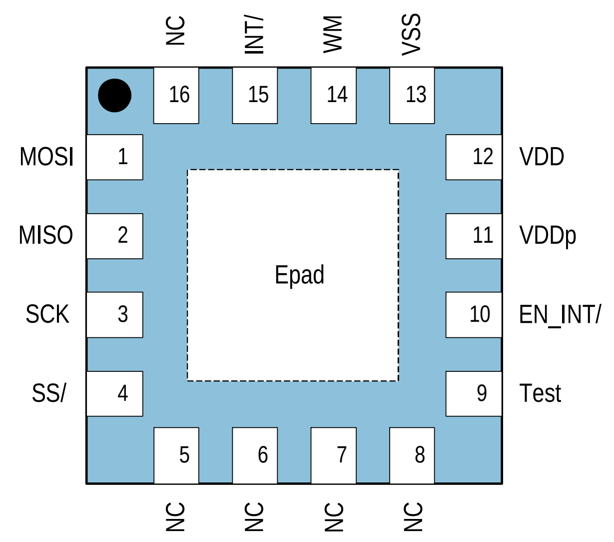


Figure 4:
Pin Description

Pin Number	Name	Type	Description
1	MOSI	Digital input	SPI bus data input
2	MISO	Digital output, tri-state buffer	SPI bus data output
3	SCK	Digital input Schmitt trigger	SPI clock
4	SS/	Digital input	SPI Slave Select, active low
5	NC	-	Leave unconnected
6	NC		
7	NC		
8	NC		
9	Test	Analog	Test pin, connect to VSS
10	EN_INT/	Digital input	Enable interrupt, active low

Pin Number	Name	Type	Description
11	VDDp	Supply	Peripheral power supply, 1.8V to VDD
12	VDD		Analog and digital power supply, 3.0V to 3.6V
13	VSS		Ground
14	WM	Digital I/O	**Low:** 3-wire mode **High:** 4-wire mode
15	INT/	Digital output, tri-state buffer	Interrupt output. Active LOW, when conversion is finished
16	NC	-	Leave unconnected
Epad	-	-	Exposed pad, leave unconnected

Absolute Maximum Ratings

Stresses beyond those listed in "Absolute Maximum Ratings" on page 5 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in "Electrical Characteristics" on page 6 is not implied. Exposure to absolute maximum rating conditions for periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
		Electrical Parameters			
VDD	DC supply voltage	-0.3	5.0	V	
VDDp	Peripheral supply voltage	-0.3	VDD+0.3	V	
V_{IN}	Input pin voltage	-0.3	5.0	V	
I_{scr}	Input current (latchup immunity)	-100	100	mA	Norm: JEDEC 78
		Electrostatic Discharge			
ESD	Electrostatic discharge	±1	-	kV	Norm: MIL-STD-883 E method 3015
		Continuous Power Dissipation			
Θ_{JA}	Package thermal resistance	-	33.5	°C/W	Velocity=0, Multi Layer PCB; JEDEC Standard Testboard
P_t	Total power dissipation		36	mW	
		Temperature Ranges and Storage Conditions			
T_{strg}	Storage temperature	-55	125	°C	
T_{BODY}	Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
	Humidity non-condensing	5	85	%	
MSL	Moisture Sensitive Level	3			Represents a maximum floor life time of 168h

Electrical Characteristics

Operating Conditions

Figure 6:
Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
VDD	DC supply voltage		3.0	3.6	V
VDDp	Peripheral supply voltage		1.8	VDD	V
V_{IN}	Input pin voltage		-0.3	VDDp +0.3	V
T_{amb}	Ambient operating temperature		-40	85	°C
	External components	Power supply filter, pin VDD (see "Power Supply Filter" on page 10)	2.2	4.7	µF
			15	33	Ω
		Ceramic capacitor, pin VDDp to VSS	100		nF

System Parameters

Figure 7:
System Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{on}	Current consumption	Normal operating mode			8.5	mA
I_{off}	Current consumption	Low power mode with activated POR (POR_OFF = 0x00) – default setting			33	µA
		Low power mode with deactivated POR (POR_OFF = 0x5A)			3	µA
$t_{readout}$	Readout rate	Time between READ ANGLE command and INTERRUPT			500	µs
t_{PwrUp}	Power up time	Minimum time after power up before the sensor is operational			580	µs
R_d	Lateral displacement range	Misalignment of the center of the magnet to the center of the die			±0.5	mm
B_Z	Magnetic input field		30		90	mT
B_{Z00}	Magnetic input field range	Gain = 00	58		90	mT

Symbol	Parameter	Conditions	Min	Typ	Max	Units
B_{Z01}	Magnetic input field range	Gain = 01	51		80	mT
B_{Z10}	Magnetic input field range	Gain = 10	39		62	mT
B_{Z11}	Magnetic input field range	Gain = 11	30		47	mT
N_{00}	Noise (rms)	Within B_{z00} magnetic input field range and Gain = 00			0.128	deg_{rms}
N_{01}	Noise (rms)	Within B_{z01} magnetic input field range and Gain = 01			0.149	deg_{rms}
N_{10}	Noise (rms)	Within B_{z10} magnetic input field range and Gain = 10			0.192	deg_{rms}
N_{11}	Noise (rms)	Within B_{z11} magnetic input field range and Gain = 11			0.256	deg_{rms}
INL	Integral Non Linearity	Using Bomatec 6x2.5 mm NdFeB magnet with a maximum x/y-displacement radius of 250 µm from package center	-1.41		1.41	deg
$R_{PU/PD}$	Recommended pull-up or pull-down resistor	Applicable for daisy chain configuration	10k		50k	Ω

DC/AC Characteristics

Digital pads: MISO, MOSI, SCK, SS/, EN_INT/, INT/, WM

Figure 8:
DC/AC Characteristics

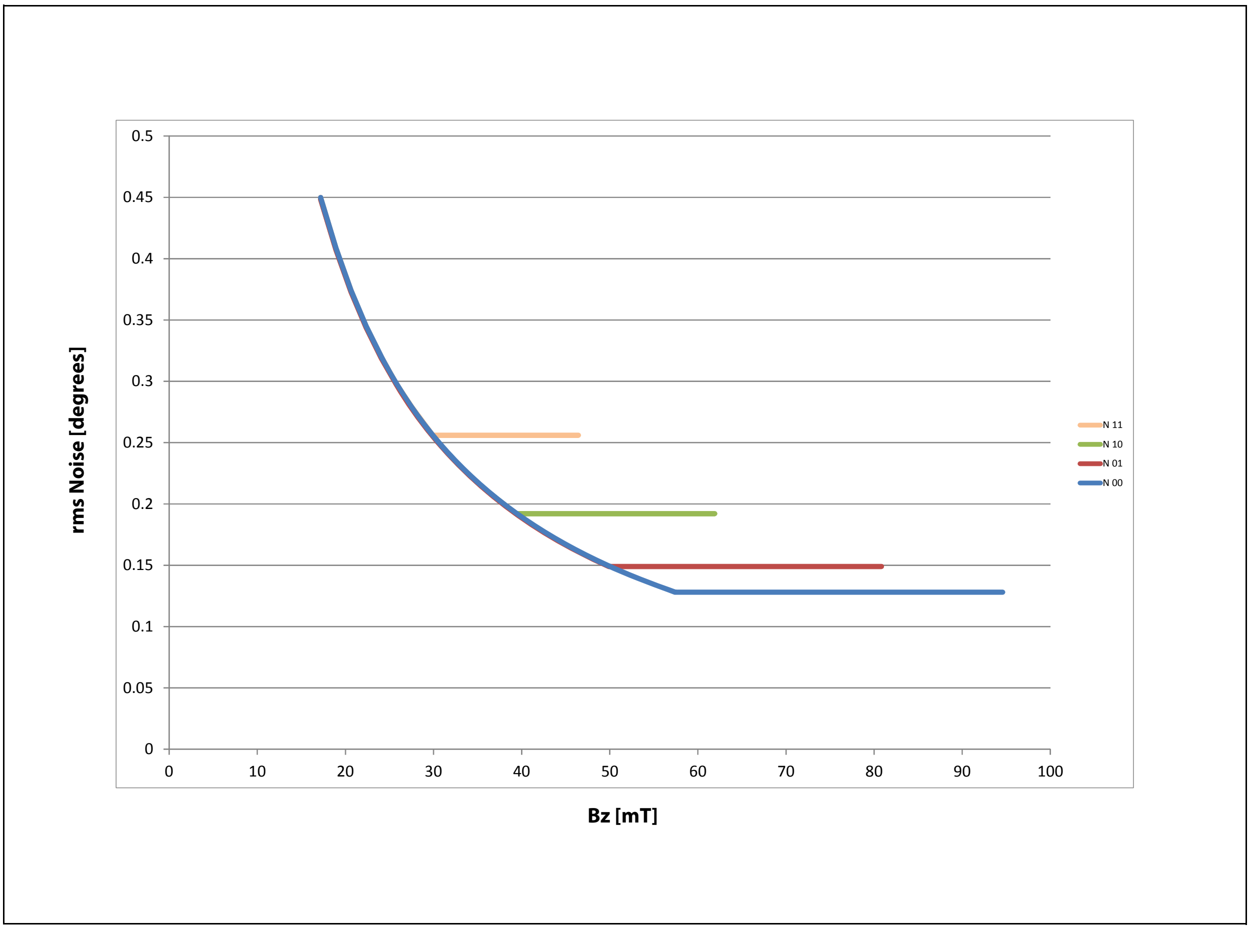
Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High level input voltage		0.7 * VDDp		V
V_{IL}	Low level input voltage	VDDp > 2.7V		0.3 * VDDp	V
V_{IL}	Low level input voltage	VDDp < 2.7V		0.25 * VDDp	V
I_{LEAK}	Input leakage current			1	µA
V_{OH}	High level output voltage		VDDp - 0.5		V
V_{OL}	Low level output voltage			VSS + 0.4	V
C_L	Capacitive load			35	pF

Detailed Description

Noise Performance

This figure shows the Worst Case Noise Performance of the AS5055A at different gain settings which can be set in the Gain Register.

Figure 9:
Worst Case Noise Performance of the AS5055A



Typical Application

The AS5055A uses on-chip Hall elements to convert the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals from the Hall elements are amplified and filtered by the analog front-end (AFE) before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the hardwired CORDIC (coordinate rotating digital computer) block to compute the angle and magnitude of the magnetic vector. The intensity of the magnetic field (magnitude) is used by the automatic gain control (AGC) to adjust the amplification level for compensation of temperature and magnetic field variations.

The internal 12-bit resolution is available by reading a register through the SPI interface. The IC settings in the AS5055A can be programmed through the SPI interface without any dedicated programmer.

Figure 10:
Typical Application Using SPI 4-Wire Mode and INT/ Output

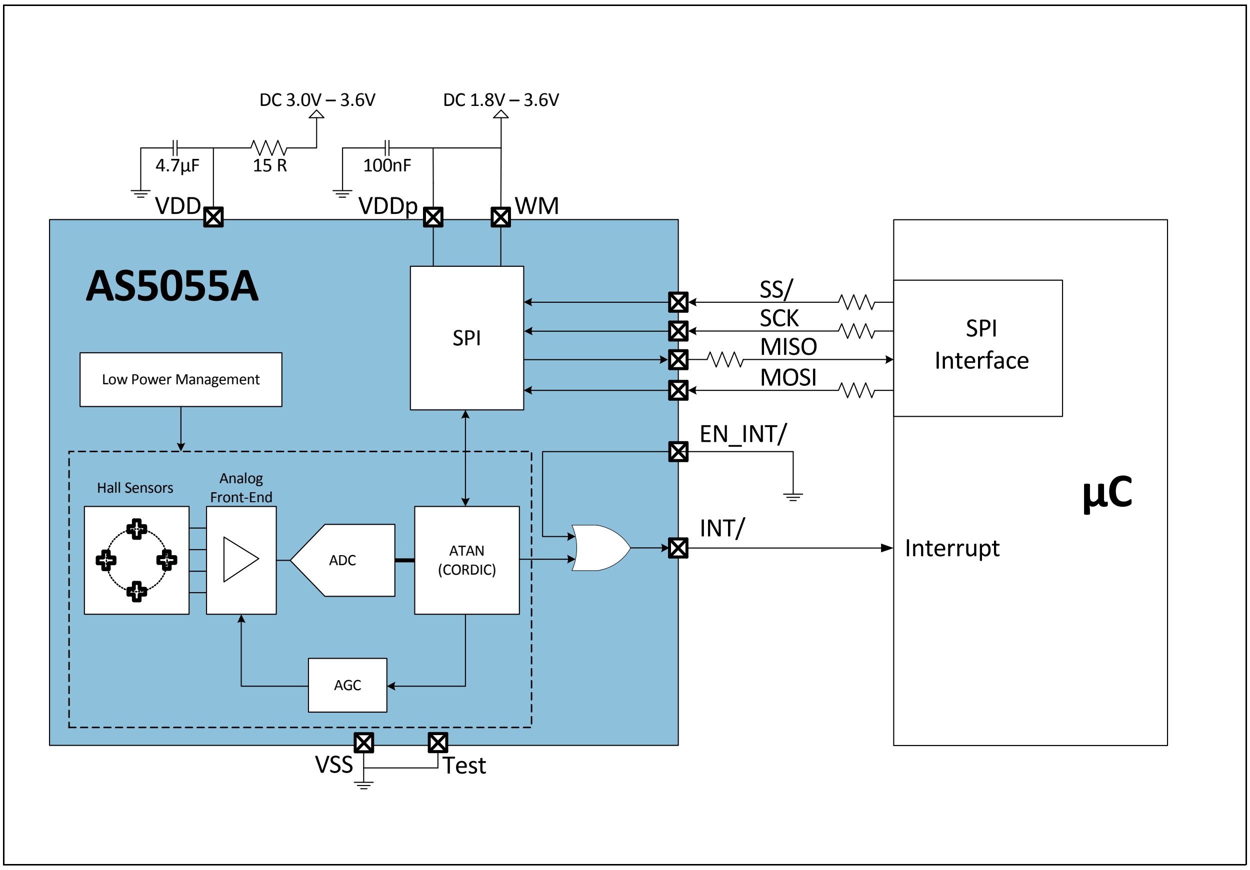


Figure 10 shows how the AS5055A can be connected to a microcontroller. The SPI interface is a slave interface for accessing the on-chip registers. The INT/ output is an active-low interrupt for informing the host microcontroller when a new result is available.

Power Supply Filter

Due to the sequential internal sampling of the Hall sensors, fluctuations on the analog power supply (pin#12: VDD) may cause additional jitter of the measured angle. This jitter can be avoided by providing a stable VDD supply.

The easiest way to achieve that is to add a RC filter: 15Ω in series and 4.7µF to ground as shown in Figure 10.

Alternatively, a filter: 33Ω + 2.2µF may be used. However with this configuration, the minimum supply voltage is 3.15V.

Reading an Angle

Sending a READ ANGLE command through the SPI interface automatically powers up the chip, drives INT/ high and starts another angle measurement. The completion of the angle measurement is indicated by driving the INT/ output low and clearing the WOW flag in the error status register. The microcontroller can respond to the interrupt by reading the angle value from the AS5055A over the SPI interface. (See Figure 11).

A READ ANGLE command must not be sent while a measurement is being performed as indicated by INT/ driven high or WOW = 1.

Reducing the Angle Jitter

The chip only performs a single angle measurement after a READ ANGLE command is received, after which it returns to low-power mode, so it is in normal operating mode for only a very short time (t_{PwrUp}).

The angle jitter can be reduced by averaging several angle measurements in the microcontroller. For example, an averaging of four samples reduces the jitter by 6dB (50%).

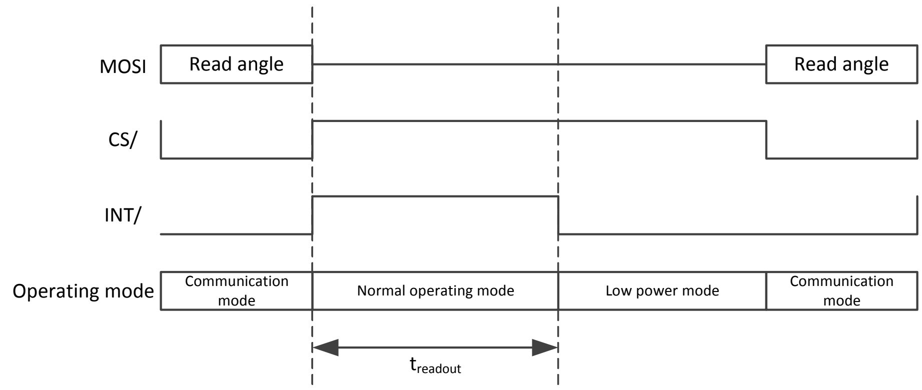
Operating Modes

After a READ ANGLE command is sent, the angle is measured and internal calculations are started. During this time (normal operating mode) the INT/ output is high until the device finishes the calculations and a second READ ANGLE command may not be sent.

After the INT/ output is driven low the device goes into low-power mode. If the microcontroller doesn't monitor the INT/ output a minimum guard time ($t_{readout}$) must be inserted before the next READ ANGLE command can be sent.

After startup the AS5055A has higher power consumption than during low-power mode. When the POR cell is deactivated the chip uses less current during low-power mode (see POR Off Register).

Figure 11:
Operating Modes



Note: Even in low power mode, the power supply must be capable of supporting the active current (I_{on}) at least for maximum $t_{readout}$, until the AS5055A is suspended to low power mode.

Daisy Chain

The AS5055A allows a Daisy Chain configuration as shown in Figure 21.

In this configuration the microcontroller can read multiple AS5055A chips using only 5 wires.

SPI Interface

The 16-bit SPI interface provides read/write access to the on-chip registers. The interface only supports slave operation mode. It communicates at clock rates up to 10 MHz.

The AS5055A SPI uses mode=1 (CPOL=0, CPHA=1) to exchange data. As shown in Figure 12, a data transfer starts with the falling edge of CSn (SCL is low). The AS5055A samples the MOSI input on the falling edge of SCL. SPI commands are executed at the end of the frame (rising edge of CSn). The bit order is MSB first. Data is protected by parity.

SPI Timing

Figure 12:
SPI Timing Diagram

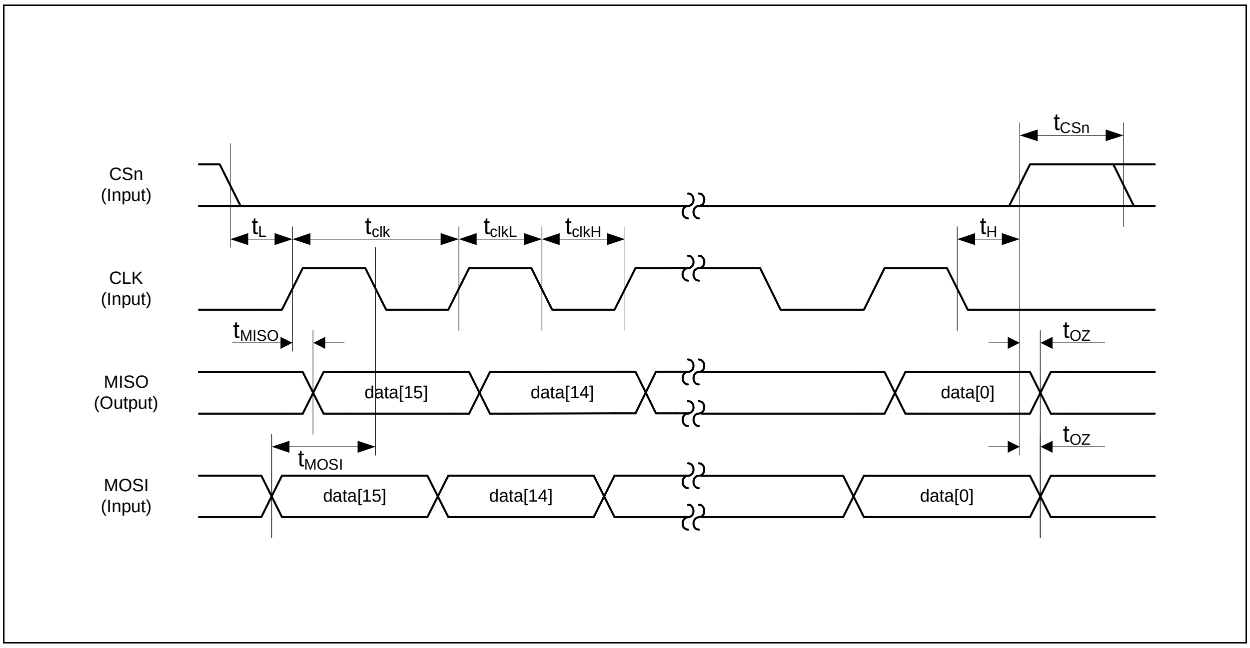


Figure 13:
SPI Timing

Parameter	Description	Min	Max	Unit
t_L	Time between CSn falling edge and CLK rising edge	50		ns
t_{clk}	Serial clock period	100		ns
t_{clkL}	Low period of serial clock	50		ns
t_{clkH}	High period of serial clock	50		ns
t_H	Time between last falling edge of CLK and rising edge of CSn	50		ns
t_{CSn}	High time of CSn between two transmissions	50		ns
t_{MOSI}	Data input valid to falling clock edge	20		ns
t_{MISO}	CLK edge to data output valid		35	ns
t_{OZ}	Release bus time after CS rising edge.		50	ns

SPI Wire Mode Selection

The SPI interface can be set in two different modes: 3-wire mode or 4-wire mode.

Figure 14:
Wire Mode Selection

WM (Pin 14)	Connection option
0	3-wire mode
1	4-wire-mode

SPI Transaction

An SPI transaction consists of a 16-bit command frame followed by a 16-bit data frame. Figure 15 shows the structure of the command frame.

SPI Command Frame

Figure 15:
SPI Command Frame

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R/W	Address 14:1														PAR

Bit	Name	Description
15	R/W	0=Write, 1=Read
14:1	Address	14 bit address to read or write
0	PAR	Parity bit (even) calculated on the upper 15 bits

To increase the reliability of communication over the SPI, an even parity bit (PAR) must be generated and sent. A wrong setting of the parity bit causes the PARITY bit in the error status register of the AS5055A to be set. The parity bit is calculated from the upper 15-bits of the command frame. The 16-bit command specifies the address and whether the transaction is a read or a write.

SPI Read Data Frame

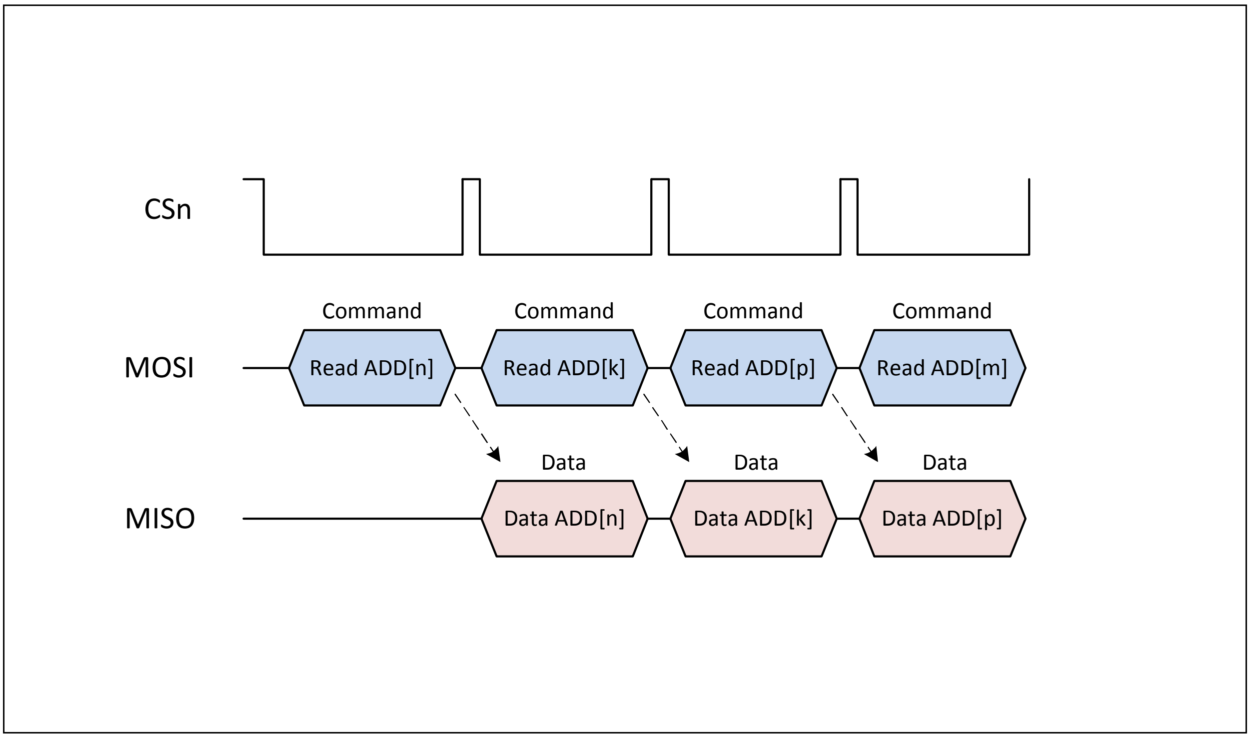
Figure 16:
SPI Read Data Frame

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data 15:2														EF	PAR

Bit	Name	Description
15:2	Data	14 bit read data
1	EF	0 = no command frame error occurred, 1 = error occurred
0	PAR	Parity bit (even) calculated on the upper 15 bits

The data is sent from the AS5055A to the microcontroller on the MISO output. The parity bit PAR is calculated for the upper 15 bits. If an error is detected in the previous SPI command frame, the EF bit is set. The addressed register is sampled on the rising edge of CSn and the data is transmitted on MISO with the next read command, as shown in Figure 17.

Figure 17:
SPI Read



SPI Write Data Frame

Figure 18:
SPI Write Data Frame

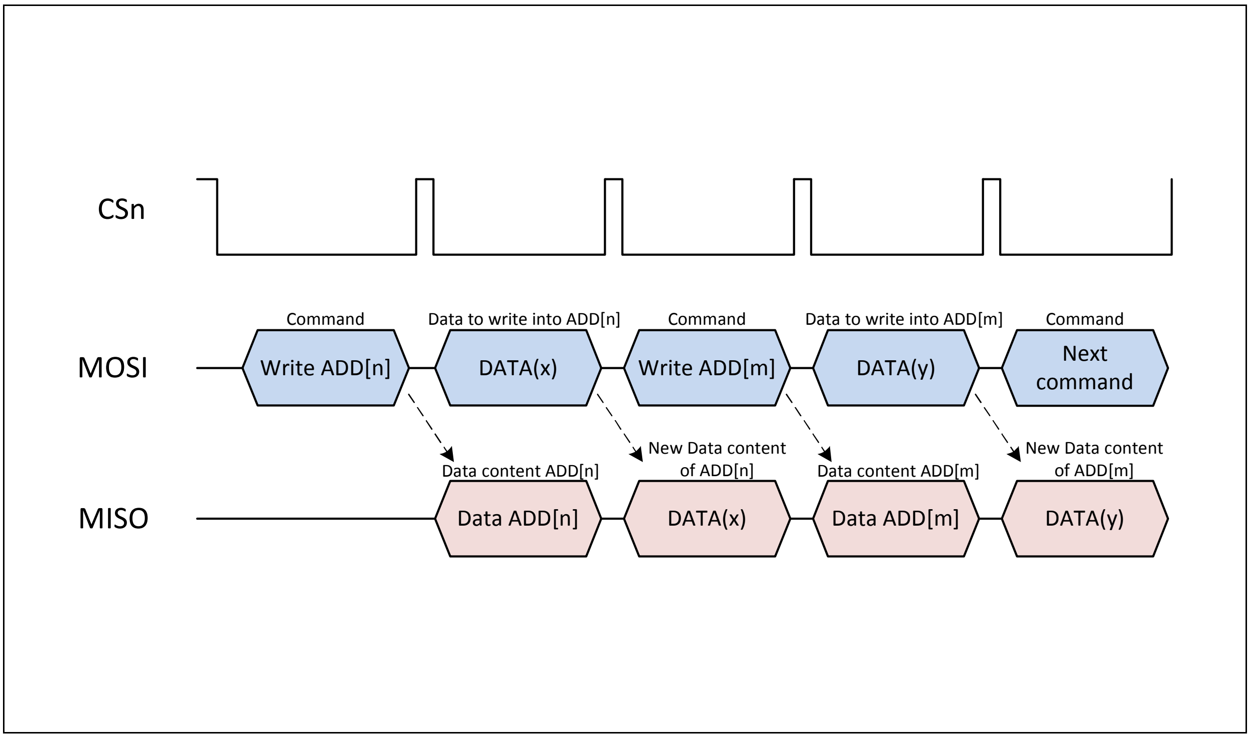
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data 15:2														DC	PAR

Bit	Name	Description
15:2	Data	14 bit write data
1	DC	Don't Care
0	PAR	Parity bit (even) calculated on the upper 15 bits

The parity bit PAR is calculated for the upper 15 bits.

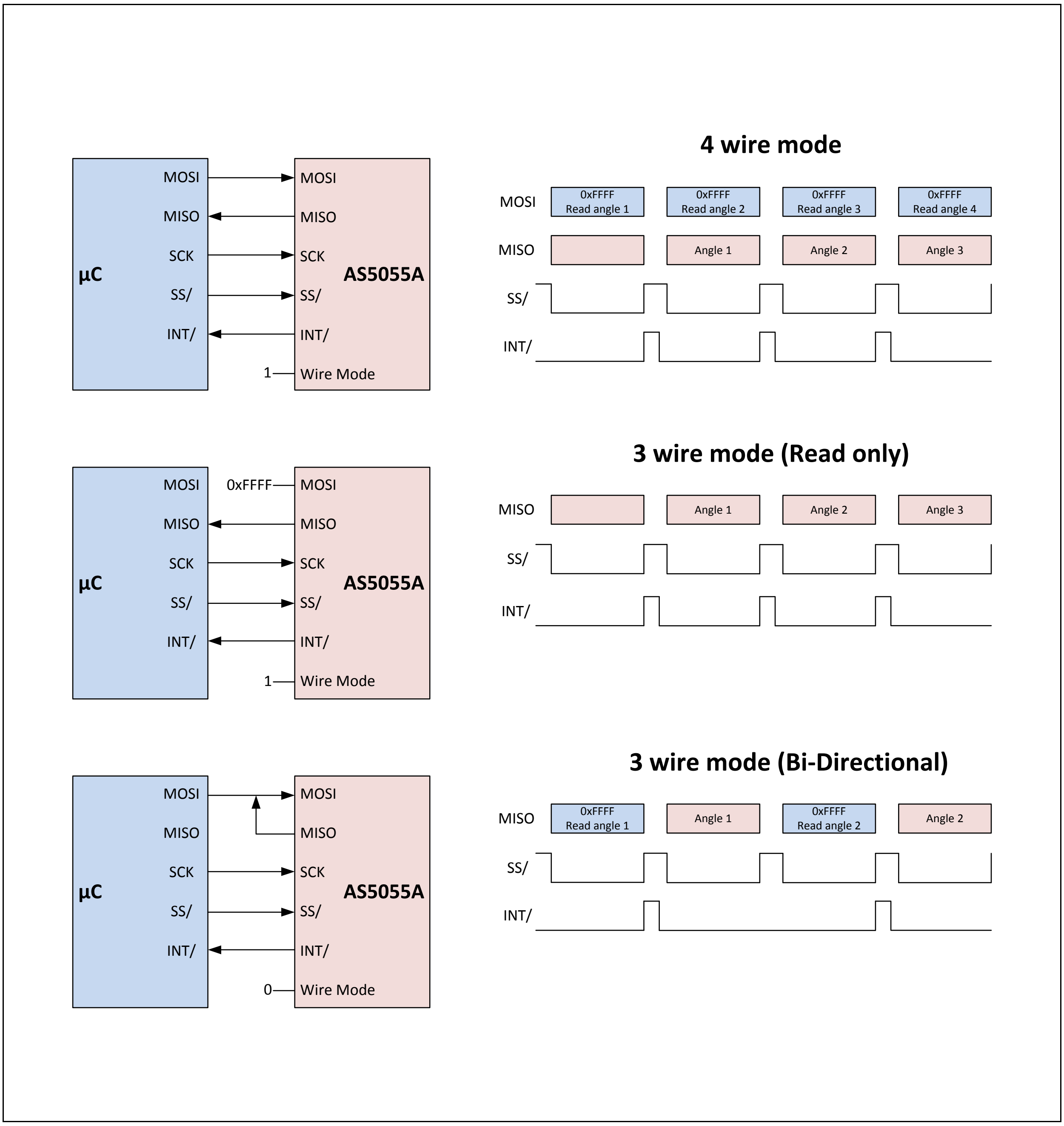
In a SPI write transaction, the write command frame (e.g. Write ADD[n]) is followed by a data frame (e.g. DATA [x]). In addition to writing an address in the AS5055A, a write command frame causes the old contents of the addressed register (e.g. DATA [y]) to be sent on MISO in the following frame. This is followed by the new contents of the addressed register (DATA [x]) as shown in Figure 19.

Figure 19:
SPI Write Transaction



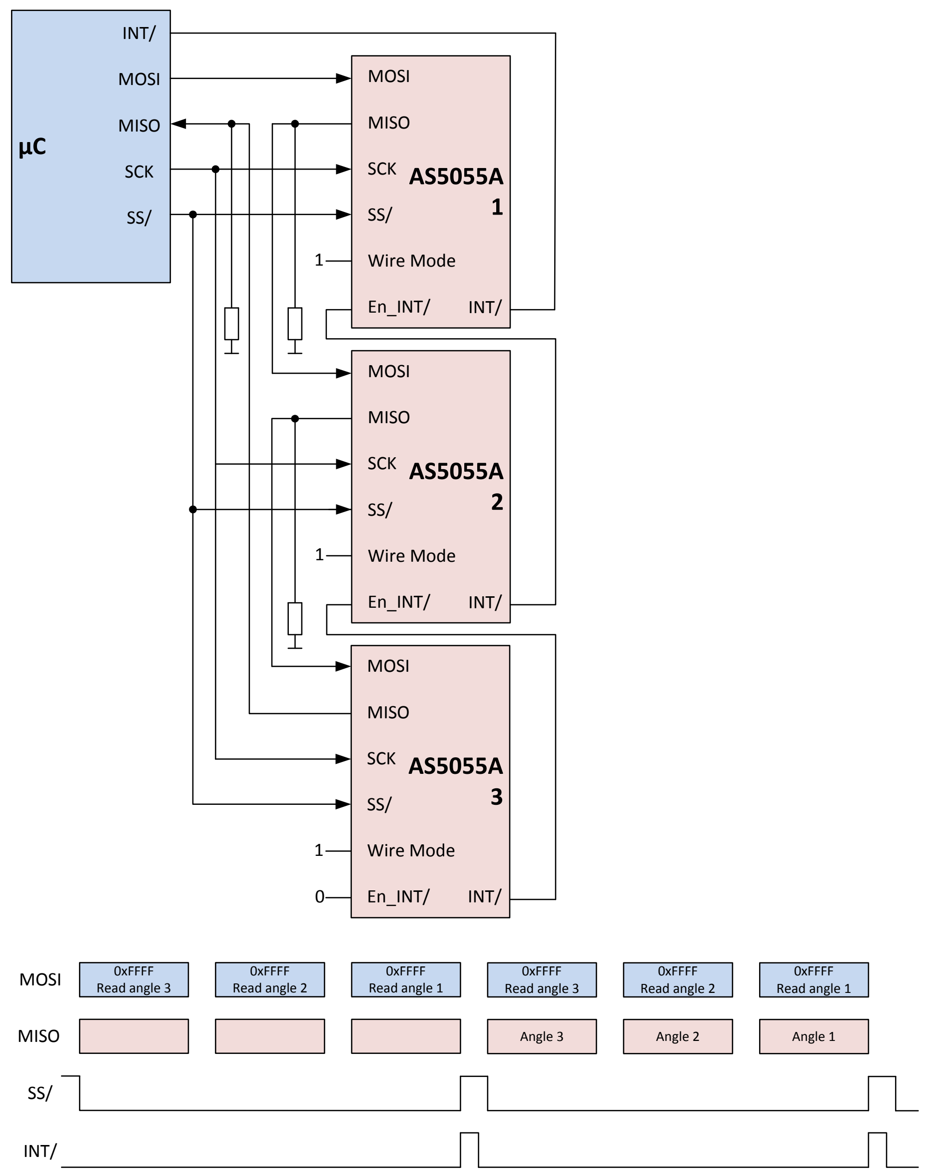
SPI Connection to the microcontroller

Figure 20:
Single Slave Mode



Daisy Chain, 4 Wire

Figure 21:
Daisy Chain, 4 Wire



Registers

The on-chip registers are shown in Figure 22.

Figure 22:
Registers

Name	Address	Bits	Mod	Default	Description
POR Off	0x3F22	7:0	R/W	0x0000	Power On Reset Off
Software Reset	0x3C00	13:0	W	0x0000	Software Reset
Master Reset	0x33A5	13:0	W	0x0000	Master Reset
Clear EF	0x3380	13:0	R	0x0000	Clear Error Flag
NOP	0x0000	13:0	W	0x0000	No Operation
AGC	0x3FF8	5:0	R/W	0x0020	Automatic Gain Control
Angular Data	0x3FFF	13:0	R	0x0000	Measured Angle
Error Status	0x335A	13:0	R	0x0000	Error Status Register
System Config	0x3F20	9:13	R	0x000	System Configuration Register 1

POR Off (0x3F22)

Writing the value 0x5A to the POR Off Register (0x3F22) deactivates the POR cell and reduces the current consumption in low power mode (I_{off}).

Software Reset (0x3C00)

Writing to the Software Reset Register initiates a Software Reset. With the RES SPI bit of the Data Package set to 1 it is possible to reset the SPI registers. After a software reset a new angle conversion is started; this is needed to set the AS5055A into an initial state. This angle is not readable by the microcontroller.

The AS5055A is ready as soon as INT/ is driven low or a minimum time ($t_{readout}$) has elapsed.

Figure 23:
Software Reset Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	0	1	1	1	1	0	0	0	0	0	0	0	0	0	DC	PAR

Figure 24:
Data Package

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DC													RES SPI	DC	PAR

Bit	Name	Description
15:3	DC	Don't Care
2	RES SPI	If set to 1 the SPI registers are reset as well
1	DC	Don't Care
0	PAR	Parity bit (even) calculated on the upper 15 bits

Master Reset (0x33A5)

Writing to the Master Reset Register initiates a Master Reset. This is similar to the Software Reset with the difference that no data package is needed.

Figure 25:
Master Reset Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	0	1	1	0	0	1	1	1	0	1	0	0	1	0	1	PAR

Clear Error Flag (0x3380)

Reading from the Clear Error Flag Register clears the Error Flag which is contained in every Read Data Frame. The Read data is 0x0000 which indicates a successful clear command.

Figure 26:
Clear Error Flag Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	PAR

Possible Conditions which force the Error Flag to be set:

- Wrong parity
- Wrong command
- Wrong number of clocks

Note: If the error flag is set to 1 because of a communication problem the flag remains set until a Clear Error Flag Command is executed.

No Operation (0x0000)

The No Operation (NOP) command represents a dummy write to the AS5055A. If no error happens the chip responds with 0x0000.

Figure 27:
NOP Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PAR

AGC – Automatic Gain Control (0x3FF8)

Writing a value different than zero to this register, stops the AGC loop and keeps a constant AGC value.

Figure 28:
AGC

Name	Read/Write	Bit Position	Description
AGC	R/W	5:0	Automatic Gain Control value

Angular Data (0x3FFF)

Figure 29:
Angular Data

Name	Read/Write	Bit Position	Description
Alarm Lo	R	13	Alarm flag, which indicates a too low magnetic field
Alarm Hi	R	12	Alarm flag, which indicates a too high magnetic field
Angle Value	R	11:0	Angular value in 12 bit binary code

Alarm Bits

Figure 30:
Alarm Bits

Alarm Hi	Alarm Lo	Description
0	0	AGC level is higher than the minimum value and lower than the maximum value.
0	1	AGC level is equal or even lower than the minimum level. Magnetic field is too weak.
1	0	AGC level is equal or even higher than the maximum level. Magnetic field is too strong.
1	1	Indicates if a major system error has occurred. (Error flags can be read out with the error status register)

Error Status (0x335A)

For detailed information of the Error Status Register please refer to "Error Monitoring" on page 22.

System Configuration Register 1 (0x3F20)

Figure 31:
System Configuration Register

Name	Read/Write	Bit Position	Description
Resolution	R	13:12	00 indicates 12 bit resolution
Chip ID	R	11:9	Silicon version 010
Gain	R	4:3	Sets gain setting

Error Monitoring

The correct operation and communication of the AS5055A is ensured by several error flags. Every read access is supported by a communication error flag (EF) to indicate a transmission error in a previous host transmission.

For additional information on the Error Status, please refer to the application note *AN5000_ErrorMonitoring*.

Error Status Register

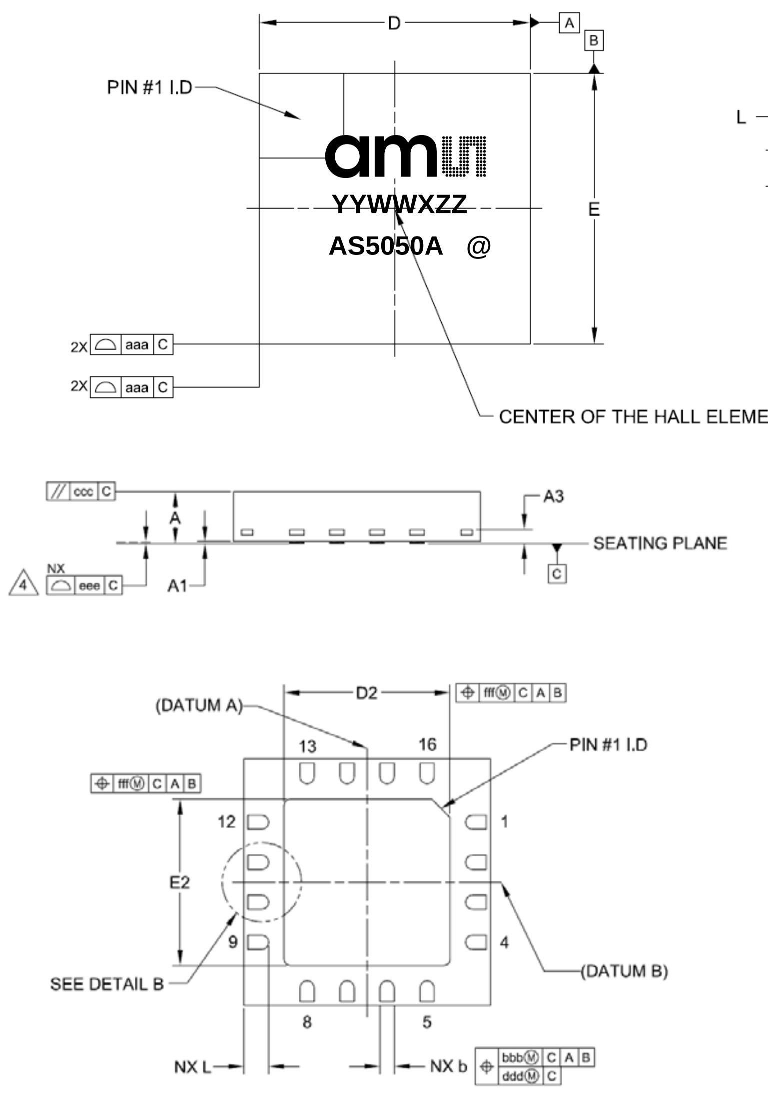
Figure 32:
Error Status Register and Description

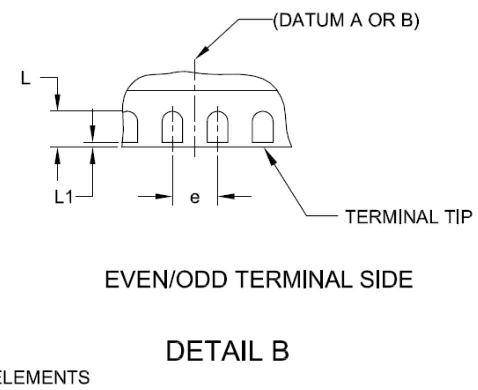
Bit	Type	Description
		Error Status DSP
13	Reserved	
12	FIELD_ALARM_LO	AGC level is equal or even higher than the maximum level. Magnetic field is too weak.
11	FIELD_ALARM_HI	AGC level is equal or even lower than the minimum level. Magnetic field is too strong.
10	RANGE	The RANGE flag signals that the Hall bias circuit has reached the head room limit. This might occur at the combination of low supply voltage, high temperature and low magnetic field. In this case, manually reducing the AGC setting (Figure 28) can be used to recover a valid Hall biasing condition.
9	CORDICOV	The CORDIC calculates the angle. An error occurs when the input signals of the CORDIC are too large. The internal algorithm fails.
8	ADCOV	The ADCOV bit occurs if the magnetic input field strength is too large for at least one Hall element. This can be the case if the magnet is displaced.
		Error Status System
7	Reserved	
6	Reserved	
5	Reserved	
4	WOW	When a READ ANGLE command is in progress, the WOW flag is set to 1. At the end of the measurement the WOW flag is cleared to 0. Only in case of deadlock the WOW flag is stuck high; in which case a MASTER RESET must be sent to clear the deadlock.
		Error Status SPI
3	Reserved	
2	ADDMON	Set to high when non existing address is used.
1	CLKMON	Set to high when the amount of clock cycles is not correct.
0	PARITY	Set to high when the transmitted parity bit does not match to calculated parity bit.

Package Drawings & Markings

The device is available in a 16-pin QFN (4x4x0.9 mm) package. The axis of the magnet must be aligned over the center of the package.

Figure 33:
Package FN – Dual Flat No-Lead Packaging Configuration





Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
L	0.35	0.40	0.45
L1	0	-	0.15
b	0.25	0.30	0.35
D		4.00 BSC	
E		4.00 BSC	
e		0.65 BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		16	

RoHS
Green

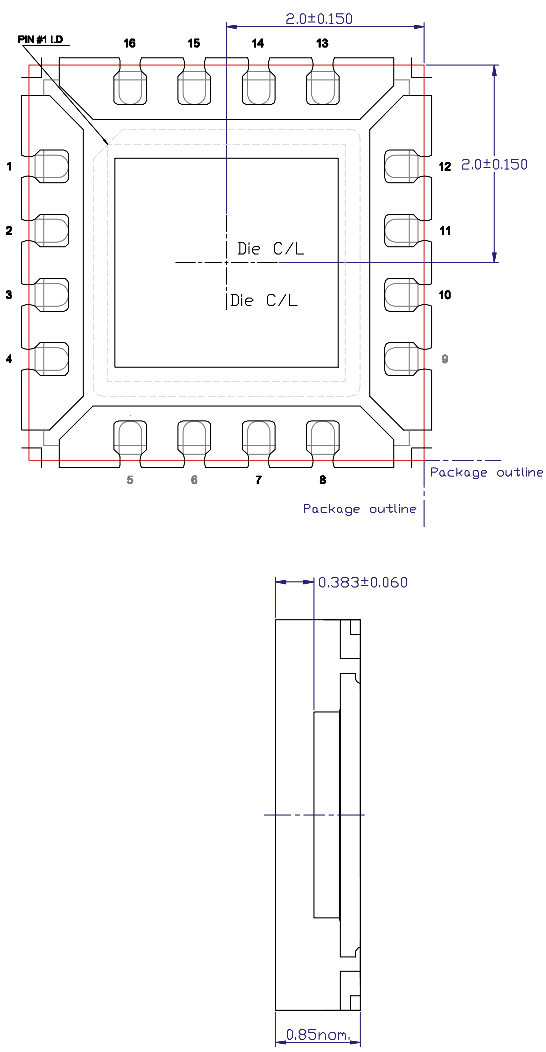
Note(s) and/or Footnote(s):

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.
6. N is the total number of terminals.

Figure 34:
Marking: YYWWXZZ

YY	WW	X	ZZ
Year (i.e. 04 for 2004)	Week	Assembly plant identifier	Assembly traceability code

Figure 35:
Vertical Cross Section of QFN 16-pin 4x4x0.85 mm package



Note(s) and/or Footnote(s):

1. All dimensions in mm.
2. Die thickness 0.254 ± 0.013
3. Adhesive thickness 0.010 ± 10, +0.01, -0.0025
4. Lead frame thickness 0.203 typ.

RoHS Compliant & ams Green Statement

RoHS: The term RoHS compliant means that ams AG products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ams AG knowledge and belief as of the date that it is provided. ams AG bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams AG has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams AG and ams AG suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Ordering & Contact Information

Figure 36:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS5055A-BQFT	16-pin QFN	AS5055A	13" Tape & Reel in dry pack	6000
AS5055A-BQFM	16-pin QFN	AS5055A	7" Tape & Reel in dry pack	500

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Headquarters
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

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