AS5132

360 Step (8.5 bit) Programmable High Speed Magnetic Rotary Encoder

1 General Description

The AS5132 is a contactless magnetic rotary encoder for accurate angular measurement over a full turn of 360 degrees. It is a system-on-chip, combining integrated Hall elements, analog frontend and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip is required.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 8.5 bit = 360 positions per revolution. This digital data is available as serial output over the interface and as a pulse width modulated (PWM) signal.

An additional U,V,W output can be used for a block commutation for a brushless DC motor. An incremental signal is available as an option.

In addition to the angle information, the strength of the magnetic field is also available as a 5-bit code.

A software programmable (OTP) zero position simplifies assembly as the zero position. The magnet does not need to be mechanically aligned.

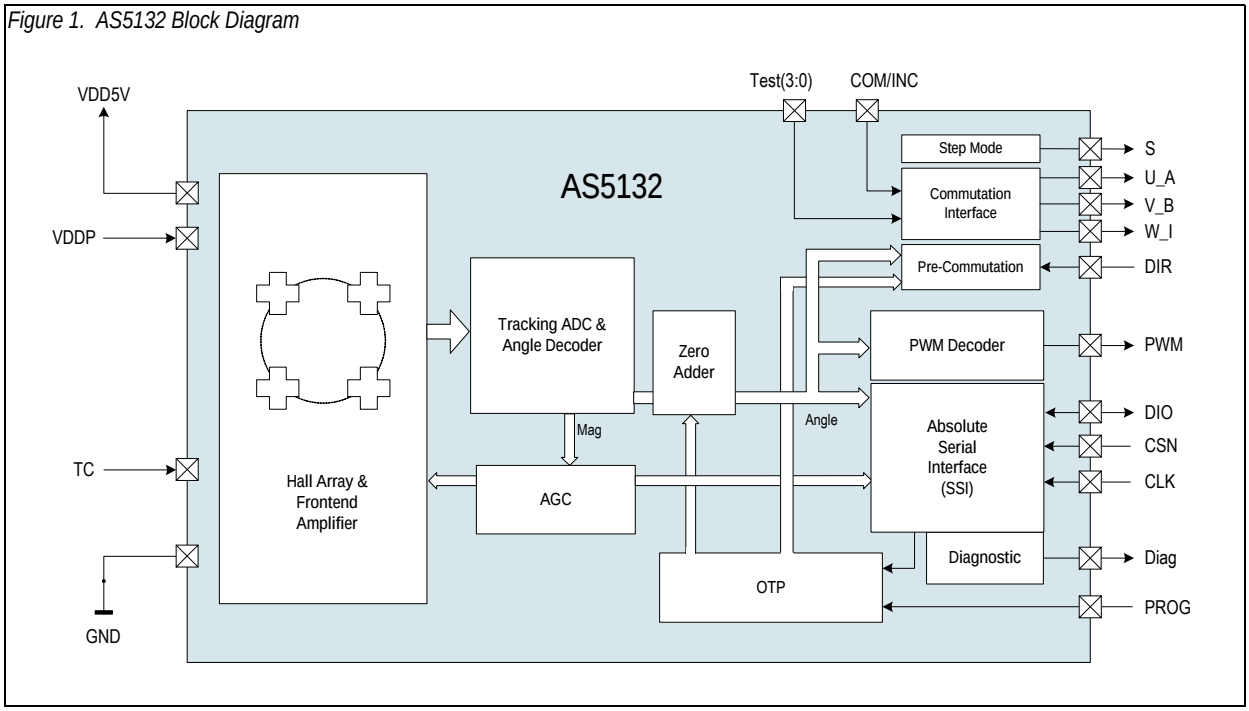
2 Key Features

- 360º contactless angular position sensing
- Two digital absolute outputs (8.5 bit):
  - Serial interface
  - PWM output
- Incremental output with adjustable number of pulses
- BLDC Output UVW, selectable for 1,2,3,4,5,6 pole pairs
- Supports external PWM clock mode
- Static and dynamic pre-commutation feature
- User programmable zero position and sensitivity
- High speed: up to 72,900 rpm
- Direct measurement of magnetic field strength allows exact determination of vertical magnet distance
- Incremental Outputs ABI Quadrature: 90ppr, step direction: 180ppr, fixed pulse width 360ppr
- 9-bit multi turn counter
- Wide magnetic field input range: 20 – 80 mT (typical)
- Wide temperature range: -40ºC to +150ºC
- Thin Small Pb-free package: SSOP 20
- Fully automotive qualified to AEC-Q100, grade 0

3 Applications

The AS5132 is suitable for contactless rotary position sensing, rotary switches (human machine interface), AC/DC motor position control and Brushless DC motor position control.

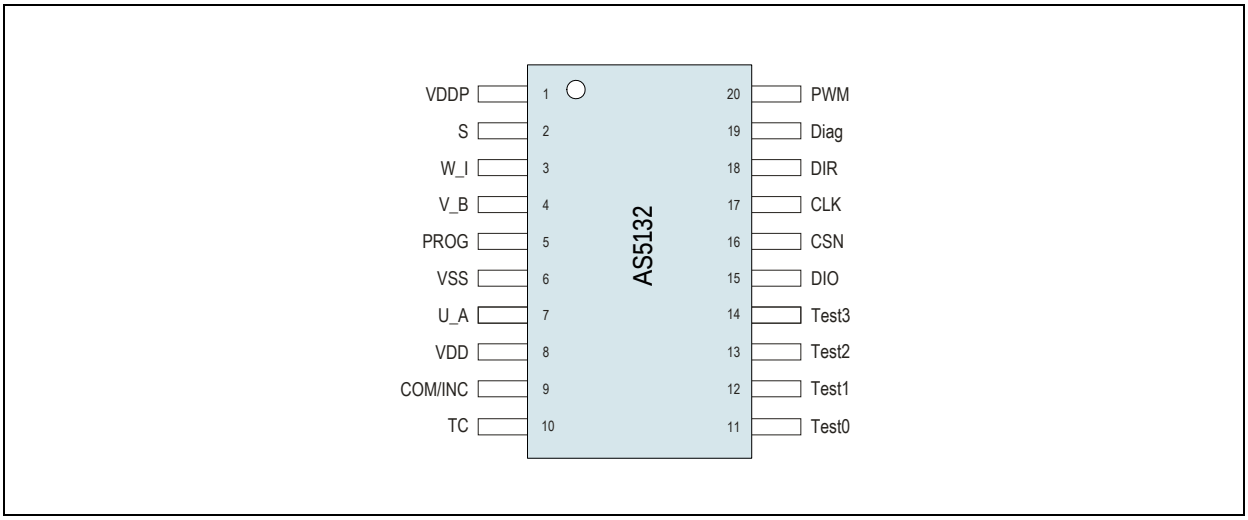
Figure 1. AS5132 Block Diagram



Contents

4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	VDDP	Supply	Supply voltage for the selected pins[1]
2	S	Digital output	Step output (8mA, VDDP)
3	W_I		Commutation output or incremental output
4	V_B		
5	PROG	Supply	Programming voltage input
6	VSS		Supply ground
7	U_A	Digital output	Commutation output or incremental output
8	VDD	Supply	Positive supply voltage
9	COM / INC	Digital input / Schmitt-Trigger	Selection of the output mode. This pin is also used for external clock mode (VDDP)
10	TC	Analog input	Test pin. Set to low in application
11	Test0	Analog input /output	Test pin, selection of output format for incremental or step mode
12	Test1		
13	Test2		
14	Test3		
15	DIO	Bi-directional digital	Data I/O for serial interface (VDDP)
16	CSN	Digital input / Schmitt-Trigger	Chip select input (active low) (VDDP)
17	CLK		Clock input for serial interface (VDDP)
18	DIR		Input signal for the pre-commutation at start-up (VDDP)
19	Diag	Digital output / Open Drain	Diagnostic output (open drain)
20	PWM	Digital output	PWM output (8mA, VDDP)

1. VDDP can be customized to the voltage levels of the peripheral circuitry to economize voltage level drivers.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
Supply voltage (V_{DD})	-0.3	7	V	Except during OTP programming
DC supply voltage (VDDP)	0.3	7	V	Cannot be higher than VDD+0.3
Input Pin Voltage (V_{IN})	VSS-0.5	VDD	V	
Input Current (latch up immunity), (I_{scr})	-100	100	mA	Norm: EIA/JESD78 Class II Level A
Electrostatic Discharge				
ESD		±2	kV	Norm: JESD22-A114E
Temperature Ranges and Storage Conditions				
Storage Temperature (T_{strg})	-55	150	°C	
Body temperature (T_{body})		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*. The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level (MSL)	3			Represents a maximum floor time of 168h

6 Electrical Characteristics

TAMB = -40ºC to 150ºC, VDD = 4.5V to 5.5V, all voltages referenced to VSS, unless otherwise noted.

6.1 Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Positive Supply Voltage		4.5		5.5	V
VDDP	Positive Supply Voltage Periphery		3.0		5.5	V
IDD	Operating Current	No load on outputs. Supply current can be reduced by using stronger magnets.		15	22	mA

6.2 System Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
N	Resolution			8.5		Bit
				1		Deg
T_{PwrUp}	Power Up Time				≤ 4100	µs
t_s	Tracking rate	Step rate of tracking ADC; 1 step = 1º			5.2	µs/step
INL_{cm}	Accuracy	Centered Magnet	-2		2	Deg
		Within horizontal displacement radius	-3		3	
t_{delay}	Propagation delay	Internal signal processing time			22	µs
TN	Transition noise	peak-peak			1.41	Deg

6.3 Magnet Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
B_Z	Magnetic Input Range	At die surface	20		80	mT
V_i	Magnet rotation speed	To maintain locked state[1]			72,900	rpm

1. Maximum rotation speed is dependent on the internal time reference.
   Maximum value is calculated with lowest sequence over all operating conditions.

6.4 Programming Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{PROG}	Programming voltage	Static voltage at pin PROG	8		8.5	V
I_{PROG}	Programming current	During programming			100	mA
$Tamb_{PROG}$	Programming ambient temperature		0		85	ºC
t_{PROG}	Programming time		2		4	µs
$V_{R,prog}$	Analog readback voltage	During analog readback mode at pin PROG			0.5	V
$V_{R,unprog}$			2		3.5	

6.5 DC Characteristics of Digital Inputs

CMOS Inputs COM/INC, CSN, CLK, DIO, DIR

Symbol	Parameter	Min	Typ	Max	Units	Note
V_{IH}	High level input voltage	0.7*VDDP		VDDP	V	COM/INC refer to VDD
V_{IL}	Low level input voltage	0		0.3*VDDP	V	
I_{LEAK}	Input leakage current			1	µA	

6.6 DC Characteristics of Digital Outputs

CMOS Outputs S, U_A, V_B, W_I, PWM, DIO

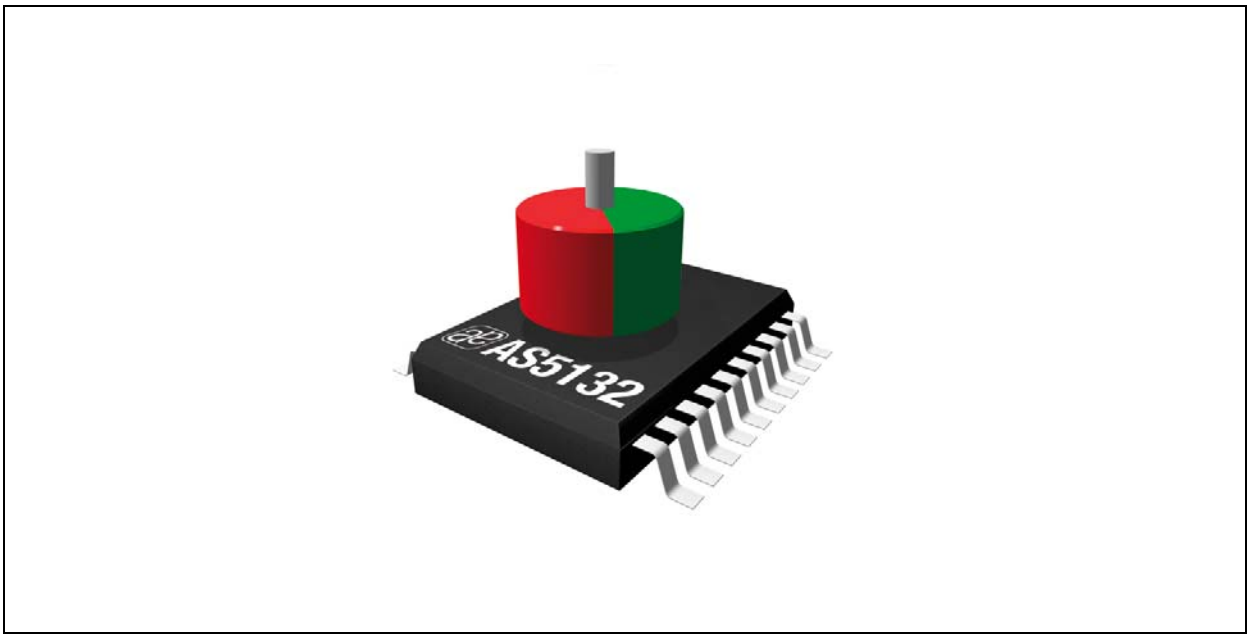
Symbol	Parameter	Min	Typ	Max	Units	Note
V_{OH}	High level output voltage	VDDP-0.5		VDDP	V	PWM and S have 8mA output load, DIO has 4mA output load.
		VDD-0.5		VDD		U_A, V_B, W_I have 4mA output load.
V_{OL}	Low level output voltage	0		VSS+0.4	V	PWM and S have 8mA output load, DIO, U_A, V_B, W_I has 4mA output load.
CL	Capacitive load			35	pF	

6.7 Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CLK}	Clock Frequency	Normal operation		5	6	MHz
f_{CLKP}	Clock Frequency programming	During OTP programming	200		650	kHz
t1	Chip select to positive edge of CLK		15			ns
t2	Setup time command bit, Data valid to positive edge of CLK		30			ns
t3	Hold time command bit, Data valid after positive edge of CLK		30			ns
t4	Float time, Last command bit to negative edge of CLK		30			ns
t5	Transfer time, Negative edge to valid data		30			ns
t6	Last CLK to positive edge CSN		30			ns
t_{CLK}	Clock period		167	200		ns

7 Detailed Description

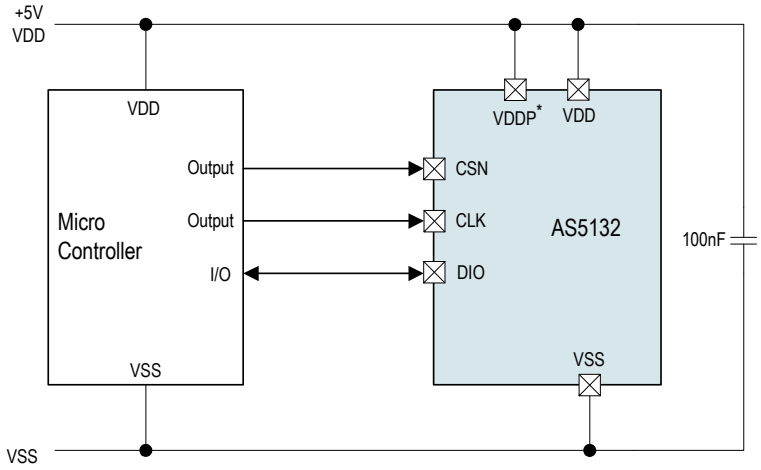
Figure 3. Typical Arrangement of AS5132 and Magnet



7.1 Synchronous Serial Interface (SSI)

The absolute angle data can be read out over the synchronous serial interface using the pins CSN, DIO and CLK. It is a bidirectional interface therefore a read or write access is possible. The organization of the protocol is byte wise and starts with the command byte followed by the data information.

Figure 4. Read / Write Serial Data Transmission



* DIO output pin is connected internally to the VDDP voltage domain. VDD and VDDP can be separately connected too.

Figure 4 shows the connection of the AS5132 to a micro controller. Depending on the command byte are different access types possible. In normal mode the number of clocks is equal the number of data bits.

Figure 5. Data Organization of the SSI Protocol 16-Bit Data

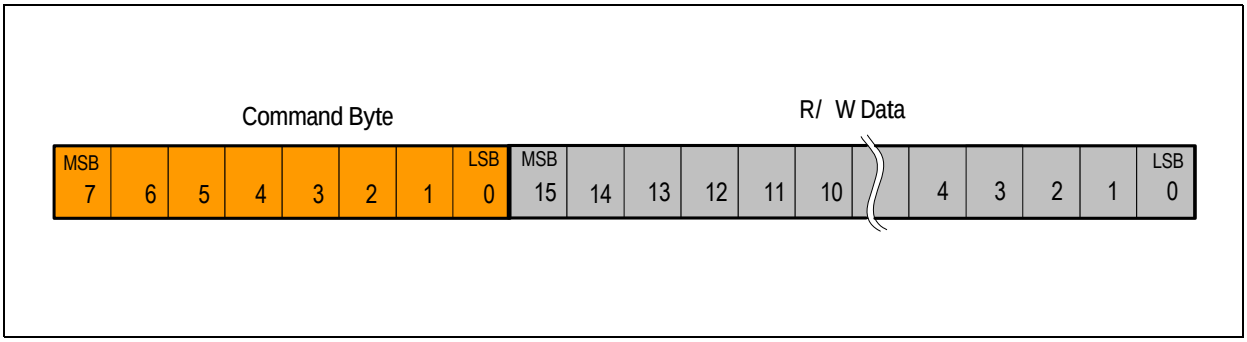


Figure 5 shows the organization of the data. The first section is used to setup the operating mode and the address. During write mode the micro controller drives the data line and generates in addition the CSN and CLK signal. Figure 6 shows this operation.

Figure 6. SSI Timing in Write Mode

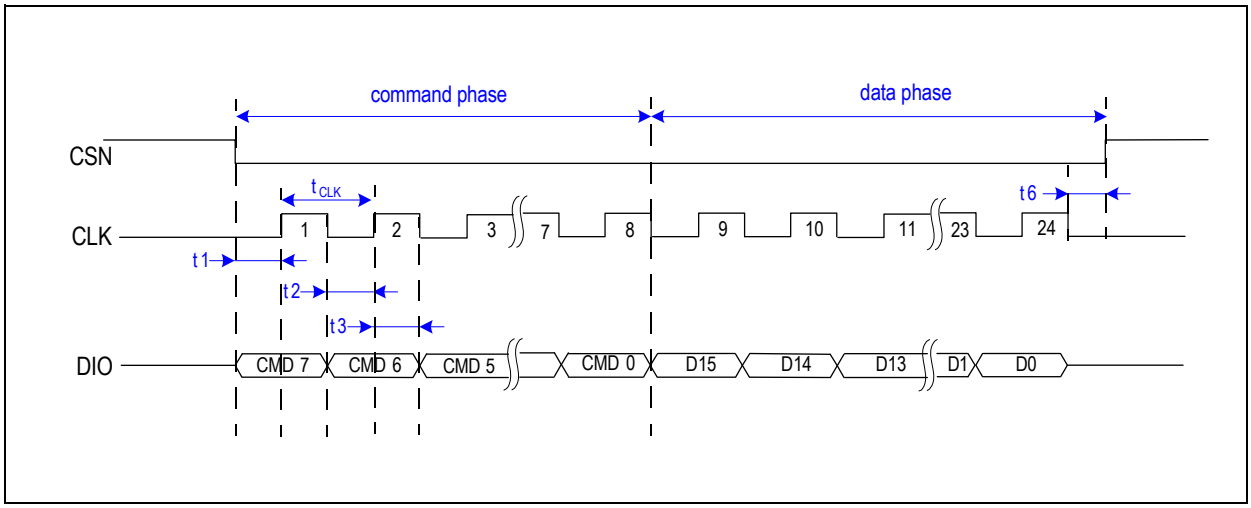


Figure 7. SSI Timing in Read Mode

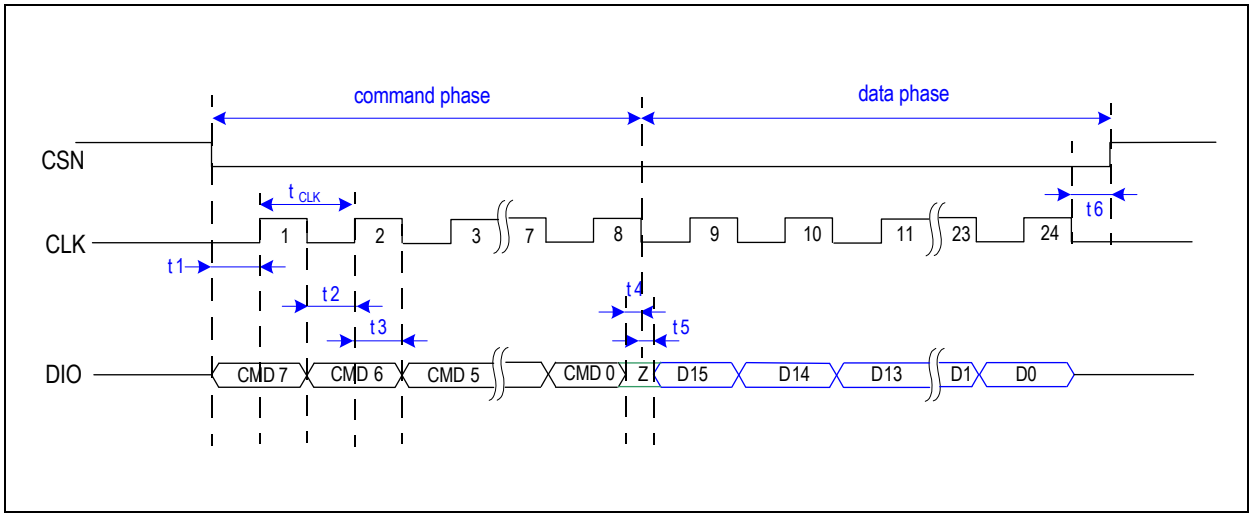


Figure 7 shows the read mode. The first 8 command data bits are written by the microcontroller. After the command data the device takes over the DIO line and writes the data information. A high impedance phase must be considered before the device drives the output line.

7.1.1 Commands of the SSI in Normal Mode

Table 3. Read/Write Interface Commands in Normal Mode

Command Name	Command Data	Access Mode	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
WRITE CONFIG	0001_0111	write		GEN RST	Hyst Dis	PRE_COM_DYN<5:0>						MTC2	MTC1					
SET MT COUNTER	0001_0100	write	MT - COUNTER <8:0>															
EN PROG	1000_0100	write	0	1	1	0	0	1	0	1	0	1	1	1	0	0	0	0
RD MT COUNTER	0000_0100	read	MT - COUNTER <8:0>									EZ ERR						P
RD_ANGLE	0000_0000	read	ANGLE <8:0>									LOCK ADC	AGC <5:1>					P

Note: Gray bits can be ignored by the user.

GEN RST: A HI generates a reset of the AS5132. GEN RST must be set to LO after reset.

Hyst_Dis: Hysteresis disable.

PRE_COM_DYN <5:0>: Absolute dynamic pre-commutation value. Depending on the setup of the pole pairs, a mechanical angle offset can be adjusted. The range is 0 to 63 mechanical degrees (LSBs).

MT-COUNTER <8:0>: The multiturn counter can be set or read over the interface.

EN PROG: This command with this data enables the access to the OTP register in extended mode. OTP Programming mode is only possible in extended mode with special connection (see Figure 11).

EZ ERR: Indicates a wrong operation of the OTP memory after programming at room temperature.

ANGLE <8:0>: Absolute angle information with angular true resolution (360 steps).

LOCK ADC: Indicates a locked ADC. An angle value is only valid in case of a locked ADC. During sleep mode is the LOCK ADC bit LO.

AGC <5:1>: Automatic gain control value indicates the magnetic field strength.

P: Parity information of the 15 data bits. Odd parity.

7.1.2 Extended Synchronous Serial Interface Mode

The absolute angle data can be read out over the synchronous serial interface using the pins CSN, DIO and CLK. It is a bidirectional interface therefore a read or write access is possible. The organization of the protocol is byte wise and starts with the command byte followed by the data information.

Figure 8. Connectivity During Programming in Extended Mode

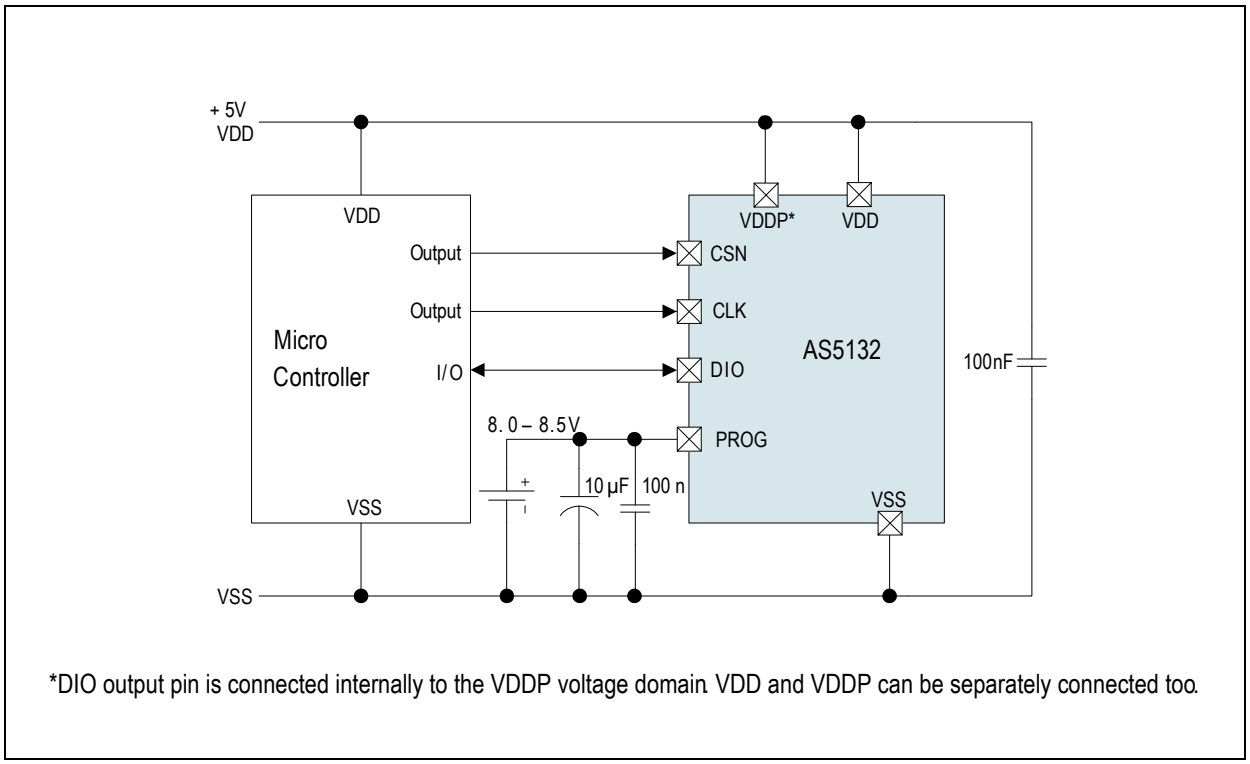


Figure 9. SSI Timing in Extended Write Mode

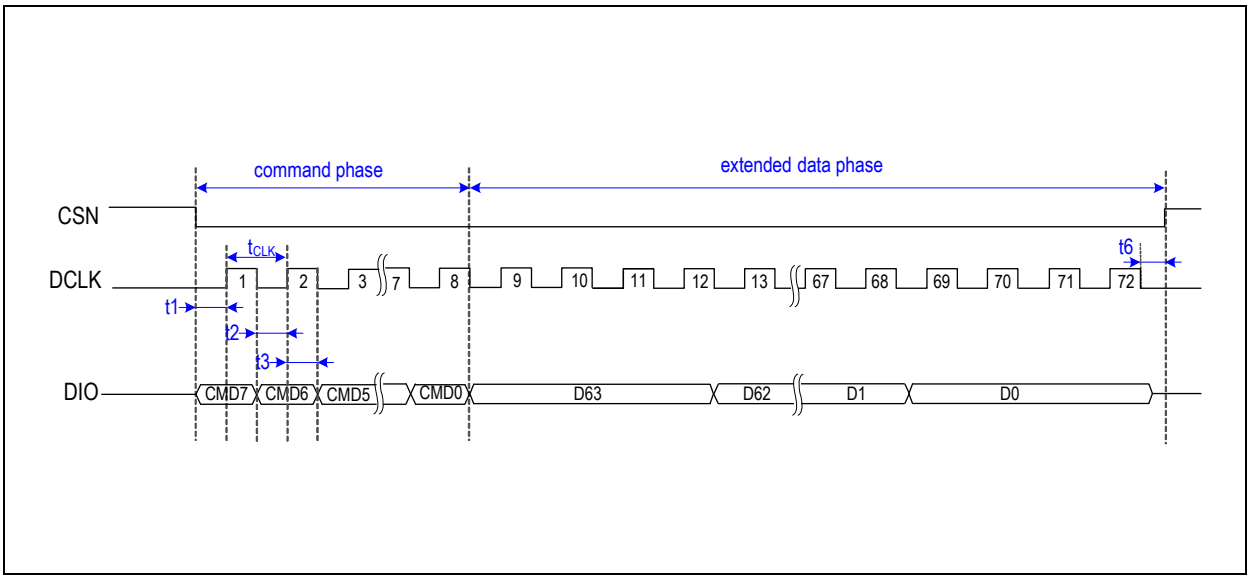
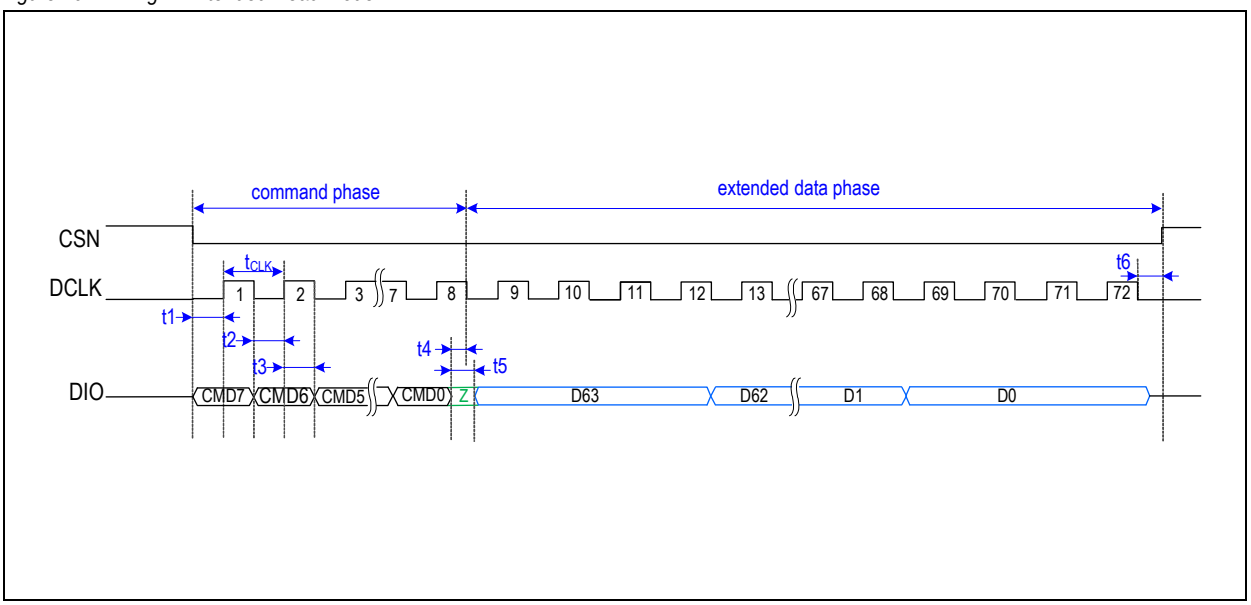


Figure 10. Timing in Extended Read Mode



In extended mode the digital interface requires four clocks per data bit. During this time the device is able to handle internal signals for special access.

Table 4. Read / Write Interface Commands in Extended Mode

Command Name	Command Data	Access Mode	MSB 63	...	17	16	15	14	13	12	11	10	9	8	...	LSB 0
WRITE OTP	0001_1111	ext. write	TST<46:0>			SENSITIVITY <1:0>		ext. CLK EN	PRE_COM_STAT <1:0>		UVW <2:0>			ZERO ANGLE <8:0>		
PROG OTP	0001_1001	ext. write	TST<46:0>			SENSITIVITY <1:0>		ext. CLK EN	PRE_COM_STAT <1:0>		UVW <2:0>			ZERO ANGLE <8:0>		
READ OTP	0000_1111	ext. write	TST<46:0>			SENSITIVITY <1:0>		ext. CLK EN	PRE_COM_STAT <1:0>		UVW <2:0>			ZERO ANGLE <8:0>		
READ ANA	0000_1001	ext. read	TST<46:0>			SENSITIVITY <1:0>		ext. CLK EN	PRE_COM_STAT <1:0>		UVW <2:0>			ZERO ANGLE <8:0>		

Note: TST is pre-programed by *ams* and used for test purpose.

Programming Parameters.

ZERO ANGLE <8:0>: Zero position value. This value is permanent added to the internal absolute position. Use range 0 to 359.

UVW <2:0>: Setup of the number of pole pairs. In the step mode configuration, the bit UVW<2> is used to invert the step mode output signal.

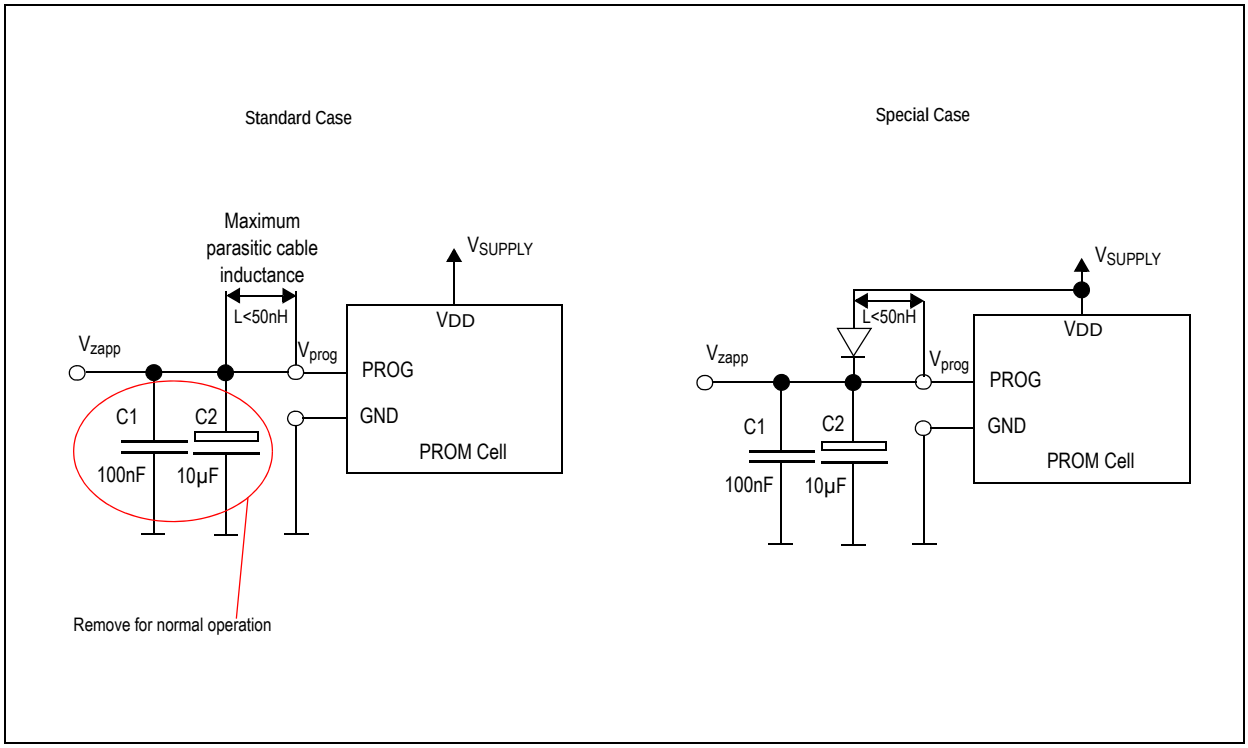
Configuration of the Number of Pole Pairs			
UVW <2:0>			Number of Pole Pairs
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	6
1	1	1	6

Setup of the Sensitivity				
SENSITIVITY <1:0>		Sensitivity Setting		
		Min	Typ	Max
0	0	1.6	1.65	1.75
0	1	1.79	1.88	1.98
1	0	2.01	2.11	2.22
1	1	2.23	2.35	2.47

Setup Parameters for the Static Pre-Commutation		
PRE_COM_STAT <1:0>		Static Pre-commutation Value in Mechanical Degrees
0	0	0
0	1	2
1	0	4
1	1	8

Ext. CLK EN: Enables the external CLK mode for the PWM output. The external CLK mode is only possible in commutation mode. The state of the pin COM/INC is not considered in this case for mode selection.

Figure 11. OTP Programming Connection



Note: The maximum capacitive load at PROG in normal operation should be less than 20pF. However, during programming the capacitors C1+C2 are needed to buffer the programming voltage during current spikes, but they must be removed for normal operation. To overcome this contradiction, the recommendation is to add a diode (4148 or similar) between PROG and VDD as shown in Figure 11 (special case setup), if the capacitors can not be removed at final assembly.

Due to D1, the capacitors C1+C2 are loaded with VDD-0.7V at startup, hence not influencing the readout of the internal OTP registers. During programming the OTP, the diode ensures that no current is flowing from PROG (8V to 8.5V) to VDD (5V).

In the standard case (see Figure 11), the verification of a correct OTP readout must be done by analog readback. The special case setup provides the analog readback of the OTP as well.

As long as the PROG pin is accessible it is recommended to use standard setup. In case the PROG pin is not accessible at final assembly, the special setup is recommended.

7.1.3 Programming Verification

After programming, the programmed OTP bits must be verified using the following methods:

Digital Read Out (Mandatory): After sending a READ OTP command, the readback information must be the same as programmed information. Otherwise, it indicates that the programming was not performed correctly.

Note: Either “Digital Verification” or “Analog Verification” must be carried out in addition to the “Digital Read Out”.

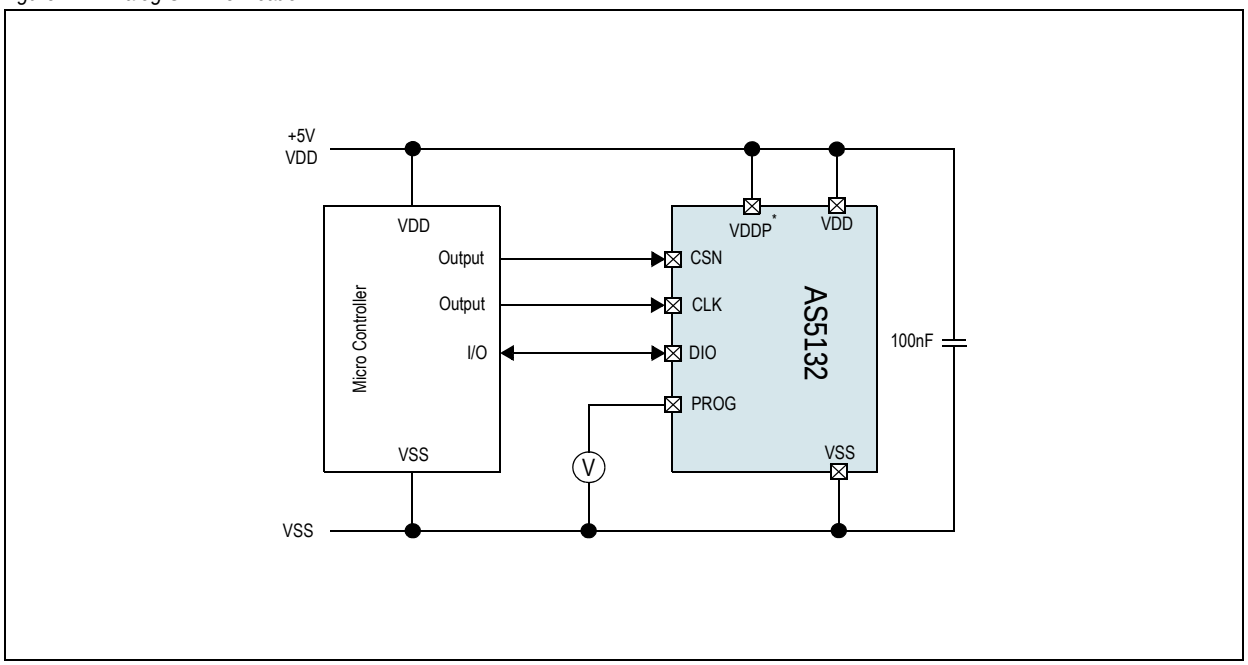
Digital Verification: Checking the EZ ERR bit (0 = OK, 1 = error)

i) At room temperature

ii) Right after the programming

Analog Verification: By switching into Extended Mode and sending a READ ANA command, the pin PROG becomes an output sending an analog voltage with each clock representing a sequence of the bits in the OTP register (starting with D61). A voltage of <500mV indicates a correctly programmed bit (“1”) while a voltage level between 2V and 3.5V indicates a correctly unprogrammed bit (“0”). Any voltage level in between indicates incorrect programming.

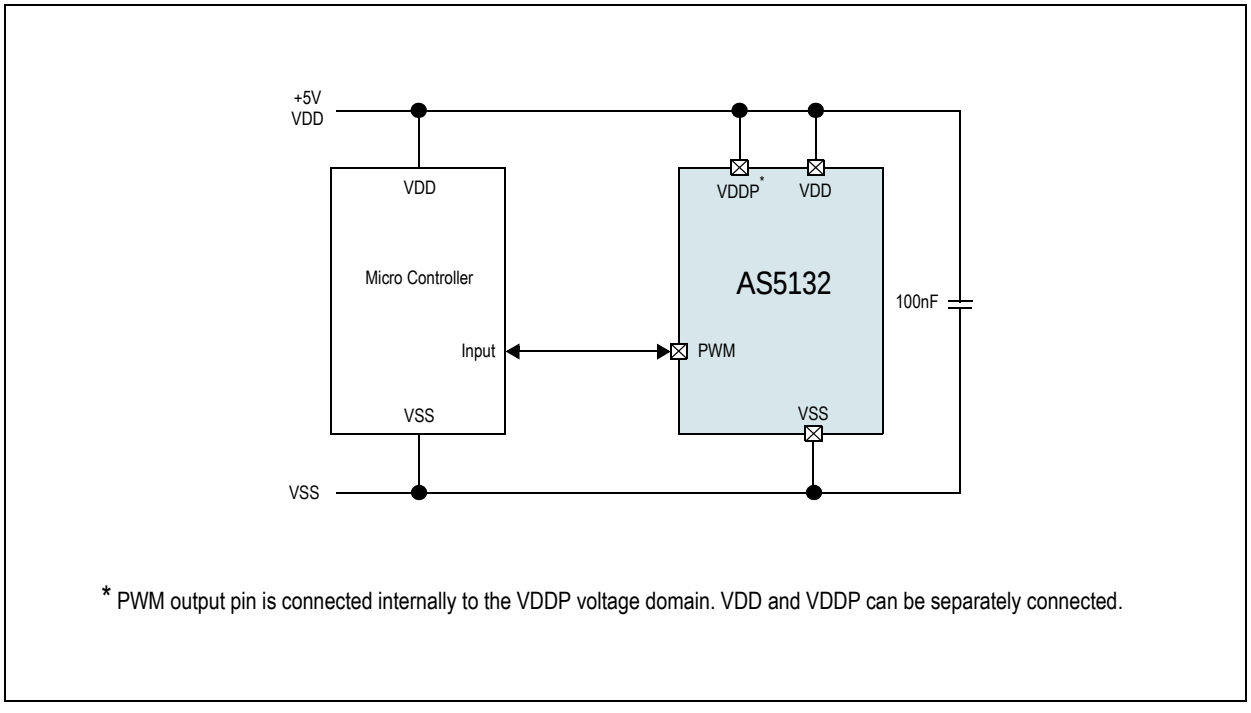
Figure 12. Analog OTP Verification



7.2 Pulse Width Modulation (PWM) Output

The AS5132 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the absolute angle position. Figure 15 shows the output format. In case of an internal error the high pulse contains 12 steps. An error can be easily identified by the external microcontroller. The zero degree angle position is build with 16 steps (12 + 4) high and 359 steps low followed by 8 exit steps.

Figure 13. PWM Output



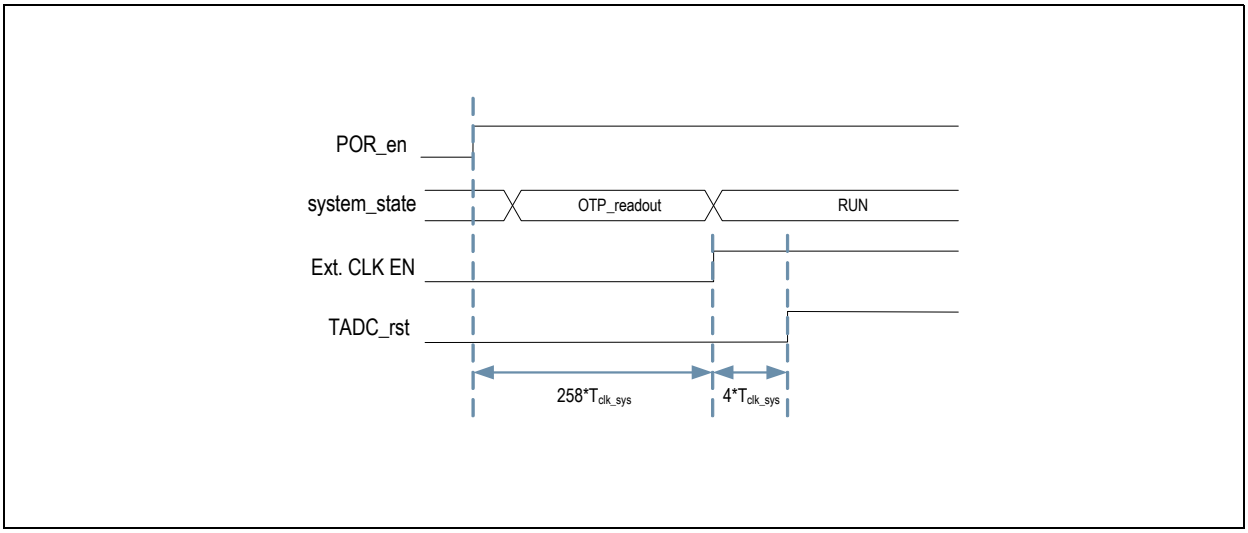
7.2.1 PWM External Clock

The PWM period depends on the setting of the OTP bit Ext. CLK EN. By default the internal clock source is used as a reference. An external clock can be connected to the pin COM/INC.

In case Ext. CLK EN is set, the output-mode which is determined by the states of {COM/INC, Test3, Test2, Test1, Test0} (see Table 6) during start-up is overwritten and U,V,W commutation mode signals are activated.

After internal power on reset (POR_en), the OTP is read out. When the Ext. CLK EN is programmed successfully, the COM/INC pin is used as external clock for the PWM block. After 4 clock cycles of Ext. CLK EN, the reset of TADC (TADC_rst) and the PWM block is released.

Figure 14. Start-up Procedure



The reset for the PWM block is synchronized to the external PWM clock. This ensures a save reset also in case the external clock on COM/INC is already running during start-up.

Figure 15. PWM Output Signal

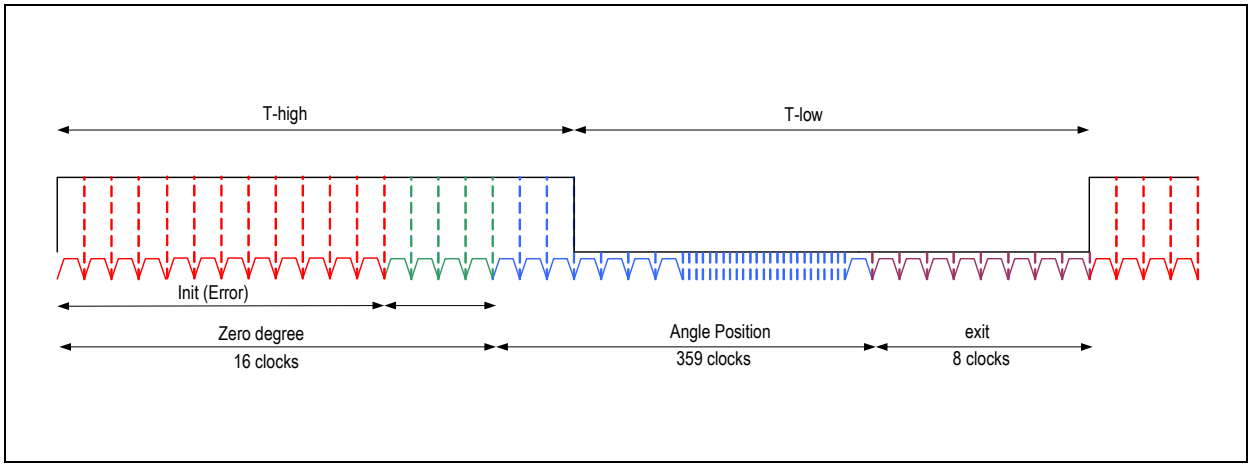


Table 5. PWM Timing with Internal and External CLK Source

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{PWMint}	PWM Period internal	600	750	900	µs	Internal clock source
T_{PWMext}	PWM Period external	383 / CLK_{PWM}			µs	External clock provided over COM / INC pin
CLK_{PWM}	Clock external mode	0		766	kHz	

7.3 Incremental Outputs

Two different incremental output modes are possible. Quadrature A/B mode and selectable Step Mode can be selected by the pins TEST0, TEST1, TEST2, TEST3 and COM / INC.

Table 6. Configuration of the Incremental Output Modes

COM / INC	TEST3	TEST2	TEST1	TEST0	Output Mode	Pin Assignment
1	0	0	0	0	Quadrature A/B/I Mode 90 pulses per channel	A → U_A B → V_B I → W_I '0' → S
1	0	0	0	1	Stepmode 24 pulses and Index width 2	'0' → U_A '0' → V_B '0' → W_I S_24_2 → S
1	0	0	1	0	Stepmode 60 pulses and Index width 2	'0' → U_A '0' → V_B '0' → W_I S_60_2 → S
1	0	0	1	1	Stepmode 90 pulses and Index width 2	'0' → U_A '0' → V_B '0' → W_I S_90_2 → S
1	0	1	0	0	Stepmode 180 pulses and Index width 2	'0' → U_A '0' → V_B '0' → W_I S_180_2 → S
0	0	0	0	0	U,V,W Commutation Mode (OTP setting)	U → U_A V → V_B W → W_I '0' → S

Note: The pin setting COM / INC has priority. In case of a low state the device is exclusively in the commutation mode. Not specified states of TEST3, TEST2, TEST1 and TEST0 in incremental mode will enable the quadrature A/B/I mode. This configuration is only read once at startup. It is not recommended to change the state during operation.

7.3.1 Quadrature A/B Output

Figure 16. Incremental Output of the AS5132

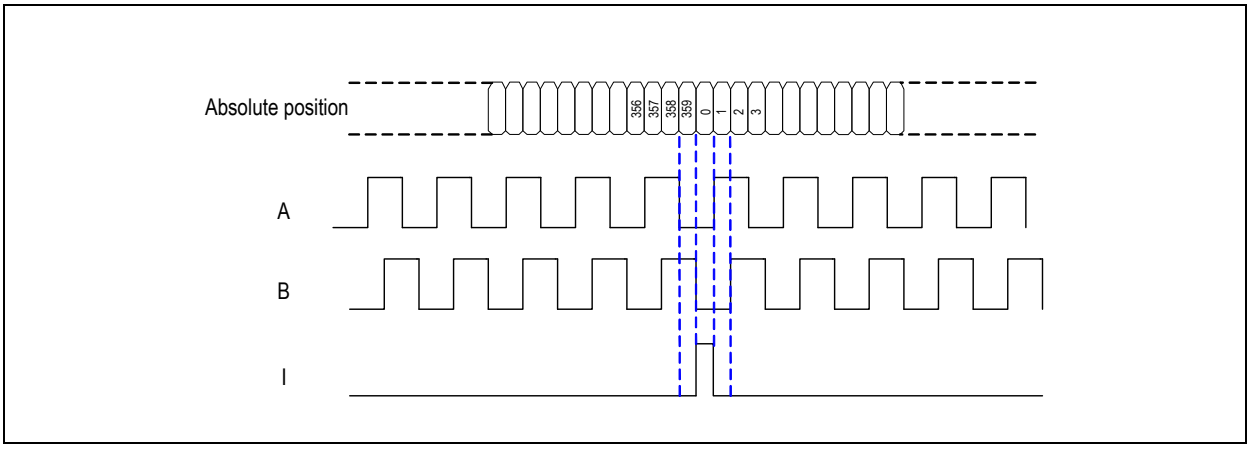
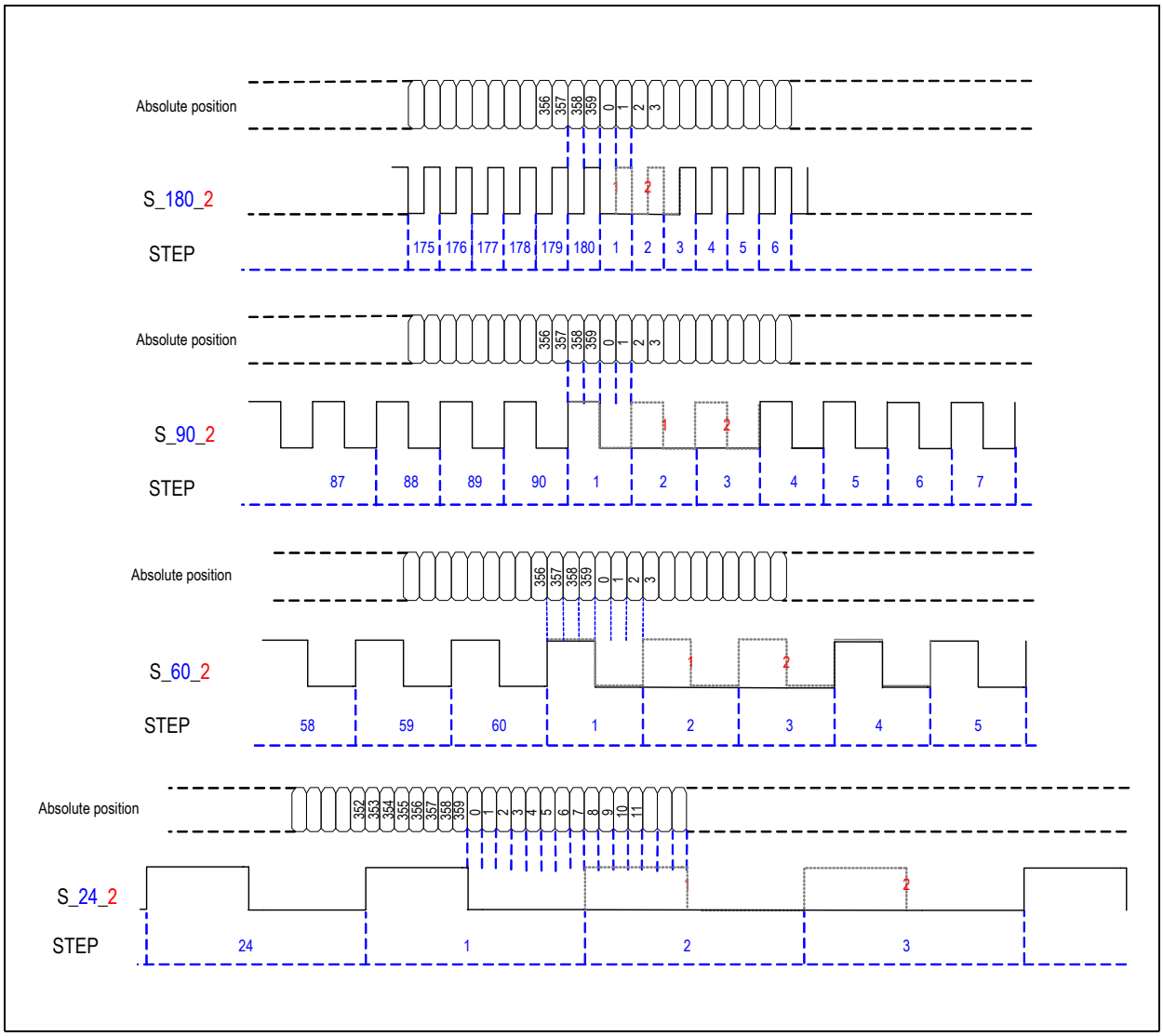


Figure 16 shows the two-channel quadrature output. The index position is mapped to the absolute mechanical zero position. The phase shift between channel A and B indicates the direction of the magnet movement. Channel A leads channel B at a clockwise rotation of the magnet (top view) by 90 electrical degrees. Channel B leads channel A at a counter-clockwise rotation.

7.3.2 Step Output Mode

Step Output mode provides a specific combination of the A incremental signal and the index signal I. The number of pulse can be configured with the input pattern of the test input pins.

Figure 17. Step Mode of the AS5132 with Different Number of Pulses



7.3.3 Pre-Commutation Function

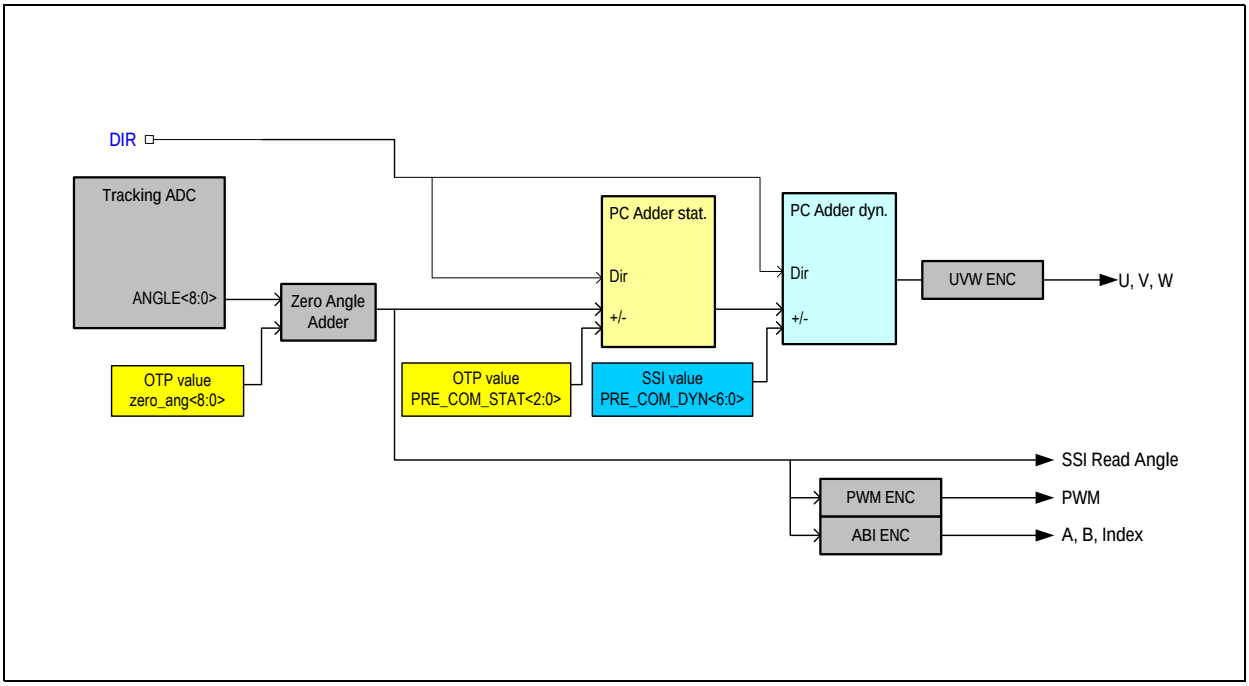
This feature can be used to optimize the torque characteristic at a certain speed of the BLDC motor. The output signals U, V and W can be shifted by a specific number of degrees back and forward. The AS5132 distinguish between the static and dynamic pre commutation value. The static value is similar to an additional zero programming and can be programmed only once. The dynamic value is stored in the interface register and can be changed during operation.

The pin DIR defines if the value of pre-commutation is added or subtracted. The dynamic commutation register will be set to zero after a rotation change indicated by the external pin DIR. Due to internal synchronization, the outputs U,V,W will change 3 internal clock cycles after the change of DIR input signal.

Table 7. Definition of the Pre-Commutation Direction

DIR	Rotation	Consequence
0	Clock wise	PRE_COM values added to absolute angle
1	Counter clock wise	PRE_COM values subtracted from absolute angle

Figure 18. Block Diagram of the Pre-Commutation Function



Note: The dynamic pre-commutation is set to zero always if the direction is changed over the pin DIR. A new value PRE_COM_DYN must be written again. The static pre-commutation is always enabled and will shift the output.

7.3.4 Commutation Output UVW

The pre-commutation function is used only at the U,V,W output. Figure 19 shows the transition on the outputs U,V,W in case of a two pole pair configuration. The static pre-commutation value was set to 12 degrees.

Figure 19. UVW Output Transitions with Pre-Commutation

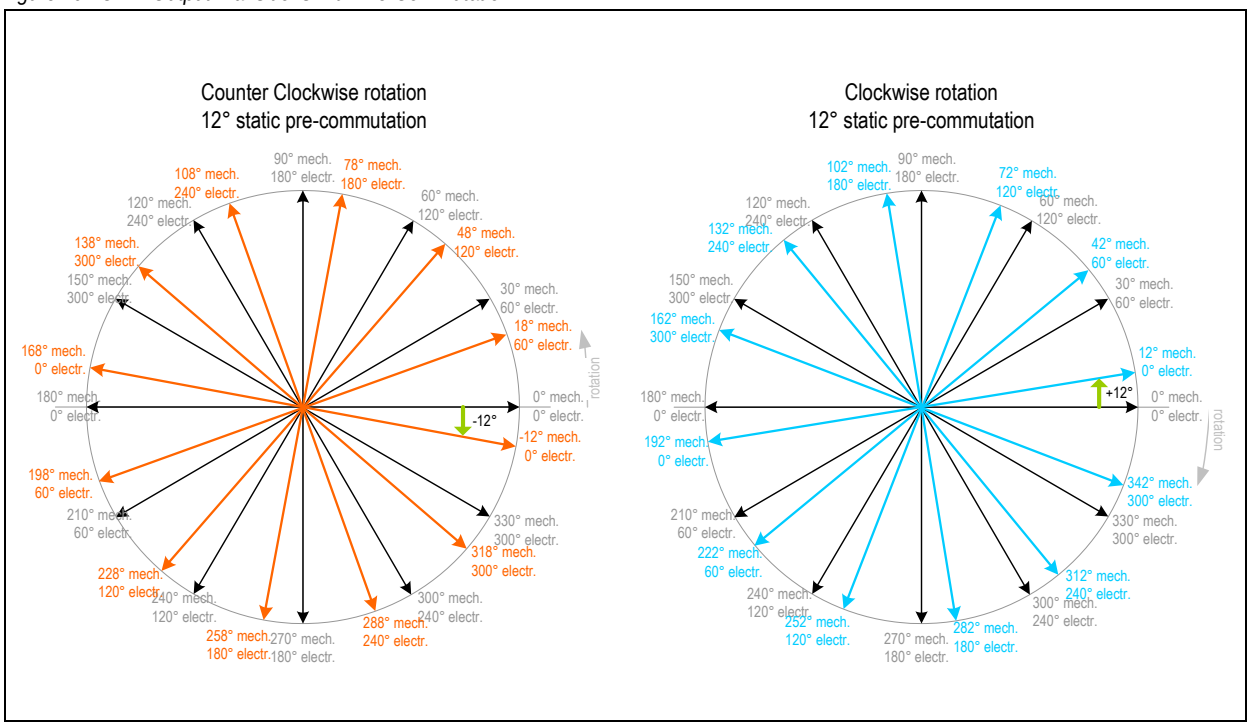
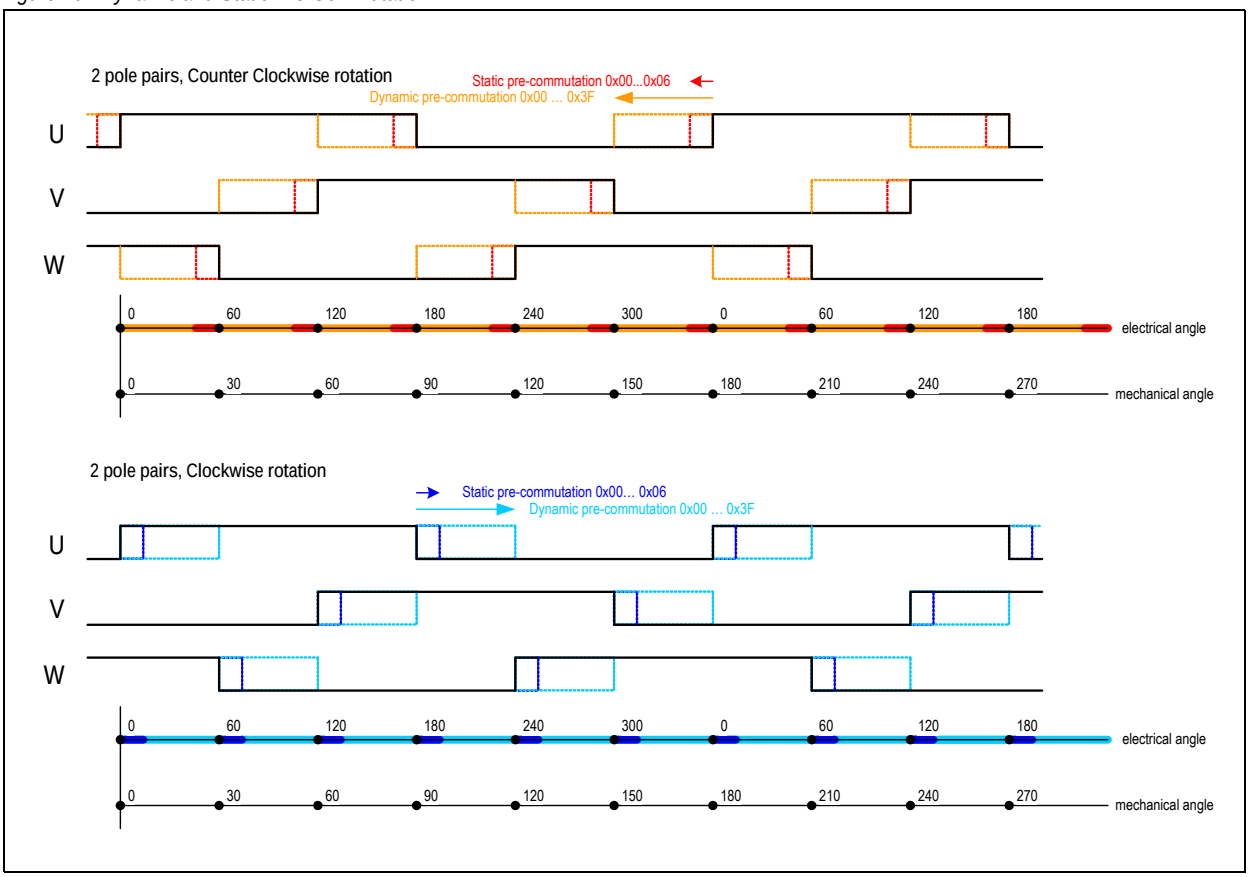


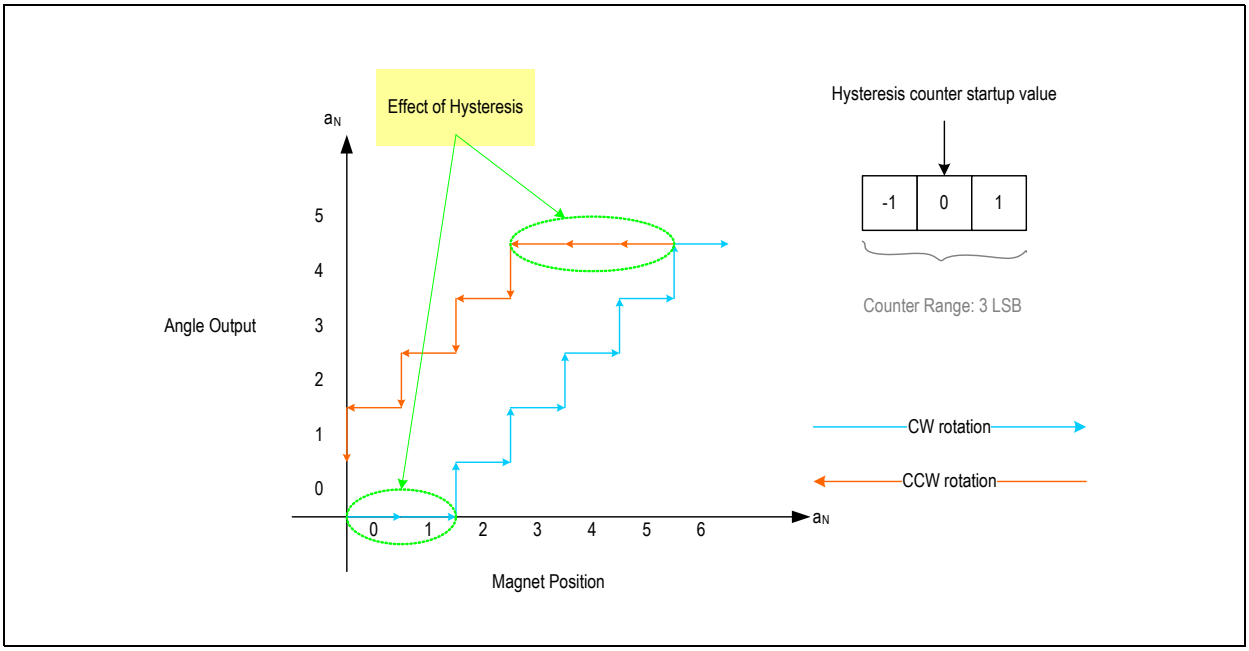
Figure 20. Dynamic and Static Pre-Commutation



7.3.5 Hysteresis of the Incremental Outputs

A hysteresis is implemented to get a stable output value at the SSI command and to reduce jitter at the PWM and UVW outputs. At start up the hysteresis counter is at 0, the range is ±1 LSB. The hysteresis can be deactivated by setting OTP bit Hyst_dis.

Figure 21. Hysteresis of the Outputs



7.3.6 Multi Turn Counter

A 9-bit register is used for counting the magnet's revolutions. With each zero transition in any direction, the output of a special counter is incremented or decremented. The initial value after reset is 0 LSB. Clockwise rotation gives increasing angle values and positive turn count. Counter clockwise rotation exhibits decreasing angle values and a negative turn count respectively.

The counter output can be reset by using command 20 – SET MT Counter. It is immediately reset by the rising clock edge of this bit. Any zero crossing between the clock edge and the next counter readout changes the counter value.

7.3.7 High Speed Operation

The AS5132 is using a fast tracking ADC (TADC) to determine the angle of the magnet. The TADC is tracking the angle of the magnet with cycle time of 2µs (typ. 1.4). Once the TADC is synchronized with the angle, it sets the LOCK bit in the status register. Once it is locked, it requires only one cycle [2µs (typ. 1.4)] to track the moving magnet. The AS5132 can operate in locked mode at rotational speeds up to max.72,900 rpm.

7.3.8 Propagation Delay

The propagation delay is the time required from reading the magnetic field by the Hall sensors to calculating the angle and making it available on the serial or PWM interface. While the propagation delay is usually negligible on low speeds, it is an important parameter at high speeds. The longer the propagation delay, the larger becomes the angle error for a rotating magnet as the magnet is moving while the angle is calculated. The position error increases linearly with speed.

7.3.9 Error Detection

The following errors are detected by the system:

- Lock bit → the TADC has not yet found a valid angular position
- AGC alarm → the AGC value is 63, magnetic field is too weak

By default, Lock bit error should activate the error condition at the outputs. The AGC alarm is permanently available at the DIAG pin.

Error condition at commutation and incremental outputs:

- U, V and W outputs all '0'
- A, B and I outputs all '1'

8 Application Information

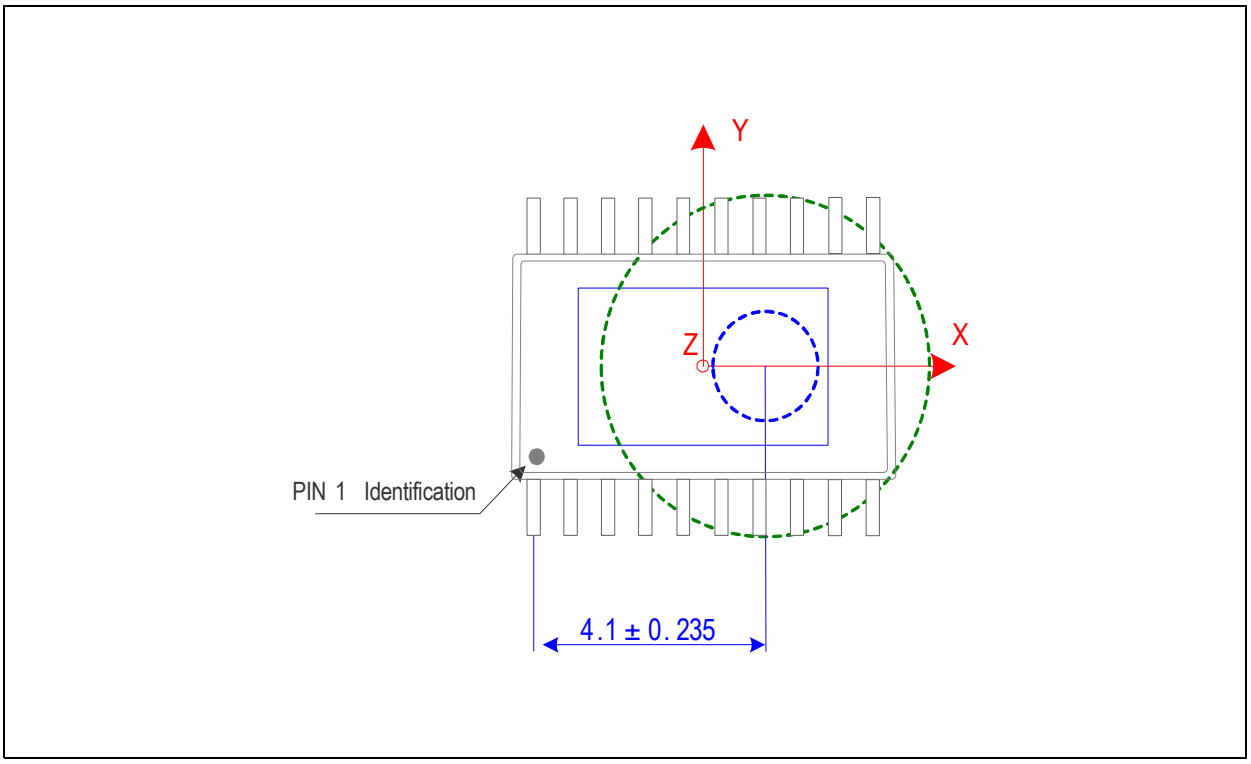
The benefits of AS5132 are as follows:

- Complete system-on-chip, no angle calibration required
- Flexible system solution provides absolute serial, PWM and incremental output formats
- Ideal for applications in harsh environments due to magnetic sensing principle
- High reliability due to non-contact sensing
- Robust system, tolerant to horizontal misalignment, airgap variations, temperature variations and external magnetic fields
- External clock mode for PWM output

8.1 Physical Placement of the Magnet

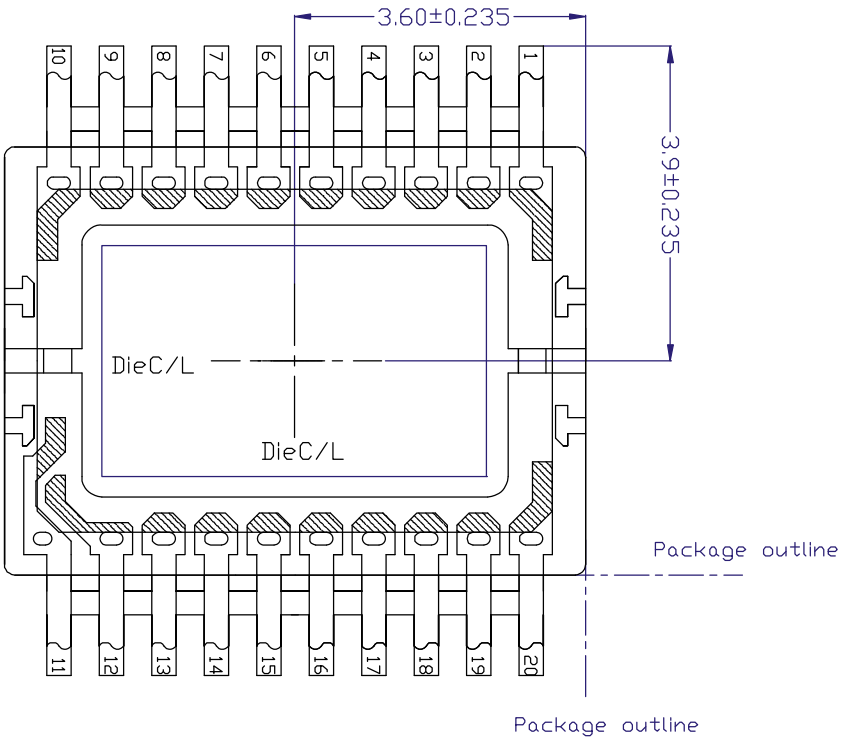
The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the IC package as shown in Figure 22.

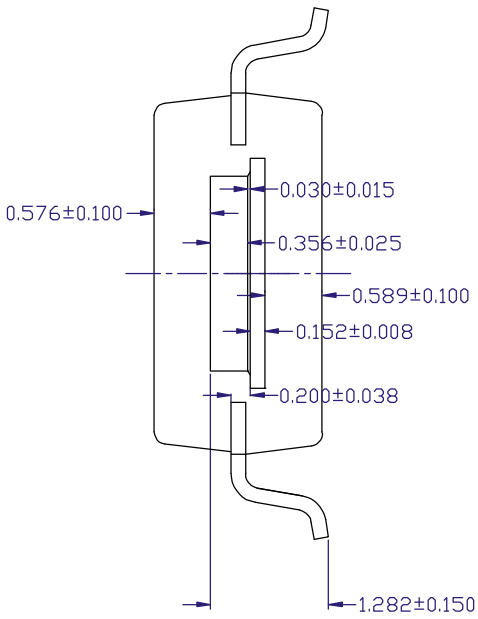
Figure 22. Defined IC Center and Magnet Displacement Radius



The centre of the Hall sensor array is shifted by a constant value in x axis indicated by the blue circle. In the application it is important to refer to this point.

Figure 23. Vertical Cross Section of SSOP-20





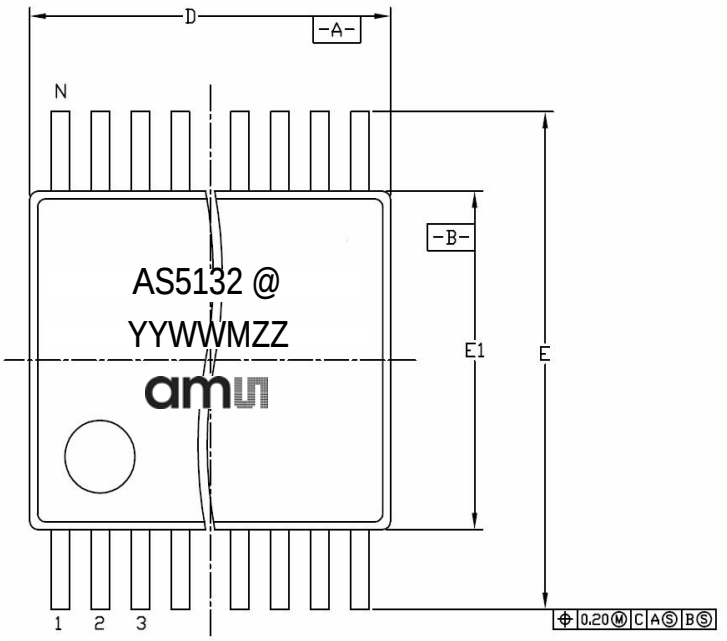
Notes:

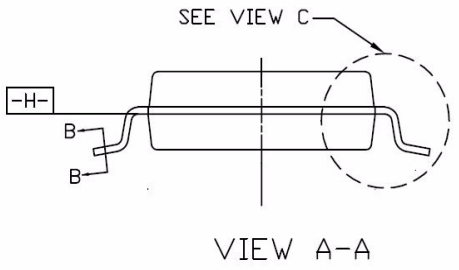
1. All dimensions in mm.
2. Die is slightly off centered.

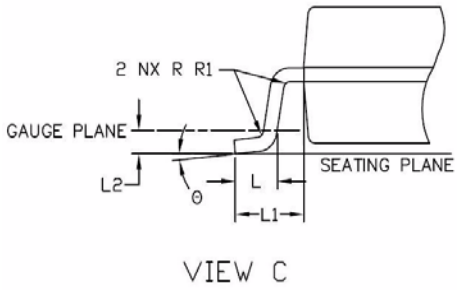
9 Package Drawings and Markings

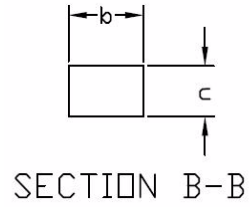
The device is available in a 20-Lead Shrink Small Outline package.

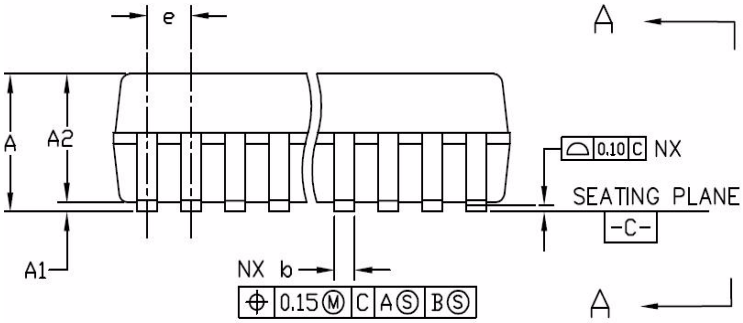
Figure 24. Package Drawings and Dimensions











Symbol	Min	Nom	Max
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
b	0.22	0.30	0.38
c	0.09	0.17	0.25
D	6.90	7.20	7.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	-	0.65 BSC	-
L	0.55	0.75	0.95
L1	-	1.25 REF	-
L2	-	0.25 BSC	-
R	0.09	-	-
Θ	0°	4°	8°
N	20		

Notes:

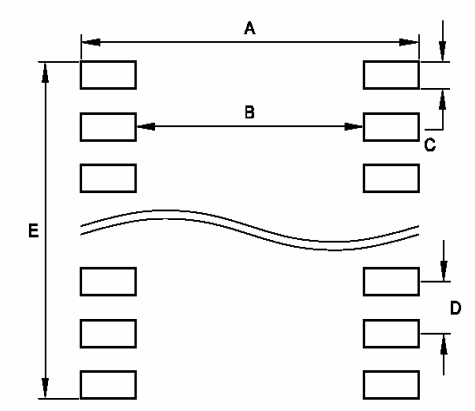
1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.

Marking: @YYWWMZZ.

@	YY	WW	M	ZZ
Sublot identifier	Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Assembly traceability code

9.1 Recommended PCB Footprint

Figure 25. PCB Footprint



Recommended Footprint Data		
Symbol	mm	inch
A	9.02	0.355
B	6.16	0.242
C	0.46	0.018
D	0.65	0.025
E	6.31	0.248

Revision History

Revision	Date	Owner	Description
0.11			Initial draft
0.18	16 Dec, 2010	mub	Updates across datasheet according to 0.18 specification document.
0.19	17 Dec, 2010		Updated System Parameters, Ext. CLK EN under Programming Parameters, Pre-Commutation Function.
0.20	22 Mar, 2011		Added OTP Programming Connection, Programming Verification, Analog OTP Verification. Updated Package Drawings and Markings and Ordering Information.
0.21	06 Apr, 2011		Updated Programming Verification.
0.22	07 Apr, 2011		Added PWM External Clock, updated Ordering Information.
0.23	27 Jul, 2011		Updated Absolute Maximum Ratings.
	04 Aug, 2011		Updated Key Features, DC Characteristics of Digital Inputs, Package Drawings and Markings.
0.24	25 Nov, 2011		Updated Vertical Cross Section of SSOP-20 (page 22) and Marking info. Added Figure 9, Figure 10.
1.0	30 Mar, 2012	ekno	Datasheet release
1.1	06 Sep, 2012		Text corrections; updated Table 4
1.2	26 Mar, 2013	mub	VDDP pin added in Figure 4 and Figure 13, IDD max corrected in Section 6.1, addded Load condition VOL/VOH in Section 6.6 and sentences corrected from 8 steps to 16 steps in Section 7.2.
1.3	12 Apr, 2013		Package Marking change, added note in Section 6.6 for VOL and VDDP pin added in Figure 8 and Figure 12.
1.4	28 Jun, 2013		Clarification of the Revision History (page 25) in versions 1.2 & 1.3.

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 8.

Table 8. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS5132-HSST	360 Step Programmable High Speed Magnetic Rotary Encoder	Tape & Reel	20-pin SSOP
AS5132-HSSM	360 Step Programmable High Speed Magnetic Rotary Encoder	Tape & Reel	20-pin SSOP

Note: All products are RoHS compliant and ams green.
Buy our products or get free samples online at www.ams.com/ICdirect

Technical Support is available at www.ams.com/Technical-Support

For further information and requests, email us at sales@ams.com
(or) find your local distributor at www.ams.com/distributor

Copyrights

Disclaimer

Devices sold by ams AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. ams AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. ams AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by ams AG is believed to be correct and accurate. However, ams AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams AG rendering of technical or other services.

Contact Information

Headquarters

ams AG
Tobelbaderstrasse 30
A-8141 Unterpremstaetten, Austria

Tel : +43 (0) 3136 500 0
Fax : +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:
http://www.ams.com/contact

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for ams ***manufacturer:***

Other Similar products are found below :

AS5045B-ASST PS081-EVA-HR MODULE AS1119-DB AS1331 EB AS1359-25-EB AS1363-30-EB AS3415 EK-ST AS3606-DB AS3630-ZWLM AS5055A-DK-ST AS5115 PB AS5XXX-UCB-1.0 AS6200-WL_DK_ST PC404A-202R AS1119-WL_DK_ST AS3932 DEMOBOARD TMG3993EVM TSL2591EVM TSL2672EVM TMD2725-DB TMD2771EVM TMD3782EVM TRK-1T02-E TSL2772EVM USB-BOX AS3400 EK-ST AS3661-EB AS3668-EB AS5145B-SS_EK_MB AS5245-QF_EK_PB AS526X-MF_EK_SB AS5510-WL_EK_DB AS5X6X-EK-ST AS5XXX-EK-PB AS5XXX-EK-USB-PB AS1119-WK_DK_ST AS1121-QF_EK_ST AS1312-TD-50_EK_ST AS1340A-TD-10_EK_ST AS3606 EVAL BOARD AS3701B-WL-ES_EK_ST AS3980-QF_DK_ST AS5030-TS_EK_AB AS5045-SS_EK_DB AS5132-SS_EK_DB AS8506-DK-ACTIVE AS8510 DEMOBOARD ENS210-QF_EK_ST TSL261R-LF DK-M3-LS-1.8-6