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AS5134

360 Step Programmable High Speed Magnetic Rotary Encoder

1 General Description

The AS5134 is a contactless magnetic rotary encoder for accurate angular measurement over a full turn of 360°. It is a system-on-chip, combining integrated Hall elements, analog front-end and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip is required. The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 8.5 bit = 360 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal. In addition to the angle information, the strength of the magnetic field is also available as a 6-bit code.

Data transmission can be configured for 1-wire (PWM), 2-wires (DCLK, DIO) or 3-wires (DCLK, DIO, CS).

A software programmable (OTP) zero position simplifies assembly as the zero position of the magnet does not need to be mechanically aligned.

A Power Down Mode together with fast startup and measurement cycles allows a very low average power consumption.

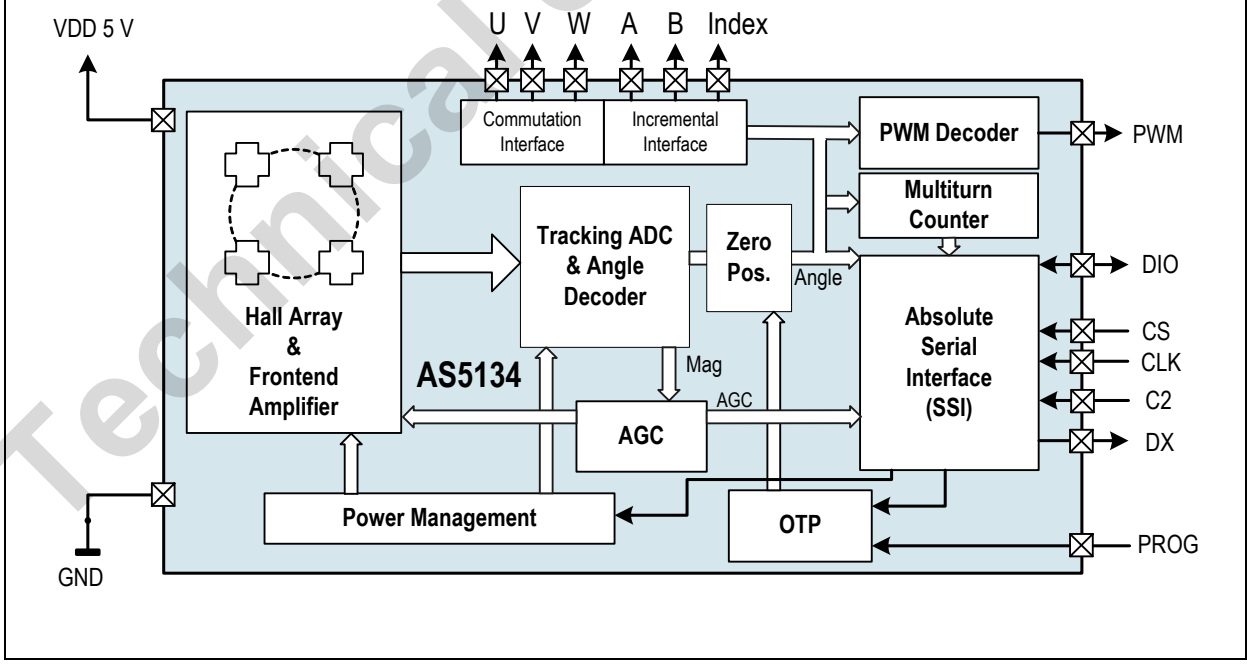
2 Key Features

- 360° contactless angular position encoding
- Two digital 360 step (8.5 bit) absolute outputs: Serial interface and Pulse width modulated (PWM) output
- User programmable zero position and sensitivity
- High speed: up to 76875 rpm
- Direct measurement of magnetic field strength allows exact determination of vertical magnet distance
- Incremental Outputs ABI Quadrature: 90 ppr, step direction: 180ppr, fixed pulse width 360ppr
- BLDC Outputs UVW, selectable for 1,2,3,4,5,6 pole pairs
- Daisy-Chain mode for cascading of multiple sensors
- 9-bit multi turn counter
- Low power mode with fast startup
- Wide magnetic field input range: 20- 80 mT
- Wide temperature range: -40°C to +140°C
- Fully automotive qualified to AEC-Q100
- Small Pb-free package: SSOP 20

3 Applications

The AS5134 is suitable for contactless rotary position sensing, rotary switches (human machine interface), AC/DC motor position control and Brushless DC motor position control.

Figure 1. AS5134 Magnetic Rotary Encoder Block Diagram



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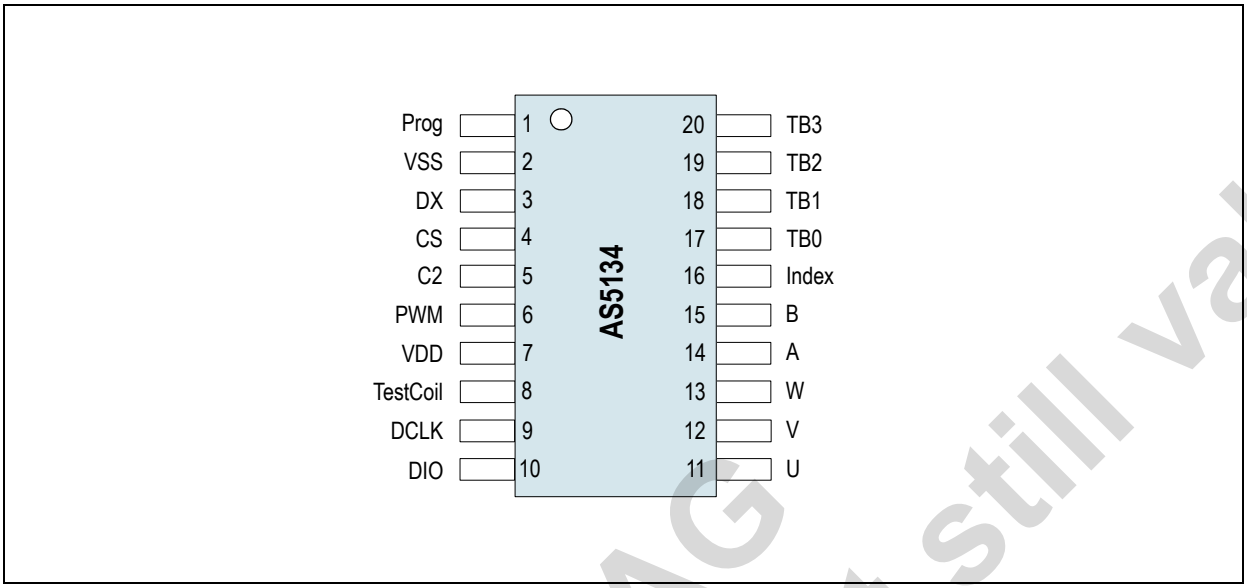
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
Prog	1	Programming voltage input, must be left open in normal operation. Maximum load = 20pF (except during programming)
VSS	2	Supply ground
DX	3	Chip select output for 2-wire mode and Daisy Chain cascading
CS	4	Chip select input for 3-wire mode
C2	5	Select between 2-wire (C2 → VDD) and 3-wire (C2 → VSS) mode
PWM	6	PWM output
VDD	7	Positive supply voltage (double bond to VDD_A and VDD_D)
Test Coil	8	Test pin
DDCLK	9	Clock input for serial interface
DIO	10	Data I/O for serial interface
U	11	Commutation output
V	12	Commutation output
W	13	Commutation output
A	14	Incremental output
B	15	Incremental output
Index	16	Incremental output
TB0	17	Test pin
TB1	18	Test pin
TB2	19	Test pin
TB3	20	Test pin

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
Supply voltage (V_{DD})	-0.3	7	V	Except during OTP programming
Input Pin Voltage (V_{IN})	VSS-0.5	VDD	V	
Input Current (latch up immunity), (I_{scr})	-100	100	mA	Norm: EIA/JESD78 ClassII Level A
Electrostatic Discharge				
ESD		±2	kV	Norm: JESD22-A114E
Temperature Ranges and Storage Conditions				
Storage Temperature (T_{strg})	-55	150	°C	
Body temperature, (T_{body})		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*. The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level (MSL)	3			Represents a maximum floor time of 168h

6 Electrical Characteristics

TAMB = -40 to 140ºC, VDD5V = 4.5-5.5V, all voltages referenced to VSS, unless otherwise noted.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Positive Supply Voltage		4.5		+5.5	V
IDD	Operating Current	No load on outputs. Supply current can be reduced by using stronger magnets.			22	mA
I_{off}	Power down current	Low Power Mode		70	120	µA
System Parameters						
N	Resolution			8.5		Bit
				1		Deg
T_{PwrUp}	Power Up Time	Startup from zero			≤4100	µs
		Startup from Low Power mode			≤500	
t_s	Tracking rate	Step rate of tracking ADC; 1 step = 1º			5.2	µs/step
INL_{cm}	Accuracy	Centered Magnet	-2		2	Deg
INL_{dm}		Within horizontal displacement radius	-3		3	Deg
t_{delay}	Propagation delay	Internal signal processing time			22	µs
TN	Transition noise	Peak-Peak			1.41	Deg
Magnet Specifications						
B_i	Magnetic Input Range	Required vertical component of the magnetic field strength on the chip surface, measured along a concentric circle with a radius of 1 mm	20		80	mT
V_i	Magnet rotation speed	to maintain locked state			76875	rpm
PWM Output						
t_{PWM}	PWM period		600	750	900	µs
f_{PWM}	PWM frequency	1 / PWM period	1.11	1.33	1.66	kHz
Programming Parameters						
V_{PROG}	Programming Voltage	Static voltage at pin Prog	8.0		8.5	V
$Tamb_{PROG}$	Programming ambient temperature	During programming	0		85	ºC
t_{PROG}	Programming time	Timing is internally generated	2		4	µs
$V_{R,prog}$	Analog readback voltage	During analog readback mode at pin Prog			0.5	V
$V_{R,unprog}$			2		3.5	
Hall Element Sensitivity Options						
sens	Hall Element sensitivity setting	sens = 00 (default)	1.60	1.65	1.75	X
		sens = 01	1.79	1.88	1.98	
		sens = 10	2.01	2.11	2.22	
		sens = 11	2.23	2.35	2.47	
DC Characteristics of Digital Inputs and Outputs						
CMOS Inputs: DDCLK, CS, DIO, C2						
VIH	High level input voltage		0.7*VDD		VDD	V
VIL	Low level input voltage		0		0.3*VDD	V
ILEAK	Input leakage current				1	µA

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS Outputs: DIO, PWM, DX						
V_{OH}	High level output voltage	Source current < 4mA	V_{DD}-0.5		V_{DD}	V
V_{OL}	Low level output voltage	Sink current < 4mA	0		V_{SS}+0.4	V
CL	Capacitive load				35	pF
CMOS Tristate Output: DIO						
IO_Z	Tristate leakage current	CS = low			1	µA

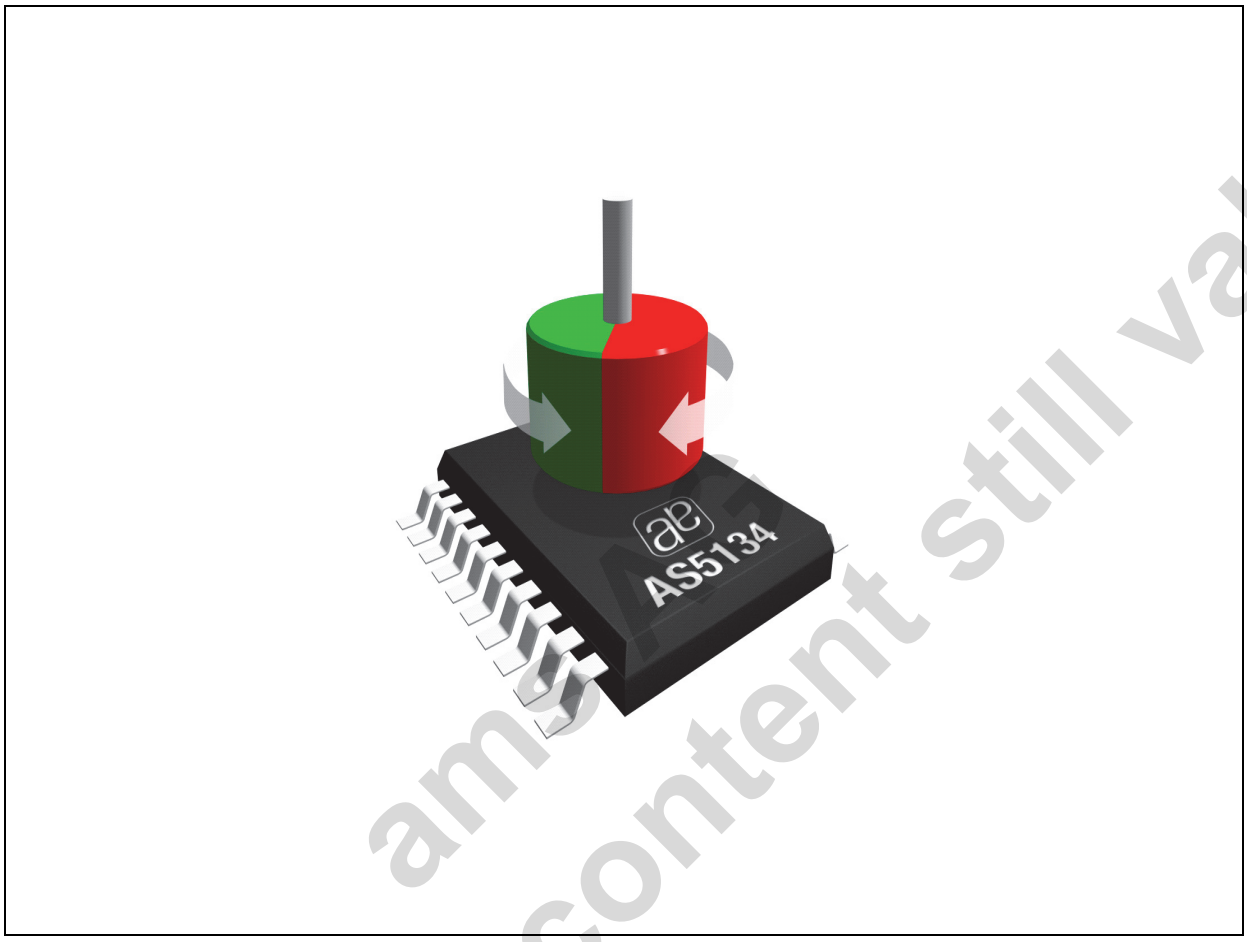
6.1 Timing Characteristics

Table 4. Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
2-/3-Wire Data Transmission						
3-Wire Interface						
f_{DCLK}	Clock Frequency	Normal operation		5	6	MHz
$f_{DCLK,P}$	Clock Frequency	During OTP programming	200		650	kHz
2-Wire Interface						
f_{DCLK}	Clock Frequency	Normal operation	0.1	5	6	MHz
$f_{DCLK,P}$	Clock Frequency	During OTP programming	200		500	kHz
General Data Transmission						
t0	Rising DCLK to CS		15		-	ns
t1	Chip select to positive edge of DCLK		15		-	ns
t2	Chip select to drive bus externally		-		-	ns
t3	Setup time command bit, Data valid to positive edge of DCLK		30		-	ns
t4	Hold time command bit, Data valid after positive edge of DCLK		30			ns
t5	Float time, Positive edge of DCLK for last command bit to bus float		30		DCLK/2	ns
t6	Bus driving time, Positive edge of DCLK for last command bit to bus drive		DCLK/2 +0		DCLK/2 +30	ns
t7	Setup time data bit, Data valid to positive edge of DCLK		DCLK/2 +0		DCLK/2 +30	ns
t8	Hold time data bit, Data valid after positive edge of DCLK		DCLK/2 +0		DCLK/2 +30	ns
t9	Hold time chip select, Positive edge DCLK to negative edge of chip select		30			ns
t10	Bus floating time, Negative edge of chip select to float bus		0		30	ns
t_{TO}	Timeout period in 2-wire mode (from rising edge of DCLK)		17		27	µs
t_{CLK}	Clock Timing			200		ns

7 Detailed Description

Figure 3. Typical Arrangement of AS5134 and Magnet



7.1 Connecting the AS5134

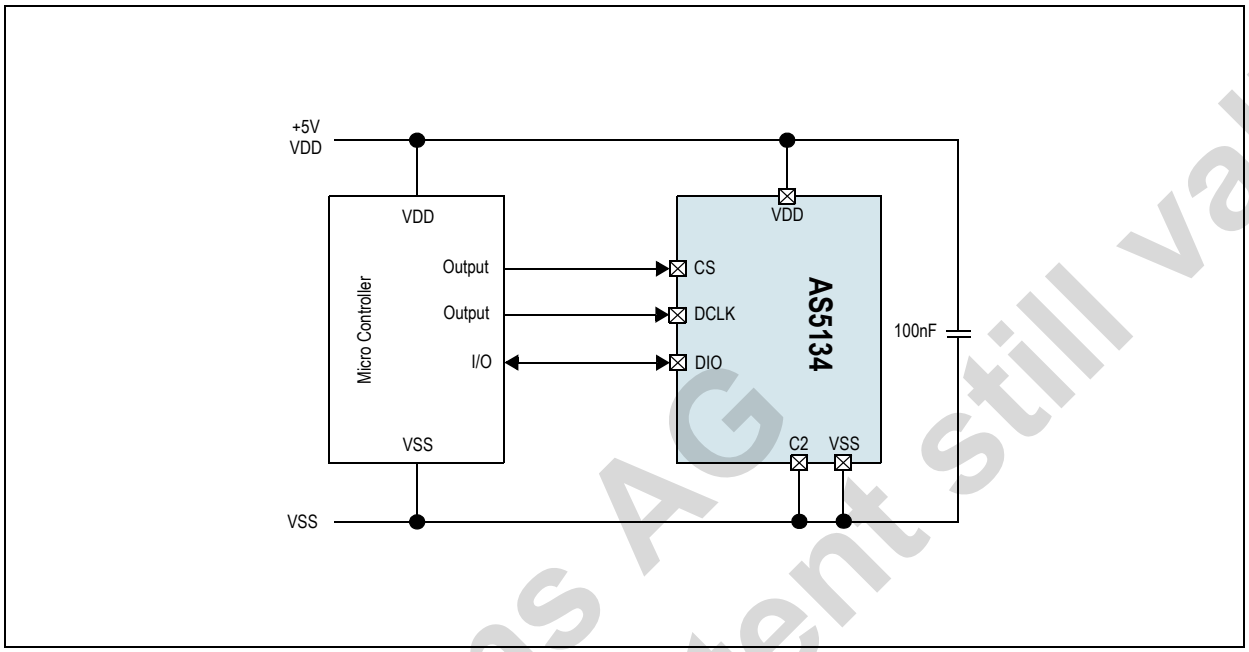
The AS5134 can be connected to an external controller in several ways as listed below:

- Serial 3-wire R/W connection
- Serial 3-wire Read-only connection
- Serial 2-Wire connection (R/W Mode)
- Serial 2-Wire Differential SSI connection
- 1-Wire PWM connection
- Analog output
- Quadrature A/B/Index output
- Brushless DC Motor Commutation Mode
- Daisy Chain Mode

7.2 Serial 3-Wire R/W Connection

In this mode, the AS5134 is connected to the external controller via three signals: Chip Select (CS), Clock (DCLK) inputs and bi-directional DIO (Data In/Out) output. The controller sends commands over the DIO pin at the beginning of each data transmission sequence, such as reading the angle or putting the AS5134 in and out of the reduced power modes.

Figure 4. SSI Read/Write Serial Data Transmission



A pull-down resistor (as shown in Figure 5) is not required. C2 is a hardware configuration input. C2 selects 3-wire mode (C2 = low) or 2-wire mode (C2 = high).

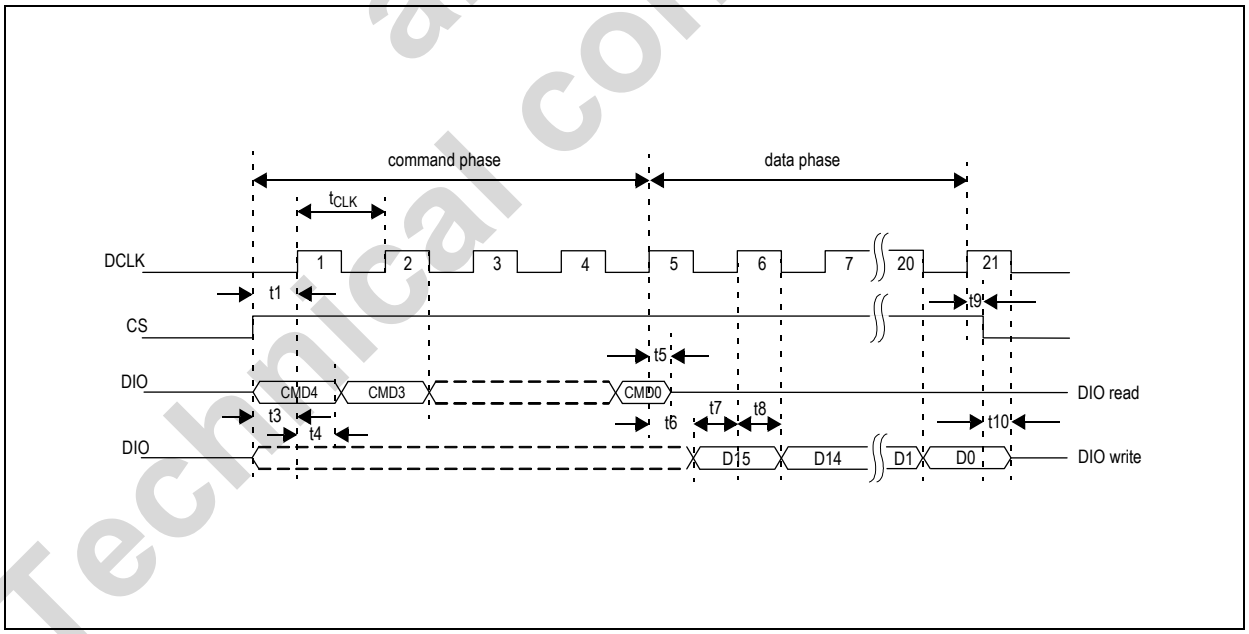


Table 5. Serial Bit Sequence (16bit read/write)

Write Command					Read/Write Data														
C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

7.3 Serial 3-Wire Read-only Connection

This connection is possible when the AS5134 is only used to provide the angular data (no power down or OTP access). The Chip Select (CS) and Clock (DCLK) connection is the same as in the R/W mode, but only a digital input pin (not an I/O pin) is required for the DIO connection. As the first 5 bits of the data transmission are command bits sent to the AS5134, both the microcontroller and the AS5134 are configured as digital inputs during this phase. Therefore, a pull-down resistor must be added to make sure that the AS5134 reads “00000” as the first 5 bits, which sets the Read_Angle command.

Note: All further application examples are shown in R/W mode, however read-only mode is also possible unless otherwise noted.

Figure 5. SSI Read-only Serial Data Transmission

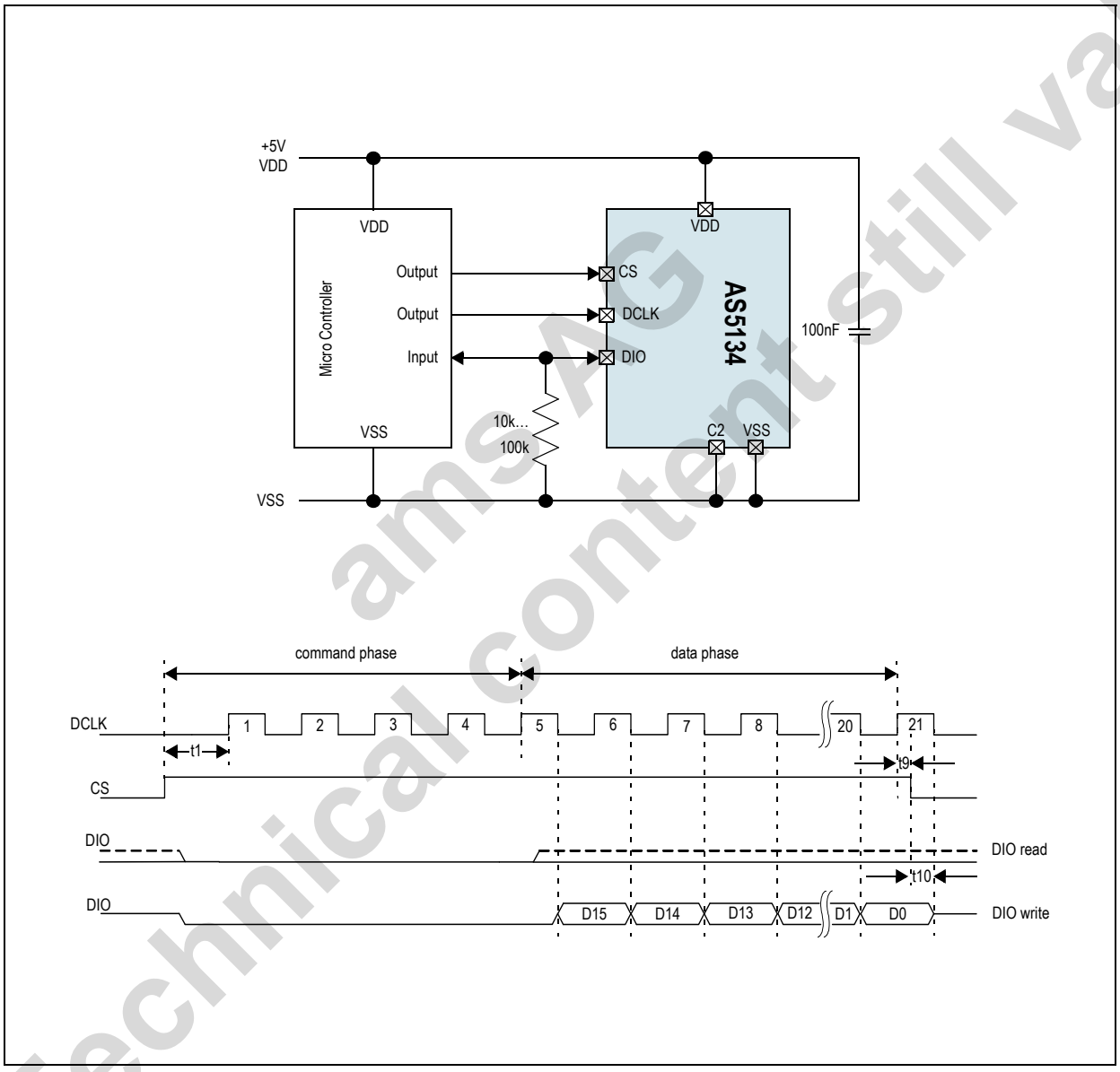


Table 6. 2-or 3-wire Read-only Serial Bit Sequence (21bit read)

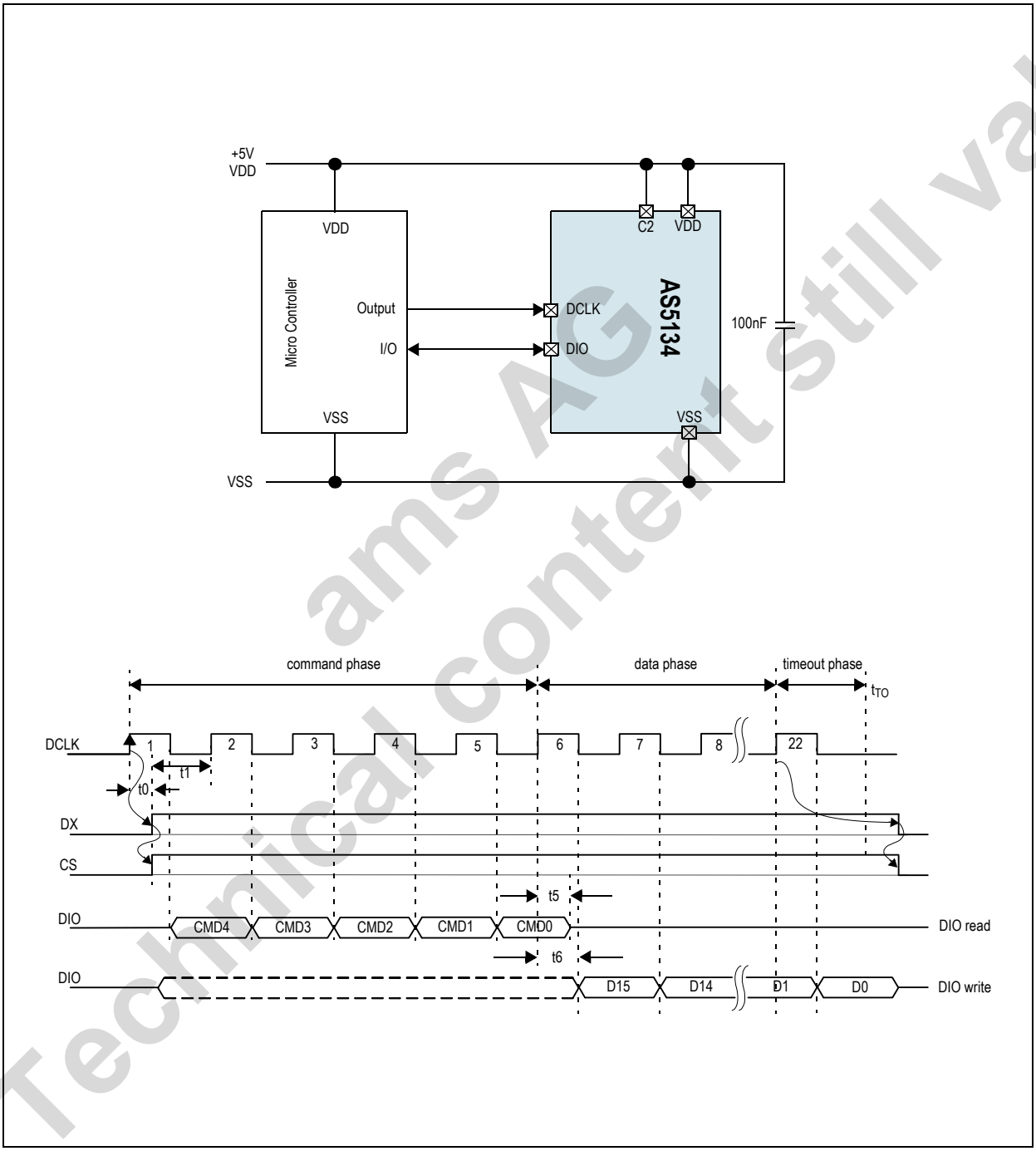
Command					Read Data														
C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	lock	AGC						Angle								

7.4 Serial 2-Wire Connection (R/W Mode)

By connecting the configuration input C2 to VDD, the AS5134 is configured to 2-wire data transmission mode. Only Clock (DCLK) and Data (DIO) signals are required. A Chip Select (CS) signal is automatically generated by the DX output, when a time-out of DCLK occurs.

Note: Read-only mode is also possible in this configuration.

Figure 6. 2-Wire R/W Mode

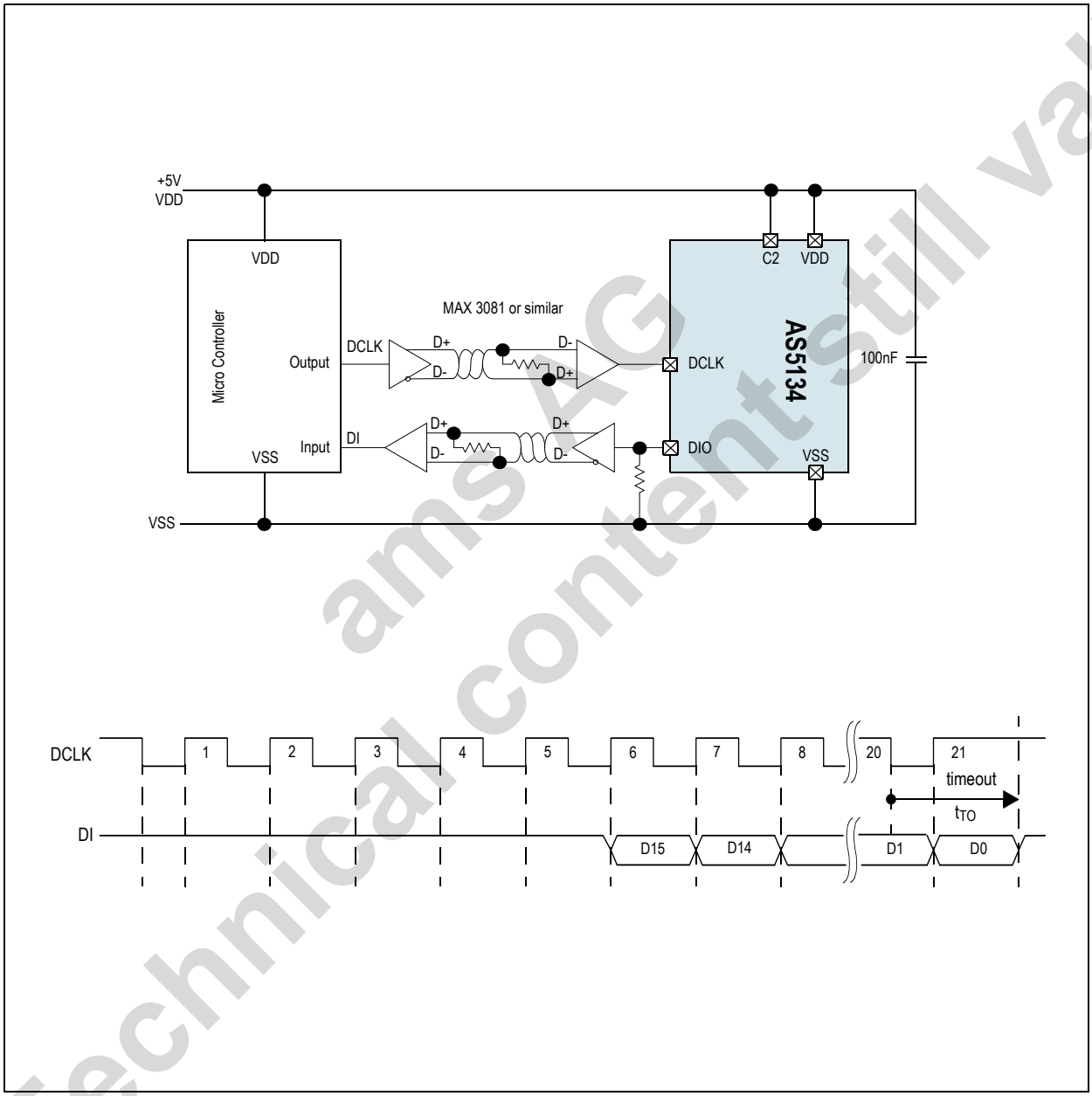


7.5 Serial 2-Wire Differential SSI Connection

With the addition of a RS-422 / RS-485 transceiver, a fully differential data transmission, according to the 21-bit SSI interface standard is possible. To be compatible with this standard, the DCLK signal must be inverted. This is done by reversing the Data+ and Data- lines of the transceiver.

Note: This type of transmission is read-only.

Figure 7. 2-Wire SSI Read-only Mode

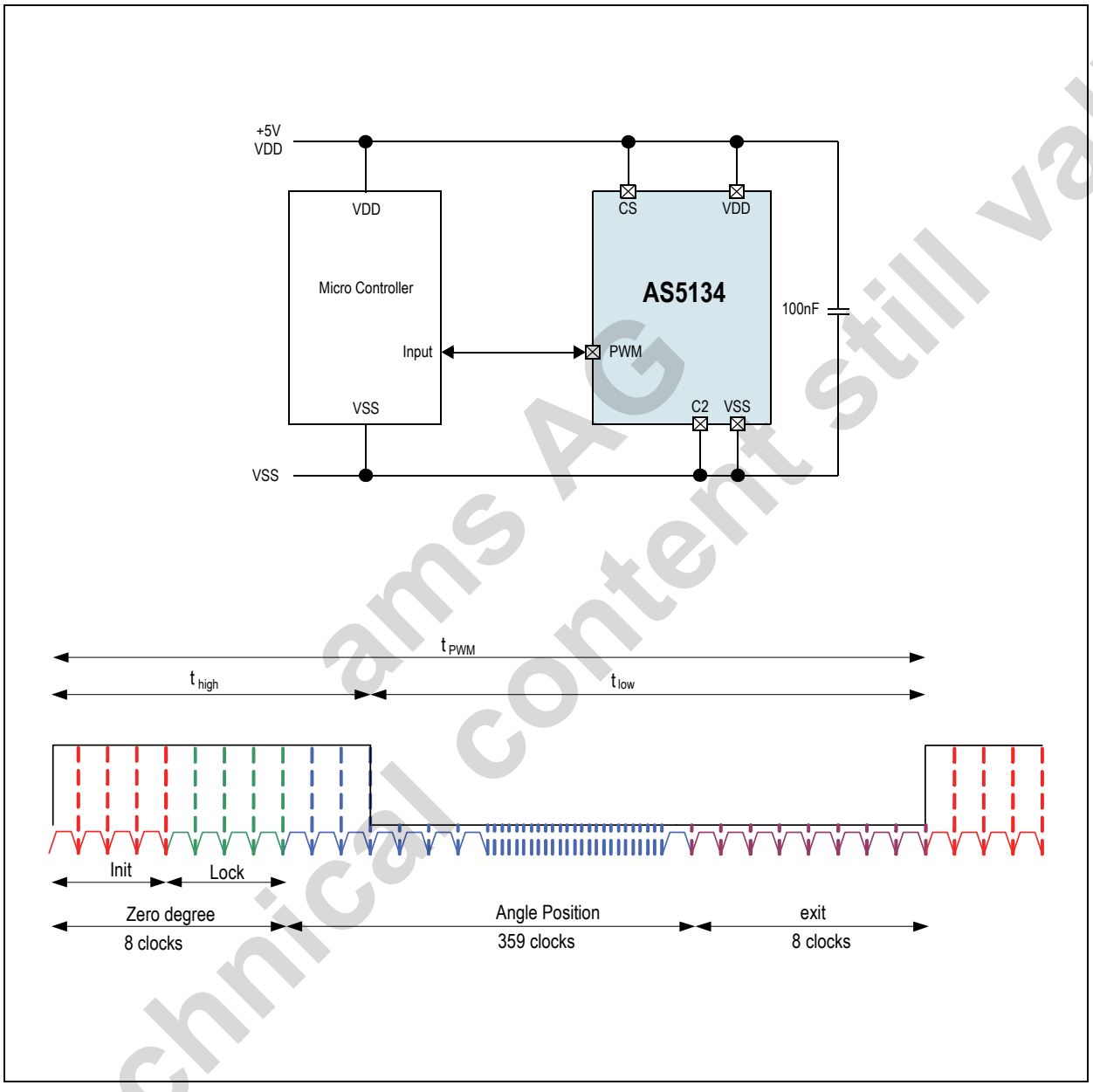


Refer to Table 6 on page 9 for information on 2-or 3-wire Read-only Serial Bit Sequence (21-bit read).

7.6 1-Wire PWM Connection

This configuration uses the least number of wires: only one line (PWM) is used for data, leaving the total number of connection to three, including the supply lines. This type of configuration is especially useful for remote sensors. Ultra Low Power Mode is not possible in this configuration, as there is no bi-directional data transmission. Pins that are not shown may be left open.

Figure 8. Data Transmission with Pulse Width Modulated (PWM) Output



The PWM signal will be generated from the actual stored angle information. The zero-angle corrected value is buffered and fixed until the next PWM-sequence is started. To ease the filtering of the PWM signal, a minimum pulse width is implemented in the protocol.

Figure 9. Output PWM Signal After Start-up at 0º Unprogrammed Zero Position

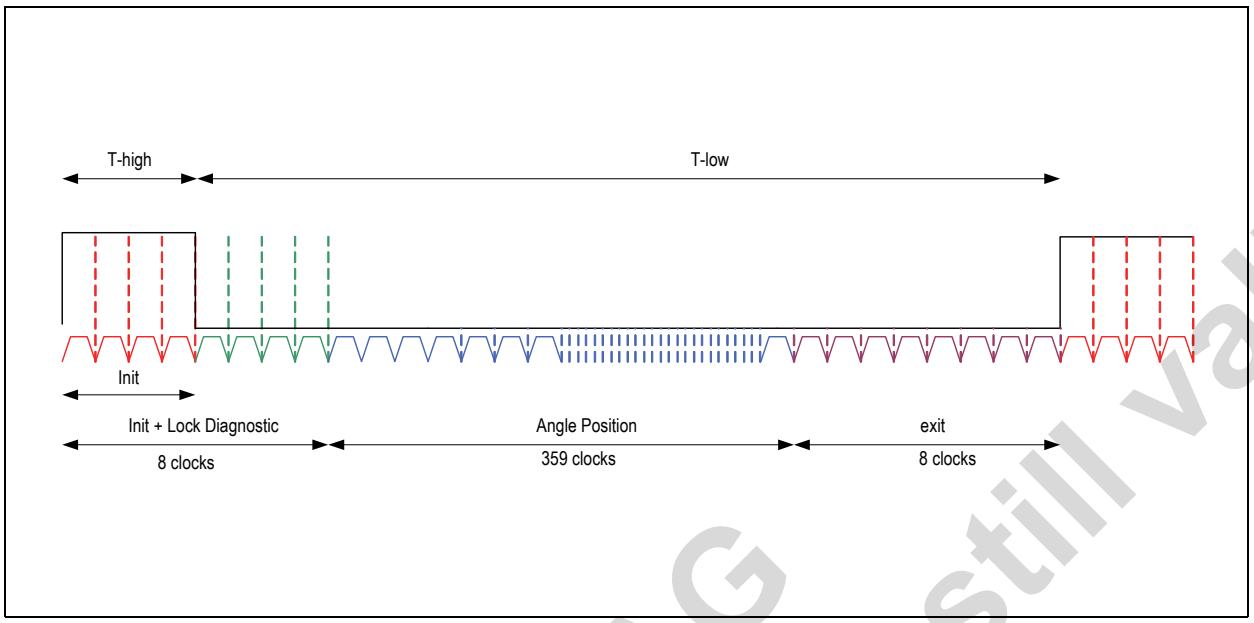
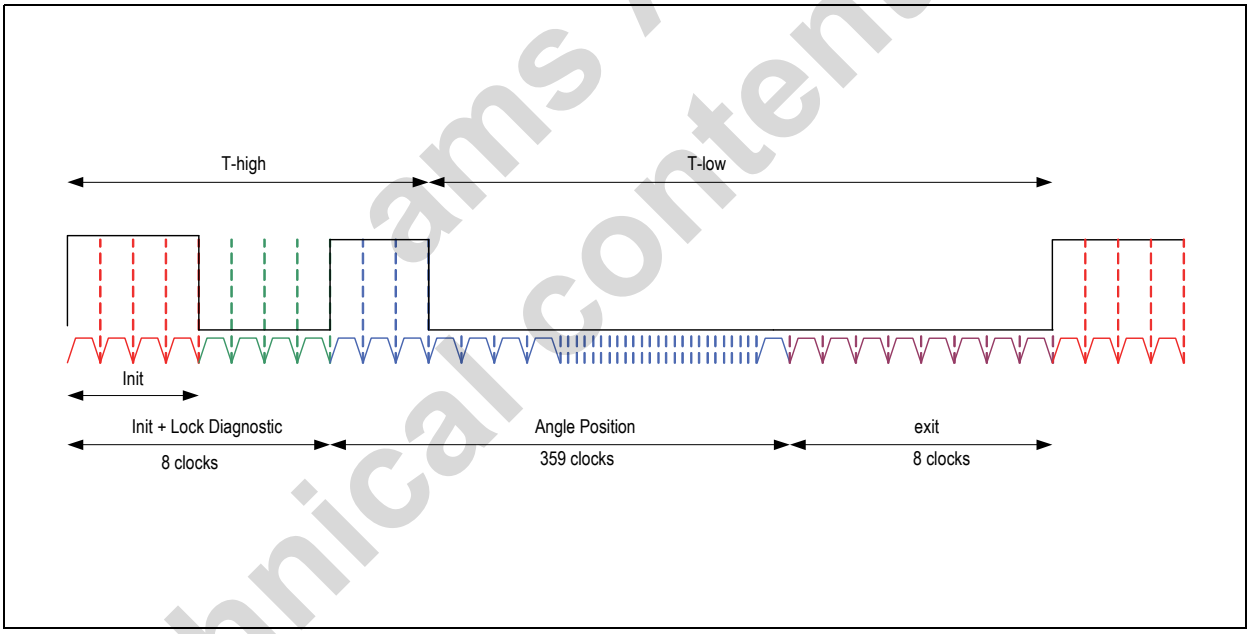


Figure 10. Output PWM Signal After Start-up at Initial 0º with a Programmed Zero Position

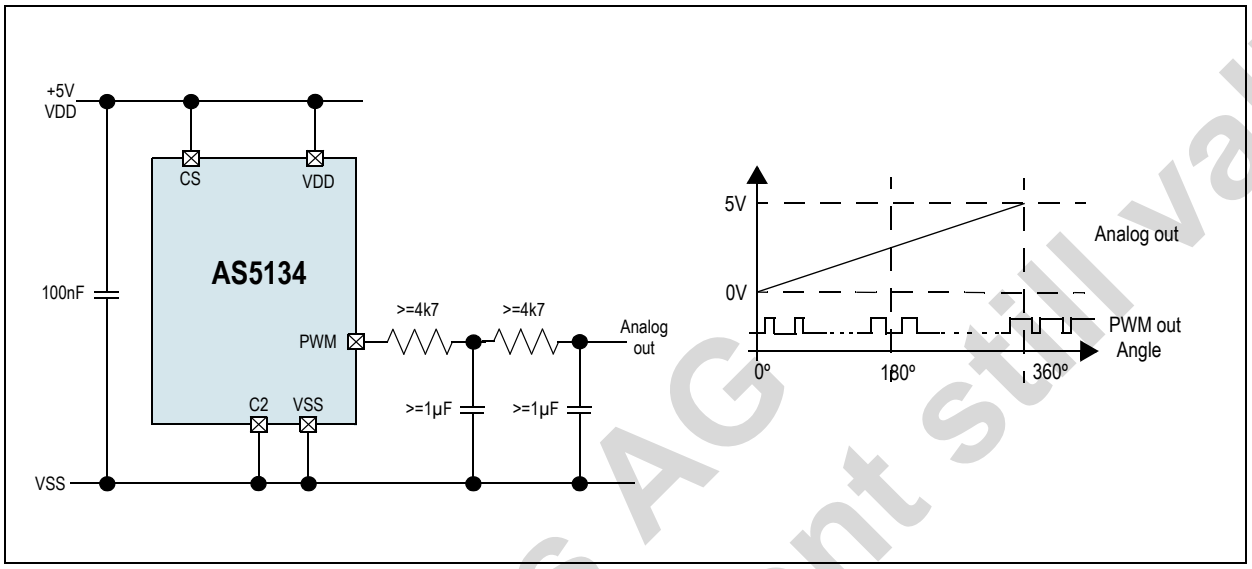


After a startup of the AS5134 at the initial zero position the PWM signal indicates a permanent lock diagnostic. This behavior can be ignored during elaboration of the PWM duty cycle. Figure 9 and Figure 10 show the different outputs depending on the OTP zero position programming. After a mechanical movement (1º) the signal will change as shown in Figure 8. A startup at any other position will also look like as shown in Figure 8.

7.7 Analog Output

This configuration is similar to the PWM connection (only three lines including supply are required). With the addition of a lowpass filter at the PWM output, this configuration produces an analog voltage that is proportional to the angle. This filter can be either passive (as shown in Figure 11) or active. The lower the bandwidth of the filter, the less ripple of the analog output can be achieved. If the AS5134 angular data is invalid, the PWM output will remain at low state and thus the analog output will be 0V. Pins that are not shown may be left open.

Figure 11. Data Transmission with Pulse Width Modulated (PWM) Output



7.8 Quadrature A/B/Index Output

The phase shift between channel A and B indicates the direction of the magnet movement. Channel A leads channel B at a clockwise rotation of the magnet (top view) by 90 electrical degrees. Channel B leads channel A at a counter-clockwise rotation.

Figure 12. Incremental Output Modes

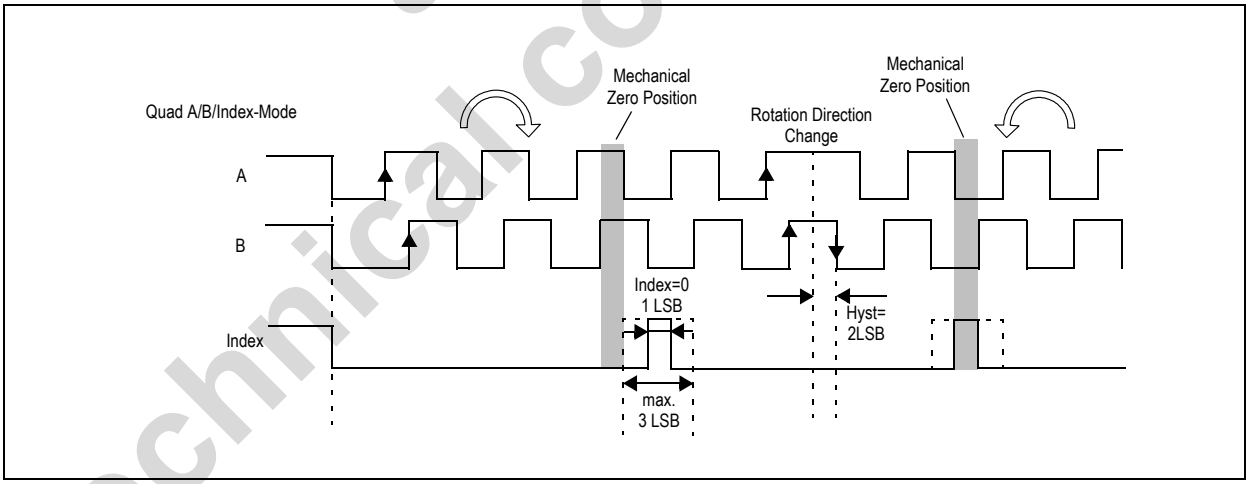


Table 7. Programming Options for the Quadrature Signals A/B/Index

Abi (13:12)		Function: output multiplexer for pin A,B,I
0	0	A → pin A, B → pin B, I(index) → pin I default value)
0	1	step → pin A, direction → pin B, I(index) → pin I
1	0	pulse → pin A, direction → pin B, I(index) → pin I
1	1	off: LO → pin A, LO → pin B, LO → pin I

7.9 Brushless DC Motor Commutation Mode

The BLDC signals will be used to control the electrical angle information – according to the amount of pole pairs and the actual mechanical angle position. Refer Figure 13 for an example of n_pole_pairs:=2. For the programming, refer to Serial Synchronous Interface (SSI) on page 18.

Figure 13. Commutation Mode

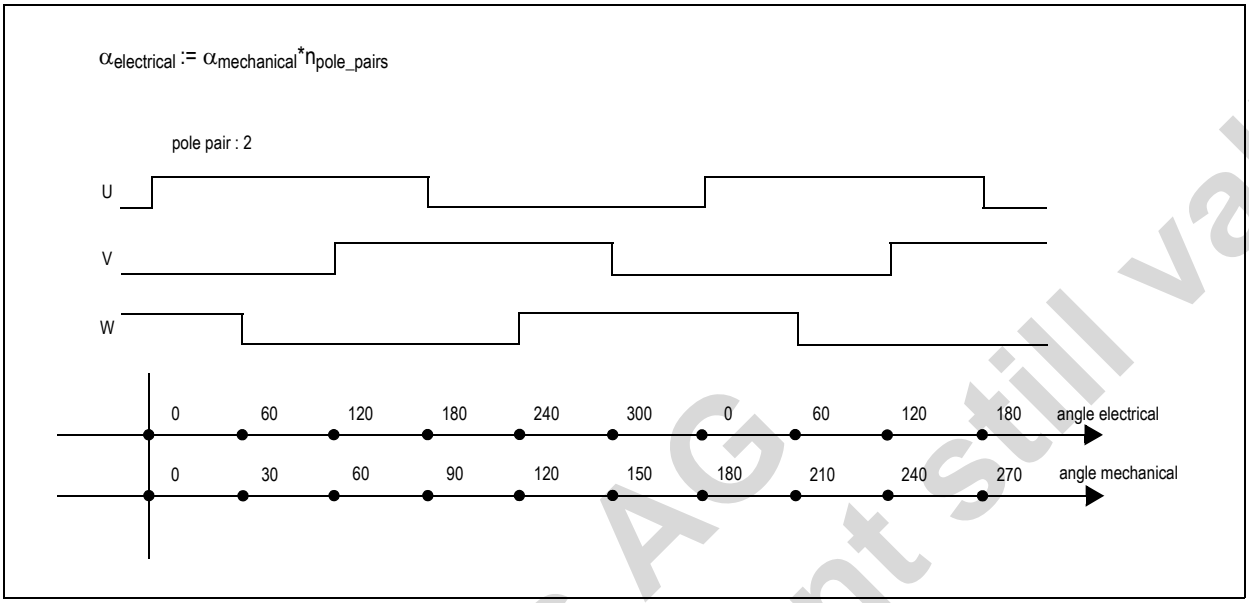


Table 8. Programming Options for the Commutation Signals U/V/W

uvw (11:9)			Function
0	0	0	BLDC Pole Pairs : 1 → electrical angle of 60º = mechanical angle: 60º
0	0	1	BLDC Pole Pairs : 2 → electrical angle of 60º = mechanical angle: 30º
0	1	0	BLDC Pole Pairs : 3 → electrical angle of 60º = mechanical angle: 20º
0	1	1	BLDC Pole Pairs : 4 → electrical angle of 60º = mechanical angle: 15º
1	0	0	BLDC Pole Pairs : 5 → electrical angle of 60º = mechanical angle: 12º
1	0	1	BLDC Pole Pairs : 6 → electrical angle of 60º = mechanical angle: 10º
1	1	1	off → LO pad U, V, W, PWM

7.10 Daisy Chain Mode

The angle information from the device and the setup for the device is handled over the digital interface. A special port (Dx) can be used to implement a daisy chain mode. Depending on the configuration, it is possible to implement a two wire or a three wire mode. In the three wire mode, each communication starts with the rising edge of the chip select signal. The Port Dx is used to transfer the chip select information from one device to the next. Refer to Figure 14 and Figure 15. In the two wire interface mode, a timeout logic ensures that the digital interface will be reset if there is no clock source available for a certain time. The synchronization between the internal free running analog clock oscillator and the external used digital clock source for the digital interface is done in a way that the digital clock frequency can vary in a wide range.

Remark: Reset for the digital interface:

3 wire mode → via chip select

2 wire mode → via timeout

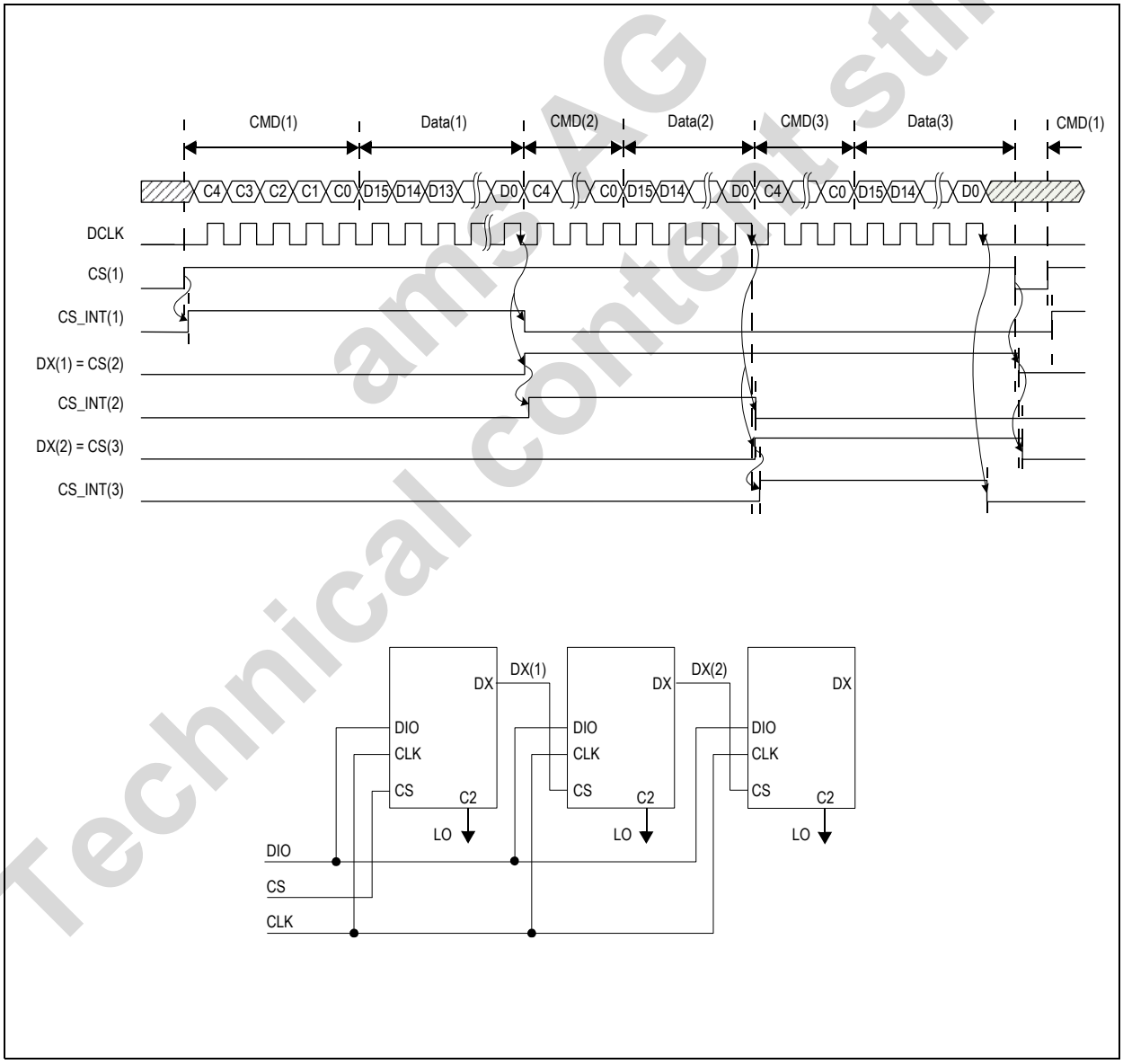
Port	Symbol	Function
Chip Select	CS	Indicates the start of a new access cycle to the device CS = LO → reset of the digital interface.
DCLK	DCLK	Clock source for the communication over the digital interface. The maximum and minimum frequency depends on the mode.

Port	Symbol	Function
Bidirectional data input output	DIO	Command and data information over one single line. The first bit of the command defines a read or write access.
Daisy Chain Port	Dx	This port enables the daisy chain configuration of several devices. **Three wire mode:** Indicates the end of an interface cycle. Dx can be used as the chip select signal for the next device in the chain. **Two wire mode:** Will be set with the first falling edge of DCLK and hence, indicates a running clock; it will be cleared at the end of the command sequence or after a timeout phase. Dx can be used as a chip select signal in the two wire mode.

Waveform – Digital Interface at Three Wire Daisy Chain Mode

Note: Defined if the Pin C2 is set to LO at all devices.

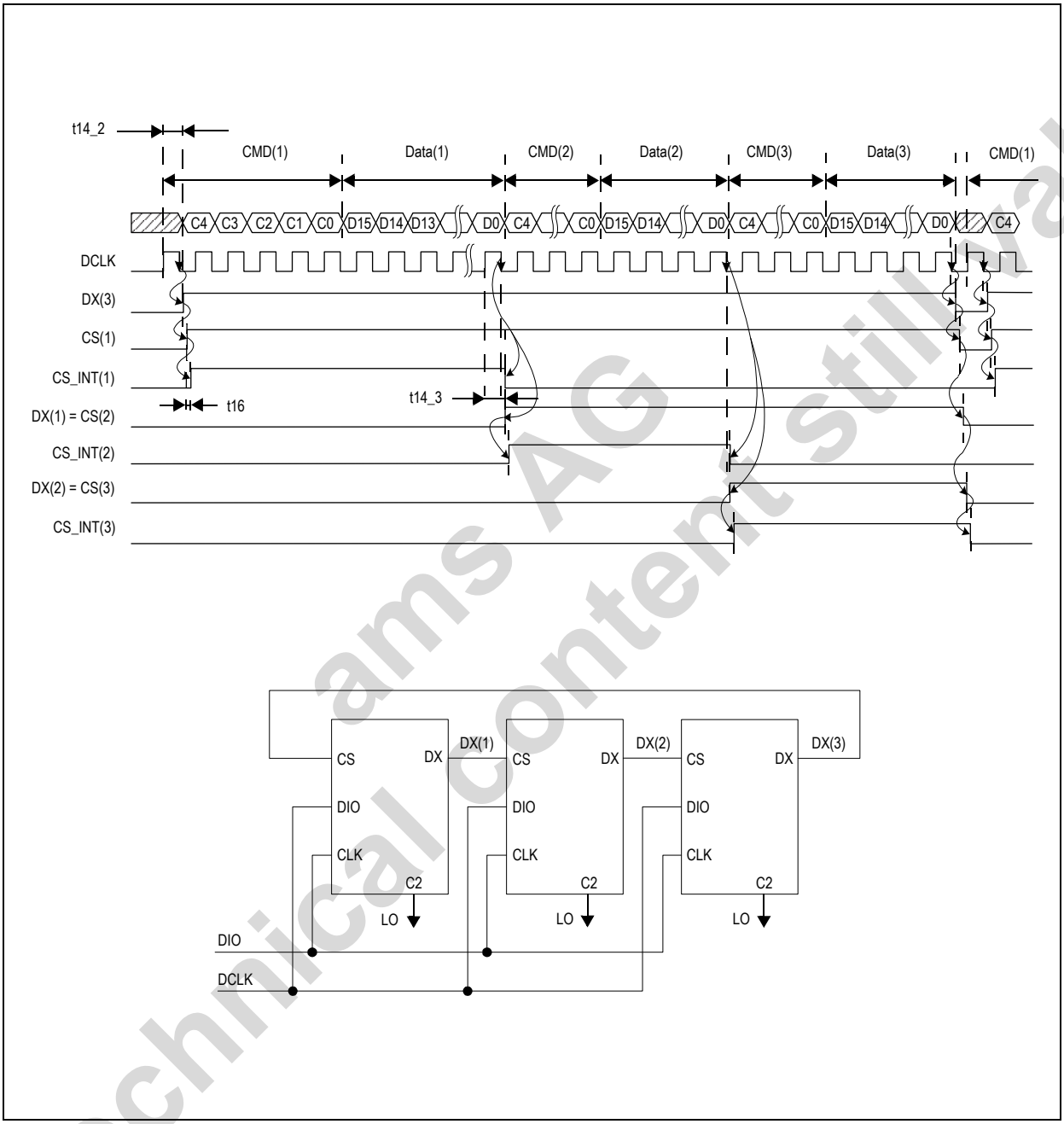
Figure 14. 3-Wire Daisy Chain Mode



Waveform – Digital Interface at Two Wire Daisy Chain Mode

Note: Defined, if the Pin C2 is set to LO at all devices except the last one where the Pin C2 is set to HI.

Figure 15. 2-Wire Daisy Chain Mode



7.11 Serial Synchronous Interface (SSI)

Normal mode is used for normal operations, whereas extended mode is for accessing the OTP.

Table 9. Commands of the SSI in Normal Mode

Digital interface at normal mode																			
#	cmd	bin	mode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23	WRITE CONFIG 1	10111	write	LP	SM_ RES	tst	tst	Hyst <1:0>		tst	tst	tst							
20	SET MT COUNTER	10100	write	multi-turn-counter <8:0>															
16	EN PROG	10000	write	1	0	0	0	1	1	0	0	1	0	1	0	1	1	1	0
4	RD MT COUNTER	00100	read	multi-turn-counter <8:0>									OTP _OK						
0	RD_ANGLE	00000	read	lock_ adc	agc <5:0>						angle <8:0>								

SM_RES: State machine reset of the digital part of the device (soft reset).

EN PROG: Enables the access to the OTP register in Extended Mode.

WRITE CONFIG: LP HI activates the sleep mode of the AS5134. The power consumption is significantly reduced. LP LO returns to normal operation mode. During sleep mode, the lock_adc bit in command 0 is LO.

RD_MT Counter: Command for read out of multi turn register.

OTP_OK: Bit shows correct readout of the OTP register after startup. The bit is valid till the next OTP access.

RD_ANGLE: Command for read out of angle value and AGC value (agc). “Lock” indicates a locked ADC.

tst: Test bits for internal testing (must be left unchanged).

Hyst (11:10): Digital Hysteresis can be set via the digital interface 0, 1, 2 (default), 3 LSB

Hyst		Function
0	0	2 LSB (default value)
0	1	1
1	0	3
1	1	0

The hysteresis can be changed over the interface. An activation of the SM_RES bit is required. This can be performed in two steps -

1. Use WRITE CONFIG 1 command and write the selected hysteresis and SM_RES = ‘1’ into the device.
2. Use again WRITE CONFIG 1 command and release SM_RES = ‘0’ with the same hysteresis setting.

SET MT COUNTER: Command for setting the Multi Turn Counter to a defined value.

LP: Default "0"; "1" for using the low power function.

lock_adc: Indicates that the tracking adc is in a locked status. For a valid angle (the magnetic field has to be in a certain range, which is indicated by the agc value) or a missing magnet the lock_adc is set.

Table 10. Commands of the SSI in Extended Mode

				Digital interface at extended mode											
Number of bits				Factory Settings											
				2	18	1	1	4	4	1	4	2	3	1	4
#	cmd	bin	mode	61 ..60	59 ..42	41	40	39 ..36	35 ..32	31	30 ..27	26 ..25	24 ..22	21	20 ..
31	WRITE OTP	11111	xt write	tst	ID	tst	tst	tst	tst	tst	tst	tst	tst	lock_otp (*)	r_ a
25	PROG_OTP	11001	xt write	tst	ID	tst	tst	tst	tst	tst	tst	tst	tst	lock_otp (*)	r_ a
15	READ_OTP	01111	xt read	tst	ID	tst	tst	tst	tst	tst	tst	tst	tst	lock_otp (*)	r_ a
9	READ ANA	01001	xt read	tst	ID	tst	tst	tst	tst	tst	tst	tst	tst	lock_otp (*)	r_ a

WRITE OTP: Writing of the OTP register. The written data is volatile. “Zero Angle” is the angle, which is set for zero position. “Sensitivity” is the gain number of bits, which allows the customer to overwrite one of the customer OTP bits <0:15>.

PROG_OTP: Programming of the OTP register. Only Bits <0:20> can be programmed by the customer. The internal factory settings are locked by a

READ_OTP: Read out the content of the OTP register. Data written by WRITE_OTP and PROG_OTP is read out.

READ ANA: Analog read out mode. The analog value of every OTP bit is available at pin 1 (PROG), which allows for a verification of the fuse proce

tst: Test bits for internal testing (must be left unchanged).

ID (59:42): Chip identifier to track the device in the field

lock_otp (21): To disable the programming of the factory bits – write access is still possible

r_add (20:17): The following OTP bits can be modified according to the requirements of the application.

r_bit (16): Redundancy bit (functionality is only implemented in the user region)

Sensitivity (15:14): Trim bit for the gain of the amplifier after the demodulator

abi (13:12): Mode selection for the incremental signals

uvw (11:9): Number of poles of the brush less dc motor - impact to the uvw signals

zero angle (8:0): Trim bit for the zero angle information

LP: Enables the low power mode to reduce the current consumption - digital registers are not reset.

Notes:

1. The Extended Mode can be enabled by sending command 16 (EN PROG).
2. The lock bit will be deleted during power down or sleep mode to ensure that the user is able to detect that the read out angle value is comp
3. In extended mode 1 data bit (wirte/read) requires 4 clock cycles (see Figure 19).

7.12 Redundancy

For a better programming reliability, a redundancy is implemented. This function can be used in case if the programming of one bit fails. With an add
programmed.

Table 11. Redundancy Addressing

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	
R_add	R_add	R_add	R_add	R_bit	Sensitivity	Sensitivity	ABI	ABI	U	V	W	ZA	ZA	ZA	Z
0	0	0	0	1	/	/	/	/	/	/	/	/	/	/	
0	0	0	1	1	/	/	/	/	/	/	/	/	/	/	
0	0	1	0	1	/	/	/	/	/	/	/	/	/	/	
0	0	1	1	1	/	/	/	/	/	/	/	/	/	/	
0	1	0	0	1	/	/	/	/	/	/	/	/	/	/	
0	1	0	1	1	/	/	/	/	/	/	/	/	/	/	
0	1	1	0	1	/	/	/	/	/	/	/	/	/	**1**	
0	1	1	1	1	/	/	/	/	/	/	/	/	**1**	/	
1	0	0	0	1	/	/	/	/	/	/	/	**1**	/	/	
1	0	0	1	1	/	/	/	/	/	/	**1**	/	/	/	
1	0	1	0	1	/	/	/	/	/	**1**	/	/	/	/	
1	0	1	1	1	/	/	/	/	**1**	/	/	/	/	/	
1	1	0	0	1	/	/	/	**1**	/	/	/	/	/	/	
1	1	0	1	1	/	/	**1**	/	/	/	/	/	/	/	
1	1	1	0	1	/	**1**	/	/	/	/	/	/	/	/	
1	1	1	1	1	**1**	/	/	/	/	/	/	/	/	/	

8 Application Information

The benefits of AS5134 are as follows:

- Complete system-on-chip, no angle calibration required
- Flexible system solution provides absolute serial, ABI, UVW and PWM outputs
- Ideal for applications in harsh environments due to magnetic sensing principle
- High reliability due to non-contact sensing
- Robust system, tolerant to horizontal misalignment, airgap variations, temperature variations and external magnetic fields

8.1 AS5134 Programming

The AS5134 offers the following user programmable options:

- ***Zero Position Programming.*** This programming option allows the user to program any rotation angle of the magnet as the new zero position. This useful feature simplifies the assembly process as the magnet does not need to be mechanically adjusted to the electrical zero position. It can be assembled in any rotation angle and later matched to the mechanical zero position by zero position programming. The 8,5-bit user programmable zero position can be applied both temporarily (command WRITE OTP, #31) or permanently (command PROG OTP, #25).
- ***Magnetic Field Optimization.*** This programming option allows the user to match the vertical distance of the magnet with the optimum magnetic field range of the AS5134 by setting the sensitivity level. The 2-bit user programmable sensitivity setting can be applied both temporarily (command WRITE OTP, #31) or permanently (command PROG OTP, #25).

8.1.1 OTP Programming Connection

Programming of the AS5134 OTP memory does not require a dedicated programming hardware. The programming can be simply accomplished over the serial 3-wire interface (see Figure 17) or the optional 2-wire interface (see Figure 6). For permanent programming (command PROG OTP, #25), a constant DC voltage of 8.0-8.5V must be connected to pin 1 (PROG). For temporary OTP write (“soft write”; command WRITE OTP, #31), the programming voltage is not required. The capacitors must be as close as possible to the pin, to ensure that a serial inductance of 50nH is not to be exceeded. The 50nH inductance could translate into a cable length of approximately 5cm.

Figure 16. OTP Programming Connection

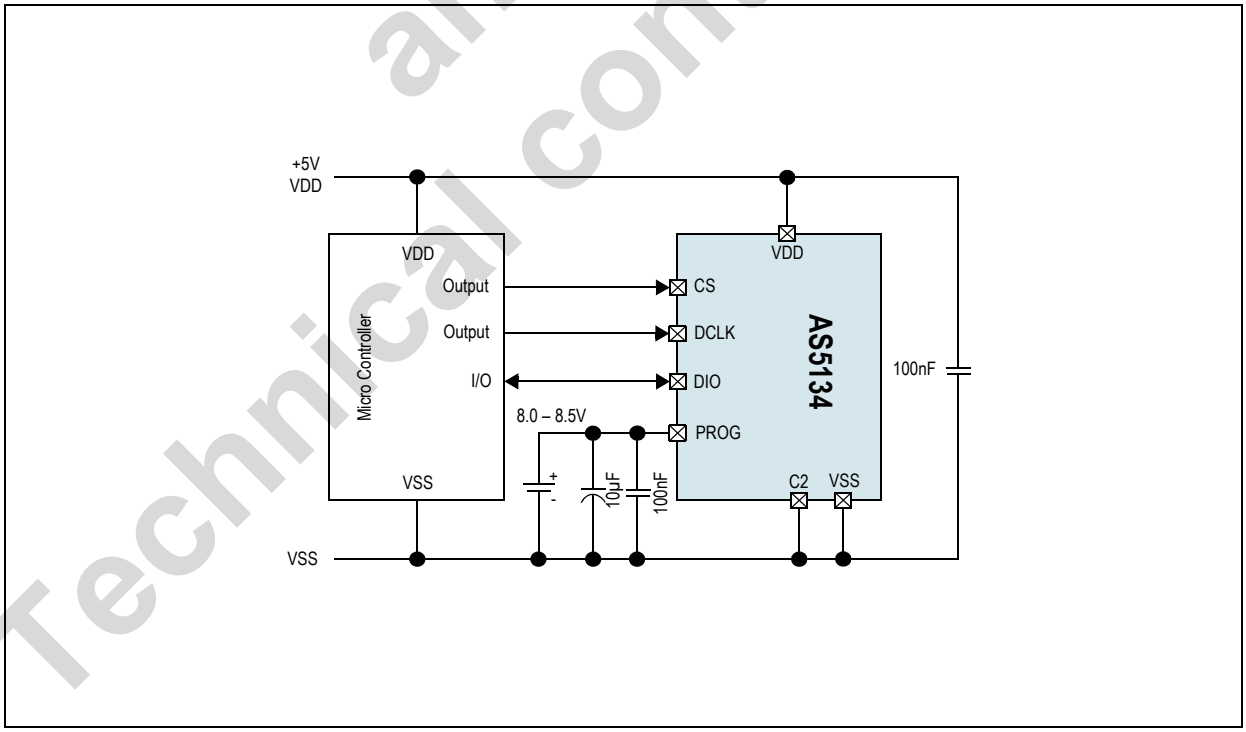
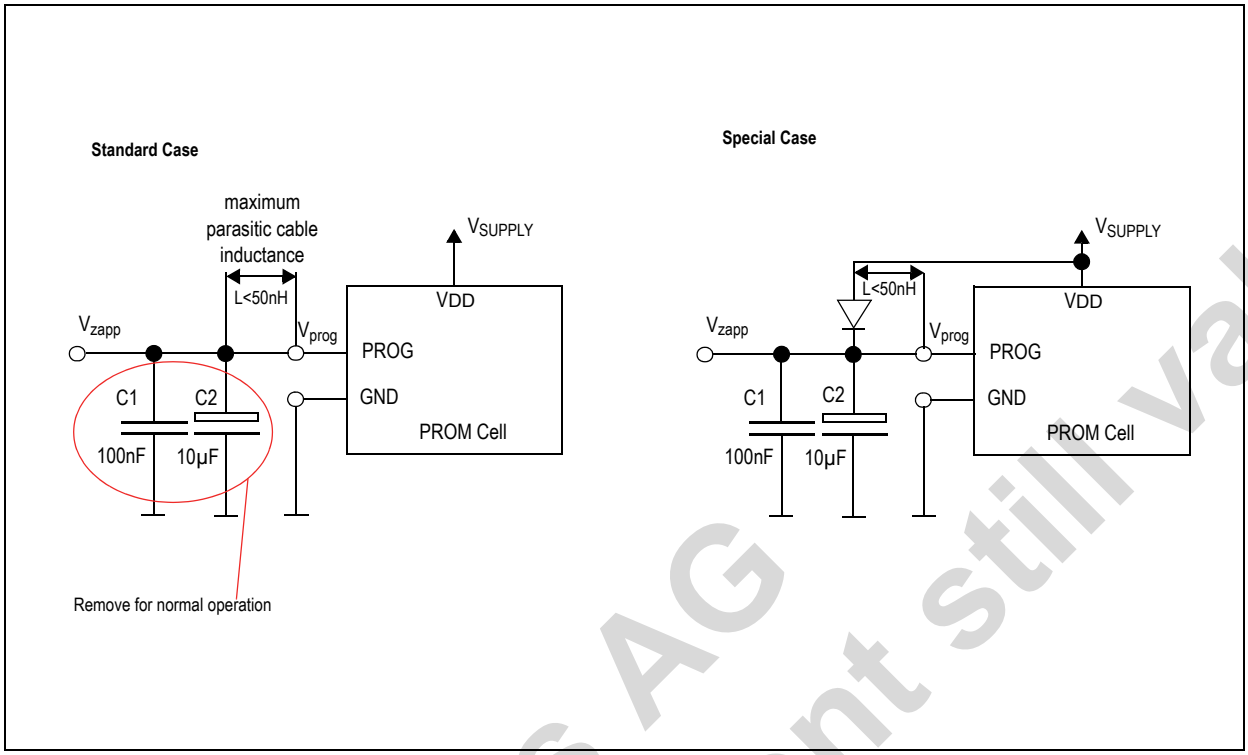


Figure 17. OTP Programming Connection



Note: The maximum capacitive load at PROG in normal operation is less than 20pF. However, during programming the capacitors C1+C2 are needed to buffer the programming voltage during current spikes, but they must be removed for normal operation. To overcome this contradiction, the recommendation is to add a diode (4148 or similar) between PROG and VDD as shown in Figure 17 (special case setup), if the capacitors can not be removed at final assembly.

Due to D1, the capacitors C1+C2 are loaded with VDD-0.7V at startup, hence not influencing the readout of the internal OTP registers. During programming the OTP, the diode ensures that no current is flowing from PROG (8-8.5V) to VDD (5V).

In the standard case (see Figure 17), the verification of a correct OTP readout can be done either by analog readback of the OTP register or with the aid of the OTP_OK bit. The special case setup provides only the OTP_OK bit for verifying the correct reading of the OTP. Analog readback is not usable in the special case mode, as the diode pulls the PROG pin to VDD.

The OTP_OK bit can be accessed with command #4 (see Table 9).

As long as the PROG pin is accessible it is recommended to use standard setup. In case the PROG pin is not accessible at final assembly, the special setup is recommended.

8.1.2 Programming Verification

After programming, the programmed OTP bits must be verified in two ways:

Digital Read Out (Mandatory): After sending a READ OTP command, the readback information must be the same as programmed information. Otherwise, it indicates that the programming was not performed correctly.

Note: Either “Digital Verification” or “Analog Verification” must be carried out in addition to the “Digital Read Out”.

Digital Verification: Checking the OTP_OK bit (0 = OK, 1 = error)

i) At room temperature

ii) Right after the programming

Analog Verification: By switching into Extended Mode and sending a READ ANA command, the pin PROG becomes an output sending an analog voltage with each clock representing a sequence of the bits in the OTP register (starting with D61). A voltage of <500mV indicates a correctly programmed bit (“1”) while a voltage level between 2V and 3.5V indicates a correctly unprogrammed bit (“0”). Any voltage level in between indicates incorrect programming.

Figure 18. Analog OTP Verification

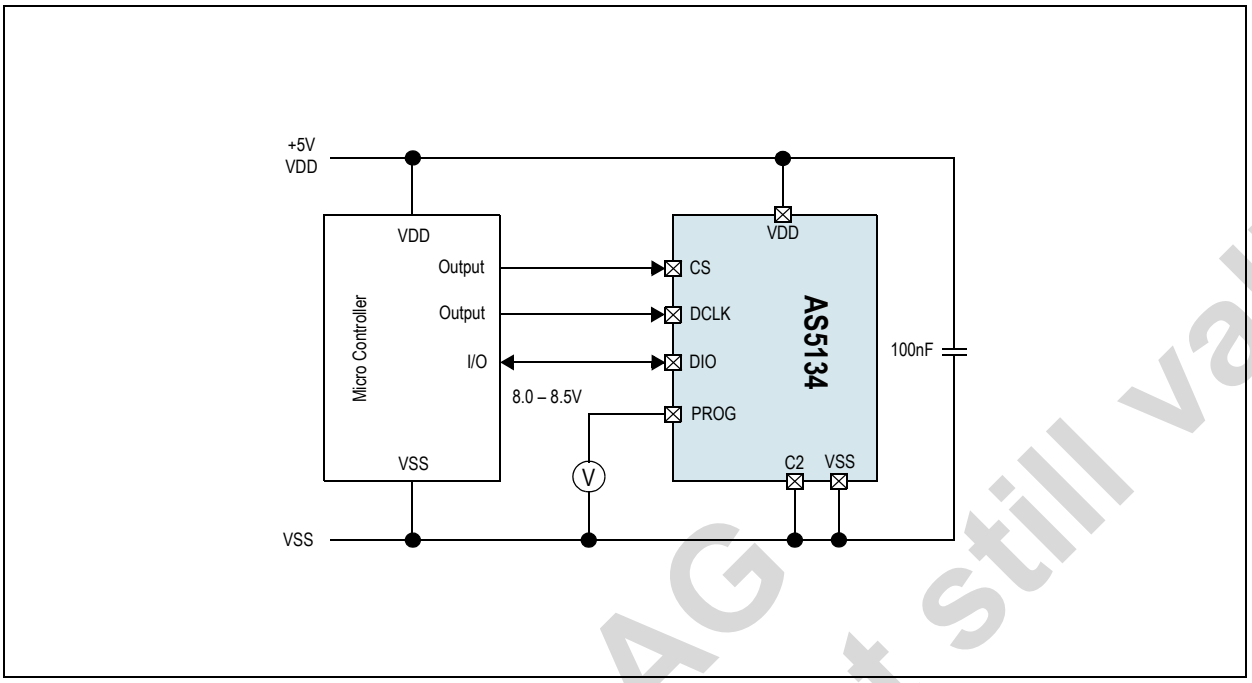
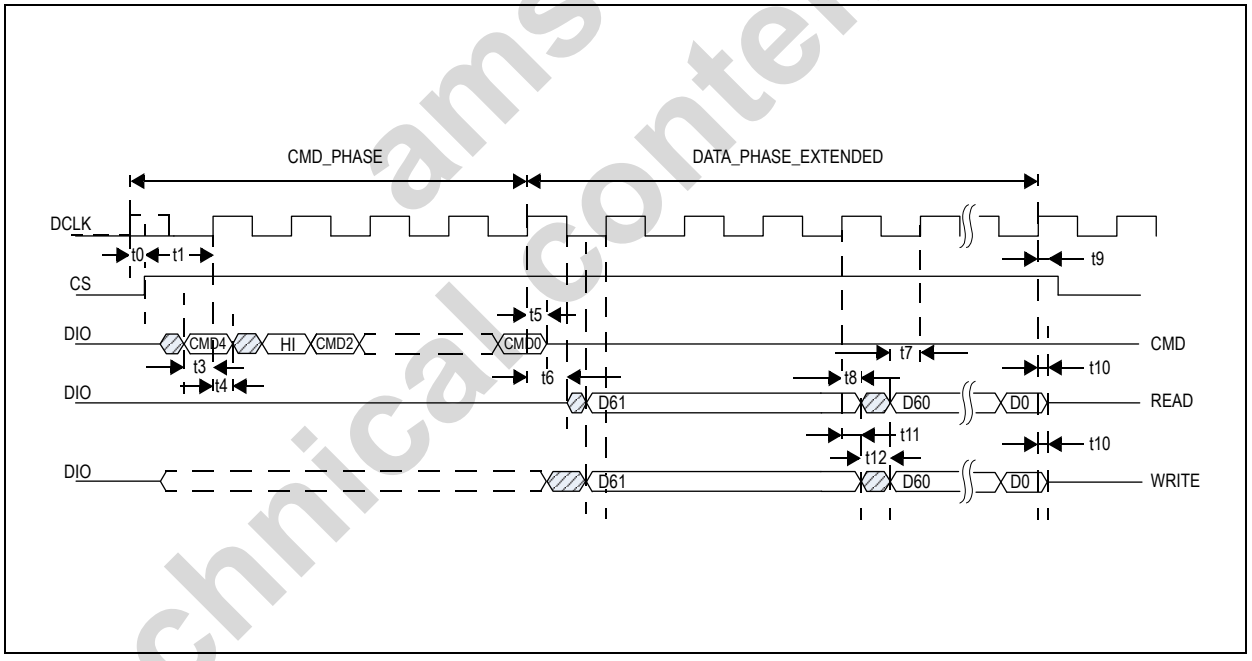


Figure 19. Extended Operation Mode: Timing of Analog Readout



8.2 AS5134 Status Indicators

8.2.1 Lock Status Bit

The Lock signal indicates, whether the angle information is valid (ADC locked, Lock = high) or invalid (ADC unlocked, Lock = low). To determine a valid angular signal at best performance, the following indicators can be set:

Lock = 1

AGC = >00H and < 3FH

After a startup of the AS5134 at the initial zero position the lock status bit will remain at (Lock=0). After a mechanical rotation (1°) the lock status bit will change to (Lock=1).

Note: The angle signal is also valid (Lock = 1), when the AGC is out of range (00H or 3FH), but the accuracy of the AS5134 is reduced due to the out of range condition of the magnetic field strength.

8.2.2 Magnetic Field Strength Indicators

The AS5134 is not only able to sense the angle of a rotating magnet, it can also measure the magnetic field strength (and hence the vertical distance) of the magnet. This additional feature can be used for several purposes:

- as a safety feature by constantly monitoring the presence and proper vertical distance of the magnet
- as a state-of-health indicator, e.g. for a power-up self test
- as a pushbutton feature for rotate-and-push types of manual input devices

The magnetic field strength information is available in two forms:

Magnetic Field Strength Software Indicator. The serial data that is obtained by command READ ANGLE contains the 6-bit AGC information. The AGC is an automatic gain control that adjusts the internal signal amplitude obtained from the Hall elements to a constant level. If the magnetic field is weak, e.g. with a large vertical gap between magnet and IC, with a weak magnet or at elevated temperatures of the magnet, the AGC value will be high. Likewise, the AGC value will be lower when the magnet is closer to the IC, when strong magnets are used and at low temperatures.

The best performance of the AS5134 will be achieved when operating within the AGC range. It will still be operational outside the AGC range, but with reduced performance especially with a weak magnetic field due to increased noise.

Factors Influencing the AGC Value. In practical use, the AGC value will depend on several factors:

- **The initial strength of the magnet.** Aging magnets show a reducing magnetic field over time which results in an increase of the AGC value. The effect of this phenomenon is relatively small and can easily be compensated by the AGC.
- **The vertical distance of the magnet.** Depending on the mechanical setup and assembly tolerances, there will always be some variation of the vertical distance between magnet and IC over the lifetime of the application using the AS5134. Again, vertical distance variations can be compensated by the AGC.
- **The temperature and material of the magnet.** The recommended magnet for the AS5134 is a diametrically magnetized, 5-6mm diameter NdFeB (Neodymium-Iron-Boron) magnet. Other magnets may also be used as long as they can maintain to operate the AS5134 within the AGC range. Every magnet has a temperature dependence of the magnetic field strength. The temperature coefficient of a magnet depends on the used material. At elevated temperatures, the magnetic field strength of a magnet is reduced, resulting in an increase of the AGC value. At low temperatures, the magnetic field strength is increased, resulting in a decrease of the AGC value. The variation of magnetic field strength over temperature is automatically compensated by the AGC.

OTP Sensitivity Adjustment. To obtain best performance and tolerance against temperature or vertical distance fluctuations, the AGC value at normal operating temperature is in the middle between minimum and maximum, hence it is around 100000 bin (20hex). To facilitate the “vertical centering” of the magnet+IC assembly, the sensitivity of the AS5134 can be adjusted in the OTP register in 4 steps. A sensitivity adjustment is recommended, when the AGC value at normal operation is close to its lower limit (around 00H). The default sensitivity setting is 00_H = low sensitivity. Any value >00_H will increase the sensitivity (see Table 3).

8.3 Multi Turn Counter

A 9-bit register is used for counting the magnet's revolutions. With each zero transition in any direction, the output of a special counter is incremented or decremented. The initial value after reset is 0 LSB. The multi turn value is encoded as complement on two. Clockwise rotation gives increasing angle values and positive turn count. Counter clockwise rotation exhibits decreasing angle values and a negative turn count respectively.

Bit Code	Decimal Value
011111111	256
---	---
01111111	127
---	---
00000011	+3
00000010	+2
00000001	+1
00000000	0
11111111	-1
11111110	-2
11111101	-3
---	---
10000000	-128
---	---
100000000	-255

The counter output can be reset by using command 20 – SET MT Counter. It is immediately reset by the rising clock edge of this bit. Any zero crossing between the clock edge and the next counter readout changes the counter value.

8.4 High Speed Operation

The AS5134 is using a fast tracking ADC (TADC) to determine the angle of the magnet. Once the TADC is synchronized with the angle, it sets the LOCK bit in the status register. In worst case, usually at start-up, the TADC requires up to 179 steps to lock. Once it is locked, it requires only one cycle to track the moving magnet. The AS5134 can operate in locked mode at rotational speeds up to 76875 rpm.

In Low Power Mode, the position of the TADC is frozen. It will continue from the frozen position once it is powered up again. If the magnet has moved during the power down phase, several cycles will be required before the TADC is locked again. The tracking time to lock in with the new magnet angle can be roughly calculated as:

$$t_{LOCK} = \frac{2\mu s * |NewAngle - OldAngle|}{1.406} \quad \text{(EQ 1)}$$

Where:

t_{LOCK} = Time required to acquire the new angle after power up from one of the reduced power modes [µs]
OldAngle = Angle position when one of the reduced power modes is activated [°]
NewAngle = Angle position after resuming from reduced power mode [°]

8.4.1 Propagation Delay

The Propagation delay is the time required from reading the magnetic field by the Hall sensors to calculating the angle and making it available on the serial or PWM interface. While the propagation delay is usually negligible on low speeds, it is an important parameter at high speeds. The longer the propagation delay, the larger becomes the angle error for a rotating magnet as the magnet is moving while the angle is calculated. The position error increases linearly with speed. The main factors that contribute to the propagation delay are discussed in detail further in this document.

8.4.2 Digital Readout Rate

Apart from the chip-internal propagation delay, the chip requires time to read and process the angle data. Due to its nature, a PWM signal is not usable at high speeds, as you get only one reading per PWM period. Increasing the PWM frequency improves it. But problems will occur at the receiving controller to resolve the PWM steps. The frequency on the AS5134 PWM output is typical 1.33kHz with a resolution of 2µs/step. A more suitable approach for high speed absolute angle measurement is using the serial interface. With a clock rate of up to 6MHz, a complete set of data (21bits) can be read in >3.5µs.

8.4.3 Low Power Mode

The target of this mode is to reduce the long time power consumption of the device for battery powered applications, without losing the actual angle information.

In Low Power Mode, the AS5134 is inactive. The last state (for e.g. the angle, AGC value, etc.) is frozen and the chip starts from this frozen state when it resumes active operation. This method provides much faster start-up than a “cold start” from zero. If the AS5134 is cycled between active and reduced current mode, a substantial reduction of the average supply current can be achieved. The minimum dwelling time is <0.5 ms. The actual active time depends on how much the magnet has moved while the AS5134 was in reduced power mode. The angle data is valid, when the status bit LOCK has been set. Once a valid angle has been measured, the AS5134 can be put back to reduced power mode. The average power consumption can be calculated as:

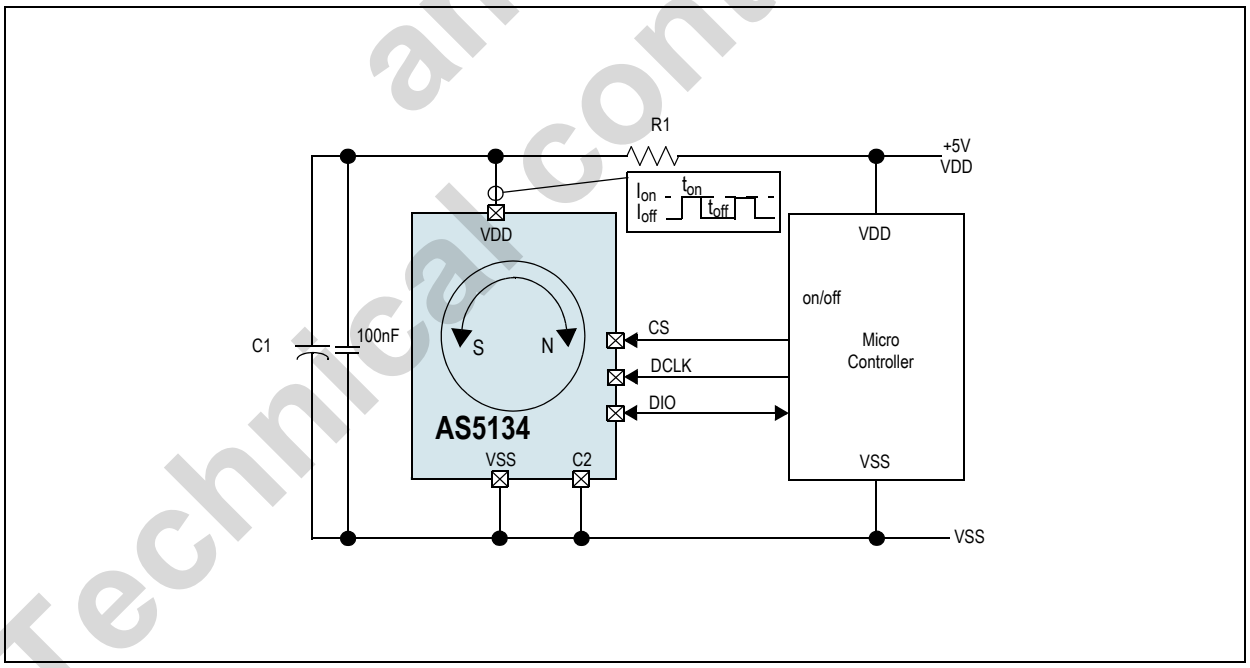
$$I_{avg} = \frac{I_{active} * t_{on} + I_{powerdown} * t_{off}}{t_{on} + t_{off}} \qquad \text{sampling interval} = t_{on} + t_{off} \qquad \textit{(EQ 2)}$$

Where:

I_{avg} = Average current consumption
I_{active} = Current consumption in active mode
$I_{power\_down} = I_{off}$: Current consumption in reduced power mode (max. 120µA)
t_{on} = Time period during which the chip is operated in active mode
t_{off} = Time period during which the chip is in reduced power mode

To access the Low Power Mode, the bit ‘LP’ <15> of the digital interface has to be set to “1”.

Figure 20. Low Power Mode Connection

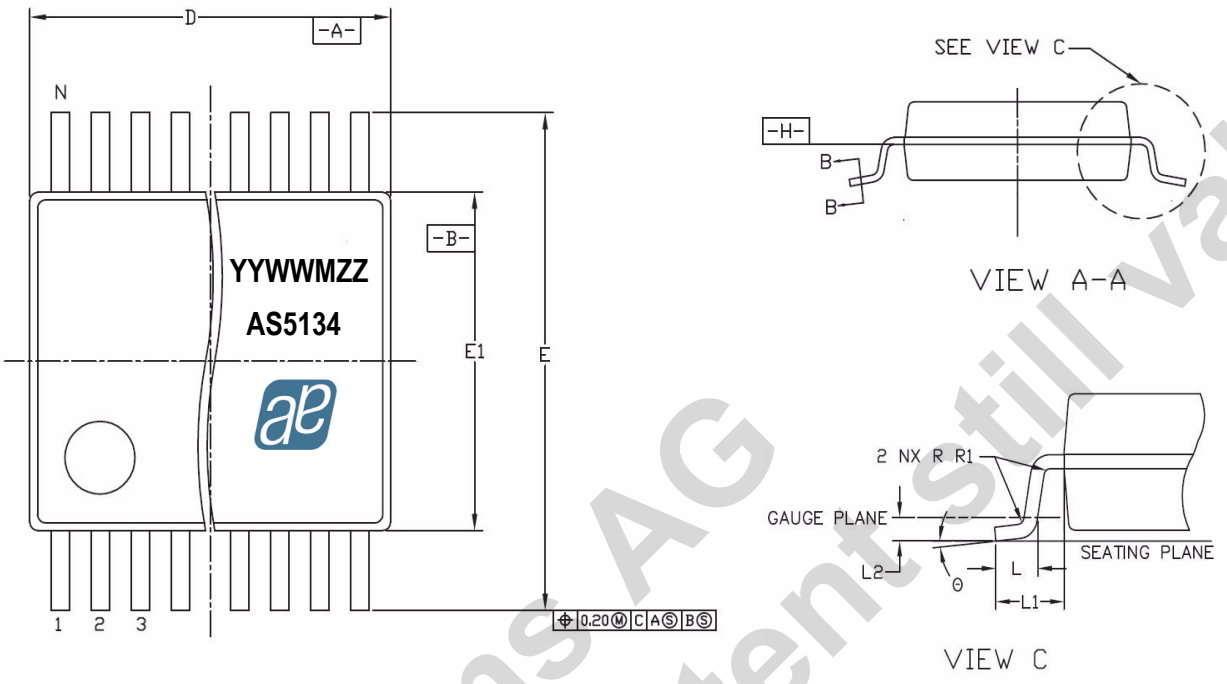


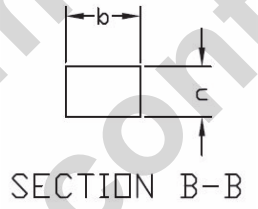
Reducing Power Supply Peak Currents. When the AS5134 is toggled between active and reduced power mode, there is the option to add an RC-filter (R1/C1) to avoid peak currents at power supply. The value of R1 is set that it maintains a VDD voltage of 4.5V – 5.5V and especially during long active periods the R1 must maintain the charge which C1 has expired. C1 can be set in such a way as it can support peak currents during the active operation period. In case of long active periods, C1 has a great value and R1 has a small value.

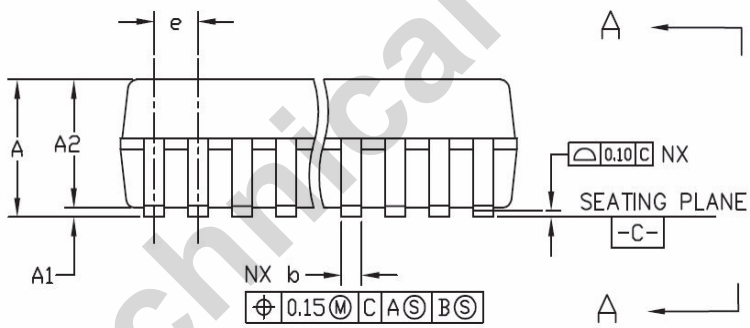
9 Package Drawings and Markings

The device is available in a 20-Lead Shrink Small Outline package.

Figure 21. Package Drawings and Dimensions







Symbol	Min	Nom	Max
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
b	0.22	0.30	0.38
c	0.09	0.17	0.25
D	6.90	7.20	7.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	-	0.65 BSC	-
L	0.55	0.75	0.95
L1	-	1.25 REF	-
L2	-	0.25 BSC	-
R	0.09	-	-
Θ	0°	4°	8°
N	20		

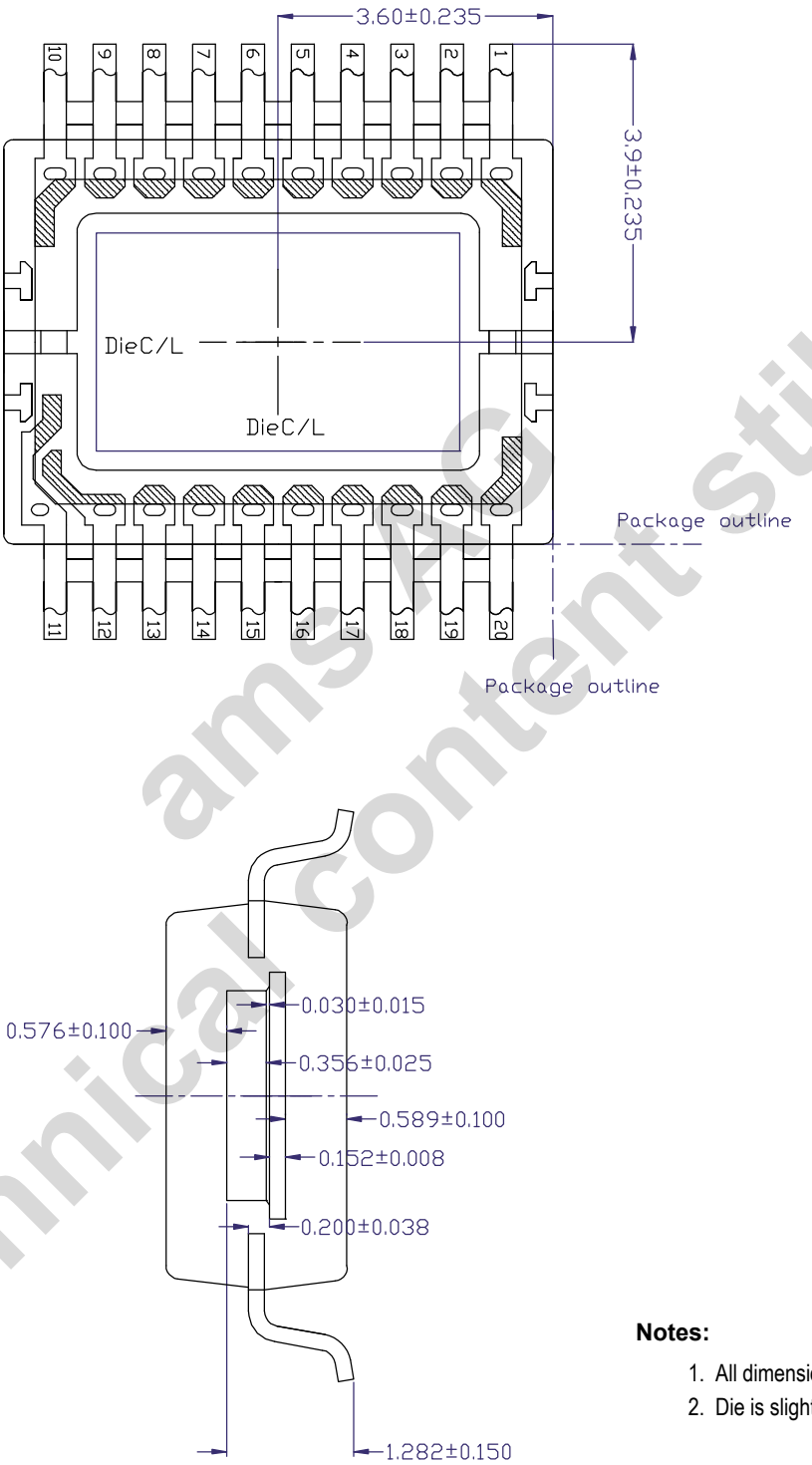
Notes:

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994.*
2. All dimensions are in millimeters. Angles are in degrees.

Marking: YYWWMZZ.

YY	WW	M	ZZ
Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Assembly traceability code

Figure 22. Vertical Cross Section of SSOP-20

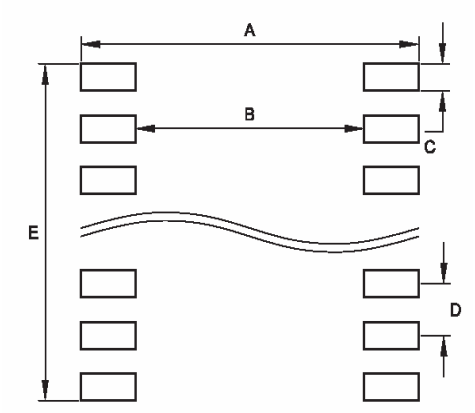


Notes:

1. All dimensions in mm.
2. Die is slightly off centered.

9.1 Recommended PCB Footprint

Figure 23. PCB Footprint



Recommended Footprint Data		
Symbol	**mm**	**inch**
A	9.02	0.355
B	6.16	0.242
C	0.46	0.018
D	0.65	0.025
E	6.31	0.248

Revision History

Revision	Date	Owner	Description
1.3	Jun 01, 2007	apg	Initial revision
1.5	May 21, 2008		Added Extended Operation Mode: Timing of Analog Readout (page 23)
1.6	Jul 07, 2008		Updated Connecting the AS5134 (page 7)
1.7	Jul 23, 2008		Updated Key Features (page 1), DC Characteristics of Digital Inputs and Outputs (page 5) Added Daisy Chain Mode (page 15)
1.8	Aug 12, 2008		Added Low Power Mode (page 26)
			Added topic on 'Accuracy'
			Added Package Drawings and Markings (page 27)
1.9	Mar 10, 2009	rfu	Updated Timing Characteristics (page 6), 2-or 3-wire Read-only Serial Bit Sequence (21bit read) (page 9), OTP Programming Connection (page 21), Programming Verification (page 22)
1.10	Apr 29, 2009	mub	Updated Electrical Characteristics (page 5)
1.11	Jun 24, 2009	jja	Maximum speed modified from 25.000 rpm to 140.000 rpm across the datasheet.
1.12	Sep 25, 2009		Maximum speed modified from 140.000 rpm to 82.000 rpm across the datasheet.
1.13	Jan 27, 2010	apg	Updated Package Drawings and Markings (page 27)
1.14	Mar 30, 2010	mub	Modified the following chapters: Key Features (page 1) Absolute Maximum Ratings (page 4) Electrical Characteristics (page 5) Timing Characteristics (page 6)
1.15	Jun 29, 2010	apg	Updated PWM period (page 5), PWM frequency (page 5)
2.0	May 23, 2011	mub	Updated Absolute Maximum Ratings, 1-Wire PWM Connection, Package Drawings and Markings
2.1	Nov 25, 2011	ekno	Updated PWM width (see Table 3), Programming Verification (page 22) and Vertical Cross Section of SSOP-20 (page 28)
2.2	Feb 29, 2012		Updated Electrical Characteristics (page 5), Vertical Cross Section of SSOP-20 (page 28), Rewrote Digital Readout Rate (page 26), Reducing Power Supply Peak Currents (page 26)
2.3	Apr 26, 2012	mub	Updated '2FH' to '3FH' in Lock Status Bit (page 24)

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 12.

Table 12. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS5134-ZSST, -ZSSM	360 Step Programmable High Speed Magnetic Rotary Encoder	Tape & Reel	20-pin SSOP

Note: All products are RoHS compliant and austriamicrosystems green.
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