AS5263

12-Bit Redundant Automotive Angle Position Sensor

General Description

The AS5263 is a contactless magnetic angle position sensor for accurate angular measurement over a full turn of 360º. A sub range can be programmed to achieve the best resolution for the application. The AS5263 includes two AS5163 in one MLF package.

It is a system-on-chip, combining integrated Hall elements, analog front-end, digital signal processing and best in class automotive protection features in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip, is required. The magnet may be placed above or below the IC.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 0.087º = 4096 positions per revolution. The start and end point of the sub segment will be programmed with a resolution of 14-bit (0.022º= 16384 steps per revolution). According to this resolution the adjustment of the application specific mechanical positions are possible. The angular output data is available over a 12-bit PWM signal or 12-bit ratiometric analog output.

An internal voltage regulator with over voltage protection and reverse polarity protection allows the AS5263 to operate in automotive application up to a voltage to 27V. Programmability over the output pin reduces the number of pins on the application connector. The AS5263 is the ideal solution for safety critical applications due to the redundant approach.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5263, 12-Bit Redundant Automotive Angle Position Sensor are listed below:

Figure 1:
Added Value of Using AS5263

Benefits	Features
• Great flexibility on angular excursion	• 360º contactless high resolution angular position sensing
• Simple programming	• User programmable start and end point of the application region • Saw tooth mode 1-4 slopes per revolution • Clamping levels • Transition point
• Failure diagnostics	• Broken GND and VDD detection for all external load cases
• Selectable output signal	• Analog output ratiometric to VDD or PWM-encoded digital output
• Ideal for applications in harsh environments due to contactless position sensing	• Wide temperature range: - 40°C to 150°C
• Stacked die redundant approach	• 32-pin MLF (7mm x 7mm) dimple package

Applications

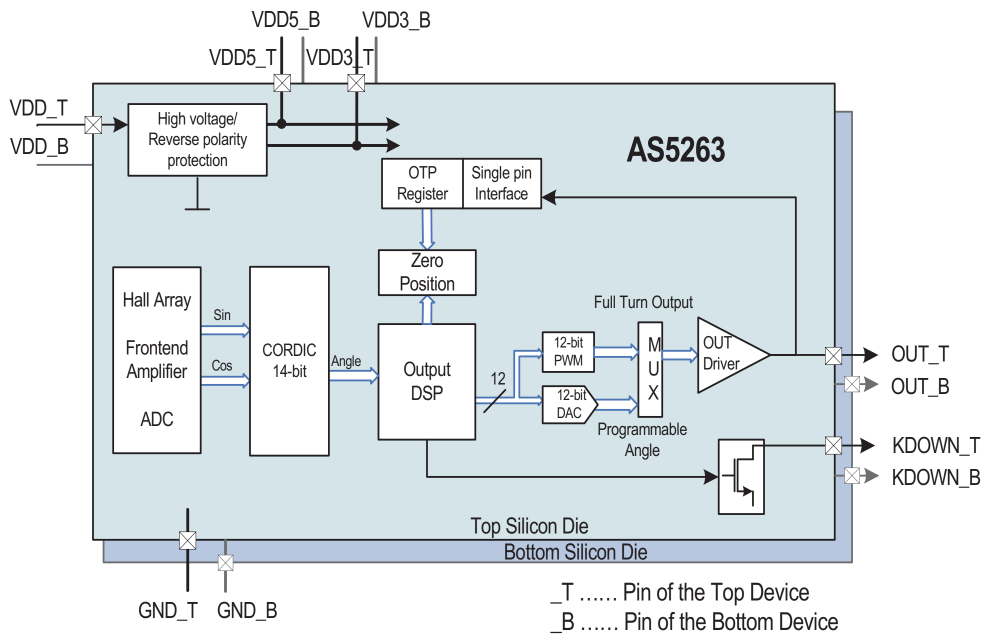
AS5263 is ideal for automotive applications like:

- Transmission gearbox position sensor
- Headlight position control
- Torque sensing
- Valve position sensing
- Pedal position sensing
- Throttle position sensing
- Non-contact potentiometers

Block Diagram

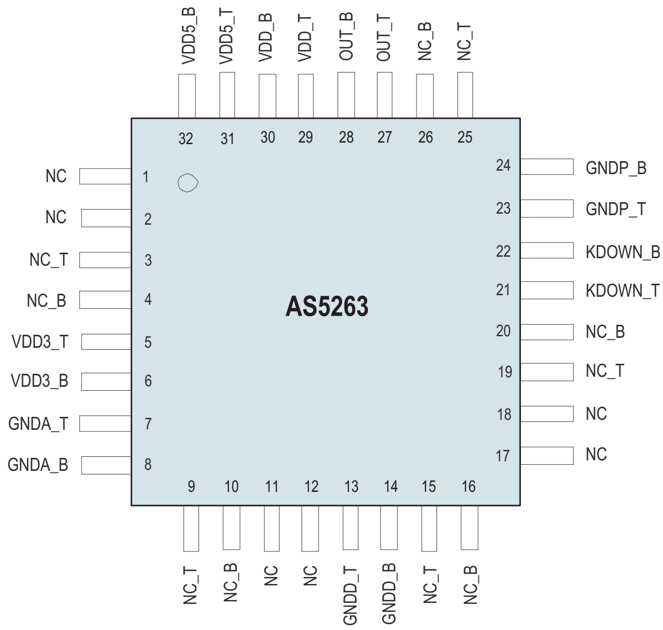
The functional blocks of this device are shown below:

Figure 2:
AS5263 Block Diagram



Pin Assignment

Figure 3:
Pin Diagram (Top View)



Pin Description

Figure 4 provides the description of each pin of the standard 32-pin MLF (7mm x 7mm) Dimple package. It is recommended to keep the electrical separation as well on the printed circuit board (PCB) in the application (see Figure 4).

Figure 4:
Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	NC	-	Not bonded
2	NC	-	Not bonded
3	NC_T	DIO/AIO multi purpose pin	**Test pin for fabrication.** Connected to top ground in the application.
4	NC_B		**Test pin for fabrication.** Connected to bottom ground in the application.

Pin Number	Pin Name	Pin Type	Description
5	VDD3_T	Supply pin	**3.45V- Regulator output, internally regulated from VDD5.** This pin needs an external ceramic capacitor of 2.2µF. Connect second terminal of capacitor to GND intended for the top die.
6	VDD3_B		**3.45V- Regulator output, internally regulated from VDD5.** This pin needs an external ceramic capacitor of 2.2µF. Connect second terminal of capacitor to GND intended for the bottom die.
7	GNDA_T		**Analog ground pin.** Connected to GND for the top die in the application.
8	GNDA_B		**Analog ground pin.** Connected to GND intended for the bottom die in the application.
9	NC_T	DIO/AIO multi purpose pin	**Test pin for fabrication.** Connected to GND intended for the top die in the application.
10	NC_B		**Test pin for fabrication.** Connected to GND intended for the bottom die in the application.
11	NC		**Test pin for fabrication.** Open in the application.
12	NC		**Test pin for fabrication.** Open in the application.
13	GNDD_T	Supply pin	**Digital ground pin.** Connected to GND intended for the top die in the application.
14	GNDD_B		**Digital ground pin.** Connected to GND intended for the bottom die in the application.
15	NC_T	DIO/AIO multi purpose pin	**Test pin for fabrication.** Connected to GND intended for the top die in the application.
16	NC_B		**Test pin for fabrication.** Connected to GND intended for the bottom die in the application.
17	NC	-	Not bonded
18	NC	-	Not bonded
19	NC_T	DIO/AIO multi purpose pin	**Test pin for fabrication.** Connected to GND intended for the top die in the application.
20	NC_B		**Test pin for fabrication.** Connected to GND intended for the bottom die in the application.
21	KDOWN_T	Digital output open drain	**Kick down functionality.** Open drain user pull-up resistor connected to the intended VDD top supply.
22	KDOWN_B		**Kick down functionality.** Open drain user pull-up resistor connected to the intended VDD bottom supply.

Pin Number	Pin Name	Pin Type	Description
23	GNDP_T	Supply pin	**Analog ground pin.** Connected to GND for the top die in the application.
24	GNDP_B		**Analog ground pin.** Connected to GND intended for the bottom die in the application.
25	NC_T	DIO/AIO multi purpose pin	**Test pin for fabrication.** Connected to GND intended for the top die in the application.
26	NC_B		**Test pin for fabrication.** Connected to GND intended for the bottom die in the application.
27	OUT_T		**Output pin.** Can be programmed as analog output or PWM output. Over this pin the programming of the top die is possible.
28	OUT_B		**Output pin.** Can be programmed as analog output or PWM output. Over this pin the programming of the bottom die is possible.
29	VDD_T	Supply pin	**Positive supply pin.** This pin is over voltage protected.
30	VDD_B		**Positive supply pin.** This pin is over voltage protected.
31	VDD5_T		**4.5V- Regulator output, internally regulated from VDD.** This pin needs an external ceramic capacitor of 2.2µF. Connect second terminal of capacitor to GND intended for the top die.
32	VDD5_B		**4.5V- Regulator output, internally regulated from VDD.** This pin needs an external ceramic capacitor of 2.2µF. Connect second terminal of capacitor to GND intended for the bottom die.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD}	DC supply voltage at pin VDD Overvoltage	-18	27	V	No operation
V_{OUT}	Output voltage OUT	-0.3	27	V	Permanent
V_{KDOWN}	Output voltage KDOWN	-0.3	27	V	
VDD3	DC supply voltage at pin VDD3	-0.3	5	V	
VDD5	DC supply voltage at pin VDD5	-0.3	7	V	
I_{scr}	Input current (latchup immunity)	-100	100	mA	JEDEC 78
Electrostatic Discharge					
ESD	Electrostatic discharge	±4		kV	MIL 883 E method 3015 This value is applicable to pins VDD, GND, OUT, and KDOWN. All other pins ±2 kV.
Temperature Ranges and Storage Conditions					
T_{Strg}	Storage temperature	-55	150	ºC	Min -67ºF; Max 302ºF
T_{Body}	Body temperature (lead-free package)		260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*. The lead finish for Pb-free leaded packages is matte tin (100% Sn).
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a maximum floor life time of 168h

Electrical Characteristics

Operating Conditions

In this specification, all the defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

T_{AMB} = -40°C to 150°C, V_{DD} = +4.5V to +5.5V, C_{LREG5} = 2.2µF, C_{LREG3} = 2.2µF, R_{PU} = 1KΩ, R_{PD} = 1KΩ to 5.6KΩ, (Analog only), C_{LOAD} =0 to 42nF, R_{PUKDWN} = 1KΩ to 5.6KΩ, C_{LOAD_KDWN} = 0 to 42nF, unless otherwise specified. A positive current is intended to flow into the pin.

Figure 6:
Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{AMB}	Ambient temperature	-40ºF to 302ºF	-40		150	ºC
I_{supp}	Supply current	Lowest magnetic input field			20	mA

Magnetic Input Specification

T_{AMB} = -40ºC to 150ºC, V_{DD} = 4.5V to 5.5V (5V operation), unless otherwise noted.

Two-Pole Cylindrical Diametrically Magnetized Source

Figure 7:
Magnetic Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Units
B_{pk}	Magnetic input field amplitude	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm	30		70	mT
B_{off}	Magnetic offset	Constant magnetic stray field			±10	mT
	Field non-linearity	Including offset gradient			5	%

Electrical System Specifications

T_{AMB} = -40ºC to 150ºC, V_{DD} = 4.5V to 5.5V (5V operation), Magnetic Input Specification, unless otherwise noted.

Figure 8:
Electrical System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution Analog and PWM Output	Angular operating range ≥ 90ºC			12	bit
INL_{opt}	Integral non-linearity (optimum) 360 degree full turn	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB}=25ºC			±0.5	deg
INL_{temp}	Integral non-linearity (optimum) 360 degree full turn	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB} = -40ºC to 150ºC			±0.9	deg
INL	Integral non-linearity 360 degree full turn	Best line fit = $(Err_{max} – Err_{min})/2$ Over displacement tolerance with 6mm diameter magnet, without calibration, T_{AMB} = -40ºC to 150ºC [1]		±1.4		deg
TN	Transition noise	1 sigma [2]		0.06		deg RMS
$VDD5_{LowTH}$	Undervoltage lower threshold	VDD5 = 5V	3.1	3.4	3.7	V
$VDD5_{HighTH}$	Undervoltage higher threshold		3.6	3.9	4.2	
t_{PwrUp}	Power-up time	Fast mode, times 2 in slow mode			10	ms
t_{delay}	System propagation delay absolute output: delay of ADC, DSP and absolute interface				100	µs

Note(s):

1. This parameter is a system parameter and is dependant on the selected magnet.
2. The noise performance is dependent on the programming of the output characteristic.
3. The INL performance is specified over the full turn of 360 degrees. An operation in an angle segment increases the accuracy.

Timing Characteristics

Figure 9:
Timing Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FRCOT	Internal Master Clock		4.05	4.5	4.95	MHz
TCLK	Interface Clock Time	TCLK = 1/ FRCOT	202	222.2	247	ns
TDETWD	WatchDog error detection time				12	ms

Detailed Description

The AS5263 is manufactured in a CMOS process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip.

The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5263 provides accurate high-resolution absolute angular position information. For this purpose, a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs that indicate movements of the used magnet towards or away from the device's surface.

A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information (see Figure 46).

The AS5263 senses the orientation of the magnetic field and calculates a 14-bit binary code. This code is mapped to a programmable output characteristic. The type of output is programmable and can be selected as PWM or analog output. This signal is available at the pins 27, 28 **(OUT_T, OUT_B)**.

The analog output and PWM output can be configured in many ways. The application angular region can be programmed in a user friendly way. The starting angle **T1** and the end point **T2** can be set and programmed according to the mechanical range of the application with a resolution of 14 bits. In addition, the **T1Y** and **T2Y** parameter can be set and programmed according to the application. The transition point 0 to 360 degree can be shifted using the break point parameter **BP**. This point is programmable with a high resolution of 14 bits of 360 degrees. The voltage for clamping level low **CLL** and clamping level high **CLH** can be programmed with a resolution of 7 bits. Both levels are individually adjustable.

These parameters are also used to adjust the PWM duty cycle.

The AS5263 also provides a compare function. The internal angular code is compared to a programmable level using hysteresis. The function is available over the output pins 21, 22 (**KDOWN_T, KDOWN_B**).

The output parameters can be programmed in an OTP register. No additional voltage is required to program the AS5263. The setting may be overwritten at any time and will be reset to default when power is cycled. To make the setting permanent, the OTP register must be programmed by using a lock bit. Else, the content could be frozen for ever.

The AS5263 is tolerant to magnet misalignment and unwanted external magnetic fields due to differential measurement technique and Hall sensor conditioning circuitry.

It is also tolerant to air gap and temperature variations due to Sin-/Cos- signal evaluation.

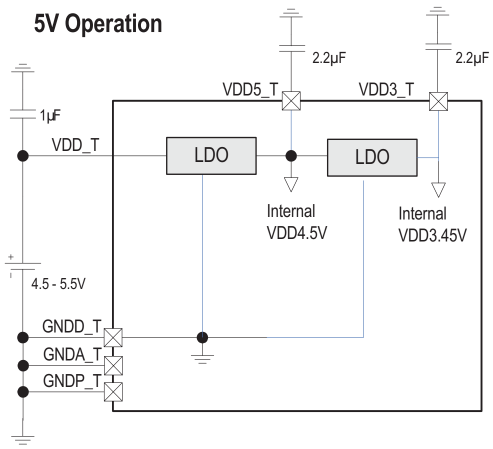
The AS5263 is tolerant to magnet misalignment and magnetic stray fields due to differential measurement technique and Hall sensor conditioning circuitry.

Operation

The AS5263 operates at 5V ±10%, using two internal Low-Dropout (LDO) voltage regulators. For operation, the 5V supply is connected to pin **VDD**. While **VDD3** and **VDD5** (LDO outputs) must be buffered by 2.2µF capacitors, the VDD requires a 1µF capacitor. All capacitors (low ESR ceramic) are supposed to be placed close to the supply pins (see Figure 10).

The **VDD3** and **VDD5** outputs are intended for internal use only. It must not be loaded with an external load.

Figure 10:
External Circuitry for the AS5263 (Figure Shows Only One Sensor Die)



Note(s):

1. The pins VDD3 and VDD5 must always be buffered by a capacitor. These pins must not be left floating, as this may cause unstable internal supply voltages, which may lead to larger output jitter of the measured angle
2. Only VDD is overvoltage protected up to 27V. In addition, the VDD has a reverse polarity protection.

VDD Voltage Monitor

VDD Overvoltage Management

If the voltage applied to the VDD pin exceeds the overvoltage upper threshold for longer than the detection time, then the device enters a low power mode reducing the power consumption. When the overvoltage event has passed and the voltage applied to the VDD pin falls below the overvoltage lower threshold for longer than the recovery time, then the device enters the normal mode.

VDD5 Undervoltage Management.

When the voltage applied to the VDD5 pin falls below the undervoltage lower threshold for longer than the VDD5_ detection time, then the device stops the clock of the digital part and the output drivers are turned OFF to reduce the power consumption. When the voltage applied to the VDD5 pin exceeds the VDD5 undervoltage upper threshold for longer than the VDD5_recovery time, then the clock is restarted and the output drivers are turned ON.

Analog Output

The reference voltage for the Digital-to-Analog converter (DAC) is taken internally from **VDD**. In this mode, the output voltage is ratiometric to the supply voltage.

Programming Parameters

The Analog output voltage modes are programmable by OTP. Depending on the application, the analog output can be adjusted. The user can program the following application specific parameters:

Figure 11:
Programming Parameters

T1	Mechanical angle start point
T2	Mechanical angle end point
T1Y	Voltage level at the T1 position
T2Y	Voltage level at the T2 position
CLL	Clamping level low
CLH	Clamping level high
BP	Break point (transition point 0 to 360 degree)

The above listed parameters are input parameters. Over the provided programming software and programmer, these parameters are converted and finally written into the AS5263 128-bit OTP memory. More details about the conversion can be found in the AN_AS5163+AS5263_V1.0 application note.

Application Specific Angular Range Programming

The application range can be selected by programming **T1** with a related **T1Y** and **T2** with a related **T2Y** into the AS5263. The internal gain factor is calculated automatically. The clamping levels **CLL** and **CLH** can be programmed independent from the **T1** and **T2** position and both levels can be separately adjusted.

Figure 12:
Programming of an Individual Application Range

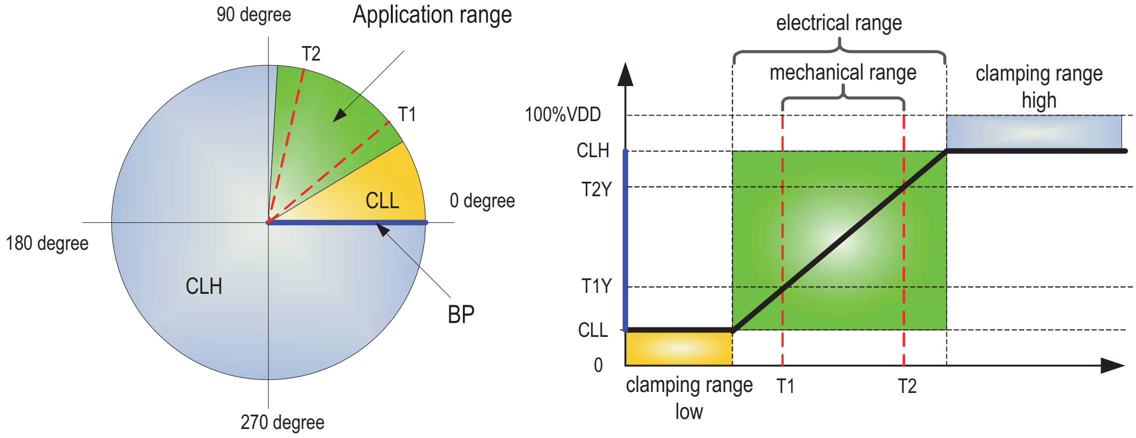
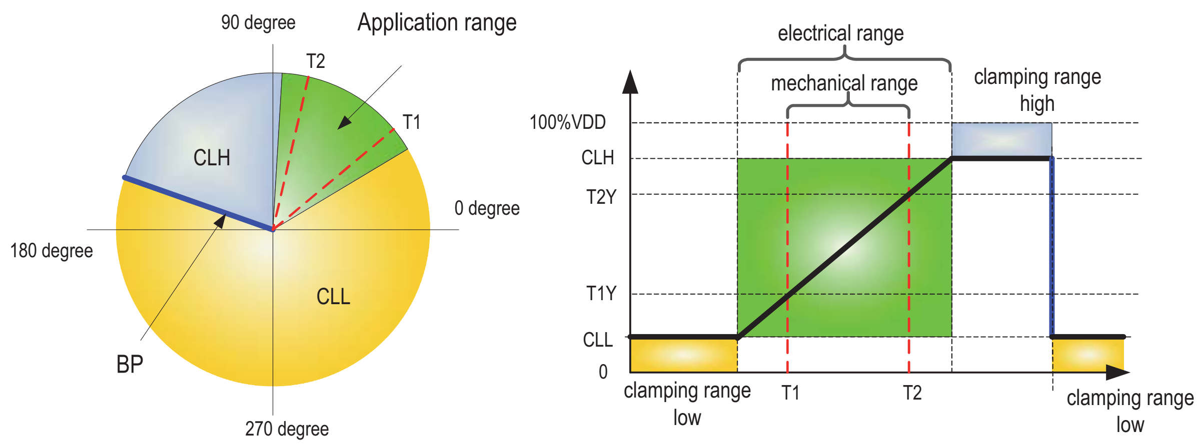


Figure 12 shows a simple example of the selection of the range. The mechanical starting point **T1** and the mechanical end point **T2** define the mechanical range. A sub range of the internal CORDIC output range is used and mapped to the needed output characteristic. The analog output signal has 12 bit, hence the level **T1Y** and **T2Y** can be adjusted with this resolution. As a result of this level and the calculated slope the clamping region low is defined. The break point **BP** defines the transition between **CLL** and **CLH**. In this example, the **BP** is set to 0 degree. The **BP** is also the end point of the clamping level high **CLH**. This range is defined by the level **CLH** and the calculated slope. Both clamping levels can be set independently form each other. The minimum application range is 12 degrees.

Application Specific Programming of the Break Point

The break point **BP** can be programmed as well with a resolution of 14 bits. This is important when the default transition point is inside the application range. In such a case, the default transition point must be shifted out of the application range. The parameter **BP** defines the new position. The function can be used also for an ON-OFF indication.

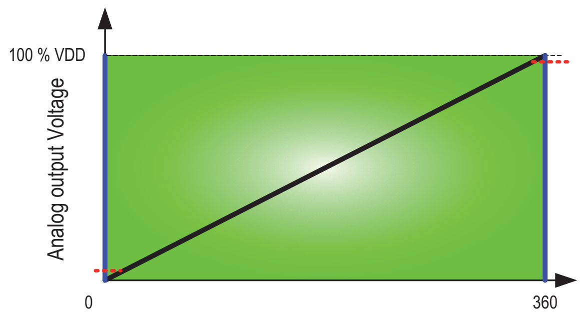
Figure 13:
Individual Programming of the Break Point BP



Full Scale Mode

The AS5263 can be programmed as well in the full scale mode. The **BP** parameter defines the position of the transition.

Figure 14:
Full Scale Mode

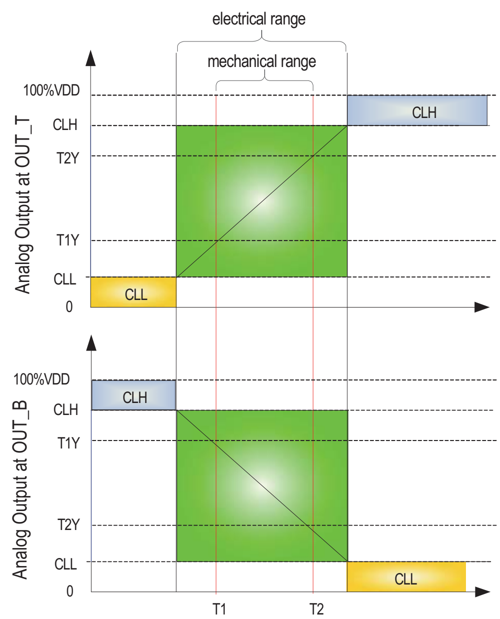


For simplification, Figure 14 describes a linear output voltage from rail to rail (0V to VDD) over the complete rotation range. In practice, this is not feasible due to saturation effects of the output stage transistors. The actual curve will be rounded towards the supply rails (as indicated Figure 14).

Inverted Dual Channel Output

The AS5263 can be programmed as described in Figure 15.

Figure 15:
Inverted Slope Output



Resolution of the Parameters

The programming parameters have a wide resolution of up to 14 bits.

Figure 16:
Resolution of the Programming Parameters

Symbol	Parameter	Resolution	Note
T1	Mechanical angle start point	14 bits	
T2	Mechanical angle stop point	14 bits	
T1Y	Mechanical start voltage level	12 bits	
T2Y	Mechanical stop voltage level	12 bits	
CLL	Clamping level low	7 bits	4096 LSBs is the maximum level
CLH	Clamping level high	7 bits	31 LSBs is the minimum level
BP	Break point	14 bits	

Figure 17:
Overview of the Angular Output Voltage

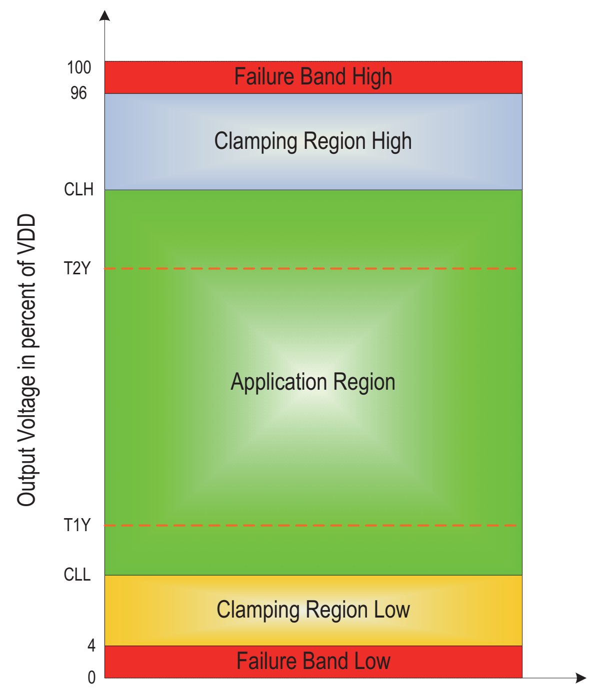


Figure 17 gives an overview of the different ranges. The failure bands are used to indicate a wrong operation of the AS5263. This can be caused due to a broken supply line. By using the specified load resistors, the output level will remain in these bands during a fail. It is recommended to set the clamping level **CLL** above the lower failure band and the clamping level **CLH** below the higher failure band.

Analog Output Diagnostic Mode

Due to the low pin count in the application, a wrong operation must be indicated by the output pin **OUT_T, OUT_B**. This could be realized using the failure bands. The failure band is defined with a fixed level. The failure band low is specified from 0% to 4% of the supply range. The failure band high is defined from 100% to 96%. Several failures can happen during operation. The output signal remains in these bands over the specified operating and load conditions. All the different failures can be grouped into the internal alarms (failures) and the application related failures.

$C_{LOAD} \leq 42nF$, $R_{PU}= 2k\Omega$ to $5.6k\Omega$

$R_{PD}= 2k\Omega$ to $5.6k\Omega$ load pull-up

Figure 18:
Different Failure Cases of AS5263

Type	Failure Mode	Symbol	Failure Band	Note
Internal alarms (failures)	Out of magnetic range (too less or too high magnetic input)	MAGRng	High/Low	Could be switched OFF by one OTP bit **EXT_RANGE**. Programmable by OTP bit **DIAG_HIGH**
	CORDIC overflow	COF	High/Low	Programmable by OTP bit **DIAG_HIGH**
	Offset compensation finished	OCF	High/Low	Programmable by OTP bit **DIAG_HIGH**
	Watchdog fail	WDF	High/Low	Programmable by OTP bit **DIAG_HIGH**
	Oscillator fail	OF	High/Low	Programmable by OTP bit **DIAG_HIGH**
Application related failures	Overvoltage condition	OV	High/Low	Dependant on the load resistor Pull up->failure band high Pull down->failure band low
	Broken VDD	BVDD		
	Broken VSS	BVSS		
	Short circuit output	SCO	High/Low	Switch OFF-> short circuit dependent

For efficient use of diagnostics, it is recommended to program to clamping levels **CLL** and **CLH**.

Analog Output Driver Parameters

The output stage is configured in a push-pull output. Therefore it is possible to sink and source currents.

$C_{LOAD} \leq 42nF$, R_{PU}= 2kΩ to 5.6kΩ

R_{PD}= 2kΩ to 5.6kΩ load pull-up

Figure 19:
General Parameters for the Output Driver

Symbol	Parameter	Min	Typ	Max	Unit	Note
IOUTSCL	Short circuit output current (low side driver)	8		32	mA	V_{OUT}=27V
IOUTSCH	Short circuit output current (high side driver)	-8		-32	mA	V_{OUT}=0V
TSCDET	Short circuit detection time	20		600	µs	Output stage turned OFF
TSCREC	Short circuit recovery time	2		20	ms	Output stage turned ON
ILEAKOUT	Output leakage current	-20		20	µA	V_{OUT}=VDD=5V
BGNDPU	Output voltage broken GND with pull-up	96		100	%VDD	R_{PU} = 2k to 5.6k
BGNDPD	Output voltage broken GND with pull-down	0		4	%VDD	R_{PD} = 2k to 5.6k
BVDDPU	Output voltage broken VDD with pull-up	96		100	%VDD	R_{PU} = 2k to 5.6k
BVDDPD	Output voltage broken VDD with pull-down	0		4	%VDD	R_{PD} = 2k to 5.6k

Note(s):

1. A Pull-Up/Down load is up to 1kΩ with increased diagnostic bands from 0%-6% and 94%-100%.

Figure 20:
Electrical Parameters for the Analog Output Stage

Symbol	Parameter	Min	Typ	Max	Units	Note
VOUT	Output voltage range	4		96	%VDD	
		6		94		Valid when 1k ≤ R_{LOAD} < 2k
VOUTINL	Output integral nonlinearity			10	LSB	
VOUTDNL	Output differential nonlinearity	-10		10	LSB	
VOUTOFF	Output offset	-50		50	mV	At 2048 LSB level
VOUTUD	Update rate of the output		100		µs	Info parameter
VOUTSTEP	Output step response			550	µs	Between 10% and 90%, R_{PD} =1kΩ, C_{LOAD}=1nF; V_{DD}=5V
VOUTDRIFT	Output voltage temperature drift	2		2	%	Of value at mid code
VOUTRATE	Output ratiometricity error	-1.5		1.5	%VDD	0.04*VDD ≤ VOUT ≤ 0.96*VDD
VOUTNOISE	Noise(1)			10	mVpp	1Hz to 30kHz; at 2048 LSB level

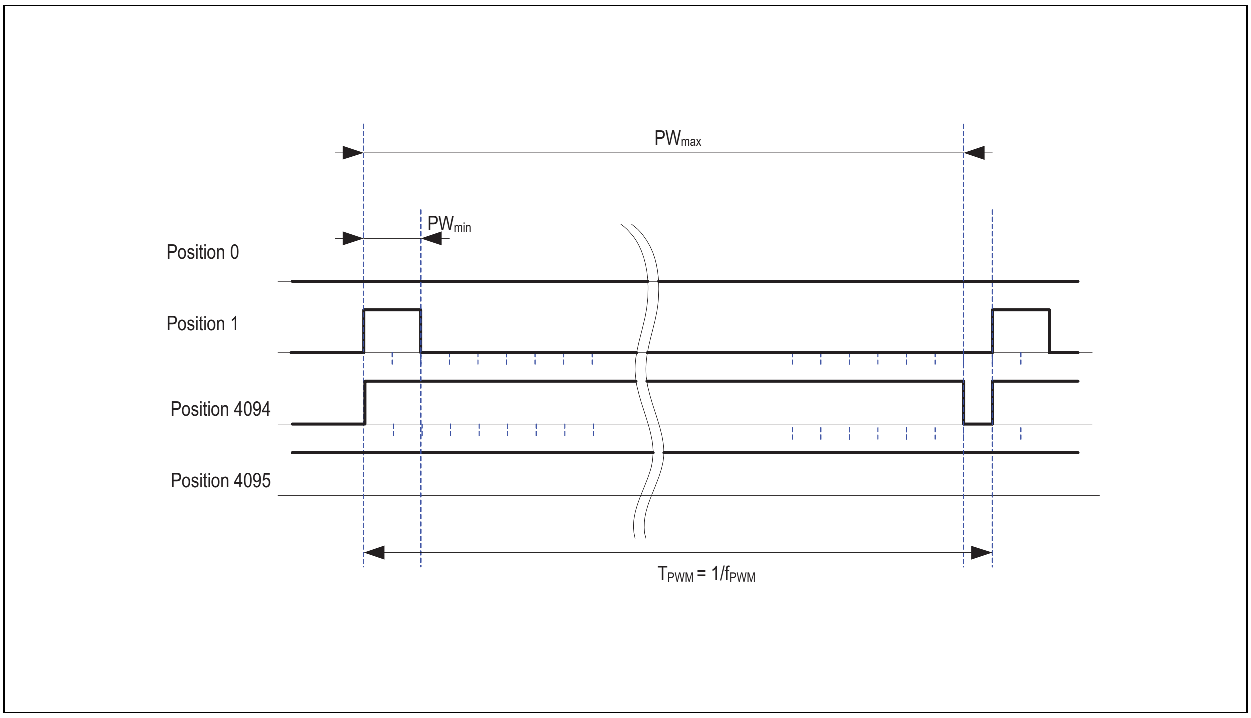
Note(s):

1. Not tested in production; characterization only.

Pulse Width Modulation (PWM) Output

The AS5263 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle. This output format is selectable over the OTP memory. If output pins **OUT_T, OUT_B** is configured as open drain configuration, then an external load resistor (pull up) is required. The PWM frequency is internally trimmed to an accuracy of ±10% over full temperature range. This tolerance can be cancelled by measuring the ratio between the ON and OFF state. In addition, the programmed clamping levels **CLL** and **CLH** will also adjust the PWM signal characteristic.

Figure 21:
PWM Output Signal



The PWM frequency can be programmed by the OTP bits **PWM_ frequency (1:0)**. Therefore, four different frequencies are possible.

Figure 22:
PWM Signal Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{PWM1}	PWM frequency1	123.60	137.33	151.06	Hz	PWM_frequency (1:0) = "11"
f_{PWM2}	PWM frequency2	247.19	274.66	302.13	Hz	PWM_frequency (1:0) = "10"
f_{PWM3}	PWM frequency3	494.39	549.32	604.25	Hz	PWM_frequency (1:0) = "01"
f_{PWM4}	PWM frequency4	988.77	1098.63	1208.50	Hz	PWM_frequency (1:0) = "00"
PW_{MIN}	MIN pulse width		(1+1)*1/ f_{PWM}		µs	
PW_{MAX}	MAX pulse width		(1+4094)*1/ f_{PWM}		ms	

Taking into consideration the AC characteristic of the PWM output including load, it is recommended to use the clamping function. The recommended range is 0% to 4% and 96% to 100%.

Figure 23:
Electrical Parameters for the PWM Output Mode

Symbol	Parameter	Min	Typ	Max	Units	Note
PWMVOL	Output voltage low	0		0.4	V	I_{OUT}=8mA
ILEAK	Output leakage	-20		20	µA	V_{OUT}=V_{DD}=5V
PWMDC	PWM duty cycle range	4		96	%	
PWMSRF	PWM slew rate	1	2	4	V/µs	Between 75% and 25% R_{PU}/R_{PD} = 1kΩ, C_{LOAD} = 1nF, VDD = 5V

Kick Down Function

The AS5263 provides a special compare function. This function is implemented using a programmable angle value with a programmable hysteresis. It will be indicated over the open drain output pin **KDOWN_T, KDOWN_B**. If the actual angle is above the programmable value plus the hysteresis, the output is switched to low. The output will remain at low level until the value KD is reached in the reverse direction.

Figure 24:
Kick Down Hysteresis Implementation

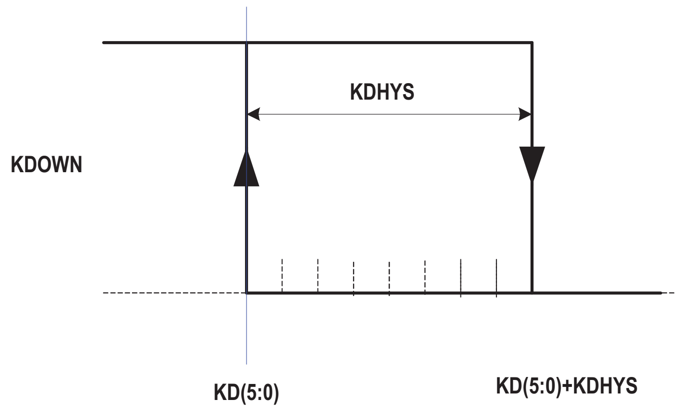


Figure 25:
Programming Parameters for the Kick Down Function

Symbol	Parameter	Resolution	Note
KD	Kick Down Angle	6 bits	
KDHYS	Kick Down Hysteresis	2 bits	KDHYS (1:0) = "00" -> 8 LSB hysteresis KDHYS (1:0) = "01" ->16 LSB hysteresis KDHYS (1:0) = "10" -> 32 LSB hysteresis KDHYS (1:0) = "11" -> 64 LSB hysteresis

Pull-up resistance 1k to 5.6K to VDD

C_{LOAD} max 42nF

Figure 26:
Electrical Parameters of the KDOWN Output

Symbol	Parameter	Min	Typ	Max	Unit	Note
IKDSC	Short circuit output current (low side driver)	6		24	mA	$V_{KDOWN} = 27V$
TSCDET	Short circuit detection time	20		600	µs	Output stage turned OFF
TSCREC	Short circuit recovery time	2		20	ms	Output stage turned ON
KDVOL	Output voltage low	0		1.1	V	$I_{KDOWN} = 6mA$
KDILEAK	Output leakage	-20		20	µA	$V_{KDOWN} = 5V$
KDSRF	KDOWN slew rate (falling edge)	1	2	4	V/µs	Between 75% and 25%, $R_{PUKDWN} = 1k\Omega$, $C_{LOAD\_KDWN} = 1nF$, VDD = 5V

Application Information

Programming the AS5263

The AS5263 programming is a one-time-programming (OTP) method, based on polysilicon fuses. The advantage of this method is that no additional programming voltage is needed. The internal LDO provides the current for programming.

The OTP consists of 128 bits, wherein several bits are available for user programming. In addition, factory settings are stored in the OTP memory. Both regions are independently lockable by built-in lock bits.

A single OTP cell can be programmed only once. By default, each cell is "0"; a programmed cell will contain a "1". While it is not possible to reset a programmed bit from "1" to "0", multiple OTP writes are possible, as long as only unprogrammed "0"-bits are programmed to "1".

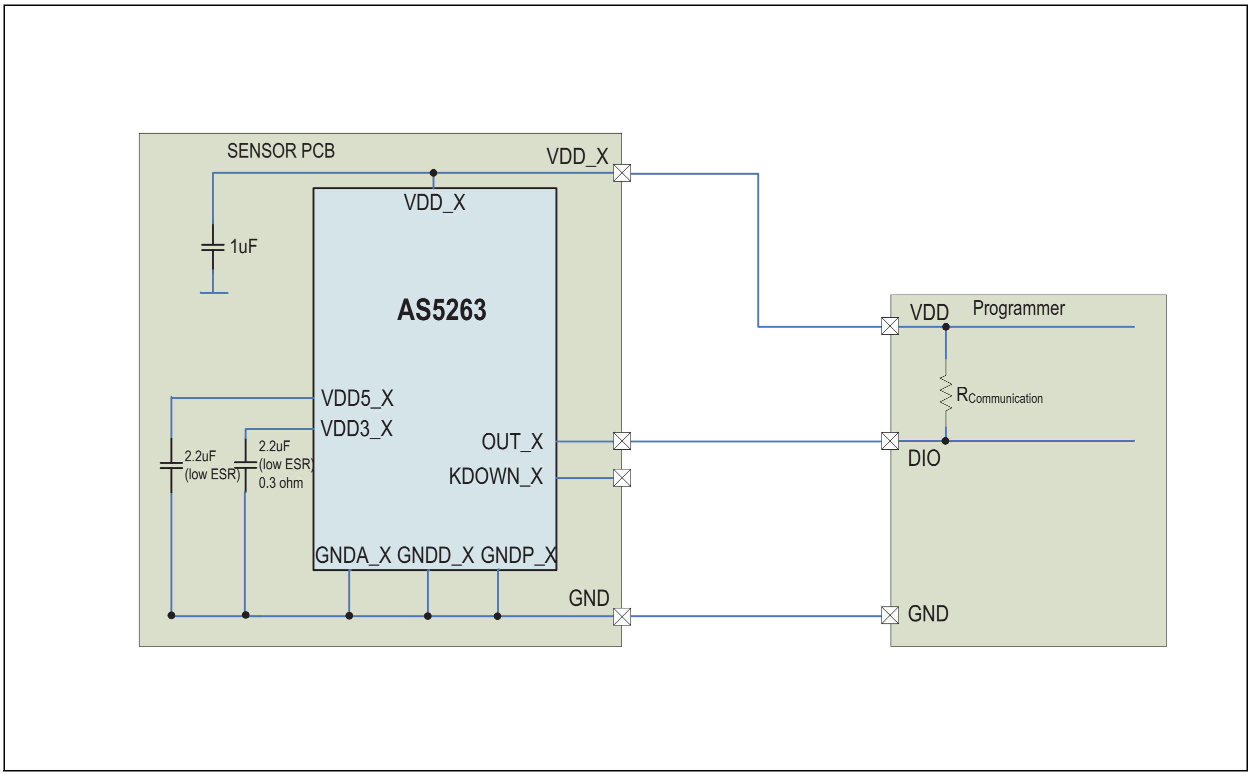
Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command. This is possible only if the user lock bit is not programmed.

Due to the programming over the output pin, the device will initially start in the communication mode. In this mode, the digital angle value can be read with a specific protocol format. It is a bidirectional communication possible. Parameters can be written into the device. A programming of the device is triggered by a specific command. With another command (pass2funcion), the device can be switched into operation mode (analog or PWM output). In case of a programmed user lock bit, the AS5263 automatically starts up in the functional operation mode. No communication of the specific protocol is possible after this.

Hardware Setup

The pin OUT and the supply connection are required for OTP memory access. Without the programmed **Mem_Lock_USER** OTP bit, the device will start up in the communication mode and will remain into an IDLE operation mode. The pull up resistor $R_{Communication}$ is required during startup. Figure 2 shows the configuration of an AS5263.

Figure 27:
Programming Schematic of the AS5263



Protocol Timing and Commands of Single Pin Interface

During the communication mode, the output level is defined by the external pull up resistor $R_{Communication}$. The output driver of the device is in tristate. The bit coding (see Figure 35) has been chosen in order to allow the continuous synchronization during the communication, which can be required due to the tolerance of the internal clock frequency. Figure 35 shows how the different logic states '0' and '1' are defined. The period of the clock T_{CLK} is defined with 222.2 ns.

The voltage levels V_H and V_L are CMOS typical.

Each frame is composed by 20 bits. The 4 MSB (CMD) of the frame specifies the type of command that is passed to the AS5263. The 16 data bits contain the communication data. There will be no operation when the 'not specified' CMD is used. The sequence is oriented in such a way that the LSB of the data is followed by the command. The number of frames vary depending on the command. The single pin programming interface block of the AS5263 can operate in slave communication or master communication mode. In the slave communication mode, the AS5263 receives the data organized in frames. The programming tool is the driver of the single communication line and can pull down the level.
In case of the master communication mode, the AS5263 transmits data in the frame format. The single communication line can be pulled down by the AS5263.

Figure 28:
Bit Coding of the Single Pin Programming Interface

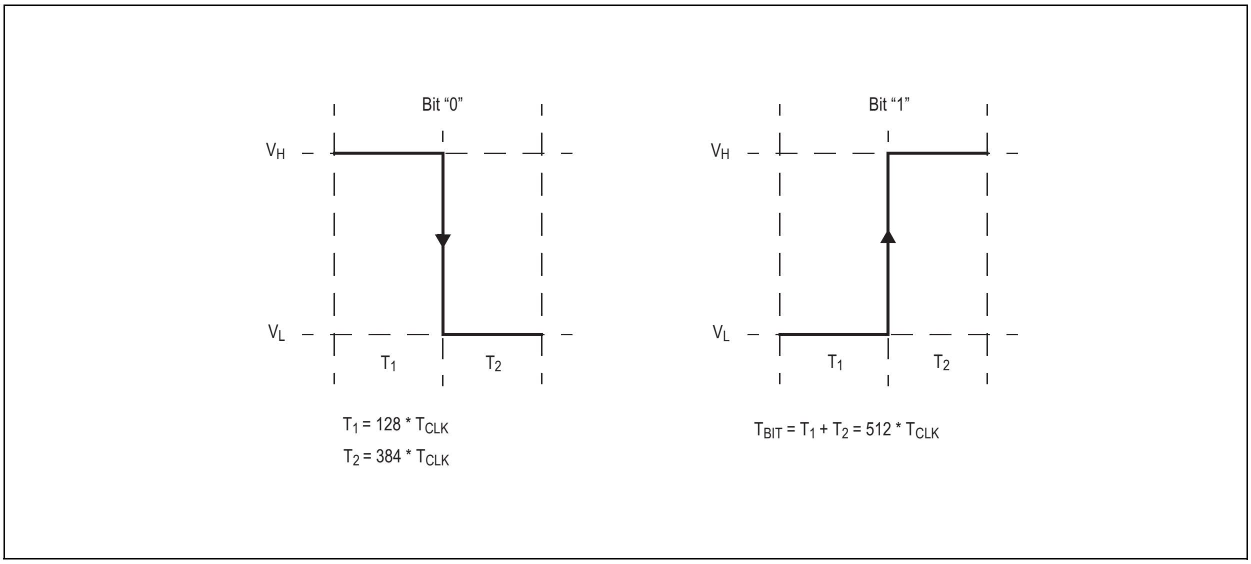


Figure 29:
Protocol Definition

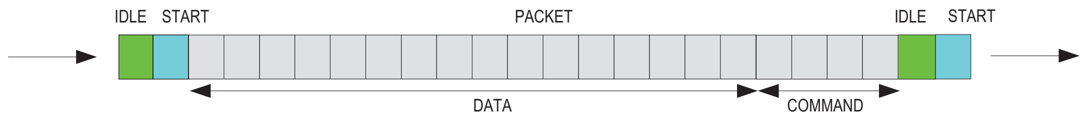


Figure 30:
OTP Commands and Communication Interface Modes

Possible Interface Commands	Description	AS5263 Communication Mode	Command CMD	Number of Frames
UNBLOCK	Resets the interface	SLAVE	0x0	1
WRITE128	Writes 128 bits (user + factory settings) into the device	SLAVE	0x9 (0x1)	8
READ128	Reads 128 bits (user + factory settings) from the device	SLAVE and MASTER	0xA	9
UPLOAD	Transfers the register content into the OTP memory	SLAVE	0x6	1
DOWNLOAD	Transfers the OTP content to the register content	SLAVE	0x5	1
FUSE	Command for permanent programming	SLAVE	0x4	1
PASS2FUNC	Change operation mode from communication to operation	SLAVE	0x7	1
READ	Read related to address the user data	SLAVE and MASTER	0xB	2
WRITE	Write related to address the user data	SLAVE	0xC	1

Note(s):

1. Other commands are reserved and shall not be used.

When single pin programming interface bus is in high impedance state, the logical level of the bus is held by the pull up resistor $R_{Communication}$. Each communication begins by a condition of the bus level which is called START. This is done by forcing the bus in logical low level (done by the programmer or AS5263 depending on the communication mode). Afterwards the bit information of the command is transmitted as shown in Figure 31.

Figure 31:
Bus Timing for the WRITE128 Command

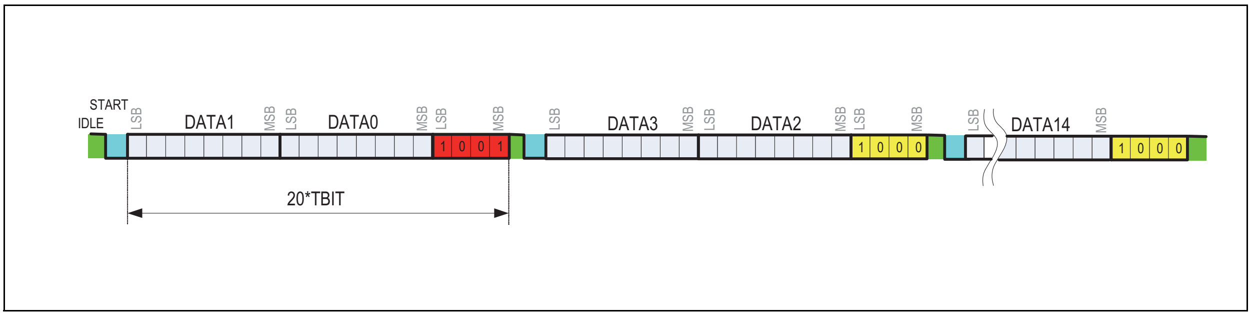
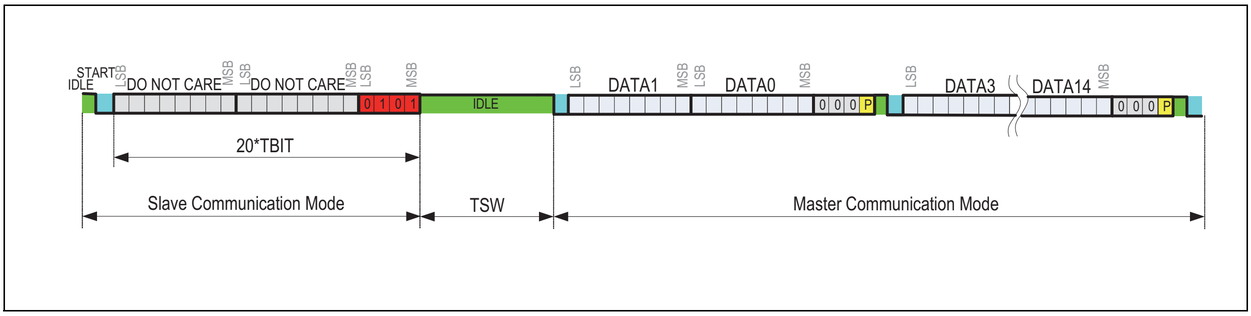
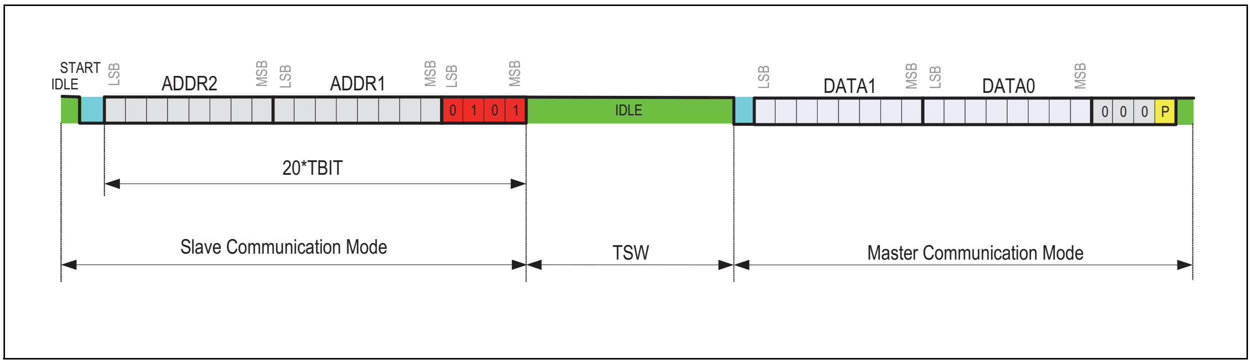


Figure 32:
Bus Timing for the READ128 Command



In case of READ or READ128 command (seeFigure 32) the idle phase between the command and the answer is 10 TBIT (TSW).

Figure 33:
Bus Timing for the READ Commands



In case of a WRITE command, the device stays in slave communication mode and will not switch to master communication mode.

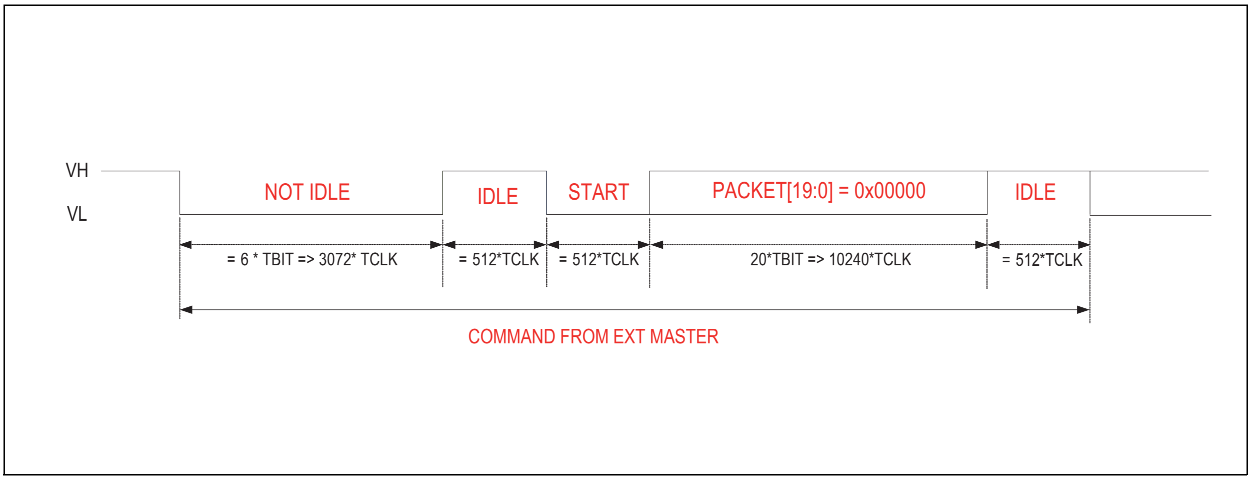
When using other commands like DOWNLOAD, UPLOAD, etc. instead of READ or WRITE, it does not matter what is written in the address fields (ADDR1, ADDR2).

UNBLOCK

The Unblock command can be used to reset only the one-wire interface of the AS5263 in order to recover the possibility to communicate again without the need of a POR after a stacking event due to noise on the bus line or misalignment with the AS5263 protocol.

The command is composed by a not idle phase of at least 6 TBIT followed by a packet with all 20 bits at zero (see Figure 34).

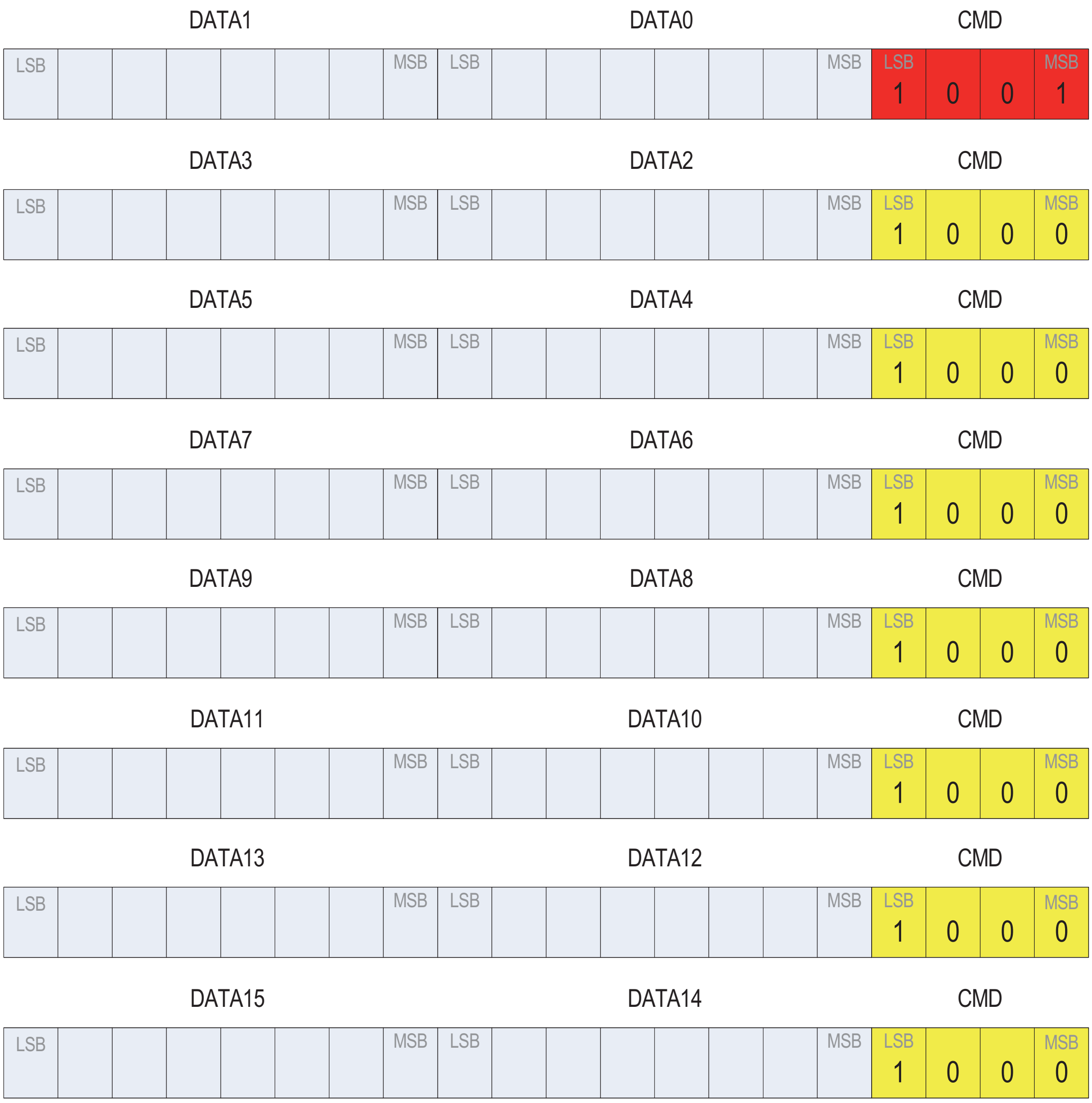
Figure 34:
Unblock Sequence



WRITE128

Figure 35 illustrates the format of the frame and the command.

Figure 35:
Frame Organization of the WRITE128 Command



The command contains 8 frames. With this command, the AS5263 receives only frames. This command will transfer the data in the special function registers (SFRs) of the device. The data is not permanent programmed using this command.

Figure 43 describe the organization of the OTP data bits.

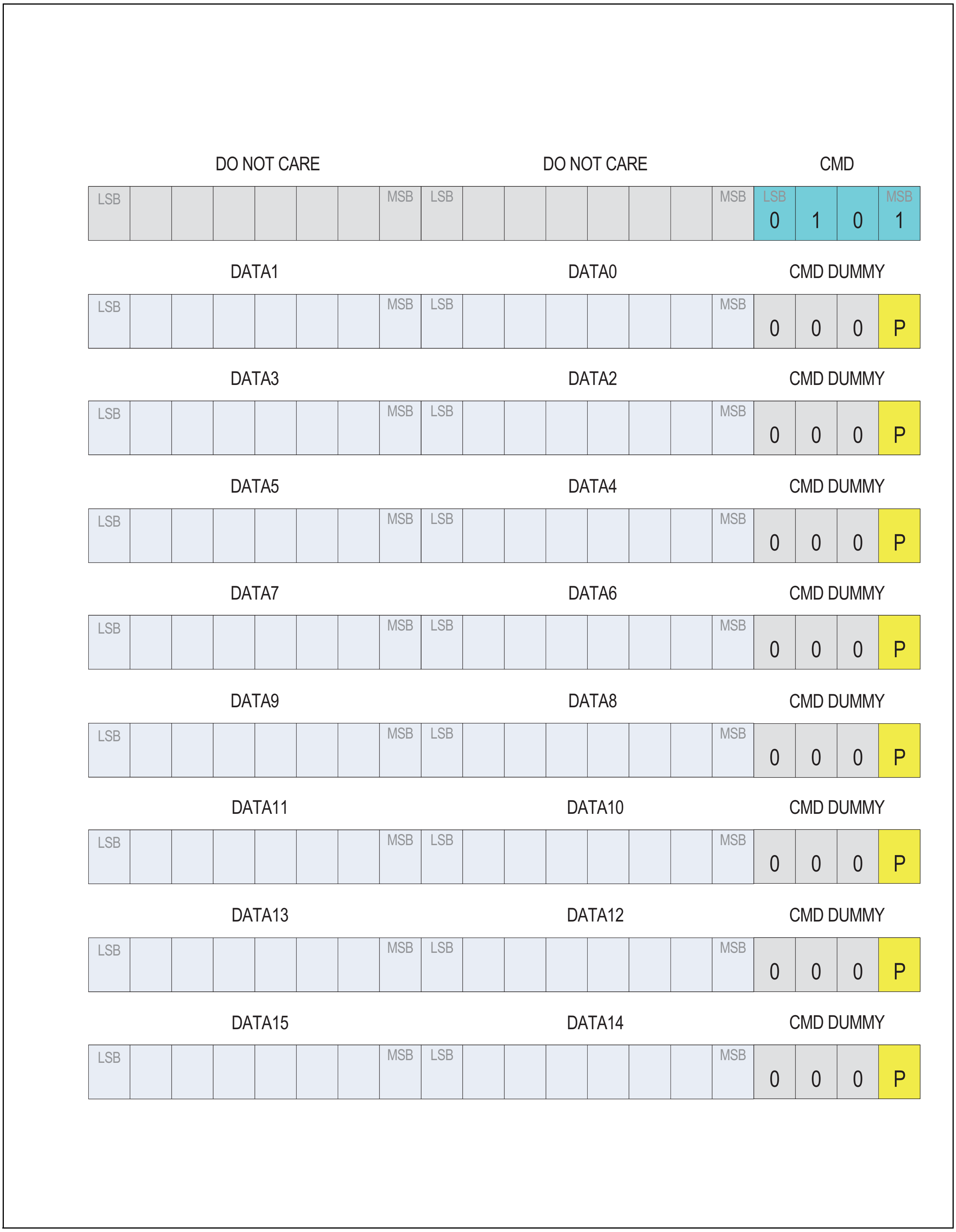
The access is performed with CMD field set to 0x9. The next 7 frames with CMD field set to 0x1. The 2 bytes of the first command will be written at address 0 and 1 of the SFRs; the 2 bytes of the second command will be written at address 2 and 3; and so on, in order to cover all the 16 bytes of the 128 SFRs.

Note(s): It is important to always complete the command. All 8 frames are needed. In case of a wrong command or a communication error, a power-on reset must be performed. The device will be delivered with the programmed **Mem_Lock_AMS** OTP bit. This bit locks the content of the factory settings. It is impossible to overwrite this particular region. The written information will be ignored.

READ128

Figure 36 illustrates the format of the frame and the command.

Figure 36:
Frame Organization of the READ128 Command



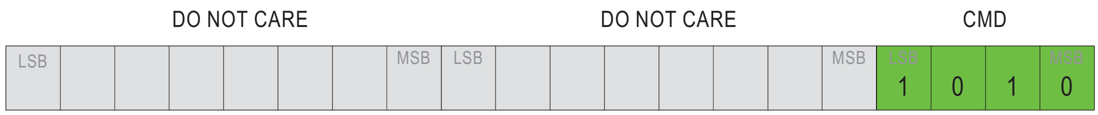
The command is composed by a first frame transmitted to the AS5263. The device is in slave communication mode. The device remains for the time T_{SWITCH} in IDLE mode before changing into the master communication mode. The AS5263 starts to send 8 frames. This command will read the SFRs. The numbering of the data bytes correlates with the address of the related SFR.

An even parity bit is used to guarantee a correct data transmission. Each parity (P) is related to the frame data content of the 16 bit word. The MSB of the CMD dummy (P) is reserved for the parity information.

DOWNLOAD

Figure 37 shows the format of the frame.

Figure 37:
Frame Organization of the DOWNLOAD Command



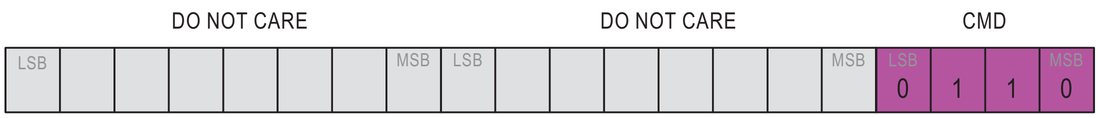
The command consists of one frame received by the AS5263 (slave communication mode). The OTP cell fuse content will be downloaded into the SFRs.

The access is performed with CMD field set to 0x5.

UPLOAD

Figure 38 shows the format of the frame.

Figure 38:
Frame Organization of the UPLOAD Command



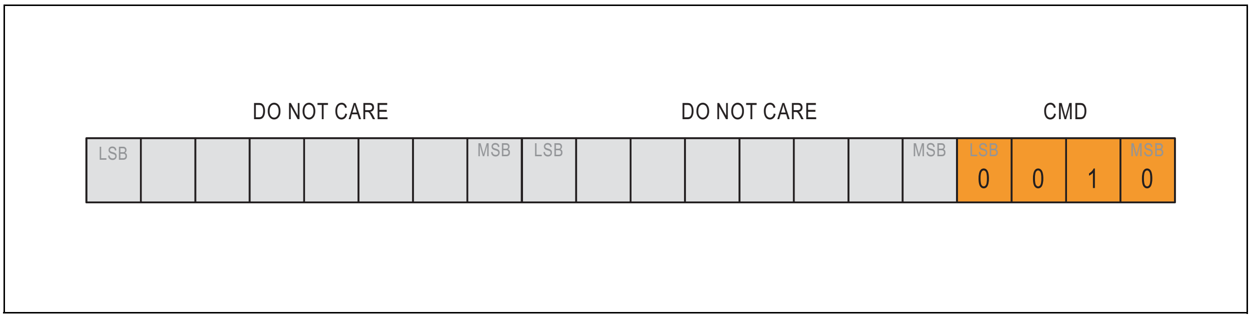
The command consists of one frame received by the AS5263 (slave communication mode) and transfers the data from the SFRs into the OTP fuse cells. The OTP fuses are not permanent programmed using this command.

The access is performed with CMD field set to 0x6.

FUSE

Figure 39 shows the format of the frame.

Figure 39:
Frame Organization of the FUSE Command



The command consists of one frame received by the AS5263 (slave communication mode) and it is giving the trigger to permanent program the non volatile fuse elements.

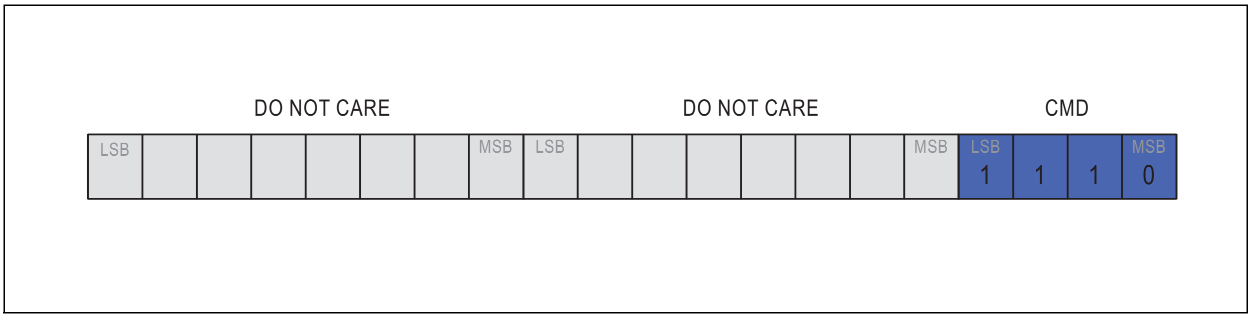
The access is performed with CMD field set to 0x4.

Note(s): After this command, the device automatically starts to program the built-in programming procedure. It is not allowed to send other commands during this programming time. This time is specified to 4ms after the last CMD bit.

PASS2FUNC

Figure 40 shows the format of the frame.

Figure 40:
Frame Organization of the PASS2FUNC Command



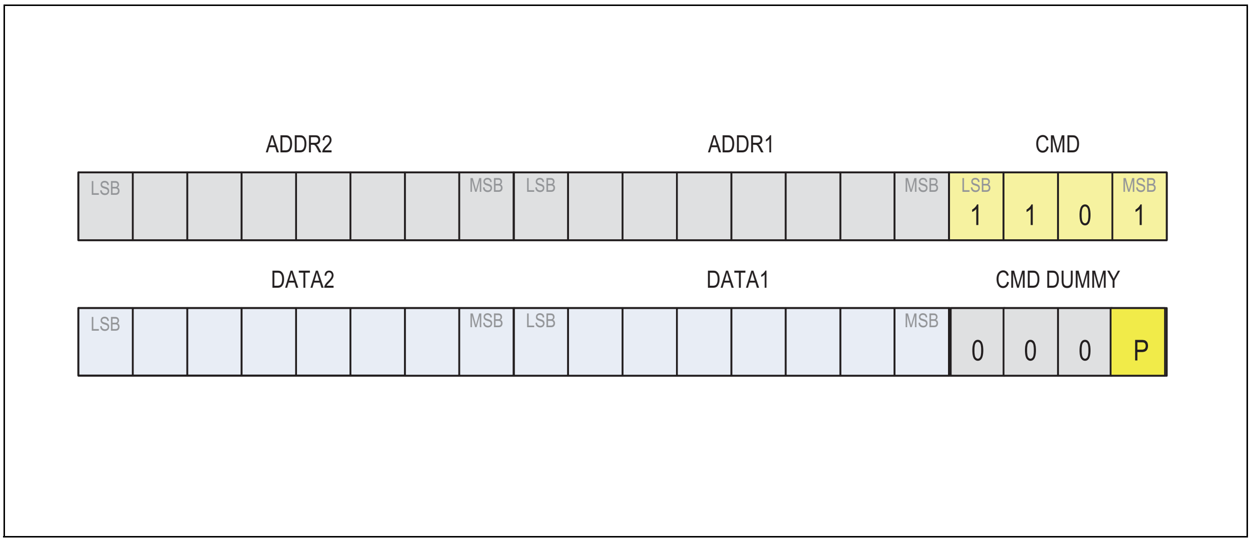
The command consists of one frame received by the AS5263 (slave communication mode). This command stops the communication receiving mode, releases the reset of the DSP of the AS5263 device and starts to work in functional mode with the values of the SFR currently written.

The access is performed with CMD field set to 0x7.

READ

Figure 41 shows the format of the frame.

Figure 41:
Frame Organization of the READ Command



The command is composed by a first frame sent to the AS5263. The device is in slave communication mode. The device remains for the time T_{SWITCH} in IDLE mode before changing into the master communication mode. The AS5263 starts to send the second frame transmitted by the AS5263.

The access is performed with CMD field set to 0xB.

When the AS5263 receives the first frame, it sends a frame with data value of the address specified in the field of the first frame.

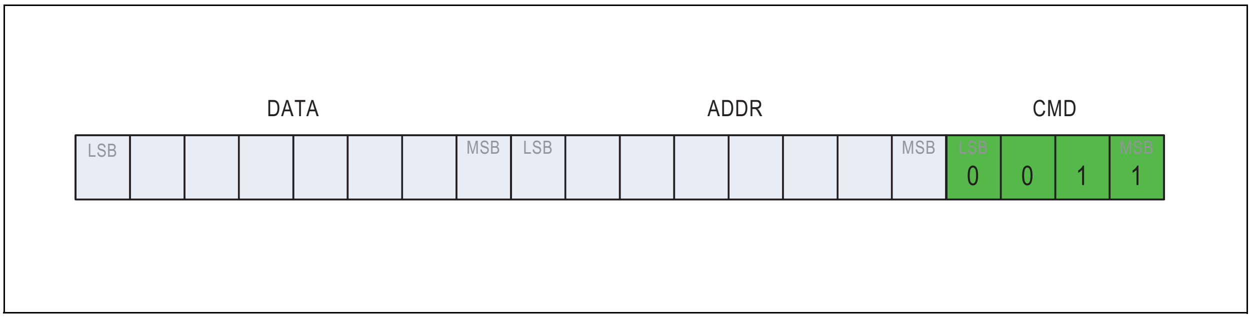
Figure 45 shows the possible readable data information for the AS5263 device.

An even parity bit is used to guarantee a correct data transmission. The parity bit (P) is generated by the 16 data bits. The MSB of the CMD dummy (P) is reserved for the parity information.

WRITE

Figure 42 shows the format of the frame.

Figure 42:
Frame Organization of the WRITE Command



The command consists of one frame received by the AS5263 (slave communication mode). The data byte will be written to the address. The access is performed with CMD field set to 0xC.

Figure 45 shows the possible write data information for the AS5263 device.

Note(s): It is not recommended to access OTP memory addresses using this command.

OTP Programming Data

Figure 43:
OTP Data Organization

Data Byte	Bit Number	Symbol	Default	Description	
DATA15 (0x0F)	0	AMS_Test	FS	**ams** Test Area	Factory Settings
	1	AMS_Test	FS		
	2	AMS_Test	FS		
	3	AMS_Test	FS		
	4	AMS_Test	FS		
	5	AMS_Test	FS		
	6	AMS_Test	FS		
	7	AMS_Test	FS		
DATA14 (0x0E)	0	AMS_Test	FS		
	1	AMS_Test	FS		
	2	AMS_Test	FS		
	3	AMS_Test	FS		
	4	ChipID<0>	FS	Chip ID	
	5	ChipID<1>	FS		
	6	ChipID<2>	FS		
	7	ChipID<3>	FS		
DATA13 (0x0D)	0	ChipID<4>	FS		
	1	ChipID<5>	FS		
	2	ChipID<6>	FS		
	3	ChipID<7>	FS		

Data Byte	Bit Number	Symbol	Default	Description	
DATA13 (0x0D)	4	ChipID<8>	FS	Chip ID	Factory Settings
	5	ChipID<9>	FS		
	6	ChipID<10>	FS		
	7	ChipID<11>	FS		
DATA12 (0x0C)	0	ChipID<12>	FS		
	1	ChipID<13>	FS		
	2	ChipID<14>	FS		
	3	ChipID<15>	FS		
	4	ChipID<16>	FS		
	5	ChipID<17>	FS		
	6	ChipID<18>	FS		
	7	ChipID<19>	FS		
DATA11 (0x0B)	0	ChipID<20>	FS		
	1	MemLock_AMS	1	Lock of the Factory Setting Area	
	2	KD<0>	0	Kick Down Threshold	Customer Settings
	3	KD<1>	0		
	4	KD<2>	0		
	5	KD<3>	0		
	6	KD<4>	0		
	7	KD<5>	0		
DATA10 (0x0A)	0	ClampLow<0>	0	Clamping Level Low	
	1	ClampLow<1>	0		
	2	ClampLow<2>	0		
	3	ClampLow<3>	0		
	4	ClampLow<4>	0		
	5	ClampLow<5>	0		
	6	ClampLow<6>	0		
	7	DAC_MODE	0	DAC12/DAC10 Mode	

Data Byte	Bit Number	Symbol	Default	Description	
DATA9 (0x09)	0	ClampHi<0>	0	Clamping Level High	Customer Settings
	1	ClampHi<1>	0		
	2	ClampHi<2>	0		
	3	ClampHi<3>	0		
	4	ClampHi<4>	0		
	5	ClampHi<5>	0		
	6	ClampHi<6>	0		
	7	DIAG_HIGH	0	Diagnostic Mode, default=0 for Failure Band Low	
DATA8 (0x08)	0	OffsetIn<0>	0	Offset	
	1	OffsetIn<1>	0		
	2	OffsetIn<2>	0		
	3	OffsetIn<3>	0		
	4	OffsetIn<4>	0		
	5	OffsetIn<5>	0		
	6	OffsetIn<6>	0		
	7	OffsetIn<7>	0		
DATA7 (0x07)	0	OffsetIn<8>	0		
	1	OffsetIn<9>	0		
	2	OffsetIn<10>	0		
	3	OffsetIn<11>	0		
	4	OffsetIn<12>	0		
	5	OffsetIn<13>	0		
	6	OP_Mode<0>	0	Selection of Analog='00' or PWM Mode='01'	
	7	OP_Mode<1>	0		

Data Byte	Bit Number	Symbol	Default	Description	
DATA6 (0x06)	0	OffsetOut<0>	0	Output Offset	Customer Settings
	1	OffsetOut<1>	0		
	2	OffsetOut<2>	0		
	3	OffsetOut<3>	0		
	4	OffsetOut<4>	0		
	5	OffsetOut<5>	0		
	6	OffsetOut<6>	0		
	7	OffsetOut<7>	0		
DATA5 (0x05)	0	OffsetOut<8>	0		
	1	OffsetOut<9>	0		
	2	OffsetOut<10>	0		
	3	OffsetOut<11>	0		
	4	KDHYS<0>	0	Kick Down Hysteresis	
	5	KDHYS<1>	0		
	6	PWM Frequency<0>	0	Select the PWM Frequency (4 frequencies)	
	7	PWM Frequency<1>	0		
DATA4 (0x04)	0	BP<0>	0	Break Point	
	1	BP<1>	0		
	2	BP<2>	0		
	3	BP<3>	0		
	4	BP<4>	0		
	5	BP<5>	0		
	6	BP<6>	0		
	7	BP<7>	0		

Data Byte	Bit Number	Symbol	Default	Description	
DATA3 (0x03)	0	BP<8>	0	Break Point	Customer Settings
	1	BP<9>	0		
	2	BP<10>	0		
	3	BP<11>	0		
	4	BP<12>	0		
	5	BP<13>	0		
	6	FAST_SLOW	0	Output Data Rate	
	7	EXT_RANGE	0	Enables a Wider z-Range	
DATA2 (0x02)	0	Gain<0>	0	Gain	
	1	Gain<1>	0		
	2	Gain<2>	0		
	3	Gain<3>	0		
	4	Gain<4>	0		
	5	Gain<5>	0		
	6	Gain<6>	0		
	7	Gain<7>	0		
DATA1 (0x01)	0	Gain<8>	0		
	1	Gain<9>	0		
	2	Gain<10>	0		
	3	Gain<11>	0		
	4	Gain<12>	0		
	5	Gain<13>	0		
	6	Invert_Slope	0	Clockwise /Counterclockwise Rotation	
	7	Lock_OTPCUST	0	Customer Memory Lock	

Data Byte	Bit Number	Symbol	Default	Description	
DATA0 (0x00)	0	redundancy<0>	0	Redundancy Bits	Customer Settings
	1	redundancy<1>	0		
	2	redundancy<2>	0		
	3	redundancy<3>	0		
	4	redundancy<4>	0		
	5	redundancy<5>	0		
	6	redundancy<6>	0		
	7	redundancy<7>	0		

Note(s):

1. Factory settings (FS) are used for testing and programming at **ams**. These settings are locked (only read access possible).

Data Content

- **Redundancy (7:0):** For a better programming yield, a redundancy is implemented. In case the programming of one bit fails, then this function can be used. With an address (7:0) one bit can be selected and programmed.
- **Lock_OTPCUST** = 1, locks the customer area in the OTP and the device, from hereon, starts in operating mode.

Figure 44:
Redundancy

Redundancy Code	OTP Bit Selection
Redundancy <7:0> in decimal	
0	None
1	OP_Mode<1>
2	DIAG_HIGH
3	PWM Frequency<0>
4 - 10	ClampHi<6> - ClampHi<0>
11 - 17	ClampLow<6> - ClampLow<0>
18	OP_Mode<0>
19 - 32	OffsetIn<13> - OffsetIn<0>
33 - 46	Gain<13> - Gain<0>
47 - 60	BP<13> - BP<0>
61 - 72	OffsetOut<11> - OffsetOut<0>
73	Invert_Slope
74	FAST_SLOW
75	EXT_RANGE
76	DAC_MODE
77	Lock_OTPCUST
78 - 83	KD<5> - KD<0>
84 - 85	KDHYS<1> - KDHYS<0>
86	PWM Frequency<1>

- **Invert_Slope** = 1, inverts the output characteristic in analog output mode.
- **Gain (7:0):** With this value one can adjust the steepness of the output slope can be adjusted.
- **EXT_RANGE = 1,** provides a wider z-Range of the magnet by turning OFF the alarm function.
- **FAST_SLOW = 1**, improves the noise performance due to internal filtering.
- **BP (13:0):** The breakpoint can be set with resolution of 14 bit.
- **PWM Frequency (1:0):** Four different frequency settings are possible. Please refer to Figure 22.
- **KDHYS (1:0):** Avoids flickering at the KDOWN output (pin 11). For settings, refer to Figure 23.
- **OffsetOut (11:0):** Output characteristic parameter
- **ANALOG_PWM = 1**, selects the PWM output mode.
- **OffsetIn (13:0):** Output characteristic parameter
- **DIAG_HIGH = 1:** In case of an error, the signal goes into high failure-band.
- **ClampHI (6:0):** Sets the clamping level high with respect to VDD.
- **DAC_MODE** disables filter at DAC
- **ClampLow (6:0):** Sets the clamping level low with respect to VDD.
- **KD (5:0):** Sets the kick-down level with respect to VDD.

Read / Write User Data

Figure 45:
Read / Write Data

Area Region	Address	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RW User Data	0x10	16	CORDIC_OUT[7:0]							
	0x11	17	0	0	CORDIC_OUT[13:8]					
	0x12	18	OCF	COF	0	0	0	0	DSP_RES	R1K_10K
	0x17	23	AGC_VALUE[7:0]							

Read Only
Read and Write

Data Content

Data only for read:

- **CORDIC_OUT(13:0):** 14-bit absolute angular position data.
- **OCF** (**O**ffset **C**ompensation **F**inished): logic high indicates the finished Offset Compensation Algorithm. As soon as this bit is set, the AS5263 has completed the startup and the data is valid.
- **COF** (**C**ORDIC **O**ver**f**low): Logic high indicates an out of range error in the CORDIC part. When this bit is set, the CORDIC_OUT(13:0) data is invalid. The absolute output maintains the last valid angular value. This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.
- **AGC_VALUE (7:0):** magnetic field indication.

Data for write and read:

- **DSP_RES** resets the DSP part of the AS5263 the default value is 0. This is active low. The interface is not affected by this reset.
- **R1K_10K** defines the threshold level for the OTP fuses. This bit can be changed for verification purpose. A verification of the programming of the fuses is possible. The verification is mandatory after programming.

Programming Procedure

Note(s): After programming the OTP fuses, a verification is mandatory. The procedure described below must be strictly followed to ensure properly programmed OTP fuses.

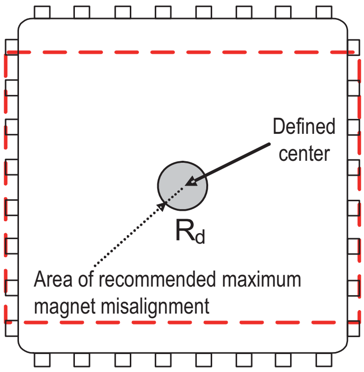
- Pull-Up on OUT pin
- VDD=5V
- Wait startup time, device enters communication mode
- Write128 command: The trimming bits are written in the SFR memory.
- Read128 command: The trimming bits are read back. Compare read data to previous written data. If the data matches, then proceed further.
- Upload command: The SFR memory is transferred into the OTP RAM.
- Fuse command: The OTP RAM is written in the Poly Fuse cells.
- Wait fuse time (6 ms)
- Write command (R1K_10K=1): Poly Fuse cells are transferred into the RAM cells compared with 10KΩ resistor.
- Download command: The OTP RAM is transferred into the SFR memory.
- Read128 command: The fused bits are read back. Compare read data to previous written and read data. If the data matches, then proceed further.
- Write command (R1K_10K=0): Poly Fuse cells are transferred into the RAM cells compared with 1KΩ resistor.
- Download command: The OTP RAM is transferred into the SFR memory.
- Read128 command: The fused bits are read back. Compare read data to previous written and two times read data. If the data matches, then proceed further.
- Pass2Func command or POR: Go to Functional mode.

An equal output of all read out data is sufficient to verify the OTP programming. If the data output is a mismatch, then the programming of the OTP was not successful and can cause a change of the OTP register content during operation over temperature and life time.

Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in Figure 46.

Figure 46:
Defined Chip Center and Magnet Displacement Radius



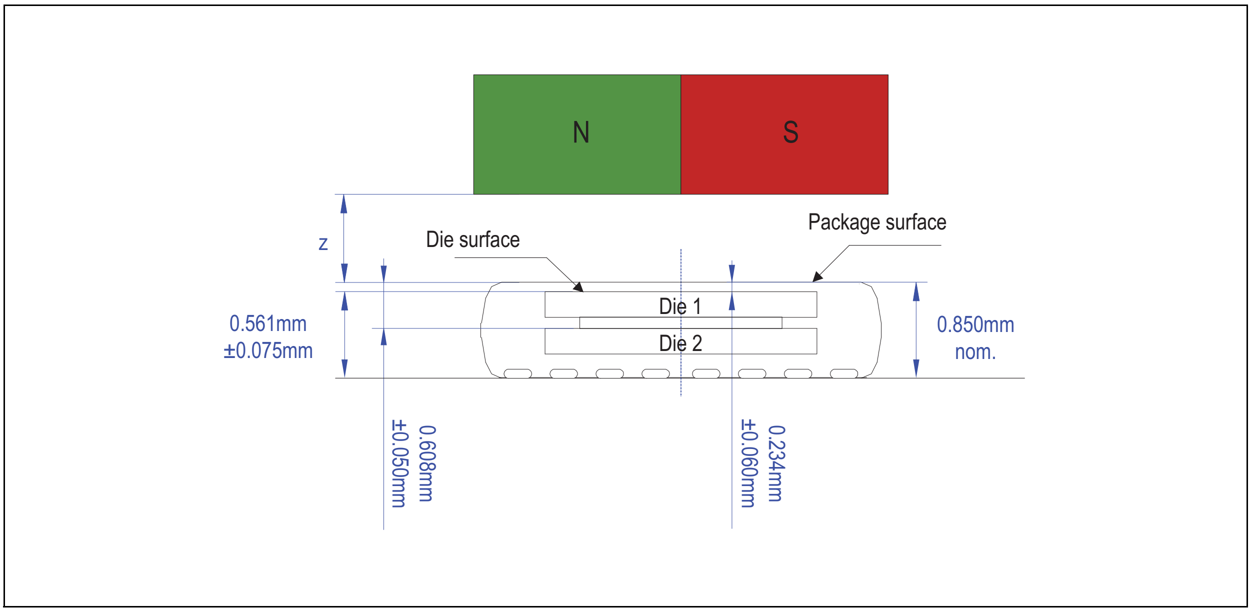
Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm (larger magnets allow more displacement) from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 46). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.5mm, provided the recommended magnet material and dimensions (6mm x 3mm) are used. Larger distances are possible, as long as, the required magnetic field strength stays within the defined limits.

However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by an alarm forcing the output into the failure band.

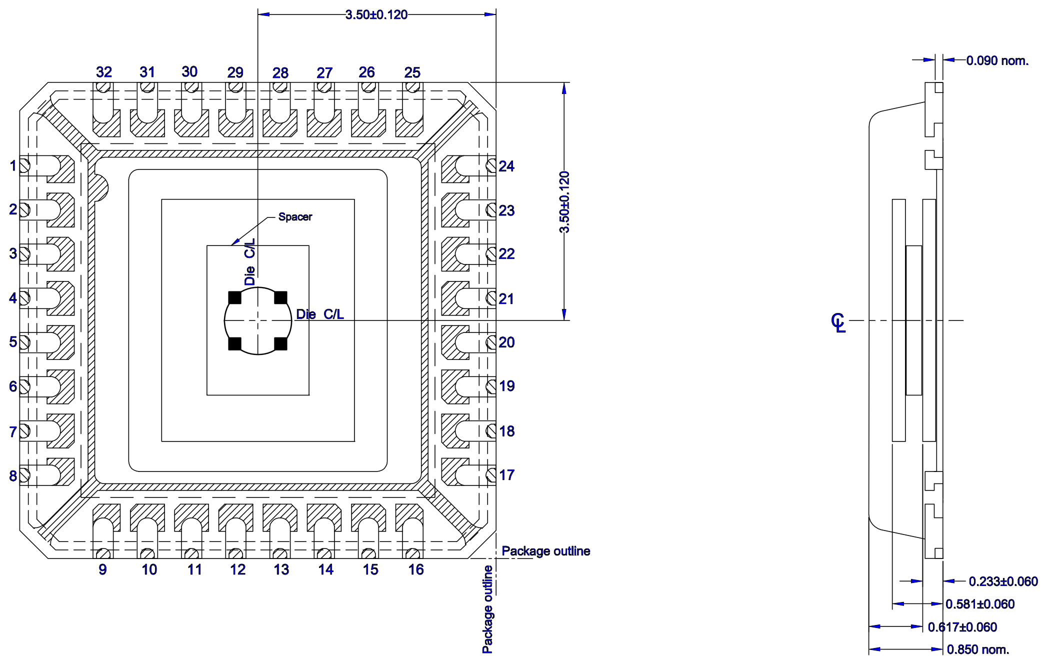
Figure 47:
Vertical Placement of the Magnet



Mechanical Data

The internal Hall elements are placed in the center of the package on a circle with a radius of 1 mm.

Figure 48:
Hall Element Position



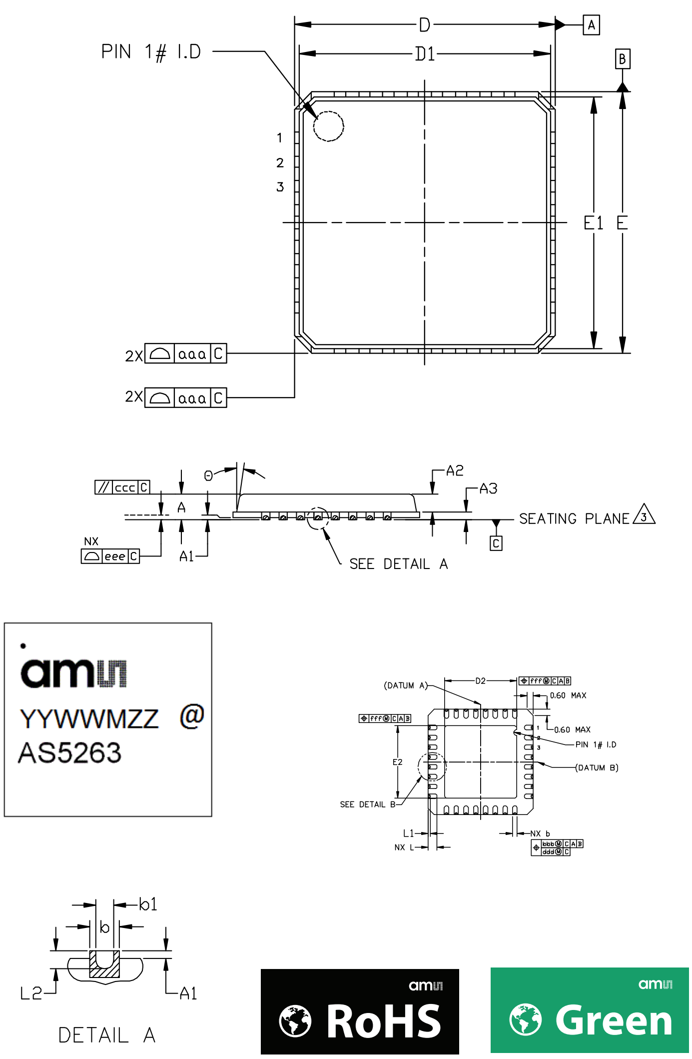
Note(s):

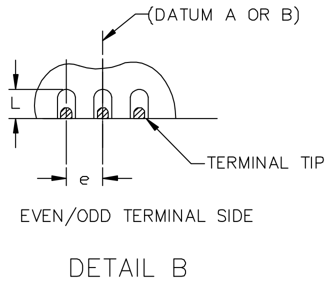
1. All dimensions in mm.
2. Die thickness 150µm.
3. Adhesive thickness 12µm (nom).
4. Spacer thickness 178µm (typ).

Package Drawings & Markings

The device is available in a 32-pin MLF (7mm x 7mm) dimple package.

Figure 49:
Package Drawings & Dimensions





Symbol	Min	Typ	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3		0.20 REF	
L	0.50	0.60	0.70
L1	0.05	0.15	0.25
L2	0.05	0.10	0.15
Q	0º	-	14º
b	0.25	0.30	0.35
b1	0.15	0.20	0.25
D		7.00 BSC	
E		7.00 BSC	
e		0.65 BSC	
D1		6.75 BSC	
E1		6.75 BSC	
D2	4.70	4.80	4.90
E2	4.70	4.80	4.90
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		32	

Note(s):

1. Dimensions and tolerancing confirm to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Unilateral coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Figure 50:
Marking: YYWWMZZ@

YY	WW	M	ZZ	@
Year	Manufacturing Week	Plant identifier	Traceability code	Sublot identifier

Note(s):

1. IC's marked with a white dot or the letters "ES" denote engineering samples.

Ordering & Contact Information

The devices are available as the standard products shown in Figure 51.

Figure 51:
Ordering Information

Ordering Code	Package	Description	Delivery Form	Delivery Quantity
AS5263-HQFT	32-pin MLF (7mm x 7mm) Dimple	Redundant 12-bit Magnetic Rotary Encoder with MLF Dimple Option	Tape & Reel	4000 pcs/reel
AS5263-HQFM				500 pcs/reel

Not Recommended for New Designs!

ams AG is discontinuing production of this device. Final lifetime buy order must be placed by DECEMBER 31, 2017.

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1-08 (2016-Jul-18) to current revision 1-09 (2017-Jul-18)	Page
Update of document status	
Update of Ordering Information section by adding NRND statement	52

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision
2. Correction of typographical errors is not explicitly mentioned.

Content Guide