

# AS7024

## Biosensors

### General Description

The AS7024 device provides a flexible analog front end for light sensing applications. The photodiode input circuit can be configured in different ways to guarantee best tradeoff between speed and sensitivity for a large number of different sensing applications.

AS7024 is targeted for wearables (fitness band, smart watch).

*Ordering Information and Content Guide appear at end of datasheet.*

### Key Benefits and Features

The benefits and features of AS7024, Biosensors are listed below:

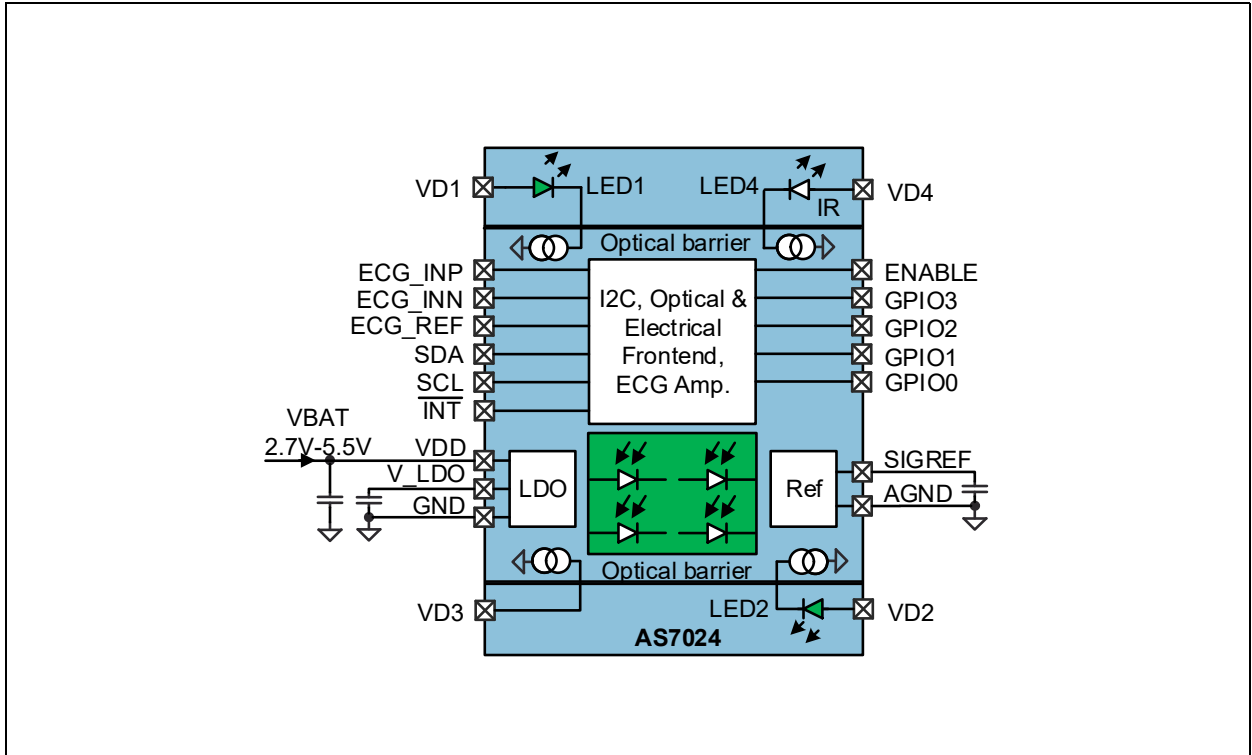
**Figure 1:**  
Added Value of Using AS7024

Benefits	Features
<ul style="list-style-type: none"> <li>Allows smallest application size e.g. narrow HRM measurement band</li> </ul>	<ul style="list-style-type: none"> <li>Single device integrated optical solution</li> </ul>
<ul style="list-style-type: none"> <li>Good HRM measurement quality</li> </ul>	<ul style="list-style-type: none"> <li>Low noise analog optical front end</li> </ul>
<ul style="list-style-type: none"> <li>Additional information for end user</li> </ul>	<ul style="list-style-type: none"> <li>Analog electrical front end (e.g. for temperature sensing using a NTC or galvanic skin resistivity (GSR))</li> </ul>
<ul style="list-style-type: none"> <li>Long operating time</li> </ul>	<ul style="list-style-type: none"> <li>Hardware sequencer to offload processor</li> <li>Adjustable LED driver with current control</li> </ul>
<ul style="list-style-type: none"> <li>Works reliably with ambient light</li> </ul>	<ul style="list-style-type: none"> <li>Synchronous demodulator</li> </ul>

### Applications

The device is suitable for optical sensor platform.

Figure 2:  
Application Schematic AS7024

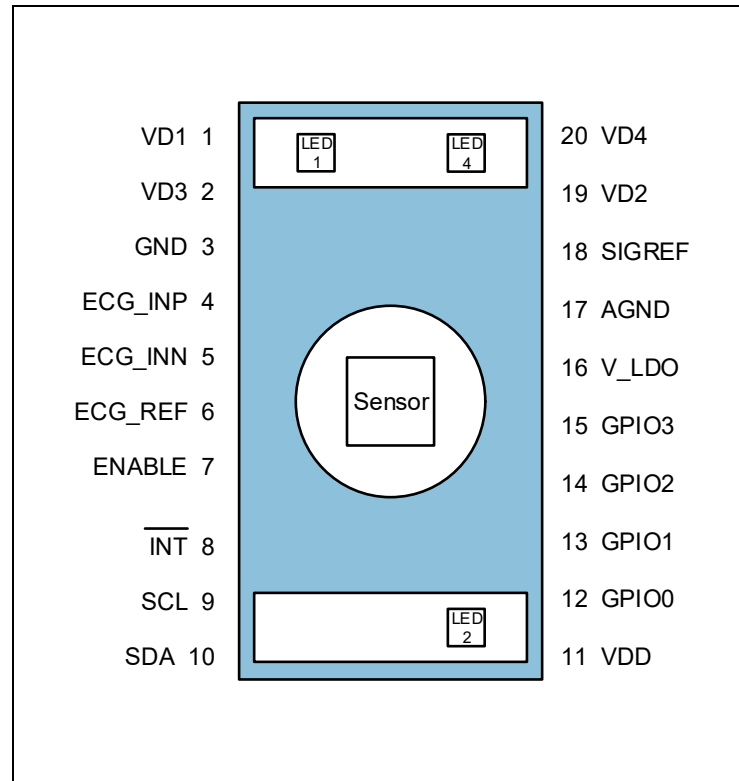


## Pin Assignments

**Figure 3:**  
AS7024 Optical Module Pinout (Top View)

### Optical Module Pinout:

This drawing is not to scale



**Figure 4:**  
Pin Description

Pin No.	Pin Name	Description
1	VD1	Supply voltage for LED D1
2	VD3	Connection to current sink 3
3	GND	Power supply ground. All voltages are referenced to GND.
4	ECG_INP	ECG amplifier positive input
5	ECG_INN	ECG amplifier negative input
6	ECG_REF	ECG amplifier reference output
7	ENABLE	Enable input for AS7024. Active high. Setting this input to low resets all internal registers and the AS7024 enters power down mode. Setting it high allows operation of the AS7024. If ENABLE is not used (AS7024 always enabled), connect to VDD.
8	$\overline{\text{INT}}$	Open drain interrupt output pin. Active low.
9	SCL	I <sup>2</sup> C serial clock input terminal – the device does not use clock stretching therefore SCL is only an input terminal.

Pin No.	Pin Name	Description
10	SDA	I <sup>2</sup> C serial data I/O terminal – open drain.
11	VDD	Supply voltage. Connect a 2.2μF capacitor to GND.
12	GPIO0	General purpose input/output
13	GPIO1	General purpose input/output
14	GPIO2	General purpose input/output
15	GPIO3	General purpose input/output
16	V_LDO	1.9V output voltage. Connect 2.2μF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 or 0201 sized GRM033R60J225ME47 from Murata – needs to have >1μF with 1.0V voltage bias); do not load externally
17	AGND	Analog ground. Connect to low noise GND
18	SIGREF	Analog reference output. Connect 2.2μF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 or 0201 sized GRM033R60J225ME47 from Murata – needs to have >1μF specified for 1.0V voltage bias); do not load externally The typical operating voltage on this pin is 0.6V (sigref_en=1)
19	VD2	Supply voltage for LED D2
20	VD4	Supply voltage for LED D4

## Absolute Maximum Ratings

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:  
Absolute Maximum Ratings <sup>(1)</sup>

Symbol	Parameter	Min	Max	Units	Comments
<b>Electrical Parameters</b>					
VDD	Supply Voltage to Ground		6V	V	
V <sub>IN</sub>	Input Pin Voltage to Ground pins GPIO0/1/2/3	-0.3	VDD+0.3V max. 6V	V	Diode to VDD
V <sub>IN-OTHER</sub>	Input Pin Voltage to Ground pins SCL/SDA/INT/ENABLE and VD1/VD2/VD3/VD4	-0.3	5.5	V	No internal diode to VDD or V_LDO
V <sub>VD1/2/3/4-INTERNAL</sub>	Voltage between internal pin of VD1-VD4 to VDD		VDD+0.3V	V	Internal diode between current source (internal node at anode of the LED if the pin has a LED otherwise VD1/2/3/4 pin) and VDD
V <sub>IN-LDO</sub>	Input Pin Voltage to Ground for pin V_LDO	-0.3	VDD+0.3V max. 6V	V	Diode to VDD
V <sub>IN-LDO-DIODE</sub>	Input Pin Voltage to Ground pins for ECG_INP/ECG_INN/ECG_REF/SIGREF	-0.3	V_LDO+0.3V max. 6V	V	Diode to V_LDO
V <sub>GND-AGND</sub>	Analog to power ground voltage difference	-0.3	+0.3	V	
I <sub>SCR</sub>	Input Current (latch-up immunity)	-100	100	mA	JEDEC JESD78 Connect specified capacitor on SIGREF and V_LDO during latchup test
<b>Electrostatic Discharge</b>					
ESD <sub>HBM</sub>	Electrostatic Discharge HBM		±2.0	kV	JS-001-2014

Symbol	Parameter	Min	Max	Units	Comments
<b>Temperature Ranges and Storage Conditions</b>					
T <sub>STRG</sub>	Storage Temperature Range	-40	85	°C	
T <sub>BODY</sub>	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices."
RH <sub>NC</sub>	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time of 168h

**Note(s):**

1. All optical customer designs shall be reviewed by **ams** before production.

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

VDD=2.7 to 5.5V, typ. values are at  $T_{AMB}=25^{\circ}\text{C}$  (unless otherwise specified).

**Figure 6:**  
**Operating Conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Supply voltage		2.7	3.8	5.5	V
$T_{AMB}$	Operating free-air temperature		-30		70	$^{\circ}\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IDD	Supply current	ENABLE=VDD, Ido_en=0; osc_en=0; internal LDO operating in low power mode – only I <sup>2</sup> C communication possible, no blocks shall be enabled <sup>(1)</sup>		22		μA
		ENABLE=VDD, Ido_en=1; osc_en=0; internal LDO operating and bandgap running – I <sup>2</sup> C communication possible, analog blocks can be enabled <sup>(1)</sup>		32		μA
		ENABLE=VDD, Ido_en=1, osc_en=1; internal LDO operating and bandgap and oscillator running – I <sup>2</sup> C communication possible, analog blocks can be enabled <sup>(1)</sup>		86		μA
		SIGREF buffer (sigref_en=1)		52		μA
		transimpedance amplifier (pd_amp_en=1)		110		μA
		Optical front end operating (one channel)		200		μA
		Gain stage (ofe1_gain_en=1 or ofe2_gain_en=1)		75		μA
		ADC sampling at 20Hz with 64μs settling time		4.5		μA
		ECG amplifier and frontend (need SIGREF enabled)		190		μA
		ECG leakage compensation (ecg_low_leakage_en=1), low pass filter, high pass filter and gain stage		151		μA
		Power down, no I <sup>2</sup> C communication possible <sup>(2)</sup> ENABLE=GND		0.5		μA
VOL	GPIO0-3, INT, SDA output low voltage	With 3 mA load With 6 mA load	0 0		0.4 0.8	V
VOH	GPIO0-3 output high voltage	With 3 mA load	2.3		VDD	V
VIH	GPIO0-3, SCL, SDA, ENABLE input high voltage		1.25			V



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	GPIO0-3, SCL, SDA, ENABLE input low voltage				0.54	V
ILEAK1	GPIO0-3, SCL, SDA, ENABLE, INT		-1		1	μA
ILEAK2	VD1, VD23 pins		-1		1	μA
E_f2M	Tolerance of internal 2MHz oscillator	0°C to 70°C, VDD<5.0V	-2		+2	%
		-30°C to 70°C	-4		+2	%
<b>ECG Amplifier and Filter</b>						
ILEAK_ECG	ECG pins leakage current	Lab evaluation shows <math>\pm 20\text{nA}</math> maximum leakage current. Not production tested.		±1		nA
V <sub>NOISE_ECG</sub>	Integrated noise	ADC sampling at 400Hz; low pass filter set to 40Hz, PPG channel operating in parallel		20		μV
CMRR <sub>ECG</sub>	Common mode rejection ratio	Measured at 50Hz and 100Hz		73		dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>LED</b>						
$I_{LED}$	Allowed operating LED current range		0		50	mA
		1/10 duty cycle @ 1 kHz			100	
$V_{F_{LED}}$	Forward voltage	Green LED, add compliance voltage of LED driver, $I_{LED}=10\text{mA}$ , add compliance voltage of LED driver ( $V_{Dmin}$ ) to obtain minimum voltage on the pin to drive the current at $T_{AMB}=25^{\circ}\text{C}$		3.1	3.3	V
		IR LED, $I_{LED}=20\text{mA}$		1.4		
$\lambda_p$	Peak wavelength at $I_{LED}=20\text{mA}$	Green LED		527		nm
		IR LED		940		
<b>LED Driver</b>						
$I_{LED1/2/3/4}$	LED output current range	LED current is adjustable with 10 bits – registers curr1/2/3/4	0		100	mA
	Tolerance	At 35mA output current (currX[9:0]=166h, X=1...4), $V_{DD}<5.0\text{V}$	-7		7	%
$V_{Dmin}$	Output voltage compliance			0.3		V
$V_{Dmax}$	Output voltage maximum				5.5	V

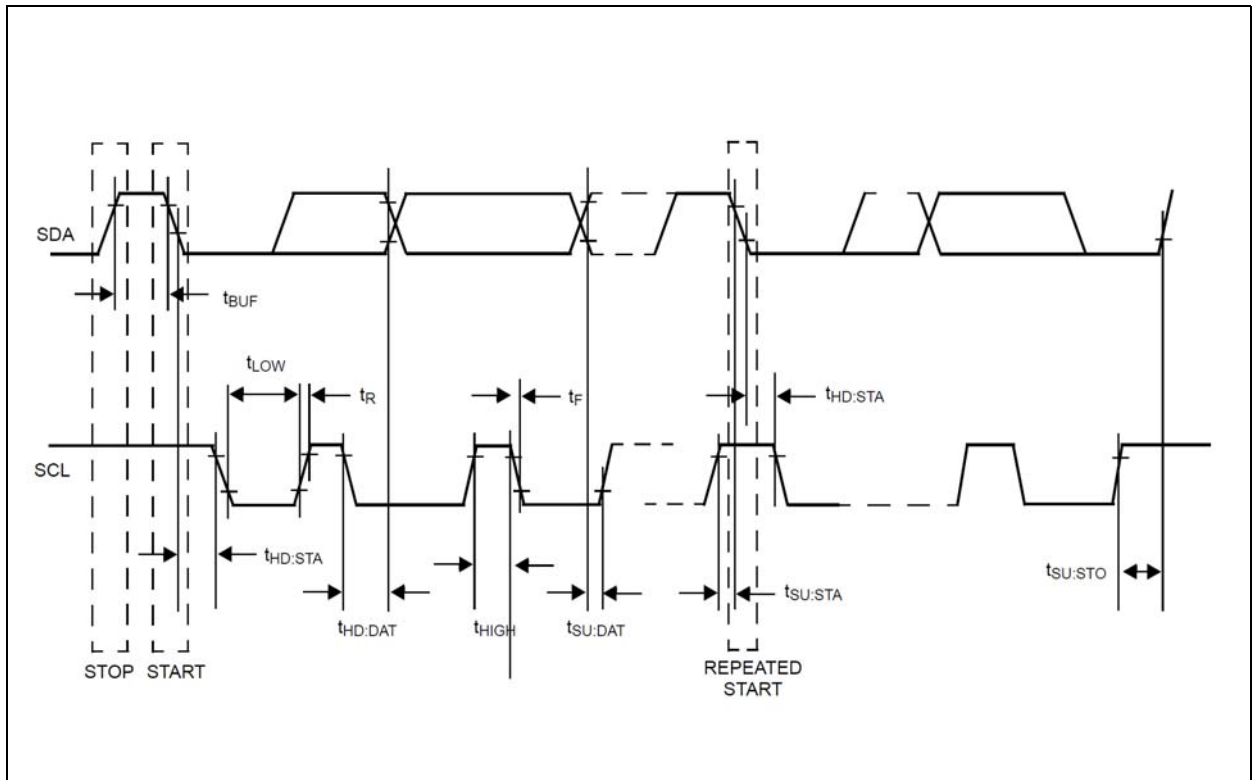
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Photodiode</b>						
Re <sub>PD1-4</sub>	Irradiance responsivity photodiode PD1...PD4	$\lambda_p=525\text{nm}$ , 4 photodiodes used pd1/2/3/4=1, gain_g=4x, gain_en=1, pd_ampres = 7M $\Omega$		45.9		mV/ ( $\mu\text{W}$ /cm <sup>2</sup> )
	Irradiance responsivity photodiode B	$\lambda_p=940\text{nm}$ , gain_g=4x, gain_en=1, pd_ampres=7M $\Omega$		0.3		
I <sub>d</sub>	Dark current	E <sub>e</sub> =0, T <sub>AMB</sub> =25°C	0		1	nA
I <sub>os</sub>	Extrapolated offset current	T <sub>AMB</sub> =25°C	-1		1	nA
<b>ADC</b>						
V <sub>ref</sub>	ADC reference voltage			1.6		V
	Resolution		14			Bit
INL	Relative accuracy	T <sub>AMB</sub> =25°C	-8		8	LSB
DNL	Differential nonlinearity <sup>(3)</sup>			1.5		LSB
	Offset error		-8		8	LSB
	Gain error		-8		8	LSB
SNR	Signal-to-noise ratio		F <sub>sample</sub> = 1kHz, F <sub>signal</sub> =100Hz		80	
THD	Total harmonic distortion	F <sub>sample</sub> = 1kHz, F <sub>signal</sub> =100Hz		-70		dB
T <sub>conv</sub>	Conversion rate	14 bit resolution			50	ksps
V <sub>in</sub>	Input voltage range		0		V <sub>ref</sub>	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>I<sup>2</sup>C Mode Timings</b>						
$f_{\text{SCLK}}$	SCL Clock Frequency		0		400	kHz
$t_{\text{BUF}}$	Bus Free Time Between a STOP and START Condition		1.3			$\mu\text{s}$
$t_{\text{HD:STA}}$	Hold Time (Repeated) START Condition <sup>(4)</sup>		0.6			$\mu\text{s}$
$t_{\text{LOW}}$	LOW Period of SCL Clock		1.3			$\mu\text{s}$
$t_{\text{HIGH}}$	HIGH Period of SCL Clock		0.6			$\mu\text{s}$
$t_{\text{SU:STA}}$	Setup Time for a Repeated START Condition		0.6			$\mu\text{s}$
$t_{\text{HD:DAT}}$	Data Hold Time <sup>(5)</sup>		0		0.9	$\mu\text{s}$
$t_{\text{SU:DAT}}$	Data Setup Time <sup>(6)</sup>		100			ns
$t_{\text{R}}$	Rise Time of Both SDA and SCL Signals		20		300	ns
$t_{\text{F}}$	Fall Time of Both SDA and SCL Signals		20		300	ns
$t_{\text{SU:STO}}$	Setup Time for STOP Condition		0.6			$\mu\text{s}$
$C_{\text{B}}$	Capacitive Load for Each Bus Line	CB — total capacitance of one bus line in pF			400	pF
$C_{\text{I/O}}$	I/O pin Capacitance (SDA, SCL)				10	pF

**Note(s):**

- GPIO0-3 configured to draw minimum current (software dependent).
- The design of AS7024 is done in a way that it does not affect other I<sup>2</sup>C communication on SCL/SDA even if AS7024 is in power down.
- Specified only typical value for DNL to reduce production test time.
- After this period, the first clock pulse is generated.
- A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIHMIN of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- A fast-mode device can be used in a standard-mode system, but the requirement  $t_{\text{SU:DAT}} = 250\text{ns}$  must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{\text{R max}} + t_{\text{SU:DAT}} = 1000 + 250 = 1250\text{ns}$  before the SCL line is released.

**Figure 7:**  
**I<sup>2</sup>C Mode Timing Diagram**

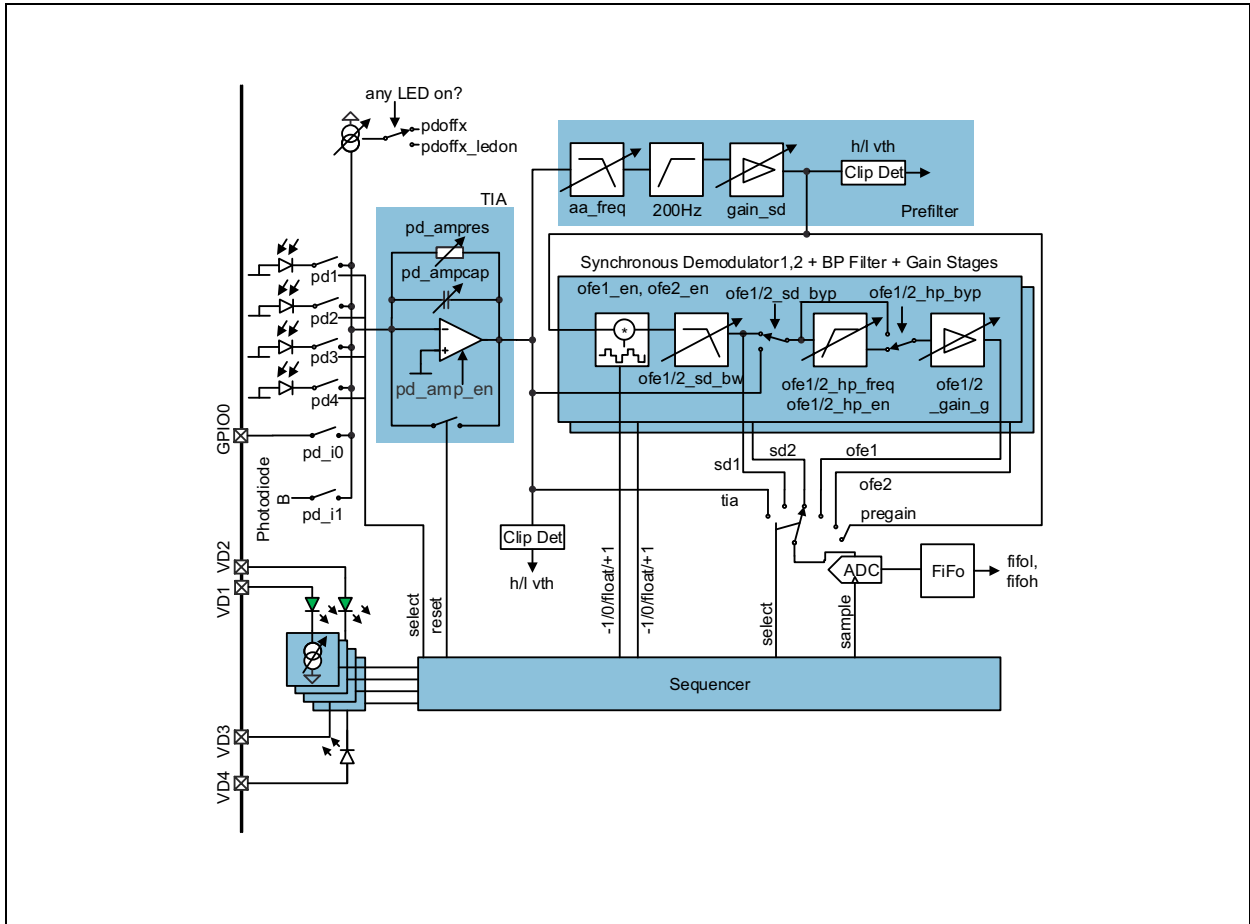


**I<sup>2</sup>C Mode Timing Diagram:** This figure shows the different timings required for I<sup>2</sup>C communication.

Detailed Description

Optical Analog Front End

Figure 8:  
Optical Analog Front End



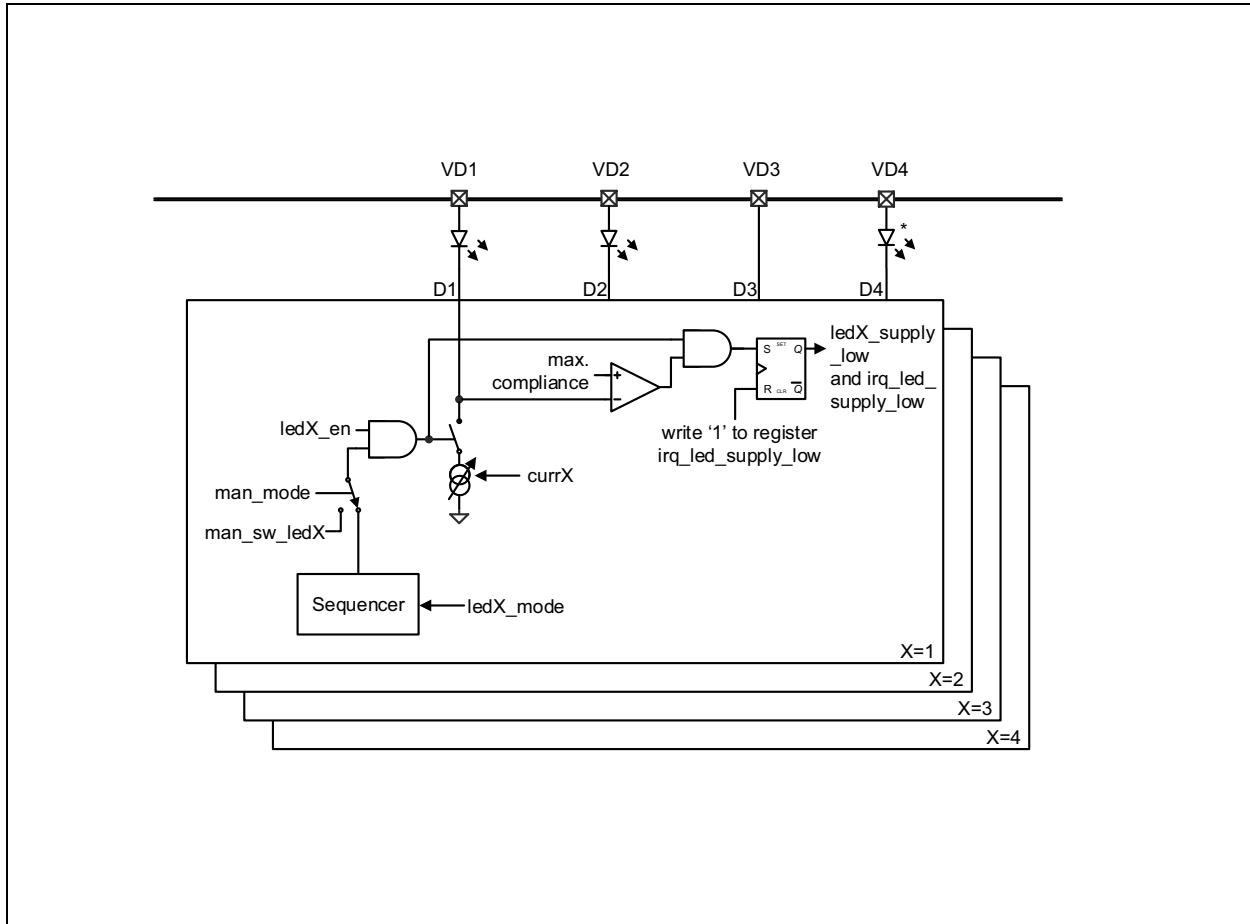
**LEDs**

Two green LEDs are used with anode on pin VD1 and VD2. A IR LED is connected with anode to pin VD4. VD3 allows direct access to the current sink 3.

### LED-Driver

The LED-driver outputs can be controlled manually or by the built in sequencer. See [Optical Front End Operating Modes](#)

**Figure 9:**  
LED Drivers



LED Configuration Registers

Figure 10:  
LED\_CFG Register

0x10: LED_CFG					
Field	Name	Rst	Type	Description	
6	sigref_en	0	RW	Signal reference: Is required for all analog blocks (except PD_Amp or light-to-frequency operation) 0 ... Disable signal reference 1 ... Enable signal reference	
5:4	sigref_voltage	0	RW	Voltage setting of SIGREF – datasheet parameters are guaranteed only for default value of 0.6V.	
				<b>Setting</b>	<b>IMAX</b>
				0	0.6V (default)
				1	0.7V
				2	0.8V
3	led4_en	0	RW	0 ... Disables LED4 output source. 1 ... Enables LED4 output source.	
2	led3_en	0	RW	0 ... Disables LED3 output source. 1 ... Enables LED3 output source.	
1	led2_en	0	RW	0 ... Disables LED2 output source. 1 ... Enables LED2 output source.	
0	led1_en	0	RW	0 ... Disables LED1 output source. 1 ... Enables LED1 output source.	

The LED\_CURR defines the LED output current. Warning: it is recommended to configure the current only when the output is not active, as there is no latch implemented to keep the 10 bits consistent. New values are applied directly and immediately.

Figure 11:  
LED1\_CURRL Register

0x12: LED1_CURRL				
Field	Name	Rst	Type	Description
7:6	curr1[1:0]	0	RW	LED1 output current lower 2 bits



**Figure 12:**  
LED1\_CURRH Register

0x13: LED1_CURRH				
Field	Name	Rst	Type	Description
7:0	curr1[9:2]	0	RW	LED1 output current upper 8 bits Coding for curr1[9:0]: 000h ... 786µA 001h ... 883µA (1 LSB=97µA) 002h ... 980µA 166h ... 35mA 3FFh ... 100mA

**Figure 13:**  
LED2\_CURRL Register

0x14: LED2_CURRL				
Field	Name	Rst	Type	Description
7:6	curr2[1:0]	0	RW	LED2 output current lower 2 bits

**Figure 14:**  
LED2\_CURRH Register

0x15: LED2_CURRH				
Field	Name	Rst	Type	Description
7:0	curr2[9:2]	0	RW	LED2 output current upper 8 bits Coding for curr2[9:0]: 000h ... 786µA 001h ... 883µA (1 LSB=97µA) 002h ... 980µA 166h ... 35mA 3FFh ... 100mA

**Figure 15:**  
LED3\_CURRL Register

0x16: LED3_CURRL				
Field	Name	Rst	Type	Description
7:6	curr3[1:0]	0	RW	LED3 output current lower 2 bits

**Figure 16:**  
LED3\_CURRH Register

0x17: LED3_CURRH				
Field	Name	Rst	Type	Description
7:0	curr3[9:2]	0	RW	LED3 output current upper 8 bits Coding for curr3[9:0]: 000h ... 786μA 001h ... 883μA (1 LSB=97μA) 002h ... 980μA 166h ... 35mA 3FFh ... 100mA

**Figure 17:**  
LED4\_CURRL Register

0x18: LED4_CURRL				
Field	Name	Rst	Type	Description
7:6	curr4[1:0]	0	RW	LED4 output current lower 2 bits

**Figure 18:**  
LED4\_CURRH Register

0x19: LED4_CURRH				
Field	Name	Rst	Type	Description
7:0	curr4[9:2]	0	RW	LED4 output current upper 8 bits Coding for curr4[9:0]: 000h ... 786μA 001h ... 883μA (1 LSB=97μA) 002h ... 980μA 166h ... 35mA 3FFh ... 100mA

**Figure 19:**  
**LED12\_MODE Register**

0x2c: LED12_MODE					
Field	Name	Rst	Type	Description	
7	man_sw_led2 <sup>(1)</sup>	0	RW	0 ... LED output D2 disabled. (High impedance) 1 ... LED output D2 enabled	
6:4	led2_mode	0	RW	LED2 mode	
				<b>Setting</b>	<b>Behavior</b>
				0	Always OFF
				1	Always ON when sequencer is active
				2	Controlled by sequencer
				3	Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.
				4	Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.
				5	Controlled by sequencer, only ON in every fourth iteration, starting at 1: 1, 5, 9 etc.
				6	Controlled by sequencer: secondary LED timing
7	Do not use				
3	man_sw_led1 <sup>(1)</sup>	0	RW	0 ... LED output D1 disabled. (High impedance) 1 ... LED output D1 enable	

0x2c: LED12_MODE					
Field	Name	Rst	Type	Description	
2:0	led1_mode	0	RW	LED1 mode	
				<b>Setting</b>	<b>Behavior</b>
				0	Always OFF
				1	Always ON when sequencer is active
				2	Controlled by sequencer
				3	Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.
				4	Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.
				5	Controlled by sequencer, only ON in every fourth iteration, starting at 0: 0, 4, 8 etc.
				6	Controlled by sequencer: secondary LED timing
				7	Do not use

**Note(s):**

- Function enabled only in manual mode

**Figure 20:**  
**LED34\_MODE Register**

0x2d: LED34_MODE					
Field	Name	Rst	Type	Description	
7	man_sw_led4 <sup>(1)</sup>	0	RW	0 ... LED output D4 disabled. (High impedance) 1 ... LED output D4 enabled	
6:4	led4_mode	0	RW	LED4 mode	
				<b>Setting</b>	<b>Behavior</b>
				0	Always OFF
				1	Always ON when sequencer is active
				2	Controlled by sequencer
				3	Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.
				4	Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.
				5	Controlled by sequencer, only ON in every fourth iteration, starting at 3: 3, 7, 11 etc.
				6	Controlled by sequencer: secondary LED timing
7	Do not use				
3	man_sw_led3 <sup>(1)</sup>	0	RW	0 ... LED output D3 disabled. (High impedance) 1 ... LED output D3 enabled	

0x2d: LED34_MODE					
Field	Name	Rst	Type	Description	
2:0	led3_mode	0	RW	LED3 mode	
				<b>Setting</b>	<b>Behavior</b>
				0	Always OFF
				1	Always ON when sequencer is active
				2	Controlled by sequencer
				3	Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.
				4	Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.
				5	Controlled by sequencer, only ON in every fourth iteration, starting at 2: 2, 6, 10 etc.
				6	Controlled by sequencer: secondary LED timing
7	Do not use				

**Note(s):**

1. Function enabled only in manual mode

The MAN\_SEQ\_CFG register is used to configure the operation of the optical front end.

**Figure 21:**  
MAN\_SEQ\_CFG Register

0x2e: MAN_SEQ_CFG				
Field	Name	Rst	Type	Description
7	man_mode	0	RW	0 ... Enables Sequencer 1 ... Enables Manual control of optical front end
6	man_sw_sdmult	0	RW	If man_mode=1 0 ... Disables synchronous demodulator multiplication 1 ... Enables synchronous demodulator multiplication
5	man_sw_sdpol	0	RW	If man_mode=1 0 ... Negative polarity in synchronous demodulator multiplication 1 ... Positive polarity in synchronous demodulator multiplication
4	man_sw_itg	0	RW	If man_mode=1 0 ... All integrator capacitors are shorted. Integrator is reset 1 ... Integrator capacitors are charging up. Integrator is running

0x2e: MAN_SEQ_CFG									
Field	Name	Rst	Type	Description					
3:1	diode_ctrl	0	RW	Connection of Photodiodes PD1, PD2, PD3, PD4 to the photodiode amplifier. 0 ... PD1-PD4 are connected 1 ... PD1 synchronous to LED1, PD2 sync/to LED2, PD3 sync/to LED3, PD4 sync/to LED4 2 ... PD1 synchronous to LED1, PD2 sync/to LED1, PD3 sync/to LED2, PD4 sync/to LED2 3 ... PD1 synchronous to LED1, PD2 sync/to LED1, PD3 sync/to LED4, PD4 sync/to LED4 4 ... SPO2 mode *(obsolete): (negedge(sdm1) or negedge(sdp1)) - PD1=0 PD2=0 PD3=1 PD4=1; (negedge(sdm2) or negedge(sdp2)) - PD1=1 PD2=1 PD3=0 PD4=0 Note that PD_CFG.pdX takes precedence - to turn OFF one photo diode, the respective bit has to be de-asserted in the PD_CFG register.					
				<b>PD_CFG.pdX</b>	<b>diode_ctrl</b>	<b>Photo Diode1</b>	<b>Photo Diode2</b>	<b>Photo Diode3</b>	<b>Photo Diode4</b>
				0	xx	OFF	OFF	OFF	OFF
				1	0	ON	ON	ON	ON
				1	1	LED1	LED2	LED3	LED4
				1	2	LED1	LED1	LED2	LED2
				1	3	LED1	LED1	LED4	LED4
				1	4	SPO2 mode (obsolete)			
1	5..7	Do not use							
0	seq_en	0	RW	0 ... Disables sequencer 1 ... Enables sequencer					

**Figure 22:**  
LEDSTATUS Register

0xa2: LEDSTATUS				
Field	Name	Rst	Type	Description
3	led4_supply_low	0	RO	If this bit is asserted, LED4 voltage has been too low.
2	led3_supply_low	0	RO	If this bit is asserted, LED3 voltage has been too low.
1	led2_supply_low	0	RO	If this bit is asserted, LED2 voltage has been too low.
0	led1_supply_low	0	RO	If this bit is asserted, LED1 voltage has been too low.

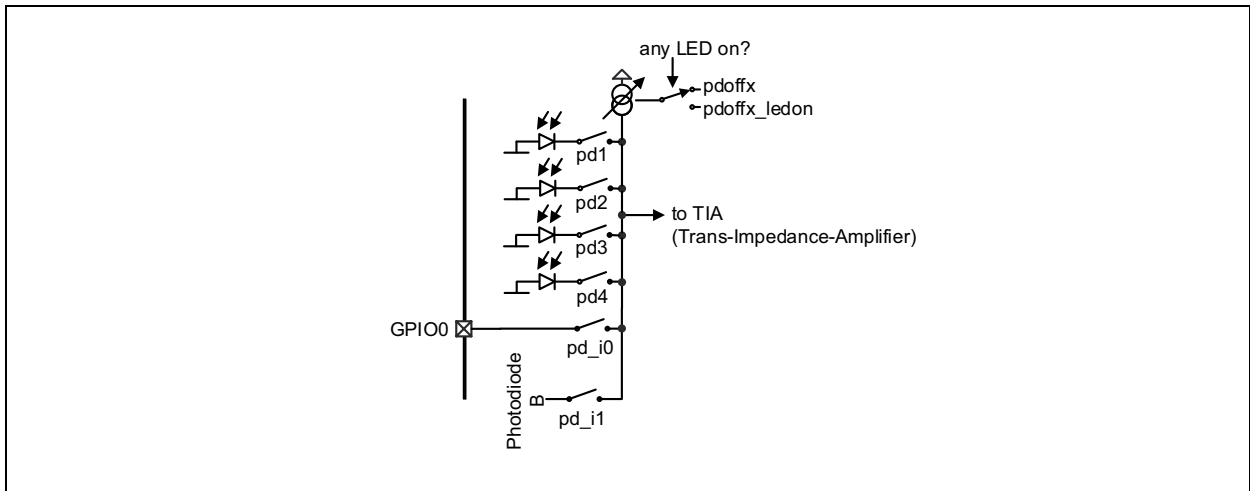
An asserted bit can be cleared by writing a '1' to the irq\_led\_supply\_low bit.

**Photodiode Selection**

In order to have flexible arrangement of the use photodiodes, PD1-PD4 can be individually connected to the photodiode amplifier input. The optional offset current allows cancellation of constant light sources like sunlight. In case of an external photodiode or any other sensor with (low) current output, the pins GPIO0 and GPIO1 can be used as input.

Additionally the sequencer can control the diodes – see diode\_ctrl described in register MAN\_SEQ\_CFG.

**Figure 23:  
Photodiode Selection**





**Photodiode Registers**

The PD\_CFG register is used to configure the input to the photo amplifier.

**Figure 24:**  
**PD\_CFG Register**

0x1a: PD_CFG				
Field	Name	Rst	Type	Description
5	pd4	0	RW	0 ... Photodiode PD4 is disconnected from photo amplifier 1 ... Photodiode PD4 is connected to photo amplifier (as defined in diode_ctrl)
4	pd3	0	RW	0 ... Photodiode PD3 is disconnected from photo amplifier 1 ... Photodiode PD3 is connected to photo amplifier (as defined in diode_ctrl)
3	pd2	0	RW	0 ... Photodiode PD2 is disconnected from photo amplifier 1 ... Photodiode PD2 is connected to photo amplifier (as defined in diode_ctrl)
2	pd1	0	RW	0 ... Photodiode PD1 is disconnected from photo amplifier 1 ... Photodiode PD1 is connected to photo amplifier (as defined in diode_ctrl)
1	pd_i1	0	RW	0... Photodiode B (see <a href="#">Photodiode Characteristics</a> ) disconnected from TIA input 1... Photodiode B (see <a href="#">Photodiode Characteristics</a> ) connected to TIA input; set ltf1_sel=0 and ltf2_sel=0.
0	pd_i0	0	RW	0 ... GPIO0-input is disconnected from photo amplifier 1 ... GPIO0-input is connected to photo amplifier; set gpio_a[0]=1.

**Figure 25:**  
PDOFFX\_LED OFF Register

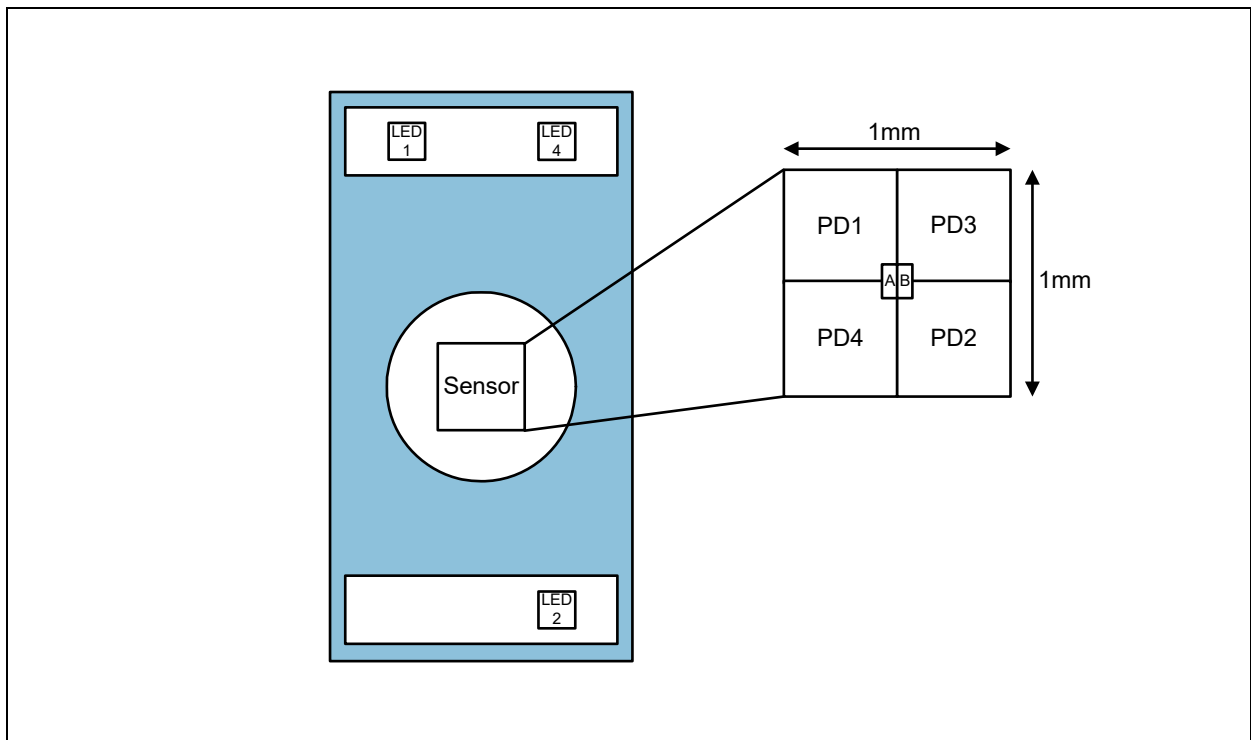
0x1b: PDOFFX_LED OFF				
Field	Name	Rst	Type	Description
7:0	pdoffx_ledoff	0	RW	Input offset current if all LEDs are OFF (all sw_led* sequencer outputs are zero) loffset = pdoffx_ledoff*10nA 0 ... Offset source is turned OFF

**Figure 26:**  
PDOFFX\_LED ON Register

0x1c: PDOFFX_LED ON				
Field	Name	Rst	Type	Description
7:0	pdoffx_ledon	0	RW	Input offset current if at least one LED is ON (one or more sw_led* sequencer outputs are non-zero) loffset = pdoffx_ledon*10nA 0 ... Offset source is turned OFF

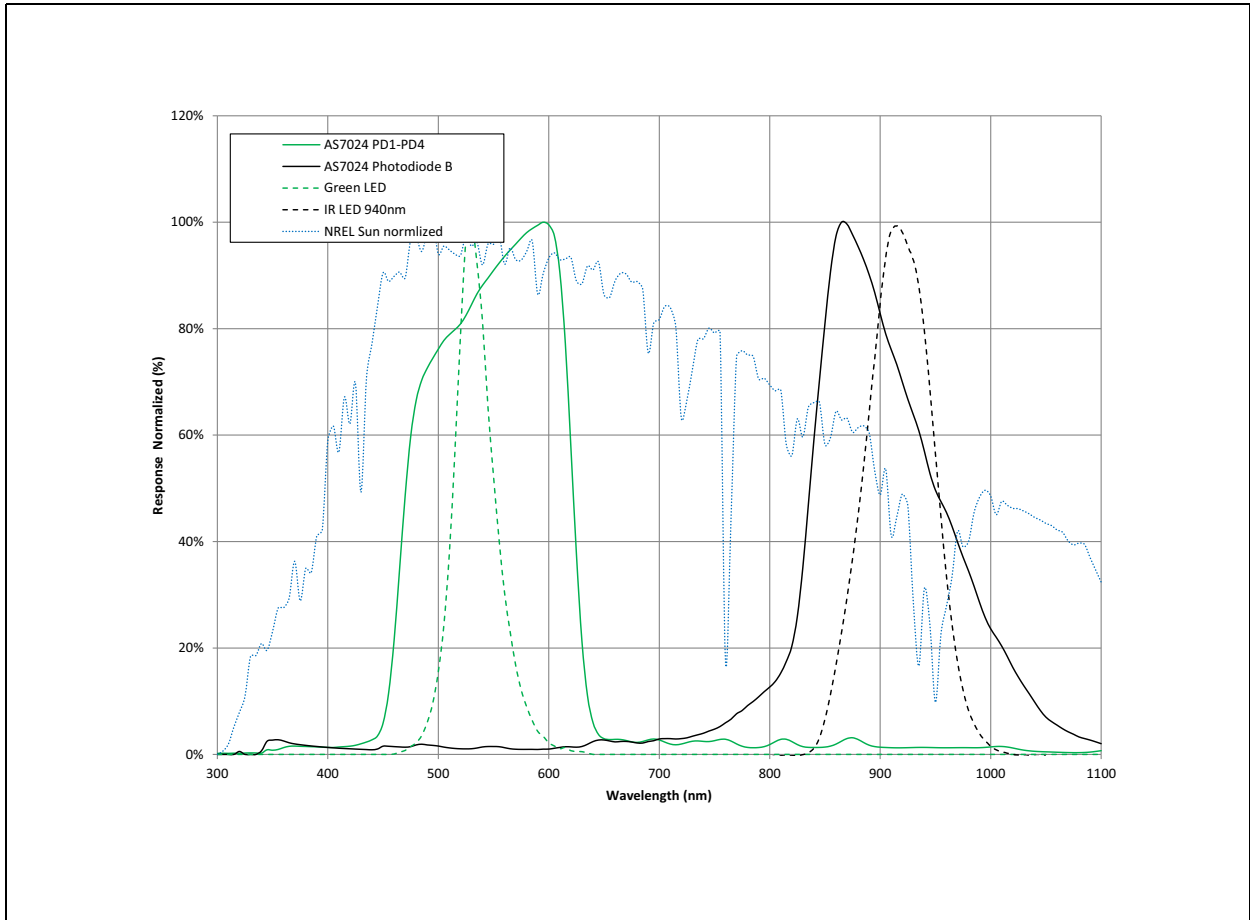
### Photodiode Characteristics

**Figure 27:**  
Photodiode Arrangement – Orientation as in [Figure 2](#)



For operation and characteristics of photodiode 'A' and photodiode 'B' see [Light-to-Frequency Mode](#).

**Figure 28:**  
**Photodiode Sensitivity (solid green and black) and LED Emission Spectrum (dotted green and dotted black)**



**Note(s):**

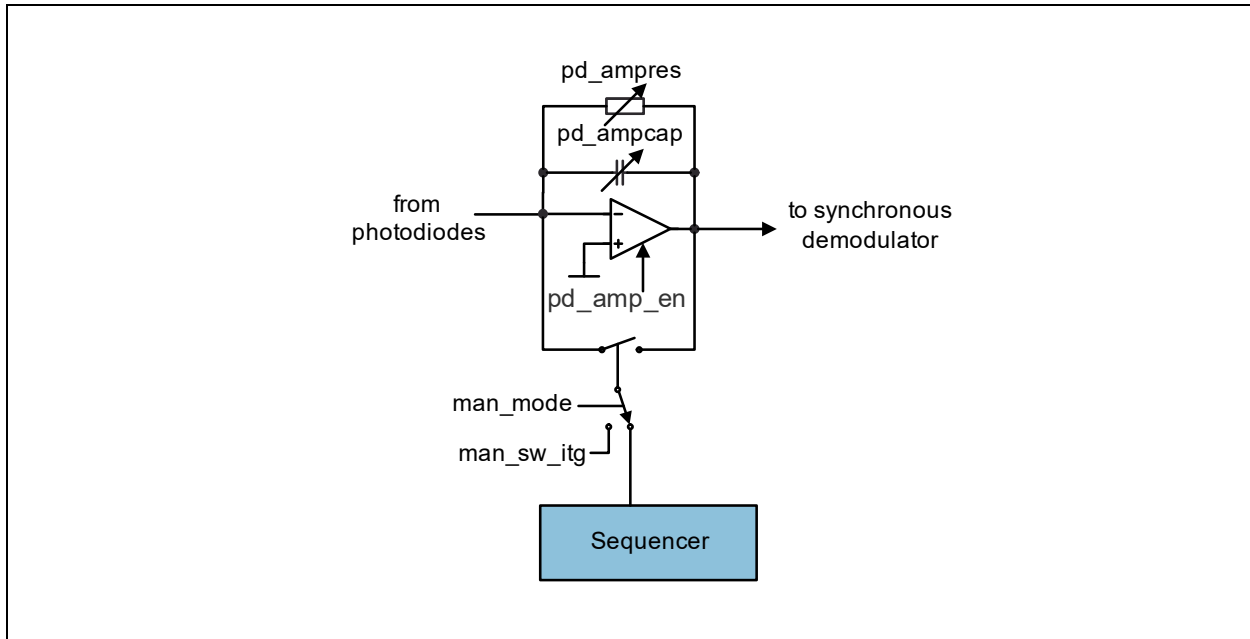
1. All 4 photodiodes used pd1/2/3/4=1; perpendicular; perpendicular light source and no diffuser used on AS7024; due to the difference in photodiode size the absolute response for Photodiode B (0.01mm<sup>2</sup>) is much lower compared to PD1-PD4 (0.8mm<sup>2</sup>).

**Photodiode Trans-Impedance Amplifier (TIA)**

The photodiode amplifier can be configured in three different modes:

- Photocurrent to frequency converter – see [Light-to-Frequency Mode Registers](#)
- Photocurrent to voltage converter
- Photocurrent integrator

**Figure 29:**  
Trans-Impedance-Amplifier (TIA)



The integration time  $t_{INT}$  is defined either by the sequencer ( $man\_mode=0$ ) or manually through the bit  $sw\_itg$  if  $man\_mode=1$ .

Use following settings for the programming of the TIA:

**Figure 30:**  
TIA Programming Settings

pd_ampres	pd12341	pd_ampcap	pd_ampcomp	pd_ampvo	Gain
1	1 ...4	13	1	15	1V/μA
2	1 ...4	7	1	15	2V/μA
3	1 ...4	5	1	15	3V/μA
4	1 ...2	2	0	15	5V/μA
	3 ...4	3			
5	1 ...2	2	0	15	7V/μA
	3 ...4	3			
6	1	1	0	15	10V/μA
	2 ...4	2			
7	1 ...2	1	0	15	15V/μA
	3 ...4	2			
<b>Low Bandwidth Mode</b>					
5	1 ...4	31	3	15	7V/μA
<b>Integrating Mode (pd_ampres=0)</b>					
0	1 ...4	10	3	15	1V/pQ
0	1 ...4	20	3	15	1/2V/pQ
0	1 ...4	30	3	15	1/3V/pQ

**Note(s):**

1. pd1234: number of active photodiodes (for example, pd1=1, pd2=0, pd3=1, pd4=0 -> pd1234=2).

### Photodiode TIA Registers

**Figure 31:**  
PD\_AMPRCCFG Register

0x1d: PD_AMPRCCFG					
Field	Name	Rst	Type	Description	
7:5	pd_ampres	0	RW	Feedback resistor	
				<b>Setting</b>	<b>Resistance</b>
				0	No resistor in feedback of amplifier – photocurrent integrator
				1	1MΩ
				2	2MΩ
				3	3MΩ
				4	5MΩ
				5	7MΩ
				6	10MΩ
7	15MΩ				
4:0	pd_ampcap	0	RW	Feedback capacitor	

The PD\_AMPCFG register is used to configure the operating mode of the photoamplifier.

**Figure 32:**  
PD\_AMPCFG Register

0x1e: PD_AMPCFG				
Field	Name	Rst	Type	Description
7	pd_amp_en	0	RW	0 ... Activates power down mode of photo-amplifier 1 ... Enables photo-amplifier (direct or automatic pd_amp_auto mode) also set en_bias_ofe=1
6	pd_amp_auto	0	RW	0 ... Normal TIA mode 1 ... Enable TIA only when seq_itg is set (i.e. controlled by sequencer itg setting) also set en_bias_ofe=1
5:2	pd_ampvo	15	RW	OpAmp offset. Can be used to limit signal in darkness and to shorten rise times
1:0	pd_ampcomp	3	RW	OpAmp compensation, depending on gain and number of used photo diodes Capacitor = pd_ampcap*0.1 pF

**Figure 33:**  
**PD\_THRESHCFG Register**

0x1f: PD_THRESHCFG				
Field	Name	Rst	Type	Description
7:4	pd_clipdetect_h_thresh	0	RW	If the voltage on the output of the TIA exceed this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as 0 ... 1824mV 1 ... 1748mV 2 ... 1672mV 3 ... 1596mV 4 ... 1520mV 5 ... 1444mV 6 ... 1368mV 7 ... 1292mV 8 ... 1216mV 9 ... 1140mV 10 ... 1064mV 11 ... 988mV 12 ... 912mV 13 ... 836mV 14 ... 760mV 15 ... 684mV
3:0	pd_clipdetect_l_thresh	0	RW	If the voltage on the output of the TIA falls below this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as 0 ... 67mV 1 ... 143mV 2 ... 219mV 3 ... 295mV 4 ... 371mV 5 ... 447mV 6 ... 523mV 7 ... 599mV 8 ... 675mV 9 ... 751mV 10 ... 827mV 11 ... 903mV 12 ... 979mV 13 ... 1055mV 14 ... 1131mV 15 ... 1207mV



### Voltage Mode of the Photodiode Amplifier

The output voltage of the photodiode amplifier is depending on the feedback component:

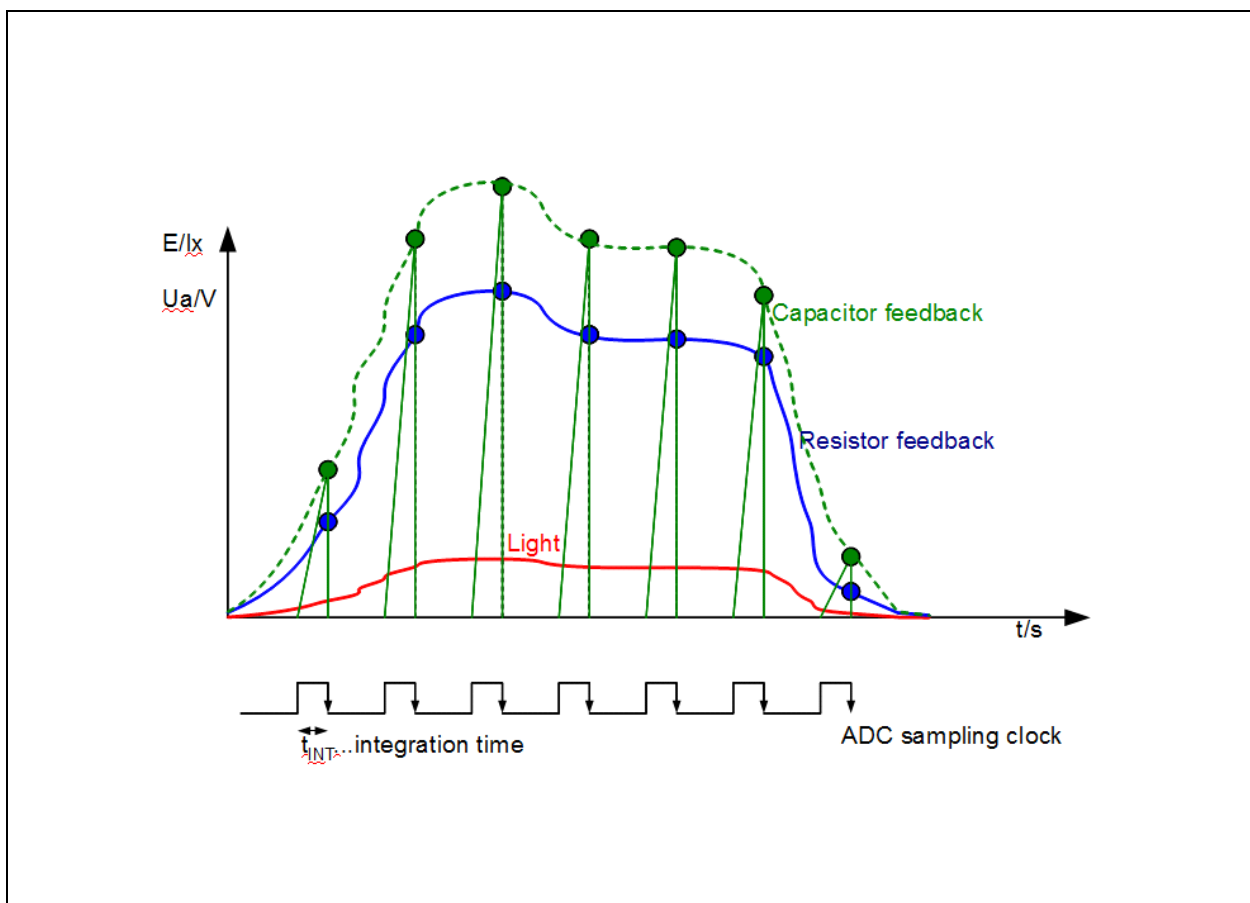
(EQ1) Feedback resistor:  $U_{out} = I_{photo} \cdot R_{fb}$

(EQ2) Feedback capacitor:  $U_{out} = I_{photo} \cdot \frac{t_{INT}}{C_{fb}}$

**Note(s):** The integration time  $t_{INT}$  is defined either by the sequencer ( $man\_mode=0$ ) or manually through the bit  $sw\_itg$  if  $man\_mode=1$ .

For the synchronous demodulator only use the resistive feedback.

**Figure 34:**  
Difference Between Resistive and Capacitive Feedback



With reference to [Figure 34](#),

- **Green:** Capacitive Integration
- **Green Dotted:** Effective Value from Capacitive Mode
- **Blue:** Resistive Feedback
- **Red:** Light Intensity

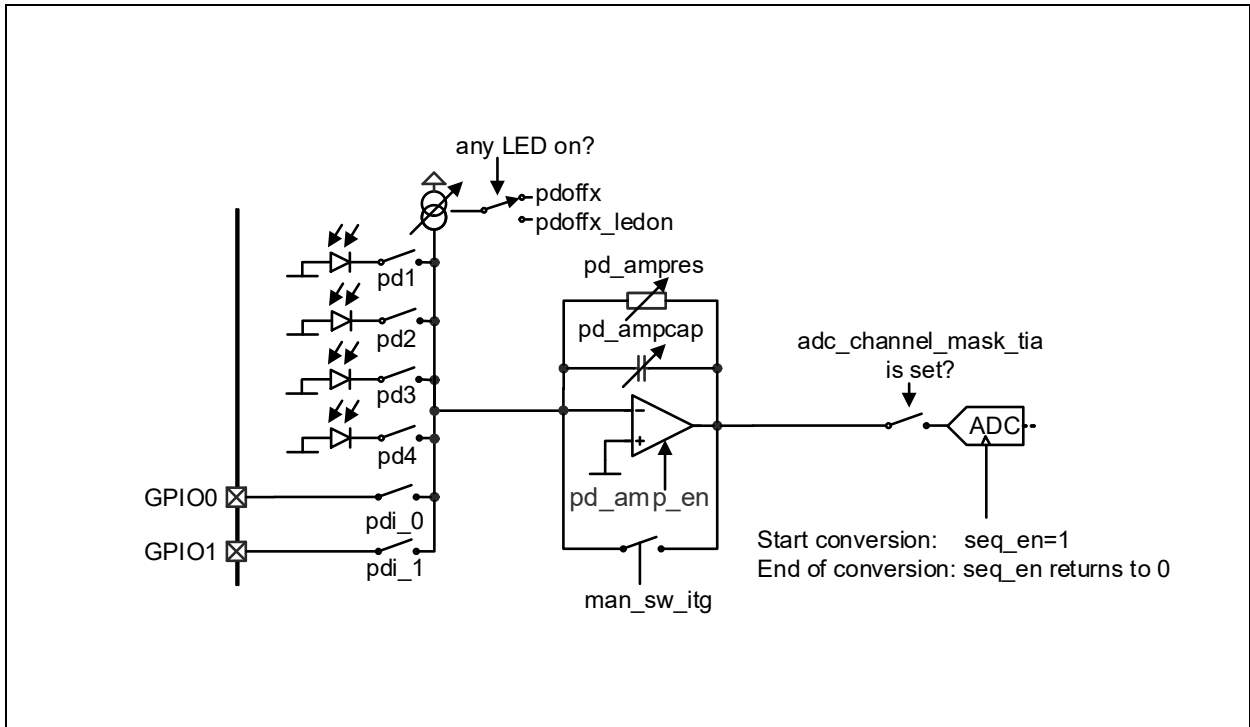
### Optical Front End Operating Modes

Once the photodiode amplifier is configured the measurement can be done in two different ways. Either the LED-outputs, the photodiode amplifier and the ADC are controlled manually by means of register bits, or they are controlled by a built in sequencer.

#### Manual Operation of the Optical Frontend:

The optical front end can be manually controlled via the register `man_mode=1`

**Figure 35:**  
Manual Operation of the Optical Frontend and LED <sup>(1)</sup>



**Note(s):**

- 1. Applies only if `man_mode=1`

For manual operation of the LEDs and its current sinks see [LED-Driver](#).

### Sequencer

In order to synchronize the LED-currents, the integration time and the ADC-sampling time, a built in sampling Sequencers can be used. The sequencer generates the 8 bit-timings based on a 1  $\mu$ s clock which can be pre-scaled with seq\_div. The results of the analog to digital conversion are automatically stored in a pipeline buffer or in register adc\_data and the ADC FIFO.

The timings can be programmed with following registers (apply for man\_mode=0):

**Figure 36:**  
Sequencer Control Registers Overview

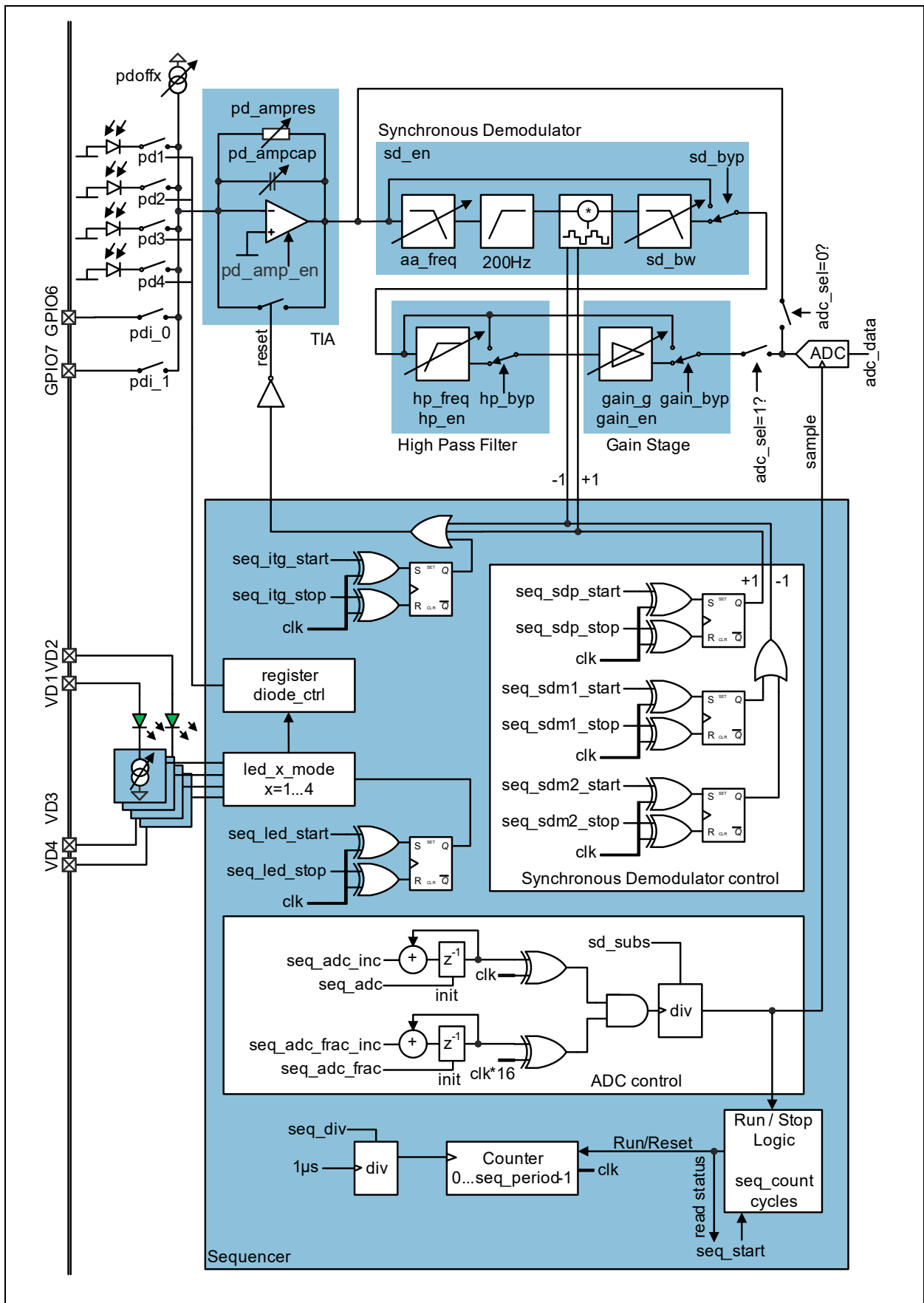
Register	Description
seq_div	Divider of the 1 $\mu$ s input clock for all sequencer timings
seq_count	Number of measurements in one sequence
seq_start	Writing 1 starts the sequencer, 0 stops the sequencer
seq_period	Time of one measurement cycle
seq_led_start	Start time of the LED drivers within one cycle
seq_led_stop	Stop time of the LED drivers within one cycle
seq_secled_start	Start time of the secondary LED drivers within one cycle (used for SpO2)
seq_secled_stop	Stop time of the secondary LED drivers within one cycle (used for SpO2)
seq_itg_start	Start time of the integrator
seq_itg_stop	Stop time of the integrator
seq_sdp1_start	Start time of the synchronous demodulator's 1 positive multiplication
seq_sdp1_stop	Stop time of the synchronous demodulator's 1 positive multiplication
seq_sdm1_start	Start time of the synchronous demodulator's 1 negative multiplication
seq_sdm1_stop	Stop time of the synchronous demodulator's 1 negative multiplication
seq_sdp2_start	Start time of the synchronous demodulator's 2 positive multiplication
seq_sdp2_stop	Stop time of the synchronous demodulator's 2 positive multiplication
seq_sdm2_start	Start time of the synchronous demodulator's 2 negative multiplication
seq_sdm2_stop	Stop time of the synchronous demodulator's 2 negative multiplication
seq_adc	Sampling position of the ADC

Register	Description
seq_adc2tia, seq_adc3tia	If the TIA channel is selected allow a second (and third) conversion within this cycle.
sd_subs, sd_subs_always	Synchronous demodulator subsampling ratio between sequencer frequency and ADC sampling frequency.
ulp	Ultra low power bit for the sequencer. If this bit is set and sd_subs>0, it disables the LED pulses and powers off the TIA in all sequences but the one where the TIA is sampled. This bit can be used to optimize the power consumption of the LEDs and the AS7024 <sup>(2)</sup> .
irq_adc_timing_error	The sequencer setup caused a timing error on ADC conversion.

**Note(s):**

1. The lowest data value of all registers except seq\_count and seq\_div is 1.
2. This bit is located in register ADC\_CFGB bit 1.

**Figure 37:**  
**Block Diagram of Sequencer**



**Sequencer Registers**

**Figure 38:**  
SEQ\_CNT Register

0x30: SEQ_CNT				
Field	Name	Rst	Type	Description
7:0	seq_count	0	RW	Number of measurements in one sequence. If seq_count = 0x0 the sequencer is running continuously if started by seq_start=1 or seq_start_sync=1. This register is reset by disabling/enabling of seq_start=0 (but not by osc_off=1)

The SEQ\_DIV register sets the input divider for the main clock.

**Figure 39:**  
SEQ\_DIV Register

0x31: SEQ_DIV				
Field	Name	Rst	Type	Description
7:0	seq_div	0	RW	Divider value Sequencer time increment $t_{clk} = (seq\_div + 1) * 1\mu s$

**Figure 40:**  
SEQ\_START Register

0x32: SEQ_START				
Field	Name	Rst	Type	Description
1	seq_start_sync	0	R_PUSH	Similar to seq_start, but the sequencer will wait for overflow of the frequency divider that feeds all the switched-cap filters. This means 1) that it could take anything between 0 and 8ms before the sequencer actually starts. And 2) That the generated frequencies are in phase with the sequencer. For this to have any effect, the sequencer period should be selected with the selected frequencies (sd_bw, hp_freq) in mind.
0	seq_start	0	R_PUSH	Writing 1 starts the sequencer(s) in the according to the configuration and upon rising edge of seq_start ADC selects first channel. Writing 0 stops the sequencer(s). In manual mode, writing 1 starts one ADC conversion but does not initialize the ADC channel selection. Reading returns 1 if the sequencer is running (sequencer mode), respectively if the ADC is converting (manual mode)

With the SEQ\_START register sets the configured sequencer can be started

**Figure 41:**  
SEQ\_PER Register

0x33: SEQ_PER				
Field	Name	Rst	Type	Description
7:0	seq_period	0	RW	t_period Sequencer period $T = t\_period * (seq\_div+1) * 1\mu s$

The SEQ\_PER register sets one measurement cycle of the sequencer.

**Figure 42:**  
SEQ\_LED\_STA Register

0x34: SEQ_LED_STA				
Field	Name	Rst	Type	Description
7:0	seq_led_start	0	RW	LED start time

The SEQ\_LED register sets the LED drive timing. Data is stored as 16-bit value.

**Figure 43:**  
SEQ\_LED\_STO Register

0x35: SEQ_LED_STO				
Field	Name	Rst	Type	Description
7:0	seq_led_stop	0	RW	LED stop time

**Figure 44:**  
SEQ\_SECLED\_STA Register

0x36: SEQ_SECLED_STA				
Field	Name	Rst	Type	Description
7:0	seq_secled_start	0	RW	Secondary LED start time

The SEQ\_LED register sets the secondary LED drive timing which is used in ledX\_mode 6 only. Data is stored as 16-bit value.

**Figure 45:**  
SEQ\_SECLED\_STO Register

0x37: SEQ_SECLED_STO				
Field	Name	Rst	Type	Description
7:0	seq_secled_stop	0	RW	Secondary LED stop time

**Figure 46:**  
SEQ\_ITG\_STA Register

0x38: SEQ_ITG_STA				
Field	Name	Rst	Type	Description
7:0	seq_itg_start	1	RW	Integrator start time (start time=1 and stop time=0 means that it's - by default - always ON) Turning OFF the integrator actually means discharge the capacitor. This is only useful in capacitive integration mode, without the synchronous demodulator.

The SEQ\_ITG register sets the photoamplifier integration time. Data is stored as 16-bit value.

**Figure 47:**  
SEQ\_ITG\_STO Register

0x39: SEQ_ITG_STO				
Field	Name	Rst	Type	Description
7:0	seq_itg_stop	0	RW	Integrator stop time

**Figure 48:**  
SEQ\_SDP1\_STA Register

0x3a: SEQ_SDP1_STA				
Field	Name	Rst	Type	Description
7:0	seq_sdp1_start	0	RW	Positive multiplication start time 1



The SEQ\_SDP register sets the synchronous demodulator positive multiplication time. Data is stored as 16-bit value.

**Figure 49:**  
SEQ\_SDP1\_STO Register

0x3b: SEQ_SDP1_STO				
Field	Name	Rst	Type	Description
7:0	seq_sdp1_stop	0	RW	Positive multiplication stop time 1

**Figure 50:**  
SEQ\_SDP2\_STA Register

0x3c: SEQ_SDP2_STA				
Field	Name	Rst	Type	Description
7:0	seq_sdp2_start	0	RW	Positive multiplication start time 2

The SEQ\_SDP register sets the synchronous demodulator positive multiplication time. Data is stored as 16-bit value

**Figure 51:**  
SEQ\_SDP2\_STO Register

0x3d: SEQ_SDP2_STO				
Field	Name	Rst	Type	Description
7:0	seq_sdp2_stop	0	RW	Positive multiplication stop time 2

**Figure 52:**  
SEQ\_SDM1\_STA Register

0x3e: SEQ_SDM1_STA				
Field	Name	Rst	Type	Description
7:0	seq_sdm1_start	0	RW	Negative multiplication start time 1

The SEQ\_SDM1 register sets the synchronous demodulator negative multiplication time 1. Data is stored as 16-bit value

**Figure 53:**  
SEQ\_SDM1\_STO Register

0x3f: SEQ_SDM1_STO				
Field	Name	Rst	Type	Description
7:0	seq_sdm1_stop	0	RW	Negative multiplication stop time 1

**Figure 54:**  
SEQ\_SDM2\_STA Register

0x40: SEQ_SDM2_STA				
Field	Name	Rst	Type	Description
7:0	seq_sdm2_start	0	RW	Negative multiplication start time 2

The SEQ\_SDM2 register sets the synchronous demodulator negative multiplication time 2. Data is stored as 16-bit value

**Figure 55:**  
SEQ\_SDM2\_STO Register

0x41: SEQ_SDM2_STO				
Field	Name	Rst	Type	Description
7:0	seq_sdm2_stop	0	RW	Negative multiplication stop time 2

**Figure 56:**  
SEQ\_ADC Register

0x42: SEQ_ADC				
Field	Name	Rst	Type	Description
7:0	seq_adc	0	RW	ADC sampling time The ADC conversion needs to be finished before the sequencer period ends otherwise ADC samples can be lost.

The SEQ\_ADC register defines the time when the ADC starts sampling during each measurement cycle.

**Figure 57:**  
**SEQ\_ADC2TIA Register**

0x43: SEQ_ADC2TIA				
Field	Name	Rst	Type	Description
7:0	seq_adc2tia	0	RW	<p>ADC second sampling time for TIA: If this time is non-zero, an ADC conversion is started at the given cycle, but only if adc_sel is currently selecting TIA. For all other channels, there is only a single ADC conversion executed in the sequencer period.</p> <p>Warning: If non-zero, seq_adc must be non-zero as well, and seq_adc2tia bigger than seq_adc. The difference must be high enough so that the second ADC conversion is started after the first ADC conversion has finished.</p> <p>Also, if the seq_adc2tia features is used, there is the additional restriction that the second ADC conversion has to be finished before the end of the sequencer period.</p>

**Figure 58:**  
**SEQ\_ADC3TIA Register**

0x44: SEQ_ADC3TIA				
Field	Name	Rst	Type	Description
7:0	seq_adc3tia	0	RW	<p>ADC third sampling time for TIA: same as seq_adc2tia. Also must make sure to not overlap ADC conversions! Also, adc3tia must be after adc2tia</p>

**Figure 59:**  
**SD\_SUBS Register**

0x45: SD_SUBS				
Field	Name	Rst	Type	Description
7:0	sd_subs	0	RW	<p>Synchronous demodulator subsampling ratio between sequencer frequency and ADC sampling frequency.  <math>ADC-F_{sample} = Sequencer\_Frequency / (sd\_subs + 1)</math>            When setting to 0, then in every sequencer iteration the ADC will run.            When setting to 1, then the first sequencer iteration will not trigger the ADC, but the second one will.            Setting to N will make N iterations without ADC, followed by one iteration with the ADC measurement executed.            It is recommended to use the ADC interrupt in this case and not the sequencer interrupt.            Also see sd_subs_always which significantly affects this mechanism.</p>

**Figure 60:**  
**SEQ\_CFG Register**

0x46: SEQ_CFG				
Field	Name	Rst	Type	Description
0	sd_subs_always	0	RW	If this bit is asserted, all sequencer periods are subject to subsampling as defined in SD_SUBS. If this bit is zero, then only the first period of an "ADC cycle" is duplicated sd_subs times, all other periods are regular. One "ADC cycle" is the time from the sequence in which adc_sel is pointing to the "smallest" adc channel up and including the sequence of the "largest" adc channel.

**Figure 61:**  
**SEQ\_ERR Register**

0x47: SEQ_ERR				
Field	Name	Rst	Type	Description
7	irq_adc_timing_error	0	SS_WC	The ADC was started by the sequencer (or manually) while it was still converting. This does not flag an interrupt but when playing with the sequencer settings we suggest to check this flag to make sure that there is no problem with the sequencer programming

**Figure 62:**  
**CYC\_COUNTER Register**

0x60: CYC_COUNTER				
Field	Name	Rst	Type	Description
7:0	cycle_counter	0	RO	Current cycle counter value

The SEQ\_COUNTER register shows the current value of the sequence counter and period counter

**Figure 63:**  
**SEQ\_COUNTER Register**

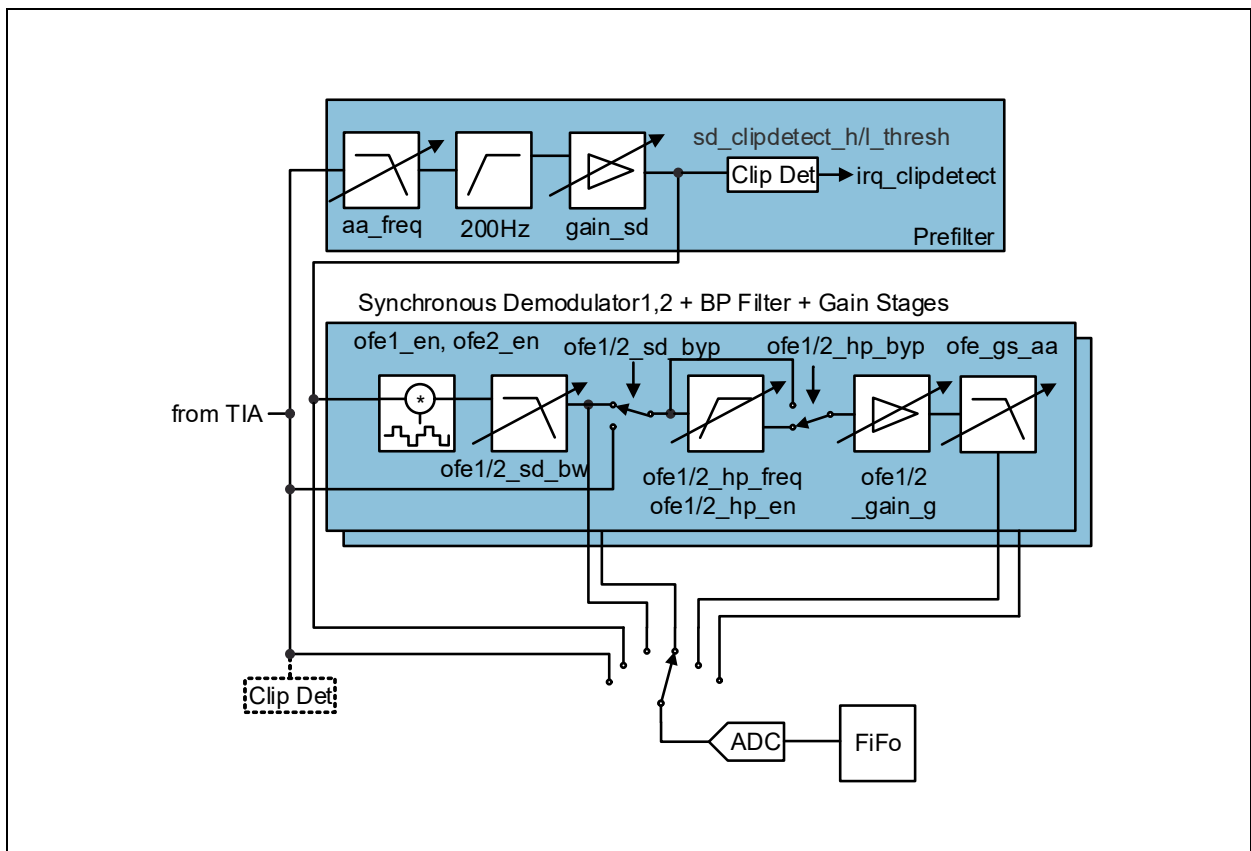
0x61: SEQ_COUNTER				
Field	Name	Rst	Type	Description
7:0	sequence_counter	0	RO	Current sequence counter value

**Figure 64:**  
**SUBS\_COUNTER Register**

0x62: SUBS_COUNTER				
Field	Name	Rst	Type	Description
7:0	subs_counter	0	RO	Current subsampling counter value

## Optical Signal Conditioning

Figure 65:  
Optical Signal Conditioning



### Synchronous Demodulator

Two optional synchronous demodulators can be used to detect small optical signals in the presence of large unwanted noise (ambient light). Since the detector synchronizes to the LED frequency, the demodulator can only be used if the measurement sequencer is running.

It includes an input filter (high pass at 200Hz, adjustable low pass) and a 2nd order adjustable output low pass. The demodulator itself multiplies the signal by +1 / 0 / -1 with a timing which is controlled by the sequencer.

**Note(s):** The optical signal conditioning stage needs `sigref_en=1` for operation.

### High Pass Filter

Two optional high pass filters can be used to remove unwanted DC-components from the signal and allow further amplification. In order to guarantee fast settling times of the filter, four cutoff frequencies can be chosen.

### Gain Stage

Two optional gain stages can be used to amplify the signal after the DC-component has been removed.

**Optical Signal Conditioning Registers**

**Figure 66:**  
**OFE\_CFGA Register**

0x50: OFE_CFGA					
Field	Name	Rst	Type	Description	
7	ofe2_en	0	RW	Enable OFE2	
6	ofe1_en	0	RW	Enable OFE1	
5	en_bias_ofe	0	RW	Enable bias for OFE and TIA	
4:3	aa_freq	0	RW	Anti-aliasing filter cut-OFF frequency	
				<b>Setting</b>	<b>Signal</b>
				0	10kHz
				1	20kHz
				2	40kHz
2:0	gain_sd	0	RW	SD gain	
				<b>Setting</b>	<b>Nominal Gain</b>
				0	1
				1	2
				2	4
				3	8
				4	16
				5	32
				6	64
				7	reserved

**Figure 67:**  
**OFE\_CFGB Register**

0x51: OFE_CFGB				
Field	Name	Rst	Type	Description
7:4	sd_clipdetect_h_thresh	0	RW	If the voltage on the output of the gain_sd stage (input of synchronous demodulator) exceed this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as: 0 ... 1824mV 1 ... 1748mV 2 ... 1672mV 3 ... 1596mV 4 ... 1520mV 5 ... 1444mV 6 ... 1368mV 7 ... 1292mV 8 ... 1216mV 9 ... 1140mV 10 ... 1064mV 11 ... 988mV 12 ... 912mV 13 ... 836mV 14 ... 760mV 15 ... 684mV
3:0	sd_clipdetect_l_thresh	0	RW	If the voltage on the output of the gain_sd stage (input of synchronous demodulator) falls below this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as: 0 ... 67mV 1 ... 143mV 2 ... 219mV 3 ... 295mV 4 ... 371mV 5 ... 447mV 6 ... 523mV 7 ... 599mV 8 ... 675mV 9 ... 751mV 10 ... 827mV 11 ... 903mV 12 ... 979mV 13 ... 1055mV 14 ... 1131mV 15 ... 1207mV



**Figure 68:**  
**OFE\_CFGC Register**

0x52: OFE_CFGC				
Field	Name	Rst	Type	Description
6	prefilter_aa_byp	0	RW	0 ... Anti aliasing filter (aa_filter) is used 1 ... Bypass anti aliasing filter
5	prefilter_hp_byp	0	RW	0 ... Use 200Hz high pass filter 1 ... Bypass 200Hz high pass filter
4	prefilter_gain_byp	0	RW	0 ... Use gain_sd stage 1 ... Bypass gain_sd stage
3	prefilter_bypass_en	0	RW	0 ... Use prefilter unless any of the above register is set 1 ... Bypass complete prefilter
2	prefilter_aa_en	0	RW	0 ... Anti aliasing filter (aa_filter) is OFF 1 ... Anti aliasing filter is ON
1	prefilter_hp_en	0	RW	0 ... 200Hz high pass filter is OFF 1 ... 200Hz high pass filter is ON
0	prefilter_gain_en	0	RW	0 ... gain_sd stage is OFF 1 ... gain_sd stage is ON

**Figure 69:**  
**OFE\_CFGD Register**

0x53: OFE_CFGD					
Field	Name	Rst	Type	Description	
1:0	ofe_gs_aa	0	RW	OFE anti aliasing	
				<b>Setting</b>	<b>Nominal Gain</b>
				0	Bypass
				1	fc=100Hz
				2	fc=300Hz
				3	fc=826Hz

**Figure 70:**  
**OFE1\_CFGA Register**

0x54: OFE1_CFGA				
Field	Name	Rst	Type	Description
7	ofe1_sd_pol_init	0	RW	The low level driver shall ensure that this register is 0 if one of the seq_sdm pulses is first, and is 1 if the seq_sdp is first within a sequence.
6	ofe1_sd_en	0	RW	0 ... Power down of the Synchronous demodulator 1 ... Enable Synchronous demodulator
5	ofe1_hp_en	0	RW	0 ... Power down of the high pass filter 1 ... Enable high pass filter
4	ofe1_gain_en	0	RW	0 ... Power down of the Gain stage 1 ... Enable Gain stage
3	ofe1_sd_byp	0	RW	0 ... Synchronous demodulator is used 1 ... Synchronous demodulator is bypassed
2	ofe1_hp_byp	0	RW	0 ... HP filter is used 1 ... HP filter is bypassed
1	ofe1_gain_byp	0	RW	0 ... Gain stage is used 1 ... Gain stage is bypassed
0	ofe1_sd_hld	0	RW	SD hold 0 ... Output of synchronous demodulator is forced to SIGREF if not set to +1 or -1 1... Output of synchronous demodulator is tristated if not set to +1 or -1

**Figure 71:**  
**OFE1\_CFGB Register**

0x55: OFE1_CFGB					
Field	Name	Rst	Type	Description	
6:4	ofe1_gain_g	0	RW	Gain	
				<b>Setting</b>	<b>Gain</b>
				0	1
				1	2
				2	4
				3	8
				4	16
				5	32
				6	64
				7	Do not use
3:2	ofe1_sd_bw	0	RW	Synchronous demodulator low pass filter.	
				<b>Setting</b>	<b>Frequency</b>
				0	10Hz
				1	20Hz
				2	40Hz
1:0	ofe1_hp_freq	0	RW	High pass filter cutoff frequency	
				<b>Setting</b>	<b>Cutoff Frequency</b>
				0	0.33Hz
				1	1.32Hz
				2	5.28Hz
			3	10.56Hz	

**Figure 72:**  
**OFE2\_CFGA Register**

0x58: OFE2_CFGA				
Field	Name	Rst	Type	Description
7	ofe2_sd_pol_init	0	RW	The low level driver shall ensure that this register is 0 if one of the seq_sdm pulses is first, and is 1 if the seq_sdp is first within a sequence.
6	ofe2_sd_en	0	RW	0 ... Power down of the synchronous demodulator 1 ... Enable synchronous demodulator
5	ofe2_hp_en	0	RW	0 ... Power down of the high pass filter 1 ... Enable high pass filter
4	ofe2_gain_en	0	RW	0 ... Power down of the Gain stage 1 ... Enable Gain stage
3	ofe2_sd_byp	0	RW	0 ... Synchronous demodulator is used 1 ... Synchronous demodulator is bypassed
2	ofe2_hp_byp	0	RW	0 ... HP filter is used 1 ... HP filter is bypassed
1	ofe2_gain_byp	0	RW	0 ... Gain stage is used 1 ... Gain stage is bypassed
0	ofe2_sd_hld	0	RW	SD hold 0 ... Output of synchronous demodulator is forced to SIGREF if not set to +1 or -1 1 ... Output of synchronous demodulator is tristated if not set to +1 or -1

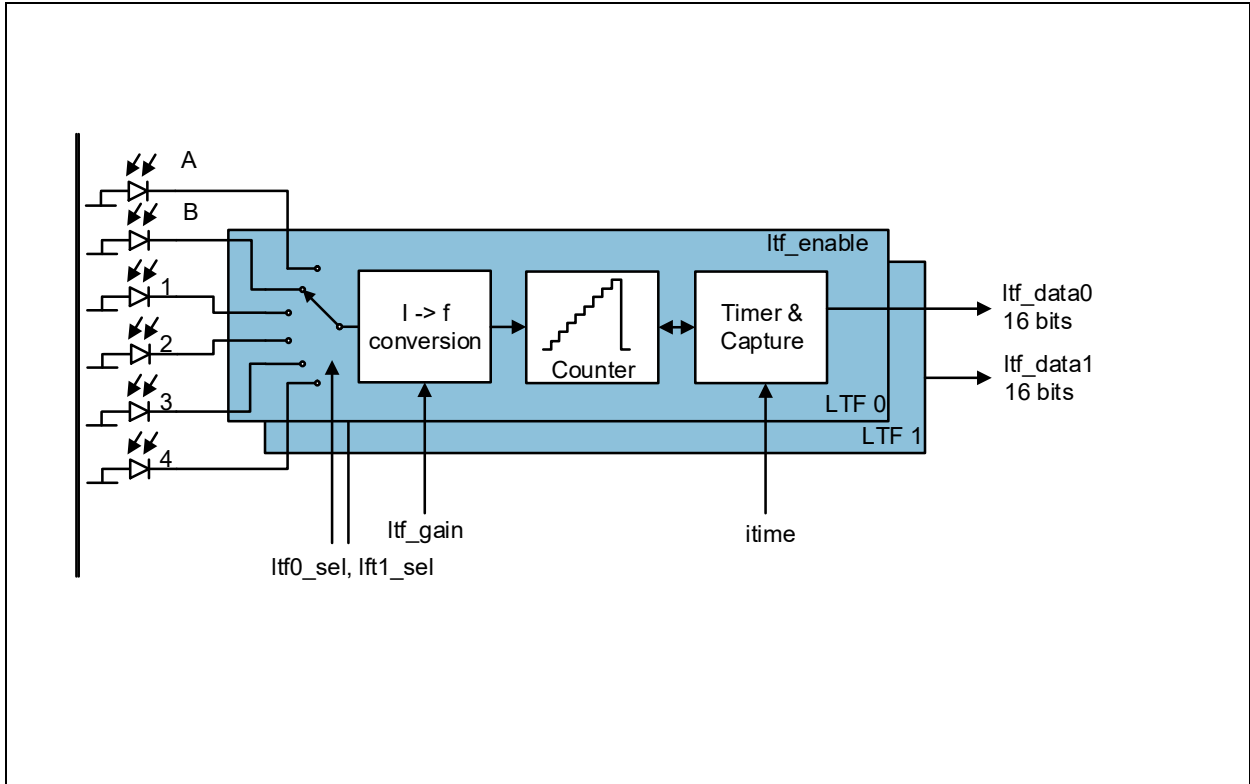
**Figure 73:**  
**OFE2\_CFGB Register**

0x59: OFE2_CFGB					
Field	Name	Rst	Type	Description	
6:4	ofe2_gain_g	0	RW	Gain	
				<b>Setting</b>	<b>Gain</b>
				0	1
				1	2
				2	4
				3	8
				4	16
				5	32
				6	64
				7	Do not use
3:2	ofe2_sd_bw	0	RW	Synchronous demodulator low pass filter.	
				<b>Setting</b>	<b>Frequency</b>
				0	10Hz
				1	20Hz
				2	40Hz
1:0	ofe2_hp_freq	0	RW	High pass filter cutoff frequency	
				<b>Setting</b>	<b>Cutoff Frequency</b>
				0	0.33Hz
				1	1.32Hz
				2	5.28Hz
	3	10.56Hz			

### Light-to-Frequency Mode

The LTF (light-to-frequency, or FM, frequency mode) mode.

**Figure 74:**  
Light-to-Frequency Mode Internal Circuit



**Note(s):**

1. Do not use diodes which are connected to the TIA (register pd\_a, pd\_b, pd1...4) at the same time when lft\_en is enabled on the same diode.

**Light-to-Frequency Mode Registers****Figure 75:**  
**LTFDATA0\_L Register**

0x20: LTFDATA0_L				
Field	Name	Rst	Type	Description
7:0	ltfdata0[7:0]	0	RO	LTF result channel 0 low byte. Software must make sure that the LTF integration is not running when accessing the LTFDATA registers. These are the direct counter registers, they are not latched. If buffering is required, consider using FIFO mode.

**Figure 76:**  
**LTFDATA0\_H Register**

0x21: LTFDATA0_H				
Field	Name	Rst	Type	Description
7:0	ltfdata0[15:8]	0	RO	LTF result channel 0 high byte

**Figure 77:**  
**LTFDATA1\_L Register**

0x22: LTFDATA1_L				
Field	Name	Rst	Type	Description
7:0	ltfdata1[7:0]	0	RO	LTF result channel 1 low byte. Software must make sure that the LTF integration is not running when accessing the LTFDATA registers. If buffering is required, consider using FIFO mode.

**Figure 78:**  
**LTFDATA1\_H Register**

0x23: LTFDATA1_H				
Field	Name	Rst	Type	Description
7:0	ltfdata1[15:8]	0	RO	LTF result channel 1 high byte

**Figure 79:**  
ITIME Register

0x24: ITIME				
Field	Name	Rst	Type	Description
7:0	itime	0	RW	<p>LTF integration time. MODCLK is 2/3MHz (666.67kHz). One LSB of itime is 3.072ms (2048 MODCLK cycles). 0=3.072ms</p> <p>...</p> <p>255=786.432ms</p> <p>Using the itime_unit register (see below), the unit of itime can be reduced by 2, 4, or 8. This shorter integration times can be selected (required for flicker detection), but it can also be used to increase the resolution of itime. For example, if 50ms integration time are desired, the best value for regular itime would be 15 (=16 periods=49.152ms). However, but setting itime_unit=2 (LSB=768μs), one can select 64 (=65 periods=49.9ms)</p> <p>Warning: selecting an integration time smaller than 3.072ms will reduce the resolution of the conversion, as the maximum Itfdata value is not 1024 (10 bits) anymore, but 512 (9 bits) in case of 1.536ms integration time, 256 (8 bits) for 768μs and 128 (7 bits) for 384μs</p>



**Figure 80:**  
**LTF\_CONFIG Register**

0x25: LTF_CONFIG				
Field	Name	Rst	Type	Description
7	infinite_itime	0	RW	If this is asserted, then integration does not stop. The ITIME setting is ignored. Use with watch the ltfdata counters. (Warning: must be filtered in software to prevent inconsistent upper/lower byte). It's implemented as a count disable on the integration counter, so when resetting bit to 0 again, the itime counter will continue and results can be read afterwards through the regular mechanisms (ltfdata or FIFO) This is intended for very long integration times - as the timing is controlled by software/I <sup>2</sup> C, accuracy fully depends on the system and I <sup>2</sup> C master.
6	az_disable_auto	0	RW	0: Run autozero on both channels every time FM mode is activated for the first time after ENAB is being asserted. 1: Do not run autozero automatically. Autozero can only be activated manually (AZ_CONTROL)
5:4	reserved	0	RW	Reserved – leave at 0.
1	ltf_fifo_mode	0	RW	Run LTF integrations back to back, the LTF modulator is running continuously (the modulators are not reset between integrations cycles). After each integration, the result gets written to the FIFO. The FIFO is being filled automatically, FIFO threshold interrupt is flagged as configured. The first item read from the FIFO is from channel 0, the next one from channel 1, etc. Note that there is no ltf_done interrupt triggered after each integration. A FIFO threshold of 1 can be used to generate an interrupt for each result. irq_ltf_enab should be kept asserted to avoid missing an ltf_sat interrupt. Do not enable ADC/sequencer FIFO mode and ltf_fifo_mode at the same time, corrupted data would be the result. Make sure to empty the FIFO in time, if the FIFO is full, new data is not being stored in the FIFO. Source of data read from the FIFO after an overflow condition is undefined (can be from channel 0 or channel 1) Stop the procedure by clearing this bit.
0	ltf_enable	0	RW	This bit must be asserted for any LTF function (powers up the LTF clock tree)

**Figure 81:**  
LTF\_SEL Register

0x26: LTF_SEL					
Field	Name	Rst	Type	Description	
6:4	ltf1_sel	2	RW	Select the sensor diode for LTF1	
				<b>Setting</b>	<b>Source</b>
				0	A
				1	A/16
				2	B
				3	B/16
				4	PD1
				5	PD2
				6	PD3
				7	PD4
2:0	ltf0_sel	0	RW	Select the sensor diode for LTF0	
				<b>Setting</b>	<b>Source</b>
				0	A
				1	A/16
				2	B
				3	B/16
				4	PD1
				5	PD2
				6	PD3
				7	PD4

**Figure 82:**  
LTF\_GAIN Register

0x27: LTF_GAIN					
Field	Name	Rst	Type	Description	
5:4	itime_unit	0	RW	Select the itime unit. See itime register description.	
				<b>Setting</b>	<b>Behavior</b>
				0	Normal, time LSB=3.072ms
				1	/2, LSB=1.536ms
				2	/4, time LSB=768μs
				3	/8, time LSB=384μs
3:0	ltf_gain	0	RW	Select the gain	
				<b>Setting</b>	<b>Gain</b>
				0	0.25
				1	0.5
				2	1
				3	2
				4	4
				5	8
				6	16
				7	32
				8	64
				9-15	Reserved – do not use

**Figure 83:**  
LTF\_CONTROL Register

0x28: LTF_CONTROL				
Field	Name	Rst	Type	Description
0	ltf_start	0	R_PUSH	Writing 1 starts the counter, and it will run for the specified time (itime). Afterwards it stops automatically and interrupt is flagged. writing 0 to the counter stops it as well. reading the value returns whether the counter is running. If ltf_fifo_mode is non-zero, then FM conversions are done continuously until a 0 is written to this bit again.

**Figure 84:**  
AZ\_CONTROL Register

0x29: AZ_CONTROL				
Field	Name	Rst	Type	Description
1	az_enable_1	0	RW_SM	Writing a '1' to this register starts the AZ engine for channel 1. This is usually not necessary, as AZ is executed automatically before the first LTF integration (unless az_disable_auto is set) The bit is cleared to '0' automatically when the AZ has finished. You cannot write a '0' to this register.
0	az_enable_0	0	RW_SM	The same as az_enable_1, but for channel 0.

**Figure 85:**  
OFFSET0 Register

0x2a: OFFSET0				
Field	Name	Rst	Type	Description
7:0	offset0[7:0]	0	RW_SM	This register holds the value of the offset on the channel 0 OpAmp. It can be overwritten, and it gets overwritten by the auto-zero mechanism. The value is in sign/magnitude encoding. The value is $\pm 127$ , sign/magnitude

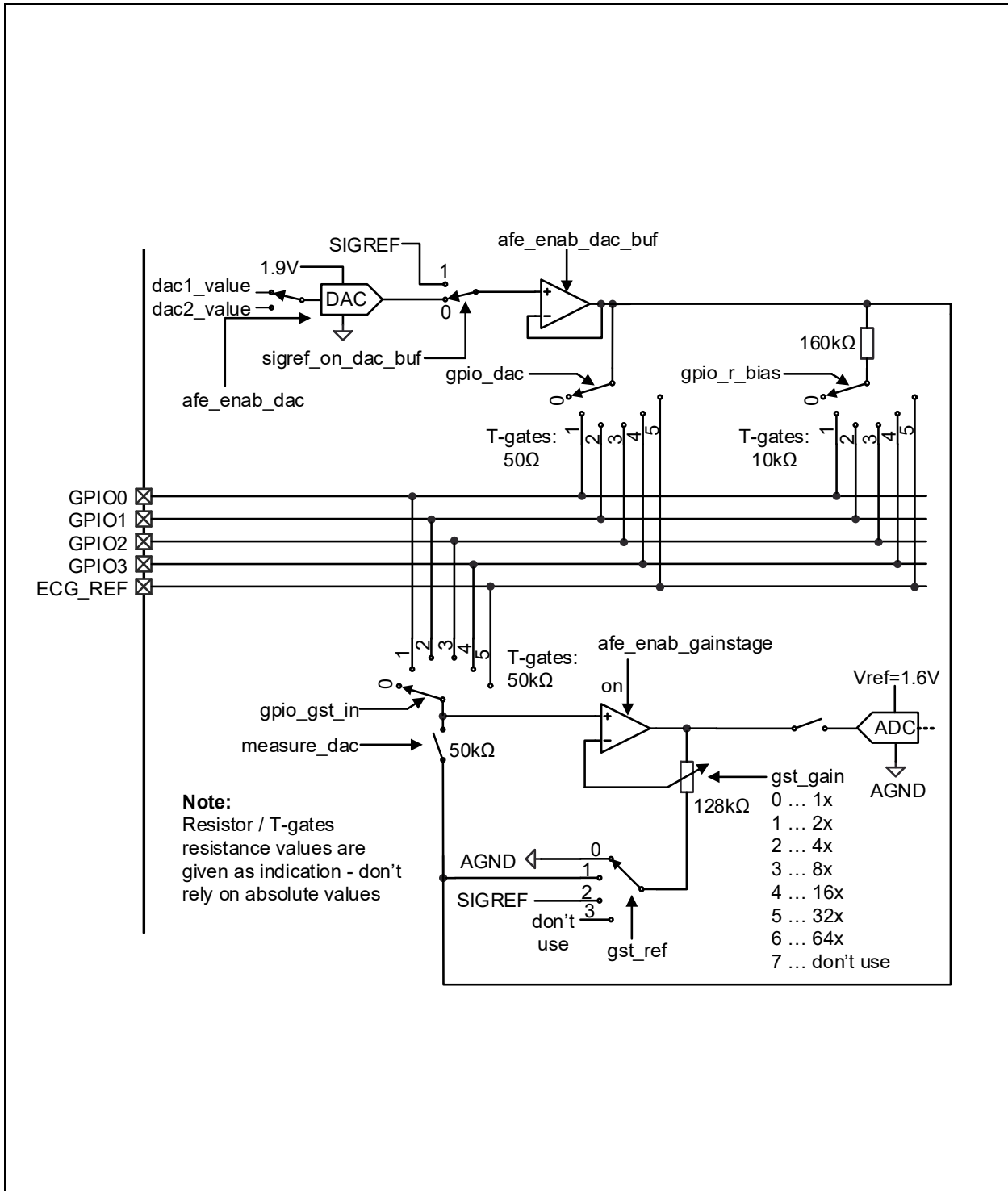
**Figure 86:**  
OFFSET1 Register

0x2b: OFFSET1				
Field	Name	Rst	Type	Description
7:0	offset1[7:0]	0	RW_SM	This register holds the value of the offset on the channel 1 OpAmp. It can be overwritten, and it gets overwritten by the auto-zero mechanism. The value is in sign/magnitude encoding. The value is $\pm 127$ , sign/magnitude

### Electrical Analog Front End

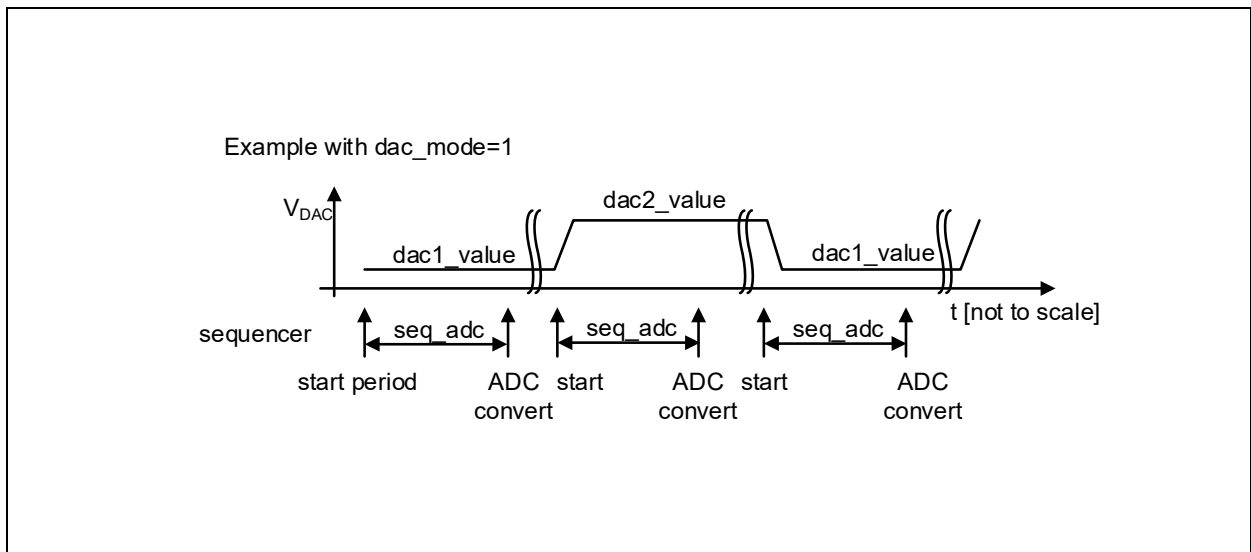
The electrical analog front end consists of three identical signal paths with independent settings of bias condition, gain and offset.

**Figure 87:**  
Electrical Analog Front End Internal Circuit



### DAC Switching

**Figure 88:**  
Electrical Analog Front End DAC Level Switching



If register `dac_mode` is not zero, the DAC switches its codes between `dac1_value` and `dac2_value` on the beginning of every/every 2nd/every 4th sequencer cycle where the ADC is converting the electrical frontend channel. ADC conversions of any other channel do not switch the DAC.

#### Input Pins

Four general purpose pins and `ECG_REF` can be used either as configurable GPIO pin or as analog input pins for the electrical analog front end. The analog inputs can be configured to setup different amplifier topologies.

#### EAF (Electrical Analog Frontend) Registers

**Figure 89:**  
AFE\_CFG Register

0x70: AFE_CFG				
Field	Name	Rst	Type	Description
3	<code>afe_enab</code>	0	RW	0 ... EAF bias deactivated 1 ... EAF bias activated (need to be set for any functions of the EAF are used).
2	<code>afe_enab_dac</code>	0	RW	0 ... DAC inside the EAF OFF 1 ... DAC inside the EAF ON
1	<code>afe_enab_dac_buf</code>	0	RW	0 ... DAC buffer ON 1 ... DAC buffer OFF
0	<code>afe_enab_gainstage</code>	0	RW	0 ... Gain stage in EAF OFF 1 ... Gain stage in EAF ON

The AFE\_CFG register is used to configure the analog frontend.

**Figure 90:**  
EAF\_GST Register

0x80: EAF_GST					
Field	Name	Rst	Type	Description	
7:5	gpio_gst_in	0	RW	Gain stage input selection	
				<b>Setting</b>	<b>Meaning</b>
				0	Not connected
				1	GPIO0
				2	GPIO1
				3	GPIO2
				4	GPIO3
				5	ECG_REF
4:3	gst_ref	0	RW	Gain stage reference voltage	
				<b>Setting</b>	<b>Meaning</b>
				0	AGND
				1	DAC buffer
				2	SIGREF
3	Reserved				
2:0	gst_gain	0	RW	Gain stage gain	
				<b>Setting</b>	<b>Meaning</b>
				0	1
				1	2
				2	4
				3	8
				4	16
				5	32
				6	64
7	Reserved				

The EAF register is used to configure the electrical frontend

**Figure 91:**  
EAF\_BIAS Register

0x81: EAF_BIAS					
Field	Name	Rst	Type	Description	
7:5	gpio_r_bias	0	RW	Resistive biasing	
				<b>Setting</b>	<b>Meaning</b>
				0	No resistive biasing
				1	Resistive biasing on GPIO0
				2	Resistive biasing on GPIO1
				3	Resistive biasing on GPIO2
				4	Resistive biasing on GPIO3
				5	Resistive biasing on ECG_REF

**Figure 92:**  
EAF\_DAC Register

0x82: EAF_DAC					
Field	Name	Rst	Type	Description	
4	sigref_on_dac_buf	0	RW	If asserted, connect SIGREF to DAC buffer.	
3	measure_dac	0	RW	If this bit is asserted, the DAC output is connected to the gain stage input (independent of gpio_gst_in selection, therefore the DAC output is measurable on the GPIO pin)	
2:0	gpio_dac	0	RW	DAC on GPIO	
				<b>Setting</b>	<b>Meaning</b>
				0	No DAC biasing
				1	DAC on GPIO0
				2	DAC on GPIO1
				3	DAC on GPIO2
				4	DAC on GPIO3
5	DAC on ECG_REF				



**Figure 93:**  
EAF\_DAC1\_L Register

0x83: EAF_DAC1_L				
Field	Name	Rst	Type	Description
7:6	dac1_value[1:0]	0	RW	DAC value 1 (2LSB)

The EAF\_DAC1/2\_L/H registers is used to configure the dac value. See register dac\_mode for selection of dac register 1 or 2.

**Figure 94:**  
EAF\_DAC1\_H Register

0x84: EAF_DAC1_H				
Field	Name	Rst	Type	Description
7:0	dac1_value[9:2]	0	RW	DAC value 1 (upper 8 bits) 10 bit value: 0x000 ... 0V 0x3FF ... 1.9V

**Figure 95:**  
EAF\_DAC2\_L Register

0x85: EAF_DAC2_L				
Field	Name	Rst	Type	Description
7:6	dac2_value[1:0]	0	RW	DAC value 2 (2LSB)

**Figure 96:**  
EAF\_DAC2\_H Register

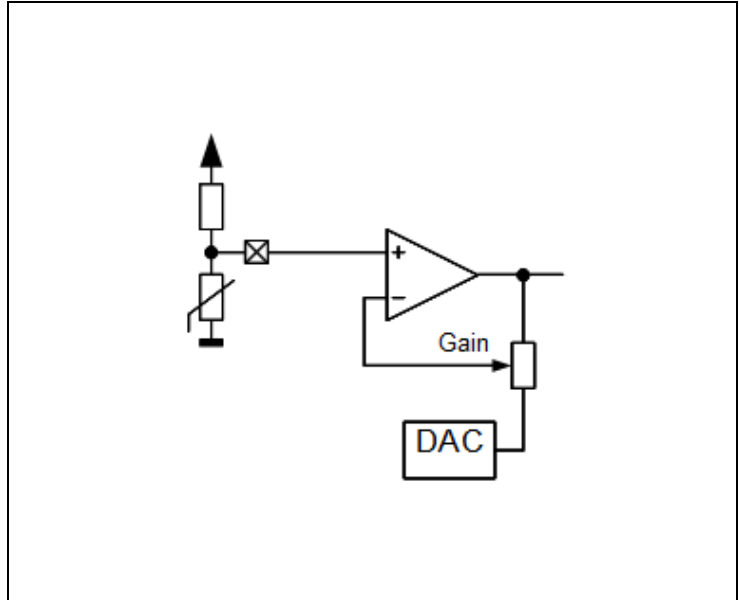
0x86: EAF_DAC2_H				
Field	Name	Rst	Type	Description
7:0	dac2_value[9:2]	0	RW	DAC value 2 (upper 8 bits) 10 bit value: 0x000 ... 0V 0x3FF ... 1.9V

**Figure 97:**  
EAF\_DAC\_CFG Register

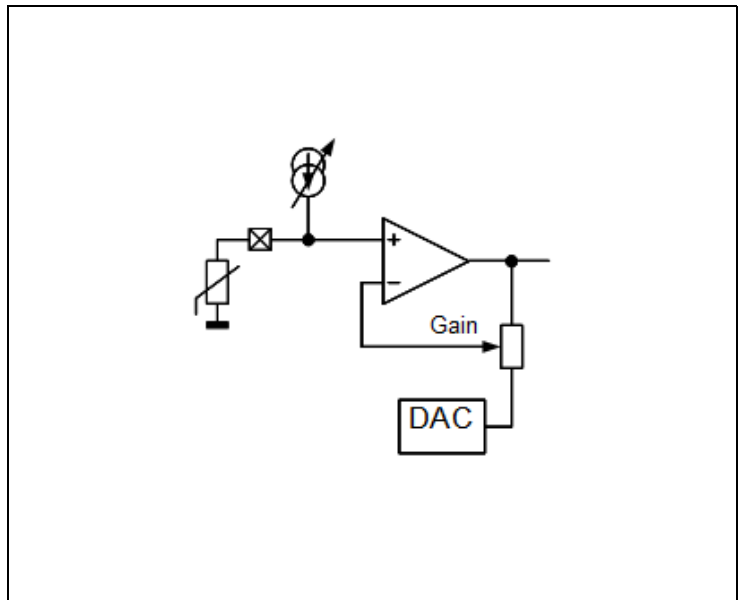
0x87: EAF_DAC_CFG					
Field	Name	Rst	Type	Description	
1:0	dac_mode	0	RW	DAC mode The EAF has a DAC that can be switched out on GPIOs. dac_mode 0 uses statically dac1_value, the other modes switch dynamically between the two values. The system switches from one value to the next always at the beginning of a sequence in which the ADC will sample the AFE channel.	
				<b>Setting</b>	<b>Meaning</b>
				0	1-1-1-1-1-1-1-1-1-1-
				1	1-2-1-2-1-2-1-2-1-2-
				2	1-1-2-2-1-1-2-2-1-1-2-
3	1-1-1-1-2-2-2-2-1-1-1-				

**Possible Configurations of Every Amplifier Stage**

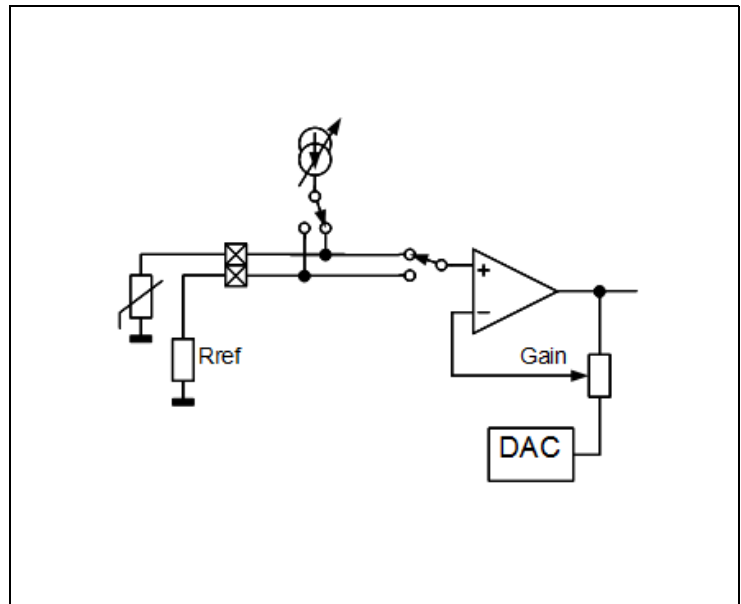
**Figure 98:**  
**Non Inverting Amplifier with Offset and Input Voltage Divider (Temperature Sensor)**



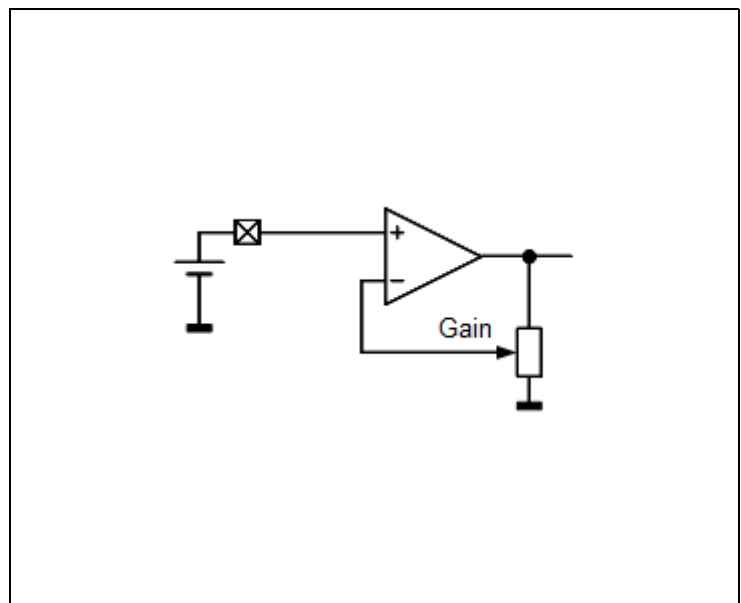
**Figure 99:**  
**Non Inverting Amplifier with Current Source and Offset (Temperature Sensor)**



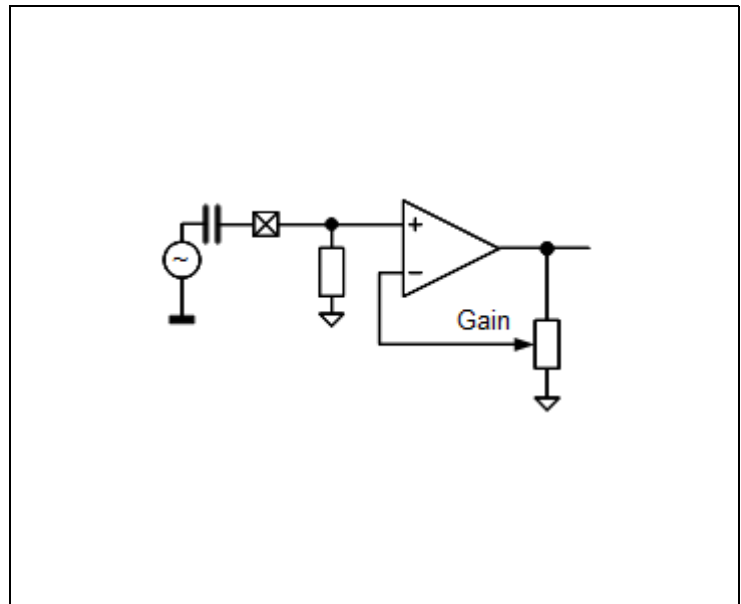
**Figure 100:**  
**Non Inverting Amplifier with Current Source and Reference Path (Temperature Sensor)**



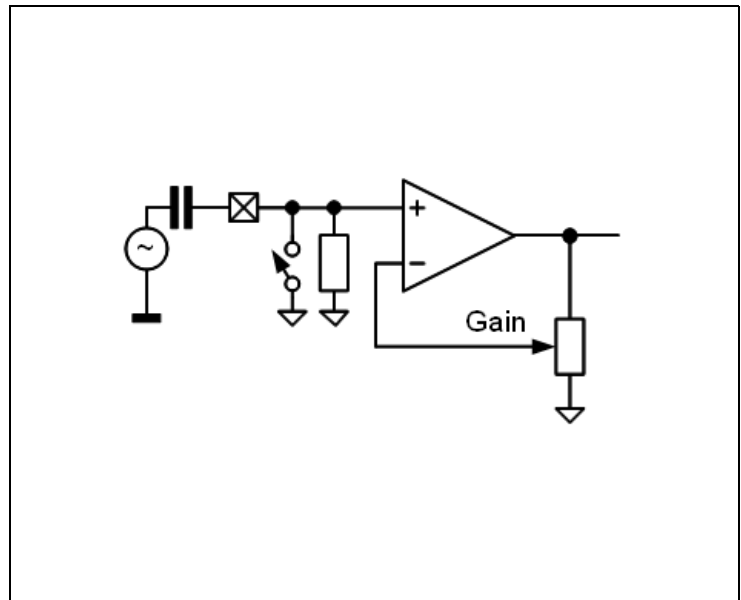
**Figure 101:**  
**Non Inverting Amplifier High Impedance, GND Referenced**



**Figure 102:**  
Non Inverting Amplifier with DC-Blocking, Referenced to  $V_{\text{ADCRef}/2}$

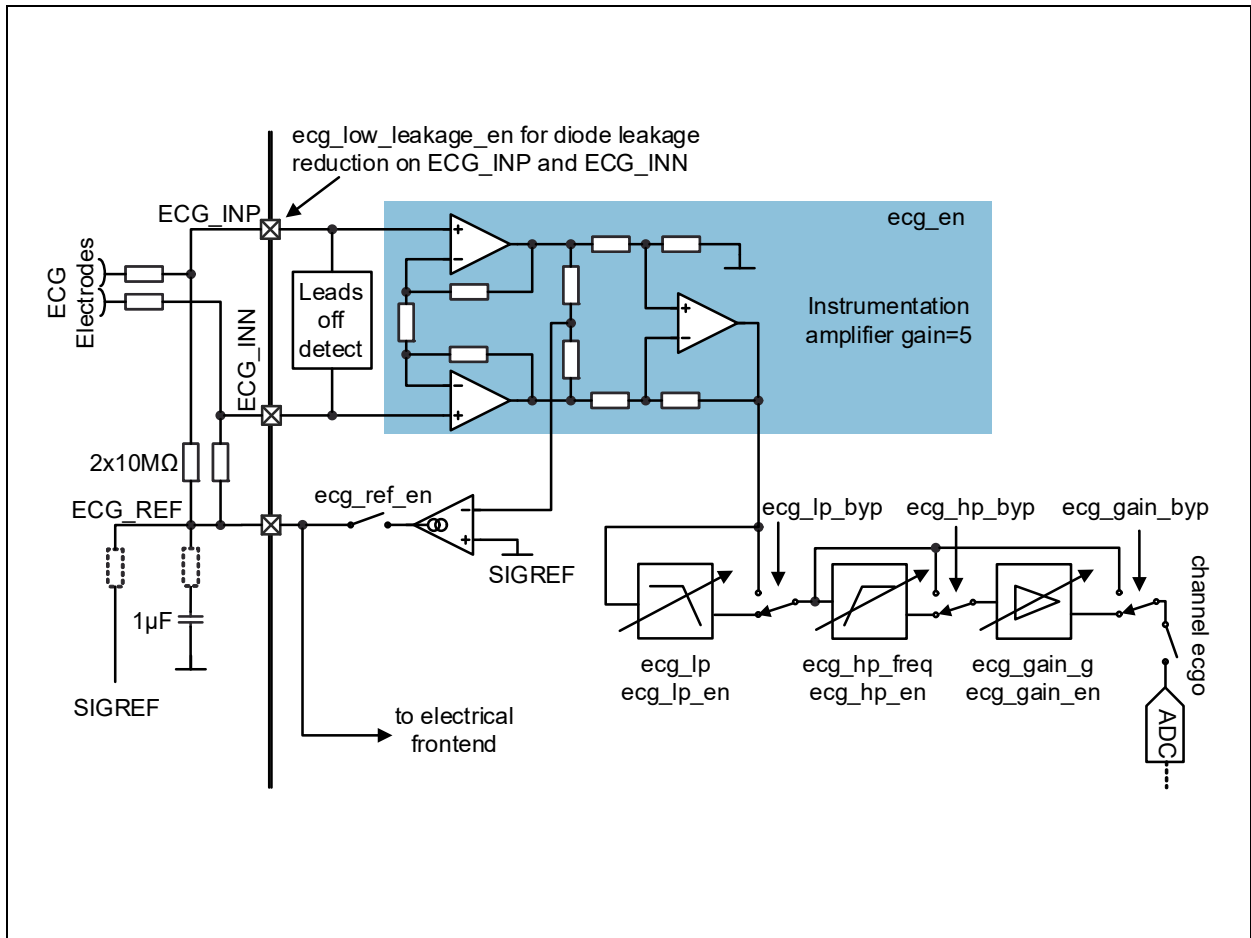


**Figure 103:**  
Non Inverting Amplifier with DC-Blocking and Fast Settling Time, Referenced to  $\text{ADCRef} / 2$



### ECG Amplifier

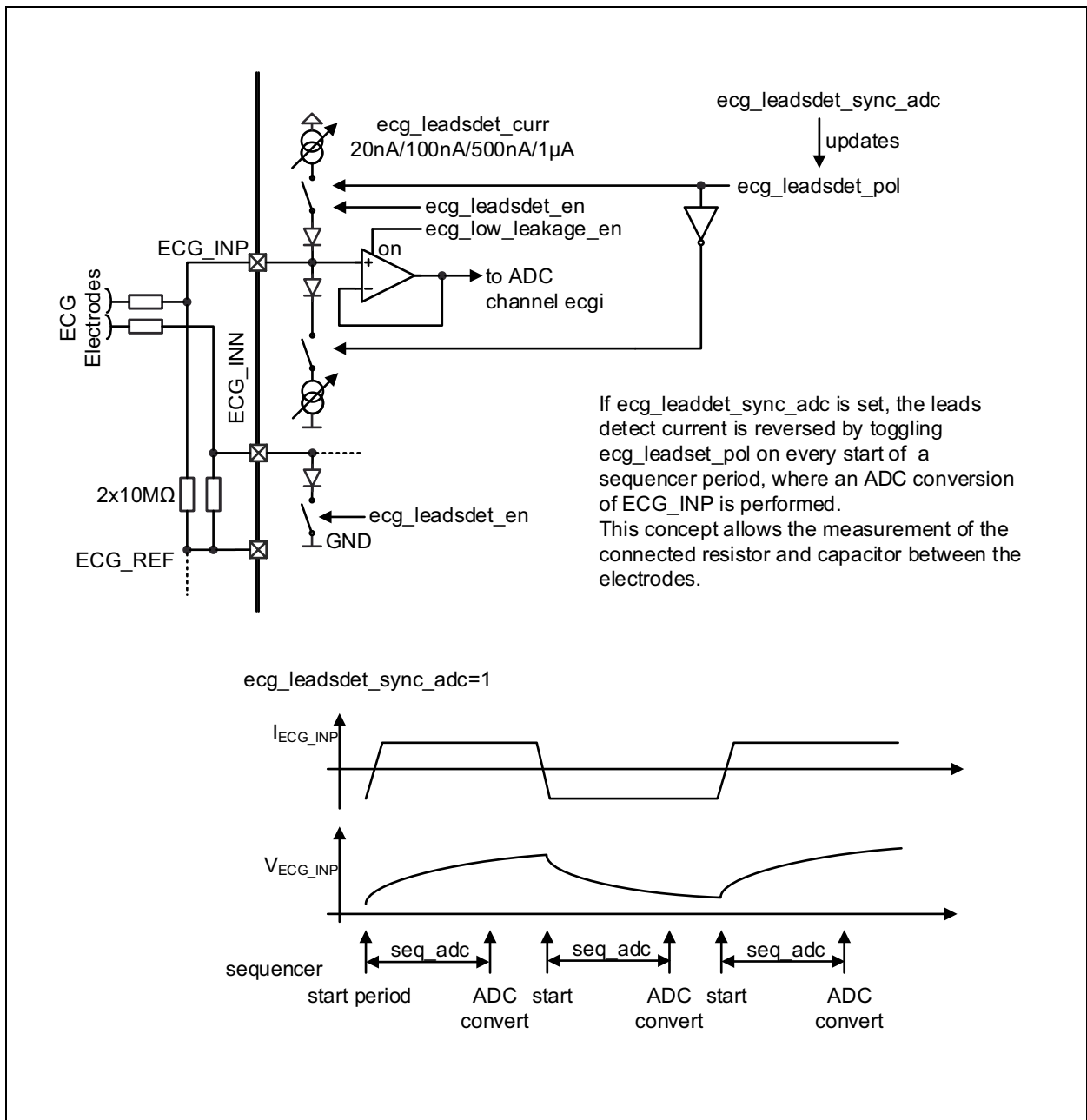
Figure 104:  
ECG Amplifier Internal Circuit



The ECG (electro cardiogram) amplifier is a high impedance, low noise instrumentation amplifier with analog circuitry to bandpass filter the signal and amplify it before converting it with the ADC.

### ECG Lead OFF Detection

**Figure 105:**  
ECG Lead OFF Detection Internal Circuit



The ECG lead OFF detection can be used for detection if the user actually touches the leads. It is a circuitry to measure the capacitor and/or resistance between the two lead inputs ECG\_INP and ECG\_INN.

### ECG Registers

Figure 106:  
ECG\_CFGA Register

0x5c: ECG_CFGA				
Field	Name	Rst	Type	Description
7	ecg_en	0	RW	Enable ECG instrumentation amplifier
6	not used	NA	NA	Do not rely on the content of this register
5	ecg_lp_en	0	RW	0 ... LP filter disabled 1 ... LP filter enabled
4	ecg_hp_en	0	RW	0 ... Power down of the high pass filter 1 ... Enable high pass filter
3	ecg_gain_en	0	RW	0 ... Power down of the Gain stage 1 ... Enable Gain stage
2	ecg_lp_byp	0	RW	0 ... LP stage is used 1 ... LP stage is bypassed
1	ecg_hp_byp	0	RW	0 ... HP filter is used 1 ... HP filter is bypassed
0	ecg_gain_byp	0	RW	0 ... Gain stage is used 1 ... Gain stage is bypassed



**Figure 107:**  
ECG\_CFGB Register

0x5d: ECG_CFGB						
Field	Name	Rst	Type	Description		
6:5	ecg_lp_freq	0	RW	ECG low pass filter.		
				<b>Setting</b>	<b>Frequency</b>	
				0	40Hz	
				1	80Hz	
				2	160Hz	
				3	320Hz	
4:3	ecg_hp_freq	0	RW	High pass filter cutoff frequency		
				<b>Setting</b>	<b>Filter Frequency</b>	<b>Cutoff Frequency</b>
				0	122Hz	0.33Hz
				1	488Hz	1.32Hz
				2	1953Hz	5.28Hz
				3	3906Hz	10.56Hz
2:0	ecg_gain_g	0	RW	Gain		
				<b>Setting</b>	<b>Gain</b>	
				0	1	
				1	2	
				2	4	
				3	8	
				4	16	
				5	32	
				6	64	
				7	128	

**Figure 108:**  
ECG\_CFGC Register

0x5e: ECG_CFGC				
Field	Name	Rst	Type	Description
1	ecg_low_leakage_en	0	RW	Enable ECG leakage compensation
0	ecg_ref_en	0	RW	ECG Reference Feedback Amplifier Enable

**Figure 109:**  
ECG\_CFGD Register

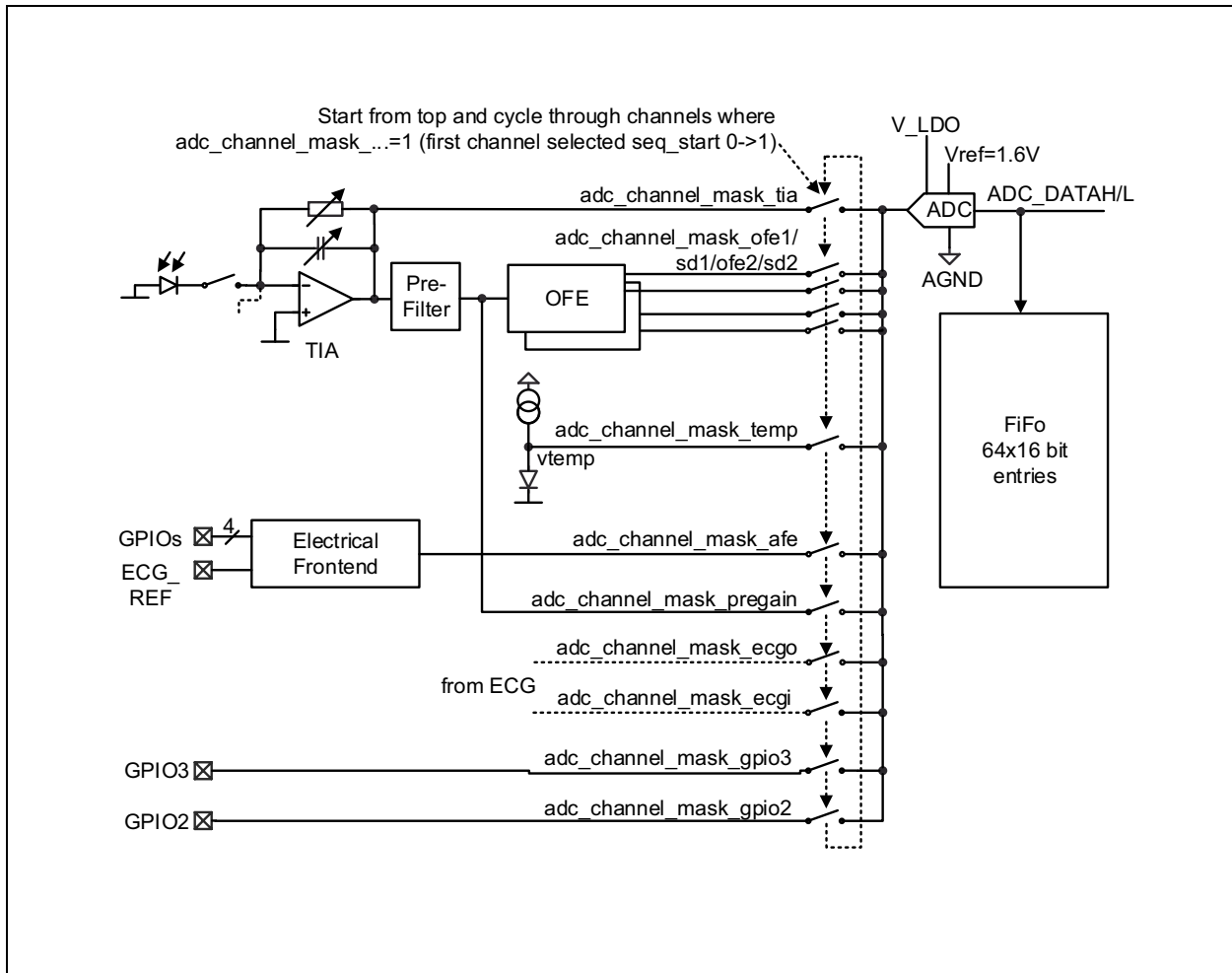
0x5f: ECG_CFGD					
Field	Name	Rst	Type	Description	
4	ecg_leadsdet_sync_adc	0	RW	ECG Leads Detection Automatic Update. If this is asserted, then ecg_leadsdet_pol is inverted automatically at the start of a sequence (at count=2) if in this sequence the ADC will convert the ECGi channel.	
3	ecg_leadsdet_pol	0	RW_SM	ECG Leads Detection Polarity. Can be written to manually if ecg_leadsdet_sync_adc is clear, otherwise it is automatically toggled.	
2:1	ecg_leadsdet_curr	0	RW	ECG Leads Detection Current	
				<b>Setting</b>	<b>Current</b>
				0	20nA
				1	100nA
				2	500nA
3	1μA				
0	ecg_leadsdet_en	0	RW	ECG Leads Detection Enable	

### ADC and FIFO

The ADC is a 14bit successive-approximation register (SAR) type. It supports 14bit with conversion time up to 50ksps.

The ADC is started by the sequencer and its timing or in manual mode (man\_mode=1) by setting seq\_start=1 (seq\_start stays '1' as long as the conversion runs). The AS7024 can be configured to trigger an interrupt upon end of conversion.

**Figure 110:**  
ADC Internal Circuit and Multiplexer



For best accuracy, the ADC can be optionally calibrated.

**Note(s):** If GPIO2 or GPIO3 is used as ADC input, there is no anti-aliasing filter in front of the ADC (needs to be added externally).

### ADC Threshold

At the output of the ADC converter a digital threshold can be enabled. If the output of the ADC exceeds the threshold `adc_threshold`, it triggers an interrupt. This mechanism can be used to identify if an object is in proximity of the sensor and then to interrupt the host. In cases where no object is detected, the host can be sleeping therefore reducing power consumption of the system.

For detailed description of the threshold calculation see the register `ADC_THRESHOLD` and `ADC_THRESHOLD_CFG` description.

### ADC Registers

Figure 111:  
ADC\_THRESHOLD Register

0x68: ADC_THRESHOLD				
Field	Name	Rst	Type	Description
7:0	<code>adc_threshold</code>	0xff	RW	If the ADC returns a value above <code>adc_threshold</code> (not equal), then the <code>adc_threshold</code> interrupt can be triggered. Note that when comparing, only the upper 8 bits are compared, the lower 6 bits are ignored. A value of 0xff can therefore never trigger the interrupt.

Figure 112:  
ADC\_THRESHOLD\_CFG Register

0x69: ADC_THRESHOLD_CFG				
Field	Name	Rst	Type	Description
1	<code>adc_thresh_differential</code>	0	RW	If <code>adc_thresh_tiaonly</code> is asserted and any of <code>seq_adc[23]tia</code> is non-zero, meaning that there are two or three ADC TIA measurements in one sequencer period, then the second is subtracted from the first, and the <i>difference</i> is being compared to the <code>adc_threshold</code> .
0	<code>adc_thresh_tiaonly</code>	0	RW	Normally, the <code>adc_threshold</code> works regardless of the <code>adc</code> channel. If this bit is set, then the threshold is only checked if the <code>adc</code> channel is TIA.

**Figure 113:**  
**ADC\_CFGA Register**

0x88: ADC_CFGA					
Field	Name	Rst	Type	Description	
3:1	adc_multi_n	0	RW	Defines number of samples that are taken in multimode (adc_multimode =1) <sup>(1)</sup>	
				<b>Setting</b>	<b>Number of Samples per ADC Conversion Command</b>
				0	2
				1	4
				2	8
				3	16
				4	32
				5	48
				6	64
7	96				
0	adc_multimode	0	RW	0 ... If ADC is started one sample is measured 1 ... If ADC is started multiple samples are stored in sequence in the FIFO. The number of samples is defined with "adc_multi_n".	

**Note(s):**

1. If the ADC is triggered with the sequencer, the very first ADC conversion after seq\_en=1 stores the number of samples according to above table. All subsequent samples use one sample less (e.g. 7 instead of 8).

The ADC\_CFGA,B,C register is used to configure the ADC operation.

**Figure 114:**  
ADC\_CFGB Register

0x89: ADC_CFGB							
Field	Name	Rst	Type	Description			
5:3	adc_clock	0	RW	ADC clock divider: The ADC clock is freely configurable.			
				<b>Setting</b>	<b>Periods</b>	<b>µs</b>	<b>kHz</b>
				0	2	1	1000
				1	4	2	500
				2	6	3	333
				3	8	4	250
				4	10	5	200
				5	12	6	167
				6	14	7	143
				7	16	8	125
2	adc_calibration	0	RW	To activate the optional self calibration, this bit must be asserted, and an ADC “conversion” has to be started in manual mode (man_mode=1) by asserting seq_start.			
1	ulp	0	RW	Ultra low power bit for the sequencer. If this bit is set and sd_subs>0, it disables the LED pulses and powers off the TIA in all sequences but the one where the TIA is sampled.			
0	adc_en	0	RW	0 ... Reset ADC 1 ... Enable ADC Warning: In reset state the ADC clears its calibration data. Re-calibration is necessary next time it is enabled again.			

**Figure 115:**  
**ADC\_CFGC Register**

0x8a: ADC_CFGC							
Field	Name	Rst	Type	Description			
4	adc_selfpd	1	RW	1 ... Power down the ADC when not converting; use this to conserve power, but set adc_settling_time to minimum 64us to permit settling of the ADC reference buffer. 0 ... Always enable ADC			
3	adc_discharge	1	RW	0: Suppress ADC capacitor discharging – use with caution 1: Discharge ADC capacitor before tracking If asserted, the capacitor is discharged before the tracking phase. If zero, the discharge phase is suppressed and the tracking phase is started one cycle earlier.			
2:0	adc_settling_time	0	RW	ADC settling time: Use with synchronous demodulator. It defines the number of ADC clock cycles the sampling window is kept open additionally. If the gain stage in the optical frontend is used (gain_byp=0), set this to minimum 8µs. If adc_selfpd=1, set this to minimum 64µs.			
				<b>Setting</b>	<b>Periods</b>	<b>µs (@500kHz)</b>	<b>µs (@250kHz)</b>
				0	0	0	0
				1	4	8	16
				2	8	16	32
				3	16	32	64
				4	32	64	128
				5	64	128	256
				6	128	256	512
7	256	512	1ms				

**Figure 116:**  
ADC\_CHANNEL\_MASK\_L Register

0x8b: ADC_CHANNEL_MASK_L				
Field	Name	Rst	Type	Description
7	adc_channel_mask_pregain	0	RW	Pregain channel selection
6	adc_channel_mask_afe	0	RW	Electrical front end
5	adc_channel_mask_temp	0	RW	Temperature measurement
4	adc_channel_mask_sd2	0	RW	Synchronous modulator 2 output just before the gain stage
3	adc_channel_mask_ofe2	0	RW	Synchronous modulator 2 output after the gain stage
2	adc_channel_mask_sd1	0	RW	Synchronous modulator 1 output just before the gain stage
1	adc_channel_mask_ofe1	0	RW	Synchronous modulator 1 output after the gain stage
0	adc_channel_mask_tia	0	RW	Transimpedance amplifier output

The adc channel is chosen automatically from the bits within the adc\_channel\_mask\_\* set. It starts from right and finishes left (LSB->MSB) and wraps back from the most significant asserted bit to the least significant of the asserted bits. After every ADC conversion it switches to the next enabled channel, (except around the adc2tia/adc3tia cases). See register description FIFOH and FIFOL for encoding of the first channel in the data stream.

This applies to both, manual mode and sequencer mode. In sequencer mode, it starts with the smallest channel when the sequencer is being started. In manual mode, the adc\_sel is reset with every write to either ADC\_CHANNEL\_MASK\_L or ADC\_CHANNEL\_MASK\_H



**Figure 117:**  
ADC\_CHANNEL\_MASK\_H Register

0x8c: ADC_CHANNEL_MASK_H				
Field	Name	Rst	Type	Description
3	adc_channel_mask_gpio2	0	RW	GPIO2 input – set gpio2_a=1 and Write 0x47 to register 0xC6 Write 0x0C to register 0xC2 Write 0x0C to register 0xC3
2	adc_channel_mask_gpio3	0	RW	GPIO3 input – set gpio3_a=1 and Write 0x47 to register 0xC6 Write 0x0C to register 0xC2 Write 0x0C to register 0xC3
1	adc_channel_mask_ecgi	0	RW	ECG amplifier input – use for leads off detection
0	adc_channel_mask_ecgo	0	RW	ECG amplifier output – amplified ECG signal

**Figure 118:**  
ADC\_DATA\_L Register

0x8e: ADC_DATA_L				
Field	Name	Rst	Type	Description
7:0	adc_data[7:0]	0	RO	Current ADC output: low byte.

The ADC\_DATA register shows the current raw output of the ADC

**Figure 119:**  
ADC\_DATA\_H Register

0x8f: ADC_DATA_H				
Field	Name	Rst	Type	Description
5:0	adc_data[13:8]	0	RO	Current ADC output: high byte warning: there is no latch mechanism implemented to guarantee consistency if the ADC is possibly running when reading this register, then the data can be corrupted - use the FIFO to guarantee data consistency.

**FIFO Registers**

**Figure 120:**  
FIFO\_CFG Register

0x78: FIFO_CFG				
Field	Name	Rst	Type	Description
5:0	fifo_threshold	19	RW	FIFO threshold. The fifo_threshold interrupt is flagged if there are more than this many entries in the FIFO. 0 ... Interrupt with 1 (16bit) entry in FIFO 63 ... Interrupt when FIFO is full but one; note that the FIFO is 64 entries deep

**Figure 121:**  
FIFO\_CNTRL Register

0x79: FIFO_CNTRL				
Field	Name	Rst	Type	Description
0	fifo_clear	0	PUSH1	Write a 1 here to clear the FIFO can be useful when switching from one sequencer mode to another to make sure that there are no old FIFO entries left

**Figure 122:**  
FIFOSTATUS Register

0xa3: FIFOSTATUS				
Field	Name	Rst	Type	Description
7	fifooverflow	0	RO	FIFO overflow indicator
6:0	fifolevel	0	RO	FIFO fill level (0 ...64)

**Figure 123:**  
FIFOL Register

0xfe: FIFOL				
Field	Name	Rst	Type	Description
7:0	fifol	0	PUSHPOP	Low byte of FIFO

FIFOL can be read out with single reads (2 consecutive I<sup>2</sup>C addresses have to be read to get one FIFO entry) or with block-read (up to 2 x fifo\_depth values can be read in a single block-read)

Upon reading of FIFOH, it automatically advances the internal read pointer and decreases FIFO level.

If reading beyond end of FIFO, data will return 00h. There is no underrun flag, this is not an error condition.

Use ams SDK functions to read from the FIFO register to keep the reading in synchronization with the ADC channel selection. If synchronization is no concern use [fifoh[7:0]:fifol[7:2]] as ADC result as the ADC data is multiplied by x4 before it is pushed in to the FIFO. FIFOL[0] is used as an ADC first channel indication. The first channel indication bit toggles upon every new entry unless the first ADC channel is transmitted. Then toggling can be stopped for up to 5 FIFO entries and the very first stopping indicates the first ADC channel. To allow encoding of any number of ADC channels, the first ADC channel encoding is dropped from time to time.

**Figure 124:**  
FIFOH Register

0xff: FIFOH				
Field	Name	Rst	Type	Description
7:0	fifoh	0	PUSHPOP	High byte of FIFO

See [Interrupts](#) for the actual FIFO interrupt.

## Digital Interface

### Power Management

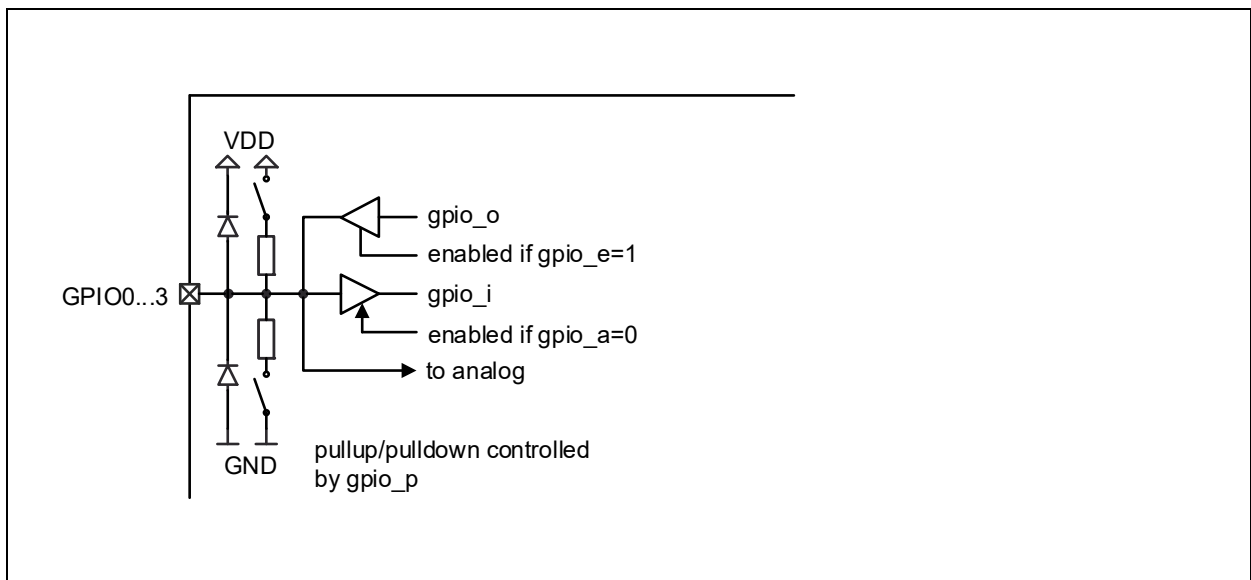
After setting the pin ENABLE=1 the AS7024 registers can be accessed by the I<sup>2</sup>C interface. Before enabling any additional function (current source, TIA, ADC...) set the bit Ido\_en=1 to set the internal LDO to normal mode.

For operating the ADC or the sequencer enable the oscillator by setting osc\_en=1.

### GPIO Pins

Each of the GPIO pins can be digitally controlled and is capable of adding a pullup and/or pulldown:

Figure 125:  
GPIO Internal Circuit



### Interrupts

An interrupt output pin INT can be used to interrupt the host. Following interrupt sources are possible

**irq\_adc:** End of ADC conversion

**irq\_sequencer:** End of sequencer sequence reached.

**irq\_ltf:** A light-to-frequency conversion is finished.

**irq\_adc\_threshold:** ADC threshold triggered – see [ADC Threshold](#).

**irq\_fifothreshold:** FIFO almost full (as defined in register fifo\_threshold)

**irq\_fifooverflow:** FIFO overflow (error condition, data is lost)

**irq\_clipdetect:** TIA output and/or SD output exceeded threshold– see details in CLIPSTATUS

**irq\_led\_supply\_low:** led supply low comparator triggered – see details in LEDSTATUS

Depending on the setting in register INTENAB each of the above interrupt source can assert INT output pin (active low).

### **I<sup>2</sup>C**

The AS7024 includes an I<sup>2</sup>C slave using an I<sup>2</sup>C address of 0x30 (7-bit format; R/W bit has to be added) respectively 60h (8-bit format for writing) and 61h (8-bit format for reading). It expects external pullup resistors.

#### ***I<sup>2</sup>C Serial Control Interface***

#### **I<sup>2</sup>C Feature List**

Fast mode (400kHz) and standard mode (100kHz) support

7+1-bit addressing mode

Write formats: Single-Byte-Write, Page-Write

Read formats: Current-Address-Read, Random-Read, Sequential-Read

SDA input delay and SCL spike filtering by integrated RC-components

#### **I<sup>2</sup>C Protocol**

**Figure 126:**  
**I<sup>2</sup>C Symbol Definition**

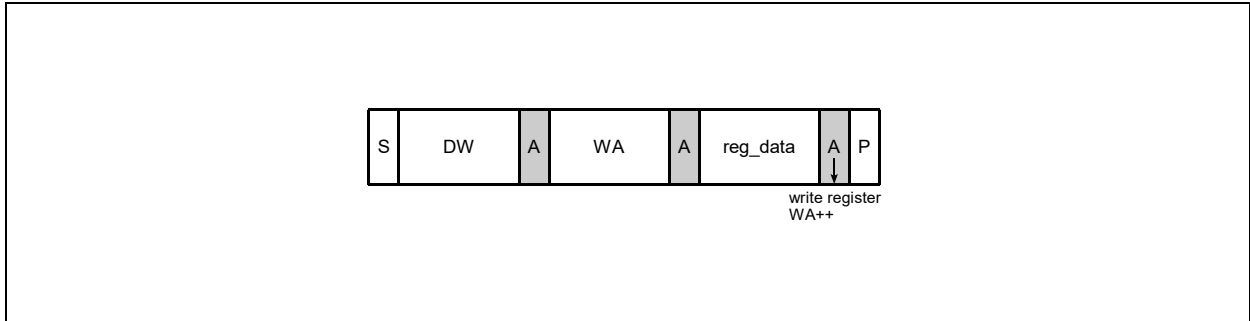
Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	0110 0000b (60h)
DR	Device address for read	R	0110 0001b (61h)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	During acknowledge

**I<sup>2</sup>C Symbol Definition:** Shows the symbols used in the following mode descriptions.

**I<sup>2</sup>C Write Access**

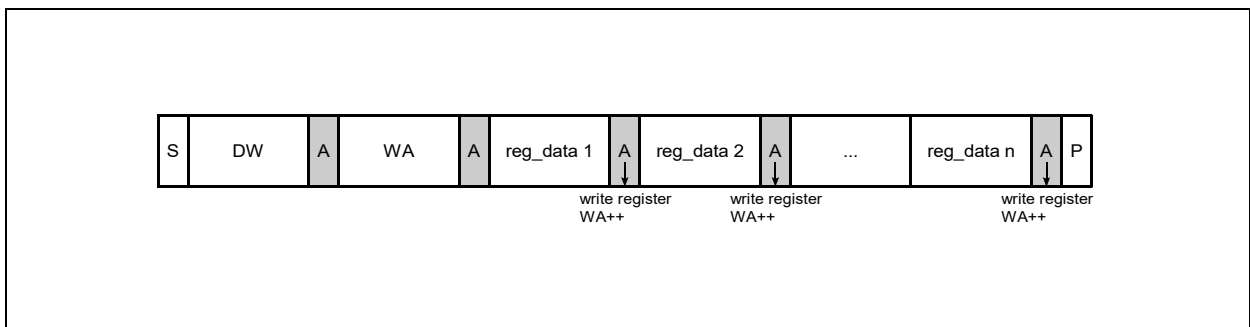
Byte Write and Page Write formats are used to write data to the slave.

**Figure 127:**  
I<sup>2</sup>C Byte Write



**I<sup>2</sup>C Byte Write:** Shows the format of an I<sup>2</sup>C byte write access.

**Figure 128:**  
I<sup>2</sup>C Page Write



**I<sup>2</sup>C Page Write:** Shows the format of an I<sup>2</sup>C page write access.

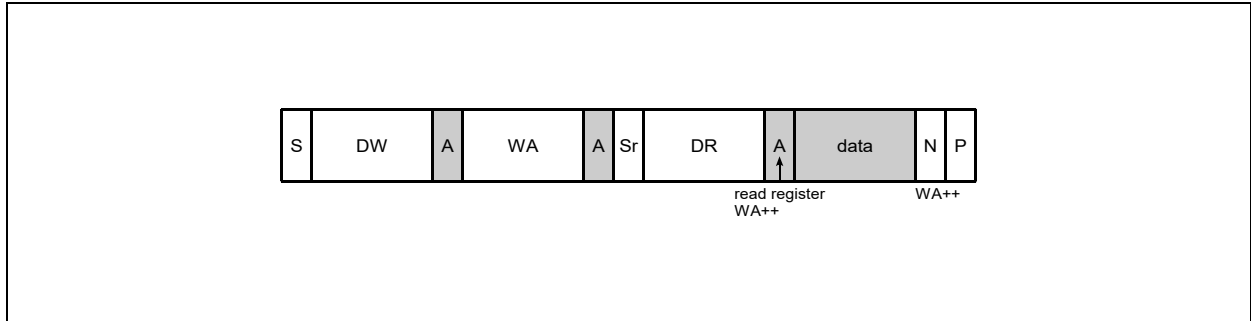
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

### I<sup>2</sup>C Read Access

Random, Sequential and Current Address Read are used to read data from the slave.

**Figure 129:**  
I<sup>2</sup>C Random Read



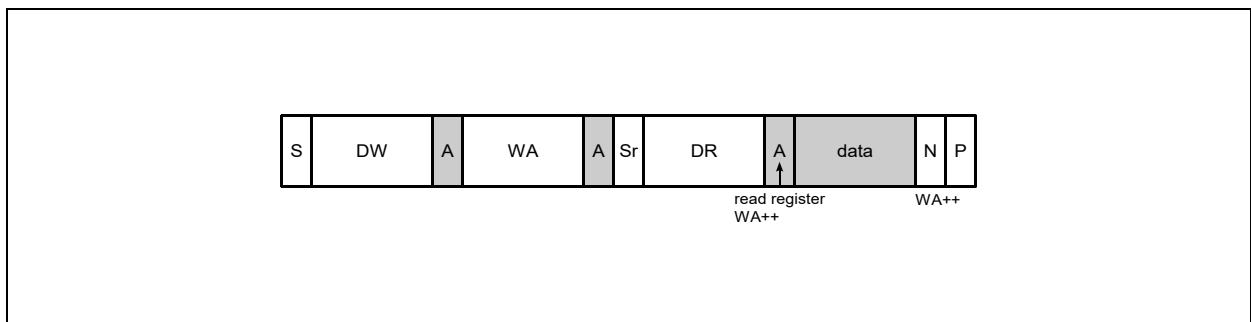
**I<sup>2</sup>C Random Read:** Shows the format of an I<sup>2</sup>C random read access.

Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

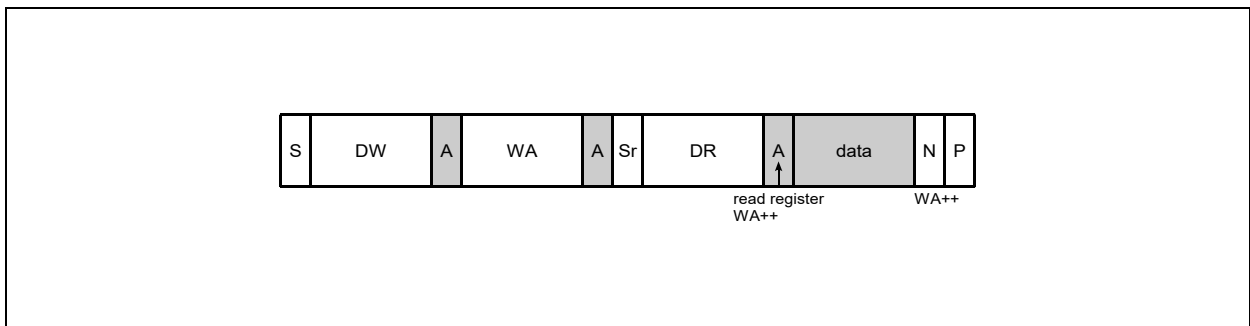
**Figure 130:**  
I<sup>2</sup>C Sequential Read



**I<sup>2</sup>C Sequential Read:** Shows the format of an I<sup>2</sup>C sequential read access.

Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

**Figure 131:**  
I<sup>2</sup>C Current Address Read



**I<sup>2</sup>C Current Address Read:** Shows the format of an I<sup>2</sup>C current address read access.

To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.



### Power, GPIO, ID and Interrupt Registers

**Figure 132:**  
CONTROL Register

0x00: CONTROL				
Field	Name	Rst	Type	Description
1	osc_en	0	RW	Enable the oscillator. The oscillator must be enabled for any analog block (ADC, sequencer, optical frontend, sequencer); not mandatory for current sinks or ECG amplifier
0	ldo_en	0	RW	If the EN input is not asserted, the chip is in reset. If asserted, I <sup>2</sup> C transactions are possible. Upon assertion of ldo_en, the reference and the LDO are enabled. The LDO must be enabled for anything but plain I <sup>2</sup> C register read/write

**Figure 133:**  
GPIO\_A Register

0x08: GPIO_A				
Field	Name	Rst	Type	Description
3	gpio3_a	0	RW	1=Put GPIO3 in analog mode; set this bit when used for an analog function e.g. the electrical frontend. If set execute following I <sup>2</sup> C commands (otherwise an internal pulldown will be enabled) in this sequence: Write 0x47 to register 0xC6 Write 0x0C to register 0xC2 Write 0x0C to register 0xC3
2	gpio2_a	0	RW	1=Put GPIO2 in analog mode If set execute following I <sup>2</sup> C commands (otherwise an internal pulldown will be enabled) in this sequence: Write 0x47 to register 0xC6 Write 0x0C to register 0xC2 Write 0x0C to register 0xC3
1	gpio1_a	0	RW	1=Put GPIO1 in analog mode <sup>(1)</sup>
0	gpio0_a	0	RW	1=Put GPIO0 in analog mode <sup>(1)</sup>

**Note(s):**

1. No further I<sup>2</sup>C commands are required (different to GPIO2/3).

**Figure 134:**  
GPIO\_E Register

0x09: GPIO_E				
Field	Name	Rst	Type	Description
3	gpio3_e	0	RW	GPIO3 output enabled if set
2	gpio2_e	0	RW	GPIO2 output enabled if set
1	gpio1_e	0	RW	GPIO1 output enabled if set
0	gpio0_e	0	RW	GPIO0 output enabled if set

**Figure 135:**  
GPIO\_O Register

0x0a: GPIO_O				
Field	Name	Rst	Type	Description
3	gpio3_o	0	RW	If gpio3_e=1, gpio3_o defines the output state of GPIO3
2	gpio2_o	0	RW	If gpio2_e=1, gpio2_o defines the output state of GPIO2
1	gpio1_o	0	RW	If gpio1_e=1, gpio1_o defines the output state of GPIO1
0	gpio0_o	0	RW	If gpio0_e=1, gpio0_o defines the output state of GPIO0

**Figure 136:**  
GPIO\_I Register

0x0b: GPIO_I				
Field	Name	Rst	Type	Description
3	gpio3_i	0	RO	The digital value sensed on GPIO3
2	gpio2_i	0	RO	The digital value sensed on GPIO2
1	gpio1_i	0	RO	The digital value sensed on GPIO1
0	gpio0_i	0	RO	The digital value sensed on GPIO0

**Figure 137:**  
GPIO\_P Register

0x0c: GPIO_P				
Field	Name	Rst	Type	Description
7	gpio3_pd	0	RW	GPIO3 pulldown configuration 0: No pulldown on GPIO3 1: Pulldown to GND on GPIO3
6	gpio3_pu	0	RW	GPIO3 pullup configuration 0: No pullup on GPIO3 1: Pullup to VDD on GPIO3
5	gpio2_pd	0	RW	GPIO2 pulldown configuration
4	gpio2_pu	0	RW	GPIO2 pullup configuration
3	gpio1_pd	0	RW	GPIO1 pulldown configuration
2	gpio1_pu	0	RW	GPIO1 pullup configuration
1	gpio0_pd	0	RW	GPIO0 pulldown configuration
0	gpio0_pu	0	RW	GPIO0 pullup configuration

**Figure 138:**  
GPIO\_SR Register

0x0d: GPIO_SR				
Field	Name	Rst	Type	Description
3	gpio3_sr	0	RW	GPIO3 slew rate configuration 0: Default slew rate 1: Increased slew rate
2	gpio2_sr	0	RW	GPIO2 slew rate configuration
1	gpio1_sr	0	RW	GPIO1 slew rate configuration
0	gpio0_sr	0	RW	GPIO0 slew rate configuration

**Figure 139:**  
**SUBID Register**

0x91: SUBID				
Field	Name	Rst	Type	Description
7:3	subid	NA	RO	Defines product version. Do not rely on bits defined as 'X'. 1XXXXb
2:0	Revision	NA	RO	Reserved. Do no use and do not rely that the content stays the same for each device.

Internal information: At least one bit is set on subid.

**Figure 140:**  
**ID Register**

0x92: ID					
Field	Name	Rst	Type	Description	
7:2	id	0	RO	Part Number Identification.	
				<b>Value</b>	<b>Meaning</b>
				110011	AS7024
1:0	id_reserved	0	RO	Reserved. Do no use and do not rely that the content stays the same for each device.	

**Figure 141:**  
**STATUS Register**

0xa0: STATUS				
Field	Name	Rst	Type	Description
7	irq_led_supply_low	0	R_PUSH1	Check LEDSTATUS
6	irq_clipdetect	0	R_PUSH1	Check CLIPSTATUS
5	irq_fifooverflow	0	R_PUSH1	FIFO overflow (error condition, new data is lost)
4	irq_fifothreshold	0	R_PUSH1	FIFO is almost full (as defined in fifo_threshold, usually 3/4)
3	irq_adc_threshold	0	R_PUSH1	The ADC value was above the programmed adc_threshold register setting
2	irq_ltf	0	R_PUSH1	LTF measurement is done. check LTFSTATUS (or ignore it)
1	irq_sequencer	0	R_PUSH1	All configured sequencer iterations have finished
0	irq_adc	0	R_PUSH1	ADC has finished

The STATUS register shows the current state of the interface. Some bits in here can trigger an interrupt.

An asserted bit can be cleared by writing a '1' to it - in case of irq\_led\_supply\_low and irq\_clipdetect, this also clears the underlying condition in the CLIPSTATUS and LEDSTATUS registers.

The FIFO threshold interrupt cannot be cleared directly, but only by lowering the FIFO level. The FIFO overflow interrupt is sticky and must be cleared explicitly.

**Figure 142:**  
**CLIPSTATUS Register**

0xa1: CLIPSTATUS				
Field	Name	Rst	Type	Description
3	pd_clipdetect_l	0	RO	If this bit is asserted, photo diode amplifier has been below the lower threshold
2	pd_clipdetect_h	0	RO	If this bit is asserted, photo diode amplifier has been above the upper threshold
1	sd_clipdetect_l	0	RO	If this bit is asserted, photo diode amplifier has been below the lower threshold
0	sd_clipdetect_h	0	RO	If this bit is asserted, photo diode amplifier has been above the upper threshold

An asserted bit can be cleared by writing a '1' to the irq\_clipdetect.

**Figure 143:**  
**LEDSTATUS Register**

0xa2: LEDSTATUS				
Field	Name	Rst	Type	Description
3	led4_supply_low	0	RO	If this bit is asserted, LED4 voltage has been too low.
2	led3_supply_low	0	RO	If this bit is asserted, LED3 voltage has been too low.
1	led2_supply_low	0	RO	If this bit is asserted, LED2 voltage has been too low.
0	led1_supply_low	0	RO	If this bit is asserted, LED1 voltage has been too low.

An asserted bit can be cleared by writing a '1' to the irq\_led\_supply\_low bit.

**Figure 144:**  
**INTENAB Register**

0xa8: INTENAB				
Field	Name	Rst	Type	Description
7	irq_led_supply_low_enab	0	RW	1 ... Enable led supply low interrupt
6	irq_clipdetect_enab	0	RW	1 ... Enable clipdetect interrupt
5	irq_fifooverflow_enab	0	RW	1 ... Enable fifooverflow interrupt
4	irq_fifothreshold_enab	0	RW	1 ... Enable fifothreshold interrupt
3	irq_adc_threshold_enab	0	RW	1 ... Enable irq_adc_threshold as an interrupt source
2	irq_ltf_enab	0	RW	1 ... Enable LTF as an interrupt source
1	irq_sequencer_enab	0	RW	1 ... Enable irq_sequencer as an interrupt source
0	irq_adc_enab	0	RW	1 ... Enable irq_adc as an interrupt source

Each of the STATUS register bits can cause an interrupt (register INTR) if the respective bit is asserted in the INTENAB register.

**Figure 145:**  
**INTR Register**

0xa9: INTR				
Field	Name	Rst	Type	Description
7	irq_led_supply_low_intr	0	RO	
6	irq_clipdetect_intr	0	RO	
5	irq_fifooverflow_intr	0	RO	
4	irq_fifothreshold_intr	0	RO	
3	irq_adc_threshold_intr	0	RO	
2	irq_ltf_intr	0	RO	
1	irq_sequencer_intr	0	RO	
0	irq_adc_intr	0	RO	

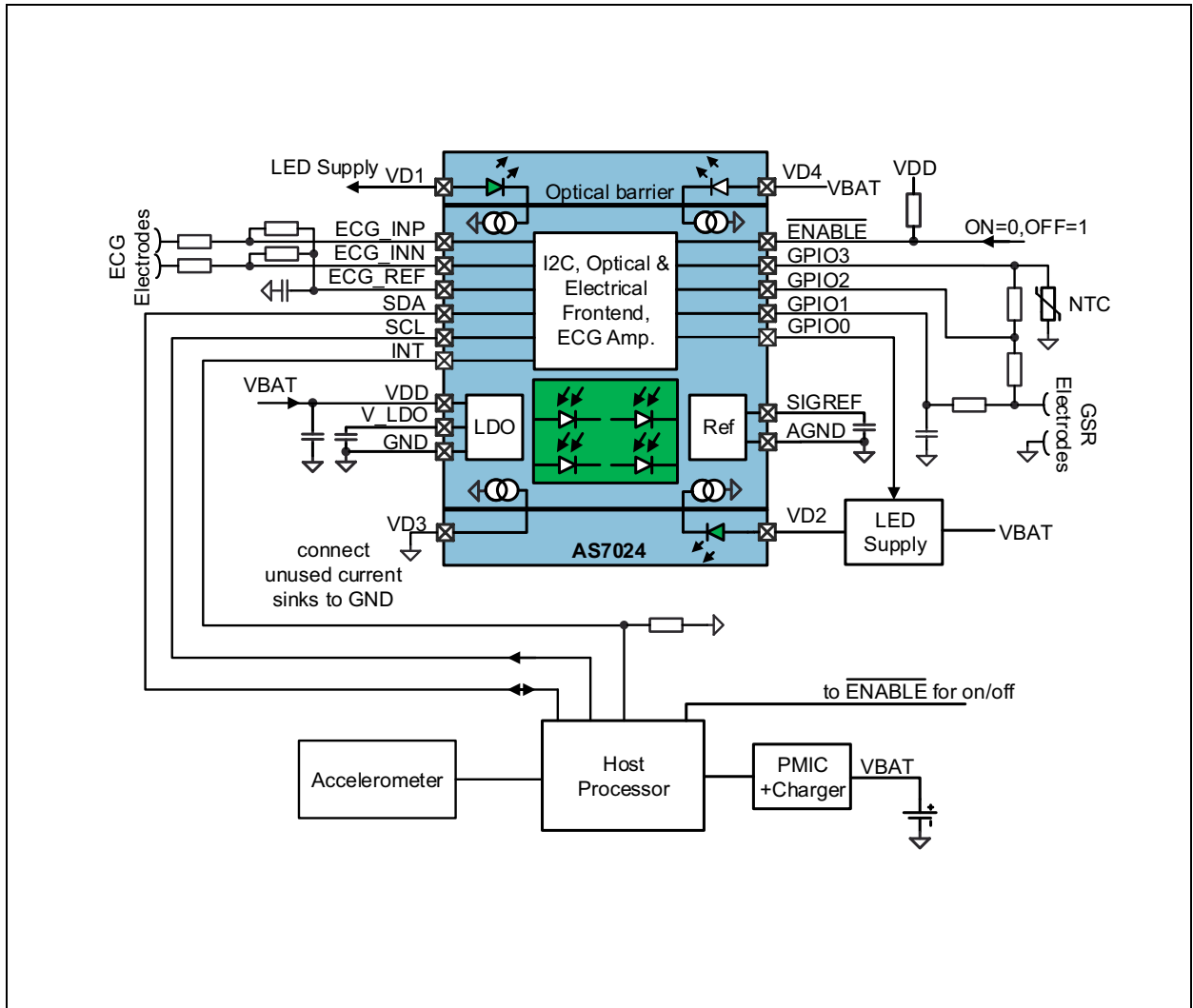
The INTR registers shows the bit or bits that are responsible for an asserted interrupt. Effectively, these bits are OR-ed together to drive the interrupt pin INT low (open drain output).

**Application Information**

The following figure shows the complete integration of the AS7024 in a mobile optical measurement system for HRM, SpO2, GSR (galvanic skin resistivity) and skin temperature using an NTC.

The device can be powered directly by a Lilon battery as it has its own power management. Nevertheless the I<sup>2</sup>C interface can be powered by 1.8V circuitry.

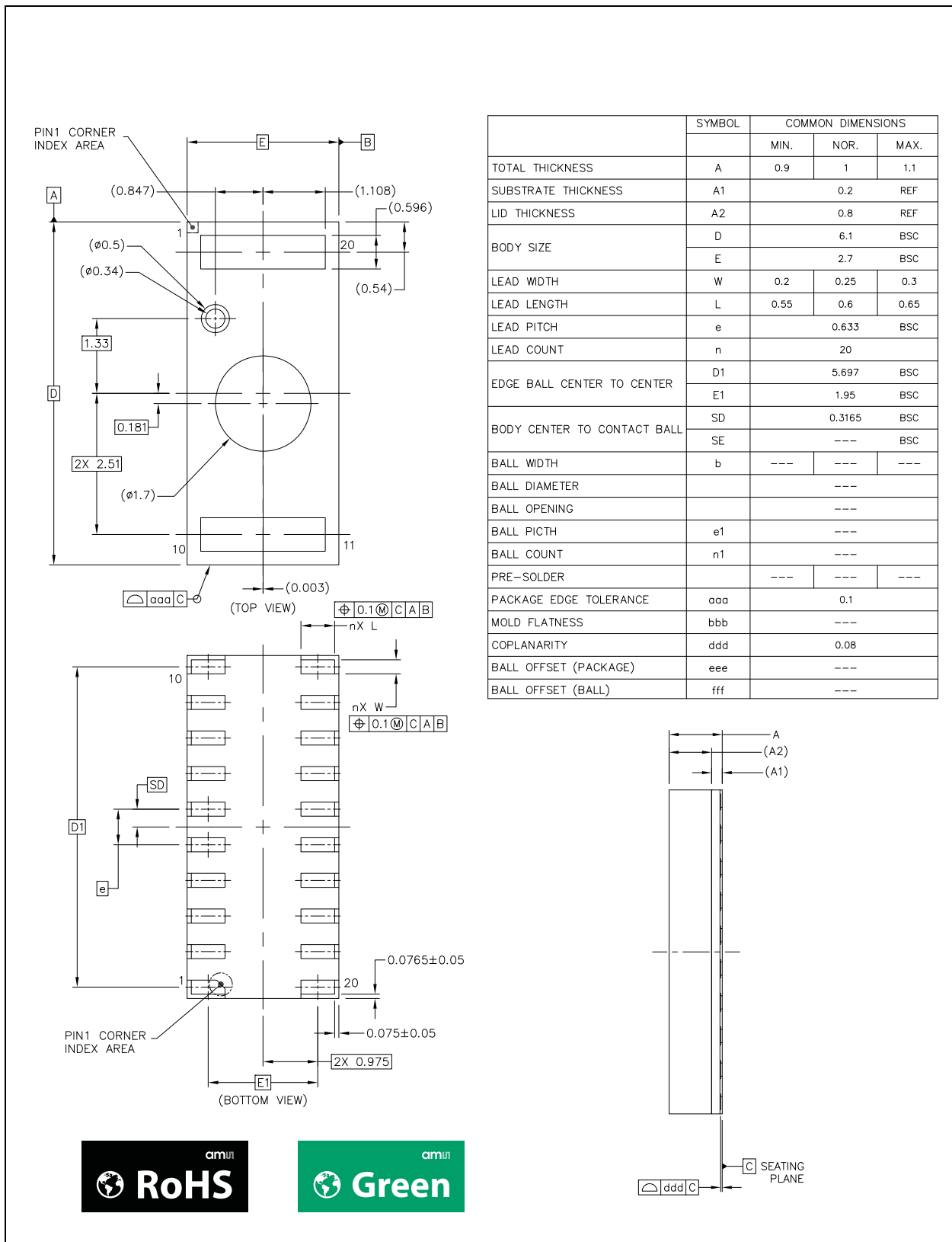
**Figure 146:**  
**Optical HRM Measurement System for Wrist-Based Application**





# Package Drawings & Markings

Figure 147:  
Package Drawing



## Ordering & Contact Information

Figure 148:  
Ordering Information

Ordering Code	Type	Marking	Delivery Form	Delivery Quantity
AS7024-AB	AS7024	NA	Tape and Reel	5000 pcs/reel

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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## Revision Information

Changes from 1-03 (2017-Sep-27) to current revision 1-04 (2018-Sep-11)	Page
Removed "Confidential" from footer	

**Note(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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