Datasheet

DS000716

AS7030B

Vital Sign Sensor

v1-00 • 2020-Jun-10

Biosensor Solution with Embedded ECG Channel

Content Guide

1 Functional Description

The operation of the AS7030B is based on photoplethysmography (PPG) and electrocardiogram (ECG). PPG is the most used HRM and HRV method, which measures the pulse rate by sampling light modulated by the blood vessels, which expand and contract as blood pulses through them. ECG is the reference for any measurement of the bio potential generated by the heart.

The embedded ECG analog front end satisfies IEC 60601-2-47 requirements.

The module includes the LEDs, photo-sensor, analog front-end (AFE) and sequencer as well as application software. In addition, the module also enables skin temperature and skin resistivity measurements by providing interfaces to external sensors.

Built-in infrared emitter and dedicated photodiode enable easy integration of proximity function in wearable or mobile devices.

Compared to the previous generation AS7030B has 250% larger photodiode with improved the optical performance. This in combination with more efficient LEDs allows reducing current consumption while achieving high PPG performances.

The AS7030B's low-power design and small form factor is particularly well suited to application in fitness bands, smart watches, sports watches and smart patches, in which board space is limited and in which users look for extended, multi-day intervals between battery recharges.

1.1 Key Benefits & Features

The benefits and features of AS7030B, Vital Sign Sensor, are listed below:

Figure 1:
Added Value of Using AS7030B

Benefits	Features
Address all skin types	Improved optical path
Higher optical NR	250% larger embedded photodiode
Allows smallest application size e.g. narrow HRM measurement band	Single device integrated optical solution
Electrocardiogram ECG with dry electrodes	Embedded low noise analog front end for ECG signals acquisition
Enabling blood pressure measurements	Synchronized PPG and ECG acquisition
Good HRM measurement quality	Low noise analog optical front end

Benefits	Features
Additional information for end user	Analog electrical front end (e.g. for temperature sensing using a NTC or galvanic skin resistivity (GSR))
Proximity function easy to implement	Built-in infrared emitter and dedicated photodiode
Integrated interference filter	Reduce negative effect of strong sunlight
Long operating time	Hardware sequencer to offload processor Adjustable LED driver with current control
Works reliably with ambient light	Synchronous demodulator

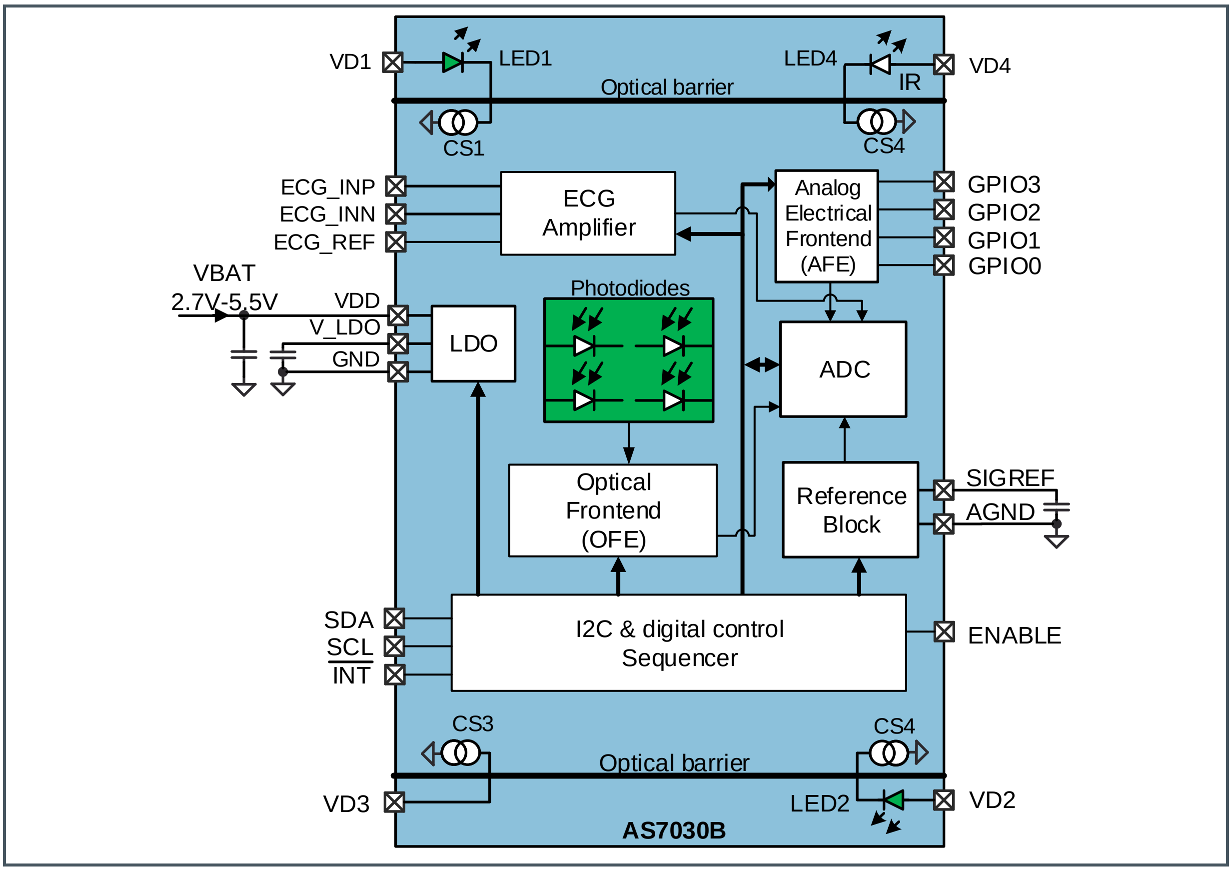
1.2 Applications

- Optical sensor platform
- Fitness band
- Smart watch
- Heart rate monitor
- Cuff less blood pressure measurements
- ECG monitoring

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2 :
Functional Blocks of AS7030B



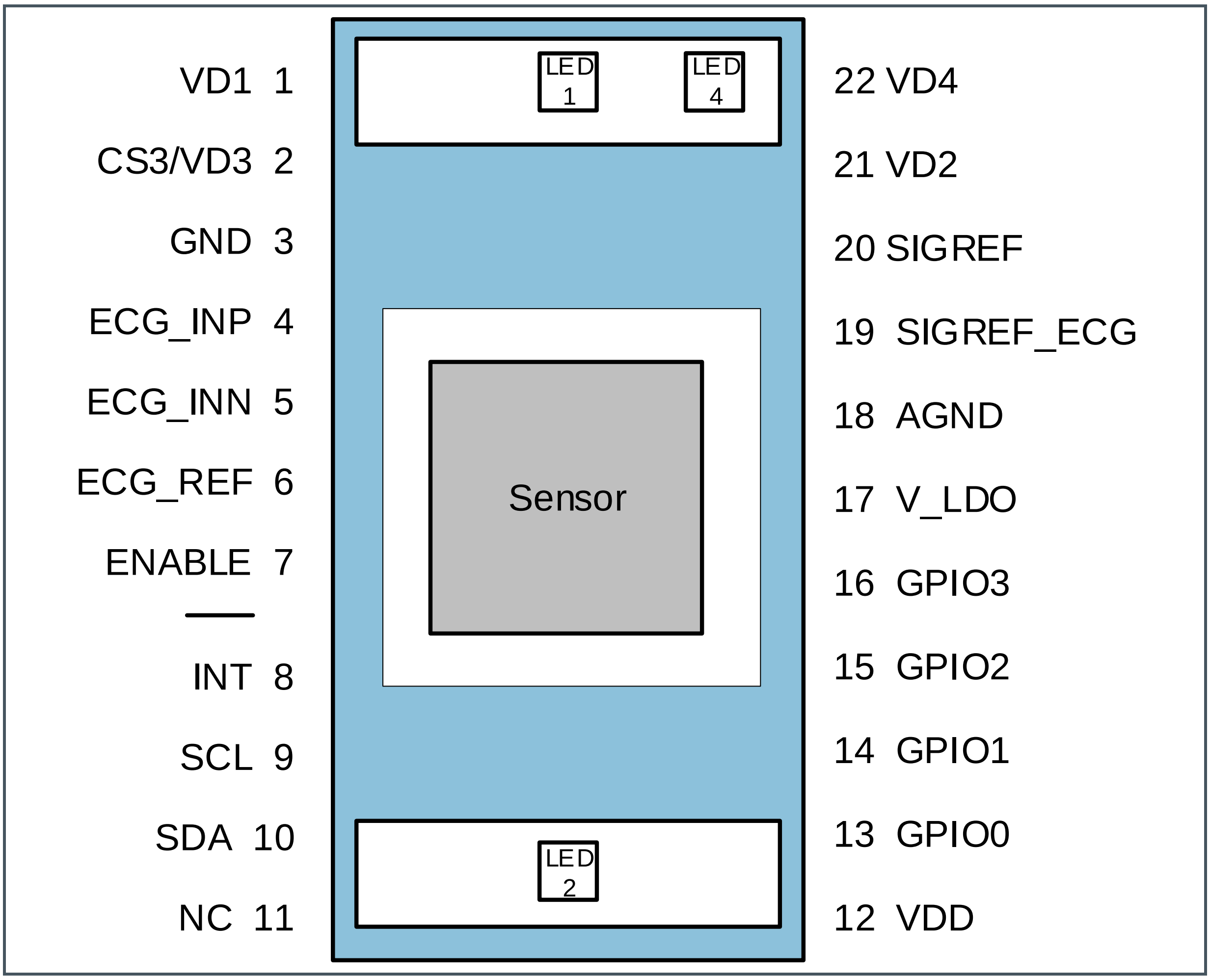
2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS7030B-COLT	OLGA-22	n.a.	Tape & Reel	5000 pcs/reel
AS7030B-COLM	OLGA-22	n.a.	Tape & Reel	500 pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pinout



3.2 Pin Description

Figure 4:
Pin Description of AS7030B

Pin Number	Pin Name	Pin Type(1)	Description
1	VD1	AI	Supply voltage for LED D1
2	VD3	AI	Connection to current sink 3
3	GND	G	Power supply ground. All voltages are referenced to GND.
4	ECG_INP	AI	ECG amplifier positive input
5	ECG_INN	AI	ECG amplifier negative input
6	ECG_REF	AO	ECG amplifier reference output
7	ENABLE	DI	Enable input for AS7030B. Active high. Setting this input to low resets all internal registers and the AS7030B enters power down mode. Setting it high allows operation of the AS7030B. If ENABLE is not used (AS7030B always enabled), connect to VDD.
8	INT	DO	Open drain interrupt output pin. Active low.
9	SCL	DI	I²C serial clock input terminal – the device does not use clock stretching therefore SCL is only an input terminal.
10	SDA	DIO	I²C serial data I/O terminal – open drain.
11	NC		Not connect
12	VDD	P	Supply voltage. Connect a 2.2 µF capacitor to GND.
13	GPIO0	GPIO	General purpose input/output
14	GPIO1	GPIO	General purpose input/output
15	GPIO2	GPIO	General purpose input/output
16	GPIO3	GPIO	General purpose input/output
17	V_LDO	AO	1.9 V output voltage. Connect 2.2 µF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 or 0201 sized GRM033R60J225ME47 from Murata – needs to have >1 µF with 1.0 V voltage bias); do not load externally
18	AGND	GND	Analog ground. Connect to low noise GND

Pin Number	Pin Name	Pin Type[(1)]	Description
19	SIGREF_ECG	AO	Analog reference output. Connect 2.2 µF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 or 0201 sized GRM033R60J225ME47 from Murata – needs to have >1 µF specified for 1.0 V voltage bias); do not load externally The typical operating voltage on this pin is 0.6 V (sigref_en=1)
20	SIGREF	AO	Analog reference output. Connect 2.2 µF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 or 0201 sized GRM033R60J225ME47 from Murata – needs to have >1µF specified for 1.0 V voltage bias); do not load externally The typical operating voltage on this pin is 0.6 V (sigref_en=1)
21	VD2	AI	Supply voltage for LED D2
22	VD4	AI	Supply voltage for LED D4

(1)
DI Digital Input
DO Digital Output
DIO Digital IO
AI Analog Input
AO Analog Output
GPIO General Purpose IO
P Power Supply

4 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5
Absolute Maximum Ratings of AS7030B

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{SUP} / V_{GND}	Supply Voltage to Ground		6	V	
V_{IN}	Input Pin Voltage to Ground pins GPIO0/1/2/3	-0.3	VDD+0.3 (max. 6 V)	V	Diode to VDD
$V_{IN\text{-}OTHER}$	Input Pin Voltage to Ground pins SCL/SDA/INT/ENABLE and VD1/VD2/VD3/VD4	-0.3	5.5	V	No internal diode to VDD or V_LDO
$V_{VD1/2/3/4\_INTERNAL}$	Voltage between internal pin of VD1-VD4 to VDD		VDD+0.3	V	Internal diode between current source (internal node at anode of the LED if the pin has a LED otherwise VD1/2/3/4 pin) and VDD
$V_{IN\text{-}LDO}$	Input Pin Voltage to Ground for pin V_LDO	-0.3	2.0	V	Diode to VDD
$V_{IN\text{-}LDO\_DIODE}$	Input Pin Voltage to Ground pins for ECG_INP/ECG_INN/ECG_REF/SIGREF	-0.3	2.0	V	Diode to V_LDO
$V_{GND\text{-}AGND}$	Analog to power ground voltage difference	-0.3	+0.3	V	
I_{SCR}	Input Current (latch-up immunity)	±100		mA	JEDEC JESD78
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±2		kV	ANSI/ESDA/JEDEC JS-001-2012
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100 % Sn)

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of AS7030B

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Supply voltage		2.7	3.8	5.5	V
T_{AMB}	Operating free-air temperature		−30		70	°C
IDD	Supply current	ENABLE=VDD, ldo_en=0; osc_en=0; internal LDO operating in low power mode – only I²C communication possible, no blocks shall be enabled (1)		22		µA
		ENABLE=VDD, ldo_en=1; osc_en=0; internal LDO operating and bandgap running – I²C communication possible, analog blocks can be enabled (1)		32		µA
		ENABLE=VDD, ldo_en=1, osc_en=1; internal LDO operating and bandgap and oscillator running – I²C communication possible, analog blocks can be enabled		86		µA
		SIGREF buffer (sigref_en=1)		52		µA
		Trans-impedance amplifier (pd_amp_en=1)		110		µA
		Optical front end operating (one channel)		200		µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Gain stage (ofe1_gain_en=1 or ofe2_gain_en=1)		75		µA
		ADC sampling at 20 Hz with 64 µs settling time		4.5		µA
		ECG amplifier and frontend (need SIGREF enabled)		190		µA
		ECG leakage compensation (ecg_low_leakage_en=1), low pass filter, high pass filter and gain stage		151		µA
		Power down, no I²C communication possible ENABLE=GND(2)		0.5		µA
VOL	GPIO0-3, INT, SDA output low voltage	With 3 mA load With 6 mA load	0 0		0.4 0.8	V
VOH	GPIO0-3 output high voltage	With 3 mA load	2.3		VDD	V
VIH	GPIO0-3, SCL, SDA, ENABLE input high voltage		1.25			V
VIL	GPIO0-3, SCL, SDA, ENABLE input low voltage				0.54	V
ILEAK1	GPIO0-3, SCL, SDA, ENABLE, INT		-1		1	µA
ILEAK2	VD1, VD2 VD3, VD4		-3		3	µA
E_f2M	Tolerance of internal 2 MHz oscillator	0 ºC to 70 ºC, VDD<5.0 V	-2		2	%
		-30 ºC to 70 ºC	-4		2	%
ECG Amplifier and Filter						
ILEAK_ECG	ECG pins leakage current	Lab evaluation shows <±20 nA maximum leakage current. Not production tested.		±1		nA

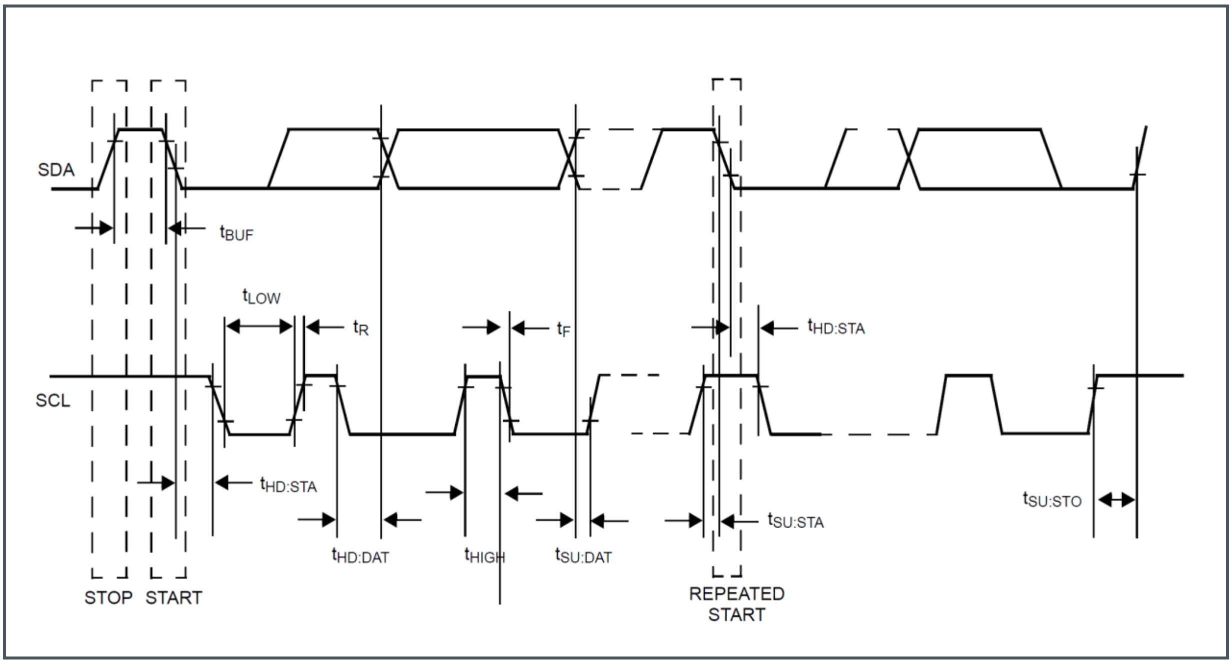
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{NOISE_ECG}	Input referred noise	Gain=192 V/V, short circuited inputs, sample rate = 1000 sps, BW 0.33 Hz÷100 Hz. Filtered		1.64		µVrms
LED						
I_{LED}	Allowed operating LED current range		0		50	mA
		1/10 duty cycle @ 1 kHz (csx_boost = 0)			100	mA
		1/10 duty cycle @ 1 kHz external LED (csx_boost = 1)			200	mA
VF_{LED}	Forward voltage	Green LED, add compliance voltage of LED driver, ILED=10 mA, add compliance voltage of LED driver (V_Dmin) to obtain minimum voltage on the pin to drive the current at T_{AMB}=25 ºC		3.1	3.3	V
		IR LED, ILED=20 mA		1.4		V
λp	Peak wavelength at I_{LED}=20 mA	Green LED		527		nm
		IR LED		940		nm
LED Driver						
$I_{LED1/2/3/4}$	LED output current range	LED current is adjustable with 10 bits – registers curr1/2/3/4 csx_boost = 0	0		100	mA
		LED current is adjustable with 10 bits – registers curr1/2/3/4 csx_boost = 1			200	mA
	Tolerance	At 35 mA output current (currX[9:0]=166 h, X=1…4), VDD<5.0 V	-7		7	%
V_Dmin	Min output voltage compliance	csx_boost = 0		0.3		V
		csx_boost = 1		0.7		V
V_Dmax	Max output voltage compliance				5.5	V
Photodiode						
Area	Photodiode area			2.5		mm^2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Re_{PD1-4}	Irradiance responsivity photodiode PD1…PD4	Wavelength = 550 nm; 4 photodiodes (PD1 - PD4) connected together; TIA resistor (pd_ampres) = 3 MΩ		212		Counts/ (µW/cm²)
	Irradiance responsivity photodiode B	Wavelength = 940 nm; TIA resistor (pd_ampres) = 3 MΩ		11		
Id	Dark current	E_e=0, T_{AMB} =25 °C	0		1	nA
Ios	Extrapolated offset current	T_{AMB} =25 °C	-1		1	nA
ADC						
Vref	ADC reference voltage			1.6		V
Nbit	Resolution		14			Bit
INL	Relative accuracy	T_{AMB} =25 °C	-8		8	LSB
DNL[(3)]	Differential nonlinearity	T_{AMB} =25 °C		1.5		LSB
	Offset error	T_{AMB} =25 °C	-8		8	LSB
	Gain error	T_{AMB} =25 °C	-8		8	LSB
SNR	Signal-to-noise ratio	Fsample = 1 kHz, Fsignal=100 Hz		80		dB
THD	Total harmonic distortion	Fsample = 1 kHz, Fsignal=100 Hz		-70		dB
Tconv	Conversion rate	14-bit resolution			50	ksps
Vin	Input voltage range		0		Vref	V
I²C Mode Timings						
f_{SCLK}	SCL clock Frequency		0		400	kHz
t_{BUF}	Bus free time Between a STOP and START condition		1.3			µs
$t_{HD:STA}$	Hold time (Repeated) START condition[(4)]		0.6			µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LOW}	LOW period of SCL clock		1.3			µs
t_{HIGH}	HIGH period of SCL clock		0.6			µs
$t_{SU:STA}$	Setup time for a repeated START condition		0.6			µs
$t_{HD:DAT}$	Data hold time(5)		0		0.9	µs
$t_{SU:DAT}$	Data setup time(6)		100			ns
t_R	Rise time of both SDA and SCL signals		20		300	ns
t_F	Fall time of Both SDA and SCL signals		20		300	ns
$t_{SU:STO}$	Setup time for STOP condition		0.6			µs
C_B	Capacitive load for each bus line	CB — total capacitance of one bus line in pF			500	pF
$C_{I/O}$	I/O pin capacitance (SDA, SCL)				10	pF

(1) GPIO0-3 configured to draw minimum current (software dependent).
(2) AS7030B I^2C interface active also in power down mode
(3) Specified only typical value for DNL to reduce production test time.
(4) After this period, the first clock pulse is generated.
(5) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHMIN of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(6) Fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns before the SCL line is released.

Figure 7:
I²C Mode Timing Diagram



6 Register Description

6.1 Register Overview

Figure 8:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Register Type 1									
0x0F	GPIO_SYNC	Not used	Not used	Not used	Not used	Not used	gpio_edge	goio_select[1:0]	
0x10	LED_CFG	sigref_en	sigref__ecg_voltage	sigref__ofe_voltage[1:0]		led4_en	led3_en	led2_en	led1_en
0X11	LED_WAIT_LOW	led_wait_low[7:0]							
0X12	LED1_CURRL	Curr1[1:0]		Not used	Not used	Not used	Not used	Not used	cs1_boost
0X13	LED1_CURRH	Curr1[9:2]							
0X14	LED2_CURRL	Curr2[1:0]		Not used	Not used	Not used	Not used	Not used	cs2_boost
0X15	LED2_CURRH	Curr2[9:0]							
0X16	LED3_CURRL	Curr3[1:0]		Not used	Not used	Not used	Not used	Not used	cs3_boost
0X17	LED3_CURRH	Curr3[9:2]							
0X18	LED4_CURRL	Curr4[1:0]		Not used	Not used	Not used	Not used	Not used	cs4_boost
0X19	LED4_CURRH	Curr4[9:2]							
0X2C	LED12_MODE	Man-sw_led2	Led2_mode[2:0]			Man_sw_led1	Led1_mode[2:0]		
0X2D	LED34_MODE	Man-sw_led4	Led4_mode[2:0]			Man-sw_led3	Led3_mode[2:0]		
0X2E	MAN_SEQ_CFG	man_mode	man_sw_sdmult	man_sw_sdpol	man_sw_itg	diode_ctrl[2:0]			seq_en
0X1A	PD_CFG	Not used	pd_boost	pd4	pd3	pd2	pd1	pd_i1	pd_i0
0X1B	PDOFFX_LEDOFF	pdoffx_ledoff[7:0]							
0X1C	PDOFFX_LEDON	pdoffx_ledon[7:0]							
0X1D	PD_AMPRCCFG	pd_ampres[2:0]			pd_ampcap[4:0]				
0X1E	PD_AMPCFG	pd_amp_en	pd_amp_auto	pd_ampvo[3:0]				pd_ampcomp[1:0]	

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X1F	OFE1_PD_THCFG	ofe1_pd_clipdetect_h_thresh[3:0]				ofe1_pd_clipdetect_l_thresh[3:0]			
0X30	SEQ_CNT	seq_count[7:0]							
0X31	SEQ_DIV	seq_div[7:0]							
0X32	SEQ_START	Not used	Not used	Not used	Not used	Not used	seq_strat_gpio	seq_start_sync	seq_start
0X33	SEQ_PER	seq_period[7:0]							
0X34	SEQ_LED_STA	seq_led_start[7:0]							
0X35	SEQ_LED_STO	seq_led_stop[7:0]							
0X36	SEQ_SECLED_STA	seq_secled_start[7:0]							
0X37	SEQ_SECLED_STO	seq_secled_stop[7:0]							
0X38	SEQ_ITG_STA	seq_itg_start[7:0]							
0X39	SEQ_ITG_STO	seq_itg_stop[7:0]							
0X3A	SEQ_SDP1_STA	seq_sdp1_start[7:0]							
0X3B	SEQ_SDP1_STO	seq_sdp1_stop[7:0]							
0X3C	SEQ_SDP2_STA	seq_sdp2_start[7:0]							
0X3D	SEQ_SDP2_STO	seq_sdp2_stop[7:0]							
0X3E	SEQ_SDM1_STA	seq_sdm1_start[7:0]							
0X3F	SEQ_SDM1_STO	seq_sdm1_stop[7:0]							
0X40	SEQ_SDM2_STA	seq_sdm2_start[7:0]							
0X41	SEQ_SDM2_STO	seq_sdm2_stop[7:0]							
0X42	SEQ_ADC	seq_adc[7:0]							
0X43	SEQ_ADC2TIA	seq_adc2tia[7:0]							
0X44	SEQ_ADC3TIA	seq_adc3tia[7:0]							
0X45	SD_SUBS	sd_subs[7:0]							
0X46	SEQ_CFG	Not used	Not used	Not used	Not used	Not used	Not used	Not used	sd_subs_always
0X47	SEQ_ERR	irq_adc_timing_error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
0X48	SEQ_OVS_SEL	ovs_sel2				ovs_sel1			
0X49	SEQ_OVS_VAL	Not used	ovs_val2			Not used	ovs_val1		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X4A	SEQ_DIS_SEL	dis_sel2[3:0]				dis_sel1[3:0]			
0X4B	SEQ_DIS_VAL1	Seq_dis_val1[7:0]							
0X4C	SEQ_DIS_VAL2	Seq_dis_val2[7:0]							
0X60	CYC_COUNTER	cycle_counter[7:0]							
0X61	SEQ_COUNTER	sequence_counter[7:0]							
0X62	SUBS_COUNTER	subs_counter[7:0]							
0X50	OFE_CFGA	ofe2_en	ofe1_en	en_bias_ofe	aa_freq[1:0]		gain_sd[2:0]		
0X51	OFE1_SD_THCFG	ofe1_sd_clipd_h_thresh [3:0]				ofe1_sd_clipd_l_thresh [3:0]			
0X52	OFE_CFGC	Not used	prefilter_aa_byp	prefilter_hp_byp	prefilter_gain_byp	prefilter_bypass_en	prefilter_aa_en	prefilter_hp_en	prefilter_gain_en
0X53	OFE_CFGD	Not used	notch_bw[1:0]		ofe_sd_hp[2:0]			ofe_gs_aa[1:0]	
0X54	OFE1_CFGA	ofe1_sd_pol_init	ofe1_sd_en	ofe1_hp_en	ofe1_gain_en	ofe1_sd_byp	ofe1_hp_byp	ofe1_gain_byp	ofe1_sd_hld
0X55	OFE1_CFGB	ofe1_gain_g[2:0]			ofe1_sd_bw[2:0]			ofe1_hp_freq[1:0]	
0X56	OFE2_PD_THCFG	ofe2_pd_clipd_h_thresh[3:0]				ofe2_pd_clipd_l_thresh[3:0]			
0X57	OFE2_SD_THCFG	ofe2_sd_clipd_h_thresh[3:0]				ofe2_sd_clipd_l_thresh[3:0]			
0X58	OFE2_CFGA	ofe2_sd_pol_init	ofe2_sd_en	ofe2_hp_en	ofe2_gain_en	ofe2_sd_byp	ofe2_hp_byp	ofe2_gain_byp	ofe2_sd_hld
0X59	OFE2_CFGB	ofe2_gain_g[2:0]			ofe2_sd_bw[1:0]			ofe2_hp_freq[1:0]	
0X20	LTFDATA0_L	ltfdata0[7:0]							
0X21	LTFDATA0_H	ltfdata0[15:8]							
0X22	LTFDATA1_L	ltfdata0[7:0]							
0X23	LTFDATA1_H	ltfdata1[15:8]							
0X24	ITIME	Itime[7:0]							
0X25	LTF_CONFIG	infinite_itime	az_disable_auto	az_mode[1:0]		Not used	ltf_prox_mode	ltf_fifo_mode	ltf_enable
0X26	LTF_SEL	Not used	ltf1_sel[2:0]			Not used	ltf0_sel[2:0]		
0X27	LTF_GAIN	Do not use	Do not use	itime_unit[1:0]		ltf_gain[3:0]			
0X28	LTF_CONTROL	Do not use	Do not use	Do not use	Do not use	Do not use	Do not use	Do not use	ltf_start
0X29	AZ_CONTROL	Do not use	Do not use	Do not use	Do not use	Do not use	Do not use	az_enable_1	az_enable_0
0X2A	OFFSET0	offset0[7:0]							
0X2B	OFFSET1	offset0[7:0]							
0X6C	LTF_THRESHOLD_LOW0	ltf_threshold_low[7:0]							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X6D	LTF_THRESHOLD_LOW1	ltf_threshold_low[15:8]							
0X6E	LTF_THRESHOLD_HIGH0	ltf_threshold_high[7:0]							
0X6F	LTF_THRESHOLD_HIGH1	ltf_threshold_high[15:8]							
0X70	EAF_CFG	Do not use	Do not use	Do not use	Do not use	eaf_enab	eaf_enab_dac	eaf_enab_dac_buf	eaf_enab_gainstage
0X80	EAF_GST	gpio_gst_in[2:0]			gst_ref[1:0]		gst_gain[2:0]		
0X81	EAF_BIAS	gpio_r_bias[2:0]			Not used	Not used	Not used	Not used	Not used
0X82	EAF_DAC	Do not use	Do not use	Do not use	sigref_on_dac_buf	measure_dac	gpio_dac[2:0]		
0X83	EAF_DAC1_L	dac1_value[]		Not used	Not used	Not used	Not used	Not used	Not used
0X84	EAF_DAC1_H	dac1_value[9:2]							
0X85	EAF_DAC2_L	dac2_value[1:0]		Not used	Not used	Not used	Not used	Not used	Not used
0X86	EAF_DAC2_H	dac2_value[9:2]							
0X87	EAF_DAC_CFG	Not used	Not used	Not used	Not used	Not used	Not used	dac_mode[1:0]	
0X5A	OFE_NOTCH	Not used	ofe2_notch_sel60	ofe2_notch_byp	ofe2_notch_en	Not used	ofe1_notch_sel60	ofe1_notch_byp	ofe1_notch_en
0X5B	ECG_MODE	ecg_notch_sel60	ecg_hp_mode[2:0]			ecg_gain_g2[1:0]		ecg_gain_g1[1:0]	
0X5C	ECG_CFGA	ecg_en	ecg_clk_off	ecg_gain_byp	ecg_lp_byp	ecg_notch_byp	ecg_diff_byp	ecg_hp_byp[1:0]	
0X5D	ECG_CFGB	ecg_fast_startup	ecg_lp_freq[1:0]		ecg_hp_freq[1:0]		ecg_gain_g[2:0]		
0X6A	ECG_THRESHOLD_LOW	ecg_threshold_low[7:0]							
0X6B	ECG_THRESHOLD_HIGH	ecg_threshold_high[7:0]							
0X5E	ECG_CFGC	Not used	Not used	Not used	Not used	Not used	Not used	ecg_low_leakage_en	ecg_ref_en
0X5F	ECG_CFGD	Not used	Not used	Not used	ecg_leadsdet_sync_adc	ecg_leadsdet_pol	ecg_leadsdet_curr[1:0]		ecg_leadsdet_en
0X68	ADC_THRESHOLD	adc_threshold[7:0]							
0X69	ADC_THRESHOLD_CFG	Not used	Not used	Not used	Not used	Not used	Not used	adc_thresh_differential	adc_thresh_tiaonly
0X88	ADC_CFGA	Not used	Not used	Not used	Not used	adc_multi_n[2:0]			adc_multimode
0X89	ADC_CFGB	Not used	Not used	adc_clock[2:0]			adc_calibration	ulp	adc_en
0X8A	ADC_CFGC	Not used	Not used	Not used	adc_selfpd	adc_discharge	adc_settling_time[2:0]		

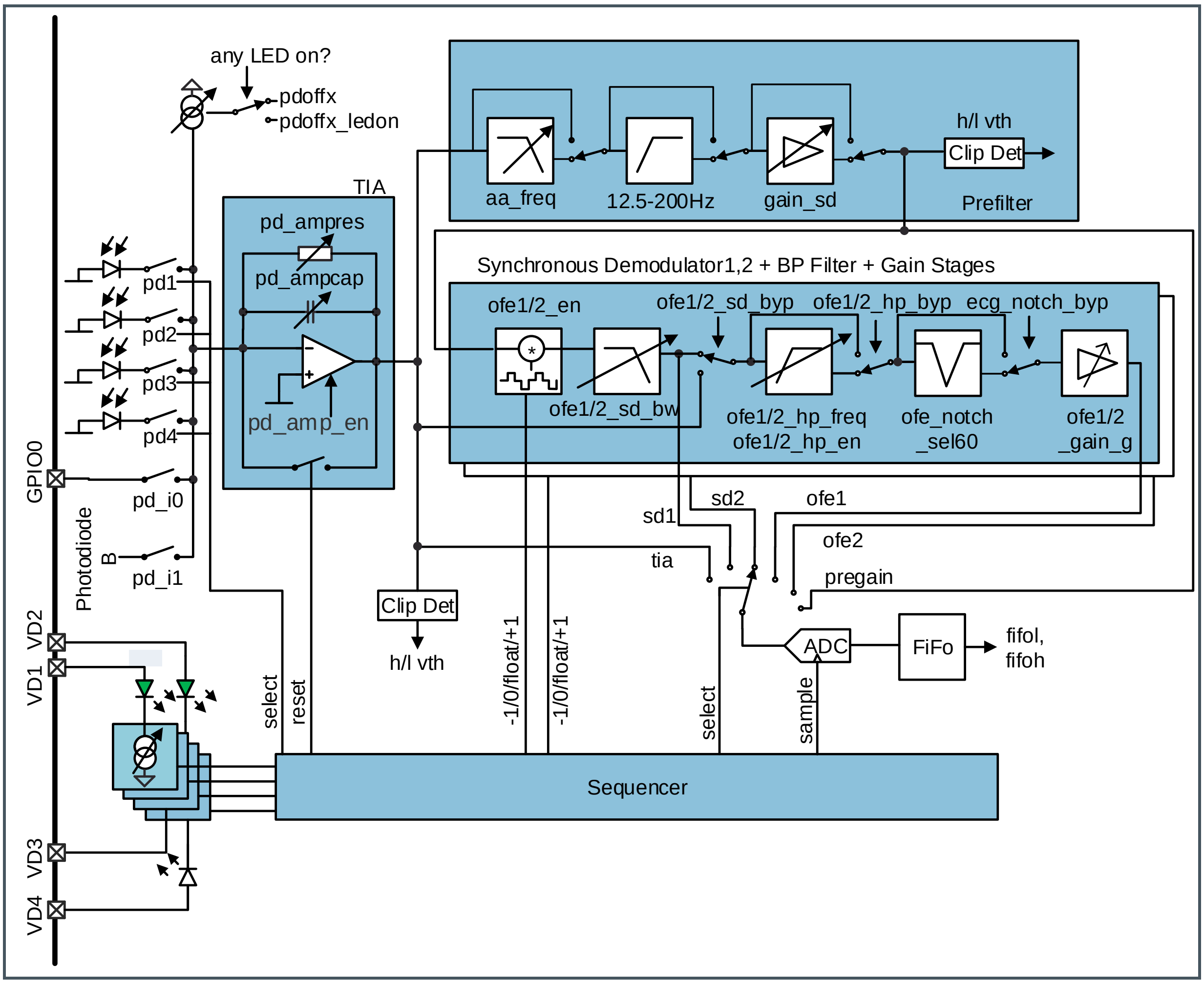
Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X8B	ADC_CHANNEL_MASK_L	adc_channel_mask_pregain	adc_channel_mask_afe	adc_channel_mask_temp	adc_channel_mask_sd2	adc_channel_mask_ofe2	adc_channel_mask_sd1	adc_channel_mask_ofe1	adc_channel_mask_tia
0X8C	ADC_CHANNEL_MASK_H	Not used	Not used	Not used	Not used	adc_channel_mask_gpio2	adc_channel_mask_gpio3	adc_channel_mask_ecgi	adc_channel_mask_ecgo
0X8E	ADC_DATA_L	adc_data[7:0]							
0X8F	ADC_DATA_H	Not used	Not used	adc_data[13:8]					
0X78	FIFO_CFG	Not used	fifo_threshold[6:0]						
0X79	FIFO_CNTRL	Not used	Not used	Not used	Not used	Not used	Not used	Not used	fifo_clear
0XFE	FIFOL	fifol[7:0]							
0XFF	FIFOH	fifoh[7:0]							
0x00	CONTROL	Not used	Not used	Not used	hs_en	Not used	clk_def	osc_en	ldo_en
0X08	GPIO_A	Not used	Not used	Not used	Not used	gpio3_a	gpio2_a	gpio1_a	gpio0_a
0X09	GPIO_E	Not used	Not used	Not used	Not used	gpio3_e	gpio2_e	gpio1_e	gpio0_e
0X0A	GPIO_O	Not used	Not used	Not used	Not used	gpio3_o	gpio2_0	gpio1_0	gpio0_0
0X0B	GPIO_I	Not used	Not used	Not used	Not used	gpio3_i	gpio2_i	gpio1_i	gpio0_i
0X0C	GPIO_P	gpio3_pd	gpio3_pu	gpio2_pd	gpio2_pu	gpio1_pd	gpio1_pu	gpio0_pd	gpio0_pu
0X0D	GPIO_SR	Not used	Not used	Not used	Not used	gpio3_sr	gpio2_sr	gpio1_sr	gpio0_sr
0X91	SUBID	subid[4:0]					Revision[2:0]		
0X92	ID	id[5:0]						id_reserved[1:0]	
0XA0	STATUS	irq_led_supply_low	irq_clipdetect	irq_fifooverflow	irq_fifothreshold	irq_adc_threshold	irq_ltf	irq_sequencer	irq_adc
0XA1	STATUS2	Not used	Not used	Not used	Not used	Not used	irq_ltf_threshold_high	irq_ltf_threshold_low	irq_ecg_threshold
0XA2	CLIPSTATUS	Not used	Not used	Not used	Not used	pd_clipdetect_l	pd_clipdetect_h	sd_clipdetect_l	sd_clipdetect_h
0XA3	LEDSTATUS	Not used	Not used	Not used	Not used	led4_supply_low	led3_supply_low	led2_supply_low	led1_supply_low
0XA4	FIFOSTATUS	Not used	Not used	Not used	Not used	Not used	Not used	Not used	fifooverflow
0XA5	LTFSTATUS	Not used	Not used	ltf1_threshold_high	ltf1_threshold_low	ltf0_threshold_high	ltf0_threshold_low	ltf_sat	ltf_done
0XA6	FIFOLEVEL	fifolevel[7:0]							
0XA8	INTENAB	irq_led_supply_low_enab	irq_clipdetect_enab	irq_fifooverflow_ena	irq_fifothreshold_enab	irq_adc_threshold_enab	irq_ltf_enab	irq_sequencer_enab	irq_adc_enab
0XA9	INTENAB2	Not used	Not used	Not used	Not used	Not used	irq_ltf1_threshold_enab	irq_ltf0_threshold_enab	irq_ecg_threshold_enab
0XAA	INTR	irq_led_supply_low_intr	irq_clipdetect_intr	irq_fifooverflow_intr	irq_fifothreshold_intr	irq_adc_threshold_intr	irq_ltf_intr	irq_sequencer_intr	irq_adc_intr

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0XAB	INTR2	Not used	Not used	Not used	Not used	Not used	irq_ltf_threshold_high_intr	irq_ltf_threshold_low_intr	irq_ecg_threshold_intr

7 Functional Description

7.1 Optical Analog Front End

Figure 9:
Optical Analog Front End



The optical front end is used for PPG measurements.

The OFE consists of:

- 4 LEDs individually configurable, operated manually or controlled by the built-in Sequencer.
  - 2 green LEDs (VD1 and VD2)
  - 1 IR LEDs (VD4)
  - 1 available for connecting an external LED to VD3

- 6 Photodiodes
  - 4 with Green filters (PD1, PD2 PD3 and PD4)
  - 1 with IR filter (PD B)
  - 1 clear (A) only connected to Light-to-Frequency block
- TIA
  - Trans Impedance Amplifier
- PREFILTER
  - LP & HP Filter and variable Gain Stage
- Synchronous Demodulators
  - SD_OFE1, SD_OEF2 with LP 6 HP filter and gain stage

The first Block in the signal path is the TIA. The TIA converts the current from Photodiodes into a voltage. The trans impedance of TIA can be adjusted in 7 steps. After the TIA follows the PREFILTER. PREFILTER includes a low pass filter with adjustable cut-off frequency, a high pass filter and a variable gain stage. This block can be bypassed. The output signal of PREFILTER is used as input for the blocks SD_OFE1 and SD_OFE2. These Block are identically built and can work in parallel. Both consists of a synchronous demodulator, a low-pass filter, a high pass filter and variable gain stage. The Sequencer controls the whole signal path, which is part of digital part.

In addition to these main blocks, there are two smaller blocks for detection of clipping signals inside the blocks. The TIA Clip detection observes the output of TIA and SD Clip detection observes the output of PREFILTER Block. The limits for clip detection can be adjusted via registers.

7.1.1 LEDs

Two green LEDs are used with anode on pin VD1 and VD2. An IR LED is connected anode pin towards VD4. VD3 allows direct access to the current sink 3

7.1.2 LED-Driver

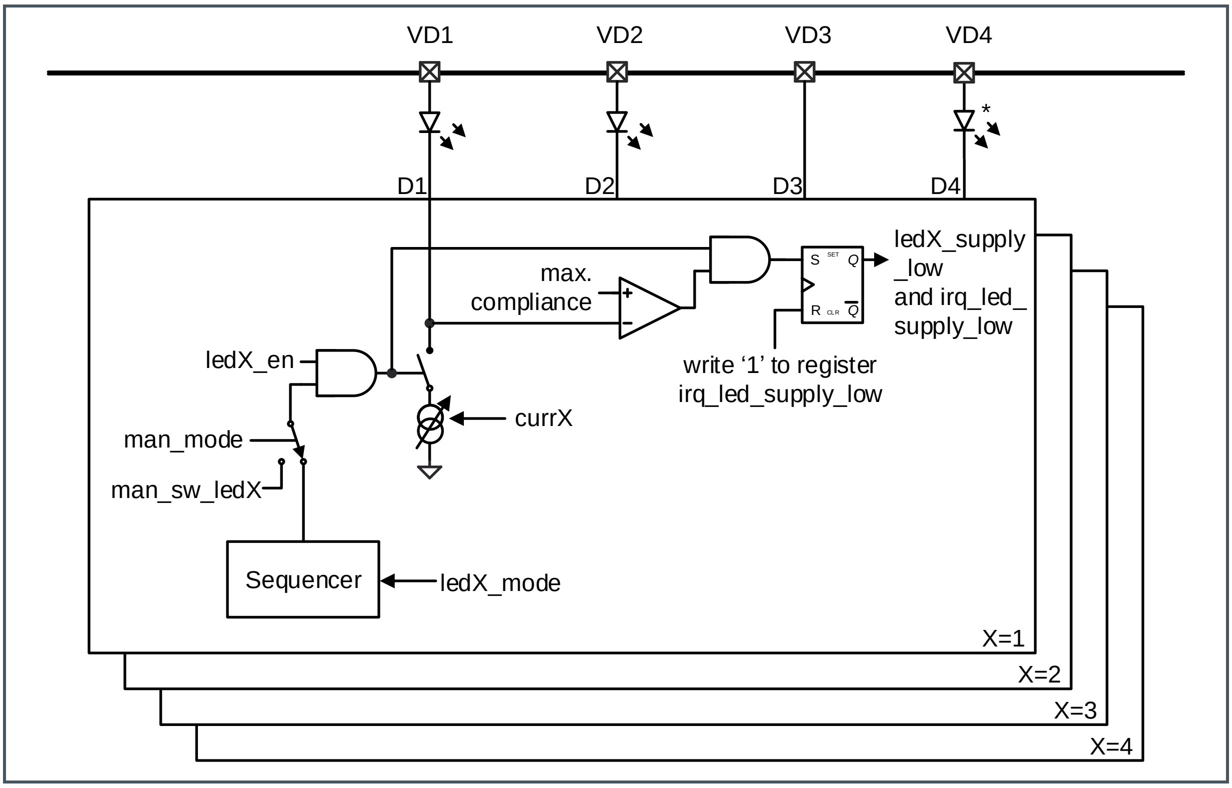
The AS7030B contains 4 identical LED driver circuits.

The LED-driver outputs can be controlled manually or by the built in sequencer. See section 7.1.9 Optical Front End Operating Modes

Information

The integration time t_{INT} is defined either by the sequencer (man_mode=0) of manually through the bit sw_itg if man_mode=1. For the synchronous demodulator only use the resistive feedback.

Figure 10:
LED Drivers



7.1.3 LED Configuration

LED_CFG Register (Address 0x10)

Figure 11:
LED_CFG Register

Addr: 0x10		LED_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sigref_en	0	RW	Signal reference: Is required for all analog blocks (except PD_Amp or light-to-frequency operation) 0: Disable signal reference 1: Enable signal reference

<table>
<tr><th>Addr: 0x10</th><th colspan="4">LED_CFG</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td>6</td><td>sigref_ecg_voltage</td><td>0</td><td>RW</td><td>Voltage setting of SIGREF_ECG – datasheet parameters are guaranteed only for default value of 0.9 V
<table><tr><th>Setting</th><th>Voltage</th></tr><tr><td>0</td><td>0.9 V (default)</td></tr><tr><td>1</td><td>0.8 V</td></tr></table></td></tr>
<tr><td>5:4</td><td>sigref_ofe_voltage</td><td>0</td><td>RW</td><td>Voltage setting of SIGREF – datasheet parameters are guaranteed only for default value of 0.6 V.
<table><tr><th>Setting</th><th>IMAX</th></tr><tr><td>00</td><td>0.6 V (default)</td></tr><tr><td>01</td><td>0.7 V</td></tr><tr><td>10</td><td>0.8 V</td></tr><tr><td>11</td><td>0.9 V</td></tr></table></td></tr>
<tr><td>3</td><td>led4_en</td><td>0</td><td>RW</td><td>0: Disables LED4 output source.
1: Enables LED4 output source.</td></tr>
<tr><td>2</td><td>led3_en</td><td>0</td><td>RW</td><td>0: Disables LED3 output source.
1: Enables LED3 output source.</td></tr>
<tr><td>1</td><td>led2_en</td><td>0</td><td>RW</td><td>0: Disables LED2 output source.
1: Enables LED2 output source.</td></tr>
<tr><td>0</td><td>led1_en</td><td>0</td><td>RW</td><td>0: Disables LED1 output source.
1: Enables LED1 output source.</td></tr>
</table>

The LED_CURR defines the LED output current.

LED_WAIT_LOW Register (Address 0x11)

Figure 12:
LED_WAIT_LOW Register

Addr: 0x11	LED_WAIT_LOW			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Led_wait_low	0	RW	Time = led_wait_low *1 µs

LED_WAIT_LOW defines the time between the switching on of an LED and the beginning of voltage monitoring. All LEDs use the same time

Attention

It is recommended to configure the current only when the output is not active, as there is no latch implemented to keep the 10 bits consistent. New values are applied directly and immediately.

LED1_CURRL Register (Address 0x12)

Figure 13:
LED1_CURRL Register

Addr: 0x12		LED1_CURRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Curr1[1:0]	0	RW	LED1 output current lower 2 bits
5:1	Not used	0	RW	Not used
0	cs1_boost	0	RW	0: Imax = 100 mA, 1 LSB=97 µA 1: Imax = 200 mA, 1 LSB=194 µA

LED1_CURRH Register (Address 0x13)

Figure 14:
LED1_CURRH Register

Addr: 0x13		LED1_CURRH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Curr1[9:2]	0	RW	LED1 output current upper 8 bits -- cs1_boost = 0 V_Dmin = 0.3 V Coding for curr1[9:0]: 000h: 786 µA 001h: 883 µA (1 LSB=97 µA with cs1_boost=0) 002h: 980 µA 166h: 35 mA 3FFh: 100 mA -- cs1_boost = 1 V_Dmin = 0.7 V Coding for curr1[9:0]: 000h: 786 µA

Addr: 0x13		LED1_CURRH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				001h 980 µA (1 LSB=194 µA with cs1_boost=1) 002h: 1.74 mA 166h: 70 mA 3FFh: 200 mA

LED2_CURRL Register (Address 0x14)

Figure 15:
LED2_CURRL Register

Addr: 0x14		LED2_CURRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Curr2[1:0]	0	RW	LED2 output current lower 2 bits
5:1	Not used	0	RW	Not used
0	Cs2_boost	0	RW	0: Imax = 100 mA, 1 LSB=97 µA 1: Imax = 200 mA, 1 LSB=194 µA

LED2_CURRH Register (Address 0x15)

Figure 16:
LED2_CURRH Register

Addr: 0x15		LED2_CURRH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Curr2[9:2]	0	RW	LED2 output current upper 8 bits -- cs2_boost = 0 V_Dmin = 0.3 V Coding for curr1[9:0]: 000h: 786 µA 001h: 883 µA (1 LSB=97 µA with cs1_boost = 0) 002h: 980 µA 166h: 35 mA 3FFh: 100 mA -- cs2_boost = 1 V_Dmin = 0.7 V

Addr: 0x15		LED2_CURRH		
Bit	Bit Name	Default	Access	Bit Description
				Coding for curr1[9:0]: 000h: 786 µA 001h: 980 µA (1 LSB=194 µA with cs1_boost=1) 002h: 1.74 mA 166h: 70 mA 3FFh: 200 mA

LED3_CURRL Register (Address 0x16)

Figure 17:
LED3_CURRL Register

Addr: 0x16		LED3_CURRL		
Bit	Bit Name	Default	Access	Bit Description
7:6	Curr3[1:0]	0	RW	LED3 output current lower 2 bits
5:1	Not used	0	RW	Not used
0	Cs3_boost	0	RW	0: Imax = 100 mA, 1 LSB=97 µA 1: Imax = 200 mA, 1 LSB=194 µA

LED3_CURRH Register (Address 0x17)

Figure 18:
LED3_CURRH Register

Addr: 0x17		LED3_CURRH		
Bit	Bit Name	Default	Access	Bit Description
7:0	Curr3[9:2]	0	RW	LED3 output current upper 8 bits --- cs3_boost = 0 V_Dmin = 0.3 V Coding for curr1[9:0]: 000h: 786 µA 001h: 883 µA (1 LSB=97 µA with cs1_boost = 0) 002h: 980 µA 166h: 35 mA 3FFh: 100 mA ---

Addr: 0x17		LED3_CURRH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				cs3_boost = 1 V_Dmin = 0.7 V Coding for curr1[9:0]: 000h: 786 µA 001h: 980 µA (1 LSB=194 µA with cs1_boost=1) 002h: 1.74 mA 166h: 70 mA 3FFh: 200 mA

LED4_CURRL Register (Address 0x18)

Figure 19:
LED4_CURRL Register

Addr: 0x18		LED4_CURRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Curr4[1:0]	0	RW	LED4 output current lower 2 bits
5:1	Not used	0	RW	Not used
0	Cs4_boost	0	RW	0: Imax = 100 mA, 1 LSB=97 µA 1: Imax = 200 mA, 1 LSB=194 µA

LED4_CURRH Register (Address 0x19)

Figure 20:
LED4_CURRH Register

Addr: 0x19		LED4_CURRH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Curr4[9:2]	0	RW	LED4 output current upper 8 bits -- cs4_boost = 0 V_Dmin = 0.3 V Coding for curr1[9:0]: 000h: 786 µA 001h: 883 µA (1 LSB=97 µA with cs1_boost = 0) 002h: 980 µA 166h: 35 mA

Addr: 0x19		LED4_CURRH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				3FFh: 100 mA --- cs3_boost = 1 V_Dmin = 0.7 V Coding for curr1[9:0]: 000h: 786 µA 001h: 980 µA (1 LSB=194 µA with cs1_boost=1) 002h: 1.74 mA 166h: 70 mA 3FFh: 200 mA

LED12_MODE Register (Address 0x2c)

Figure 21:
LED12_MODE Register

Addr: 0x2c		LED12_MODE			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	man-sw_led2	0	RW	Function enabled only in manual mode 0: LED output D2 disabled. (High impedance) 1: LED output D2 enabled	
6.4	led2_mode	0	RW	LED2 mode	
				Settings	**Behavior**
				000	Always OFF
				001	Always ON when sequencer is active
				010	Controlled by sequencer
				011	Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.
				100	Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.
				101	Controlled by sequencer, only ON in every fourth iteration, starting at 1: 1, 5, 9 etc.
				110	Controlled by sequencer: secondary LED timing
				111	Do not use

Addr: 0x2c		LED12_MODE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	man_sw_led1	0	RW	Function enabled only in manual mode 0: LED output D1 disabled. (High impedance) 1: LED output D1 enable
2.0	led1_mode	0	RW	LED1 mode **Settings** / **Behavior** 000: Always OFF 001: Always ON when sequencer is active 010: Controlled by sequencer 011: Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc. 100: Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc. 101: Controlled by sequencer, only ON in every fourth iteration, starting at 1: 1, 5, 9 etc. 110: Controlled by sequencer: secondary LED timing 111: Do not use

LED34_MODE Register (Address 0x2d)

Figure 22:
LED34_MODE Register

Addr: 0x2d		LED34_MODE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	man-sw_led4	0	RW	Function enabled only in manual mode 0: LED output D4 disabled. (High impedance) 1: LED output D4 enabled
6.4	led4_mode	0	RW	LED4 mode **Settings** / **Behavior** 000: Always OFF 001: Always ON when sequencer is active 010: Controlled by sequencer 011: Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.

Addr: 0x2d		LED34_MODE			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				100	Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.
				101	Controlled by sequencer, only ON in every fourth iteration, starting at 1: 1, 5, 9 etc.
				110	Controlled by sequencer: secondary LED timing
				111	Do not use
3	man_sw_led3	0	RW	Function enabled only in manual mode 0: LED output D3 disabled. (High impedance) 1: LED output D3 enable	
2.0	led3_mode	0	RW	LED3 mode	
				Settings	**Behavior**
				000	Always OFF
				001	Always ON when sequencer is active
				010	Controlled by sequencer
				011	Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc.
				100	Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc.
				101	Controlled by sequencer, only ON in every fourth iteration, starting at 1: 1, 5, 9 etc.
				110	Controlled by sequencer: secondary LED timing
				111	Do not use

The MAN_SEQ_CFG register is used to configure the operation of the optical front end

MAN_SEQ_CFG Register (Address 0x2e)

Figure 23:
MAN_SEQ_CFG Register

Addr: 0x2e		MAN_SEQ_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	man_mode	0	RW	0: Enables Sequencer 1: Enables Manual control of optical front end

<table>
<tr><th>Addr: 0x2e</th><th colspan="4">MAN_SEQ_CFG</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td>6</td><td>man_sw_sd mult</td><td>0</td><td>RW</td><td>If man_mode=1
0: Disables synchronous demodulator multiplication
1: Enables synchronous demodulator multiplication</td></tr>
<tr><td>5</td><td>man_sw_sd pol</td><td>0</td><td>RW</td><td>If man_mode=1
0: Negative polarity in synchronous demodulator multiplication
1: Positive polarity in synchronous demodulator multiplication</td></tr>
<tr><td>4</td><td>man_sw_itg</td><td>0</td><td>RW</td><td>If man_mode=1
0: All integrator capacitors are shorted. Integrator is reset
1: Integrator capacitors are charging up. Integrator is running</td></tr>
<tr><td>3:1</td><td>diode_ctrl</td><td>0</td><td>RW</td><td>Connection of Photodiodes PD1, PD2, PD3, PD4 to the photodiode amplifier.
0: PD1-PD4 are connected
1: PD1 synchronous to LED1, PD2 sync/to LED2 PD3 sync/to LED3, PD4 sync/to LED4
2: PD1 synchronous to LED1, PD2 sync/to LED1 PD3 sync/to LED2, PD4 sync/to LED2
3: PD1 synchronous to LED1, PD2 sync/to LED1 PD3 sync/to LED4, PD4 sync/to LED4
4: SPO2 mode *(obsolete): (negedge(sdm1) or negedge(sdp1)) - PD1=0 PD2=0 PD3=1 PD4=1; (negedge(sdm2) or negedge(sdp2)) - PD1=1 PD2=1 PD3=0 PD4=0
Note that PD_CFG.pdX takes precedence - to turn OFF one photo diode, the respective bit has to be de-asserted in the PD_CFG register.
<table>
<tr><th>PD_CFG.pdX</th><th>diode_ctrl</th><th>Photo Diode 1</th><th>Photo Diode 2</th><th>Photo Diode 3</th><th>Photo Diode 4</th></tr>
<tr><td>0</td><td>xx</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>LED1</td><td>LED2</td><td>LED3</td><td>LED4</td></tr>
<tr><td>1</td><td>2</td><td>LED1</td><td>LED1</td><td>LED2</td><td>LED2</td></tr>
<tr><td>1</td><td>3</td><td>LED1</td><td>LED1</td><td>LED4</td><td>LED4</td></tr>
<tr><td>1</td><td>4</td><td colspan="4">SPO2 mode (obsolete)</td></tr>
<tr><td>1</td><td>5..7</td><td colspan="4">Do not use</td></tr>
</table></td></tr>
<tr><td>0</td><td>seq_en</td><td>0</td><td>RW</td><td>0: Disables sequencer
1: Enables sequencer</td></tr>
</table>

LEDSTATUS Register (Address 0xa3)

Figure 24:
LEDSTATUS Register

Addr: 0xa3		LEDSTATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	NA	0	RO	Not used
3	led4_supply_low	0	RO	If this bit is asserted, LED4 voltage has been too low.
2	led3_supply_low	0	RO	If this bit is asserted, LED3 voltage has been too low.
1	led2_supply_low	0	RO	If this bit is asserted, LED2 voltage has been too low.
0	led1_supply_low	0	RO	If this bit is asserted, LED1 voltage has been too low.

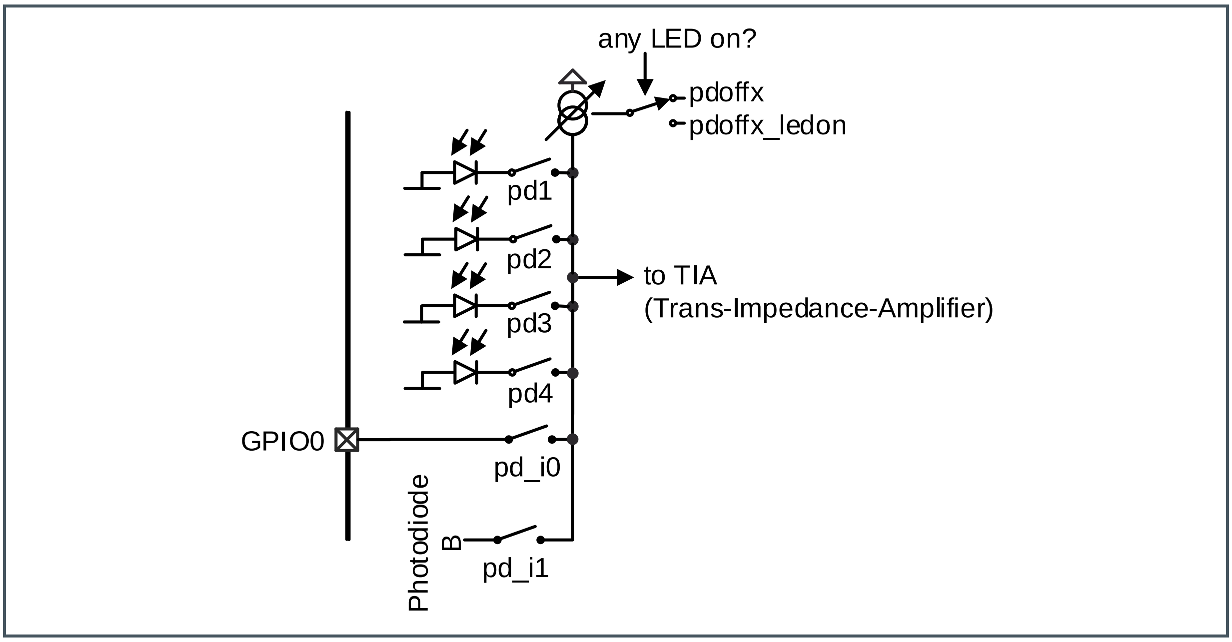
An asserted bit can be cleared by either writing a '1' to the STATUS.clipdetect bit (in normal mode) or by reading the CLIPSTATUS register (clear on read mode)

7.1.4 Photodiode Selection

In order to have flexible arrangement of the use photodiodes, PD1-PD4 can be individually connected to the photodiode amplifier input. The optional offset current allows cancellation of constant light sources like sunlight. In case of an external photodiode or any other sensor with (low) current output, the pins GPIO0 and GPIO1 can be used as input.

Additionally the sequencer can control the diodes – see diode_ctrl described in register MAN_SEQ_CFG.

Figure 25:
Photodiode Selection



PD_CFG Register (Address 0x1a)

Figure 26:
PD_CFG Register

Addr: 0x1a		PD_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	NA	0	RW	Not used
6	pd_boost	0	RW	pd_boost = 0 pdoffx_ledoff lsb = 10 nA pdoffx_ledon lsb = 10 nA
				pd_boost = 1 pdoffx_ledoff lsb = 20 nA pdoffx_ledoonlsb = 20 nA
5	pd4	0	RW	0: Photodiode PD4 is disconnected from photo amplifier 1: Photodiode PD4 is connected to photo amplifier (as defined in diode_ctrl)

Addr: 0x1a		PD_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	pd3	0	RW	0: Photodiode PD3 is disconnected from photo amplifier 1: Photodiode PD3 is connected to photo amplifier (as defined in diode_ctrl)
3	pd2	0	RW	0: Photodiode PD2 is disconnected from photo amplifier 1: Photodiode PD2 is connected to photo amplifier (as defined in diode_ctrl)
2	pd1	0	RW	0: Photodiode PD1 is disconnected from photo amplifier 1: Photodiode PD1 is connected to photo amplifier (as defined in diode_ctrl)
1	pd_i1	0	RW	0: Photodiode B (see Photodiode Characteristics) disconnected from TIA input 1: Photodiode B (see Photodiode Characteristics) connected to TIA input; set ltf1_sel=0 and ltf2_sel=0.
0	pd_i0	0	RW	0: GPIO0-input is disconnected from photo amplifier 1: GPIO0-input is connected to photo amplifier; set gpio_a[0]=1.

The PD_CFG register is used to configure the input to the photo amplifier.

PDOFFX_LEDOFF Register (Address 0x1b)

Figure 27:
PDOFFX_LEDOFF Register

Addr: 0x1b		PDOFFX_LEDOFF		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	pdoffx_ledoff	0	RW	Input offset current if all LEDs are OFF (all sw_led* sequencer outputs are zero) Ioffset = pdoffx_ledoff*10 nA if PD_CFG[6] = 0 Ioffset = pdoffx_ledoff*20 nA if PD_CFG[6] = 1 0: Offset source is turned OFF

PDOFFX_LEDON Register (Address 0x1c)

Figure 28:
PDOFFX_LEDON Register

Addr: 0x1c		PDOFFX_LEDON		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	pdoffx_ledon	0	RW	Input offset current if at least one LED is ON (one or more sw_led* sequencer outputs are non-zero) Ioffset = pdoffx_ledon*10nA if PD_CFG[6] = 0 Ioffset = pdoffx_ledon*20nA if PD_CFG[6] = 1 0: Offset source is turned OFF

7.1.5 Photodiode Characteristics

Figure 29:
Photodiode Arrangement –Orientation as in Figure 2

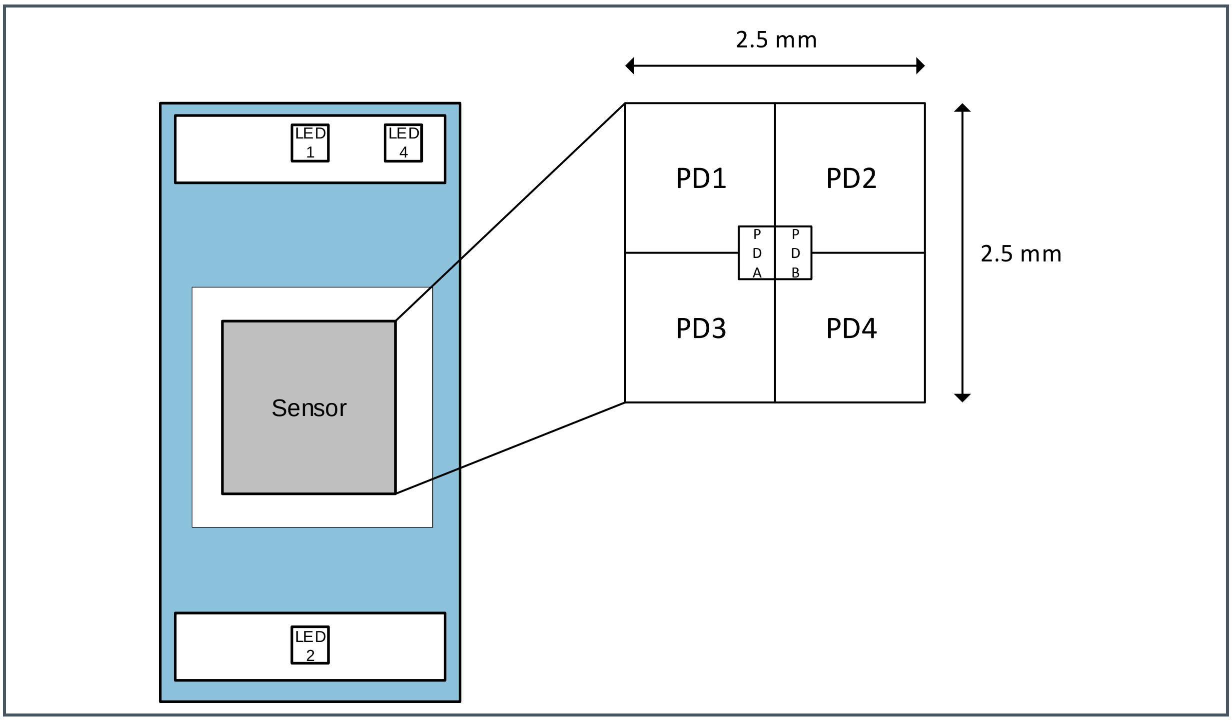
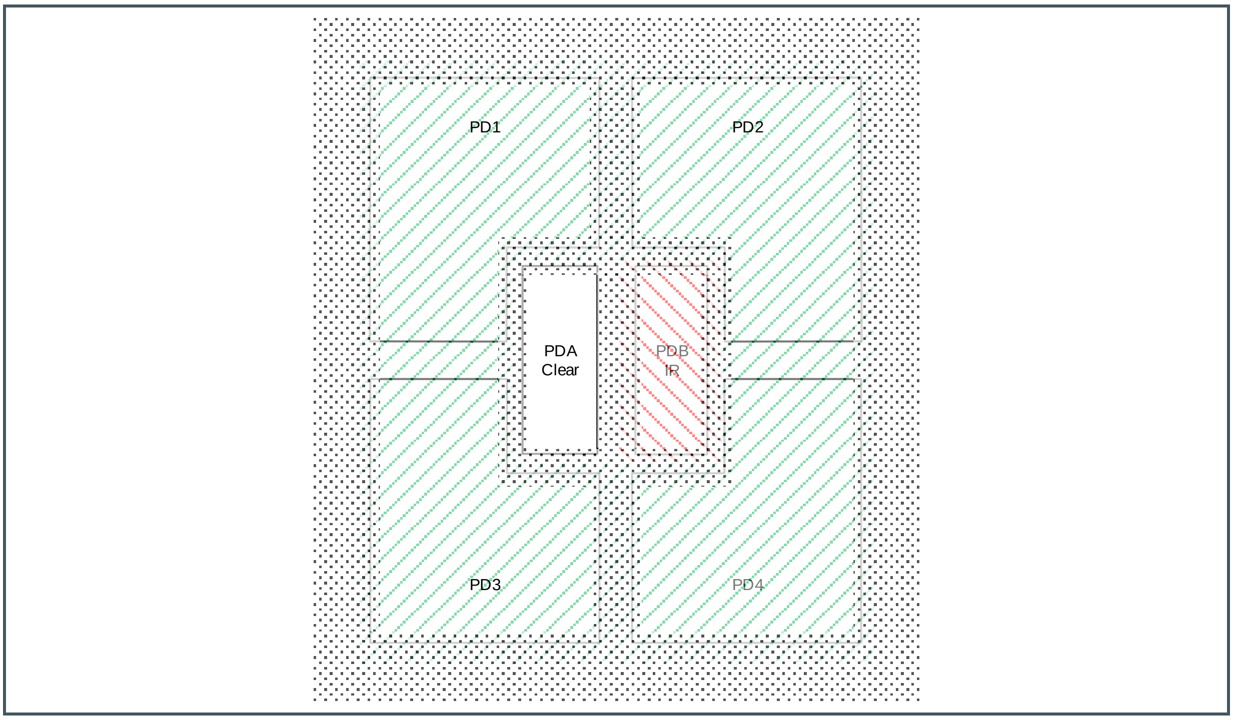
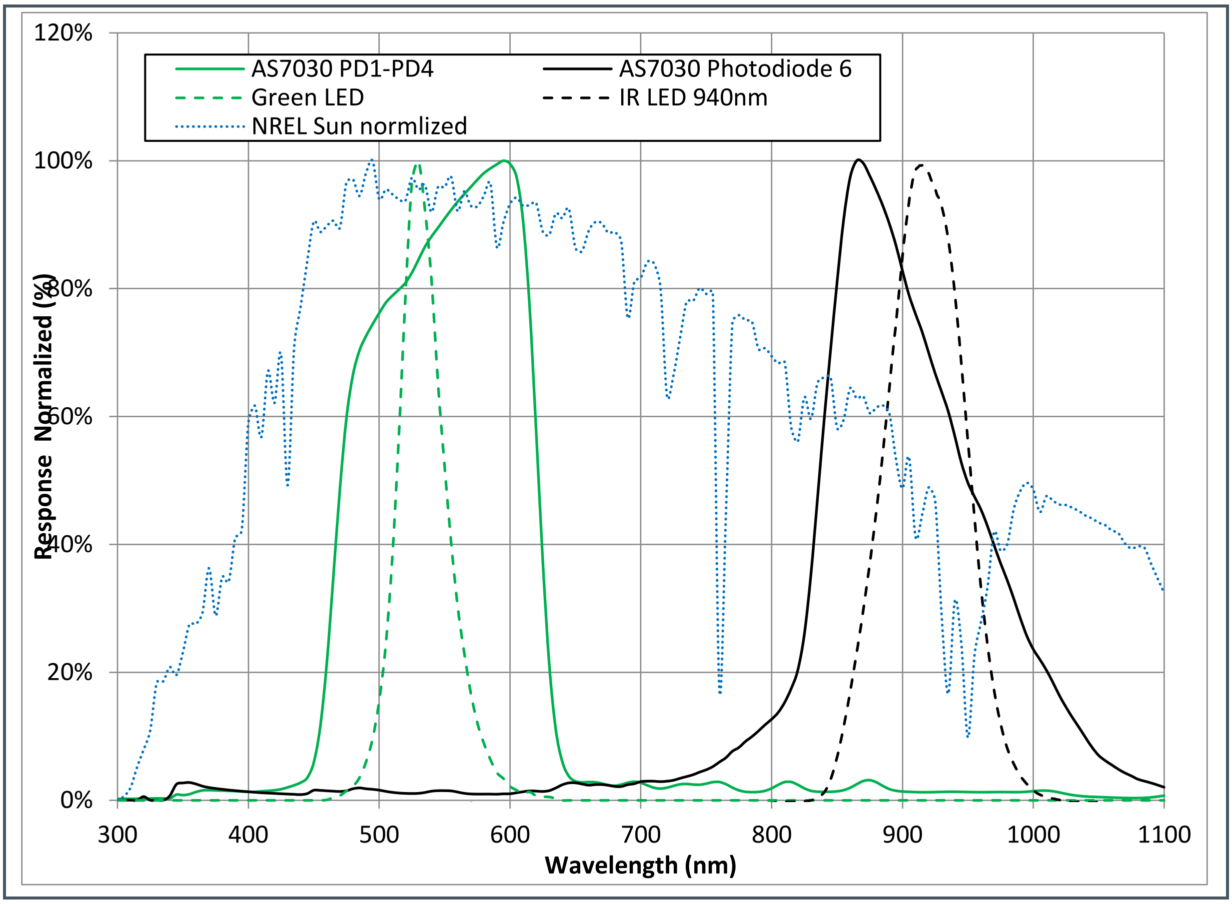


Figure 30:
Photodiode Filter Implementation



For operation and characteristics of photodiode 'PDA' and photodiode 'PDB' see section 7.1.14 Light-to-Frequency Mode.

Figure 31:
Photodiode Sensitivity (solid green and black) and LED Emission Spectrum (dotted green and dotted black)



Information

All 4 photodiodes used pd1/2/3/4=1; perpendicular light source and no diffusor used on AS7030B; due to the difference in photodiode size the absolute response for Photodiode 6 (0.01 mm^2) is much lower compared to PD1-PD4 (2.5 mm^2)

7.1.6 Photodiode Trans-Impedance Amplifier (TIA)

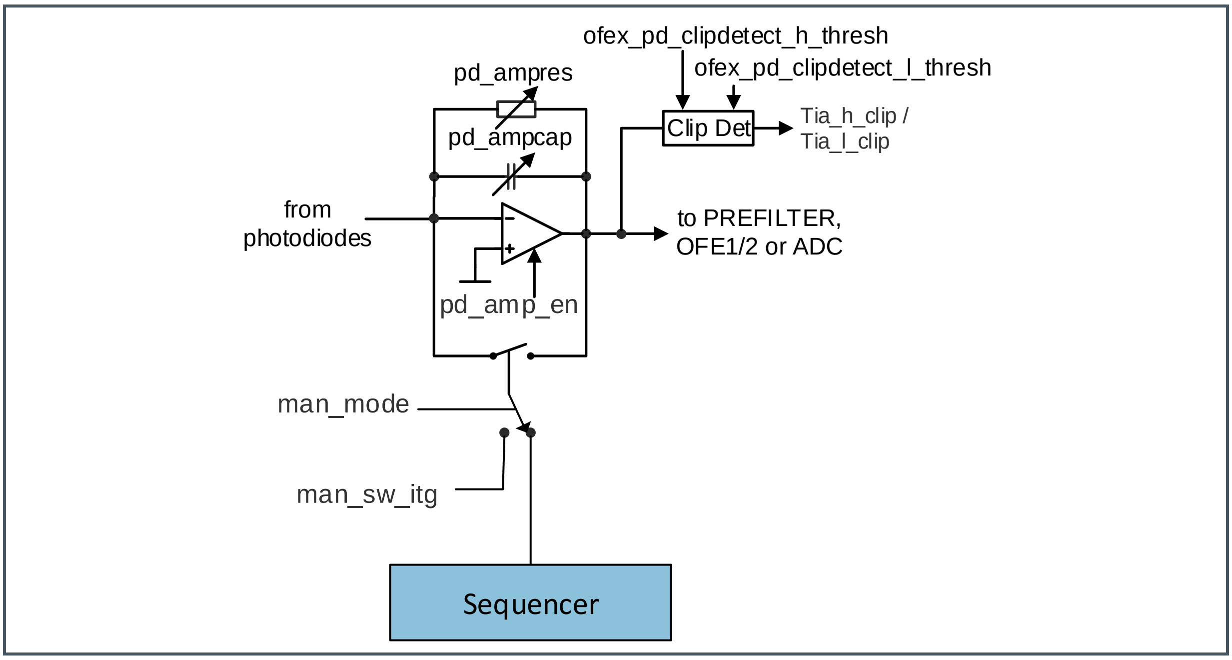
The Trans-Impedance Amplifier is used to convert the photocurrent into voltage.

The photodiode amplifier can be configured in two different modes:

- Photocurrent to voltage converter
- Photocurrent integrator

TIA block also includes a clip detection block.

Figure 32:
TIA



Use following settings for the programming of the TIA:

Figure 33:
TIA Programming Settings

pd_ampres	pd12341	pd_ampcap	pd_ampcomp	pd_ampvo	Gain
1	1…4	13	1	15	1 V/µA
2	1…4	7	1	15	2 V/µA
3	1…4	5	1	15	3 V/µA
4	1…2	2	0	15	5 V/µA
	3…4	3			
5	1…2	2	0	15	7 V/µA
	3…4	3			
6	1	1	0	15	10 V/µA
	2…4	2			
7	1…2	1	0	15	15 V/µA
	3…4	2			

pd_ampres	pd12341	pd_ampcap	pd_ampcomp	pd_ampvo	Gain
Low Bandwidth Mode					
5	1…4	31	3	15	7 V/µA
Integrating Mode (pd_ampres=0)					
0	1…4	10	3	15	1 V/pQ
0	1…4	20	3	15	1/2V/pQ
0	1…4	30	3	15	1/3V/pQ

(1) pd1234 … number of active photodiodes (for example, pd1=1, pd2=0, pd3=1, pd4=0 -> pd1234=2)

7.1.7 Photodiode TIA Registers

PD_AMPRCCFG Register (Address 0x1d)

Figure 34:
PD_AMPRCCFG Register

Addr: 0x1d		PD_AMPRCCFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	pd_ampres	0	RW	Feedback resistor	
				Setting	**Resistance**
				0	No resistor in feedback of amplifier – photocurrent integrator
				1	1 MΩ
				2	2 MΩ
				3	3 MΩ
				4	5 MΩ
				5	7 MΩ
				6	10 MΩ
				7	15 MΩ
4:0	pd_ampcap			Feedback capacitor =pd_ampcap * 0.1 pF	

The PD_AMPCFG register is used to configure the operating mode of the photoamplifier.

PD_AMPCFG Register (Address 0x1e)

Figure 35:
PD_AMPCFG Register

Addr: 0x1e		PD_AMPCFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	pd_amp_en	0	RW	0: Activates power down mode of photo-amplifier 1: Enables photo-amplifier (direct or automatic pd_amp_auto mode) also set en_bias_ofe=1
6	pd_amp_auto	0	RW	0: Normal TIA mode 1: Enable TIA only when seq_itg is set (i.e. controlled by sequencer itg setting) also set en_bias_ofe=1
5:2	pd_ampvo	1	RW	OpAmp offset can be used to limit signal in darkness and to shorten rise times
1:0	pd_ampcomp	3	RW	OpAmp compensation, depending on gain and number of used photo diodes Capacitor = pd_ampcap*0.1 pF

OFE1_PD_THCFG Register (Address 0x1f)

Figure 36:
OFE1_PD_THCFG Register

Addr: 0x1f		OFE1_PD_THCFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ofe1_pd_clipdetect_h_thresh	0	RW	If the voltage on the output of the TIA exceed this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as 0: 1824 mV 1: 1748 mV 2: 1672 mV 3: 1596 mV 4: 1520 mV 5: 1444 mV 6: 1368 mV 7: 1292 mV

Addr: 0x1f		OFE1_PD_THCFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				8: 1216 mV 9: 1140 mV 10: 1064 mV 11: 988 mV 12: 912 mV 13: 836 mV 14: 760 mV 15: 684 mV
3:0	ofe1_pd_clipdetect_l_thresh	0	RW	If the voltage on the output of the OFE2 falls below this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as 0: 76.2 mV 1: 152 mV 2: 228 mV 3: 304 mV 4: 380 mV 5: 456 mV 6: 532 mV 7: 608 mV 8: 684 mV 9: 760 mV 10: 836 mV 11: 912 mV 12: 988 mV 13: 1064 mV 14: 1140 mV 15: 1216 mV

OFE2_PD_THCFG (Address 0x56)

Figure 37:
OFE2_PD_THCFG Register

Addr: 0x56		OFE2_PD_THCFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ofe2_pd_clipd_h_thresh	0	RW	If the voltage on the output of the TIA exceed this threshold, the irq_clipdetect interrupt is asserted. The threshold is defined as 0: 1824 mV 1: 1748 mV 2: 1672 mV 3: 1596 mV 4: 1520 mV 5: 1444 mV 6: 1368 mV 7: 1292 mV 8: 1216 mV 9: 1140 mV 10: 1064 mV 11: 988 mV 12: 912 mV 13: 836 mV 14: 760 mV 15: 684 mV
3:0	ofe2_sd_clipd_l_thresh	0	RW	If the voltage on the output of the OFE2 falls below this threshold, the irq_clipdetect interrupt is asserted. The threshold is defined as 0: 76.2 mV 1: 152 mV 2: 228 mV 3: 304 mV 4: 380 mV 5: 456 mV 6: 532 mV 7: 608 mV 8: 684 mV

Addr: 0x56		OFE2_PD_THCFG		
Bit	Bit Name	Default	Access	Bit Description
				9: 760 mV 10: 836 mV 11: 912 mV 12: 988 mV 13: 1064 mV 14:1140 mV 15: 1216 mV

7.1.8 Voltage Mode of the Photodiode Amplifier

The output voltage of the photodiode amplifier is depending on the feedback component.

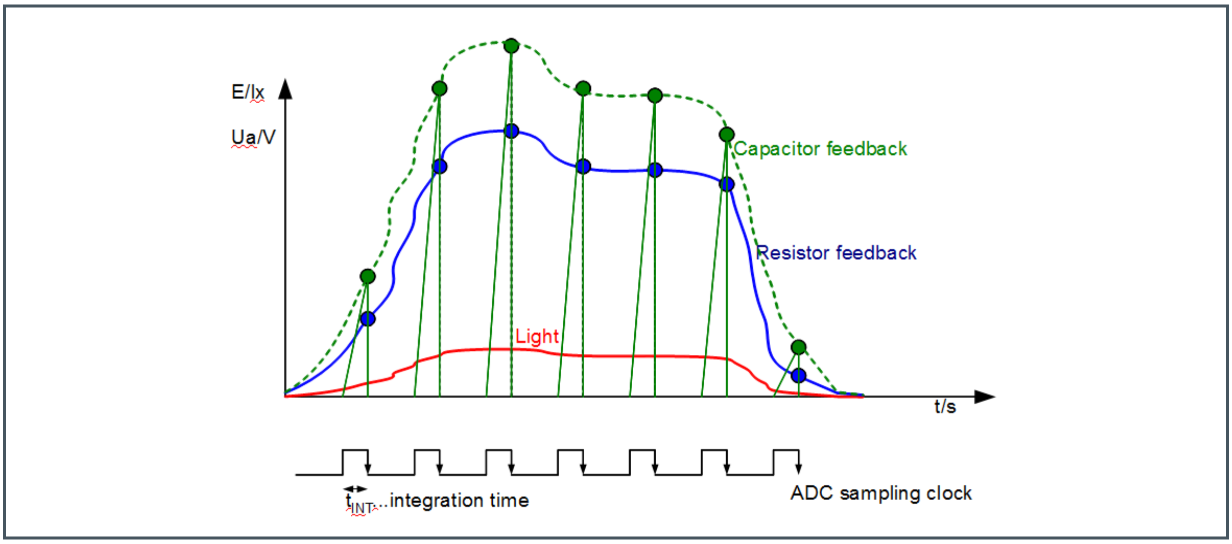
Equation 1:

$$Uout = Iphoto \cdot Rfb$$ Feedback resistor

Equation 2:

$$Uout = Iphoto \cdot \frac{tINT}{Cfb}$$ Feedback capacitor

Figure 38:
Difference Between Resistive and Capacitive Feedback



(1) **Green**: Capacitive Integration
Green Dotted: Effective Value from Capacitive Mode
Blue: Resistive Feedback
Red: Light Intensity

Information

The integration time t_{INT} is defined either by the sequencer (man_mode=0) of manually through the bit sw_itg if man_mode=1. For the synchronous demodulator only use the resistive feedback.

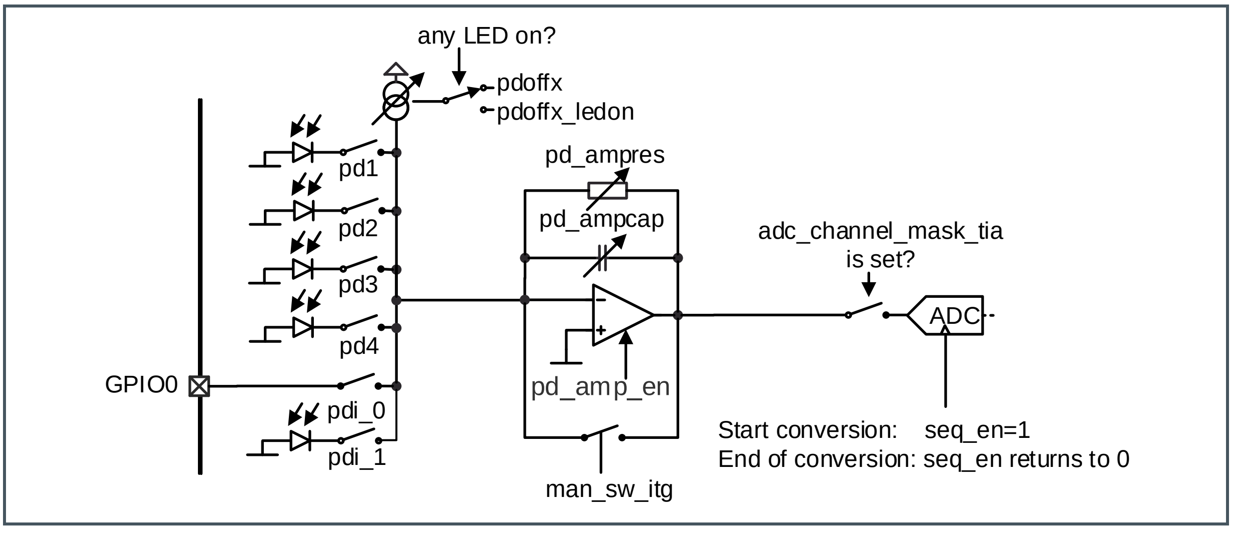
7.1.9 Optical Front End Operating Modes

Once the photodiode amplifier is configured the measurement can be done in two different ways. Either the LED-outputs, the photodiode amplifier and the ADC are controlled manually by means of register bits, or they are controlled by a built in sequencer.

Manual Operation of the Optical Frontend:

The optical front end can be manually controlled via the register man_mode=1

Figure 39:
Optical Frontend



(1) Applies only if man_mode=1.

For manual operation of the LEDs and its current sinks see 7.1.2 LED-Driver

7.1.10 Sequencer

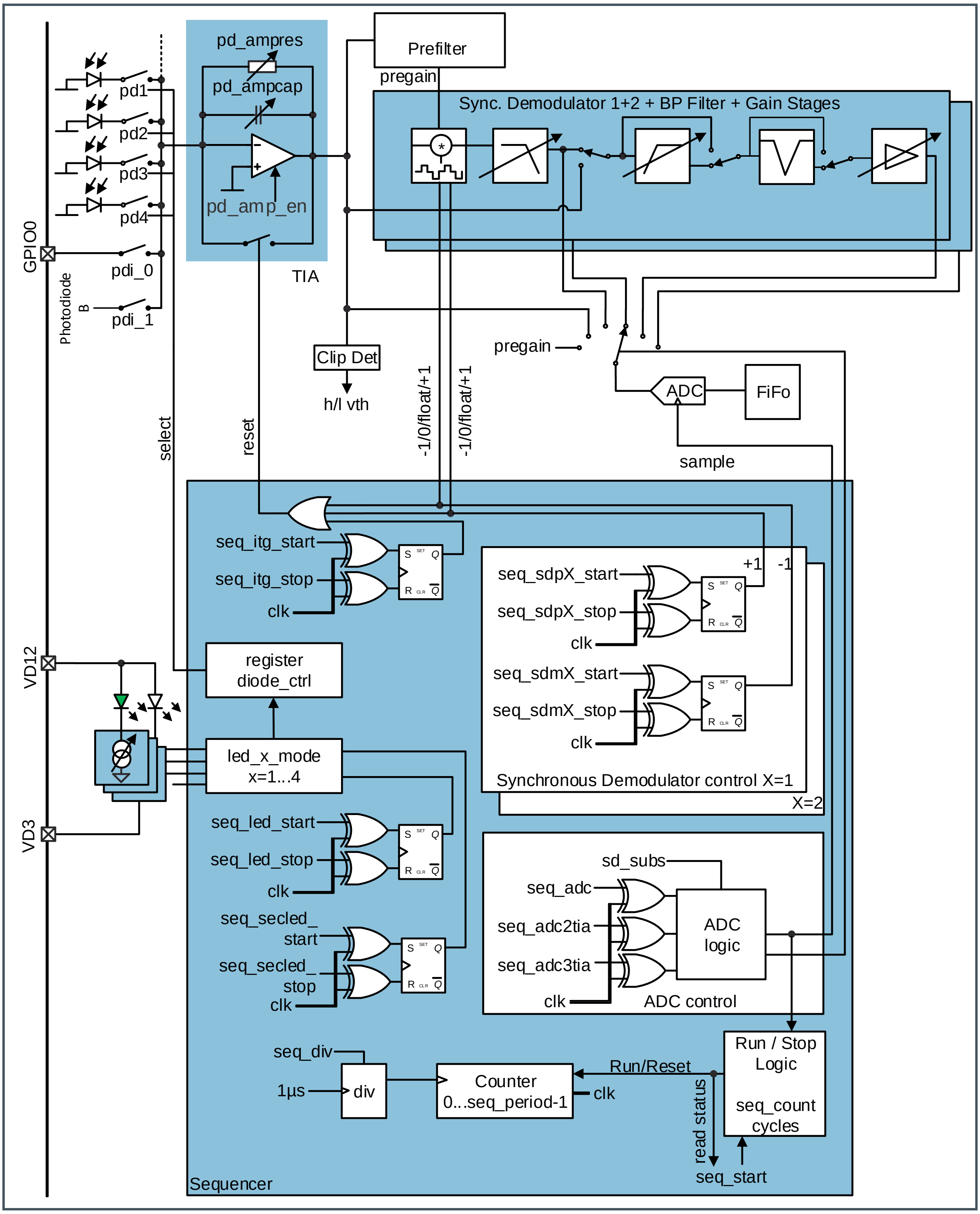
In order to synchronize the LED-currents, the integration time and the ADC-sampling time, a built in sampling sequencers can be used. The sequencer generates the 8-bit-timings based on a 1 µs clock which can be pre-scaled with seq_div. The results of the analog to digital conversion are automatically stored in a pipeline buffer or in register adc_data and the ADC FIFO.

The timings can be programmed with following registers (apply for man_mode=0):

Figure 40:
Timing Registers

Register	Description
seq_div	Divider of the 1 µs input clock for all sequencer timings
seq_count	Number of measurements in one sequence
seq_start	Writing 1 starts the sequencer, 0 stops the sequencer
seq_period	Time of one measurement cycle
seq_led_start	Start time of the LED drivers within one cycle
seq_led_stop	Stop time of the LED drivers within one cycle
seq_secled_start	Start time of the secondary LED drivers within one cycle (used for SpO2)
seq_secled_stop	Stop time of the secondary LED drivers within one cycle (used for SpO2)
seq_itg_start	Start time of the integrator
seq_itg_stop	Stop time of the integrator
seq_sdp1_start	Start time of the synchronous demodulator's 1 positive multiplication
seq_sdp1_stop	Stop time of the synchronous demodulator's 1 positive multiplication
seq_sdm1_start	Start time of the synchronous demodulator's 1 negative multiplication
seq_sdm1_stop	Stop time of the synchronous demodulator's 1 negative multiplication
seq_sdp2_start	Start time of the synchronous demodulator's 2 positive multiplication
seq_sdp2_stop	Stop time of the synchronous demodulator's 2 positive multiplication
seq_sdm2_start	Start time of the synchronous demodulator's 2 negative multiplication
seq_sdm2_stop	Stop time of the synchronous demodulator's 2 negative multiplication
seq_adc	Sampling position of the ADC
seq_adc2tia, seq_adc3tia	If the TIA channel is selected allow a second (and third) conversion within this cycle.
sd_subs, sd_subs_always	Synchronous demodulator subsampling ratio between sequencer frequency and ADC sampling frequency.
ulp	Ultra low power bit for the sequencer. If this bit is set and sd_subs>0, it disables the LED pulses and powers off the TIA in all sequences but the one where the TIA is sampled. This bit can be used to optimize the power consumption of the LEDs and the AS7030B (This bit is located in ADC_CFGB Register bit 1)
irq_adc_timing_error	The sequencer setup caused a timing error on ADC conversion.

Figure 41:
Block Diagram of Sequencer



7.1.11 Sequencer Registers

SEQ_CNT Register (Address 0x30)

Figure 42:
SEQ_CNT Register

Addr: 0x30		SEQ_CNT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_count	0	RW	Number of measurements in one sequence. If seq_count = 0x0 the sequencer is running continuously if started by seq_start=1 or seq_start_sync=1. This register is reset by disabling/enabling of seq_start=0 (but not by osc_off=1)

SEQ_DIV Register (Address 0x31)

Figure 43:
SEQ_DIV Register

Addr: 0x31		SEQ_DIV		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_div	0	RW	Divider value Sequencer time increment tclk = (seq_div + 1) * 1 µs

The SEQ_DIV register sets the input divider for the main clock.

SEQ_START (Address 0x32)

Figure 44:
SEQ_START Register

Addr: 0x32		SEQ_START		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Not used	0	R_PUSH	Not used

Addr: 0x32		SEQ_START		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	seq_start_gpio	0	R_PUSH	After programming, the sequencer waits for a synchronization pulse via GPIO (see register GPIO_SYNC). For all released ADC channels a value is recorded per synchronization pulse (see register ADC_CHANNEL).
1	seq_start_sync	0	R_PUSH	Similar to seq_start, but the sequencer will wait for overflow of the frequency divider that feeds all the switched-cap filters. This means 1) That it could take anything between 0 and 8 ms before the sequencer actually starts. 2) That the generated frequencies are in phase with the sequencer. For this to have any effect, the sequencer period should be selected with the selected frequencies (sd_bw, hp_freq) in mind.
0	seq_start	0	R_PUSH	Writing 1 starts the sequencer(s) in the according to the configuration and upon rising edge of seq_start ADC selects first channel. Writing 0 stops the sequencer(s). In manual mode, writing 1 starts one ADC conversion but does not initialize the ADC channel selection. Reading returns 1 if the sequencer is running (sequencer mode), respectively if the ADC is converting (manual mode)

With the SEQ_START register sets the configured sequencer can be started

SEQ_PER (Address 0x33)

Figure 45:
SEQ_PER Register

Addr: 0x33		SEQ_PER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_period	0	RW	t_period Sequencer period T = t_period * (seq_div+1) * 1 µs

The SEQ_PER register sets one measurement cycle of the sequencer.

SEQ_LED_STA (Address 0x34)

Figure 46:
SEQ_LED_STA Register

Addr: 0x34		SEQ_LED_STA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_led_start	0	RW	LED start time

The SEQ_LED_STA register sets the LED drive timing. Data is stored as 8-bit value.

SEQ_LED_STO (Address 0x35)

Figure 47:
SEQ_LED_STO Register

Addr: 0x35		SEQ_LED_STO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_led_stop	0	RW	LED stop time

The SEQ_LED_STO register sets the LED drive timing. Data is stored as 8-bit value.

SEQ_SECLED_STA (Address 0x36)

Figure 48:
SEQ_SECLED_STA Register

Addr: 0x36		SEQ_SECLED_STA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_secled_start	0	RW	Secondary LED start time

The SEQ_LED register sets the secondary LED drive timing which is used in ledX_mode 6 only. Data is stored as 8-bit value.

SEQ_SECLED_STO (Address 0x37)

Figure 49:
SEQ_SECLED_STO Register

Addr: 0x37		SEQ_SECLED_STO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_secled_stop	0	RW	Secondary LED stop time

SEQ_ITG_STA (Address 0x38)

Figure 50:
SEQ_ITG_STA Register

Addr: 0x38		SEQ_ITG_STA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_itg_start	0	RW	Integrator start time (start time=1 and stop time=0 means that it is - by default - always ON) Turning OFF the integrator actually means discharge the capacitor. This is only useful in capacitive integration mode, without the synchronous demodulator.

The SEQ_ITG register sets the photoamplifier integration time. Data is stored as 8-bit value.

SEQ_ITG_STO (Address 0x39)

Figure 51:
SEQ_ITG_STO Register

Addr: 0x39		SEQ_ITG_STO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_itg_stop	0	RW	Integrator stop time

SEQ_SDP1_STA (Address 0x3a)

Figure 52:
SEQ_SDP1_STA Register

Addr: 0x3a		SEQ_SDP1_STA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_sdp1_start	0	RW	Positive multiplication start time 1

The SEQ_SDP register sets the synchronous demodulator positive multiplication time. Data is stored as 8-bit value.

SEQ_SDP1_STO (Address 0x3b)

Figure 53:
SEQ_SDP1_STO Register

Addr: 0x3b		SEQ_SDP1_STO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_sdp1_stop	0	RW	Positive multiplication stop time 1

SEQ_SDP2_STA (Address 0x3c)

Figure 54:
SEQ_SDP2_STA Register

Addr: 0x3c		SEQ_SDP2_STA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_sdp2_start	0	RW	Positive multiplication start time 2

The SEQ_SDP register sets the synchronous demodulator positive multiplication time. Data is stored as 8-bit value.

SEQ_SDP2_STO (Address 0x3d)

Figure 55:
SEQ_SDP2_STO Register

Addr: 0x3d		SEQ_SDP2_STO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_sdp2_stop	0	RW	Positive multiplication stop time 2

SEQ_SDM1_STA (Address 0x3e)

Figure 56:
SEQ_SDM1_STA Register

Addr: 0x3e		SEQ_SDM1_STA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_sdm1_start	0	RW	Negative multiplication start time 1

The SEQ_SDM1 register sets the synchronous demodulator negative multiplication time 1. Data is stored as 8-bit value

SEQ_SDM1_STO (Address 0x3f)

Figure 57:
SEQ_SDM1_STO Register

Addr: 0x3f		SEQ_SDM1_STO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_sdm1_stop	0	RW	Negative multiplication stop time 1

SEQ_SDM2_STA (Address 0x40)

Figure 58:
SEQ_SDM2_STA Register

Addr: 0x40		SEQ_SDM2_STA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_sdm2_start	0	RW	Negative multiplication start time 2

The SEQ_SDM2 register sets the synchronous demodulator negative multiplication time 2. Data is stored as 8-bit value.

SEQ_SDM2_STO (Address 0x41)

Figure 59:
SEQ_SDM2_STO Register

Addr: 0x41		SEQ_SDM2_STO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_sdm2_stop	0	RW	Negative multiplication stop time 2

SEQ_ADC (Address 0x42)

Figure 60:
SEQ_ADC Register

Addr: 0x42		SEQ_ADC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_adc	0	RW	**ADC start sampling time** The ADC conversion needs to be finished before the sequencer period ends otherwise ADC samples can be lost.

The SEQ_ADC register defines the time when the ADC starts sampling during each measurement cycle.

SEQ_ADC2TIA (Address 0x43)

Figure 61:
SEQ_ADC2TIA Register

Addr: 0x43		SEQ_ADC2TIA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_adc2tia	0	RW	ADC second sampling time for TIA: If this time is non-zero, an ADC conversion is started at the given cycle, but only if adc_sel is currently selecting TIA. For all other channels, there is only a single ADC conversion executed in the sequencer period. **Warning**: If non-zero, seq_adc must be non-zero as well, and seq_adc2tia bigger than seq_adc. The difference must be high enough so that the second ADC conversion is started after the first ADC conversion has finished. Also, if the seq_adc2tia features is used, there is the additional restriction that the second ADC conversion has to be finished before the end of the sequencer period.

SEQ_ADC3TIA (Address 0x44)

Figure 62:
SEQ_ADC3TIA Register

Addr: 0x44		SEQ_ADC3TIA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_adc3tia	0	RW	ADC third sampling time for TIA: same as seq_adc2tia. Also must make sure to not overlap ADC conversions! Also, adc3tia must be after adc2tia

SD_SUBS (Address 0x45)

Figure 63:
SD_SUBS Register

Addr: 0x45		SD_SUBS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	sd_subs	0	RW	Synchronous demodulator subsampling ratio between sequencer frequency and ADC sampling frequency. ADC-Fsample = Sequencyer_Frequency/(sd_subs+1) When setting to 0, then in every sequencer iteration the ADC will run. When setting to 1, then the first sequencer iteration will not trigger the ADC, but the second one will. Setting to N will make N iterations without ADC, followed by one iteration with the ADC measurement executed. It is recommended to use the ADC interrupt in this case and not the sequencer interrupt. Also see sd_subs_always which significantly affects this mechanism.

SEQ_CFG (Address 0x46)

Figure 64:
SEQ_CFG Register

Addr: 0x46		SEQ_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Not used	0	RW	Not used
0	sd_subs_always	0	RW	If this bit is asserted, all sequencer periods are subject to subsampling as defined in SD_SUBS. If this bit is zero, then only the first period of an "ADC cycle" is duplicated sd_subs times, all other periods are regular. One "ADC cycle" is the time from the sequence in which adc_sel is pointing to the "smallest" adc channel up and including the sequence of the "largest" adc channel.

SEQ_ERR (Address 0x47)

Figure 65:
SEQ_ERR Register

Addr: 0x47		SEQ_ERR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	irq_adc_timing_error	0	SS_WC	The ADC is started by the sequencer (or manually) while it was still converting. This does not flag an interrupt but when playing with the sequencer settings we suggest to check this flag to make sure that there is no problem with the sequencer programming
6:0	Not used	0	RW	Not used

CYC_COUNTER (Address 0x60)

Figure 66:
CYC_COUNTER Register

Addr: 0x60		CYC_COUNTER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	cycle_counter	0	RO	Current cycle counter value

The SEQ_COUNTER register shows the current value of the sequence counter and period counter.

SEQ_COUNTER (Address 0x61)

Figure 67:
SEQ_COUNTER Register

Addr: 0x61		SEQ_COUNTER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	sequence_counter	0	RO	Current sequence counter value

SUBS_COUNTER (Address 0x62)

Figure 68:
SUBS_COUNTER Register

Addr: 0x62		SUBS_COUNTER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	subs_counter	0	RO	Current subsampling counter value

OVERSAMPLING/AVERAGE

Noise improvement.

Generate the programmable average of multiple sample for two input channels (e.g., PPG and ECG). The mean value is programmed as a $2^{\wedge n}$ function.

SEQ_OVS_SEL (Address 0x48)

Figure 69:
SEQ_OVS_SEL Register

Addr: 0x48		SEQ_OVS_SEL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ovs_sel2	0	RW	Selecting the ADC channel for oversampling 2
3:0	ovs_sel1	0	RW	Selecting the ADC channel for oversampling 1

SEQ_OVS_VAL (Address 0x49)

Figure 70:
SEQ_OVS_VAL Register

Addr: 0x49		SEQ_OVS_VAL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Not used	0	RW	Not used
6:4	ovs_val2	0	RW	Set value for oversampling 2, 2^ovs_val2
3	Not used	0	RW	Not used
2:0	ovs_val1	0	RW	Set value for oversampling 1, 2^ovs_val1

SEQ_DIS_SEL (Address 0x4a)

Figure 71:
SEQ_DIS_SEL Register

Addr: 0x4a		SEQ_DIS_SEL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	dis_sel2	0	RW	Select ADC for disable channel 2
3:0	dis_sel1	0	RW	Select ADC for disable channel 1

SEQ_DIS_VAL1 (Address 0x4b)

Figure 72:
SEQ_DIS_VAL1 Register

Addr: 0x4b		SEQ_DIS_VAL1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_dis_val1	0	RW	Set value n for disable channel 1 $f_{DISABLE} = f_{CYCLE}$ / (seq_dis_val1 + 1)

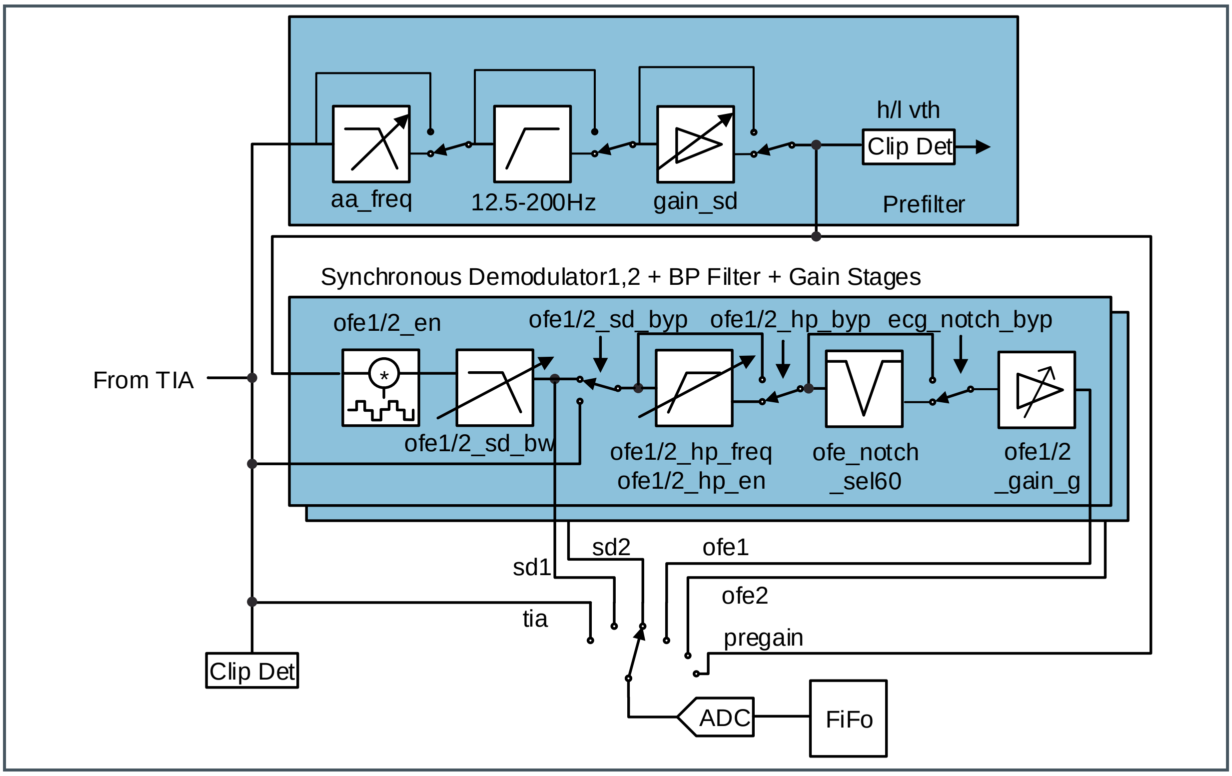
SEQ_DIS_VAL2 (Address 0x4c)

Figure 73:
SEQ_DIS_VAL2 Register

Addr: 0x4c		SEQ_DIS_VAL2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_dis_val2	0	RW	Set value n for disable channel 2 $f_{DISABLE} = f_{CYCLE}$ / (seq_dis_val2 + 1)

7.1.12 Optical Signal Conditioning

Figure 74:
Optical Signal Conditioning



Synchronous Demodulator

Two optional synchronous demodulators can be used to detect small optical signals in the presence of large unwanted noise (ambient light). Since the detector synchronizes to the LED frequency, the demodulator can only be used if the measurement sequencer is running.

It includes an input filer (adjustable high pass and low pass, notch filter) and 2nd order adjustable output low pass. The demodulator itself multiplies the signal by +1 / 0 / -1 with a timing which is controlled by the sequencer.

Information

The optical signal conditioning stage need sigref_en=1 for operation.

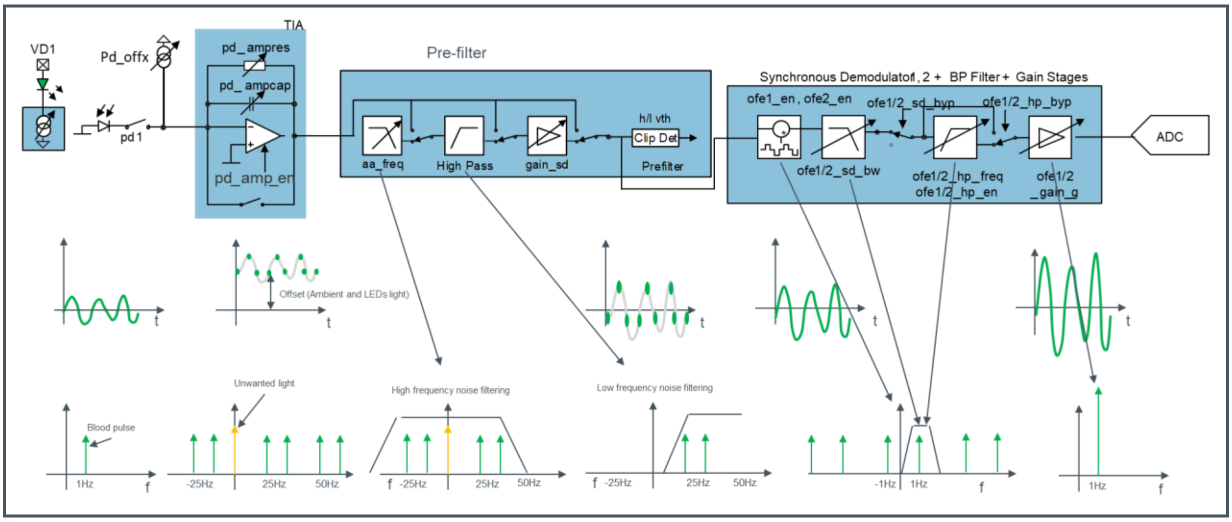
High Pass Filter

Two optional high pass filters can be used to remove unwanted DC-components from the signal and allows further amplification. In order to guarantee fast settling times of the filter, four cutoff frequencies can be chosen.

Gain Stage

Two optional gain stage can be used to amplify the signal after the DC-component has been removed.

Figure 75:
Optical Signal Conditioning Signal Path (25 Hz LED sampling rate example)



The LED that is periodically turned ON and OFF, samples the cardio-vascular pulse wave. The photodiode measures the reflected light that is modulated by the LED sampling frequency (25 Hz in the examples Figure 75). Unwanted light like red/IR ambient light or glass reflected LED light is not modulated. The signal can be sent to the Pre-filter Block where an anti-aliasing filter removes the high frequency noise, followed by a high pass filter that removes the low frequency noise and unwanted dc light. After the synchronous demodulator demodulates the signal it is filtered and amplified.

7.1.13 Optical Signal Conditioning Registers

OFE_CFGA (Address 0x50)

Figure 76:
OFE_CFGA Register

Addr: 0x50		OFE_CFGA			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	ofe2_en	0	RW	Enable OFE2	
6	ofe1_en	0	RW	Enable OFE1	
5	en_bias_ofe	0	RW	Enable bias for OFE and TIA	
4:3	aa_freq	0	RW	Anti-aliasing filter cut-off frequency	
				Settings	**Signal**
				0	10kHz
				1	20kHz
				2	40kHz
				3	60kHz
2:0	gain_sd	0	RW	SD gain	
				Settings	**Normal Gain**
				0	1
				1	2
				2	4
				3	8
				4	16
				5	32
				6	64
				7	Reserved

OFE1_SD_THCFG (Address 0x51)

Figure 77:
OFE1_SD_THCFG Register

Addr: 0x51		OFE1_SD_THCFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ofe1_sd_clipd_h_thresh	0	RW	If the voltage on the output of the gain_sd stage of OFE1 (input of synchronous demodulator) exceed this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as: 0: 1824 mV 1: 1748 mV 2: 1672 mV 3: 1596 mV 4: 1520 mV 5: 1444 mV 6: 1368 mV 7: 1292 mV 8: 1216 mV 9: 1140 mV 10: 1064 mV 11: 988 mV 12: 912 mV 13: 836 mV 14: 760 mV 15: 684 mV
3:0	ofe1_sd_clipd_l_thresh	0	RW	If the voltage on the output of the gain_sd stage OFE 1 (input of synchronous demodulator) falls below this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as: 0: 67 mV 1: 143 mV 2: 219 mV 3: 295 mV 4: 371 mV 5: 447 mV 6: 523 mV 7: 599 mV 8: 675 mV 9: 751 mV 10: 827 mV

Addr: 0x51		OFE1_SD_THCFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				11: 903 mV 12: 979 mV 13: 1055 mV 14: 1131 mV 15: 1207 mV

OFE_CFGC (Address 0x52)

Figure 78:
OFE_CFGC Register

Addr: 0x52		OFE_CFGC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Not used	0	RW	Not used
6	prefilter_aa_byp	0	RW	0: Anti-aliasing filter (aa_filter) is used 1: Bypass anti-aliasing filter
5	prefilter_hp_byp	0	RW	0: Use high pass filter 1: Bypass high pass filter
4	prefilter_gain_byp	0	RW	0: Use gain_sd stage 1: Bypass gain_sd stage
3	prefilter_bypass_en	0	RW	0: Use prefilter unless any of the above register is set 1: Bypass complete prefilter
2	prefilter_aa_en	0	RW	0: Anti aliasing filter (aa_filter) is OFF 1: Anti aliasing filter is ON
1	prefilter_hp_en	0	RW	0: High pass filter is OFF 1: High pass filter is ON
0	prefilter_gain_en	0	RW	0: gain_sd stage is OFF 1: gain_sd stage is ON

OFE_CFGD (Address 0x53)

Figure 79:
OFE_CFGD Register

<table>
<tr><th>Addr: 0x53</th><th></th><th colspan="6">OFE_CFGD</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="4">Bit Description</th></tr>
<tr><td>7</td><td>Not used</td><td>0</td><td>RW</td><td colspan="4">Not used</td></tr>
<tr><td rowspan="6">6:5</td><td rowspan="6">notch_bw</td><td rowspan="6">3</td><td rowspan="6">RW</td><td colspan="4">Bandwidth of notch filter.</td></tr>
<tr><td colspan="2">Settings</td><td colspan="2">Value</td></tr>
<tr><td colspan="2">0</td><td colspan="2">Max BW</td></tr>
<tr><td colspan="2">1</td><td colspan="2"></td></tr>
<tr><td colspan="2">2</td><td colspan="2"></td></tr>
<tr><td colspan="2">3</td><td colspan="2">Min BW (default)</td></tr>
<tr><td rowspan="7">4:2</td><td rowspan="7">ofe_sd_hp</td><td rowspan="7">0</td><td rowspan="7">RW</td><td colspan="4">High pass filter pulse rate for both synchronous demodulators. Pulse width = 1 µs</td></tr>
<tr><td>Settings</td><td colspan="2">Pulse Frequency</td><td>Cutoff Frequency</td></tr>
<tr><td>0</td><td colspan="2">125 kHz</td><td>200 Hz</td></tr>
<tr><td>1</td><td colspan="2">62.5 kHz</td><td>100 Hz</td></tr>
<tr><td>2</td><td colspan="2">31.25 kHz</td><td>50 Hz</td></tr>
<tr><td>3</td><td colspan="2">15.625 kHz</td><td>25 Hz</td></tr>
<tr><td>4</td><td colspan="2">7.8125 kHz</td><td>12.5 Hz</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">ofe_gs_aa</td><td rowspan="6">0</td><td rowspan="6">RW</td><td colspan="4">OFE anti aliasing</td></tr>
<tr><td colspan="2">Setting</td><td colspan="2">Nominal Gain</td></tr>
<tr><td colspan="2">0</td><td colspan="2">Bypass</td></tr>
<tr><td colspan="2">1</td><td colspan="2">fc=100 kHz</td></tr>
<tr><td colspan="2">2</td><td colspan="2">fc=10 kHz</td></tr>
<tr><td colspan="2">3</td><td colspan="2">fc=826 Hz</td></tr>
</table>

OFE1_CFGA (Address 0x54)

Figure 80:
OFE1_CFGA Register

Addr: 0x54		OFE1_CFGA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ofe1_sd_pol_init	0	RW	The low level driver shall ensure that this register is 0 if one of the seq_sdm pulses is first, and is 1 if the seq_sdp is first within a sequence.
6	ofe1_sd_en	0	RW	0: Power down of the Synchronous demodulator 1: Enable Synchronous demodulator
5	ofe1_hp_en	0	RW	0: Power down of the high pass filter 1: Enable high pass filter
4	ofe1_gain_en	0	RW	0: Power down of the Gain stage 1: Enable Gain stage
3	ofe1_sd_byp	0	RW	0: Synchronous demodulator is used 1: Synchronous demodulator is bypassed
2	ofe1_hp_byp	0	RW	0: HP filter is used 1: HP filter is bypassed
1	ofe1_gain_byp	0	RW	0: Gain stage is used 1: Gain stage is bypassed
0	ofe1_sd_hld	0	RW	SD hold 0: Output of synchronous demodulator is forced to SIGREF if not set to +1 or -1 1: Output of synchronous demodulator is tristated if not set to +1 or -1

OFE1_CFGB (Address 0x55)

Figure 81:
OFE1_CFGB Register

Addr: 0x55		OFE1_CFGB			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	ofe1_gain_g	0	RW	Gain for synchronous demodulator 1.	
				Settings	**Gain**
				0	1
				1	2
				2	4
				3	8

Addr: 0x55		OFE1_CFGB				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
				4	16	
				5	32	
				6	64	
				7	128	
4:2	ofe1_sd_bw	0	RW	Low pass clock for synchronous demodulator 1 and cutoff frequency		
				Settings	**Clock Frequency**	**Cutoff Frequency**
				0	31.25 kHz	10 Hz
				1	62.5 kHz	20 Hz
				2	125 kHz	40 Hz
				3	250 kHz	80 Hz
				4	15.625 kHz	5 Hz
				5	7.8125 kHz	2.5 Hz
1:0	of1e_hp_freq	0	RW	High pass filter pulse rate for synchronous demodulator 1. Pulse width = 1 µs		
				Settings	**Pulse Frequency**	**Cutoff Frequency**
				0	122 Hz	0.33 Hz
				1	488 Hz	1.32 Hz
				2	1935 Hz	5.28 Hz
				3	3906 Hz	10.56 Hz

OFE2_SD_THCFG (Address 0x57)

Figure 82:
OFE2_SD_THCFG Register

Addr: 0x57		OFE2_SD_THCFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ofe2_sd_clipd_h_thresh	0	RW	If the voltage on the output of the gain_sd stage of OFE2 (input of synchronous demodulator) exceed this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as: 0: 1824 mV 1: 1748 mV

Addr: 0x57		OFE2_SD_THCFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				2: 1672 mV 3: 1596 mV 4: 1520 mV 5: 1444 mV 6: 1368 mV 7: 1292 mV 8: 1216 mV 9: 1140 mV 10: 1064 mV 11: 988 mV 12: 912 mV 13: 836 mV 14: 760 mV 15: 684 mV
3:0	ofe2_sd_clipd_l_thresh	0	RW	If the voltage on the output of the gain_sd stage OFE 2 (input of synchronous demodulator) falls below this threshold the irq_clipdetect interrupt is asserted. The threshold is defined as: 0: 67 mV 1: 143 mV 2: 219 mV 3: 295 mV 4: 371 mV 5: 447 mV 6: 523 mV 7: 599 mV 8: 675 mV 9: 751 mV 10: 827 mV 11: 903 mV 12: 979 mV 13: 1055 mV 14: 1131 mV 15: 1207 mV

OFE2_CFGA (Address 0x58)

Figure 83:
OFE2_CFGA Register

Addr: 0x58		OFE2_CFGA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ofe2_sd_pol_init	0	RW	The low level driver shall ensure that this register is 0 if one of the seq_sdm pulses is first, and is 1 if the seq_sdp is first within a sequence.
6	ofe2_sd_en	0	RW	0: Power down of the Synchronous demodulator 1: Enable Synchronous demodulator
5	ofe2_hp_en	0	RW	0: Power down of the high pass filter 1: Enable high pass filter
4	ofe2_gain_en	0	RW	0: Power down of the Gain stage 1: Enable Gain stage
3	ofe2_sd_byp	0	RW	0: Synchronous demodulator is used 1: Synchronous demodulator is bypassed
2	ofe2_hp_byp	0	RW	0: HP filter is used 1: HP filter is bypassed
1	ofe2_gain_byp	0	RW	0: Gain stage is used 1: Gain stage is bypassed
0	ofe2_sd_hld	0	RW	SD hold 0: Output of synchronous demodulator is forced to SIGREF if not set to +1 or -1 1: Output of synchronous demodulator is tristated if not set to +1 or -1

OFE2_CFGB (Address 0x59)

Figure 84:
OFE2_CFGB Register

<table>
<tr><th colspan="2">Addr: 0x59</th><th colspan="4">OFE2_CFGB</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">7:5</td><td rowspan="6">ofe2_gain_g</td><td rowspan="6">0</td><td rowspan="6">RW</td><td colspan="2">Gain for synchronous demodulator 2.</td></tr>
<tr><td>Settings</td><td>Gain</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>2</td><td>4</td></tr>
<tr><td>3</td><td>8</td></tr>
</table>

Addr: 0x59		OFE2_CFGB				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
				4	16	
				5	32	
				6	64	
				7	128	
4:2	ofe2_sd_bw	0	RW	Low pass clock for synchronous demodulator 2 and cutoff frequency		
				Settings	**Clock Frequency**	**Cutoff Frequency**
				0	31.25 kHz	10 Hz
				1	62.5 kHz	20 Hz
				2	125 kHz	40 Hz
				3	250 kHz	80 Hz
				4	15.625 kHz	5 Hz
				5	7.8125 kHz	2.5 Hz
1:0	of2e_hp_freq	0	RW	High pass filter pulse rate for synchronous demodulator 2. Pulse width = 1 µs		
				Settings	**Pulse Frequency**	**Cutoff Frequency**
				0	122 Hz	0.33 Hz
				1	488 Hz	1.32 Hz
				2	1935 Hz	5.28 Hz
				3	3906 Hz	10.56 Hz

OFE_NOTCH (Address 0x5a)

Figure 85:
OFE_NOTCH Register

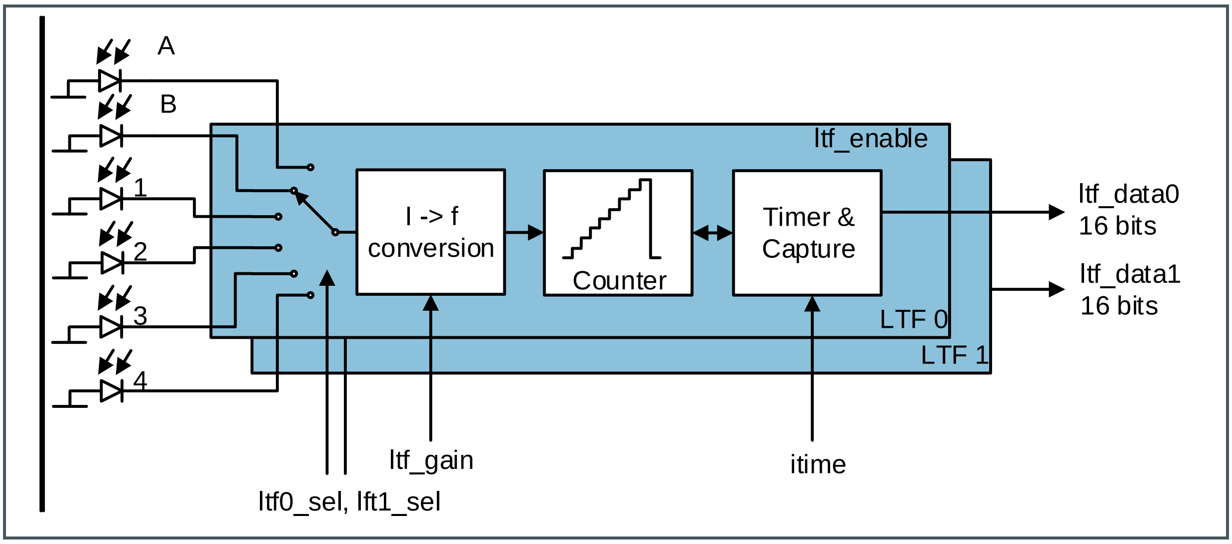
Addr: 0x5a		OFE_NOTCH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Not used	0	RW	Not used
6	ofe2_notch_sel60	0	RW	0: Fc=50 Hz 1: Fc=60 Hz
5	ofe2_notch_byp	1	RW	0: OFE2 Notch filter Not bypassed 1: OFE2 Notch bypassed

Addr: 0x5a		OFE_NOTCH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	ofe2_notch_en	0	RW	0: Power down of the OFE2 high pass filter 1: Enable OFE2 Notch filter
3	Not used	0	RW	Not used
2	ofe1_notch_sel60	0	RW	0: Fc= 50 Hz 1: Fc= 60 Hz
1	ofe1_notch_byp	1	RW	0: OFE1 Notch filter Not bypassed 1: OFE1 Notch bypassed
0	ofe1_notch_en	0	RW	0: Power down of the OFE1 high pass filter 1: Enable OFE1 Notch filter

7.1.14 Light-to-Frequency Mode

The LTF (light-to-frequency, or FM, frequency mode) mode.

Figure 86:
Light-to-Frequency Mode Internal Circuit



(1) Do not use diodes which are connected to the TIA (register pd_a, pd_b, pd1...4) at the same time when ltf_en is enabled on the same diode.

LTFDATA0_L (Address 0x20)

Figure 87:
LTFDATA0_L Register

Addr: 0x20		LTFDATA0_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ltfdata0[7:0]	0	RO	LTF result channel 0 low byte. Software must make sure that the LTF integration is not running when accessing the LTFDATA registers. These are the direct counter registers, they are not latched. If buffering is required, consider using FIFO mode.

LTFDATA0_H (Address 0x21)

Figure 88:
LTFDATA0_H Register

Addr: 0x21		LTFDATA0_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ltfdata0[15:8]	0	RO	LTF result channel 0 high byte

LTFDATA1_L (Address 0x22)

Figure 89:
LTFDATA1_L Register

Addr: 0x22		LTFDATA1_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ltfdata0[7:0]	0	RO	LTF result channel 1 low byte. Software must make sure that the LTF integration is not running when accessing the LTFDATA registers. If buffering is required, consider using FIFO mode.

LTFDATA1_H (Address 0x23)

Figure 90:
LTFDATA1_H Register

Addr: 0x23		LTFDATA1_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ltfdata1[15:8]	0	RO	LTF result channel 1 high byte

ITIME (Address 0x24)

Figure 91:
ITIME Register

Addr: 0x24		ITIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Itime	0	RW	LTF integration time. MODCLK is 2/3 MHz (666.67 kHz). One LSB of itime is 3.072 ms (2048 MODCLK cycles). 0: 3.072 ms ... 255: 786.432 ms Using the itime_unit register (see below), the unit of itime can be reduced by 2, 4, or 8. This shorter integration times can be selected (required for flicker detection), but it can also be used to increase the resolution of itime. For example, if 50 ms integration time are desired, the best value for regular itime would be 15 (=16 periods=49.152 ms). However, but setting itime_unit=2 (LSB=768 µs), one can select 64 (=65 periods=49.9 ms) Warning: selecting an integration time smaller than 3.072 ms will reduce the resolution of the conversion, as the maximum ltfdata value is not 1024 (10 bits) anymore, but 512 (9 bits) in case of 1.536 ms integration time, 256 (8 bits) for 768 µs and 128 (7 bits) for 384 µs

LTF_CONFIG (Address 0x25)

Figure 92:
LTF_CONFIG Register

Addr: 0x25		LTF_CONFIG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	infinite_itime	0	RW	If this is asserted, then integration does not stop. The ITIME setting is ignored. Use with watch the ltfdata counters. (Warning: must be filtered in software to prevent inconsistent upper/lower byte). It is implemented as a count disable on the integration counter, so when resetting bit to 0 again, the itime counter will continue and results can be read afterwards through the regular mechanisms (ltfdata or FIFO) This is intended for very long integration times - as the timing is controlled by software/I²C, accuracy fully depends on the system and I²C master.
6	az_disable_auto	0	RW	0: Run autozero on both channels every time FM mode is activated for the first time after ENAB is being asserted. 1: Do not run autozero automatically. Autozero can only be activated manually (AZ_CONTROL)
5:4	az_mode	0	RW	Autozero mechanism: It is a simple and robust follower circuit that requires as many cycles as offsetvalue minus startvalue. Mode 0 is the safe default mode, mode 1 is used in production test to be sure that the DAC can generate all values. Mode 2 can be used if AZ time is an issue, if one is certain that the AZvalue has not changed much: typically if full AZ has been run, one can assume that offset only changes a little bit from temperature. **Settings** – **Mode** 0 – Always start at zero when searching the best offset value,128+16 cycles 1 – Always start at the previous offset with the auto-zero mechanism, 256+16 cycles 2 – Always start at the previous offset with the auto-zero mechanism, 16+16 cycles 3 – Not used
3	Not used	0	RW	Not used
2	ltf_prox_mode	0	RW	LTF proximity mode

Addr: 0x25		LTF_CONFIG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	ltf_fifo_mode	0	RW	Run LTF integrations back to back, the LTF modulator is running continuously (the modulators are not reset between integrations cycles). After each integration, the result gets written to the FIFO. The FIFO is being filled automatically, FIFO threshold interrupt is flagged as configured. The first item read from the FIFO is from channel 0, the next one from channel 1, etc. Note that there is no ltf_done interrupt triggered after each integration. A FIFO threshold of 1 can be used to generate an interrupt for each result. irq_ltf_enab should be kept asserted to avoid missing an ltf_sat interrupt. Do not enable ADC/sequencer FIFO mode and ltf_fifo_mode at the same time, corrupted data would be the result. Make sure to empty the FIFO in time, if the FIFO is full, new data is not being stored in the FIFO. Source of data read from the FIFO after an overflow condition is undefined (can be from channel 0 or channel 1) Stop the procedure by clearing this bit.
0	ltf_enable	0	RW	This bit must be asserted for any LTF function (powers up the LTF clock tree)

LTF_SEL (Address 0x26)

Figure 93:
LTF_SEL Register

Addr: 0x26		LTF_SEL			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	Do not use	0	RW	Do not use	
6:4	ltf1_sel	2	RW	Select the sensor diode for LTF1	
				Setting	**Source**
				0	Clear
				1	Not used
				2	IR
				3	Not used

Addr: 0x26		LTF_SEL			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				4	PD1
				5	PD2
				6	PD3
				7	PD4
3	Not used	0	RW	Not used	
2:0	ltf0_sel	0	RW	Select the sensor diode for LTF0	
				Setting	**Source**
				0	Clear
				1	Not used
				2	IR
				3	Not used
				4	PD1
				5	PD2
				6	PD3
				7	PD4

LTF_GAIN (Address 0x27)

Figure 94:
LTF_GAIN Register

<table>
<tr><th>Addr: 0x27</th><th></th><th colspan="4">LTF_GAIN</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td>7:6</td><td>Do not use</td><td>0</td><td>RW</td><td colspan="2">Do not use</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">itime_unit</td><td rowspan="6">0</td><td rowspan="6">RW</td><td colspan="2">Select the itime unit.
See ITIME register description (Figure 91).</td></tr>
<tr><td>Setting</td><td>Behavior</td></tr>
<tr><td>0</td><td>Normal, time LSB=3.072 ms</td></tr>
<tr><td>1</td><td>/2, LSB=1.536 ms</td></tr>
<tr><td>2</td><td>/4, time LSB=768 µs</td></tr>
<tr><td>3</td><td>/8, time LSB=384 µs</td></tr>
<tr><td rowspan="12">3:0</td><td rowspan="12">ltf_gain</td><td rowspan="12">0</td><td rowspan="12">RW</td><td colspan="2">Select the gain</td></tr>
<tr><td>Setting</td><td>Gain</td></tr>
<tr><td>0</td><td>0.25</td></tr>
<tr><td>1</td><td>0.5</td></tr>
<tr><td>2</td><td>1</td></tr>
<tr><td>3</td><td>2</td></tr>
<tr><td>4</td><td>4</td></tr>
<tr><td>5</td><td>8</td></tr>
<tr><td>6</td><td>16</td></tr>
<tr><td>7</td><td>24</td></tr>
<tr><td>8</td><td>64</td></tr>
<tr><td>9-15</td><td>Reserved – do not use</td></tr>
</table>

LTF_CONTROL (Address 0x28)

Figure 95:
LTF_CONTROL Register

Addr: 0x28		LTF_CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Do not use	0	R_PUSH	Do not use

Addr: 0x28		LTF_CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	ltf_start	0	R_PUSH	Writing 1 starts the counter, and it will run for the specified time (itime). Afterwards it stops automatically and interrupt is flagged. writing 0 to the counter stops it as well. reading the value returns whether the counter is running. If ltf_fifo_mode is non-zero, then FM conversions are done continuously until a 0 is written to this bit again.

AZ_CONTROL (Address 0x29)

Figure 96:
AZ_CONTROL Register

Addr: 0x29		AZ_CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	Do not use	0	RW_SM	Do not use
1	az_enable_1	0	RW_SM	Writing a '1' to this register starts the AZ engine for channel 1. This is usually not necessary, as AZ is executed automatically before the first LTF integration (unless az_disable_auto is set) The bit is cleared to '0' automatically when the AZ has finished. You cannot write a '0' to this register.
0	az_enable_0	0	RW_SM	The same as az_enable_1, but for channel 0.

OFFSET0 (Address 0x2a)

Figure 97:
OFFSET0 Register

Addr: 0x2a		OFFSET0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	offset0[7:0]	0	RW_SM	This register holds the value of the offset on the channel 0 OpAmp. It can be overwritten, and it gets overwritten by the auto-zero mechanism. The value is in sign/magnitude encoding. The value is ±127, sign/magnitude

OFFSET1 (Address 0x2b)

Figure 98:
OFFSET1 Register

Addr: 0x2b		OFFSET1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	offset0[7:0]	0	RW_SM	This register holds the value of the offset on the channel 1 OpAmp. It can be overwritten, and it gets overwritten by the auto-zero mechanism. The value is in sign/magnitude encoding. The value is ±127, sign/magnitude

LTF_THRESHOLD_LOW0 (Address 0x6c)

Figure 99:
LTF_THRESHOLD_LOW0 Register

Addr: 0x6c		LTF_THRESHOLD_LOW0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ltf_threshold_low[7:0]	00	RW	If LTF returns a value above ltf_threshold_low (not equal), then the ltf_threshold_low interrupt can be triggered

LTF_THRESHOLD_LOW1 (Address 0x6d)

Figure 100:
LTF_THRESHOLD_LOW1 Register

Addr: 0x6d		LTF_THRESHOLD_LOW1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ltf_threshold_low[15:8]	00	RW	If LTF returns a value above ltf_threshold_low (not equal), then the ltf_threshold_low interrupt can be triggered

LTF_THRESHOLD_HIGH0 (Address 0x6e)

Figure 101:
LTF_THRESHOLD_HIGH0 Register

Addr: 0x6e		LTF_THRESHOLD_HIGH0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ltf_threshold_high[7:0]	FF	RW	If LTF returns a value below ltf_threshold_high (not equal), then the ltf_threshold_high interrupt can be triggered.

LTF_THRESHOLD_HIGH1 (Address 0x6f)

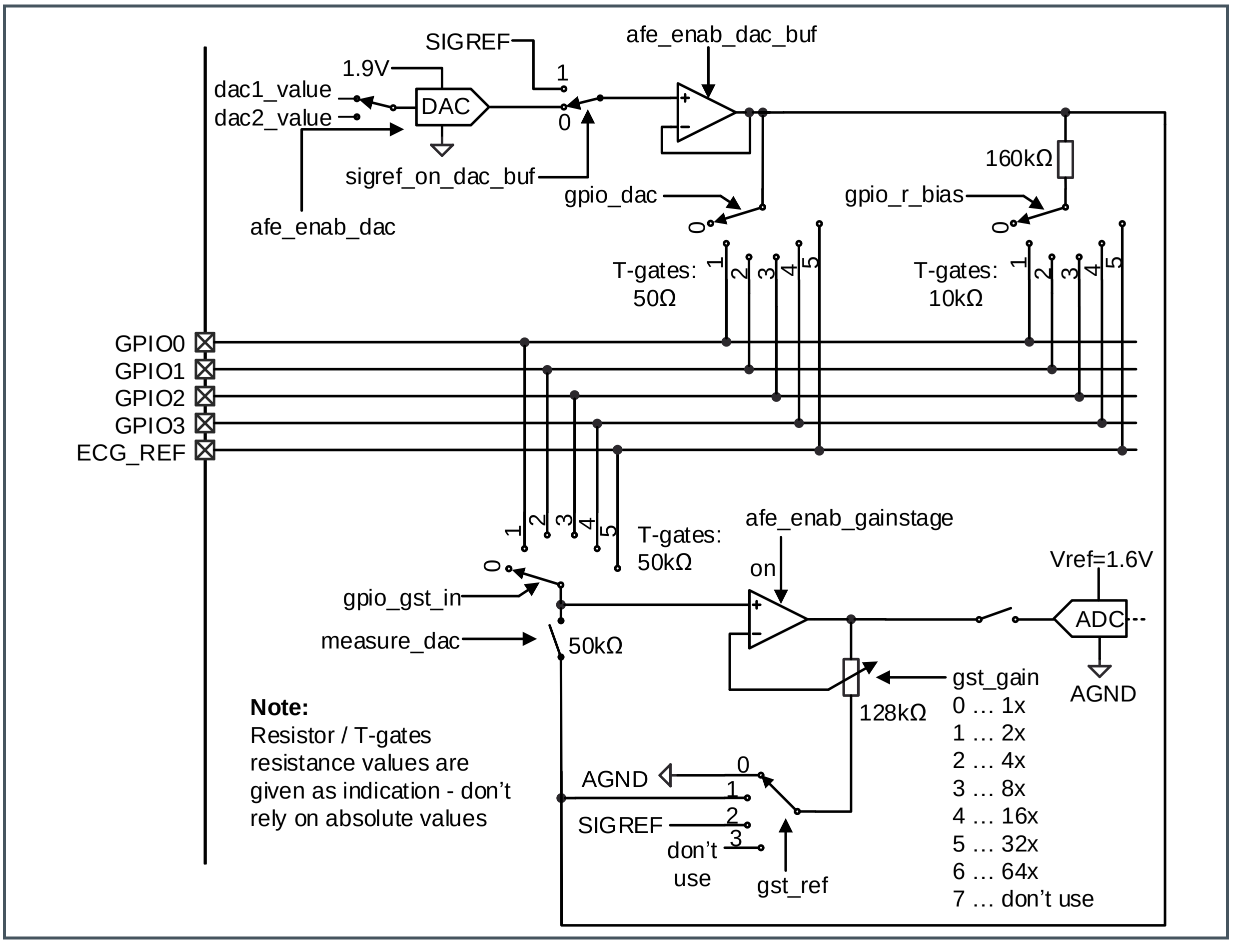
Figure 102:
LTF_THRESHOLD_HIGH1 Register

Addr: 0x6f		LTF_THRESHOLD_HIGH1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ltf_threshold_high[15:8]	FF	RW	If LTF returns a value below ltf_threshold_high (not equal), then the ltf_threshold_high interrupt can be triggered.

7.1.15 Electrical Analog Front End

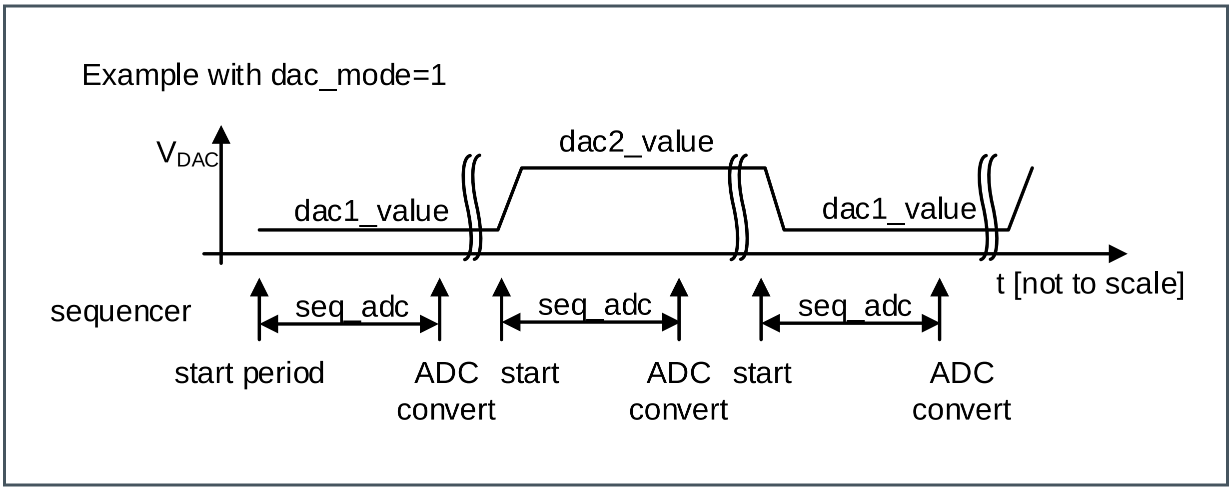
The electrical analog front end consists of three identical signal paths with independent settings of bias condition, gain and offset. Four general purpose pins and ECG_REF can be used either as configurable GPIO pin or as analog input pins for the electrical analog front end. The analog inputs can be configured to setup different amplifier topologies.

Figure 103:
Electrical Analog Front End



DAC Switching

Figure 104:
Electrical Analog Front End DAC Level Switching



If bit dac_mode is not zero, the DAC switches its codes between dac1_value and dac2_value on the beginning of every/every 2nd/every 4th sequencer cycle where the ADC is converting the electrical frontend channel. ADC conversions of any other channel do not switch the DAC.

Input Pins

Four general purpose pins and ECG_REF can be used either as configurable GPIO pin or as analog input pins for the electrical analog front end. The analog inputs can be configured to setup different amplifier topologies.

7.1.16 EAF (Electrical Analog Frontend) Registers

EAF_CFG (Address 0x70)

Figure 105:
EAF_CFG Register

Addr: 0x70		EAF_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Do not use	0	RW	Do not use
3	eaf_enab	0	RW	0: EAF bias deactivated 1: EAF bias activated (need to be set for any functions of the EAF are used).

Addr: 0x70		EAF_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	eaf_enab_dac	0	RW	0: DAC inside the EAF OFF 1: DAC inside the EAF ON
1	eaf_enab_dac_buf	0	RW	0: DAC buffer OFF 1: DAC buffer ON
0	eaf_enab_gainstage	0	RW	0: Gain stage in EAF OFF 1: Gain stage in EAF ON

The EAF_CFG register is used to configure the analog frontend.

EAF_GST (Address 0x80)

Figure 106:
EAF_GST Register

<table>
<tr><th colspan="2">Addr: 0x80</th><th colspan="4">EAF_GST</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="8">7:5</td><td rowspan="8">gpio_gst_in</td><td rowspan="8">0</td><td rowspan="8">RW</td><td colspan="2">Gain stage input selection</td></tr>
<tr><td>Setting</td><td>Meaning</td></tr>
<tr><td>0</td><td>Not connected</td></tr>
<tr><td>1</td><td>GPIO0</td></tr>
<tr><td>2</td><td>GPIO1</td></tr>
<tr><td>3</td><td>GPIO2</td></tr>
<tr><td>4</td><td>GPIO3</td></tr>
<tr><td>5</td><td>ECG_REF</td></tr>
<tr><td rowspan="6">4:3</td><td rowspan="6">gst_ref</td><td rowspan="6">0</td><td rowspan="6">RW</td><td colspan="2">Gain stage reference voltage</td></tr>
<tr><td>Setting</td><td>Meaning</td></tr>
<tr><td>0</td><td>AGND</td></tr>
<tr><td>1</td><td>DAC buffer</td></tr>
<tr><td>2</td><td>SIGREF</td></tr>
<tr><td>3</td><td>Reserved</td></tr>
<tr><td rowspan="4">2:0</td><td rowspan="4">gst_gain</td><td rowspan="4">0</td><td rowspan="4">RW</td><td colspan="2">Gain stage gain</td></tr>
<tr><td>Setting</td><td>Meaning</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>2</td></tr>
</table>

Addr: 0x80		EAF_GST			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				2	4
				3	8
				4	16
				5	32
				6	64
				7	Reserved

The EAF register is used to configure the electrical frontend

EAF_BIAS (Address 0x81)

Figure 107:
EAF_BIAS Register

Addr: 0x81		EAF_BIAS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	gpio_r_bias	0	RW	Resistive biasing	
				Setting	**Meaning**
				0	No resistive biasing
				1	Resistive biasing on GPIO0
				2	Resistive biasing on GPIO1
				3	Resistive biasing on GPIO2
				4	Resistive biasing on GPIO3
				5	Resistive biasing on ECG_REF
4:0	Not used	0	RW	Do not use	

EAF_DAC (Address 0x82)

Figure 108:
EAF_DAC Register

Addr: 0x82		EAF_DAC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Do not use	0	RW	Do not use

Addr: 0x82		EAF_DAC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	sigref_on_dac_buf	0	RW	If asserted, connect SIGREF to DAC buffer.
3	measure_dac	0	RW	If this bit is asserted, the DAC output is connected to the gain stage input (independent of gpio_gst_in selection, therefore the DAC output is measurable on the GPIO pin)
2:0	gpio_dac	0	RW	DAC on GPIO **Setting** – **Meaning** 0 – No DAC biasing 1 – DAC on GPIO0 2 – DAC on GPIO1 3 – DAC on GPIO2 4 – DAC on GPIO3 5 – DAC on ECG_REF

EAF_DAC1_L (Address 0x83)

Figure 109:
EAF_DAC1_L Register

Addr: 0x83		EAF_DAC1_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	dac1_value[1:0]	0	RW	DAC value 1 (2LSB)
5:0	Not used	0	RW	Not used

The EAF_DAC1/2_L/H registers is used to configure the dac value. See bit dac_mode for selection of dac register 1 or 2

EAF_DAC1_H (Address 0x84)

Figure 110:
EAF_DAC1_H Register

Addr: 0x84		EAF_DAC1_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	dac1_value[9:2]	0	RW	DAC value 1 (upper 8 bits)

Addr: 0x84		EAF_DAC1_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				10-bit value: 0x000: 0 V 0x3FF: 1.9 V

EAF_DAC2_L (Address 0x85)

Figure 111:
EAF_DAC2_L Register

Addr: 0x85		EAF_DAC2_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	dac2_value[1:0]	0	RW	DAC value 2 (2LSB)
5:0	Not used	0	RW	Not used

EAF_DAC2_H (Address 0x86)

Figure 112:
EAF_DAC2_H Register

Addr: 0x86		EAF_DAC2_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	dac2_value[9:2]	0	RW	DAC value 1 (upper 8 bits) 10-bit value: 0x000: 0 V 0x3FF: 1.9 V

EAF_DAC_CFG (Address 0x87)

Figure 113:
EAF_DAC_CFG Register

Addr: 0x87		EAF_DAC_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	Not used	0	RW	Not used

Addr: 0x87		EAF_DAC_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1:0	dac_mode	0	RW	DAC mode The EAF has a DAC that can be switched out on GPIOs. dac_mode 0 uses statically dac1_value, the other modes switch dynamically between the two values. The system switches from one value to the next always at the beginning of a sequence in which the ADC will sample the AFE channel. **Setting** – **Meaning** 0 – 1-1-1-1-1-1-1-1-1-1- 1 – 1-2-1-2-1-2-1-2-1-2-1- 2 – 1-1-2-2-1-1-2-2-1-1-2- 3 – 1-1-1-1-2-2-2-2-1-1-1-

Possible Configurations of Every Amplifier Stage

Figure 114:
Non Inverting Amplifier with Offset and Input Voltage Divider (Temperature Sensor)

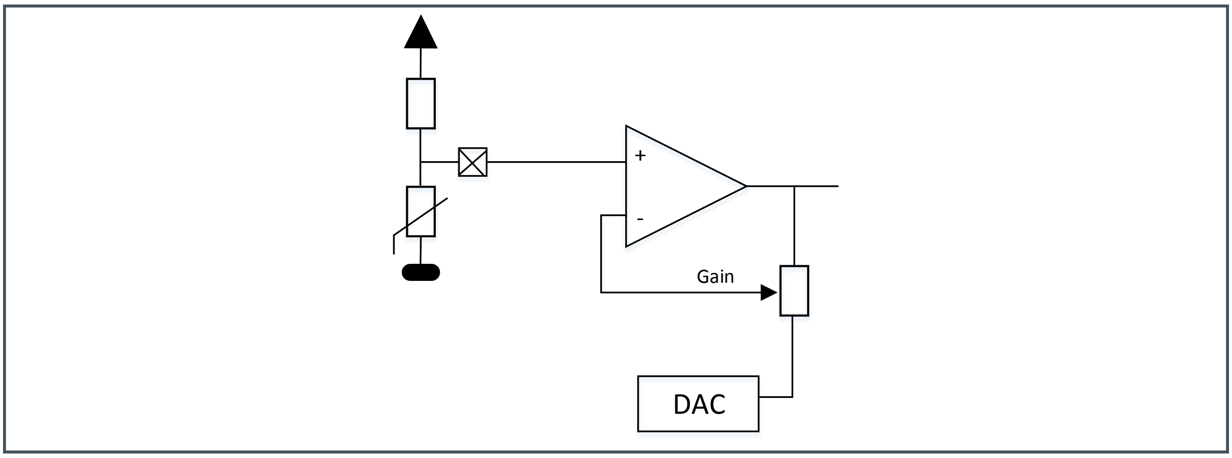


Figure 115:
Non Inverting Amplifier with Current Source and Offset (Temperature Sensor)

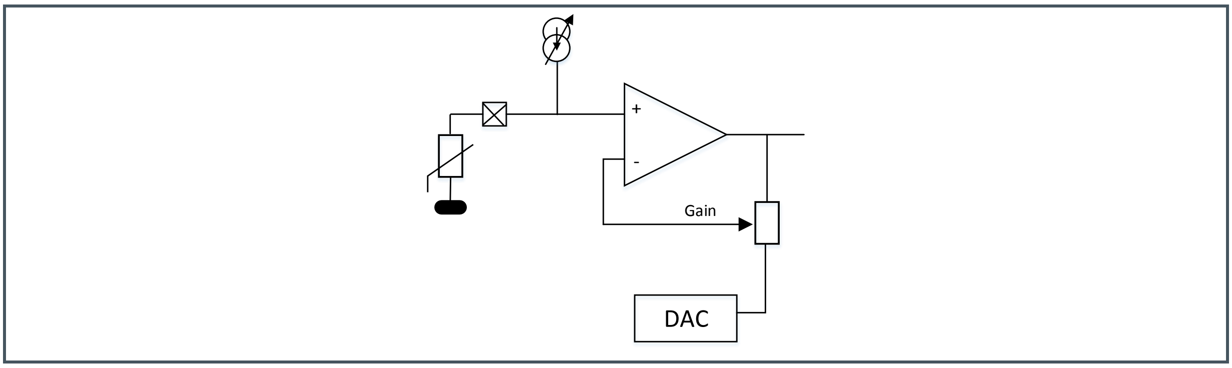


Figure 116:
Non Inverting Amplifier with Current Source and Reference Path (Temperature Sensor)

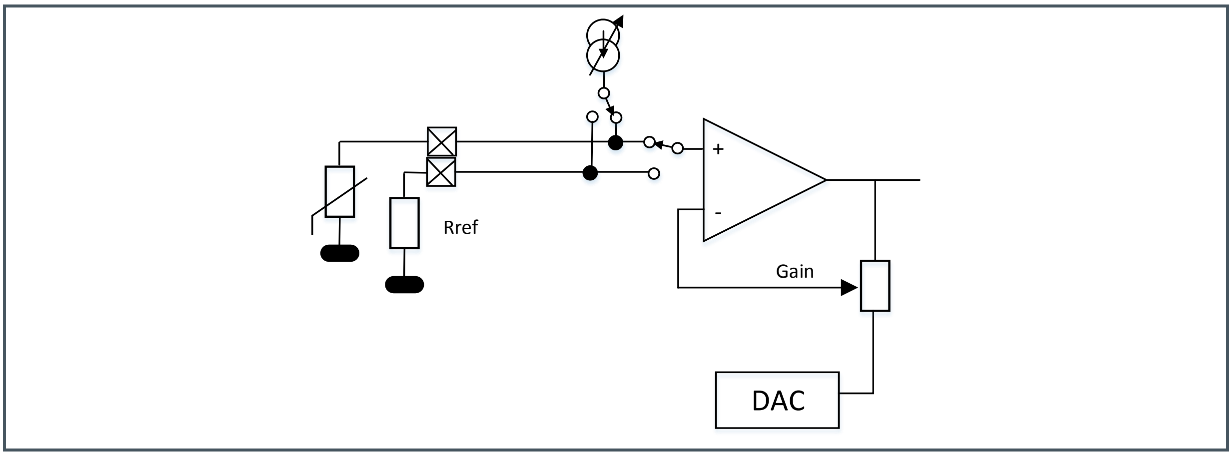


Figure 117:
Non Inverting Amplifier High Impedance, GND Referenced

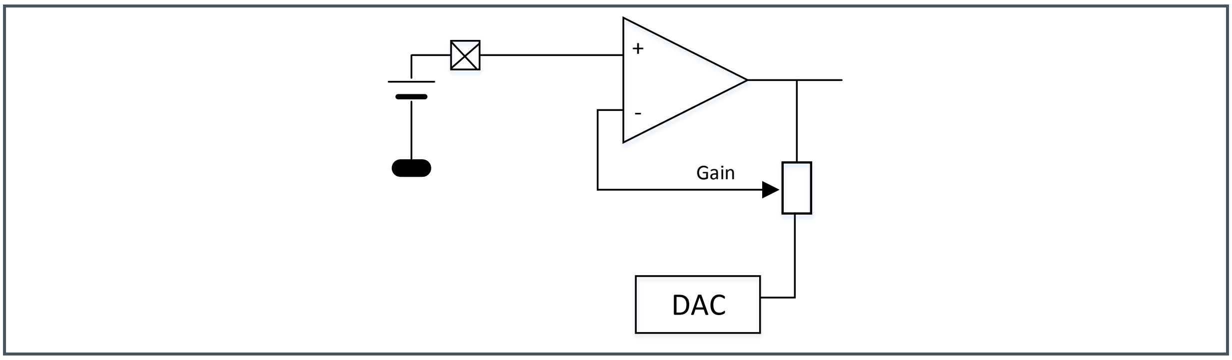


Figure 118:
Non Inverting Amplifier with DC-Blocking, Referenced to V_ADCRef/2

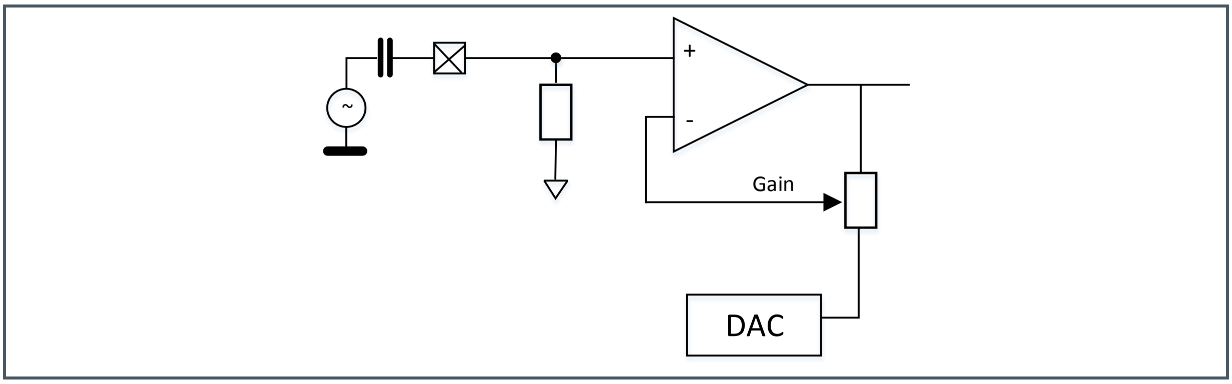
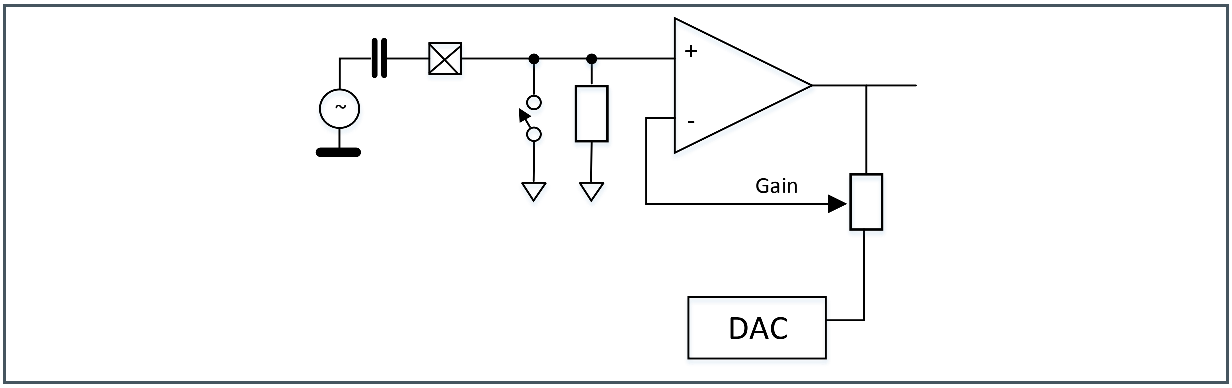


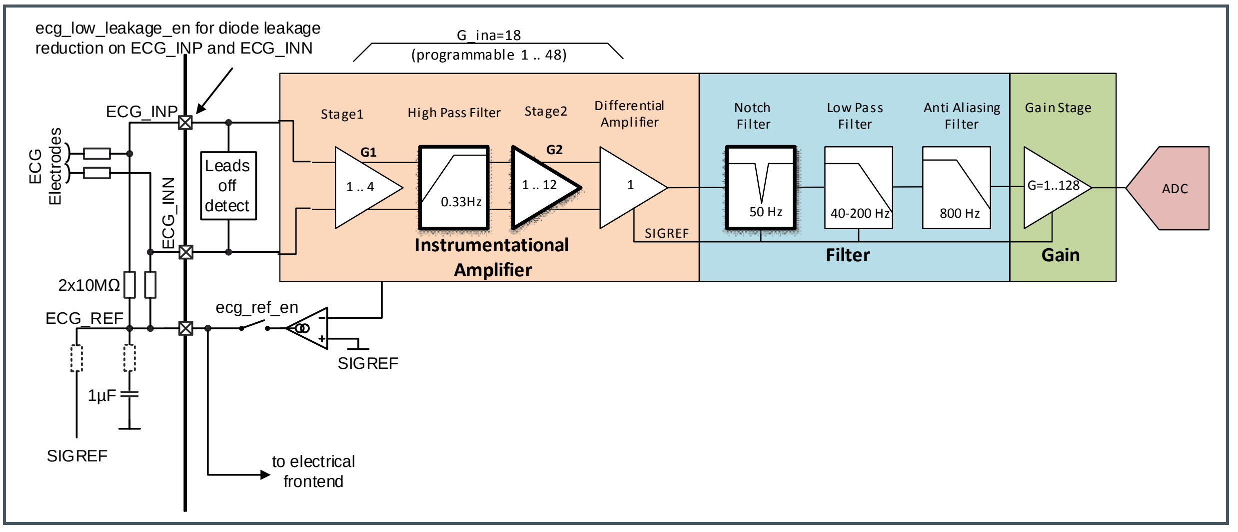
Figure 119:
Non Inverting Amplifier with DC-Blocking and Fast Settling Time, Referenced to ADCRef /2



7.1.17 ECG Amplifier

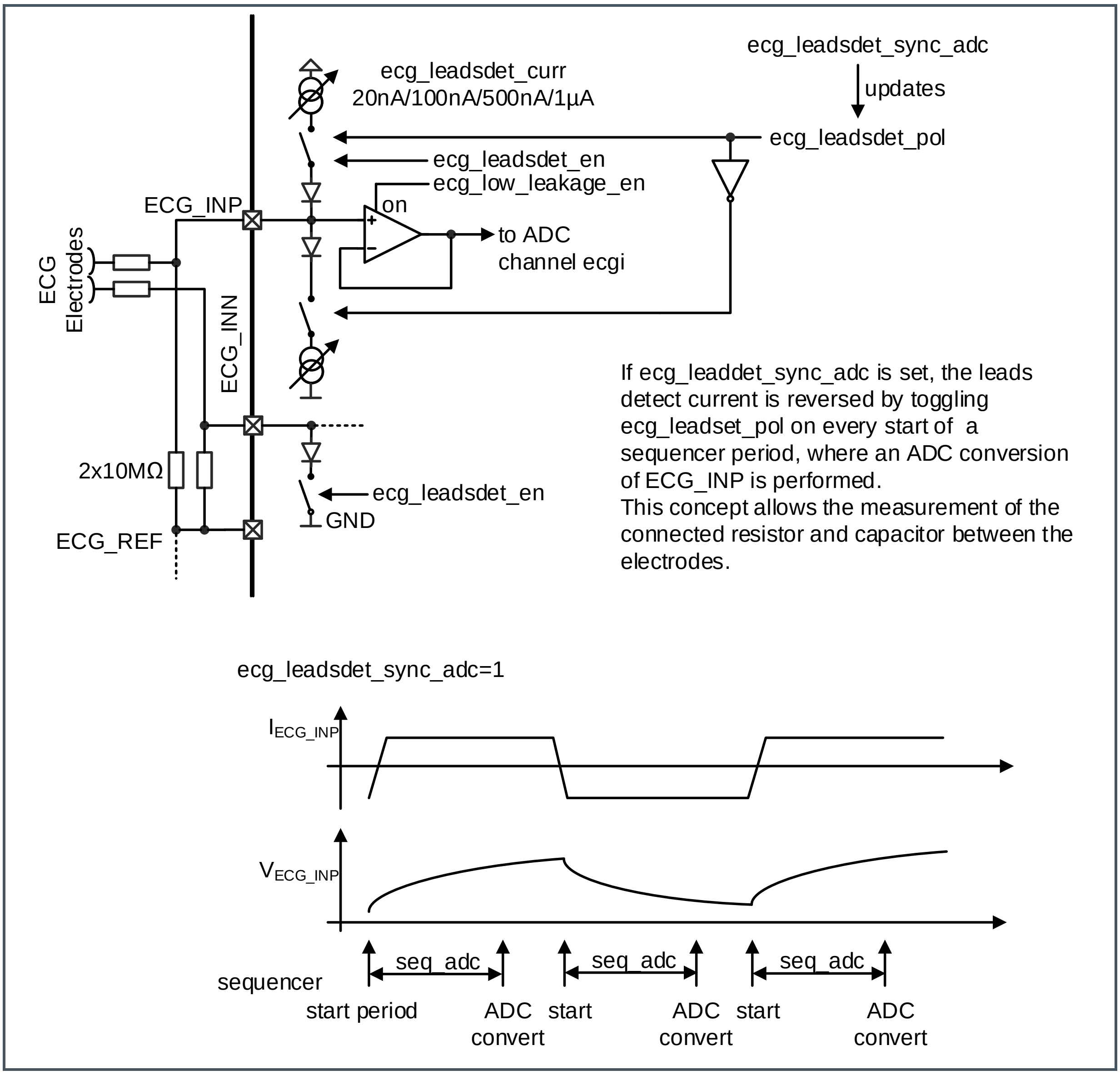
The ECG (electro cardiogram) amplifier is a high impedance, low noise instrumentation amplifier with analog circuitry to band pass filter the signal. Gain is distributed between 3 gain stages. The gain in the first stage determines the tradeoff between achievable noise level and achievable input offset voltage. An optional 50/60 Hz notch filter can be enabled to attenuate unwanted noise from mains coupling.

Figure 120:
ECG Amplifier Circuitry



ECG Lead OFF Detection

Figure 121:
ECG Lead-OFF Detection



The ECG lead OFF detection can be used for detection if the user actually touches the leads. It is a circuitry to measure the capacitor and/or resistance between the two lead inputs ECG_INP and ECG_INN.

7.1.18 ECG Registers

ECG_MODE (Address 0x5b)

Figure 122:
ECG_MODE Register

<table>
<tr><th>Addr: 0x5b</th><th colspan="5">ECG_MODE</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td>7</td><td>ecg_notch_sel60</td><td>0</td><td>RW</td><td colspan="2">0: Fc=50 Hz
1: Fc=60 Hz</td></tr>
<tr><td>6:4</td><td>ecg_hp_mode</td><td>0</td><td>RW</td><td colspan="2">0: Differential A-B</td></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">ecg_gain_g2</td><td rowspan="6">2</td><td rowspan="6">RW</td><td colspan="2">Gain INA2</td></tr>
<tr><td>Setting</td><td>Gain Factor</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>4</td></tr>
<tr><td>2</td><td>6</td></tr>
<tr><td>3</td><td>12</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">ecg_gain_g1</td><td rowspan="6">2</td><td rowspan="6">RW</td><td colspan="2">Gain INA1</td></tr>
<tr><td>Setting</td><td>Gain Factor</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>2</td><td>3</td></tr>
<tr><td>3</td><td>4</td></tr>
</table>

ECG_CFGA (Address 0x5c)

Figure 123:
ECG_CFGA Register

Addr: 0x5c		ECG_CFGA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ecg_en	0	RW	Enable ECG instrumentation amplifier
6	ecg_clk_off	0	RW	0: All ECG clocks enable 1: All ECG clocks disable

Addr: 0x5c		ECG_CFGA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	ecg_gain_byp	0	RW	0: Gain stage is used 1: Gain stage is ECGREF
4	ecg_lp_byp	0	RW	0: LP stage is used 1: LP stage is bypassed
3	ecg_notch_byp	1	RW	0: Notch stage is used 1: Notch stage is bypassed
2	ecg_diff_byp	0	RW	0: Diffamp stage isused 1: Diffamp stage is bypassed
1:0	ecg_hp_byp	0	RW	00: HP filter is used 01: Not used 10: Not Used 11: HP filter is bypassed

ECG_CFGB (Address 0x5d)

Figure 124:
ECG_CFGB Register

<table>
<tr><th colspan="2">Addr: 0x5d</th><th colspan="5">ECG_CFGB</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="3">Bit Description</th></tr>
<tr><td>7</td><td>ecg_fast_startup</td><td>0</td><td>RW</td><td colspan="3">ECG fast startup</td></tr>
<tr><td rowspan="6">6:5</td><td rowspan="6">ecg_lp_freq</td><td rowspan="6">0</td><td rowspan="6">RW</td><td colspan="3">ECG low pass cutoff frequency</td></tr>
<tr><th>Setting</th><th>Pulse Frequency</th><th>Cutoff Frequency</th></tr>
<tr><td>0</td><td>31.25 kHz</td><td>40 Hz</td></tr>
<tr><td>1</td><td>62.5 kHz</td><td>80 Hz</td></tr>
<tr><td>2</td><td>125 kHz</td><td>160 Hz</td></tr>
<tr><td>3</td><td>250 kHz</td><td>320 Hz</td></tr>
<tr><td rowspan="5">4:3</td><td rowspan="5">ecg_hp_freq</td><td rowspan="5">0</td><td rowspan="5">RW</td><td colspan="3">ECG High pass filter cutoff frequency</td></tr>
<tr><th>Setting</th><th>Filter Frequency</th><th>Cutoff Frequency</th></tr>
<tr><td>0</td><td>122 Hz</td><td>0.33 Hz</td></tr>
<tr><td>1</td><td>488 Hz</td><td>1.32 Hz</td></tr>
<tr><td>2</td><td>1935 Hz</td><td>5.28 Hz</td></tr>
</table>

Addr: 0x5d		ECG_CFGB				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
				3	3906 Hz	10.56 Hz
2:0	ecg_gain_g	0	RW	Gain		
				Setting	**Gain**	
				0	1	
				1	2	
				2	4	
				3	8	
				4	16	
				5	32	
				6	64	
				7	128	

ECG_CFGC (Address 0x5e)

Figure 125:
ECG_CFGC Register

Addr: 0x5e		ECG_CFGC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	Not used	0	RW	Do not use
1	ecg_low_leakage_en	0	RW	Enable ECG leakage compensation
0	ecg_ref_en	0	RW	ECG Reference Feedback Amplifier Enable

ECG_CFGD (Address 0x5f)

Figure 126:
ECG_CFGD Register

Addr: 0x5f		ECG_CFGD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Not used	0	RW	Do not use

<table>
<tr><th colspan="2">Addr: 0x5f</th><th colspan="3">ECG_CFGD</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td>4</td><td>ecg_leadsdet_sync_adc</td><td>0</td><td>RW</td><td>ECG Leads Detection Automatic Update. If this is asserted, then ecg_leadsdet_pol is inverted automatically at the start of a sequence (at count=2) if in this sequence the ADC will convert the ECGi channel.</td></tr>
<tr><td>3</td><td>ecg_leadsdet_pol</td><td>0</td><td>RW</td><td>ECG Leads Detection Polarity. Can be written to manually if ecg_leadsdet_sync_adc is clear, otherwise it is automatically toggled.</td></tr>
<tr><td>2:1</td><td>ecg_leadsdet_curr</td><td>0</td><td>RW</td><td>ECG Leads Detection Current<table><tr><th>Setting</th><th>Current</th></tr><tr><td>0</td><td>20 nA</td></tr><tr><td>1</td><td>100 nA</td></tr><tr><td>2</td><td>500 nA</td></tr><tr><td>3</td><td>1 µA</td></tr></table></td></tr>
<tr><td>0</td><td>ecg_leadsdet_en</td><td>0</td><td>RW</td><td>ECG Leads Detection Enable</td></tr>
</table>

ECG_THRESHOLD_LOW (Address 0x6a)

Figure 127:
ECG_THRESHOLD_LOW Register

Addr: 0x6a		ECG_THRESHOLD_LOW		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ecg_threshold_low	0	RW	If the ADC returns an ECG value below agc_threshold_low (not equal) at ecg_leadsdet_pol=0, then the lead_off interrupt can be triggered.

ECG_THRESHOLD_HIGH (Address 0x6b)

Figure128:
ECG_THRESHOLD_HIGH Register

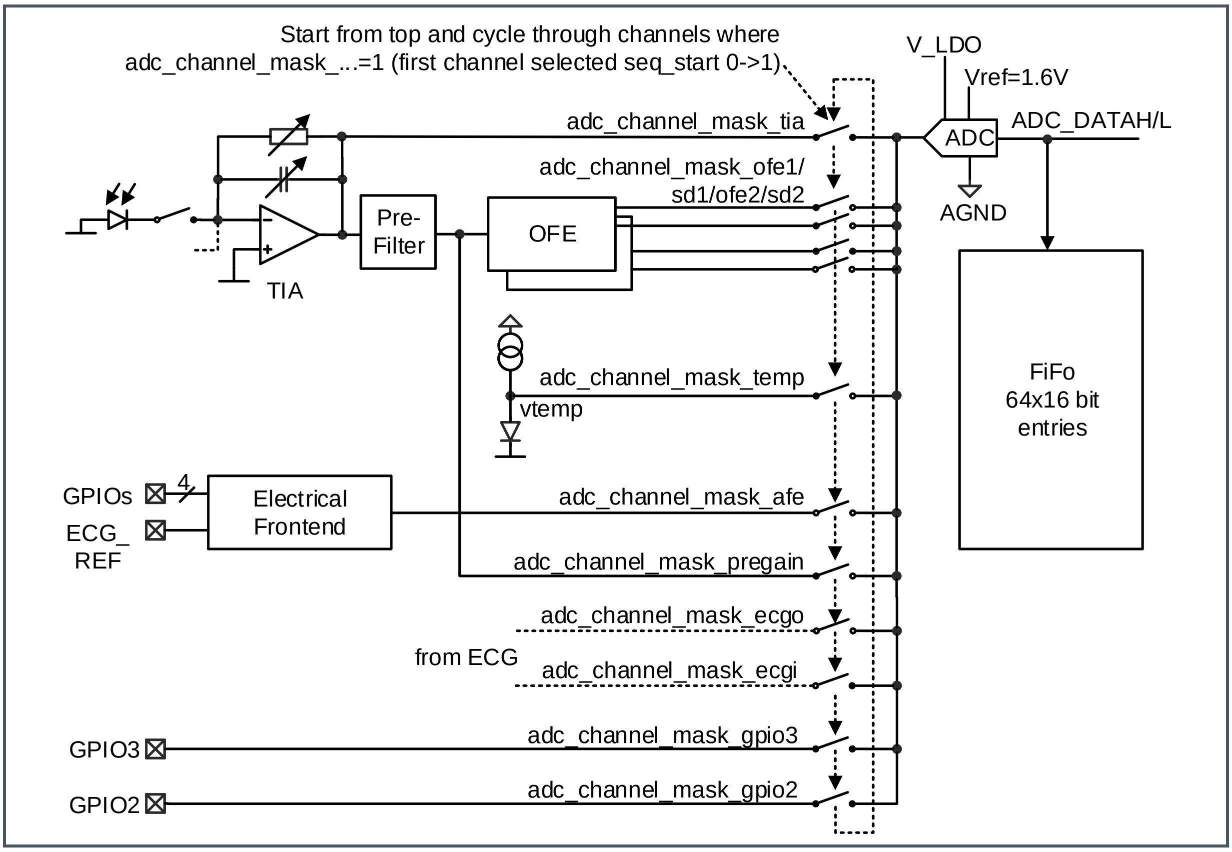
Addr: 0x6b		ECG_THRESHOLD_HIGH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ecg_threshold_high	FF	RW	If the ADC returns an ECG value above agc_threshold_high (not equal) at ecg_leadsdet_pol=1, then the lead_off interrupt can be triggered

7.1.19 ADC and FIFO

The ADC is a 14-bit successive-approximation register (SAR) type. It supports 14-bit with conversion time up to 50 ksps.

The ADC is started by the sequencer and its timing or in manual mode (man_mode=1) by setting seq_start=1 (seq_start stays ‘1’ as long as the conversion runs). The AS7030B can be configured to trigger an interrupt upon end of conversion.

Figure 129:
ADC Internal Circuit and Multiplexer



For best accuracy, the ADC can be optionally calibrated.

Information

If GPIO2 or GPIO3 is used as ADC input, there is no anti-aliasing filter in front of the ADC (needs to be added externally).

7.1.20 ADC Threshold

At the output of the ADC converter a digital threshold can be enabled. If the output of the ADC exceeds the threshold adc_threshold, it triggers an interrupt. This mechanism can be used to identify if an object is in proximity of the sensor and then to interrupt the host. In cases where no object is detected, the host can be sleeping therefore reducing power consumption of the system.

7.1.21 ADC Registers

ADC_THRESHOLD (Address 0x68)

Figure 130:
ADC_THRESHOLD Register

Addr: 0x68		ADC_THRESHOLD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	adc_threshold	0xff	RW	If the ADC returns a value above adc_threshold (not equal), then the adc_threshold interrupt can be triggered. Note that when only the upper 8 bits are compared, the lower 6 bits are ignored. A value of 0xff can therefore never trigger the interrupt

ADC_THRESHOLD_CFG (Address 0x69)

Figure 131:
ADC_THRESHOLD_CFG Register

Addr: 0x69		ADC_THRESHOLD_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	Not used	0	RW	Not used
1	adc_thresh_differential	0	RW	If adc_thresh_tia only is asserted and any of seq_adc[23]tia is non-zero, meaning that there are two or three ADC TIA measurements in one sequencer period, then the second is subtracted from the first, and the *difference* is being compared to the adc_threshold.
0	adc_thresh_tiaonly	0	RW	Normally, the adc_threshold works regardless of the adc channel. If this bit is set, then the threshold is only checked if the adc channel is TIA

ADC_CFGA (Address 0x88)

**Figure 132:
ADC_CFGA Register**

Addr: 0x88		ADC_CFGA			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	Not used	0	RW	Not used	
3:1	adc_multi_n	0	RW	Defines number of samples that are taken in multimode (adc_multimode =1)	
				Setting	**Number of Samples per ADC Conversion Command**
				0	2
				1	4
				2	8
				3	16
				4	32
				5	48
				6	64
				7	96
0	adc_multimode	0	RW	0: If ADC is started one sample is measured 1: If ADC is started multiple samples are stored in sequence in the FIFO. The number of samples is defined with "adc_multi_n".	

Information

If the ADC is triggered with the sequencer, the very first ADC conversion after seq_en=1 stores the number of samples according to above table. All subsequent samples use one sample less (e.g. 7 instead of 8).

ADC_CFGB (Address 0x89)

Figure 133:
ADC_CFGB Register

Addr: 0x89		ADC_CFGB					
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
7:6	Not used	0	RW	Not used			
5:3	adc_clock	0	RW	ADC clock divider: The ADC clock is freely configurable			
				Setting	**Periods**	**µs**	**kHz**
				0	2	1	1000
				1	4	2	500
				2	6	3	333
				3	8	4	250
				4	10	5	200
				5	12	6	167
				6	14	7	143
				7	16	8	125
2	adc_calibration	0	RW	To activate the optional self calibration, this bit must be asserted, and an ADC “conversion” has to be started in manual mode (man_mode=1) by asserting seq_start.			
1	ulp	0	RW	Ultra low power bit for the sequencer. If this bit is set and sd_subs>0, it disables the LED pulses and powers off the TIA in all sequences but the one where the TIA is sampled.			
0	adc_en	0	RW	0: Reset ADC 1: Enable ADC Warning: In reset state the ADC clears its calibration data. Re-calibration is necessary next time it is enabled again.			

ADC_CFGC (Address 0x8a)

Figure 134:
ADC_CFGC Register

Addr: 0x8a		ADC_CFGC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Not used	0	RW	Not used

<table>
<tr><th colspan="2">Addr: 0x8a</th><th colspan="6">ADC_CFGC</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="4">Bit Description</th></tr>
<tr><td>4</td><td>adc_selfpd</td><td>0</td><td>RW</td><td colspan="4">1: Power down the ADC when not converting; use this to conserve power, but set adc_settling_time to minimum 64µs to permit settling of the ADC reference buffer.
0: Always enable ADC</td></tr>
<tr><td>3</td><td>adc_discharge</td><td>0</td><td>RW</td><td colspan="4">0: Suppress ADC capacitor discharging – use with caution
1: Discharge ADC capacitor before tracking
If asserted, the capacitor is discharged before the tracking phase. If zero, the discharge phase is suppressed and the tracking phase is started one cycle earlier</td></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">adc_settling_time</td><td rowspan="10">0</td><td rowspan="10">RW</td><td colspan="4">ADC settling time: Use with synchronous demodulator. It defines the number of ADC clock cycles the sampling window is kept open additionally.
If the gain stage in the optical frontend is used (gain_byp=0), set this to minimum 8 µs. If adc_selfpd=1, set this to minimum 64 µs.</td></tr>
<tr><th>Setting</th><th>Periods</th><th>µs (@500 kHz)</th><th>µs (@250 kHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>4</td><td>8</td><td>16</td></tr>
<tr><td>2</td><td>8</td><td>16</td><td>32</td></tr>
<tr><td>3</td><td>16</td><td>32</td><td>64</td></tr>
<tr><td>4</td><td>32</td><td>64</td><td>128</td></tr>
<tr><td>5</td><td>64</td><td>128</td><td>256</td></tr>
<tr><td>6</td><td>128</td><td>256</td><td>512</td></tr>
<tr><td>7</td><td>256</td><td>512</td><td>1 ms</td></tr>
</table>

ADC_CHANNEL_MASK_L (Address 0x8b)

Figure 135:
ADC_CHANNEL_MASK_L Register

Addr: 0x8b		ADC_CHANNEL_MASK_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	adc_channel_mask_pregain	0	RW	Pregain channel selection
6	adc_channel_mask_afe	0	RW	Electrical front end

Addr: 0x8b		ADC_CHANNEL_MASK_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	adc_channel_mask_temp	0	RW	Temperature measurement
4	adc_channel_mask_sd2	0	RW	Synchronous modulator 2 output just before the gain stage
3	adc_channel_mask_ofe2	0	RW	Synchronous modulator 2 output after the gain stage
2	adc_channel_mask_sd1	0	RW	Synchronous modulator 1 output just before the gain stage
1	adc_channel_mask_ofe1	0	RW	Synchronous modulator 1 output after the gain stage
0	adc_channel_mask_tia	0	RW	Trans-impedance amplifier output

The adc channel is chosen automatically from the bits within the adc_channel_mask_* set. It starts from right and finishes left (LSB->MSB) and wraps back from the most significant asserted bit to the least significant of the asserted bits. After every ADC conversion it switches to the next enabled channel, (except around the adc2tia/adc3tia cases). See register description FIFOH (Figure 144) and FIFOL (Figure 143) for encoding of the first channel in the data stream.

This applies to both, manual mode and sequencer mode. In sequencer mode, it starts with the smallest channel when the sequencer is being started. In manual mode, the adc_sel is reset with every write to either ADC_CHANNEL_MASK_L or ADC_CHANNEL_MASK_H.

ADC_CHANNEL_MASK_H (Address 0x8c)

Figure 136:
ADC_CHANNEL_MASK_H Register

Addr: 0x8c		ADC_CHANNEL_MASK_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Not used	0	RW	Not used
3	adc_channel_mask_gpio2	0	RW	GPIO2 input – set gpio2_a=1 and Write 0x47 to register 0xC6 Write 0x0C to register 0xC2 Write 0x0C to register 0xC3
2	adc_channel_mask_gpio3	0	RW	GPIO3 input – set gpio3_a=1 and Write 0x47 to register 0xC6 Write 0x0C to register 0xC2 Write 0x0C to register 0xC3
1	adc_channel_mask_ecgi	0	RW	ECG amplifier input – use for leads off detection

Addr: 0x8c		ADC_CHANNEL_MASK_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	adc_channel_mask_ecgo	0	RW	ECG amplifier output – amplified ECG signal

ADC_DATA_L (Address 0x8e)

Figure 137:
ADC_DATA_L Register

Addr: 0x8e		ADC_DATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	adc_data[7:0]	0	RO	Current ADC output: low byte

The ADC_DATA register shows the current raw output of the ADC.

ADC_DATA_H (Address 0x8f)

Figure 138:
ADC_DATA_H Register

Addr: 0x8f		ADC_DATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Not used	0	RO	Not used
5:0	adc_data[13:8]	0	RO	Current ADC output: High byte warning: there is no latch mechanism implemented to guarantee consistency if the ADC is possibly running when reading this register, then the data can be corrupted - use the FIFO to guarantee data consistency

7.1.22 FIFO Register

FIFO_CFG (Address 0x78)

Figure 139:
FIFO_CFG Register

Addr: 0x78		FIFO_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Not used	0	RW	Not used
6:0	fifo_threshold	0	RW	FIFO threshold: The fifo_threshold interrupt is flagged if there are more than this many entries in the FIFO. 0: Interrupt with 1 (16-bit) entry in FIFO 127: Interrupt when FIFO is full but one

FIFO_CNTRL (Address 0x79)

Figure 140:
FIFO_CNTRL Register

Addr: 0x79		FIFO_CNTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Not used	0	RW	Not used
0	fifo_clear	0	PUSH1	Write a 1 here to clear the FIFO. Can be useful when switching from one sequencer mode to another to make sure that there are no old FIFO entries left

FIFOSTATUS (Address 0xa4)

Figure 141:
FIFOSTATUS Register

Addr: 0xa4		FIFOSTATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Not used	0	RO	Not used
0	fifo overflow	0	RO	FIFO overflow indicator

FIFOLEVEL (Address 0xa6)

Figure 142:
FIFOLEVEL Register

Addr: 0xa6		FIFOLEVEL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	fifolevel	0	RO	FIFO fill level (0..128)

FIFOL (Address 0xFE)

Figure 143:
FIFOL Register

Addr: 0xfe		FIFOL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	fifol	0	PUSHPOP	Low byte of FIFO

FIFOL can be read out with single reads (2 consecutive I²C addresses have to be read to get one FIFO entry) or with block-read (up to 2 x fifo_depth values can be read in a single block-read)

Upon reading of FIFOH, it automatically advances the internal read pointer and decreases FIFO level. If reading beyond end of FIFO, data will return 00h. There is no underrun flag, this is not an error condition.

Use **ams** SDK functions to read from the FIFO register to keep the reading in synchronization with the ADC channel selection. If synchronization is no concern use [fifoh[7:0] : fifol[7:2]] as ADC result as the ADC data is multiplied by x4 before it is pushed in to the FIFO. FIFOl[0] is used as an ADC first channel indication. The first channel indication bit toggles upon every new entry unless the first ADC channel is transmitted. Then toggling can be stopped for up to 5 FIFO entries and the very first stopping indicates the first ADC channel. To allow encoding of any number of ADC channels, the first ADC channel encoding is dropped from time to time.

FIFOH (Address 0xff)

Figure 144:
FIFOH Register

Addr: 0xff		FIFOH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	fifoh	0	PUSHPOP	High byte of FIFO

See Interrupts for the actual FIFO interrupt.

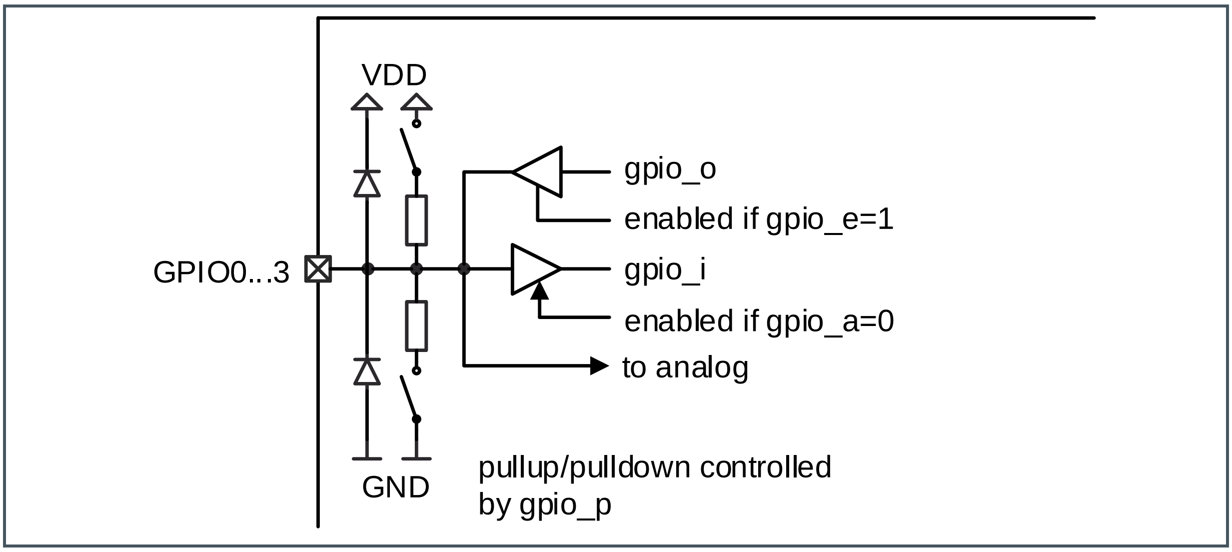
7.1.23 Digital Interface

After setting the pin ENABLE=1 the AS7030B registers can be accessed by the I²C interface. Before enabling any additional function (current source, TIA, ADC…) set the bit ldo_en=1 to set the internal LDO to normal mode.

For operating the ADC or the sequencer enable the oscillator by setting osc_en=1

GPIO Pins

Figure 145:
GPIO Pin Diagram



Interrupts

An interrupt output pin INT can be used to interrupt the host. Following interrupt sources are possible:

irq_adc: End of ADC conversion

irq_sequencer: End of sequencer sequence reached

irq_ltf: A light-to-frequency conversion is finished

irq_adc_threshold: ADC threshold triggered – see ADC Threshold

irq_fifothreshold: FIFO almost full (as defined in bit fifo_threshold)

irq_fifooverflow: FIFO overflow (error condition, data is lost)

irq_clipdetect: TIA output and/or SD output exceeded threshold– see details in CLIPSTATUS Register

irq_led_supply_low: LED supply low comparator triggered – see details in LEDSTATUS Register

Depending on the setting in register INTENAB each of the above interrupt source can assert INT output pin (active low).

7.2 I²C

The AS7030B includes an I²C slave using an I²C address of 0x30 (7-bit format; R/W bit has to be added) respectively 60 h (8-bit format for writing) and 61 h (8-bit format for reading). It expects external pull-up resistors.

7.2.1 I²C Serial Interface

I²C Feature List

- Fast mode (400 kHz) and standard mode (100 kHz) support
- 7+1-bit addressing mode
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

I²C Protocol

Figure 146:
I²C Symbol Definition

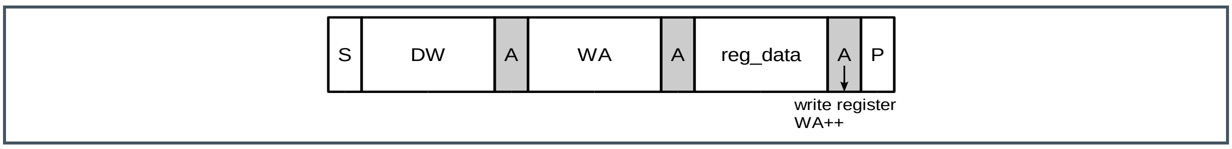
Symbol	Definition	RW	Note
S	Start condition after stop	R	1-bit
Sr	Repeated start	R	1-bit
DW	Device address for write	R	0110 0000b (60 h)
DR	Device address for read	R	0110 0001b (61 h)
WA	Word address	R	8-bit
A	Acknowledge	W	1-bit
N	No Acknowledge	R	1-bit
reg_data	Register data/write	R	8-bit
data (n)	Register data/read	W	8-bit
P	Stop condition	R	1-bit
WA++	Increment word address internally	R	During acknowledge

I²C Symbol Definition: Shows the symbols used in the following mode descriptions.

I²C Write Access

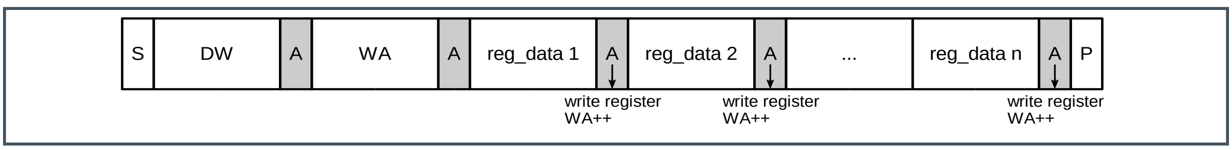
Byte Write and Page Write formats are used to write data to the slave

Figure 147:
I²C Byte Write



I²C Byte Write: Shows the format of an I²C byte write access

Figure 148:
I²C Page Write

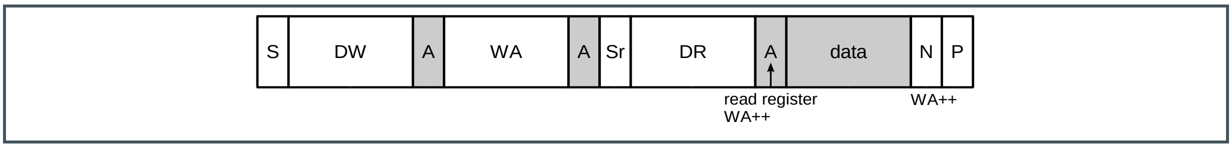


I²C Page Write: Shows the format of an I²C page write access

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 149:
I²C Random Read



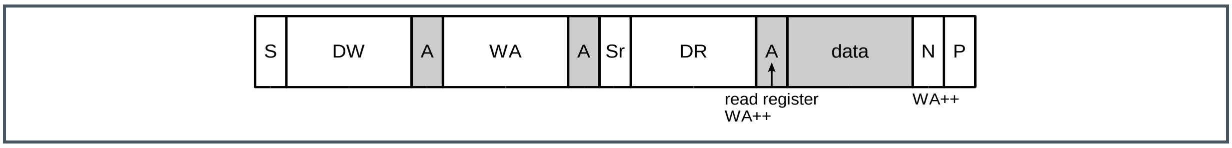
I²C Random Read: Shows the format of an I²C random read access

Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

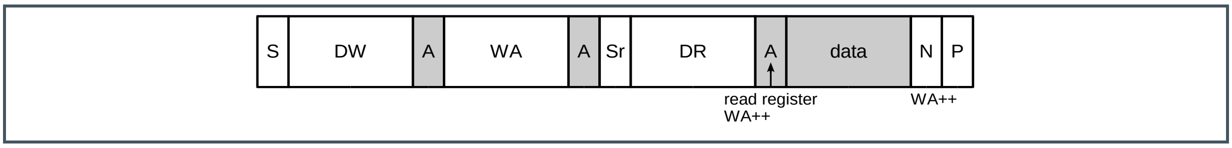
Figure 150:
I²C Sequential Read



I²C Sequential Read: Shows the format of an I²C sequential read access

Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 151:
I²C Current Address Read



I²C Current Address Read: Shows the format of an I²C current address read access.

To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission, the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

CONTROL (Address 0x00)

Figure 152:
CONTROL Register

Addr: 0x00		CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Not used	0	RW	Not used
4	hs_en	0	RW	Enable I²C high speed
3	Not used	0	RW	Not used
2	clk_def	0	RW	Set the internal system frequency Programming is only possible if oscillator is be disable 0: 2 MHz. 1: 1 MHz

Addr: 0x00		CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	osc_en	0	RW	Enable the oscillator. The oscillator must be enabled for any analog block (ADC, sequencer, optical frontend, sequencer); not mandatory for current sinks or ECG amplifier
0	ldo_en	0	RW	If the EN input is not asserted, the chip is in reset If asserted, I²C transactions are possible. Upon assertion of ldo_en, the reference and the LDO are enabled The LDO must be enabled for anything but plain I²C register read/write

GPIO_A (Address 0x08)

Figure 153:
GPIO_A Register

Addr: 0x08		GPIO_A		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Not used	0	RW	Not used
3	gpio3_a	0	RW	1: Put GPIO3 in analog mode; set this bit when used for an analog function e.g. the electrical frontend. If set execute following I²C commands (otherwise an internal pulldown will be enabled) in this sequence: Write 0x47 to register 0xC6 Write 0x0C to register 0xC2 Write 0x0C to register 0xC3
2	gpio2_a	0	RW	1: Put GPIO2 in analog mode If set execute following I²C commands (otherwise an internal pulldown will be enabled) in this sequence: Write 0x47 to register 0xC6 Write 0x0C to register 0xC2 Write 0x0C to register 0xC3
1	gpio1_a	0	RW	1: Put GPIO1 in analog mode
0	gpio0_a	0	RW	1: Put GPIO0 in analog mode

GPIO_E (Address 0x09)

Figure 154:
GPIO_E Register

Addr: 0x09		GPIO_E		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Not used	0	RW	Not used
3	gpio3_e	0	RW	GPIO3 output enabled if set
2	gpio2_e	0	RW	GPIO2 output enabled if set
1	gpio1_e	0	RW	GPIO1 output enabled if set
0	gpio0_e	0	RW	GPIO0 output enabled if set

GPIO_O (Address 0x0a)

Figure 155:
GPIO_O Register

Addr: 0x0a		GPIO_O		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Not used	0	RW	Not used
3	gpio3_o	0	RW	If gpio3_e=1, gpio3_o defines the output state of GPIO3
2	gpio2_0	0	RW	If gpio2_e=1, gpio2_o defines the output state of GPIO2
1	gpio1_0	0	RW	If gpio1_e=1, gpio1_o defines the output state of GPIO1
0	gpio0_0	0	RW	If gpio0_e=1, gpio0_o defines the output state of GPIO0

GPIO_I (Address 0x0b)

Figure 156:
GPIO_I Register

Addr: 0x0b		GPIO_I		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Not used	0	RO	Not used

Addr: 0x0b		GPIO_I		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	gpio3_i	0	RO	The digital value sensed on GPIO3
2	gpio2_i	0	RO	The digital value sensed on GPIO2
1	gpio1_i	0	RO	The digital value sensed on GPIO1
0	gpio0_i	0	RO	The digital value sensed on GPIO0

GPIO_P (Address 0x0c)

Figure 157:
GPIO_P Register

Addr: 0x0c		GPIO_P		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio3_pd	0	RW	GPIO3 pulldown configuration 0: No pulldown on GPIO3 1: Pulldown to GND on GPIO3
6	gpio3_pu	0	RW	GPIO3 pullup configuration 0: No pullup on GPIO3 1: Pullup to VDD on GPIO3
5	gpio2_pd	0	RW	GPIO2 pulldown configuration
4	gpio2_pu	0	RW	GPIO2 pullup configuration
3	gpio1_pd	0	RW	GPIO1 pulldown configuration
2	gpio1_pu	0	RW	GPIO1 pullup configuration
1	gpio0_pd	0	RW	GPIO0 pulldown configuration
0	gpio0_pu	0	RW	GPIO0 pullup configuration

GPIO_SR (Address 0x0d)

Figure 158:
GPIO_SR Register

Addr: 0x0d		GPIO_SR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Not used	0	RW	Not used

Addr: 0x0d		GPIO_SR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	gpio3_sr	0	RW	GPIO3 slew rate configuration 0: Default slew rate 1: Increased slew rate
2	gpio2_sr	0	RW	GPIO2 slew rate configuration
1	gpio1_sr	0	RW	GPIO1 slew rate configuration
0	gpio0_sr	0	RW	GPIO0 slew rate configuration

GPIO_SYNC (Address 0x0f)

Figure 159:
GPIO_SYNC Register

Addr: 0x0f		GPIO_SYNC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Not used	0	RW	Not used
2	gpio_edge	0	RW	Used edge on selected GPIO for synchronization. 0: posedge 1: negedge
1:0	gpio_select	0	RW	0: GPIO0 1: GPIO1 2: GPIO2 3: GPIO3

An external synchronization signal can be used to start the sequencer for an ADC cycle.

The synchronization signal is available via a GPIO.

The used GPIO and Edge (positive, negative or both) can be programmed.

SUBID (Address 0x91)

Figure 160:
SUBID Register

Addr: 0x91		SUBID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	subid	NA	RO	Defines product version. Do not rely on bits defined as ‘X’. 1XXXXb
2:0	Revision	NA	RO	Reserved. Do no use and do not rely that the content stays the same for each device.

ID (Address 0x92)

Figure 161:
ID Register

Addr: 0x92		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	id	15	RO	Part number identification **Value** / **Meaning** 010101 / AS7030B
1:0	Id_reserved	NA	RO	Reserved. Do no use and do not rely that the content stays the same for each device.

STATUS (Address 0xa0)

Figure 162:
STATUS Register

Addr: 0xa0		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	irq_led_supply_low	0	R_PUSH1	Check LEDSTATUS
6	irq_clipdetect	0	R_PUSH1	Check CLIPSTATUS
5	irq_fifooverflow	0	R_PUSH1	FIFO overflow (error condition, new data is lost)

Addr: 0xa0		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	irq_fifothreshold	0	R_PUSH1	FIFO is almost full (as defined in fifo_threshold, usually 3/4)
3	irq_adc_threshold	0	R_PUSH1	The ADC value was above the programmed adc_threshold register setting
2	irq_ltf	0	R_PUSH1	LTF measurement is done. check LTFSTATUS (or ignore it)
1	irq_sequencer	0	R_PUSH1	All configured sequencer iterations have finished
0	irq_adc	0	R_PUSH1	ADC has finished

The STATUS register shows the current state of the interface. Some bits in here can trigger an interrupt.

An asserted bit can be cleared by writing a '1' to it - in case of irq_led_supply_low and irq_clipdetect, this also clears the underlying condition in the CLIPSTATUS and LEDSTATUS registers.

The FIFO threshold interrupt cannot be cleared directly, but only by lowering the FIFO level. The FIFO overflow interrupt is sticky and must be cleared explicitly.

STATUS2 (Address 0xa1)

Figure 163:
STATUS2 Register

Addr: 0xa1		STATUS2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Not used	0	R_PUSH1	Not used
2	irq_ltf_threshold_high	0	R_PUSH1	The LTF value was above the programmed ltf_threshold_high register setting
1	irq_ltf_threshold_low	0	R_PUSH1	The LTF value was below the programmed ltf_threshold_low register setting

Addr: 0xa1		STATUS2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	irq_ecg_threshold	0	R_PUSH1	If programmed ecg_leadsdet_pol=0, the ecg ADC value was below the programmed ecg_threshold_low setting If programmed ecg_leadsdet_pol=1, the ecg ADC value was above the programmed ecg_threshold_high setting

The STATUS2 register shows the current state of the interface. Some bits in here can trigger an interrupt.

In normal mode, an asserted bit can be cleared by writing a '1' to it (in normal mode).

In clear-on-read mode, reading the STATUS2 register clears all bits.

CLIPSTATUS (Address 0xa2)

Figure 164:
CLIPSTATUS Register

Addr: 0xa2		CLIPSTATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Not used	0	RO	Not used
3	pd_clipdetect_l	0	RO	If this bit is asserted, photo diode amplifier has been below the lower threshold
2	pd_clipdetect_h	0	RO	If this bit is asserted, photo diode amplifier has been above the upper threshold
1	sd_clipdetect_l	0	RO	If this bit is asserted, photo diode amplifier has been below the lower threshold
0	sd_clipdetect_h	0	RO	If this bit is asserted, photo diode amplifier has been above the upper threshold

LEDSTATUS (Address 0xa3)

Figure 165:
LEDSTATUS Register

Addr: 0xa3		LEDSTATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Not used	0	RO	Not used
3	led4_supply_low	0	RO	If this bit is asserted, LED4 voltage has been too low
2	led3_supply_low	0	RO	If this bit is asserted, LED3 voltage has been too low
1	led2_supply_low	0	RO	If this bit is asserted, LED3 voltage has been too low
0	led1_supply_low	0	RO	If this bit is asserted, LED1 voltage has been too low

LTFSTATUS (Address 0xa5)

Figure 166:
LTFSTATUS Register

Addr: 0xa5		LTFSTATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Not used	0	RO	Not used
5	ltf1_threshold_high	0	RO	The LTF1 value was above the programmed ltf_threshold_high register setting
4	ltf1_threshold_low	0	RO	The LTF1 value was below the programmed ltf_threshold_low register setting
3	ltf0_threshold_high	0	RO	The LTF0 value was above the programmed ltf_threshold_high register setting
2	ltf0_threshold_low	0	RO	The LTF0 value was below the programmed ltf_threshold_low register setting
1	ltf_sat	0	RO	Analog saturation occurred. Note that reading this bit is optional, as the ltfdata values are set to 0xffff in case of saturation.
0	ltf_done	0	RO	LTF measurement completed

INTENAB (Address 0xa8)

Figure 167:
INTENAB Register

Addr: 0xa8		INTENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	irq_led_supply_low_enab	0	RW	1: Enable LED supply low interrupt
6	irq_clipdetect_enab	0	RW	1: Enable clipdetect interrupt
5	irq_fifooverflow_ena	0	RW	1: Enable fifooverflow interrupt
4	irq_fifothreshold_enab	0	RW	1: Enable fifothreshold interrupt
3	irq_adc_threshold_enab	0	RW	1: Enable irq_adc_threshold as an interrupt source
2	irq_ltf_enab	0	RW	1: Enable LTF as an interrupt source
1	irq_sequencer_enab	0	RW	1: Enable irq_sequencer as an interrupt source
0	irq_adc_enab	0	RW	1: Enable irq_adc as an interrupt source

Each of the STATUS register bits can cause an interrupt (register INTR) if the respective bit is asserted in the INTENAB register

INTENAB2 (Address 0xa9)

Figure 168:
INTENAB2 Register

Addr: 0xa9		INTENAB2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Not used	0	RW	Not used
2	irq_ltf1_threshold_enab	0	RW	1: Enable ltf_treshold_high or ltf_treshold_low in ltf1 as interrupt source
1	irq_ltf0_threshold_enab	0	RW	1: Enable ltf_treshold_high or ltf_treshold_low in ltf0 as interrupt source
0	irq_ecg_threshold_enab	0	RW	1: Enable ecg_treshold_high or ecg_treshold_low as interrupt source

INTR (Address 0xaa)

Figure 169:
INTR Register

Addr: 0xaa		INTR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	irq_led_supply_low_intr	0	RO	
6	irq_clipdetect_intr	0	RO	
5	irq_fifooverflow_intr	0	RO	
4	irq_fifothreshold_intr	0	RO	
3	irq_adc_threshold_intr	0	RO	
2	irq_ltf_intr	0	RO	
1	irq_sequencer_intr	0	RO	
0	irq_adc_intr	0	RO	

The INTR registers shows the bit or bits that are responsible for an asserted interrupt. Effectively, these bits are OR-ed together to drive the interrupt pin INT low (open drain output).

INTR2 (Address 0xab)

Figure 170:
INTR2 Register

Addr: 0xab		INTR2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Not used	0	RO	Not used
2	irq_ltf_threshold_high_intr	0	RO	ltf_treshold_high in ltf0 or/and ltf1
1	irq_ltf_threshold_low_intr	0	RO	ltf_treshold_low in ltf0 or/and ltf1
0	irq_ecg_threshold_intr	0	RO	ecg_treshold_high or ecg_treshold_low

8 Application Information

8.1 Application Examples

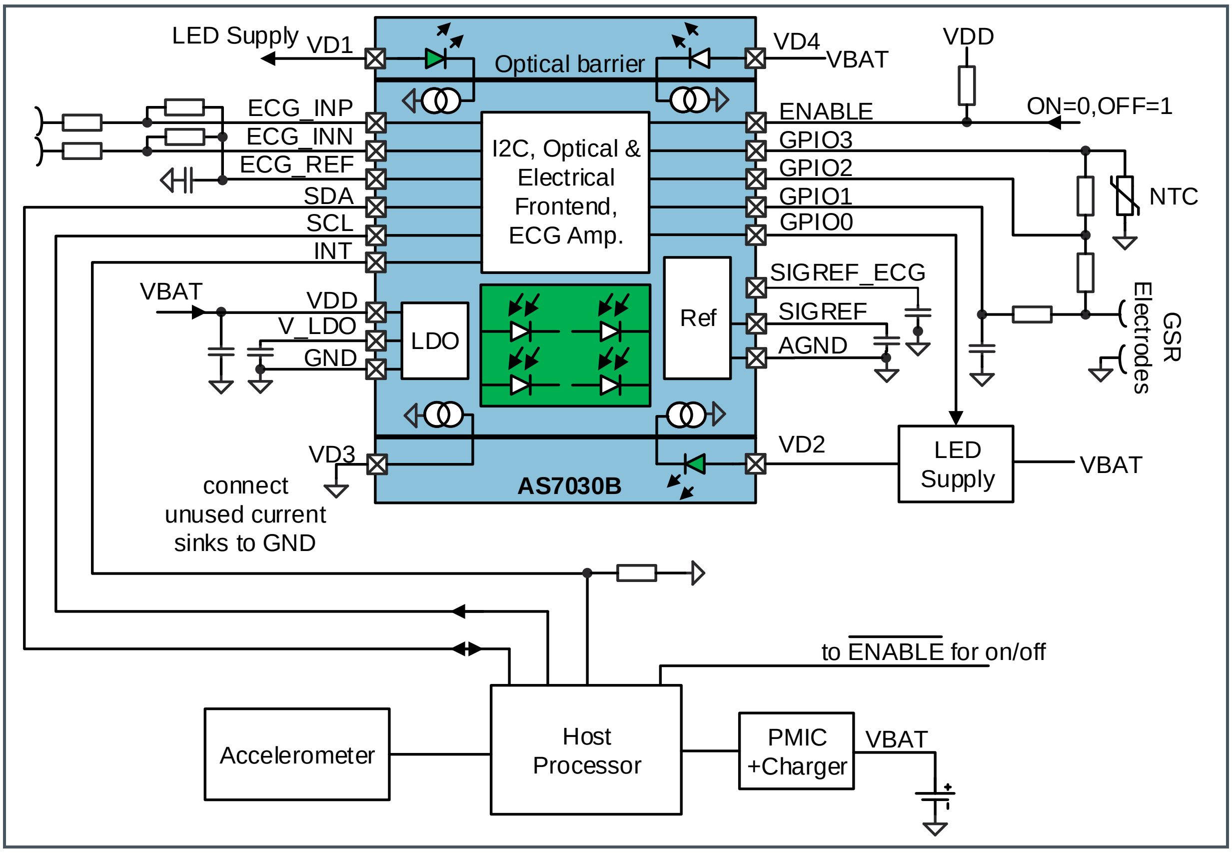
The following figure shows the complete integration of the AS7030B in a mobile optical measurement system for HRM, GSR (galvanic skin resistivity) and skin temperature using an NTC.

The device can be powered directly by a Li-ion battery as it has its own power management. Nevertheless the I²C interface can be powered by 1.8 V circuitry.

Information

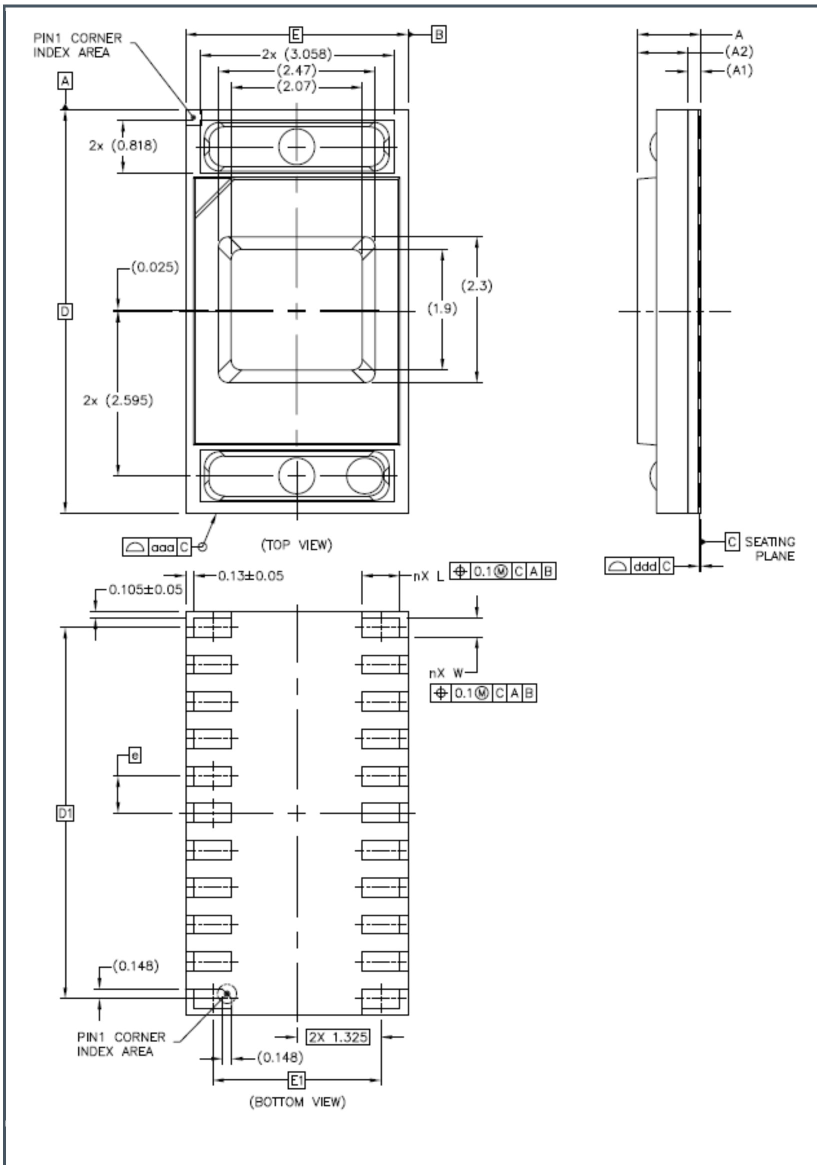
AS7030B can be used in the same configuration for e.g. a fitness band or a smart watch.

Figure 171:
AS7030B Optical HRM Measurement System for Wrist Based Application



9 Package Drawings & Markings

Figure 172:
OLGA-22 Package Outline Drawing



Ref.	Min	Nom	Max
A	0.9	1	1.1
A1		0.2	REF
A2		0.8	REF
D		6.36	BSC
E		3.51	BSC
W	0.25	0.3	0.35
L	0.55	0.6	0.65
e		0.585	BSC
N		22	
D1		5.85	BSC
E1		2.65	BSC
SD		---	BSC
SE		---	BSC
aaa		0.1	
ddd		0.08	

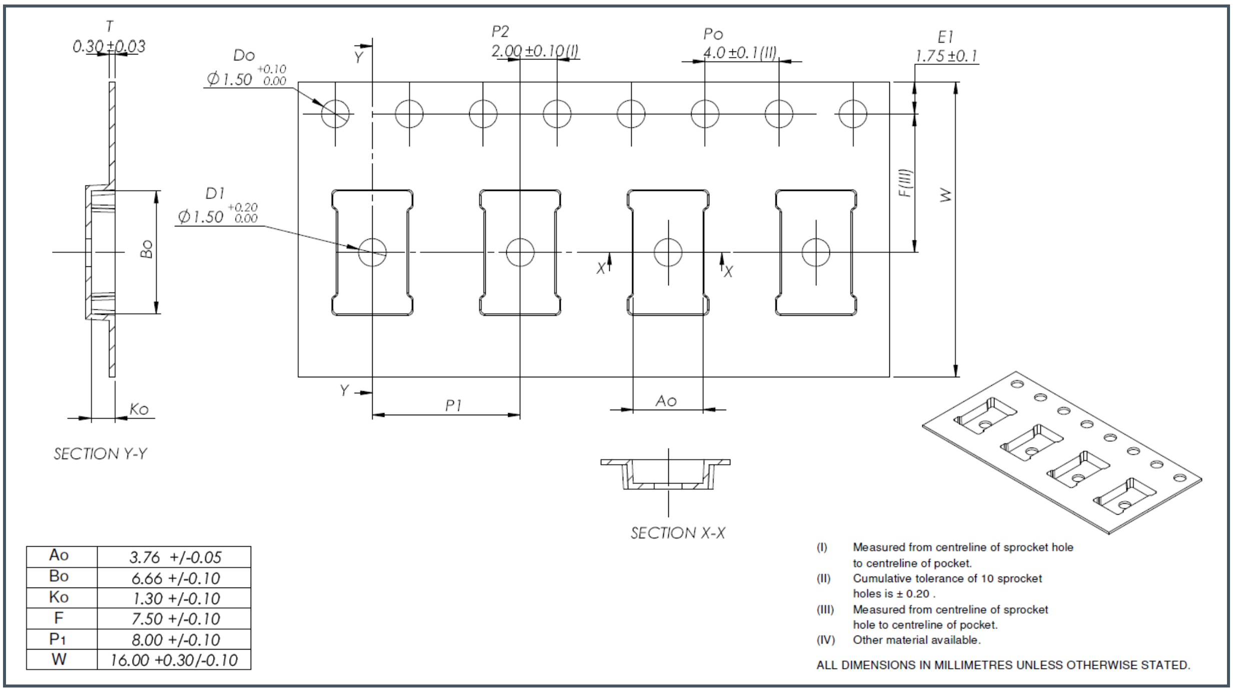
RoHS

Green

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.

10 Tape & Reel Information

Figure 173:
AS7030B Tape Dimensions



11 Soldering & Storage Information

Figure 174:
Solder Reflow Profile Graph

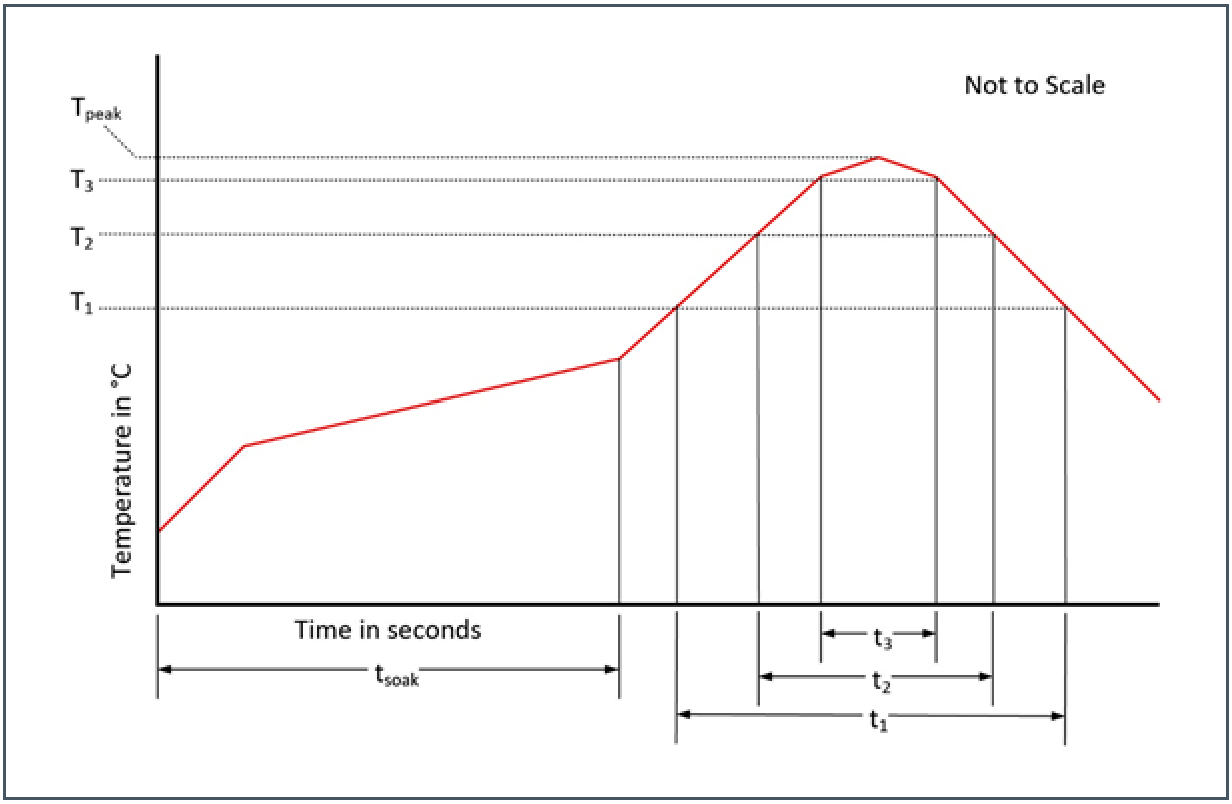


Figure 175:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max −5 °C/s

12 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
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Changes from previous version to current revision v1-00	Page
Initial version	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

13 Legal Information

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