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Coverpage: AS89000 Datasheet

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#### DATASHEET AS89000

#### Multi-channel programmable gain transimpedance amplifier

QSOP16 Order No.: 305100002 Status: preliminary

#### INTRODUCTION

The AS89000-devices are a family of integrated circuits of **programmable gain transimpedance amplifiers** with **4 channels** per IC (more custom specific, on request).

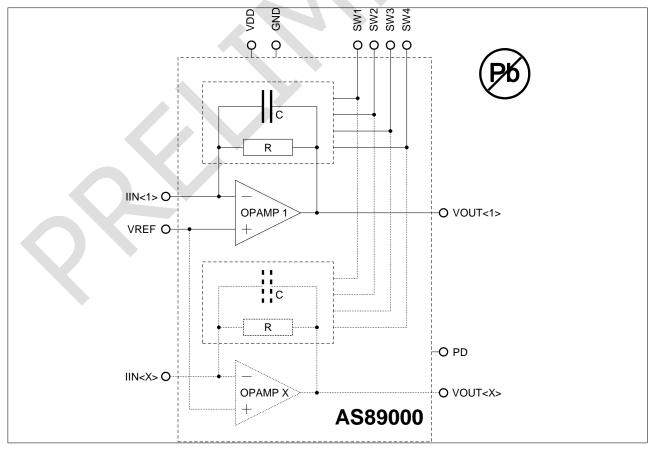
The AS89000-devices are mainly used for **signal conditioning of sensors with current outputs**. They are especially suitable for connection of photodiodes of **array and row sensors**. The possibility to **adjust the transimpedance in 8 stages** is a special feature.

The adjustment is made by programming three pins and is valid for all channels together.

The device packages (naked chip on request) are RoHS conform and optimized for **COB- mounting and SMD**.

#### **1 BLOCK DIAGRAM**

Figure 1: Block diagram



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## amu

V3.01

INT	RODUCT	ION1
1	BLOCK	DIAGRAM1
2	DESCRI	PTION OF INTERFACE
	2.1	Pin Assignment
	2.2	Adjustment of Transimpedance3
	2.3	Switchable Frequency Rrange3
	2.4	Power Down Mode
3	DESCRI	PTION OF FUNCTION4
4	ELECTR	ICAL CHARACTERISTICS
	4.1	Maximum Conditions
	4.2	Operating Conditions
	4.3	AC/DC-Characteristics
5	РАСКА	SES7
	5.1	Shape & Dimensions7
	5.2	Pin Configuration
	5.3	Soldering Information
6	APPLIC	ATIONS
	6.1	Connection of ams Sensors Germany Color Sensor
	6.2	Temperature Compensation of AS89000 via Reference Method 10
	6.3	Output Signals V <sub>OUT</sub> 11
ORI	DERING	INFORMATION12
LEG	AL NOTE	ES AND WARNINGS

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#### **2 DESCRIPTION OF INTERFACE**

#### 2.1 Pin Assignment

Table	1:	Pin	assignment

SIGNAL NAME	ΤΥΡ	A/D <sup>A</sup>	FUNCTION			
VDD	input	a/d	power supply			
GND	input	a/d	ground			
VREF	input	а	reference voltage			
SW1	input	d	input 1 for adjustment of transimpedance of AS89000-amplifier (pull			
SW2	input	d	input 2 for adjustment of transimpedance of AS89000-amplifier (p			
SW3	input	d	input 3 for adjustment of transimpedance of AS89000-amplifier (p			
SW4	input	d	switchable frequency range depended on input capacitance of the photo-sensor (pull down)			
PD	input	d	power down mode (pull down)			
IIN <x></x>	input	а	analog current input of amplifier X			
VOUT <x></x>	output	а	analog voltage output of amplifier X			

<sup>a</sup>) analog or digital

#### 2.2 Adjustment of Transimpedance

Table 2: Adjustment of Transimpedance

SETTIN	IGS OF DIGITAL	INPUTS	
SW1	SW2	SW3	TRANSIMPEDANCE R
VDD	VDD	VDD	20 MΩ - <b>stage 1</b>
GND	VDD	VDD	10 MΩ - stage 2
GND	VDD	GND	5 MΩ – <b>stage 3</b>
VDD	GND	VDD	2 MΩ – <b>stage 4</b>
GND	GND	VDD	1 M $\Omega$ – stage 5
VDD	GND	GND	500 kΩ – <b>stage 6</b>
VDD	VDD	GND	100 kΩ – <b>stage 7</b>
GND	GND	GND	25 kΩ <sup>b</sup> – <b>stage 8</b>

<sup>b</sup>) default by pull down

### 2.3 Switchable Frequency Rrange

Table 3: Switchable Frequency Rra	าตค

SETTINGS OF DIGITAL INPUT	
SW4	ALLOWED CAPACITANCE OF PHOTO-SENSOR
VDD	< 5 pF
GND	< 80 pF <sup>c</sup>

<sup>c</sup>) default by pull down

#### 2.4 Power Down Mode

Table 4: Power Down Mode							
SETTINGS OF DIGITAL INPUT							
PD	BIAS CURRENT OF THE IC						
VDD	< 8 µA						
GND	typical <sup>d</sup>						

<sup>d</sup>) default by pull down

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#### **3 DESCRIPTION OF FUNCTION**

The AS89000-devices are programmable gain transimpedance amplifiers<sup>1</sup> with different numbers of channels (AS89000 – 4 channels). There is one transimpedance amplifier per channel between a current input IIN<X> and a voltage output<sup>2</sup> VOUT<X>. Its transimpedance is selectable in 8 stages. This adjustment can be effected by setting of digital inputs SW1, SW3 and SW4 and is valid for all channels simultaneously (chapter 2.2).

Also simultaneously valid for all channels is a compensation of the input capacitance of photosensors for two possible frequency ranges (switchable by SW4, chapter 2.3).

The pins SW1, SW2, SW3 and SW4 are pull down inputs.

The second input of all transimpedance amplifiers is used for a *common* supply by a reference voltage necessarily fed in through the pin VREF.

All channels are compensated for an external input capacitance of the photo-sensor of smaller than 80 pF (SW4 = GND). The power supply for the AS89000-devices is typical 3 V to 5 V between VDD and GND.

The power down mode is adjusted by PD = VDD and switches off the functionality. In that case it must be pointed out that the transimpedance resistor of stage 8 is between the particular inputs and outputs. The amplifiers are switched off (tri-state).

#### 4 ELECTRICAL CHARACTERISTICS

#### 4.1 Maximum Conditions

Violations of absolute maximum conditions are not allowed under any circumstances, otherwise the IC can be destroyed.

PARAMETER	NAME	MIN	МАХ	UNIT
power supply	VDD	0.3	7.0	V
input and output voltages	$\Rightarrow$ IC-pinning	0.3	VDD+0.3	V
power dissipation	Рор		0.025	w
operating temperature	T <sub>OP</sub>	-40	125	°C
storage temperature	T <sub>STG</sub>	-55	155	°C
weight	m		0,08	g

All voltages are referenced to GND = 0 V.

#### 4.2 Operating Conditions

All voltages are referenced to GND = 0 V.

Table 5: Operating Conditions

PARAMETER	NAME	MIN	ТҮР	ΜΑΧ	UNIT	CONDITIO N
supply voltage	VDD	2.7	3 to 5	5.5	V	
bias current AS89000	I(VDD)		2.5	4.0	mA	27°C, VDD=5.5 V

<sup>1</sup> work as inverted amplifiers

 $^{2}$  V<sub>OUT</sub> = V<sub>REF</sub> - I<sub>In</sub> \* R

PARAMETER

		—C	
ТҮР	ΜΑΧ	UNIT	CONDITIO N
	-	-	

						N
bias current AS89000	I(VDD)			8	μA	PD=VDD
operating temperature	T <sub>OP</sub>	-40	27	125	°C	
input high level	$V_{\mathrm{IH}}$	0.7-VDD		VDD+0.3	V	
input low level	V <sub>IL</sub>	-0.3		0.8	V	
reference voltage	VREF	0.4		VDD-0.4	V	

#### 4.3 AC/DC-Characteristics

Unless otherwise specified the data in this table is valid for  $T_{OP}$  = 27°C and VDD = 5 V.

MIN

All voltages are referenced to GND = 0 V.

NAME

Table 6: AC/DC-Characteristics

PARAMETER	NAME	MIN	ΤΥΡ	ΜΑΧ	UNIT	CONDITION
			0.025		μA	stage 1
			0.05		μA	stage 2
			0.1		μA	stage 3
			0.25		μA	stage 4
			0.5		μA	stage 5
			1		μA	stage 6
			5		μA	stage 7
			20		μA	stage 8
		14000	20000	26700	kΩ	stage 1
		7000	10000	13350	kΩ	stage 2
		3500	5000	6700	kΩ	stage 3
		1400	2000	2670	kΩ	stage 4
		700	1000	1335	kΩ	stage 5
		350	500	670	kΩ	stage 6
		70	100	133	kΩ	stage 7
		17	25	34	kΩ	stage 8
		4	6	16	kHz	stage 1, T <sub>OP</sub> (4.2)
		7	11	28	kHz	stage 2, T <sub>OP</sub> (4.2)
		11	16	42	kHz	stage 3, T <sub>OP</sub> (4.2)
		18	26	66	kHz	stage 4, $T_{OP}$ (4.2)
		25	35	95	kHz	stage 5, T <sub>OP</sub> (4.2)
		35	50	130	kHz	stage 6, T <sub>OP</sub> (4.2 )
		80	120	280	kHz	stage 7, T <sub>OP</sub> (4.2 )
		160	300	580	kHz	stage 8, T <sub>OP</sub> (4.2)
		4	6	16	kHz	stage 1, T <sub>OP</sub> (4.2 )
		7	11	28	kHz	stage 2, T <sub>OP</sub> (4.2 )

#### AS89000

#### V3.01

PARAMETER	NAME	MIN	ΤΥΡ	ΜΑΧ	UNIT	CONDITION
signal frequency at input SW4 = VDD	f <sub>3dB</sub>	14	21	45	kHz	stage 3, T <sub>OP</sub> (4.2)
		35	54	130	kHz	stage 4, T <sub>OP</sub> (4.2 )
		70	110	260	kHz	stage 5, T <sub>OP</sub> (4.2 )
(C <sub>PHOTO-SESNOR</sub> < 5pF)		100	160	360	kHz	stage 6, T <sub>OP</sub> (4.2 )
		260	380	780	kHz	stage 7, T <sub>OP</sub> (4.2 )
		500	800	1700	kHz	stage 8, T <sub>OP</sub> (4.2)
temperature coefficient of the feedback resistor <sup>3</sup>	TC <sub>R</sub>		-3300		ppm/K	
offset voltage	V <sub>OFF</sub> <sup>4</sup>	-10		10	mV	T <sub>OP</sub> (4.2)
capacitive load at VOUT <x></x>	C <sub>LOAD</sub>			50	pF	$I_{LOAD}$ < 0.5 mA per output
pull down current SW1, SW2, SW3, SW4, PD	I <sub>PDPAD</sub>			200	μA	digital inputs
input capacitance of external connected photo-sensors	CPHOTO- SENSOR			80	pF	per input SW4 = GND
input capacitance of external connected photo-sensors	CPHOTO- SENSOR			5	pF	per input SW4 = VDD
tolerance of the feedback resistors between the four channels	TOL <sub>R</sub> <sup>5</sup>	1		10	%	DC input current; for all stages

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 $<sup>^{\</sup>scriptscriptstyle 3}$  see also chapter 6.2

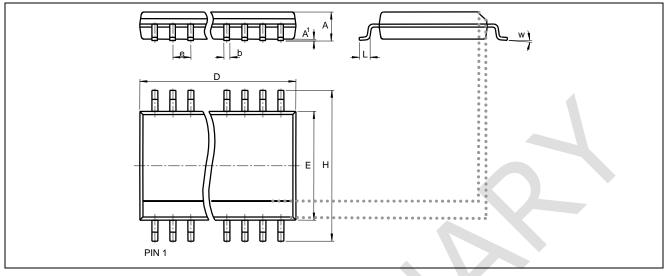
 $<sup>^4</sup>$  V\_{OFF} = VOUT<X> - VREF; results from input offset voltage and input leakage current

<sup>&</sup>lt;sup>5</sup> up to max. 1% available on request

#### **5 PACKAGES**

#### 5.1 Shape & Dimensions

Figure 2: Shape & Dimensions



#### 1) tapered edge

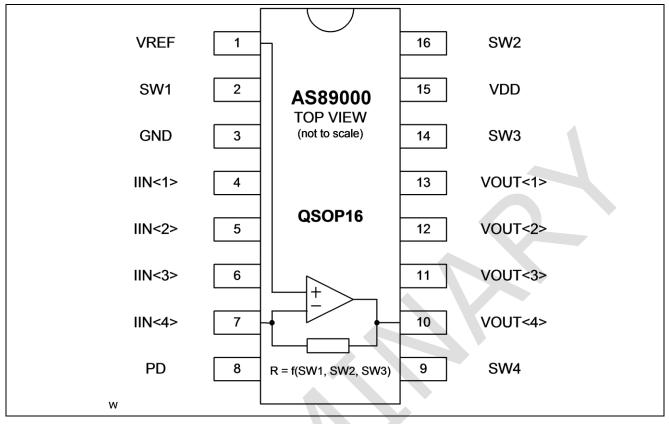
As shown in the figure PIN 1 is located on the bottom of the left corner of the outline.

Table 7: dimensions - mm

ТҮР	PACKAGE	D	E	н	Α	A1	e	b	L	w
AS89000	QSOP16	4.90	3.80	6.00	1.75	0.15	0.635	0.38	0.72	4°

### 5.2 Pin Configuration

Figure 3: Pin Configuration



V3.01

#### 5.3 Soldering Information

The solder reflow profile should fulfil the specifications for the reflow profile parameters given in Table 8. These parameters follow the IPC/JEDEC standard J-STD-020D.1. The temperature should be measure at the top of the package.

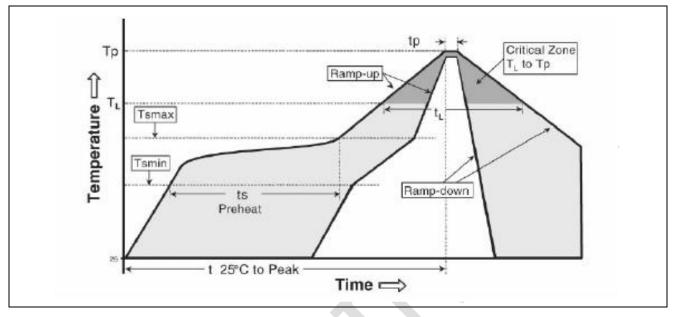


Figure 4: Recommended reflow profile

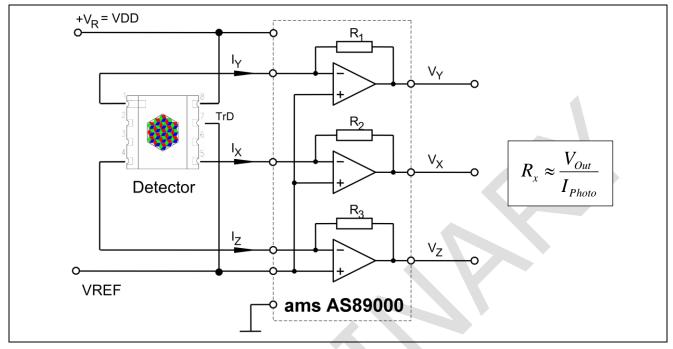
PROFILE PARAMETER	ASSEMBLY, CONVECTION
ramp-up rate (Tsmax to Tp)	2-3°C/second
preheat temperature (Tsmin to Tsmax)	150°C to 200°C
preheat time (ts)	60 – 120 seconds
time above T <sub>L</sub> , 217°C ( $t_L$ )	60 – 150 seconds
peak temperature (Tp)	260°C
time within 5°C of peak temperature (tp)	20 – 40 seconds
ramp-down rate	6°C/second
time 25°C to peak temperature	8 minutes max.

Table 8: Reflow profile parameters

### **6** APPLICATIONS

#### 6.1 Connection of ams Sensors Germany Color Sensor

Figure 5: Circuit for the conversion of sensor's photo current to an equivalent voltage by using the amplifier AS89000



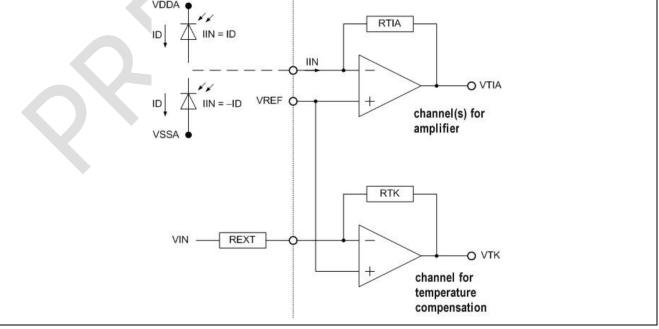
Opposite figure shows a circuit for the conversion of sensor's photo current to an equivalent voltage by using the amplifier AS89000. The resulted voltage can be processed e.g. with an ADC. By the selection of suitable resistors/amplifying stage the output voltage range can be adjusted to the photo current value by programming the pin-programmable transimpedance amplifier AS89000.

#### 6.2 Temperature Compensation of AS89000 via Reference Method

The following description shows a possible approach for reduction the temperature dependency of amplifier via reference channel (use the 4<sup>th</sup> channel of AS89000).

VDDA RTIA IIN = IDID IIN

Figure 6: Possible approach for reduction the temperature dependency of amplifier via reference channel



AS89000

V3.01

The input of the reference channel is connected with an external resistor that will load with an input voltage which is different to VREF.

The output voltage of the measuring channel is explained in the coming formula:

(1) 
$$VTIA(T) = VREF(T) - IIN * RTIA(T)$$

IIN is the input current, which is supplied by the external sensor. The output voltage of the channel for the temperature compensation is defined:

(2) 
$$VTK(T) = VREF(T) - \frac{VIN(T) - VREF(T)}{REXT(T)} * RTK(T)$$

The following voltages will calculate for temperature compensation with a resistor.

(3) 
$$\Delta VTIA(T) = VREF(T) - VTIA(T)$$
  
(4)  $\Delta VTK(T) = VREF(T) - VTK(T)$ 

For example the voltage  $\Delta VTK(T0)$  will detect during the initialization of the system. The value is equivalent to a constant for the temperature T0, which prevailed at the time of initialization. All further measurements will calibrate by this value.

(5) 
$$\Delta VTIAkorrigiert(T) = \Delta VTIA(T) * \frac{\Delta VTK(T0)}{\Delta VTK(T)}$$

All variables of the channel for temperature compensation are affected by temperature effects. Therefore there is an additional coefficient necessary. That coefficient should be highly reduced opposite to the named above value of the RTIA (typical -3300 ppm/K).

(6) 
$$TK = TK(REXT) - \frac{VIN}{VIN - VREF} * TK(VIN) + \frac{VREF}{VIN - VREF} * TK(VREF)$$

"TK(REXT)" is the temperature coefficient of the external resistor, "TK(VIN)" is the temperature coefficient of the input voltage and "TK(VREF)" is the temperature coefficient of the reference voltage.

Please consider the following interrelationship by the choice of resistors REXT and RTK in term of the selected voltages VIN and VREF (values from (2) and (4)).

(7) 
$$\frac{REXT}{RTK} > \left| \frac{VIN}{VREF} - 1 \right|$$

The adherence of this non-equation ensures, that the voltage VTK is located in the working range. That means the amplifier of the channel for temperature compensation doesn't go into saturation.

Furthermore you can calculate the absolute value of the transimpedance resistor RTK for a certain actual existing temperature.

(8) 
$$RTK(T) = REXT(T) * \frac{VREF(T) - VTK(T)}{VIN(T) - VREF(T)}$$

#### 6.3 Output Signals VOUT

AS89000 works by the principle of a connected op-amp:

 $V_{OUT} = V_{REF} - I_{In} * R \quad \{\text{limited by GROUND ...VREF}\}$  $I_{IN} = 0 \quad \Rightarrow V_{OUT} = V_{REF}$  $I_{IN} = max. \quad \Rightarrow V_{OUT} = 0$ 



#### **ORDERING INFORMATION**

NAME	STATUS	PACKAGE	ARTICLE
AS89000	Series	QSOP16	305100002

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