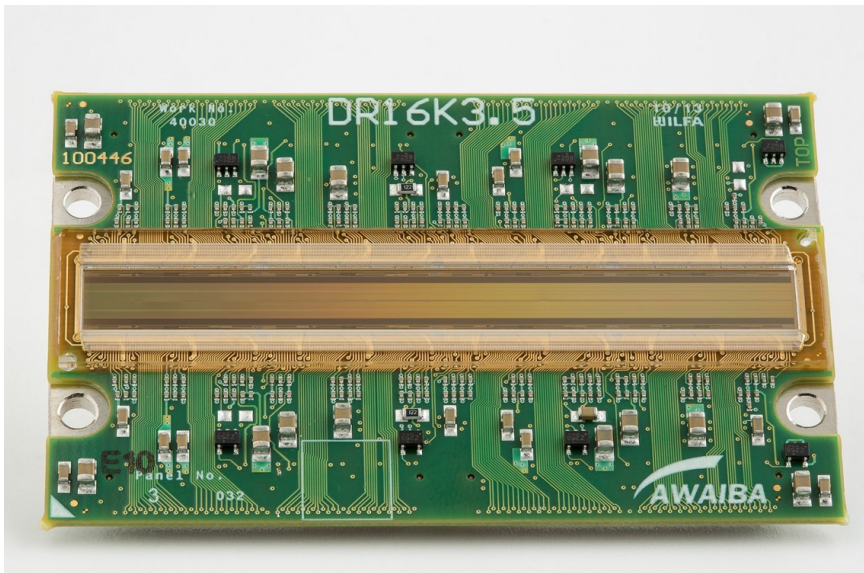


DRAGSTER



Revision History:

| <i>Version</i> | <i>Date</i> | <i>Modifications</i> | <i>Author</i> |
|----------------|-------------|---------------------------------|-----------------|
| 3.2.2 | 09/09/15 | Updated Document | Fátima Baptista |
| 3.2.3 | 04/05/16 | Update LCC Drawings | José Félix |
| 3.2.4 | 13/05/16 | Updated pinout | Fátima Baptista |
| 3.2.5 | 29/06/16 | Updated table 6 | Fátima Baptista |
| 3.2.6 | 01/08/16 | Updated Spectral Response graph | José Félix |
| 3.2.7 | 12/08/16 | Updated package information | Fátima Baptista |
| 3.2.8 | 06/06/17 | Updated section 12 | Fátima Baptista |

Table of Contents

| | |
|---|----|
| 1 Introduction..... | 8 |
| 2 Disclaimer..... | 10 |
| 3 General Statements and Conventions..... | 11 |
| 3.1 Tolerances..... | 11 |
| 3.2 Power supply..... | 11 |
| 3.3 Clock specification..... | 11 |
| 3.4 Digital numbers..... | 11 |
| 3.5 Metric units..... | 11 |
| 4 Block Diagram..... | 12 |
| 5 External Components..... | 14 |
| 6 Electrical Description..... | 18 |
| 6.1 Absolute Maximum Ratings..... | 18 |
| 6.2 Electrical overstress immunity..... | 19 |
| 6.3 Latch-up immunity..... | 19 |
| 6.4 “Power ON” Sequence..... | 19 |
| 6.5 Operating Conditions..... | 20 |
| 6.6 Electrical characteristics..... | 21 |
| 6.7 Optical characteristics DR-2k-7, DR-4k-7, DR-6k-7, DR-8k-7..... | 23 |
| 6.8 Optical characteristics DR-2x2k-7, DR-2x4k-7, DR-2x8k-7..... | 25 |
| 6.9 Optical characteristics DR-4k-3.5, DR-8k-3.5, DR-16k-3.5..... | 27 |
| 6.10 Dragster Relative Spectral Response..... | 29 |
| 6.10.1 Filter transmission for RGB Bayer pattern sensor versions..... | 30 |
| 6.10.2 Color filter arrangement for RGB Dragster versions..... | 30 |
| 6.11 Placement of pixels DR-Xk-7..... | 31 |
| 6.11.1 Test & special pixels DR-Xk-7..... | 31 |
| 6.12 Placement of pixels DR-Xk-3.5..... | 32 |
| 6.12.1 Test & special pixels DR-Xk-3.5..... | 32 |
| 7 Functional Description..... | 33 |
| 7.1 General sensor description..... | 33 |
| 7.1.1 Functional description Dragster Pixel..... | 35 |
| 7.1.1.1 Anti Blooming circuitry..... | 36 |
| 7.1.1.2 Anti corona circuitry..... | 37 |
| 7.1.1.3 Analogue Gain..... | 37 |
| 7.1.1.4 CDS reference generation..... | 37 |
| 7.1.1.5 Pixel Level ADC..... | 38 |

| | |
|---|----|
| 7.1.1.6 Digital Readout concept..... | 42 |
| 7.2 Configuration Bit Overview..... | 43 |
| 7.3 Register definition..... | 45 |
| 7.3.1 CONTROL register 1..... | 45 |
| 7.3.2 CONTROL register 2..... | 46 |
| 7.3.3 Inversed ADC Gain Register..... | 47 |
| 7.3.4 Offset register..... | 48 |
| 7.3.5 CONTROL register 3..... | 48 |
| 7.3.6 Threshold register 1..... | 49 |
| 7.3.7 Threshold register 2..... | 50 |
| 7.3.8 Threshold register 3..... | 50 |
| 7.3.9 End of Range register..... | 50 |
| 7.3.10 Test Multiplexer register..... | 51 |
| 7.4 Serial 4 wire configuration interface..... | 53 |
| 7.4.1 Writing Operation..... | 53 |
| 7.4.2 Reading Operation..... | 54 |
| 7.5 Timing diagrams | 55 |
| 8 Pins and functionality..... | 58 |
| 9 Tap organization | 59 |
| 9.1.1 Tap organization DR-2k-7, DR-4k-7, DR-8k-7..... | 59 |
| 9.1.2 Tap organization DR-6k-7..... | 60 |
| 9.1.3 Tap organization DR-4k-3.5, DR-8k-3.5, DR-16k-3.5..... | 61 |
| 9.1.4 Tap organization DR-2x2k-7, DR-2x4k-7, DR-2x8k-7..... | 62 |
| 9.1.5 Tap organization DR-2x2k-7-RGB, DR-2x4k-7-RGB, DR-2x8k-7-RGB..... | 63 |
| 10 Packages overview..... | 64 |
| 11 Mechanical Drawings..... | 67 |
| 11.1 LCC Package drawings DR2k-7..... | 67 |
| 11.2 LCC package drawings DR2x2k-7, DR4k-3.5..... | 68 |
| 11.3 Invar package drawing DR4k-7 | 69 |
| 11.4 Invar package drawing DR-2x4k-7, DR8k-3.5..... | 70 |
| 11.5 Invar package drawing DR2k-7, DR2x2k-7, DR4k-3.5..... | 71 |
| 11.6 Invar package drawing DR6k-7..... | 72 |
| 11.7 Invar package drawing DR8k-7..... | 73 |
| 11.8 Invar package drawing DR-2x8k-7, DR-16k-3.5..... | 74 |
| 12 Connectors pin outlined..... | 75 |
| 12.1 Pinout DR2k-7-LCC, DR2x2k-7-LCC, DR4k-3.5-LCC..... | 75 |

| | |
|---|----|
| 12.2 Connectors for different versions of Invar headboard packages..... | 78 |
| 12.2.1 Connector number identification and pin numbers..... | 79 |
| | 79 |
| 12.3 Connector signal assignment for Invar head board DR-2x2k-7-Invar, DR-4k-3.5-Invar, DR-2k-7-Invar..... | 80 |
| 12.3.1 Connector 1 | 80 |
| 12.3.2 Connector 2 | 83 |
| 12.4 Connector signal assignment for Invar head board variations DR-4k-7, DR-8k-7, DR-8k-3.5, DR-16k-3.5, DR-2x4k-7, DR-2x8k-7..... | 86 |
| 12.4.1 Connector 1 | 86 |
| 12.4.2 Connector 2 | 89 |
| 12.4.3 Connector 3 | 92 |
| 12.4.4 Connector 4 | 95 |
| 12.5 Connector signal assignment for Invar head board DR-6K-7..... | 98 |

Index of Tables

| | |
|---|----|
| Table 1: Recommended values for capacitors and inductances..... | 15 |
| Table 2: Optional external components..... | 16 |
| Table 3: Absolute maximum ratings | 18 |
| Table 4: Operating conditions..... | 20 |
| Table 5: Electrical characteristics..... | 21 |
| Table 6: Power consumption for Dragster Invar package | 22 |
| Table 7: Power consumption for Dragster LCC package..... | 22 |
| Table 8: Optical characteristics for DR-2k-7, DR-4k-7, DR-6k-7, DR-8k-7 | 23 |
| Table 9: Optical Characteristics for DR-2x2k-7, DR-2x4k-7, DR2x8k-7..... | 26 |
| Table 10: Optical characteristics DR-4k-3.5, DR-8k-3.5, DR-16k-3.5..... | 27 |
| Table 11: Test multiplexer channels..... | 52 |
| Table 12: Pins and functionality..... | 58 |
| Table 13: Package overview..... | 66 |
| Table 14: Connectors for different chip versions..... | 78 |

Index of Figures

| | |
|--|----|
| Fig 1: Block diagram of a Dragster Element..... | 13 |
| Fig 2: Recommended power supply strategy for the sensor head board. *The component DAC1 is optional..... | 14 |
| Fig 3: External components for the option to control the ADC offset by an external DAC for the case of a sensor with 4 segments..... | 16 |
| Fig 4: Equivalent load scheme for use of external DAC..... | 17 |
| Fig 5: Dragster Relative Spectral Response measured according EMVA1288..... | 29 |
| Fig 6: Spectral transmission of colour filters..... | 30 |
| Fig 7: Color filter arrangement on Dragster dual line sensors..... | 30 |
| Fig 8: Placement of pixels sensors with 7µm pixel pitch..... | 31 |
| Fig 9: Placement of pixels sensor variations with 3.5µm pixel pitch..... | 32 |
| Fig 10: Interconnection of ADC reference voltages in case of 7µm pixel pitch sensors with multiple segments..... | 33 |
| Fig 11: Interconnection of ADC reference voltages in case of 3.5µm pixel pitch sensors with multiple segments..... | 34 |
| Fig 12: Overview of pipelined integration ADC and readout sequence..... | 35 |
| Fig 13: Overview of the functional blocks for the analogue part of the pixel..... | 36 |
| Fig 14: Functional block diagram of the pixel level ADC..... | 38 |
| Fig 15: ADC transfer function in linear mode and registers defining the ADC parameters..... | 39 |
| Fig 16: ADC transfer function in companding mode..... | 40 |
| Fig 17: Adaptation of the ADC conversion step in companding ADC mode..... | 41 |
| Fig 18: Writing operation..... | 53 |
| Fig 19: Reading operation..... | 54 |
| Fig 20: Timing diagram..... | 55 |
| Fig 21: Timing diagram..... | 56 |
| Fig 22: Detail end of integration start ADC and readout..... | 57 |
| Fig 23: Tap organization DR-2k-7, DR-4k-7, DR-8k-7..... | 59 |
| Fig 24: Tap organization DR-6k-7..... | 60 |
| Fig 25: Tap organization DR-4k-3.5, DR-8k-3.5, DR-16k-3.5..... | 61 |
| Fig 26: Tap organization DR-2x2k-7, DR-2x4k-7, DR-2x8k-7..... | 62 |
| Fig 27: Tag organization DR-2x2k-7-RGB, DR-2x4k-7-RGB, DR-2x8k-7-RGB..... | 63 |
| Fig 28: Four Views of LCC Package Drawings for DR2k-7 | 67 |
| Fig 29: Four Views of LCC Package Drawings for DR2x2k-7 B&W and RGB, DR4k-3.5..... | 68 |
| Fig 30: Top view DR-B&W-4k-7-Invar. If not otherwise noted all tolerances are +/- 0.1mm..... | 69 |
| Fig 31: DR-B&W-4k-7-Invar. Tolerance +/- 0.1mm..... | 69 |
| Fig 32: Top view DR-B&W-2x4k-7-Invar and DR-B&W-8K-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm..... | 70 |
| Fig 33: DR-B&W-2x4k-7-Invar, DR-B&W-8K-3.5-Invar. Tolerance +/- 0.1mm..... | 70 |

Fig 34: Top view DR-B&W-2k-7-Invar, DR-B&W-2x2k-7-Invar, DR-B&W-4k-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm.....71

Fig 35: DR-B&W-2k-7-Invar, DR-B&W-2x2k-7-Invar, DR-B&W-4k-3.5-Invar.. Tolerance +/- 0.1mm.....71

Fig 36: Top view DR-B&W-6k-7-Invar. If not otherwise noted all tolerances are +/- 0.1mm.....72

Fig 37: DR-B&W-6k-7-Invar. Tolerance +/- 0.1mm.....72

Fig 38: Top view DR-B&W-8k-7-Invar. If not otherwise noted all tolerances are +/- 0.1mm.....73

Fig 39: DR-B&W-8k-7-Invar. Tolerance +/- 0.1mm.....73

Fig 40: Top view DR-B&W-2x8k-7-Invar and DR-B&W-16k-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm.....74

Fig 41: DR-B&W-2x8k-7-Invar, DR-B&W-16k-3.5-Invar. Tolerance +/- 0.1mm.....74

Fig 42: Identification of connector number and pin numbers, DR-16K-3.5 back view79

1 Introduction

DRAGSTER is a platform of a digital line-scan sensors. The sensor family is made using three types of basic elements: a single line element with 2048 pixel resolution and 7 μ m pixel size and pitch, a dual line element with 2048 pixel resolution and 7 μ m pixel size and pitch and a 4096 pixels element with 3.5 μ m pixel size and pitch. Any of the following types can be made, where “1x” means single line and “2x” means dual line:

| Line | Resolution |
|------|------------|
| 1x | 2K |
| | 4K |
| | 6K |
| | 8K |
| | 16K |
| 2x | 2K |
| | 4K |
| | 8K |

The chip versions with dual line are optionally available with Bayer Pattern RGB filters placed on the sensors.

For all variations the basic readout and control electronics are identical. Other different variations of pixel aspect ratios can be implemented, please contact AWAIBA if you require customized resolution sensors based on Dragster architecture.

The current specification covers the following device variations:

| Part Number | Number of pixels | Pixel size | Package Type |
|---------------------|------------------|---------------------------|--------------|
| DR-B&W-2K-7-LCC | 1x2048 | 7 μ m x 7 μ m | LCC |
| DR-B&W-2K-7-Invar | 1x2048 | 7 μ m x 7 μ m | Invar module |
| DR-B&W-4K-3.5-LCC | 1x4096 | 3.5 μ m x 3.5 μ m | LCC |
| DR-B&W-4K-3.5-Invar | 1x4096 | 3.5 μ m x 3.5 μ m | Invar module |
| DR-B&W-4K-7-Invar | 1x4096 | 7 μ m x 7 μ m | Invar module |
| DR-B&W-6K-7-Invar | 1x6175 | 7 μ m x 7 μ m | Invar module |
| DR-B&W-8K-3.5-Invar | 1x8192 | 3.5 μ m x 3.5 μ m | Invar module |
| DR-B&W-8K-7-Invar | 1x8192 | 7 μ m x 7 μ m | Invar module |

| | | | |
|-----------------------|---------|---------------|--------------|
| DR-B&W-16K-3.5-Invar | 1x16384 | 3.5µm x 3.5µm | Invar module |
| DR-B&W-2x2K-7-LCC | 2x2048 | 7µm x 7µm | LCC |
| DR-RGB-2x2K-7-LCC | | | |
| DR-B&W-2x2K-7-Invar | 2x2048 | 7µm x 7µm | Invar module |
| DR-RGB-2x2K-7-Invar | | | |
| DR-B&W-2x4K-7-Invar | 2x4096 | 7µm x 7µm | Invar module |
| DR-RGB-2x4K-7-Invar | | | |
| DR-B&W-2x8K-7-Invar** | 2x8192 | 7µm x 7µm | Invar module |
| DR-RGB-2x8K-7-Invar** | | | |

** sales restrictions may apply to some markets

2 Disclaimer

The Integrated Circuit (IC) has been or will be designed and developed so as to conform in all material respects to the preceding introduced specification based on the performance indication and guideline from the silicon manufacturer regarding the target CMOS technology. Any change to the specification shall be mutually consulted and determined with the prior written consent of the parties. Any changes to the specifications required by the Customer shall be mutually agreed upon and laid down in writing as a supplement to or correction of the specifications.

AWAIBA does not warrant and Customer therefore expressly waives the existence of any parameters or features of the IC, which are not explicitly mentioned in the specification. It is the customer's responsibility and obligation to check compliance of the IC to the requirements of the application. The IC will not be designed for use as critical¹ component in medical, military or live sustaining ² applications. Any use of the IC without prior written consent of AWAIBA in such applications is prohibited.

The above mentioned warranty is the only warranty given by AWAIBA. AWAIBA expressly disclaims all other warranties, whether expressed, implied, or statutory, including, without limitation, any implied or statutory warranties of merchantability, fitness for a particular purpose, and non-infringement, and any warranty that may arise by reason of usage of trade, custom or course of dealing, and customer hereby expressly waives any such warranties.

1) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

2) Life support devices, systems or applications are devices, systems or applications which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided, can be reasonably expected to result in a significant injury to the user.

3 General Statements and Conventions

Info only

Text in this document between “{ info only:” and “end info}” or “{“ and “}” is for information only. Parameters and information given in this section contain background information . Performance and parameters given in these sections can not be guaranteed. No implicit nor explicit specification can be derived from these sections.

3.1 Tolerances

For all parameters, nominal value, upper, and lower bound of guaranteed specification are indicated. Parameters indicated without tolerances are for info only and can not be guaranteed.

3.2 Power supply

The lowest supply voltage in the chip is referred to as VSS. VSSxx indicates the lowest power supply voltage of a sub block xx of the circuit. All VSS power supply's have the same potential at all pins at any time. 0V is defined as being the voltage applied to the VSS pins.

The highest supply voltage of a sub block xx of the circuit is referred to as VDDxx. All pins carrying identical VDDxx power supply net labels have the same potential at any time, neglecting parasitic effects.

All voltage specifications are referred to VSS unless otherwise specified. All positive currents flow into a pin. The sinking of current means that current is flowing into a pin. The sourcing of current means that current is flowing out of a pin.

3.3 Clock specification

All timing information treated by a digital control part refers to the master clock frequency which is supplied on pin Main clk, unless otherwise specified.

3.4 Digital numbers

When ever referred to the output signal this is indicated in DN (Digital Numbers) equalling 1 unit (1LSB) of the on chip ADC. This quantity is sometimes also referred to as "grey levels".

3.5 Metric units

Unless otherwise indicated all measurements and units follow metric units. Mechanical dimensions are by default given in mm.

4 Block Diagram

The sensor features a low noise pixel with true CDS and global shutter for interleaved readout and integration operation. Each pixel has an on pixel ADC and 13bit readout register. AD conversion is made to 12.2 bits and for output clamped to 12bit to guarantee full 4096 DN signal swing. The ADC gain can be programmed in a range of -6dB till + 20 dB by means of an 8bit DAC controlled over the serial configuration interface.

The readout is made by 2 12bit wide digital taps organized in odd / even order for each 2k segment. (full 13 bit readout is possible for special purposes). For each line segment, all 2k pixels have to be read out.

For sensor versions with 3.5 μ m pixel pitch, two 2k segment readout circuits are placed on each side of the pixel line, to lead to a basic segment of 4k pixels, even pixels read out over the bottom readout, odd pixels read out over the top readout.

Start of integration, end of integration and optional start of readout are started upon individual external trigger events. To enhance dynamic range multiple non destructive readouts are possible.

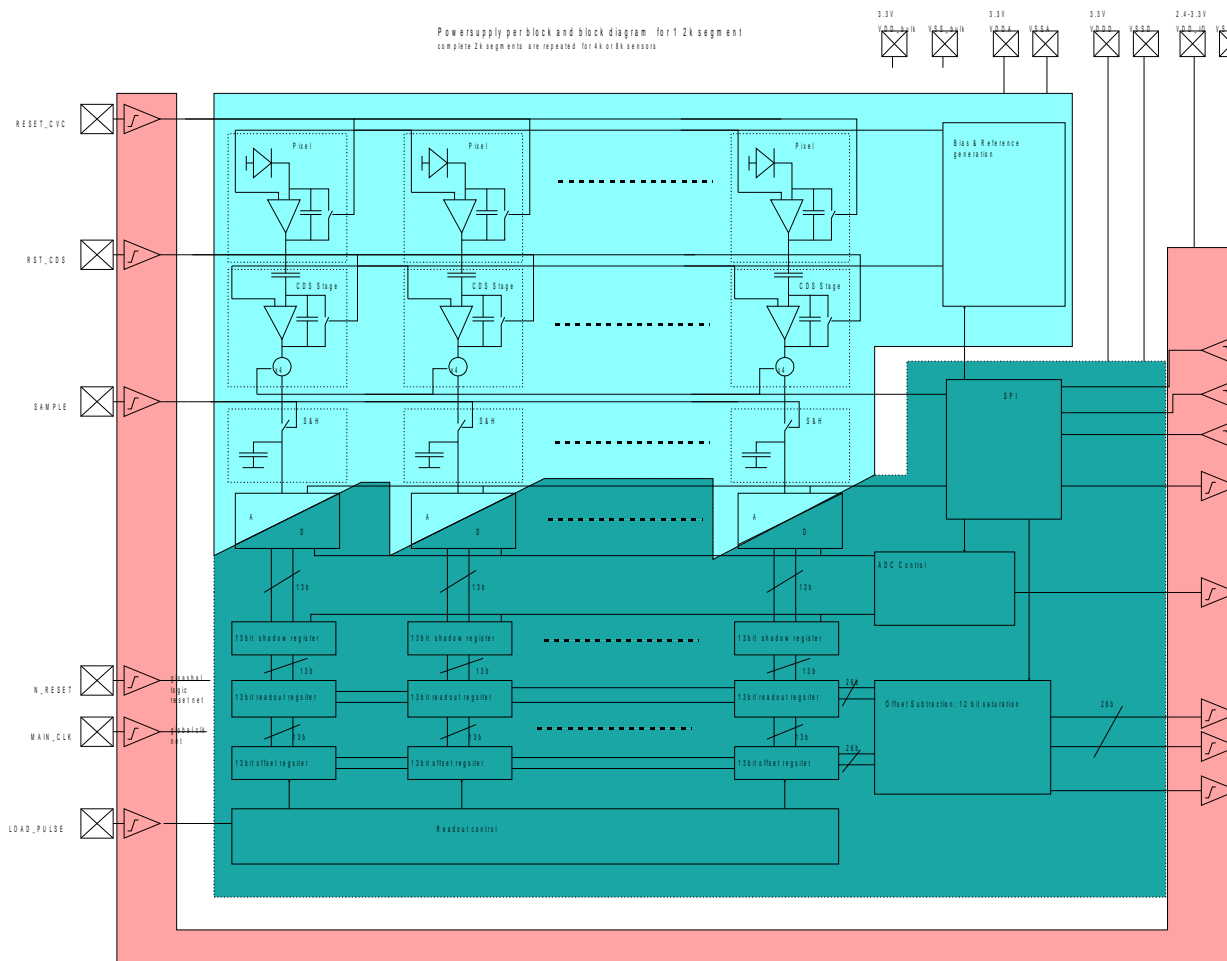


Fig 1: Block diagram of a Dragster Element

5 External Components

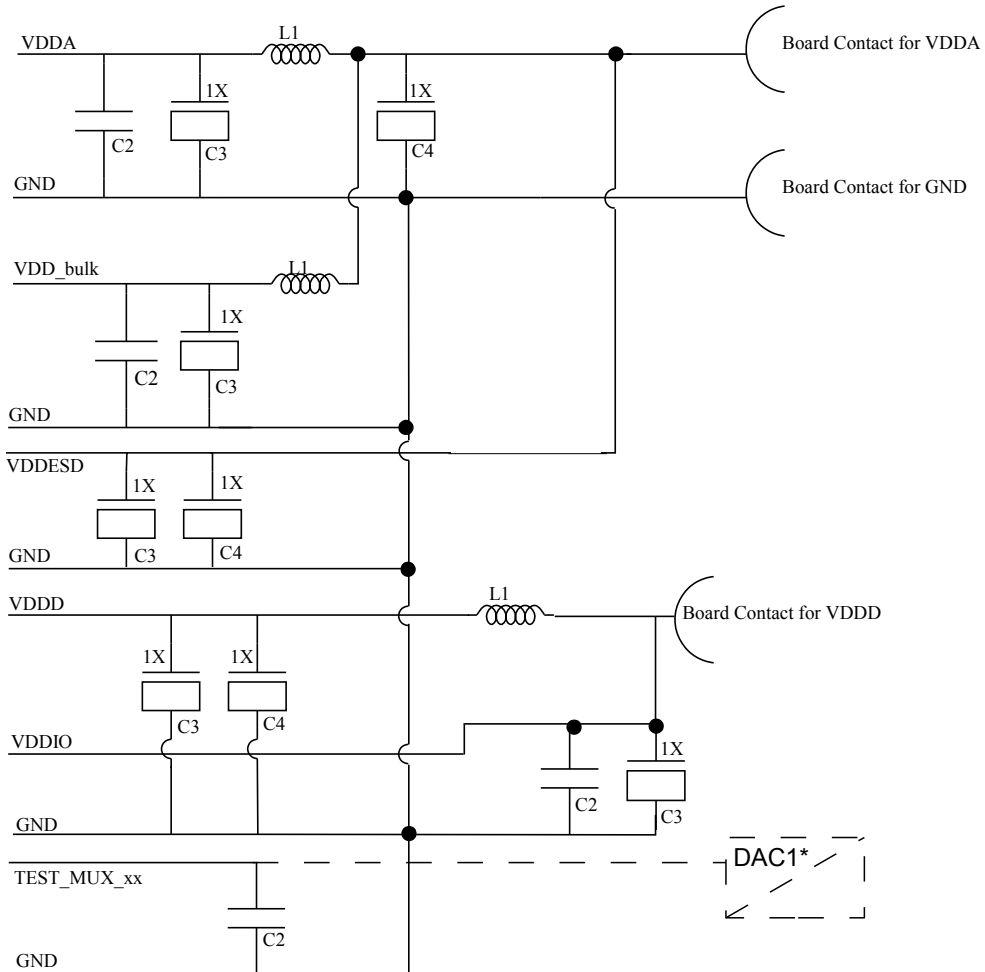


Fig 2: Recommended power supply strategy for the sensor head board. *The component DAC1 is optional

| Component | Description | Nominal value | Tolerance | Voltage range |
|-----------|---|---------------|-----------|--|
| C2 | Power decoupling capacitor, close to each VDDx connector pin low ESR Ceramic | 10nF | +/- 25% | >3.6V |
| C3 | Power decoupling capacitor, placed one time per power supply. Tantal type. | 10uF | +/- 25% | >3.6V |
| C4 | Power decoupling capacitor, placed one time per power supply. Tantal type. | 100uF | +/- 25% | >3.6V |
| L1 | Power decoupling inductance | 10nH | +/- 25% | dimension according power consumption of respective sensor variation |
| C5 | Additional decoupling capacitor on the outputs of TEST_MUX * | 10nF | +/- 25% | >3.6V |

Table 1: Recommended values for capacitors and inductances

* optional additional components 1) If the “TEST_MUX_XX_#” signals are accessible an additional capacitance should be placed in this signal and then by writing Register 0x0A with the value 0x0F the line by line offset noise is reduced significantly.

{ info only:

The external circuit schematic to be used for this solution is shown in Figure 3, where an external DAC is used to set the ADC offset (black reference) in more fine steps and possibly with better temperature stability, though for most applications the external DAC is not necessary. If the “TEST_MUX_XX_#” signals are accessible, an external DAC can be used to directly set the ADC offset. To achieve that the “TEST_MUX_XX_#” outputs should be connected and 0x0F should be written to register 0x0A in all segments. Also, make sure the DAC output impedance is higher than 200KOhm. Such DAC may permit to provide more fine tuning to the pixel black level. On chip there is an 8 bit resolution DAC for this purpose but an external ADC can provide benefit if more fine adjustment steps are required. For sensors with 3.5µm pixel or dual line sensors such DAC has to be provided for top and bottom side separately, though is not mandatory.

Once the individual DAC offset's are equalized over the external connection, the black level can be adjusted by writing the same value to the registers on each segment.

In case of sensors with readout tap's on top and bottom side different values can be written on top and bottom side SPI's in order to equalize the odd even pixels offset, respectively the line offset.

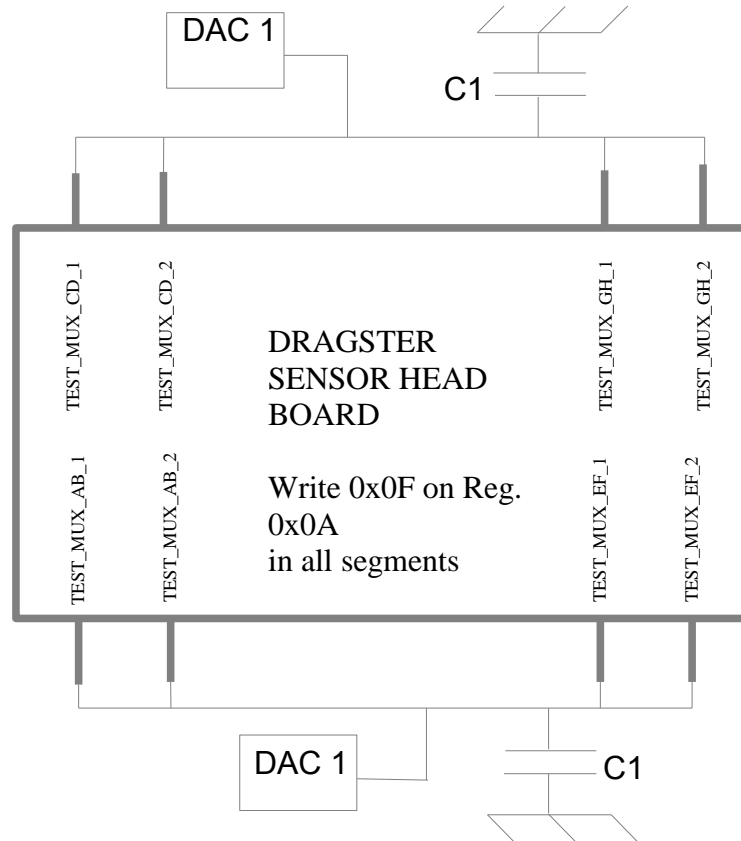


Fig 3: External components for the option to control the ADC offset by an external DAC for the case of a sensor with 4 segments.

| Component | Description | Nominal value | Tolerance | Voltage range |
|-----------|--|----------------------|--|---------------|
| DAC 1 | Optional additional DAC on outputs of TEST_MUX | 1V – 2.5V (or wider) | Output resistance < 1k Ohm Vnoise rms < 0.5mV | >3.6V |

Table 2: Optional external components

In order to adjust the ADC black reference an external reference voltage is supplied via the DAC where lowering the voltages shifts the output signal to higher digital values.

Figure 4 illustrates the equivalent internal circuit when using an external DAC to set the black level reference. The load circuit the DAC sees is in parallel for as many segments are connected to the same DAC.

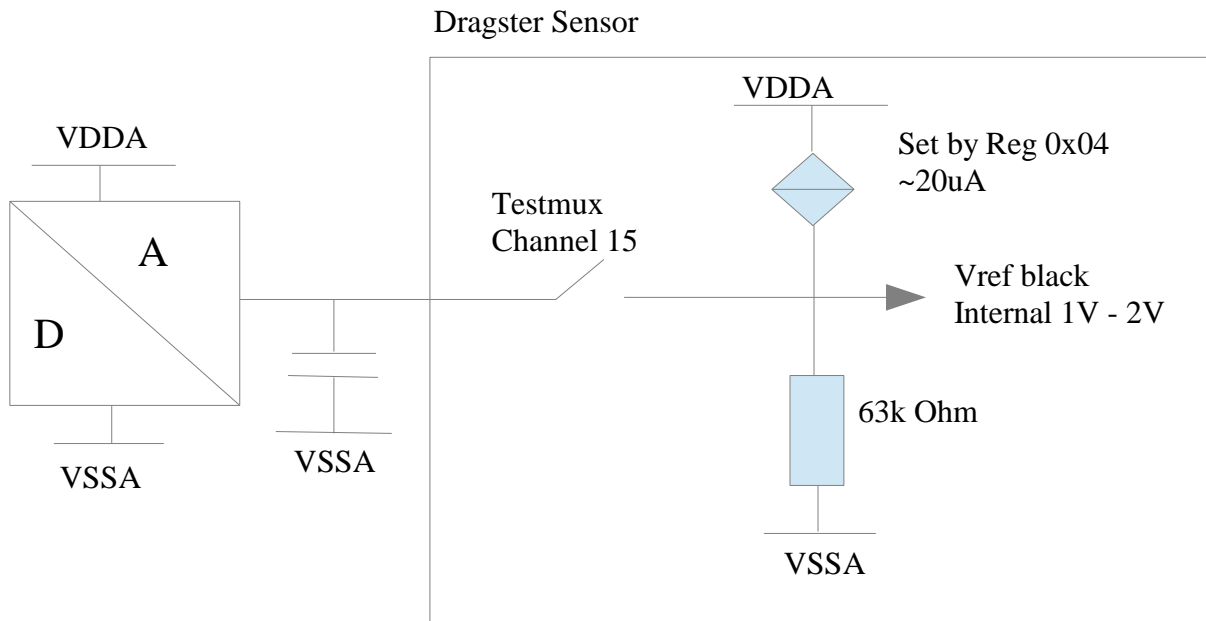


Fig 4: Equivalent load scheme for use of external DAC

: end info }

6 Electrical Description

The sensor will comply to the specifications listed in this section within the operating ranges listed in the respective section.

An applied signal must not have a deviation from the ideal signal, at the pin of the circuit, such that the circuit or the parameter under test are affected significantly.

Proper decoupling of the circuit according to chapter 5 is required. The following section defines the limits of functional operation and parametric characteristics of the circuit, and reliability. Note that functionality of the circuit outside the operating range as specified in this section is not guaranteed.

6.1 Absolute Maximum Ratings

Stresses above those listed in this clause may cause immediate and permanent device failure. Operation outside the operating conditions for extended periods may affect device reliability. It is not implied that more than one of these conditions can be violated simultaneously.

Total cumulative dwell time above the maximum operating rating for temperature must be less than 100 hours.

| Symbol | Description | Min | Max | Unit |
|--------|--|------|----------------------------|------|
| VDD | Power supply voltage (digital) | -0.3 | 3.6 | V |
| VIO | Voltage on any IO | -0.3 | VDDIO +0.3 or 3.6 | V |
| IIO | DC forward BIAS current, input or output | | -24 (source) +24 (sink) | mA |
| Tj | Junction temperature | -55 | 125 | °C |
| Ta | Operating Temperature Range* | 0 | 60 | °C |

Table 3: Absolute maximum ratings

*The Operating Temperature Range is regarding the ambient temperature that is more suitable for a good performance of the sensor. It is considered with no heat dissipation, since it's the environment temperature.

6.2 Electrical overstress immunity

Electrostatic discharges on component level:

The device withstands 1k Volts Human Body Model ESD pulses when tested according to MIL STD 883 method 3015.7

6.3 Latch-up immunity

Static latch-up protection level is 10mA at 25°C when tested according to EIA/JESD78.

6.4 “Power ON” Sequence

To avoid latch up problems that can create faulty operation points, the correct sequential “Power On” sequence for all devices in INVAR headboard package is:

- 1) VDDESD
- 2) VDDA
- 3) VDD_BULK
- 4) VDDD
- 5) VDDIO
- 6) ramp up signals on any inputs
- 7) release N_RESET_XX

If the control over all supplies is not possible, at least care must be taken for the sensor supplies to raise up in the following order:

- 1) VDDESD
- 2) VDD_BULK; VDDA; VDDD; VDDIO
- 3) ramp up signals on any inputs
- 4) release N_RESET_XX

For the LCC package versions, it is important that VDD ramps prior to any digital input signal.

In any condition the two following situations are to be avoided:

Fault A: any VDDx is supplied before VDDESD or to a higher value than VDDESD

Fault B: digital inputs are supplied prior to supply of VDDESD

6.5 Operating Conditions

| Symbol | Description | Min | Typical | Max | Unit |
|-----------------|--|----------------|---------|----------------|--------|
| VDDD | Power supply voltage (digital) | 3.2 | 3.3 | 3.4 | V |
| VDDA | Power supply voltage (analogue) | 3.2 | 3.3 | 3.4 | V |
| VDDES | Power supply voltage ESD | 3.2 | 3.3 | 3.4 | V |
| VDDIO | Power supply voltage IO | 2.4* | 3.3 | 3.4 | V |
| GND | Ground supply | | 0 | | V |
| Fclk | Input Clock Frequency | 1** | | 85*** | MHz |
| Duty clk | Input Clock Duty cycle up to 50MHz | 45 | 55 | 70 | % |
| Duty clk | Input Clock Duty cycle up to >50MHz | 55 | 57 | 65 | % |
| Jitter clk | Input Clock Jitter | | | <5% Tclk | % Tclk |
| Cload | Load capacitance on digital I/O's | | | 10 | pF |
| Tj | Junction temperature | 0 | 27 | +80 | °C |
| VnrmsVDDD | RMS Noise on VDD digital | | | 20 | mV |
| VnppVDDD | Peak to Peak Noise on VDD digital | | | 100 | mV |
| VnrmsVDDA | RMS Noise on VDD analogue | | | 5 | mV |
| VnppVDDA | Peak to Peak Noise on VDD analogue | | | 20 | mV |
| VnrmsVDD/IO | RMS Noise on VDD I/O | | | 20 | mV |
| VnppVDD/IO | Peak to Peak Noise on VDD I/O | | | 100 | mV |
| Vil | Low level input voltage | -0.3 | 0 | 0.4 | V |
| Vih | High level input voltage | 0.8xVD D/IO | VDD/IO | VDD/IO +0.3 | V |
| Tsetup, data in | Setup Time for digital input signals relative to rising edge of Mclk at Mclk pin | 3 | | | ns |
| Thold, data in | Hold Time for digital input signals relative to rising edge of Mclk st Mclk pin | 3 | | | ns |
| Tsetup, MOSI | Setup Time for MOSI input signals relative to rising edge of SCLK | 3 | | | ns |
| Thold, MOSI | Hold Time for MOSI input signals relative to rising edge of SCLK | 5 | | | ns |

Table 4: Operating conditions

* VDDIO < 3.0V is not recommended for pixel_clock speeds above 40MHz and may not meet the slew rate specifications in all cases.

** Fclk can be lower than 1MHz however the ADC conversion accuracy might be reduced.

*** The ADC can be clocked with up to 100MHz for faster conversion when using clock reduction for readout.

6.6 Electrical characteristics

Current consumptions are for one segment of 2k pixels, multiples apply for higher resolution sensors.

| Symbol | Description | Min | Max | Unit |
|------------------|---|------------|------|------|
| V _{ol} | Low level output voltage | | 0.5 | V |
| V _{oh} | High level output voltage | VDD/IO-0.6 | | V |
| I _{il} | Low level input leakage (V _i =0) | | +/-1 | uA |
| I _{ih} | High level input leakage (V _i =VDD/IO) | | +/-1 | uA |
| tslew, rising* | Output slew rate of rising edge | | 5 | ns |
| tslew, falling* | Output slew rate of falling edge | | 5 | ns |
| P _{tot} | Power Consumption per 2k segment | | 400 | mW |
| I (VDDA) | Current to analog devices per 2k segment | | 50 | mA |
| I (VDDD) | Current to Digital devices per 2k segment | | 30 | mA |
| I (VDDIO) | Current for I/O per 2k segment | | 40 | mA |

Table 5: Electrical characteristics

* The output swing on signal pixel_clock (if enabled) may be smaller at pixel clock rates above 60MHz

Resulting maximum current consumption for the different chip variations

| Sensor | I(VDDA) / mA | I(VDDD) / mA | I(VDDIO) / mA * | Ptot /mW ** (total power consumption) |
|-----------------|--------------|--------------|-----------------|--|
| DR-2k-7-Invar | 50 | 30 | 40 | 400 |
| DR-4k-3.5-Invar | 100 | 120 | 80 | 800 |
| DR-2x2k-7-Invar | 100 | 120 | 80 | 800 |
| DR-4k-7 | 100 | 60 | 80 | 800 |
| DR-6k-7 | 220 | 90 | 120 | 1420 |
| DR-8k-7 | 260 | 150 | 160 | 1850 |
| DR-8k-3.5 | 200 | 120 | 160 | 1600 |
| DR-16k-3.5 | 520 | 320 | 160 | 3500 |
| DR-2x4k-7 | 200 | 120 | 160 | 1600 |
| DR-2x8k-7 | 500 | 240 | 320 | 3500 |

Table 6: Power consumption for Dragster Invar package

| Sensor | I(VDDA) / mA | I(VDDD) / mA | Ptot /mW ** (total power consumption) |
|---------------|--------------|--------------|--|
| DR-2k-7-LCC | 75 | 65 | 460 |
| DR-4k-3.5-LCC | 240 | 170 | 920 |
| DR-2x2k-7-LCC | 240 | 170 | 9200 |

Table 7: Power consumption for Dragster LCC package

* @ 10pF

** At VDDIO = 3.3V 46MHz Clod dig 10pF 20% I/O activity

6.7 Optical characteristics DR-2k-7, DR-4k-7, DR-6k-7, DR-8k-7

| Parameter | Min | Typ/ Target | Max | unit |
|---|------|--------------------------------------|----------|--------------------|
| Pixel size | | 7 x 7 | | µm |
| Pixel pitch in x direction | | 7 | | µm |
| Number of dark pixels in most left segment | | 32 | | pixels |
| Fill Factor | | 100 | | % |
| Quantum efficiency at 630nm | 50 | 60 | 70 | % |
| Full Well capacity (4) | 30 | 46 | 65 | ke- |
| Total System Gain K | | 0.076 | | DN/e- |
| DSNU rms (1;5) | | 4 | 10 | DN/12bit |
| Responsivity (1) | | 77 | | DN/nJ/cm2 (@12bit) |
| Responsvity analogue gain 4x (6) | | 310 | | DN/nJ/cm2 (@12bit) |
| PRNU rms (1;5) | | 0.7% | 3% | % (full scale) |
| PRNU pp (1; 5) | | 4% | 8% | % (full scale) |
| ADC Programmable gain | -6 | | 20 | dB |
| ADC gain resolution | | 8 | | bit |
| Blooming overload tolerance | 100x | infinite | | |
| Lag | | 0 | 0.01 | % |
| Crosstalk (optical & electrical) | | 2 | 5 | % |
| Exposure time range | 2 | | infinite | us |
| Temporal noise Dark rms (2)* | | 1.5 | 4 | DN/12bit |
| Dark noise electrons rms (2)* | | 22 | | e- |
| NEE (noise equivalent energy) unity gain (1) | | 0.02 | | nJ/cm2 |
| Temporal noise Dark rms gain 4x (6)* | | 2.9 | 5 | DN/12bit |
| Dark noise electrons rms gain 4x (6)* | | 7 | | e- |
| NEE (noise equivalent energy) analogue gain x4 (6)* | | 0.01 | | nJ/cm2 |
| Non Linearity (3) | | 2 | 5 | % |
| Dark current @27C | | 3 | 50 | e-/ms |
| Maximum Line Rate | | | 80 | kScan/s |
| ADC Resolution | | 12 (13)** | | bit |
| Number of output taps | | 2 per 2k segment | | |
| Configuration Interface (1 interface / 2k segment) | | Serial 4 line | | |
| Integration control | | Asynchronous, with 6 digital signals | | |
| Trigger delay | | | 1 | us |
| Integration & Readout | | Interleaved | | |

Table 8: Optical characteristics for DR-2k-7, DR-4k-7, DR-6k-7, DR-8k-7

- (1) $T_{int}=10\mu s$, Unity gain (CDS_gain = 0 \rightarrow x1; Inverse ADC gain = 0x20h)
- (2) $T=27^{\circ}C$, $T_{int}=20\mu s$, Unity gain (CDS_gain = 0; \rightarrow x1 Inverse ADC gain = 0x20h)
- (3) Measured in % deviation from full scale signal for the signal range of 5% - 95% (according to EMVA1288 proposal for linearity measurement)
- (4) At unity gain (CDS_gain = 0 \rightarrow x1; Inverse ADC gain = 0x20h; end counter 128 (4096 ADC levels))
- (5) Ramp offset and ramp gain must be adjusted for all segments to match with each other.
- (6) $T=27^{\circ}C$, $T_{int}=20\mu s$, Unity gain (CDS_gain = 1; \rightarrow x4 Inverse ADC gain = 0x20h)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}

*** internal ADC resolution is 13bit.

6.8 Optical characteristics DR-2x2k-7, DR-2x4k-7, DR-2x8k-7

| Parameter | Min | Typ/ Target | Max | unit |
|---|------|--------------------------------------|----------|--------------------|
| Pixel size | | 7 x 7 | | µm |
| Pixel pitch in x direction | | 7 | | µm |
| Number of dark pixels in most left segment | | 2x32 | | pixels |
| Fill Factor | | 100 | | % |
| Quantum efficiency at 630nm | 50 | 60 | 70 | % |
| Full Well capacity(4) | 30 | 46 | 65 | ke- |
| Total System Gain K | | 0.076 | | DN/e- |
| DSNU rms (1;5) | | 4 | 10 | DN/12bit |
| Responsivity (1) | | 77 | | DN/nJ/cm2 (@12bit) |
| Responsvity analogue gain 4x (6) | | 310 | | DN/nJ/cm2 (@12bit) |
| PRNU rms (1;5) | | 0.7% | 3% | % (full scale) |
| PRNU pp (1; 5) | | 4% | 8% | % (full scale) |
| ADC Programmable gain | -6 | | 20 | dB |
| ADC gain resolution | | 8 | | bit |
| Blooming overload tolerance | 100x | infinite | | |
| Lag | | 0 | 0.01 | % |
| Crosstalk (optical & electrical) | | 2 | 5 | % |
| Exposure time range | 2 | | infinite | us |
| Temporal noise Dark rms (2)* | | 1.5 | 4 | DN/12bit |
| Dark noise electrons rms (2)* | | 22 | | e- |
| NEE (noise equivalent energy) unity gain (1) | | 0.02 | | nJ/cm2 |
| Temporal noise Dark rms gain 4x (6)* | | 2.9 | 5 | DN/12bit |
| Dark noise electrons rms gain 4x (6)* | | 7 | | e- |
| NEE (noise equivalent energy) analogue gain x4 (6)* | | 0.01 | | nJ/cm2 |
| Non Linearity (3) | | 2 | 5 | % |
| Dark current @ 27C | | 3 | 50 | e-/ms |
| Maximum Line Rate 2:1 TDI mode | | | 80 | kScan/s |
| Maximum Line Rate dual line mode | | | 160 | kScan/s |
| ADC Resolution | | 12 (13)*** | | bit |
| Number of output taps | | 4 for each 2x2k pixels segment | | |
| Configuration Interface (1 interface for each line and each 2k segment) | | Serial 4 line | | |
| Integration control** | | Asynchronous, with 6 digital signals | | |
| Trigger delay | | | 1 | us |
| Integration & Readout | | Interleaved | | |

Table 9: Optical Characteristics for DR-2x2k-7, DR-2x4k-7, DR2x8k-7

- (1) Tint = 10us, Unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h)
- (2) T = 27°C , Tint = 20us, Unity gain (CDS_gain = 0; -> x1 Inverse ADC gain = 0x20h)
- (3) Measured in % deviation from full scale signal for the signal range of 5% - 95% (according to EMVA1288 proposal for linearity measurement)
- (4) At unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h; end counter 128 (4096 ADC levels))
- (5) Ramp offset and ramp gain must be adjusted for all segments to match with each other.
- (6) T=27°C , Tint=20us, Unity gain (CDS_gain = 1; -> x4 Inverse ADC gain = 0x20h)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}

** each line can be triggered individually.

*** internal ADC resolution is 13bit.

6.9 Optical characteristics DR-4k-3.5, DR-8k-3.5, DR-16k-3.5

| Parameter | Min | Typ/ Target | Max | unit |
|---|------|---|----------|-----------------------------------|
| Pixel Size (x,y) | | 3.5x3.5 | | µm ² |
| Pixel Pitch in x direction | | 3.5 | | µm |
| Number of dark & special pixels in most left segment | | 64 | | pixels |
| Fill Factor | | 100 | | % |
| Quantum efficiency at 630nm | 50 | 56 | 70 | % |
| Full Well capacity(4) | 15 | 23 | 35 | ke- |
| DSNU rms (1;5) | | 4 | 10 | DN/12bit |
| Responsivity (1) | | 39 | | DN/nJ/cm ² (@12bit) |
| Responsivity CDS gain 4x (6) | | 155 | | DN/nJ/cm ² (@12bit) |
| PRNU rms (1;5) | | 0.8 | 3 | % (full scale) |
| PRNU pp (1; 5) | | 4 | 10 | % (full scale) |
| ADC Programmable gain | -6 | | 20 | dB |
| ADC gain resolution | | 8 | | bit |
| Blooming overload tolerance | 100x | infinite | | |
| Lag | | 0 | 0.1 | % |
| Crosstalk (optical & electrical) | | 2 | 5 | % |
| Exposure time range | 1 | | infinite | us |
| Temporal noise Dark rms (2)* | | 1.6 | 5 | DN/12bit |
| NEE (noise equivalent energy) unity gain (1) | | 0.04 | | nJ/cm ² |
| Temporal noise Dark rms gain 4x (6)* | | 3.4 | 6 | DN/12bit |
| NEE (noise equivalent energy) analogue gain x4 (6) | | 0.02 | | nJ/cm ² |
| Non Linearity (3) | | 2 | 5 | % |
| Maximum Line Rate | | | 80 | kScan/s |
| ADC Resolution | | 12 (13)** | | bit |
| Number of output taps | | 4per 4k pixel segment | | |
| Configuration Interface (2 Interfaces for each 4k pixel segment) | | Serial 4 line | | |
| Integration control | | Asynchronous, with 4 digital signals | | |
| Trigger delay | | | 1 | us |
| Integration & Readout | | Interleaved | | |

Table 10: Optical characteristics DR-4k-3.5, DR-8k-3.5, DR-16k-3.5

- (1) $T_{int}=10\mu s$, Unity gain ($CDS_gain = 0 \rightarrow x1$; ADC ramp = 29)
- (2) $T=27^{\circ}C$, $T_{int}=20\mu s$, Unity gain ($CDS_gain = 0$; $\rightarrow x1$ ADC ramp = 29)
- (3) Measured in % deviation from full scale signal for the signal range of 5% - 95%
(according to EMVA1288 proposal for linearity measurement)
- (4) At unity gain ($CDS_gain = 0 \rightarrow x1$; ADC ramp = 29; end counter 128 (4096 ADC levels))
- (5) Ramp offset and ramp gain must be adjusted for all segments to match with each other
Placement of pixels
- (6) $T=27^{\circ}C$, $T_{int}=20\mu s$, Unity gain ($CDS_gain = 1$; $\rightarrow x4$ ADC ramp = 29)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}

**internal ADC resolution is 13bit.

6.10 Dragster Relative Spectral Response

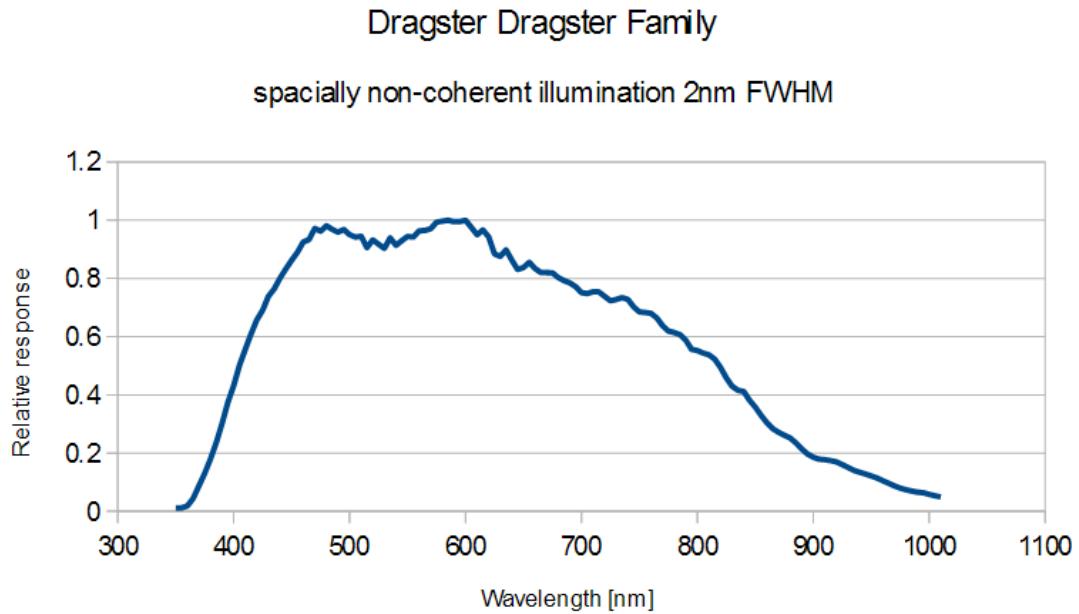


Fig 5: Dragster Relative Spectral Response measured according EMVA1288.

6.10.1 Filter transmission for RGB Bayer pattern sensor versions

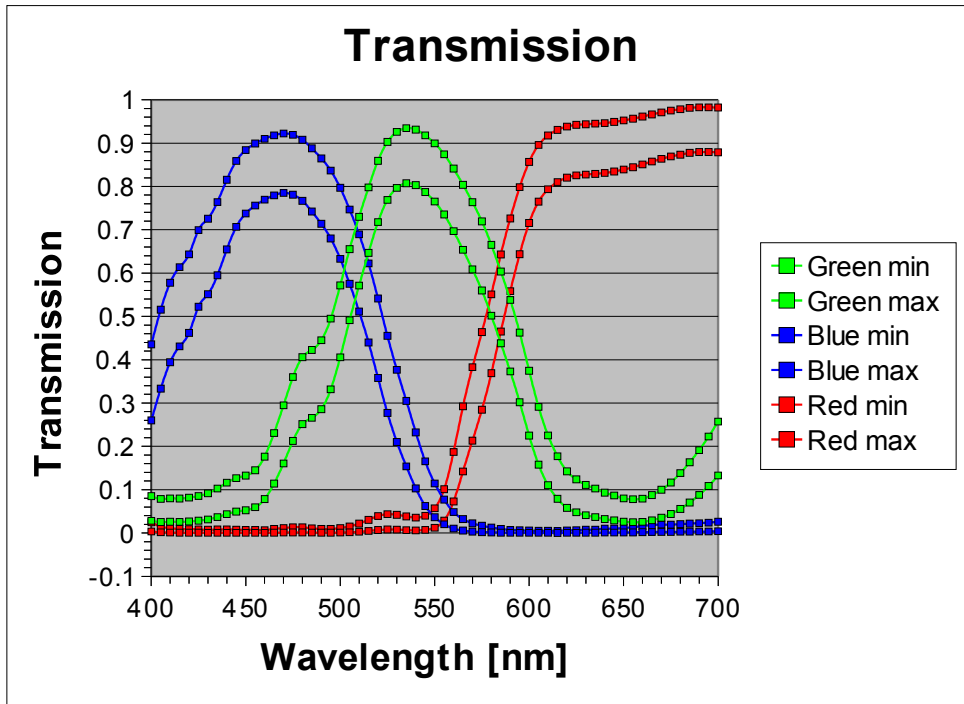


Fig 6: Spectral transmission of colour filters

6.10.2 Color filter arrangement for RGB Dragster versions

On the dual line Dragsters there's the possibility to have RGB filters that are organized in both lines as shown in the next figure.

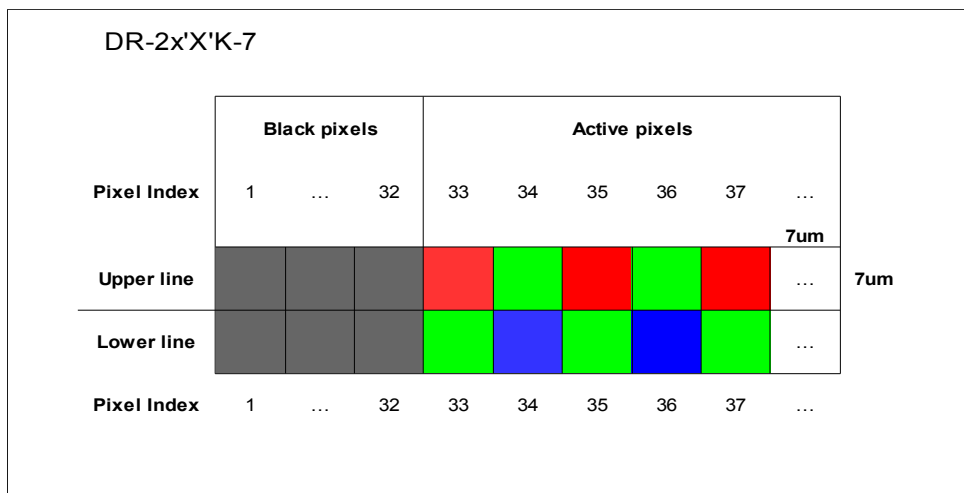


Fig 7: Color filter arrangement on Dragster dual line sensors

6.11 Placement of pixels DR-Xk-7

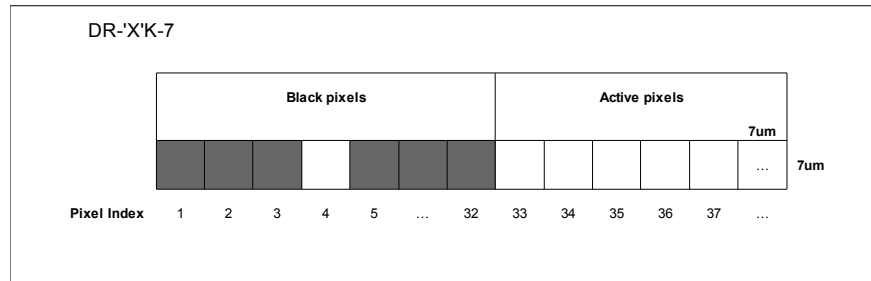


Fig 8: Placement of pixels sensors with 7um pixel pitch

6.11.1 Test & special pixels DR-Xk-7

The first 32 pixels include not only dark pixels but also special pixels like described:

1. The output from the first pixel is directly connected to the pad 1.*
2. The output from the second pixel is directly connected to the pad 2.*
3. The third pixel is a black pixel, electrically fixed to ADC low saturation
4. The fourth pixels is a white pixel, electrically fixed to ADC high saturation
5. The pixels 5 - 24 are normal pixels however the photo diode is covered by a metal light shield. They serve as a dark reference. However at longer wavelengths the metal shield will not completely shield light any more.
6. The pixels 25 -32 are electrical black pixels. In these pixels the photo diode is disconnected electrically from the readout chain. These pixels will follow all analogue and digital offset variations, however not integrate dark current or any photo current. They can be used check the validity of the dark pixels 5 - 24, or to compensate for line by line ADC offset variations.

These pixels are light sensitive. The respective outputs are connected to a test point on the head board for debugging purpose in certain package variations.

6.12 Placement of pixels DR-Xk-3.5

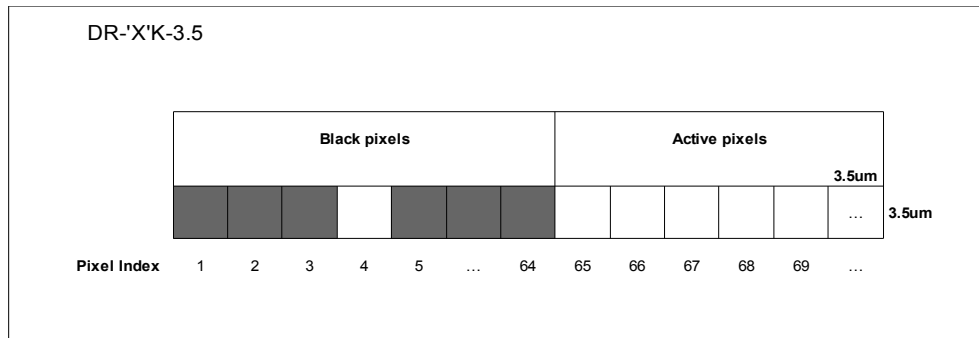


Fig 9: Placement of pixels sensor variations with 3.5µm pixel pitch

6.12.1 Test & special pixels DR-Xk-3.5

The first 64 pixels include not only dark pixels but also special pixels like described:

1. The output from the first & second pixels are directly connected to the pad 1 of the most left segments on top and bottom.*
2. The output from the third and fourth pixels are directly connected to the pad 2 of the most left segments on top and bottom.*
3. The fifth and sixth pixels are a black pixel, electrically fixed to ADC low saturation
4. The seventh and eighth pixels are white pixel, electrically fixed to ADC high saturation
5. The pixels 9 - 48 are normal pixels however the photo diode is covered by a metal light shield. They serve as a dark reference. However at longer wavelengths the metal shield will not completely shield light any more.
6. The pixels 49 - 64 are electrical black pixels. In these pixels the photo diode is disconnected electrically from the readout chain. These pixels will follow all analogue and digital offset variations, however not integrate dark current or any photo current. They can be used check the validity of the dark pixels 9 - 48, or to compensate for line by line ADC offset variations.

* These pixels are light sensitive. The respective outputs are connected to a test point on the head board for debugging purpose in certain package variations.

7 Functional Description

7.1 General sensor description

Sensors with 3.5µm pixels are structurally identical to sensors with 7µm pixel. However for the sensor with 3.5µm two independent readout blocks are placed, one on top of the sensor line, which reads out odd pixels and one at the bottom of the sensor line which reads out even pixels. Thus for sensors with 3.5µm pixels two independent segments are always placed together to form a segment with double resolution compared to the segment with 7µm pixel. Thus for sensors with 3.5µm pixel all pixel numbers indicated further in this section are double compared to the 7µm sensor variations.

The sensor is built of a line of 2080 pixels. The first 32 pixels counting from the left are designated as Black pixels, and are used to have a reference for dark current and signal offsets, the remaining 2048 are the normal pixels, responsible for the image. For readout each 2k segment is completely independent. This can be exploited to align the readout of the light sensitive pixels from each segment. To do so, the readout is started in the most left segment 16 Pixel clock cycles earlier than the more right segments. The individual start of readout for different segments can also be exploited to reduce the required signal bandwidth by sequentially addressing the SRAM blocks of different 2k segments and multiplexing the data lines.

The analogue voltage references, especially the references to define the ADC start voltage and the ADC gain are interconnected along the sensor line, however remain individual for odd and even pixels in the case of 3.5µm pixels. However each segment comprises an individual SPI block to configure these voltages. Normally it is recommended to program the registers controlling an interconnected voltage with the same settings. See figure 10 and 11 to illustrate how analogue voltages are interconnected over multiple segments and controlled over the respective SPI interfaces for sensors with 7µm and 3.5µm pixel pitch respectively.

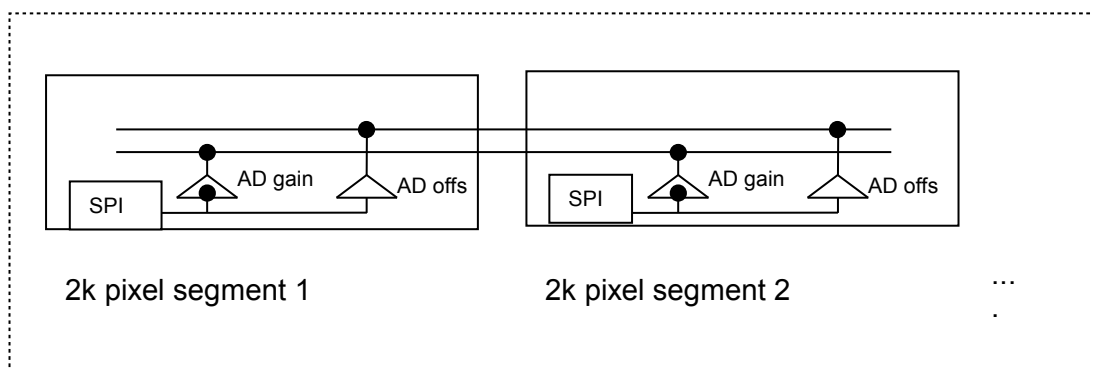


Fig 10: Interconnection of ADC reference voltages in case of 7µm pixel pitch sensors with multiple segments

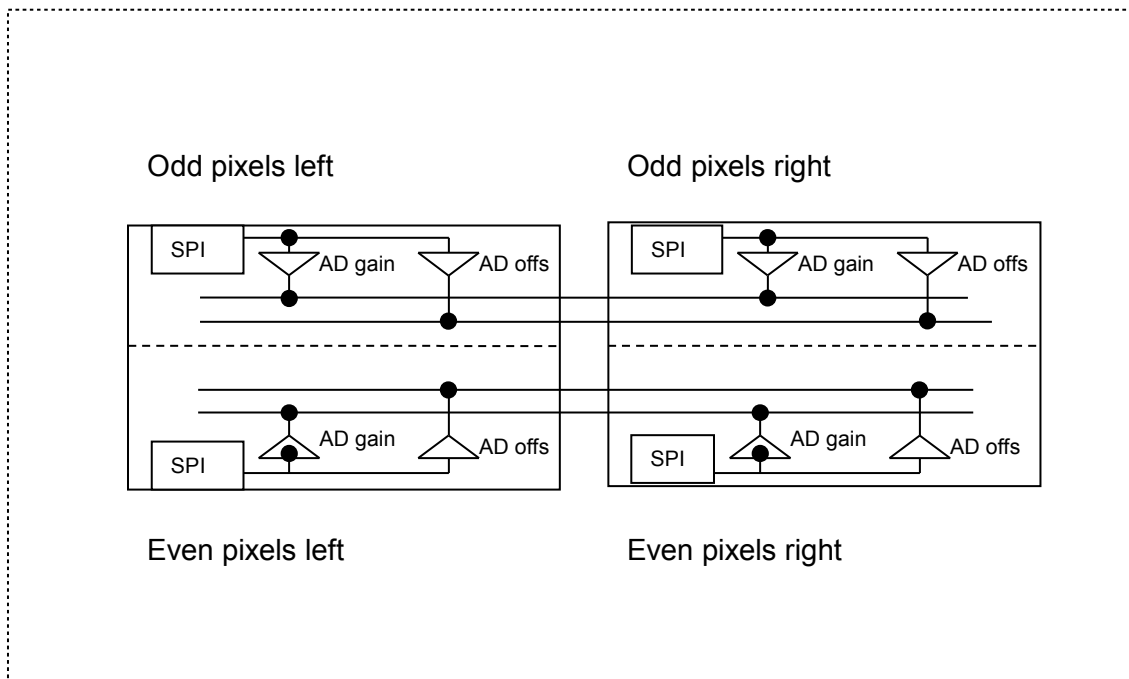
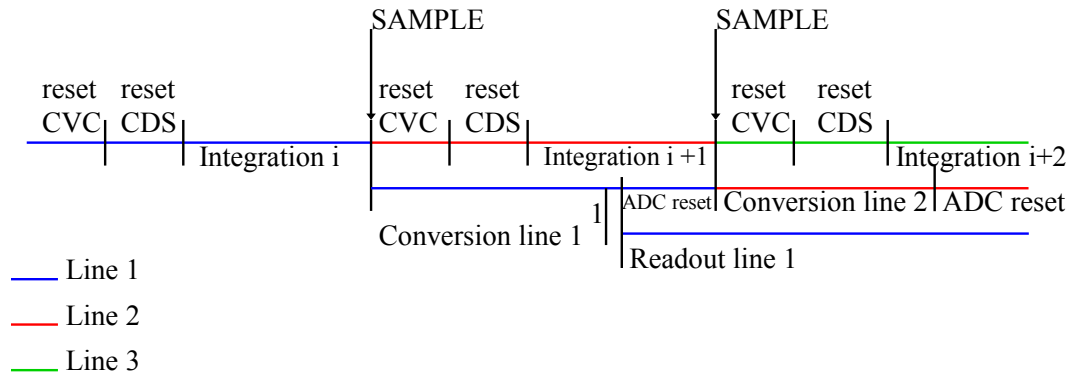


Fig 11: Interconnection of ADC reference voltages in case of 3.5 μ m pixel pitch sensors with multiple segments

The sensor features a 13 bit ramp ADC with programmable conversion gain and end range stage. The on chip digital control circuit generates all necessary control for conversion and the readout modes. However the readout of a new line can be triggered over an external signal if required. The ADC conversion range (maximum number of bit's can be programmed over the serial interface. Higher conversion range requires longer ADC conversion time.

The sensor enables interleaved integration, A/D conversion and readout, therefor the overall pipeline delay is 2 minimum line times.

Dragster readout pipeline delay overview



1 - Transfer from Shadow to Readout Register

Fig 12: Overview of pipelined integration ADC and readout sequence

7.1.1 Functional description Dragster Pixel

The Dragster line scan sensors features a highly sophisticated pixel, which provides true CDS capability for elimination of reset noise. Other features include programmable analogue gain, anti “blooming” circuit and anti “corona” that can be activated by register configuration. Each pixel features a sophisticated highly programmable ADC and two 13 bit wide memory benches. The first bench is used to hold the value of the last AD conversion ready for readout while the other is used to hold a black reference value which can be subtracted from the read out signal. Pixels integration, AD conversion and line readout can be made fully pipelined so that line rate is limited by the longest operation and not by the sum of all three.

An overview of the most important blocks of the analogue part and their functionality as well as the register bit's which control the features are described in the subsequent sections:

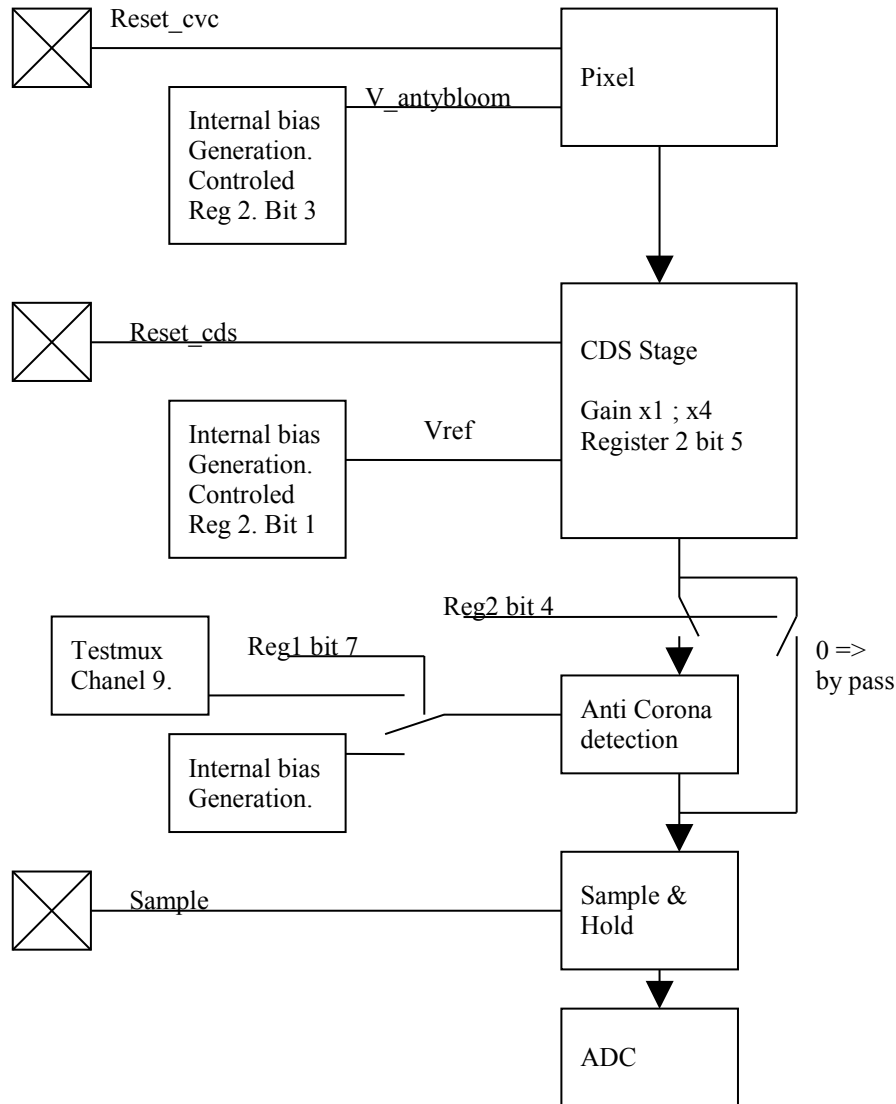


Fig 13: Overview of the functional blocks for the analogue part of the pixel

7.1.1.1 Anti Blooming circuitry

“Blooming” is a phenomena observed when a single pixel is heavily over exposed and saturates. Photo generated charges then tend to spill in neighbouring pixels. This is prevented by an internal circuit, which will drain charges when the pixel is saturated and prevent them from spilling into neighbouring pixels. This circuit is controlled by Register 2 Bit 3. 0 should be used for most applications, as it grants the largest linear signal range. Under extreme over exposure conditions this bit can be set to 1, which will start draining excessive charges earlier.

7.1.1.2 Anti corona circuitry

“Corona effect” is a phenomena sometimes observed under heavy overexposure condition when the most exposed pixels start to become dark again instead of white. This condition can be detected by a special circuitry and saturated pixels are then clamped to the white reference value before AD conversion. This circuitry can be enabled or bypassed by means of register 1 bit 7. 0 will disable the anti corona circuitry and bypass the signal, while 1 will enable it.

7.1.1.3 Analogue Gain

The pixel features a programmable analogue gain of factor x4. This gain is controlled by Register 2 bit 5. 0 uses unity gain, 1 uses a gain of x4.

7.1.1.4 CDS reference generation

The reference voltage for all CDS stages is generated in parallel by the internal bias generation block. The power consumption of the driver to this voltage can be regulated by means of register 2 bit 1. A Value of 1 will use an adaptive bias scheme to the buffer for this voltage, which will reduce power consumption when this driver is not used. 0 will chose a fixed bias value, which will result in a higher over all consumption.

{info only: The reference voltage of the CDS stage is sampled at start of integration for each line, and thus influences the finally digitized analogue value. Any noise on this signal obviously also influences the final signal value because noise will be added equally to all pixels in the line. For ultimate noise performance it's advised to compute the average of the first dark pixels 16th to 20th and subtract this value from the finally read out pixels for each line. This computation has to be done off chip, but will lead to noise performance better than the one specified : end info}

7.1.1.5 Pixel Level ADC

Each pixel features a sophisticated multi stage ADC, which minimizes the offset and gain error between individual pixels and segments. The physical block diagram of the ADC and a description of the main functional modes is given in figure 14.

For a high resolution, low noise ADC functionality, the ADC is made such that the critical analogue blocks can run at relatively low speed. Besides the inherently high quality of the ADC, the homogeneity is further be increased by using on chip digital offset cancellation.

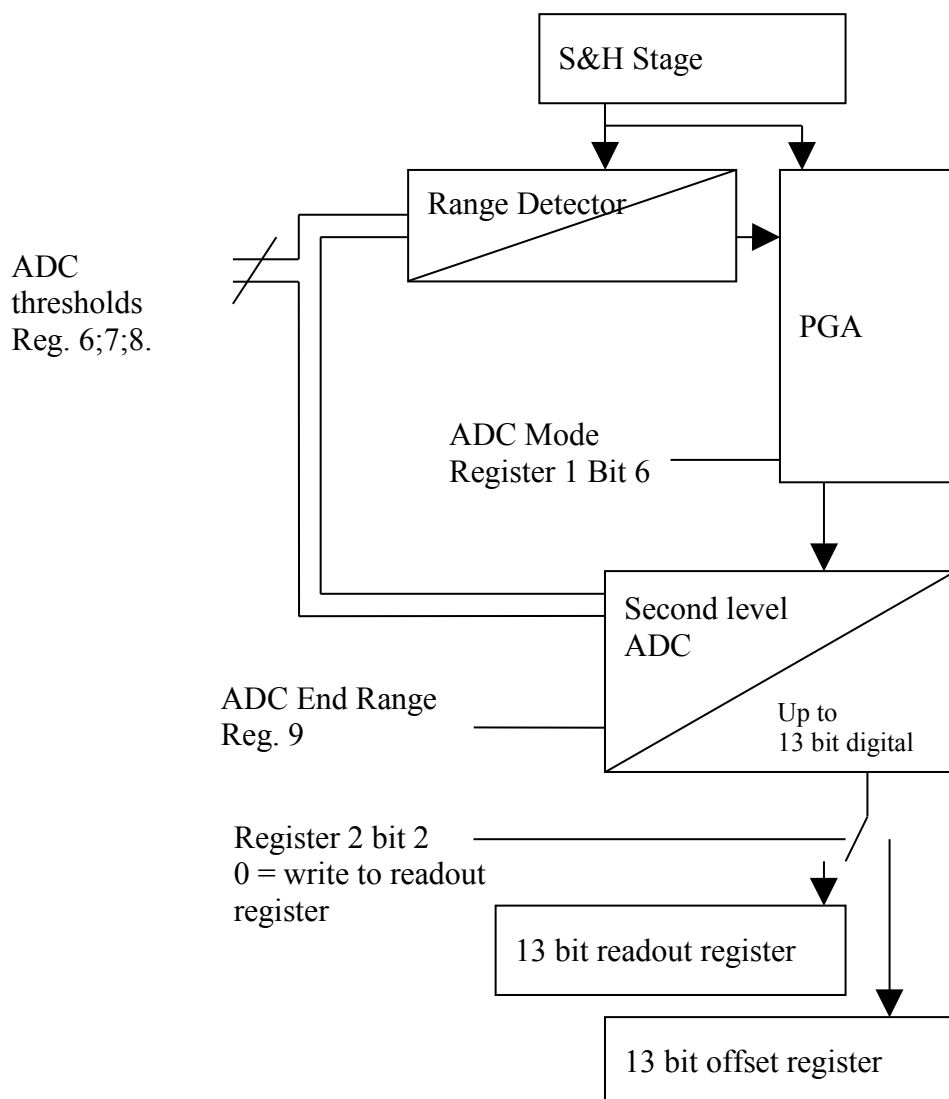


Fig 14: Functional block diagram of the pixel level ADC

The ADC features two modes of operation: "linear" AD conversion and "companding" AD conversion. On linear conversion the ADC will require as many clock cycles as the register

programmed ADC end of range. See figure 15 for a diagram of the ADC linear response function and the effect of the different registers on the transfer function.

Note: *It is important to program the End of range according to the pixel data bit width. If digital saturation logic is not enabled in the register 1 bit 5, ADC end range is above 4095 and only 12 LSB's are read out, this can create signal “wrap around” artefacts when the pixel value is over 4095.*

In order to reduce the ADC conversion time comparing to readout time and keep the ADC in linear mode, the converter can be operated at a higher clock frequency than the remaining circuitry. This is done by directly supplying the higher clock frequency to the chip main clock and programming the internal clock divider (Register 1 bits 0 and 1) such that the clock frequency in chip's readout remains below 50MHz.

An alternative to running the ADC at higher clock rate is to use the ADC's “companding” mode. As for an optical signal, the photon shot noise increases with signal level, a very small quantization step is only required at the very low signal values. For higher impinging optical signals the ADC quantization step can be increased such as to match the shot noise present in the light signal. This may significantly reduce the total ADC time required to generate a 12 bit value, while no information is lost. See figures 16 and 17 for an illustration of the “companding” ADC mode and the registers involved in programming it's response function.

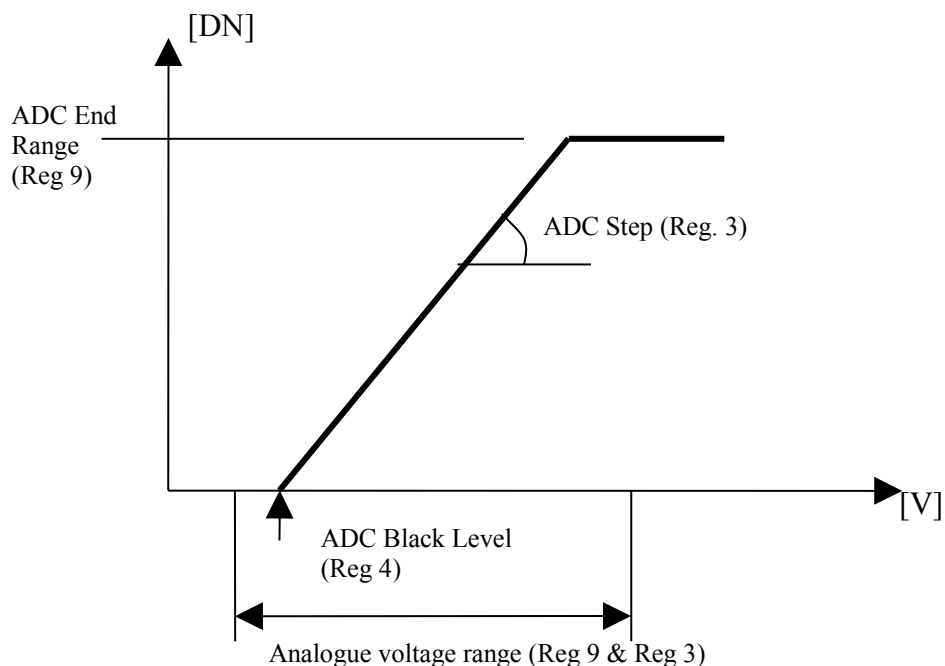


Fig 15: ADC transfer function in linear mode and registers defining the ADC parameters

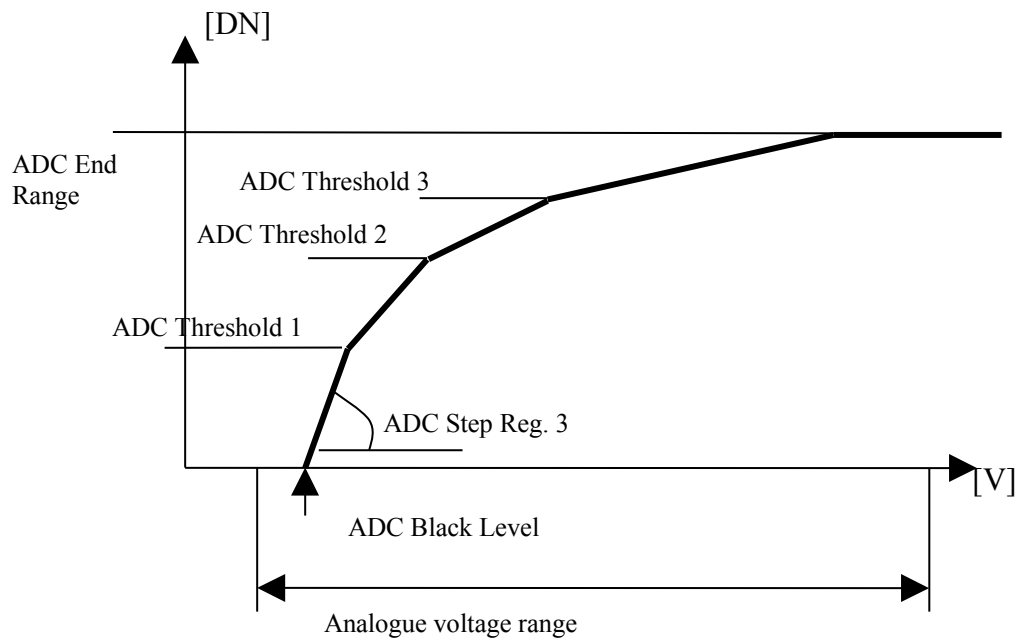


Fig 16: ADC transfer function in companding mode

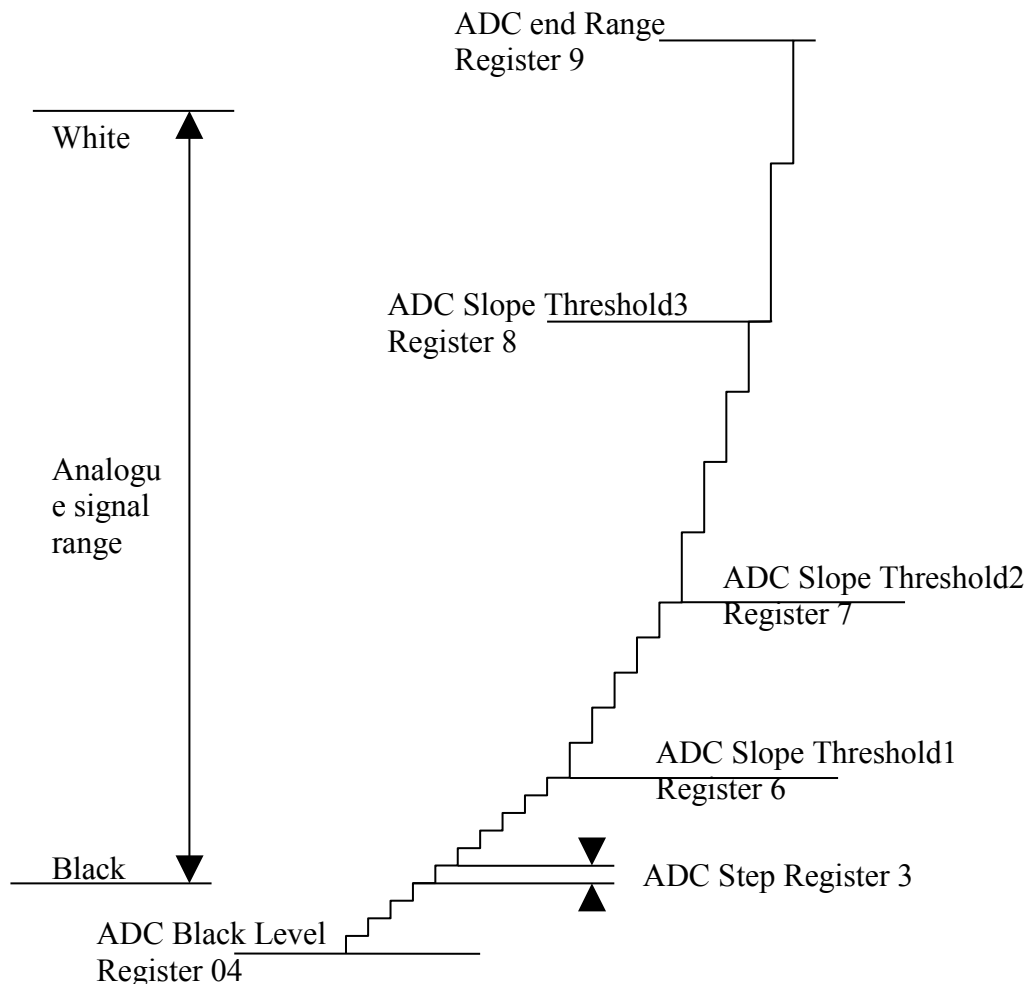


Fig 17: Adaptation of the ADC conversion step in companding ADC mode

When using “companding” ADC mode to reduce conversion time it is possible to still produce a linear sensor output by enabling on chip digital re-linearization circuitry (Register 5 bit 1). When using on chip re-linearization, the histogram will show missing codes in the range where the ADC was working in companding mode that can be corrected by enabling on chip "Dithering" (Register 1 bit 3).

Note: *When using the ADC in “companding” mode, it is important to program the 3 thresholds strictly monotonously increasing, and smaller than the “end range “ value. Otherwise the ADC will not function correctly and produce strongly distorted output signals.*

7.1.1.6 Digital Readout concept

The pixel level ADC signal is stored in an SRAM bench, with 13bit's for offset and 13 bit's for signal value. At signal readout, the digital offset cancellation features should be enabled however, to save digital power, this feature can be disabled and the direct output value of the ADC can be read out.

Note: *When switching on digital offset subtraction, it is important, that firstly the offset SRAM block is powered on (Register 5, bit 2) and that a proper offset reference is stored in the SRAM bench.*

The digital readout of the Dragster sensor is triggered by a signal “load_pulse”. This signal can either be provided externally or be generated internally (register 2 bit 0) at the earliest possible time based on the state of the integration time controlling signals (rest_cvc; reset_cds; sample) and the programmed ADC end range. When the sensor receives an external load pulse, readout is started from the most left pixel to the right on each segment. An LVAL signal is generated to indicate valid pixel data. While reading out data, it can be chosen to read out pixels directly from the “readout register” or to readout the “readout register” and the “offset register” from the SRAM bench simultaneously and to subtract offset from the readout value on chip. This process requires a valid offset that must have previously been stored in the offset register.

When using offset subtraction, a saturation logic can be enabled by means of register 1 bit 5. This logic permits to work with signal values above 4096, such that after subtraction of the black level still full 12 bit data is available.

7.2 Configuration Bit Overview

| Mode signal | Value | Description | Register control bit |
|--------------------|-------|---|----------------------|
| ADC_mode_bit | 0 | If mode bit is set to zero, linear ADC conversion is used | Register #1 bit #6 |
| | 1 | Companding AD conversion mode | |
| Re-linearization | 0 | No on chip re-linearization of companding ADC mode is computed | Register#5 bit #2 |
| | 1 | In companding mode the response is re-linearized on chip prior to signal output | |
| dithering | 0 | No Dithering | Register #1 bit #3 |
| | 1 | Dithering is used when using on chip militarization to avoid missing codes in histogram. | |
| en_sat | 0 | The digital saturation is not enabled, so the output from the subtracter will not be saturated. If the subtraction result is larger than 12 bit, the 13th bit must be read out to avoid "wrap around" | Register #1 bit #5 |
| | 1 | Digital Saturation is enabled, the output after offset subtraction will be set to 4096, when ever the results is higher or equal than 4096 | |
| offset subtraction | 0 | The digital offset is not subtracted from the read value. | Register #1bit #4 |
| | 1 | The value stored in the offset register is subtracted from the readout signal. Note: In order to work with offset Subtraction the offset SRM must be powered on. (Register 5 bit 2) | |
| writing offset | 0 | not active, values of the AD conversion go to the readout registers | Register #2 bit #2 |
| | 1 | When active, a new value is written to the offset registers. Note: prior to write an offset reference value to the offset SRAM the offset SRM must be powered on. (Register 5 bit 2) | |
| Enable offset | 0 | Offset SRAM in power down mode | Register #5 bit #2 |

| Mode signal | Value | Description | Register control bit |
|------------------------------|-------|--|----------------------------------|
| SRAM | 1 | Offset SRAM is active | Register #1 bit #1 and bit #2 |
| | 00 | readout clock set to Mclk | |
| | 01 | readout clock set to Mclk/2 ADC clk remains at MCLK | |
| | 10 | readout clock set to Mclk/4 ADC clk remains at MCLK | |
| | 11 | do not use, clock not generated | |
| Pixel clock output enable | 0 | No pixel clock is given out. (output pad in tristate) | Register # 5 bit #0 |
| | 1 | Pixel clock is given out | |
| en_anti_blooming | 0 | anti blooming feature off | Register #2 bit #3 |
| | 1 | anti blooming feature on | |
| en_control_vref | 1 | Vref comparator bias in adaptive power mode. (use this configuration) | Register #2 bit #1 |
| | 0 | Vref comparator bias is in constant low power mode. (do not use) | |
| auto_gen_load_pulse | 0 | The pulse for readout has to be provided externally | Register #2 bit #0 |
| | 1 | The pulse for readout is generated internally, immediately after completed AD conversion. (multiple readouts of the same data occur if no new AD conversion has been started after finalization of the line readout. | |
| en_white_clamp (anti corona) | 0 | The white clamp is not active | Register #2 bit #4 |
| | 1 | The clamping of white values set. White clamp is used to avoid contrast inversion of heavily over exposed scenes. (corona effect) | |
| vthr_bit | 0 | Do not use, write 0. | Register #1 bit #7 |
| | 1 | The threshold voltage for the white clamping is given internally | |
| analog_gain | 0 | No analog gain (x1) in the CDS | Register #2 bit #5 |
| | 1 | Analog gain (x4) in the CDS | |

7.3 Register definition

Every internal status of the sensor will be controlled by the serial interface and be written to the internal registers. All registers are 8bit oriented, the unused bits on a register will set to 0 and reserved for future use.

7.3.1 CONTROL register 1

Address : 0x01
Operation: R/W
Reset Value: 0xA8

| <i>0X01</i> | <i>Bit 7</i> | <i>Bit 6</i> | <i>Bit 5</i> | <i>Bit 4</i> | <i>Bit 3</i> | <i>Bit 2</i> | <i>Bit 1</i> | <i>Bit 0</i> |
|-------------|--------------|--------------|-------------------|--------------------|--------------|------------------|------------------|----------------|
| Description | Vthr bit | ADC mode bit | Enable saturation | Offset subtraction | Dithering | Clock division 2 | Clock division 1 | Update request |
| @reset | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

Bit 0 – Update_request

In order to activate a set of new register values uploaded over SPI, this bit has to be set to 1. Register data does not change unless this bit was set to 1 and a rising edge of end_adc occurred. When this bit is set, at the next rising edge of "end_adc" signal the register values are updated.

Bit 1/2 – Clock Division 1 / 2

This bits are responsible for the definition of readout clock (pixel clock), the different values are presented on the following table:

| Bit 2 | Bit 1 | Description |
|-------|-------|---|
| 0 | 0 | readout clock set to Mclk |
| 0 | 1 | readout clock set to Mclk/2 ADC clk remains at MCLK |
| 1 | 0 | readout clock set to Mclk/4 ADC clk remains at MCLK |
| 1 | 1 | do not use, clock not generated |

Bit 3 – Dithering

This bit is enables the on chip "Dithering" logic to avoid missing codes in the output histogram when on chip re-linearization is used in combination with companding ADC mode.

Set to '0' – Dithering deactivated

Set to '1' – Dithering activated

Bit 4 – Offset Subtraction

Set to '0' – The digital offset is not subtracted from the read value.

Set to '1' – The value stored in the offset register is subtracted from the readout signal.

NOTE: *If this bit is turned on, the Bit 2 in Control Register 3 (Reg 0x05) "Enable Offset SRAM" must be set to 1.*

Bit 5 – Enable Saturation

Set to '0' – The digital saturation is not enabled, so the output will cover full 13 bit. If only 12 bit are read out "wrap around" error may occur if end_adc range is not properly configured.

Set to '1' – Digital Saturation is enabled, the output will be saturated to the 12 LSB's. **NOTE:** *the 13th bit should be ignored if on chip saturation is enabled, it holds an overflow identification flag in this case*

Bit 6 – ADC mode bit

Set to '0' – Linear ADC conversion is used.

Set to '1' – Companding ADC conversion is used.

Bit 7 – Vthr bit

Set to '0' – Do not use, write 1. (Test purposes only)

Set to '1' – The threshold voltage for the white clamping is given internally.

7.3.2 CONTROL register 2

Address : 0x02

Operation: R/W

Reset Value: 0x12

| 0X02 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|--------------|--------------|---------------|-----------------------|----------------------|--------------|---------------------|---------------------|
| Description | Not used | Not used | Analogue gain | Enable white clamping | Enable anti blooming | Write Offset | Enable Control Vref | Auto Gen load Pulse |
| @reset | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

Bit 0 – Auto Gen Load Pulse

Set to '0' – The pulse for readout has to be provided externally.

Set to '1' – The pulse for readout is generated internally, immediately after completed AD conversion and once the LVAL of the previous line readout is back to 0.

Bit 1 – Enable Control Vref

Set to '0' – Vref buffer bias is in constant power mode. (not recommended)

Set to '1' – Vref buffer bias in adaptive power mode.

Bit 2 – Write Offset

Set to '0' – Not active, values of the AD conversion go to the readout registers.

Set to '1' – When active, a new value is written to the offset registers.

NOTE: *If this bit is turned on, the Bit 2 in Control Register 3 (Reg 0x05) "Enable Offset SRAM" must be set to 1.*

Bit 3 – Enable Anti Blooming

Set to '0' – Additional anti blooming feature OFF.

Set to '1' – Additional anti blooming feature ON.

NOTE: *The pixels inherent anti blooming structures will under normal conditions prevent any kind of blooming. Only under the most extreme over exposure condition this additional anti blooming circuitry may be required.*

Bit 4 – Enable White Clamping (Anti-Corona)

Set to '0' – The white clamp is not active.

Set to '1' – The clamping of white values set. White clamp is used to avoid contrast inversion of heavily over exposed scenes. (corona effect).

Bit 5 – Analogue Gain

Set to '0' – No analogue gain (x1) in the CDS.

Set to '1' – Analogue gain (x4) in the CDS.

7.3.3 Inversed ADC Gain Register

Address : 0x03
Operation: R/W
Reset Value: 0X1D

| 0X03 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Description | MSB | | | | | | | LSB |
| @reset | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |

Responsible for ADC conversion gain. Respectively the ADC conversion step. The register is proportional to the voltage step required for 1 DN.

Higher value on this register, results in a lower ADC gain. (higher voltage step for 1 DN)

7.3.4 Offset register

Address : 0x04
Operation: R/W
Reset Value: 0XC8

| 0X04 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Description | MSB | | | | | | | LSB |
| @reset | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

Responsible for ADC black level offset. The lower the value of the offset register the closer the output signal will be to the white level, whit the increasing of the register value the output signal will become more black.

7.3.5 CONTROL register 3

Address : 0x05
Operation: R/W
Reset Value: 0x12

| 0X05 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|--------------|--------------|------------------|------------------|------------------|--------------------|------------------|---------------------------|
| Description | Not used | Not used | Bandgap switch 3 | Bandgap switch 2 | Bandgap switch 1 | Enable Offset SRAM | Re-linearization | Pixel clock output enable |
| @reset | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

Bit 0 – Pixel clock output enable

Set to '0' – The pixel clock pad is in tristate mode.

Set to '1' – The pixel clock is provided to the user on the pad.

Bit 1 – Re-linearization

Set to '0' – In companding ADC mode the piece wise linear compressed data is given out.

Set to '1' – When using the companding ADC mode, the compressed data is re-linearized on chip to a linear 12bit representation. It is recommended to use "dithering" (Control register 1 bit 3) together with this feature to avoid missing codes in the output signal.

Bit 2 – Enable Offset SRAM

Set to '0' – Offset SRAM is powered down. (Stored offset values are lost).

Set to '1' – Offset SRAM is enabled.

Bit 3/4/5 – Bandgap Switch 1/2/3

These bit's can be used to trim the reference current generated by the bandgap circuit of different segments.

| Bit 5 | Bit 4 | Bit 3 | Relative current to nominal* |
|-------|-------|-------|------------------------------|
| 0 | 0 | 0 | 132,00% |
| 0 | 0 | 1 | 77,00% |
| 0 | 1 | 0 | 100,00% |
| 0 | 1 | 1 | 64,00% |
| 1 | 0 | 0 | 112,00% |
| 1 | 0 | 1 | 70,00% |
| 1 | 1 | 0 | 86,00% |
| 1 | 1 | 1 | 59,00% |

* The generated reference current can be observed at the TEST_MUX output pin's. The target is 100uA. These bit's can be used to tune the general reference back to target values in case production parameter spread leads to strong deviation. Further these bit's can be used to reduce over all power consumption, though the reference voltages, (namely ADC 0 reference will drift from target values and may have to be over driven to get proper operation at lower over all current. (Reg 0x0A channel 0x0F)

7.3.6 Threshold register 1

Address : 0x06
Operation: R/W
Reset Value: 0x01

| 0X06 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Description | MSB | | | | | | | LSB |
| @reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

This register is responsible for holding the value for the first ADC threshold in companding mode. The register content is multiplied by 32.

7.3.7 Threshold register 2

Address : 0x07
Operation: R/W
Reset Value: 0x06

| 0X07 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Description | MSB | | | | | | | LSB |
| @reset | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

This register is responsible for holding the value for the second ADC threshold in companding mode. The register content is multiplied by 32.

7.3.8 Threshold register 3

Address : 0x08
Operation: R/W
Reset Value: 0x6D

| 0X08 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Description | MSB | | | | | | | LSB |
| @reset | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |

This register is responsible for holding the value for the third ADC threshold in companding mode. The register content is multiplied by 32.

7.3.9 End of Range register

Address : 0x09
Operation: R/W
Reset Value: 0x7F

| 0X09 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Description | MSB | | | | | | | LSB |
| @reset | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

This register is responsible for holding the value to configure the end of the ADC range. (the highest digital value computed by the ADC.) The Register holds the 8 MSB's of a 13 bit

value. (the 5 LSB's are set by hard wiring to 0.) The time in master clock cycles the ADC requires for a conversion equals the value in this register multiplied by 32. Use this register to chose between 10bit, 11bit 12bit or even 13bit ADC resolution. The ADC resolution trades versus the ADC conversion time. Higher resolution thus requires longer line periods, or the ADC to be run at higher clock frequency.

7.3.10 Test Multiplexer register

Address : 0x0A

Operation: R/W

Reset Value: 0x00

| 0X0A | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Description | hv_3 | hv_2 | hv_1 | hv_0 | test_3 | test_2 | test_1 | test_0 |
| @reset | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

This register is responsible for holding the value to configure the test multiplexer. It defines the channel that will select as output for the test multiplexer. Write 0x0F

{info only:

| Channel | Signal | Comment |
|---------|-------------------|--|
| 0x00 | VSS | Reset default |
| 0x01 | Vbg | Internal Bandgap reference voltage |
| 0x02 | bias_vref | Bias reference of on chip CDS reference buffer |
| 0x03 | gnd_rst_cvc | Anti blooming reference voltage |
| 0x04 | pcas_cds | Internal reference voltage |
| 0x05 | ncas_cds | Internal reference voltage |
| 0x06 | vbias_cds | Internal reference voltage |
| 0x07 | vbias_white_clamp | Internal reference voltage |
| 0x08 | Vthr | Threshold voltage for saturation detection |
| 0x09 | vbias_cvc | Internal reference voltage |
| 0x0A | Iref | Current output (measure towards VSS) for internal bias generation. Target value 100uA |
| 0x0B | vbias_comp_1 | Internal reference voltage |
| 0x0C | Rst_cvc | Monitor of digital control signal reset_cvc |
| 0x0D | Vrst | Internal reference voltage |
| 0x0E | Rmp | Internal reference voltage |
| 0x0F | ADC_reference | Reference voltage for ADC 0 level. Can be over driven. Additional decoupling on this signal may improve noise performance. |

Table 11: Test multiplexer channels

: end info }

7.4 Serial 4 wire configuration interface

For access to the internal registers of the sensor, a serial interface with 4 wires is implemented. The interface consists in 4 different lines, one clock line (SCLK), one receive (MOSI) and transmit (MISO) line which are synchronous to each other. The fourth line is the chip select (/CS) and must be low to send/receive data through the lines. The sensor will be always slave in the application. By the use of the /CS signal the master can activate the serial interface of an individual segment or several segments together. The bus frequency range is from DC to 20MHz, but must always be lower than $MCLK/2$.

The data is sent from LSB to MSB. The command word has a length of 16 bits and contains the data of the register and the register address. It is possible to write multiple registers consecutively, sending data and address each 16 SCLK. After the last write word the SCLK should be sent for minimum 2 extra clocks, (maximum 4 SCLK) while /CS is still low.

The updating to the registers is performed after update request bit is sent at the next rising edge of "RESET_COUNTER" signal. The last word sent to the registers has to be always register 0x01 and containing the update request bit, otherwise not update is performed.

7.4.1 Writing Operation

The writing operation is performed by sending the word containing the data and the address, no acknowledge signal or indication is given back.

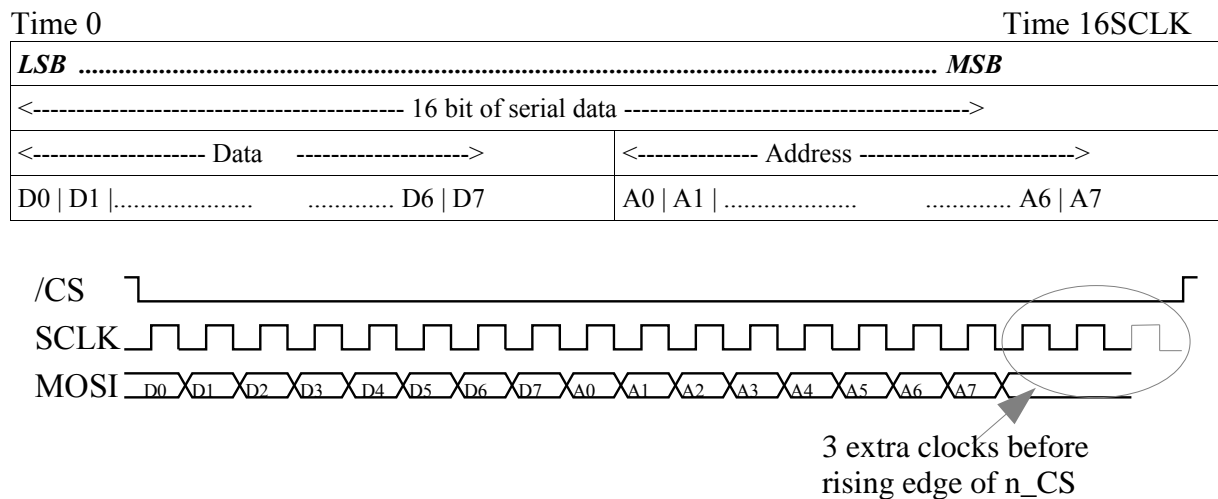


Fig 18: Writing operation

7.4.2 Reading Operation

To perform a read operation, the address for the register to be read, has to be written on register 15 (as data). MISO line, with one leading one, and with 2 SCLK delay to the last bit of the address word (LSB first).

Time 0

| | |
|-------------------------------------|---------------------------|
| LSB | |
| <----- 16 bit of serial data -----> | |
| <----- Data (read address) -----> | <----- Address R15 -----> |
| D0 D1 D6 D7 | A0 A1 A6 A7 |

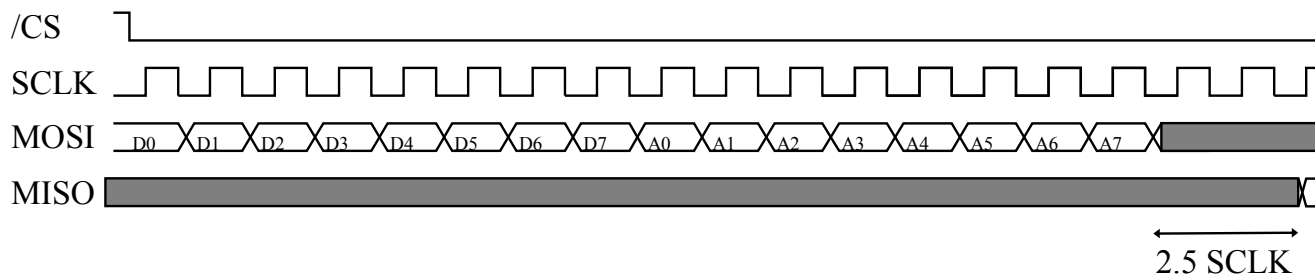


Fig 19: Reading operation

7.5 Timing diagrams

Start of integration

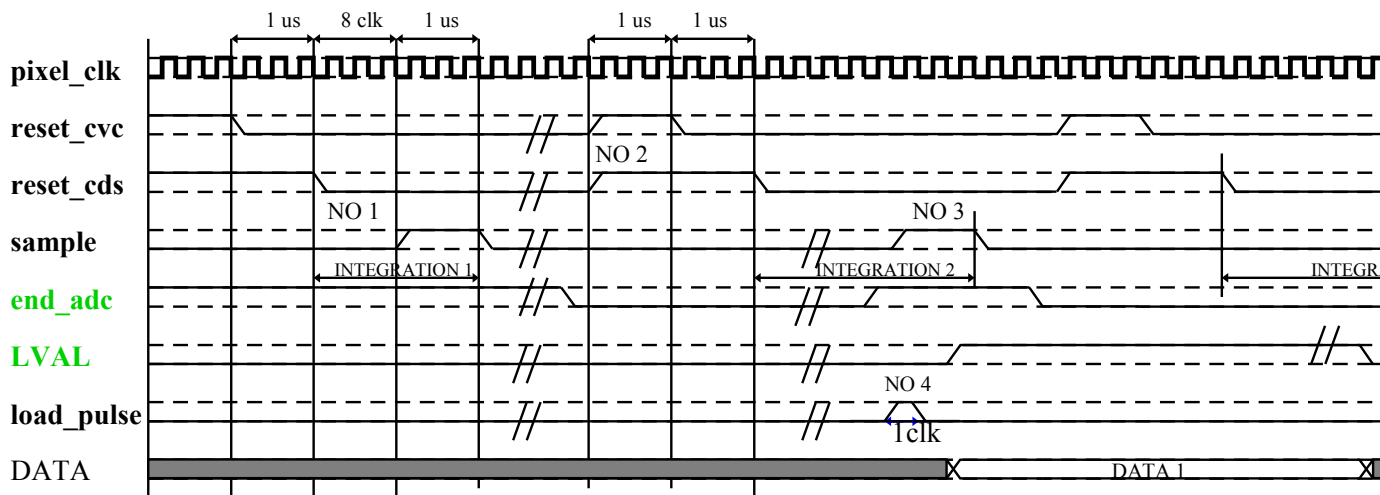


Fig 20: Timing diagram

- NO 1** - To start the integration the user should send the falling edge of RST_CVC and with a delay of 1us after at least 8clk the user can send the raising edge of SAMPLE. However the rising edge of SAMPLE should active ADC conversion. (END_ADC = HIGH) and SAMPLE should be high for at least 1us.
- NO 2** - The user can send the rising edge of RST_CVC and RST_CDS earliest 7clk after falling edge of sample, END_ADC will have it's falling edge)
- NO 3** - The raising edge of SAMPLE should only be sent if END_ADC is HIGH
- NO 4** - The load pulse should be sent, with at least 4 clocks delayed to the latest event of falling edge of LVAL

End of readout entering idle

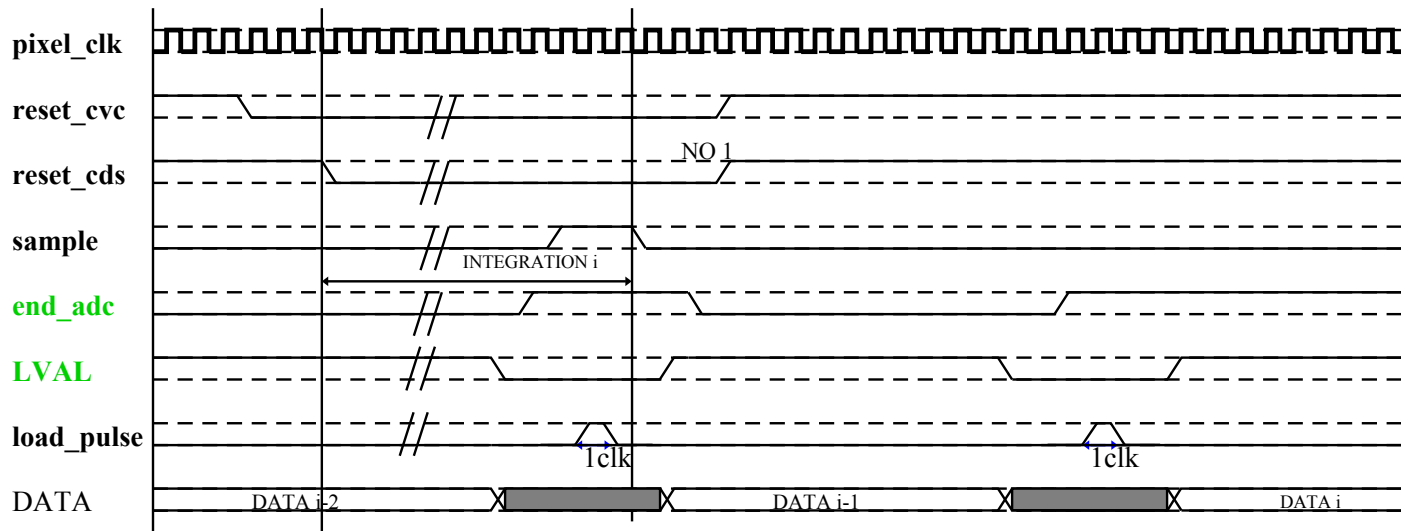
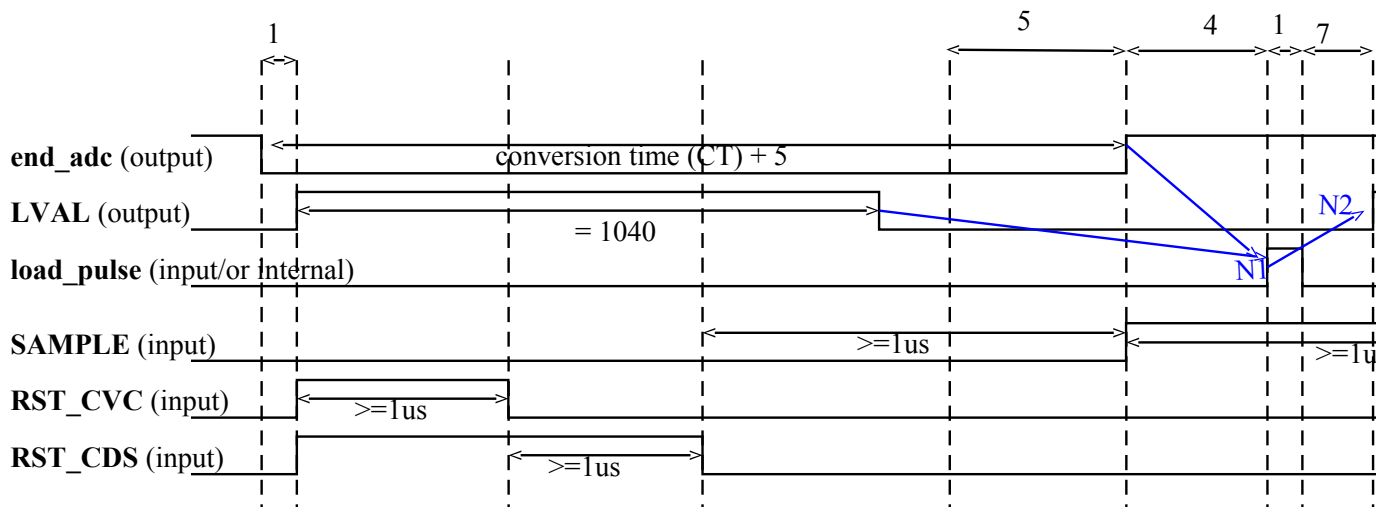


Fig 21: Timing diagram

NO 1 - To put the sensor in idle mode, the user should send the rising edge of RST_CVC and RST CDS, and

Detail end of integration start ADC and readout



NOTE 1: rising of load = the later of (rising edge end_adc; falling edge LVAL) + 4

NOTE 2: rising of LVAL = rising edge of load_pulse + 8

NOTE 3: falling of end_adc = falling edge of SAMPLE + 6

Conversion time:

if ADC_mode_bit = 0)

$$CT = \text{end_range} * 32$$

else (ADC_mode_bit = 1)

$$CT = \lceil \text{thr1} + (\text{thr2} - \text{thr1}) / 2 + (\text{thr3} - \text{thr2}) / 4 + (\text{end_range} - \text{thr3}) / 8 \rceil * 32$$

Fig 22: Detail end of integration start ADC and readout

8 Pins and functionality

| Pin Name | In-Out | Function |
|-------------|---------|--|
| Out_CVC_x | in/out | CVC output for pixel X, leave open or provide pull up/down to fix read value. |
| Out_CDS_x | in/out | CDS output for pixel X, leave open or provide pull up/down to fix read value. |
| SAMPLE | Dig in | Sample signal |
| RST_CVC | Dig in | Reset signal for CVC |
| RST_CDS | Dig in | Reset signal for CDS |
| N_CS | Dig in | Negative Chip Select for serial interface |
| SCLK | Dig in | Serial clock for serial interface |
| MOSI | Dig in | Master out / Slave in line for serial interface interface |
| MISO | Dig out | Master in / Slave out line for serial interface interface |
| VDDA | - | Analog power supply |
| VDD_Bulk | - | Bulk power supply |
| VDDD | - | Digital power supply |
| VDDES | - | ESD protection power supply |
| VDDIO | - | I/O power supply |
| VSSA | - | Analog ground |
| VSS_Bulk | - | Bulk ground |
| VSSD | - | Digital ground |
| VSSESD/IO | - | ESD protection and I/O ground |
| LVAL | Dig out | Line valid signal |
| load_pulse | Dig in | Pulse to be shift on readout chain |
| Bit 0..12 | Dig out | Bits from readout |
| end_adc | Dig out | Indication from counter beeing in reset |
| main_clk | Dig in | Main clock input |
| test_mux | NC | Leave open |
| Vref | NC | Leave open |
| n_reset | Dig in | Global reset signal. Low active |
| VDD_05 | NC | Leave open |
| Vclamp | VDDA | Connect to VDDA |
| Pixel_clock | Dig out | Outuptu pixel clock (frequeuncy only differs from main clock if klok diff is used) |

Table 12: Pins and functionality

9 Tap organization

9.1.1 Tap organization DR-2k-7, DR-4k-7, DR-8k-7

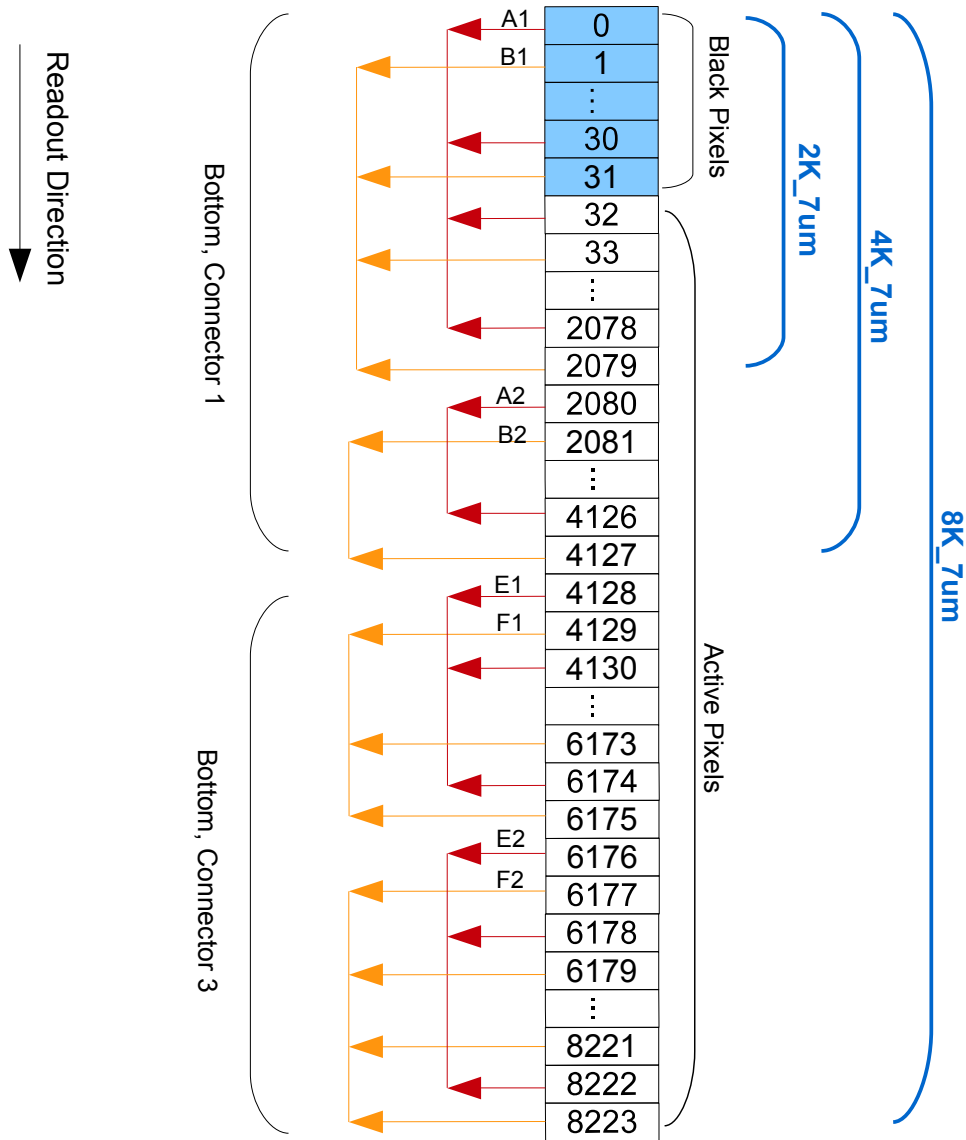


Fig 23: Tap organization DR-2k-7, DR-4k-7, DR-8k-7

9.1.2 Tap organization DR-6k-7

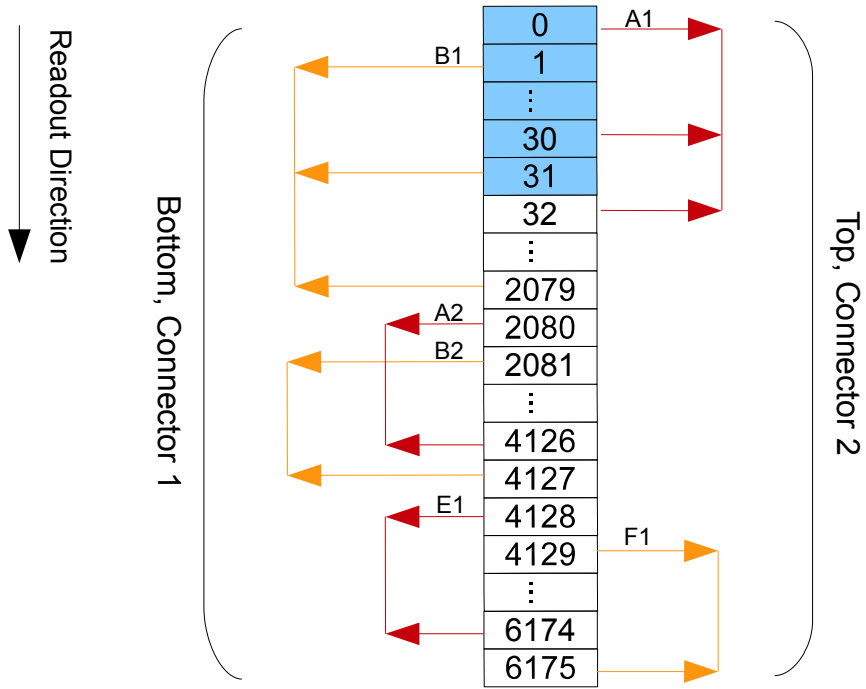


Fig 24: Tap organization DR-6k-7

9.1.3 Tap organization DR-4k-3.5, DR-8k-3.5, DR-16k-3.5

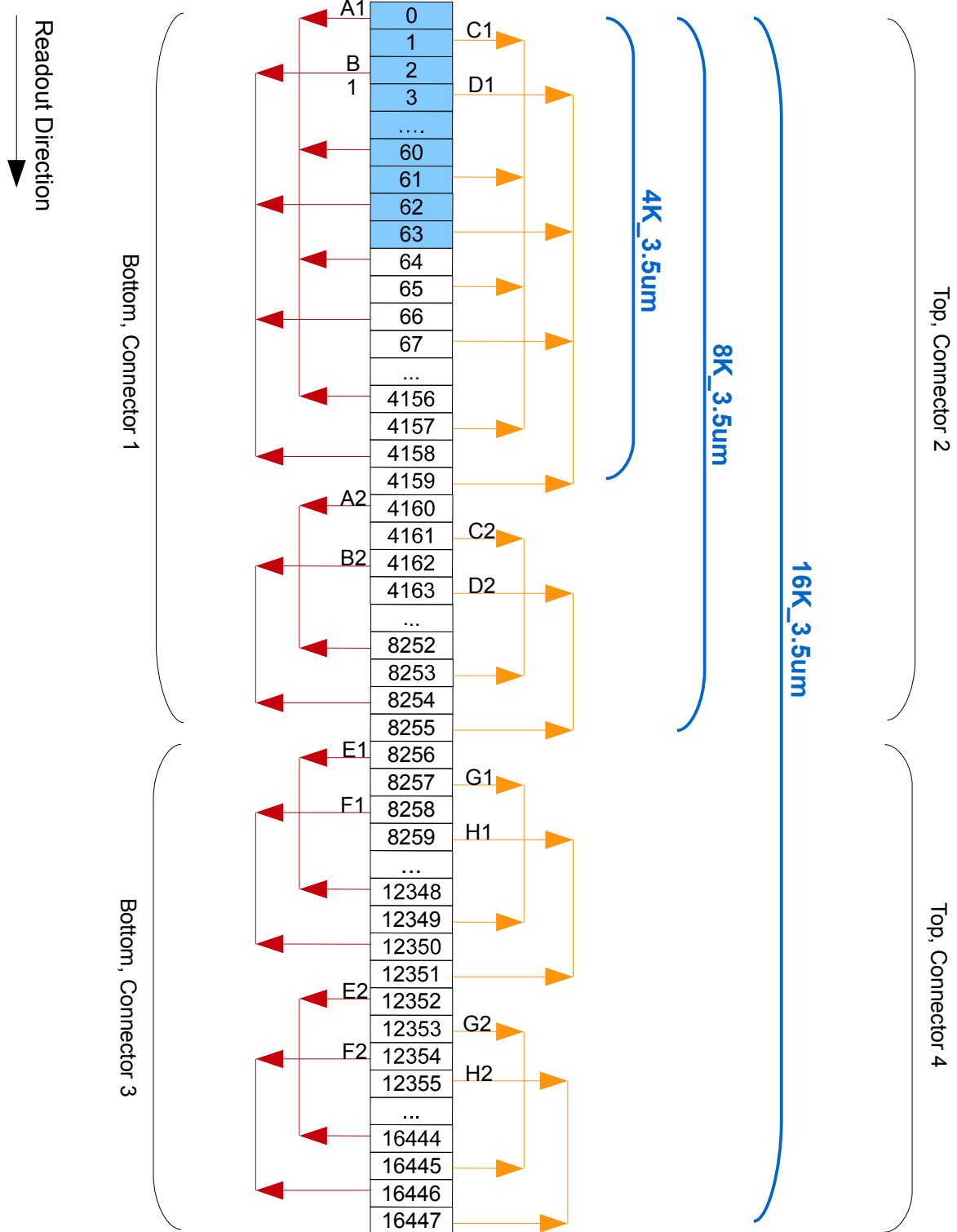


Fig 25: Tap organization DR-4k-3.5, DR-8k-3.5, DR-16k-3.5

9.1.4 Tap organization DR-2x2k-7, DR-2x4k-7, DR-2x8k-7

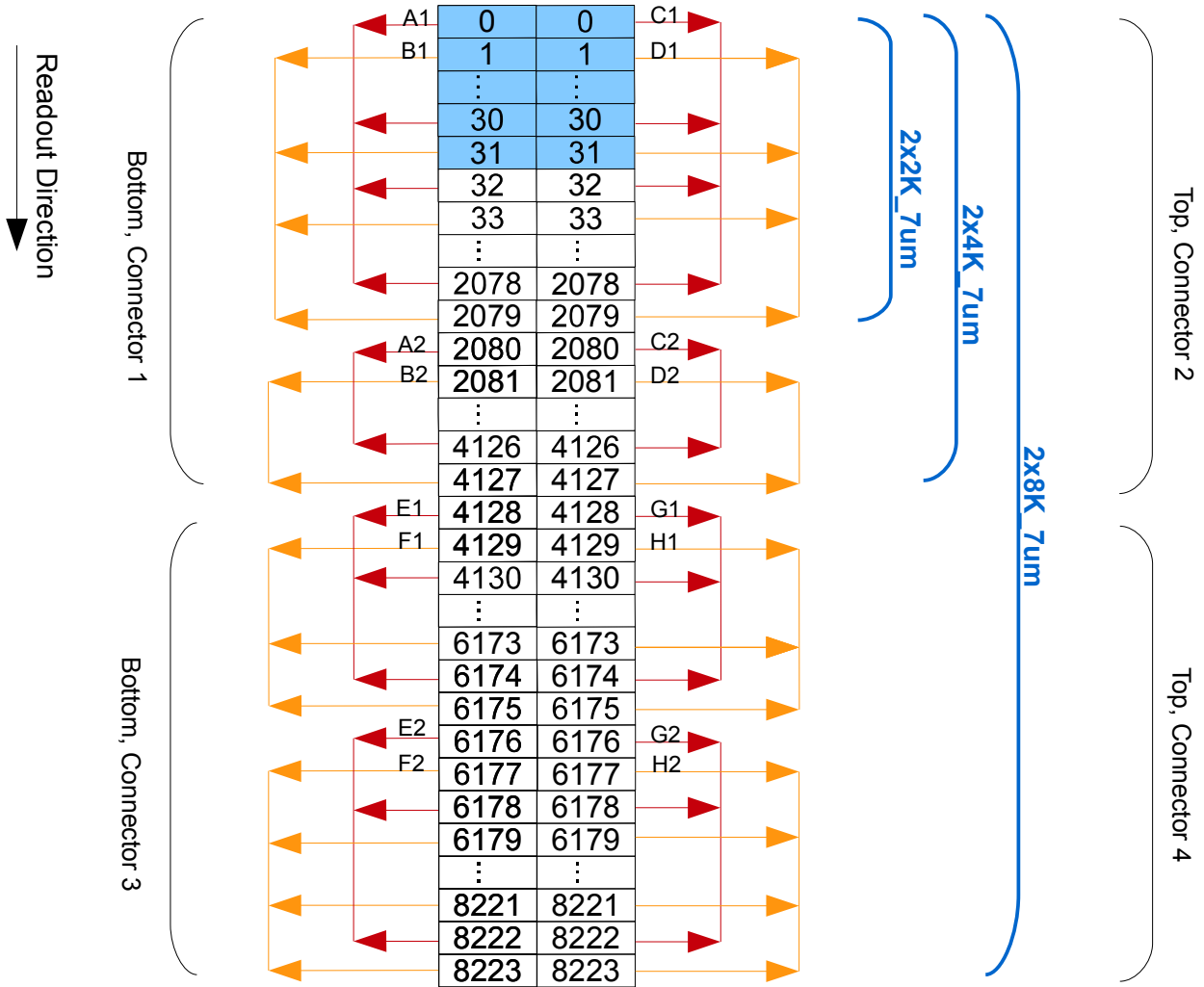


Fig 26: Tap organization DR-2x2k-7, DR-2x4k-7, DR-2x8k-7

9.1.5 Tap organization DR-2x2k-7-RGB, DR-2x4k-7-RGB, DR-2x8k-7-RGB

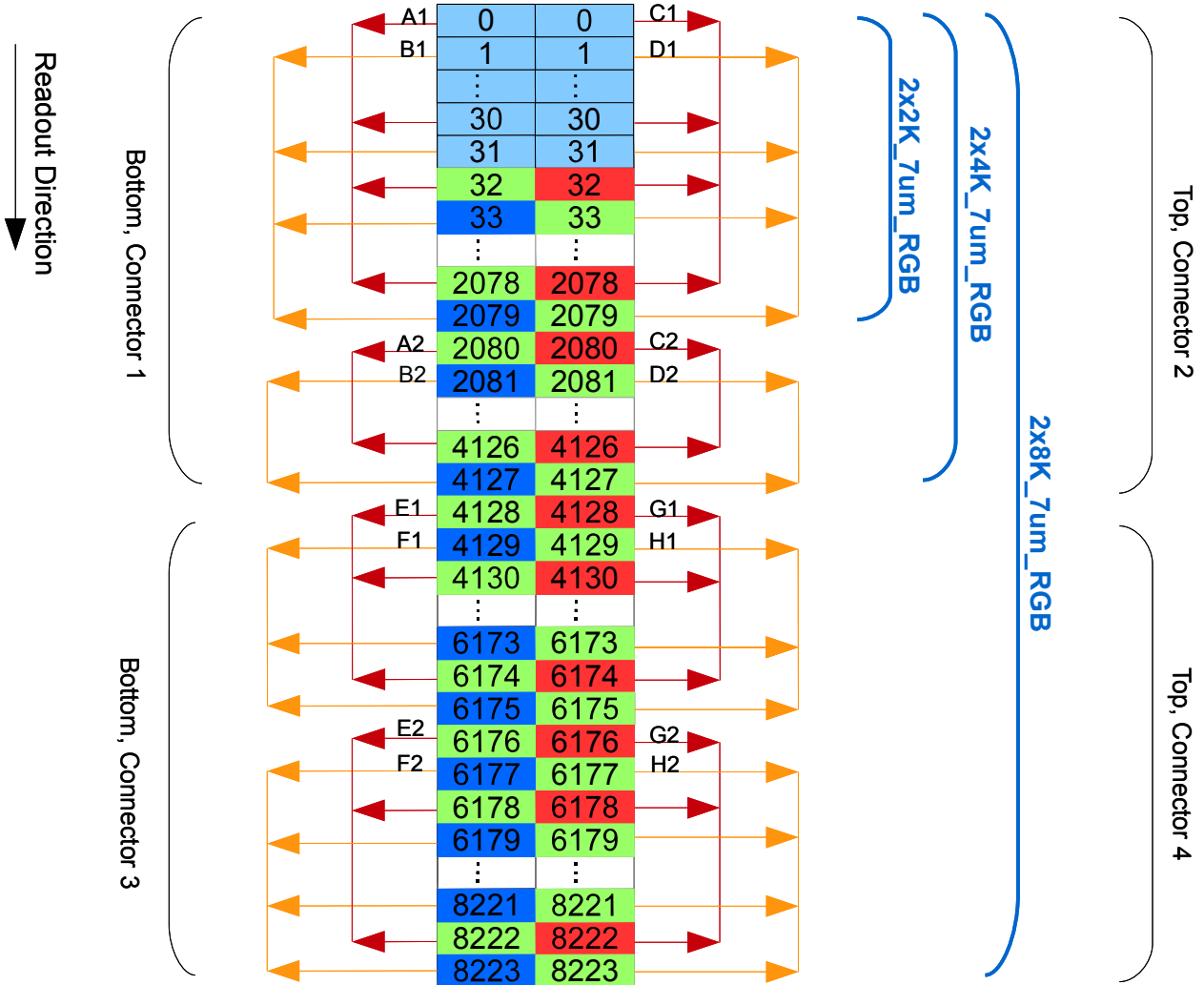


Fig 27: Tag organization DR-2x2k-7-RGB, DR-2x4k-7-RGB, DR-2x8k-7-RGB

10 Packages overview

DRAGSTER sensors are supplied with specific packages developed at Awaiba that are made to bring serious advantages to camera developers. They include years of close development with Awaiba's customers in the most demanding applications.

The available packages are organized in two main types: LCC and INVAR. The LCC is a no lead package where the silicon's carrier is FR4 while the INVAR package uses a special nickel iron alloy as heat dissipation and mechanical reference. While the LCC package is oriented for size, resolution and cost conscious applications the INVAR type is focused on high performance, where highest speed and high resolutions are the main advantages to the field application. All package types take a cover glass over sensor's silicon to protect from external dust particles. Optionally, the sensor can be delivered without cover glass and a globe top protection of bond wires.

For the customer, one of the most obvious advantage of Dragster packages are the use of commercially available connectors or low cost LCC connections. This makes each camera development fast and easy and brings also other advantages: precise mechanical alignment to the optics by taking INVAR as reference and it's CNC machined features, integrated heat dissipation plate that minimizes sensor stress in Z-axis, maximization of sensor performance in speed and noise and easily customizable package to suit any requirement. Furthermost the LCC can also be mounted as a SMD part.

Other packages are possible, like bare die or CSP, so contact AWAIBA if you require a custom package.

| Package | Sensors | Top View | Bottom View |
|---------------------------------------|-----------------------------------|--|---|
| LCC | DR-2K-7 DR-2x2K-7 DR-4K-3.5 |  |  |
| Invar with 1 connector | DR-4K-7 |  |  |
| Invar with 2 connectors | DR-2K-7 DR-2x2K-7 DR-4K-3.5 |  |  |
| | DR-2x4K-7 DR-8K-3.5 |  |  |
| | DR-6K-7 |  |  |
| Invar with 2 connectors in the bottom | DR-8K-7 |  |  |

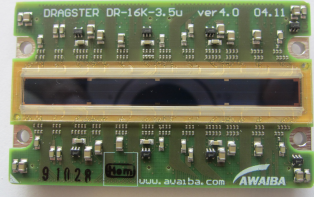
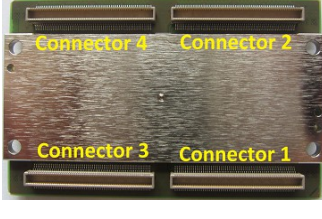
| | | | |
|--------------------------------|---------------------------------|--|---|
| <p>Invar with 4 connectors</p> | <p>DR-2x8K-7 DR-16K-3.5</p> |  |  |
|--------------------------------|---------------------------------|--|---|

Table 13: Package overview

11 Mechanical Drawings

11.1 LCC Package drawings DR2k-7

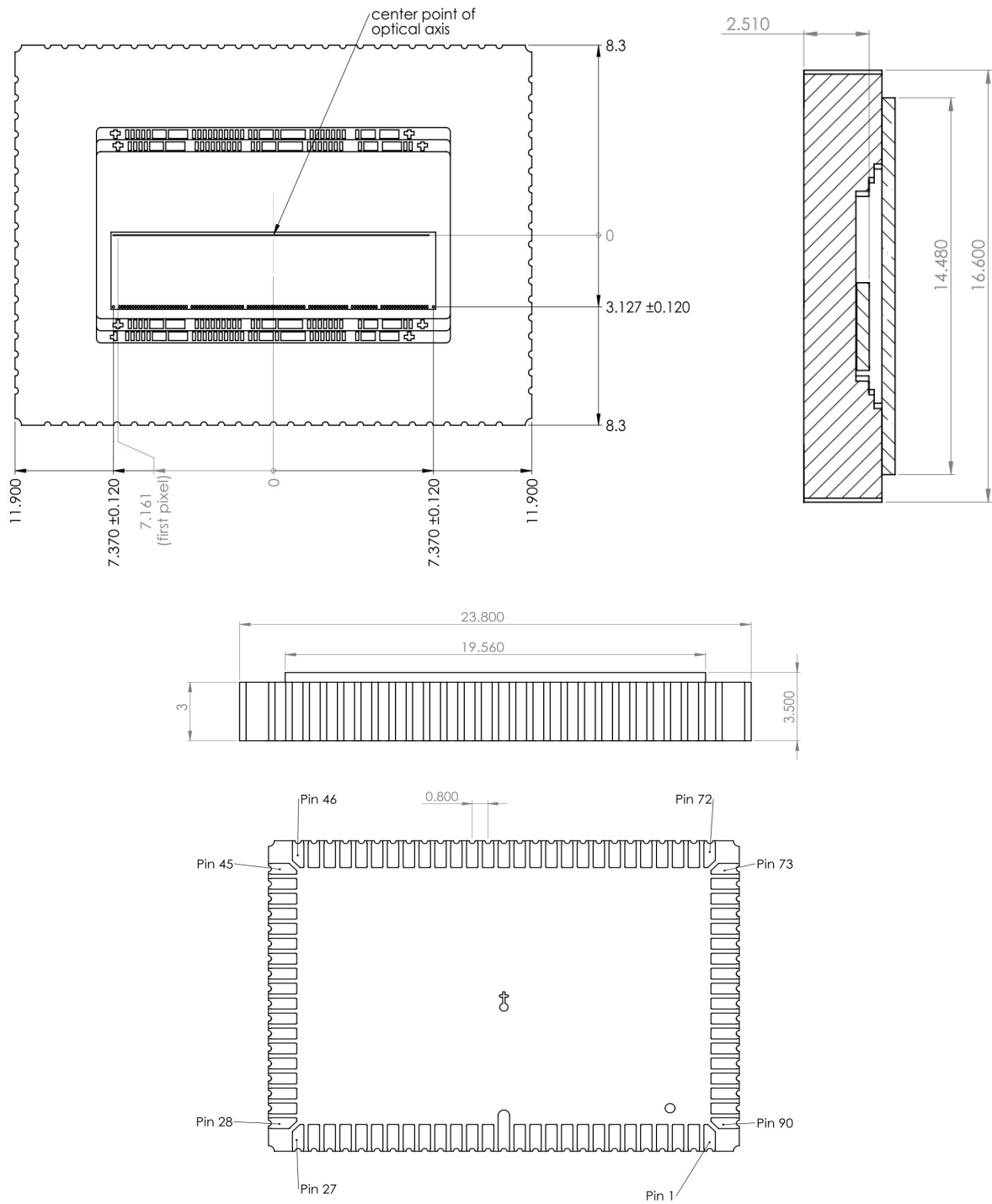


Fig 28: Four Views of LCC Package Drawings for DR2k-7

11.2 LCC package drawings DR2x2k-7, DR4k-3.5

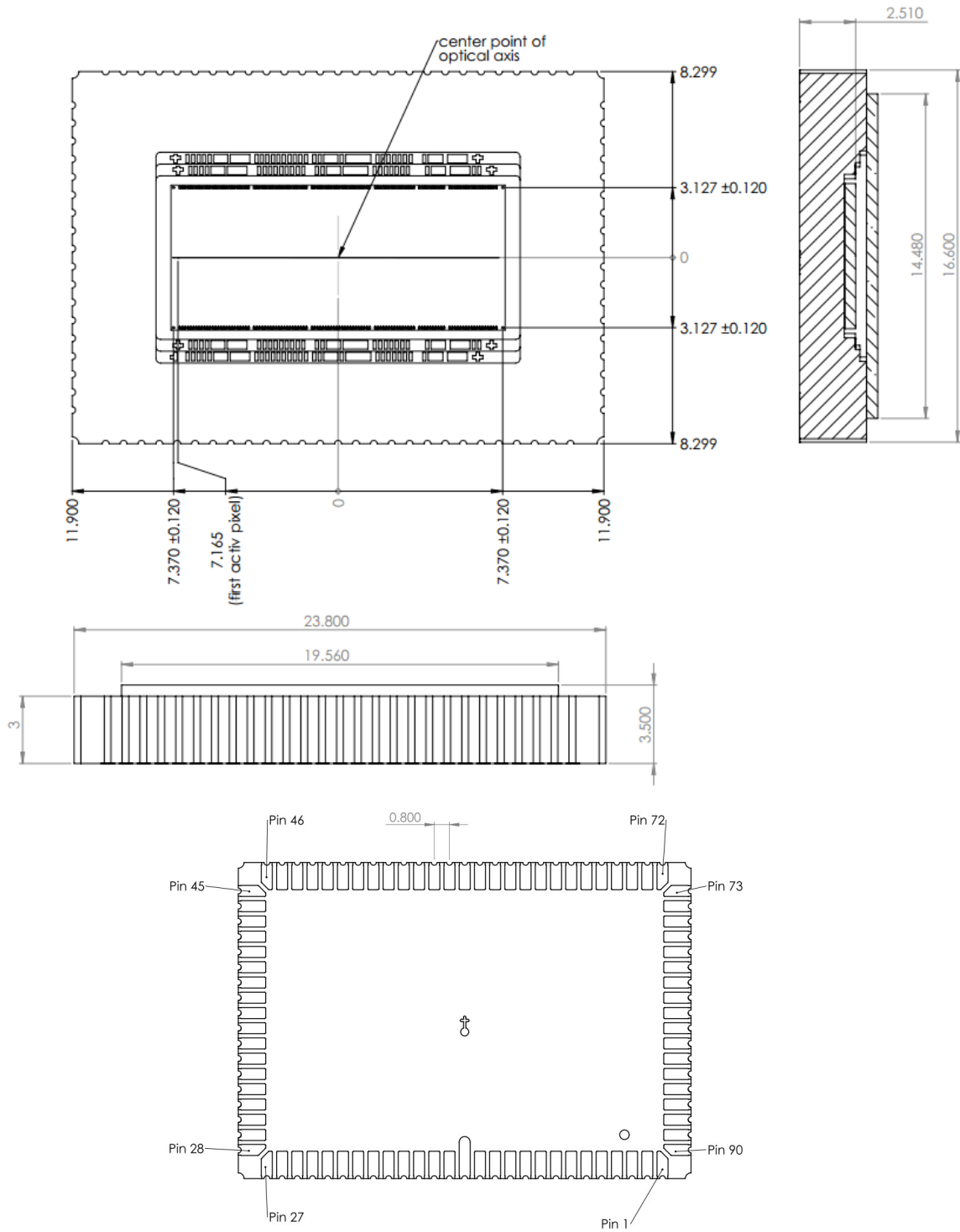


Fig 29: Four Views of LCC Package Drawings for DR2x2k-7 B&W and RGB, DR4k-3.5

11.3 Invar package drawing DR4k-7

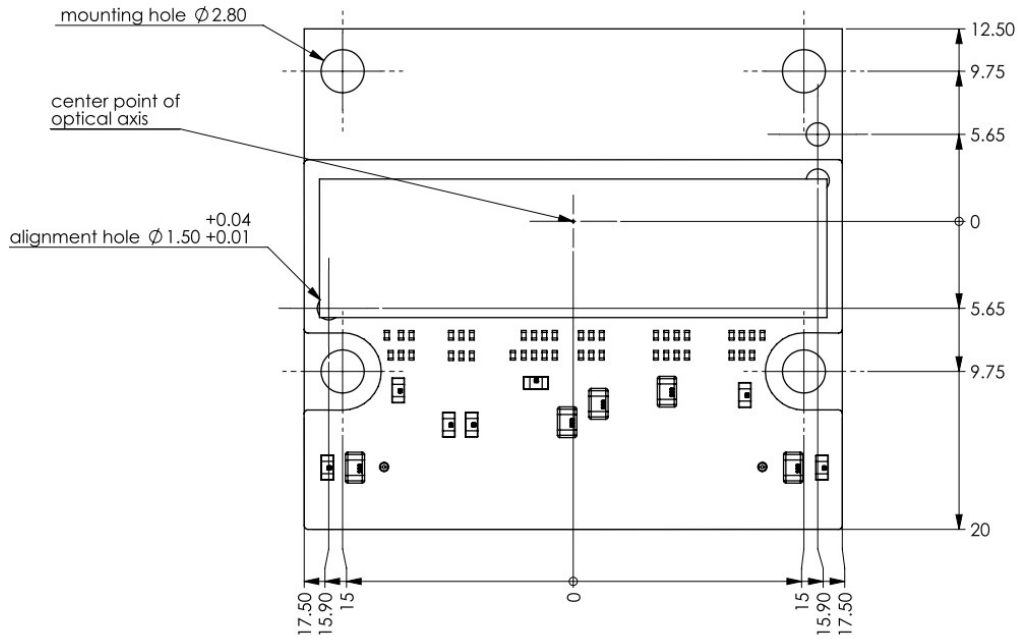


Fig 30: Top view DR-B&W-4k-7-Invar. If not otherwise noted all tolerances are +/- 0.1mm

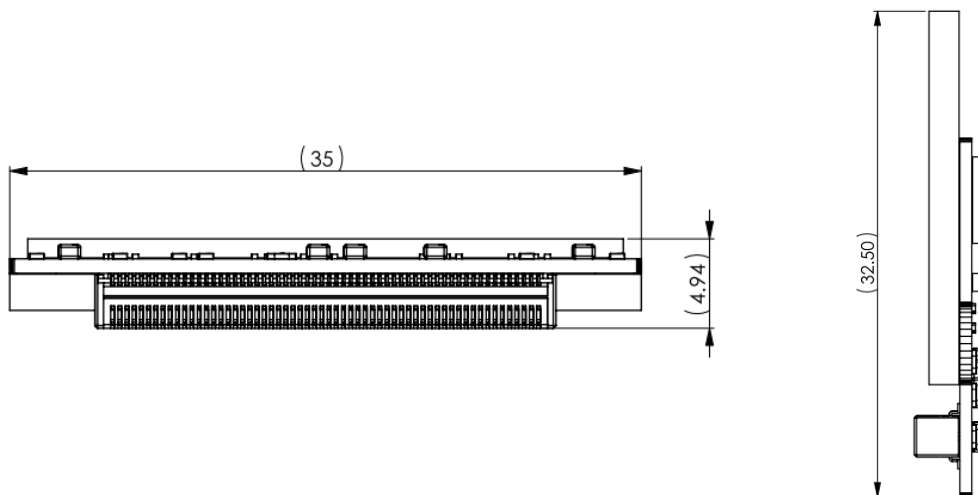


Fig 31: DR-B&W-4k-7-Invar. Tolerance +/- 0.1mm

11.4 Incar package drawing DR-2x4k-7, DR8k-3.5

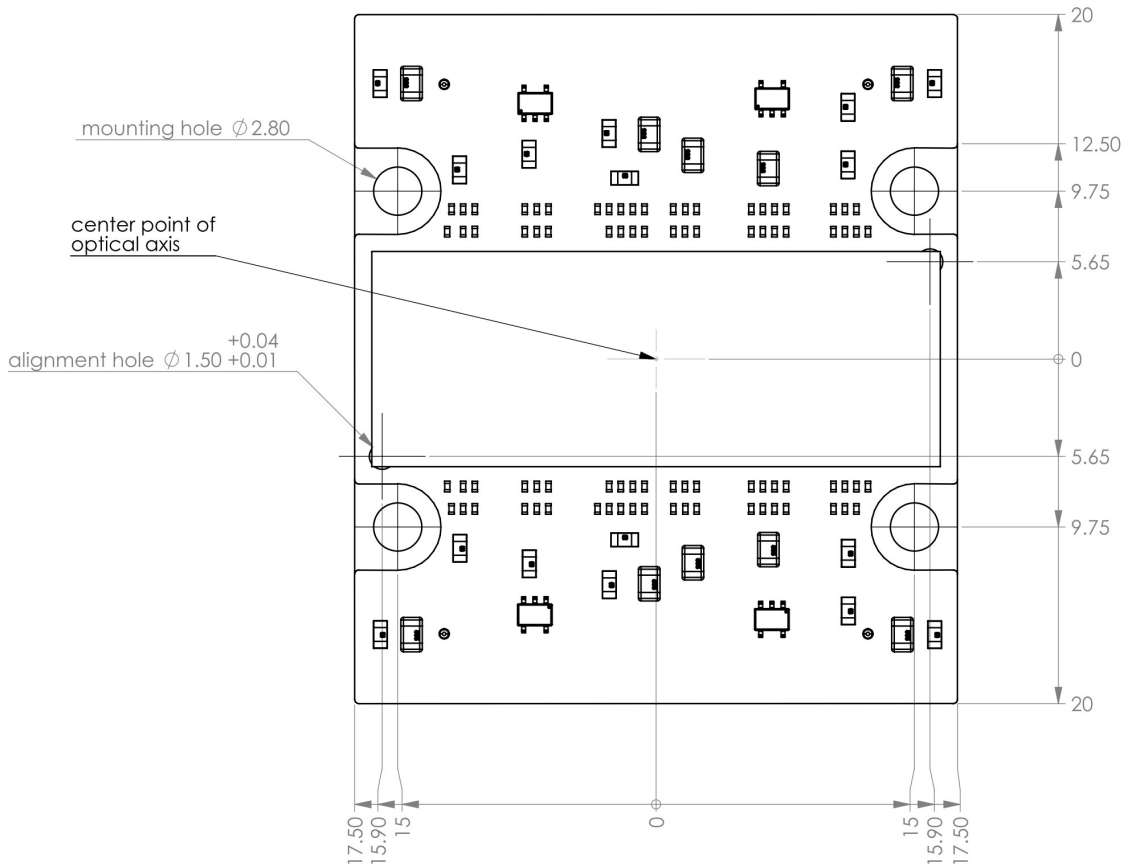


Fig 32: Top view DR-B&W-2x4k-7-Invar and DR-B&W-8K-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm

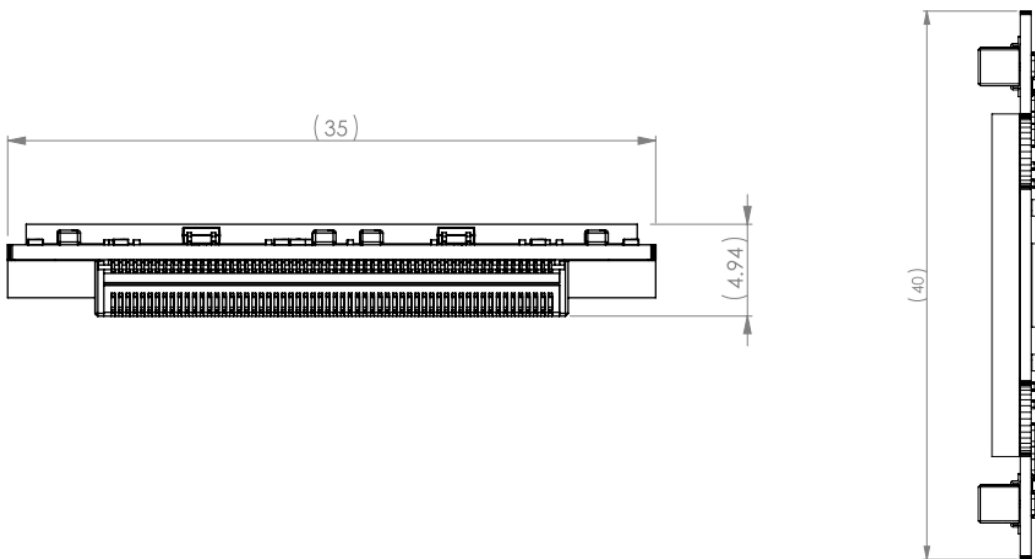


Fig 33: DR-B&W-2x4k-7-Invar, DR-B&W-8K-3.5-Invar. Tolerance +/- 0.1mm

11.5 Invar package drawing DR2k-7, DR2x2k-7, DR4k-3.5

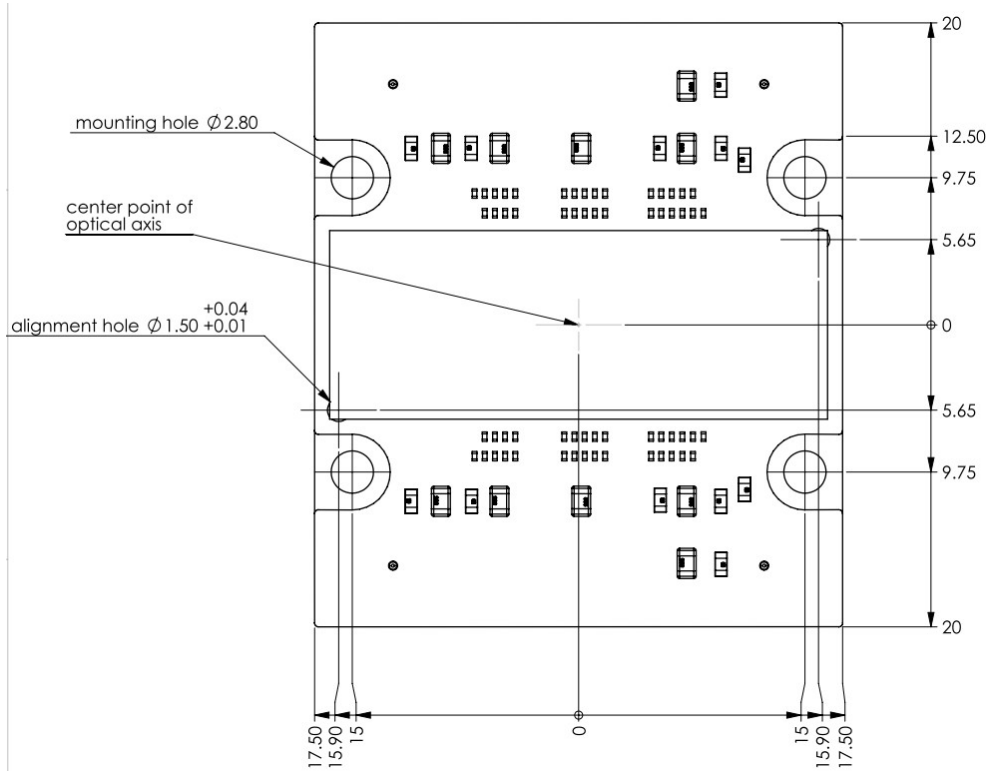


Fig 34: Top view DR-B&W-2k-7-Invar, DR-B&W-2x2k-7-Invar; DR-B&W-4k-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm

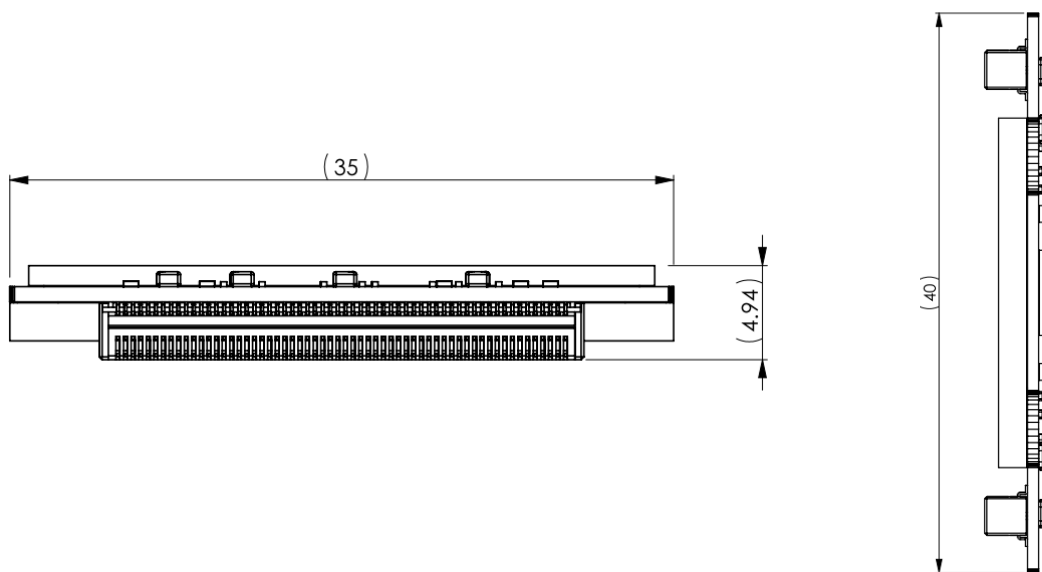


Fig 35: DR-B&W-2k-7-Invar, DR-B&W-2x2k-7-Invar, DR-B&W-4k-3.5-Invar.. Tolerance +/- 0.1mm

11.6 Invar package drawing DR6k-7

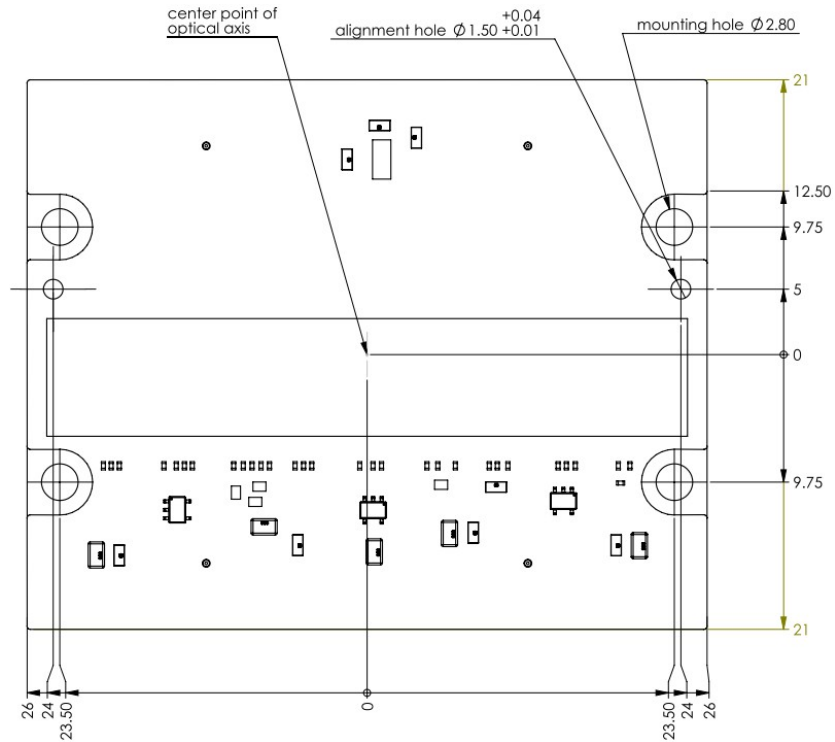


Fig 36: Top view DR-B&W-6k-7-Invar. If not otherwise noted all tolerances are +/- 0.1mm

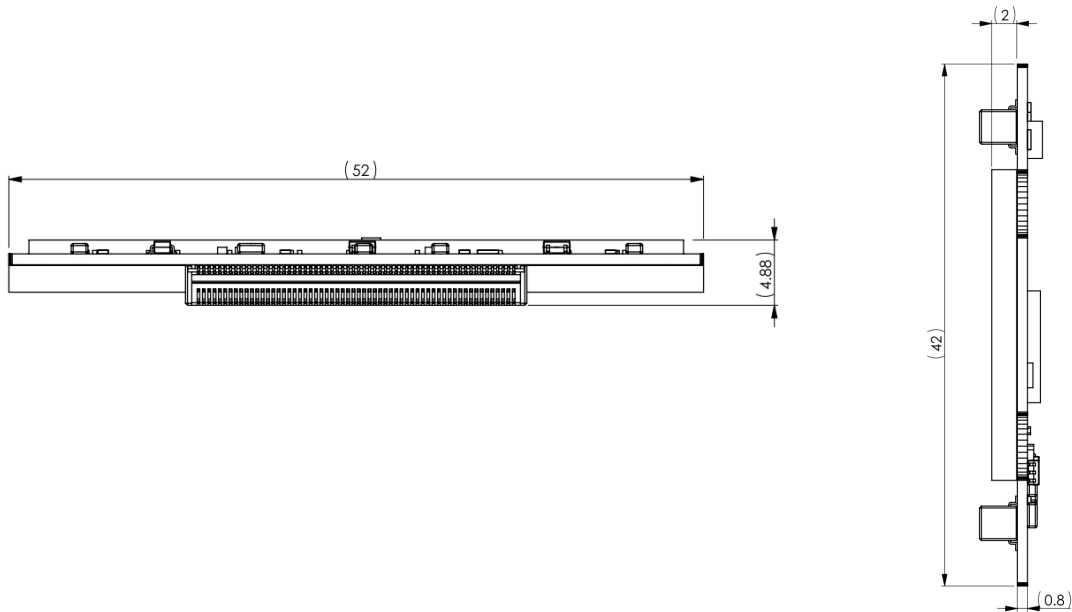


Fig 37: DR-B&W-6k-7-Invar. Tolerance +/- 0.1mm

11.7 Invar package drawing DR8k-7

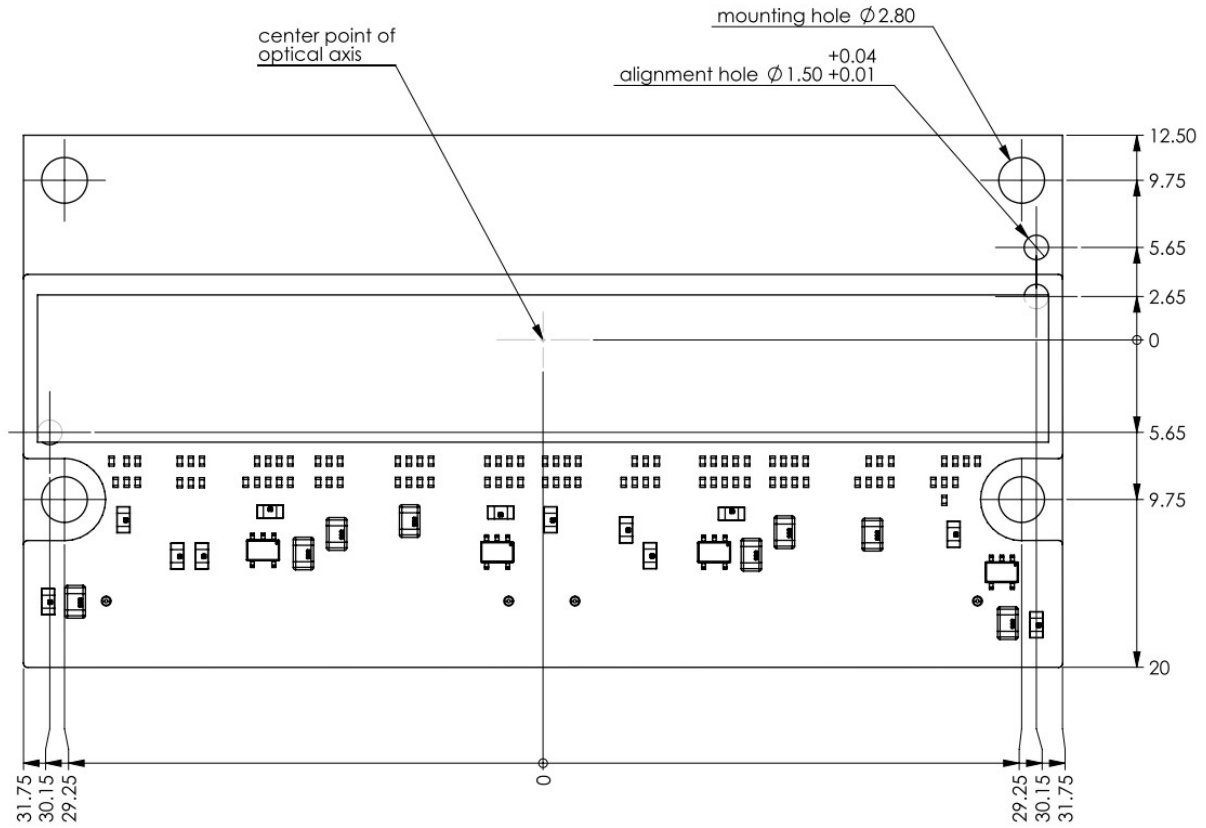


Fig 38: Top view DR-B&W-8k-7-Invar. If not otherwise noted all tolerances are +/- 0.1mm

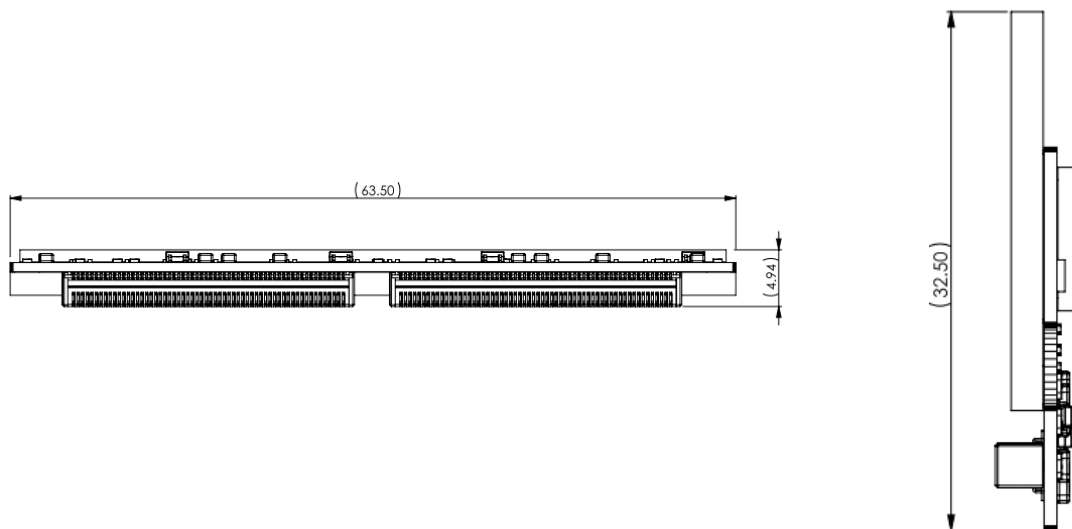


Fig 39: DR-B&W-8k-7-Invar. Tolerance +/- 0.1mm

11.8 Invar package drawing DR-2x8k-7, DR-16k-3.5

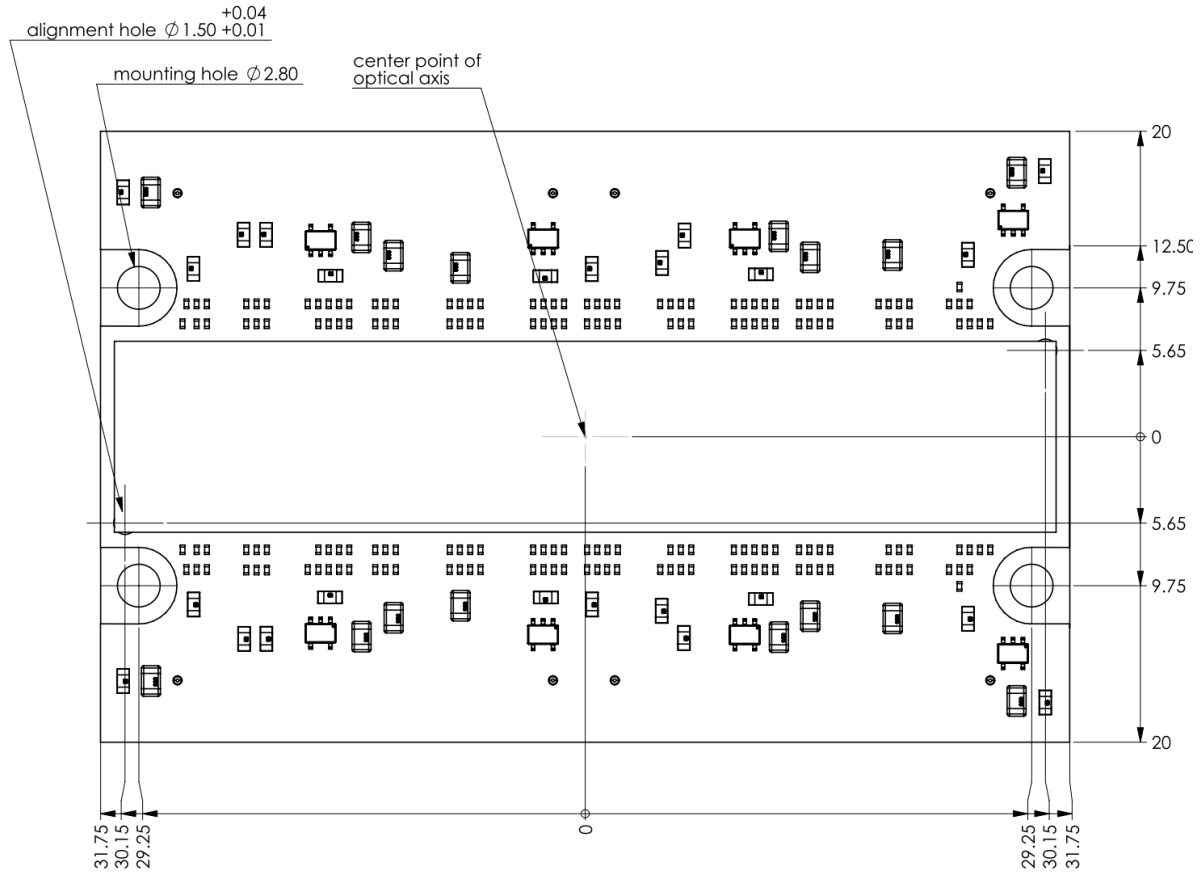


Fig 40: Top view DR-B&W-2x8k-7-Invar and DR-B&W-16k-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm

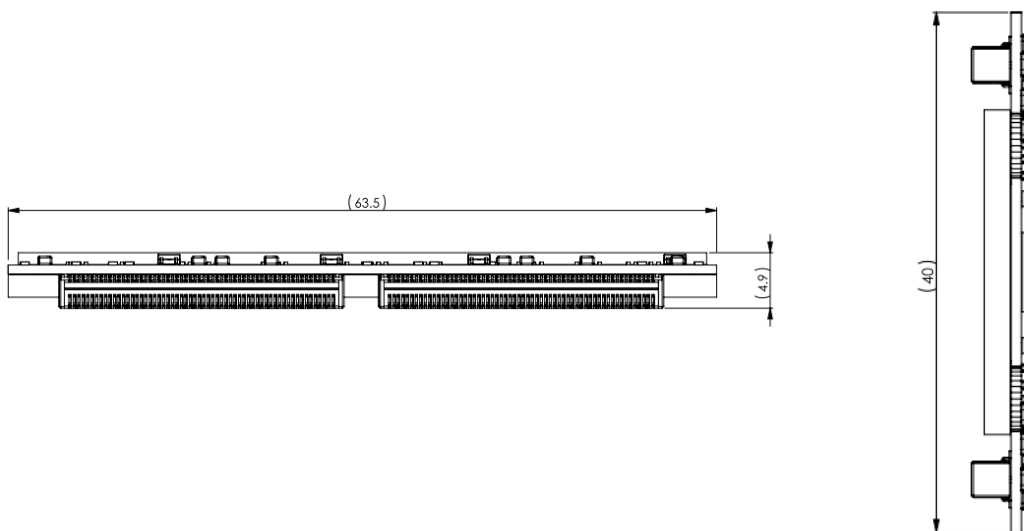


Fig 41: DR-B&W-2x8k-7-Invar, DR-B&W-16k-3.5-Invar. Tolerance +/- 0.1mm

12 Connectors pin outlined

12.1 Pinout DR2k-7-LCC, DR2x2k-7-LCC, DR4k-3.5-LCC

| Pin | Signal Name | Signal Name | Type |
|-----|--------------------------------|---------------------|----------------|
| | DR-4k-3.5-LCC DR-2x2k-7-LCC | DR-2k-7-LCC | |
| 1 | Tap A1 Bit 11 | Tap A1 Bit 11 | Digital Output |
| 2 | Tap A1 Bit 9 | Tap A1 Bit 9 | Digital Output |
| 3 | Tap A1 Bit 7 | Tap A1 Bit 7 | Digital Output |
| 4 | Tap A1 Bit 5 | Tap A1 Bit 5 | Digital Output |
| 5 | Tap A1 Bit 3 | Tap A1 Bit 3 | Digital Output |
| 6 | Tap A1 Bit 1 | Tap A1 Bit 1 | Digital Output |
| 7 | VSS | VSS | Ground |
| 8 | LVAL Tap A1/B1 | LVAL Tap A1/B1 | Digital Output |
| 9 | Tap A1 Bit 12 | Tap A1 Bit 12 | Digital Output |
| 10 | Tap A1 Bit 10 | Tap A1 Bit 10 | Digital Output |
| 11 | Tap A1 Bit 8 | Tap A1 Bit 8 | Digital Output |
| 12 | Tap A1 Bit 6 | Tap A1 Bit 6 | Digital Output |
| 13 | Tap A1 Bit 4 | Tap A1 Bit 4 | Digital Output |
| 14 | Tap A1 Bit 2 | Tap A1 Bit 2 | Digital Output |
| 15 | Tap A1 Bit 0 | Tap A1 Bit 0 | Digital Output |
| 16 | Pixel_CLK_Tap A1/B1 | Pixel_CLK_Tap A1/B1 | Digital Output |
| 17 | END_ADC_TAP A1/B1 | END_ADC_TAP A1/B1 | Digital Output |
| 18 | VSS | VSS | Ground |
| 19 | Tap B1 Bit 1 | Tap B1 Bit 1 | Digital Output |
| 20 | Tap B1 Bit 3 | Tap B1 Bit 3 | Digital Output |
| 21 | Tap B1 Bit 5 | Tap B1 Bit 5 | Digital Output |
| 22 | Tap B1 Bit 7 | Tap B1 Bit 7 | Digital Output |
| 23 | Tap B1 Bit 9 | Tap B1 Bit 9 | Digital Output |
| 24 | Tap B1 Bit 11 | Tap B1 Bit 11 | Digital Output |
| 25 | Tap B1 Bit 0 | Tap B1 Bit 0 | Digital Output |
| 26 | Tap B1 Bit 2 | Tap B1 Bit 2 | Digital Output |

| Pin | Signal Name | Signal Name | Type |
|-----|--------------------------------|---------------|----------------|
| | DR-4k-3.5-LCC DR-2x2k-7-LCC | DR-2k-7-LCC | |
| 27 | Tap B1 Bit 4 | Tap B1 Bit 4 | Digital Output |
| 28 | VSS | VSS | Ground |
| 29 | Tap B1 Bit 6 | Tap B1 Bit 6 | Digital Output |
| 30 | Tap B1 Bit 8 | Tap B1 Bit 8 | Digital Output |
| 31 | Tap B1 Bit 10 | Tap B1 Bit 10 | Digital Output |
| 32 | Tap B1 Bit 12 | Tap B1 Bit 12 | Digital Output |
| 33 | VSS | VSS | Ground |
| 34 | VDDA | VDDA | 3.3V Analogue |
| 35 | VDD | VDD | 3.3V supply |
| 36 | VDD | VDD | 3.3V supply |
| 37 | VDD | VDD | 3.3V supply |
| 38 | VDDA | VDDA | 3.3V Analogue |
| 39 | N_Reset | N_Reset | Digital Input |
| 40 | VSS | Ground | Ground |
| 41 | Tap D1 Bit 12 | Not connected | Digital Output |
| 42 | Tap D1 Bit 10 | Not connected | Digital Output |
| 43 | Tap D1 Bit 8 | Not connected | Digital Output |
| 44 | Tap D1 Bit 6 | Not connected | Digital Output |
| 45 | VSS | VSS | Ground |
| 46 | Tap D1 Bit 4 | Not connected | Digital Output |
| 47 | Tap D1 Bit 2 | Not connected | Digital Output |
| 48 | Tap D1 Bit 0 | Not connected | Digital Output |
| 49 | Tap D1 Bit 11 | Not connected | Digital Output |
| 50 | Tap D1 Bit 9 | Not connected | Digital Output |
| 51 | Tap D1 Bit 7 | Not connected | Digital Output |
| 52 | Tap D1 Bit 5 | Not connected | Digital Output |
| 53 | Tap D1 Bit 3 | Not connected | Digital Output |
| 54 | Tap D1 Bit 1 | Not connected | Digital Output |
| 55 | VSS | Ground | Ground |
| 56 | END_ADC_TAP C1/D1 | Not connected | Digital Output |

| Pin | Signal Name | Signal Name | Type |
|-----|--------------------------------|---------------|----------------|
| | DR-4k-3.5-LCC DR-2x2k-7-LCC | DR-2k-7-LCC | |
| 57 | Pixel_CLK_Tap C1/D1 | Not connected | Digital Output |
| 58 | Tap C1 Bit 0 | Not connected | Digital Output |
| 59 | Tap C1 Bit 2 | Not connected | Digital Output |
| 60 | Tap C1 Bit 4 | Not connected | Digital Output |
| 61 | Tap C1 Bit 6 | Not connected | Digital Output |
| 62 | Tap C1 Bit 8 | Not connected | Digital Output |
| 63 | Tap C1 Bit 10 | Not connected | Digital Output |
| 64 | Tap C1 Bit 12 | Not connected | Digital Output |
| 65 | LVAL Tap C1/D1 | Not connected | Digital Output |
| 66 | VSS | Ground | Ground |
| 67 | MISO C1/D1 | Not connected | Digital Output |
| 68 | Tap C1 Bit 1 | Not connected | Digital Output |
| 69 | Tap C1 Bit 3 | Not connected | Digital Output |
| 70 | Tap C1 Bit 5 | Not connected | Digital Output |
| 71 | Tap C1 Bit 7 | Not connected | Digital Output |
| 72 | Tap C1 Bit 9 | Not connected | Digital Output |
| 73 | VSS | Ground | Ground |
| 74 | Tap C1 Bit 11 | Not connected | Digital Output |
| 75 | RESET_CDS | Digital Input | Digital Input |
| 76 | N_CS C1/D1 | Not connected | Digital Input |
| 77 | MOSI | Digital Input | Digital Input |
| 78 | Main_CLK | Digital Input | Digital Input |
| 79 | Load_Pulse | Digital Input | Digital Input |
| 80 | VSS | Ground | Ground |
| 81 | VDD | 3.3V | 3.3V |
| 82 | VDD | 3.3V | 3.3V |
| 83 | VDDA | VDDA | 3.3V Analogue |
| 84 | VDDA | VDDA | 3.3V Analogue |
| 85 | N_CS A1/B1 | Digital Input | Digital Input |
| 86 | SAMPLE | Digital Input | Digital Input |

| Pin | Signal Name | Signal Name | Type |
|-----|--------------------------------|----------------|----------------|
| | DR-4k-3.5-LCC DR-2x2k-7-LCC | DR-2k-7-LCC | |
| 87 | RST_CVC | Digital Input | Digital Input |
| 88 | SCLK | Digital Input | Digital Input |
| 89 | MISO A1/B1 | Digital Output | Digital Output |
| 90 | VSS | Ground | Ground |

From LCC version v2.0 there is a separation from chip analogue power to other supplies but without separation on GND pins.

12.2 Connectors for different versions of Invar headboard packages

All Dragster modules, have up to 4 Molex connectors with 120 pin and reference 055339-1208.

The below table indicates which connectors are present for the different chip versions.

| Chip version | Present connectors | Connector Reference |
|------------------|---------------------------|---------------------|
| DR-2k-7-LCC | | |
| DR-2x2k-7-LCC | Not applied | ----- |
| DR-4k-3.5-LCC | | |
| DR-4k-7-Invar | Connector 1 | Molex 055339-1208 |
| DR-2k-7-Invar | | |
| DR-2x2k-7-Invar | | |
| DR-4k-3.5-Invar | Connector 1 & Connector 2 | Molex 055339-1208 |
| DR-2x4k-7-Invar | | |
| DR-6k-7-Invar | | |
| DR-8k-3.5-Invar | | |
| DR-8k-7-Invar | Connector 1 & Connector 3 | Molex 055339-1208 |
| DR-2x8k-7-Invar | | |
| DR-16k-3.5-Invar | Connector 1 - 4 | Molex 055339-1208 |

Table 14: Connectors for different chip versions

12.2.1 Connector number identification and pin numbers

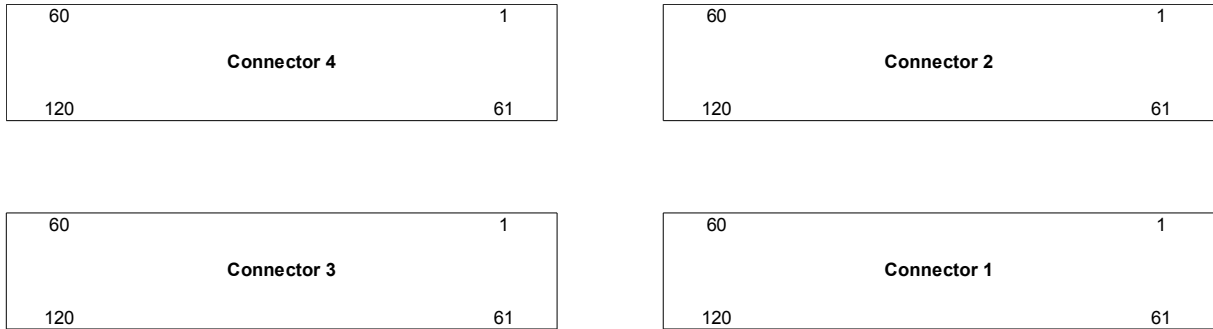


Fig 42: Identification of connector number and pin numbers, DR-16K-3.5 back view

12.3 Connector signal assignment for Invar head board DR-2x2k-7-Invar, DR-4k-3.5-Invar, DR-2k-7-Invar

For DR-2k-7-Invar Connector 2 is present but not required. Only the powers present on the connector are routed to the sensor. Connector 2 can be left completely unconnected for DR-2k-7-Invar.

12.3.1 Connector 1

| Pin Number | Signal Name | Signal Type |
|------------|-----------------|-----------------------------|
| 1 | N_CS_AB_1 | Dig in |
| 2 | MISO_AB_1 | Dig out |
| 3 | VDDA | VDDA |
| 4 | VDDD | VDDD |
| 5 | VSSA | GND |
| 6 | VSS_BULK | GND |
| 7 | VSSD | GND |
| 8 | LOAD_PULSE_AB_1 | Dig in |
| 9 | VDDIO | VDDIO |
| 10 | END_ADC_AB_1 | Dig out |
| 11 | VDDA | VDDA |
| 12 | VDD_BULK | VDD_Bulk |
| 13 | VDDD | VDDD |
| 14 | VDDES | VDDES |
| 15 | VSSA | GND |
| 16 | VSS_BULK | GND |
| 17 | VSSD | GND |
| 18 | VDDIO | VDDIO |
| 19 | TEST_MUX_AB_1 | analogue monitor leave n.c. |
| 20 | VDDA | VDDA |
| 21 | VDDD | VDDD |
| 22 | VSSA | GND |
| 23 | VSS_BULK | GND |
| 24 | VSSD | GND |
| 25 | VSSD/IO | GND |
| 26 | PIXEL_CLK_AB_1 | Dig out |
| 27 | VCLAMP_AB_1 | VDDA |
| 28 | SAMPLE_AB | Dig in |
| 29 | RST_CDS_AB | Dig in |
| 30 | RST_CVC_AB | Dig in |
| 31 | Not Connected | |
| 32 | SCLK_AB_EF | Dig in |
| 33 | MOSI_AB_EF | dig in |
| 34 | Not Connected | |
| 35 | VDDA | VDDA |
| 36 | VDD_BULK | VDD_Bulk |

| Pin Number | Signal Name | Signal Type |
|------------|---------------|-------------|
| 37 | VDDD | VDDD |
| 38 | VDDESD | VDDESD |
| 39 | VSSA | GND |
| 40 | VSS_BULK | GND |
| 41 | VSSD | GND |
| 42 | Not Connected | |
| 43 | VDDIO | VDDIO |
| 44 | Not Connected | |
| 45 | VDDA | VDDA |
| 46 | VDDD | VDDD |
| 47 | VSSA | GND |
| 48 | VSSD | GND |
| 49 | VDDIO | VDDIO |
| 50 | Not Connected | |
| 51 | VDDA | VDDA |
| 52 | VDD_BULK | VDD_Bulk |
| 53 | VDDD | VDDD |
| 54 | VDDESD | VDDESD |
| 55 | VSSA | GND |
| 56 | VSS_BULK | GND |
| 57 | VSSD | GND |
| 58 | N_RESET_AB | Dig in |
| 59 | Not Connected | |
| 60 | Not Connected | |
| 61 | VSSESD/IO | GND |
| 62 | LVAL_AB_1 | Dig out |
| 63 | BIT_12_TAP_A1 | Dig out |
| 64 | BIT_11_TAP_A1 | Dig out |
| 65 | BIT_10_TAP_A1 | Dig out |
| 66 | BIT_09_TAP_A1 | Dig out |
| 67 | BIT_08_TAP_A1 | Dig out |
| 68 | BIT_07_TAP_A1 | Dig out |
| 69 | BIT_06_TAP_A1 | Dig out |
| 70 | BIT_05_TAP_A1 | Dig out |
| 71 | BIT_04_TAP_A1 | Dig out |
| 72 | BIT_03_TAP_A1 | Dig out |
| 73 | BIT_02_TAP_A1 | Dig out |
| 74 | BIT_01_TAP_A1 | Dig out |
| 75 | BIT_00_TAP_A1 | Dig out |
| 76 | VSSESD/IO | GND |
| 77 | BIT_00_TAP_B1 | Dig out |
| 78 | BIT_01_TAP_B1 | Dig out |
| 79 | BIT_02_TAP_B1 | Dig out |
| 80 | BIT_03_TAP_B1 | Dig out |
| 81 | BIT_04_TAP_B1 | Dig out |
| 82 | BIT_05_TAP_B1 | Dig out |
| 83 | BIT_06_TAP_B1 | Dig out |
| 84 | BIT_07_TAP_B1 | Dig out |

| | | |
|-----|---------------|---------|
| 85 | BIT_08_TAP_B1 | Dig out |
| 86 | BIT_09_TAP_B1 | Dig out |
| 87 | BIT_10_TAP_B1 | Dig out |
| 88 | BIT_11_TAP_B1 | Dig out |
| 89 | BIT_12_TAP_B1 | Dig out |
| 90 | MAIN_CLK | Dig in |
| 91 | VSSSED/IO | GND |
| 92 | Not Connected | |
| 93 | Not Connected | |
| 94 | Not Connected | |
| 95 | Not Connected | |
| 96 | Not Connected | |
| 97 | Not Connected | |
| 98 | Not Connected | |
| 99 | Not Connected | |
| 100 | Not Connected | |
| 101 | Not Connected | |
| 102 | Not Connected | |
| 103 | Not Connected | |
| 104 | Not Connected | |
| 105 | Not Connected | |
| 106 | VSSSED/IO | GND |
| 107 | Not Connected | |
| 108 | Not Connected | |
| 109 | Not Connected | |
| 110 | Not Connected | |
| 111 | Not Connected | |
| 112 | Not Connected | |
| 113 | Not Connected | |
| 114 | Not Connected | |
| 115 | Not Connected | |
| 116 | Not Connected | |
| 117 | Not Connected | |
| 118 | Not Connected | |
| 119 | Not Connected | |
| 120 | VSSSED/IO | GND |



Note: SCLK and MOSI are connected between connector 1 and connector 3 in the headboard, resulting names are SCLK_AB_EF and MOSI_AB_EF. User just needs to provide the headboard one pair of this signals to connector 1 or 3 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

12.3.2 Connector 2

| Pin Number | Signal Name | Signal Type |
|------------|---------------|-------------|
| 1 | VSSESD/IO | GND |
| 2 | LVAL_CD_1 | Dig out |
| 3 | BIT_12_TAP_C1 | Dig out |
| 4 | BIT_11_TAP_C1 | Dig out |
| 5 | BIT_10_TAP_C1 | Dig out |
| 6 | BIT_09_TAP_C1 | Dig out |
| 7 | BIT_08_TAP_C1 | Dig out |
| 8 | BIT_07_TAP_C1 | Dig out |
| 9 | BIT_06_TAP_C1 | Dig out |
| 10 | BIT_05_TAP_C1 | Dig out |
| 11 | BIT_04_TAP_C1 | Dig out |
| 12 | BIT_03_TAP_C1 | Dig out |
| 13 | BIT_02_TAP_C1 | Dig out |
| 14 | BIT_01_TAP_C1 | Dig out |
| 15 | BIT_00_TAP_C1 | Dig out |
| 16 | VSSESD/IO | GND |
| 17 | BIT_00_TAP_D1 | Dig out |
| 18 | BIT_01_TAP_D1 | Dig out |
| 19 | BIT_02_TAP_D1 | Dig out |
| 20 | BIT_03_TAP_D1 | Dig out |
| 21 | BIT_04_TAP_D1 | Dig out |
| 22 | BIT_05_TAP_D1 | Dig out |
| 23 | BIT_06_TAP_D1 | Dig out |
| 24 | BIT_07_TAP_D1 | Dig out |
| 25 | BIT_08_TAP_D1 | Dig out |
| 26 | BIT_09_TAP_D1 | Dig out |
| 27 | BIT_10_TAP_D1 | Dig out |
| 28 | BIT_11_TAP_D1 | Dig out |
| 29 | BIT_12_TAP_D1 | Dig out |
| 30 | Not Connected | |
| 31 | VSSESD/IO | GND |
| 32 | Not Connected | |
| 33 | Not Connected | |
| 34 | Not Connected | |
| 35 | Not Connected | |
| 36 | Not Connected | |
| 37 | Not Connected | |
| 38 | Not Connected | |
| 39 | Not Connected | |
| 40 | Not Connected | |
| 41 | Not Connected | |
| 42 | Not Connected | |
| 43 | Not Connected | |
| 44 | Not Connected | |
| 45 | Not Connected | |
| 46 | VSSESD/IO | GND |

| | | |
|----|-----------------|-----------------------------|
| 47 | Not Connected | |
| 48 | Not Connected | |
| 49 | Not Connected | |
| 50 | Not Connected | |
| 51 | Not Connected | |
| 52 | Not Connected | |
| 53 | Not Connected | |
| 54 | Not Connected | |
| 55 | Not Connected | |
| 56 | Not Connected | |
| 57 | Not Connected | |
| 58 | Not Connected | |
| 59 | Not Connected | |
| 60 | VSSED/IO | GND |
| 61 | N_CS_CD_1 | Dig in |
| 62 | MISO_CD_1 | Dig out |
| 63 | VDDA | VDDA |
| 64 | VDDD | VDDD |
| 65 | VSSA | GND |
| 66 | VSS_BULK | GND |
| 67 | VSSD | GND |
| 68 | LOAD_PULSE_CD_1 | Dig in |
| 69 | VDDIO | VDDIO |
| 70 | END_ADC_CD_1 | Dig out |
| 71 | VDDA | VDDA |
| 72 | VDD_BULK | VDD_Bulk |
| 73 | VDDD | VDDD |
| 74 | VDDES | VDDES |
| 75 | VSSA | GND |
| 76 | VSS_BULK | GND |
| 77 | VSSD | GND |
| 78 | VDDIO | VDDIO |
| 79 | TEST_MUX_CD_1 | analogue monitor leave n.c. |
| 80 | VDDA | VDDA |
| 81 | VDDD | VDDD |
| 82 | VSSA | GND |
| 83 | VSS_BULK | GND |
| 84 | VSSD | GND |
| 85 | VSSED/IO | GND |
| 86 | PIXEL_CLK_CD_1 | Dig out |
| 87 | VCLAMP_CD_1 | VDDA |
| 88 | SAMPLE_CD | Dig in |
| 89 | RST_CDS_CD | Dig in |
| 90 | RST_CVC_CD | Dig in |
| 91 | Not Connected | |
| 92 | SCLK_CD_GH | Dig in |
| 93 | MOSI_CD_GH | Dig in |
| 94 | Not Connected | |
| 95 | VDDA | VDDA |
| 96 | VDD_BULK | VDD_Bulk |

| Pin Number | Signal Name | Signal Type |
|------------|---------------|-------------|
| 97 | VDDD | VDDD |
| 98 | VDDES | VDDES |
| 99 | VSSA | GND |
| 100 | VSS_BULK | GND |
| 101 | VSSD | GND |
| 102 | Not Connected | |
| 103 | VDDIO | VDDIO |
| 104 | Not Connected | |
| 105 | VDDA | VDDA |
| 106 | VDDD | VDDD |
| 107 | VSSA | GND |
| 108 | VSSD | GND |
| 109 | VDDIO | VDDIO |
| 110 | Not Connected | |
| 111 | VDDA | VDDA |
| 112 | VDD_BULK | VDD Bulk |
| 113 | VDDD | VDDD |
| 114 | VDDES | VDDES |
| 115 | VSSA | GND |
| 116 | VSS_BULK | GND |
| 117 | VSSD | GND |
| 118 | N_RESET_CD | Dig in |
| 119 | Not Connected | |
| 120 | Not Connected | |



Note: SCLK and MOSI are connected between connector 2 and connector 4 in the headboard, resulting names are SCLK_CD_GH and MOSI_CD_GH. The user just need to provide to the headboard one pair of this signals to connector 2 or 4 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

12.4 Connector signal assignment for Invar head board variations DR-4k-7, DR-8k-7, DR-8k-3.5, DR-16k-3.5, DR-2x4k-7, DR-2x8k-7

The signal assignment for all Invar type headboards is identical, though for smaller chip versions some connectors may not be present. The pin numbers are cyclic, when looking on the connector form the connector side right to left.

12.4.1 Connector 1

| Pin Number | Signal Name | Signal Type |
|------------|-----------------|-----------------------------|
| 1 | N_CS_AB_1 | Dig in |
| 2 | MISO_AB_1 | Dig out |
| 3 | VDDA | VDDA |
| 4 | VDDD | VDDD |
| 5 | VSSA | GND |
| 6 | VSS_BULK | GND |
| 7 | VSSD | GND |
| 8 | LOAD_PULSE_AB_1 | Dig in |
| 9 | VDDIO | VDDIO |
| 10 | END_ADC_AB_1 | Dig out |
| 11 | VDDA | VDDA |
| 12 | VDD_BULK | VDD_Bulk |
| 13 | VDDD | VDDD |
| 14 | VDDESD | VDDESD |
| 15 | VSSA | GND |
| 16 | VSS_BULK | GND |
| 17 | VSSD | GND |
| 18 | VDDIO | VDDIO |
| 19 | TEST_MUX_AB_1 | analogue monitor leave n.c. |
| 20 | VDDA | VDDA |
| 21 | VDDD | VDDD |
| 22 | VSSA | GND |
| 23 | VSS_BULK | GND |
| 24 | VSSD | GND |
| 25 | VSSESD/IO | GND |
| 26 | PIXEL_CLK_AB_1 | Dig_out |
| 27 | VCLAMP_AB_1 | VDDA |
| 28 | SAMPLE_AB | Dig in |
| 29 | RST_CDS_AB | Dig in |
| 30 | RST_CVC_AB | Dig in |
| 31 | N_CS_AB_2 | Dig in |
| 32 | SCLK_AB_EF | Dig in |
| 33 | MOSI_AB_EF | dig in |
| 34 | MISO_AB_2 | Dig out |
| 35 | VDDA | VDDA |
| 36 | VDD_BULK | VDD_Bulk |
| 37 | VDDD | VDDD |
| 38 | VDDESD | VDDESD |

| Pin Number | Signal Name | Signal Type |
|------------|------------------|-----------------------------|
| 39 | VSSA | GND |
| 40 | VSS_BULK | GND |
| 41 | VSSD | GND |
| 42 | LOAD_PULSE_AB_2 | Dig in |
| 43 | VDDIO | VDDIO |
| 44 | END_ADC_AB_2 | Dig out |
| 45 | VDDA | VDDA |
| 46 | VDDD | VDDD |
| 47 | VSSA | GND |
| 48 | VSSD | GND |
| 49 | VDDIO | VDDIO |
| 50 | TEST_MUX_AB_2 | analogue monitor leave n.c. |
| 51 | VDDA | VDDA |
| 52 | VDD_BULK | VDD_Bulk |
| 53 | VDDD | VDDD |
| 54 | VDDES | VDDES |
| 55 | VSSA | GND |
| 56 | VSS_BULK | GND |
| 57 | VSSD | GND |
| 58 | N_RESET_AB | Dig in |
| 59 | PIXEL_CLOCK_AB_2 | Dig out |
| 60 | VCLAMP_AB_2 | VDDA |
| 61 | VSSD/IO | GND |
| 62 | LVAL_AB_1 | Dig out |
| 63 | BIT_12_TAP_A1 | Dig out |
| 64 | BIT_11_TAP_A1 | Dig out |
| 65 | BIT_10_TAP_A1 | Dig out |
| 66 | BIT_09_TAP_A1 | Dig out |
| 67 | BIT_08_TAP_A1 | Dig out |
| 68 | BIT_07_TAP_A1 | Dig out |
| 69 | BIT_06_TAP_A1 | Dig out |
| 70 | BIT_05_TAP_A1 | Dig out |
| 71 | BIT_04_TAP_A1 | Dig out |
| 72 | BIT_03_TAP_A1 | Dig out |
| 73 | BIT_02_TAP_A1 | Dig out |
| 74 | BIT_01_TAP_A1 | Dig out |
| 75 | BIT_00_TAP_A1 | Dig out |
| 76 | VSSD/IO | GND |
| 77 | BIT_00_TAP_B1 | Dig out |
| 78 | BIT_01_TAP_B1 | Dig out |
| 79 | BIT_02_TAP_B1 | Dig out |
| 80 | BIT_03_TAP_B1 | Dig out |
| 81 | BIT_04_TAP_B1 | Dig out |
| 82 | BIT_05_TAP_B1 | Dig out |
| 83 | BIT_06_TAP_B1 | Dig out |
| 84 | BIT_07_TAP_B1 | Dig out |
| 85 | BIT_08_TAP_B1 | Dig out |
| 86 | BIT_09_TAP_B1 | Dig out |

| | | |
|-----|---------------|---------|
| 87 | BIT_10_TAP_B1 | Dig out |
| 88 | BIT_11_TAP_B1 | Dig out |
| 89 | BIT_12_TAP_B1 | Dig out |
| 90 | MAIN_CLK | Dig in |
| 91 | VSSSED/IO | GND |
| 92 | LVAL_AB_2 | Dig out |
| 93 | BIT_12_TAP_A2 | Dig out |
| 94 | BIT_11_TAP_A2 | Dig out |
| 95 | BIT_10_TAP_A2 | Dig out |
| 96 | BIT_09_TAP_A2 | Dig out |
| 97 | BIT_08_TAP_A2 | Dig out |
| 98 | BIT_07_TAP_A2 | Dig out |
| 99 | BIT_06_TAP_A2 | Dig out |
| 100 | BIT_05_TAP_A2 | Dig out |
| 101 | BIT_04_TAP_A2 | Dig out |
| 102 | BIT_03_TAP_A2 | Dig out |
| 103 | BIT_02_TAP_A2 | Dig out |
| 104 | BIT_01_TAP_A2 | Dig out |
| 105 | BIT_00_TAP_A2 | Dig out |
| 106 | VSSSED/IO | GND |
| 107 | BIT_00_TAP_B2 | Dig out |
| 108 | BIT_01_TAP_B2 | Dig out |
| 109 | BIT_02_TAP_B2 | Dig out |
| 110 | BIT_03_TAP_B2 | Dig out |
| 111 | BIT_04_TAP_B2 | Dig out |
| 112 | BIT_05_TAP_B2 | Dig out |
| 113 | BIT_06_TAP_B2 | Dig out |
| 114 | BIT_07_TAP_B2 | Dig out |
| 115 | BIT_08_TAP_B2 | Dig out |
| 116 | BIT_09_TAP_B2 | Dig out |
| 117 | BIT_10_TAP_B2 | Dig out |
| 118 | BIT_11_TAP_B2 | Dig out |
| 119 | BIT_12_TAP_B2 | Dig out |
| 120 | VSSSED/IO | GND |



Note: SCLK and MOSI are connected between connector 1 and connector 3 in the headboard, resulting names are SCLK_AB_EF and MOSI_AB_EF. User just need to provide to the headboard one pair of this signals to connector 1 or 3 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

12.4.2 Connector 2

| Pin Number | Signal Name | Signal Type |
|------------|---------------|---------------|
| 1 | VSSED/IO | GND |
| 2 | LVAL_CD_1 | Dig out |
| 3 | BIT_12_TAP_C1 | Dig out |
| 4 | BIT_11_TAP_C1 | Dig out |
| 5 | BIT_10_TAP_C1 | Dig out |
| 6 | BIT_09_TAP_C1 | Dig out |
| 7 | BIT_08_TAP_C1 | Dig out |
| 8 | BIT_07_TAP_C1 | Dig out |
| 9 | BIT_06_TAP_C1 | Dig out |
| 10 | BIT_05_TAP_C1 | Dig out |
| 11 | BIT_04_TAP_C1 | Dig out |
| 12 | BIT_03_TAP_C1 | Dig out |
| 13 | BIT_02_TAP_C1 | Dig out |
| 14 | BIT_01_TAP_C1 | Dig out |
| 15 | BIT_00_TAP_C1 | Dig out |
| 16 | VSSED/IO | GND |
| 17 | BIT_00_TAP_D1 | Dig out |
| 18 | BIT_01_TAP_D1 | Dig out |
| 19 | BIT_02_TAP_D1 | Dig out |
| 20 | BIT_03_TAP_D1 | Dig out |
| 21 | BIT_04_TAP_D1 | Dig out |
| 22 | BIT_05_TAP_D1 | Dig out |
| 23 | BIT_06_TAP_D1 | Dig out |
| 24 | BIT_07_TAP_D1 | Dig out |
| 25 | BIT_08_TAP_D1 | Dig out |
| 26 | BIT_09_TAP_D1 | Dig out |
| 27 | BIT_10_TAP_D1 | Dig out |
| 28 | BIT_11_TAP_D1 | Dig out |
| 29 | BIT_12_TAP_D1 | Dig out |
| 30 | NC | not connected |
| 31 | VSSED/IO | GND |
| 32 | LVAL_CD_2 | Dig out |
| 33 | BIT_12_TAP_C2 | Dig out |
| 34 | BIT_11_TAP_C2 | Dig out |
| 35 | BIT_10_TAP_C2 | Dig out |
| 36 | BIT_09_TAP_C2 | Dig out |
| 37 | BIT_08_TAP_C2 | Dig out |
| 38 | BIT_07_TAP_C2 | Dig out |
| 39 | BIT_06_TAP_C2 | Dig out |
| 40 | BIT_05_TAP_C2 | Dig out |
| 41 | BIT_04_TAP_C2 | Dig out |
| 42 | BIT_03_TAP_C2 | Dig out |
| 43 | BIT_02_TAP_C2 | Dig out |
| 44 | BIT_01_TAP_C2 | Dig out |
| 45 | BIT_00_TAP_C2 | Dig out |
| 46 | VSSED/IO | GND |

| Pin Number | Signal Name | Signal Type |
|------------|-----------------|-----------------------------|
| 47 | BIT_00_TAP_D2 | Dig out |
| 48 | BIT_01_TAP_D2 | Dig out |
| 49 | BIT_02_TAP_D2 | Dig out |
| 50 | BIT_03_TAP_D2 | Dig out |
| 51 | BIT_04_TAP_D2 | Dig out |
| 52 | BIT_05_TAP_D2 | Dig out |
| 53 | BIT_06_TAP_D2 | Dig out |
| 54 | BIT_07_TAP_D2 | Dig out |
| 55 | BIT_08_TAP_D2 | Dig out |
| 56 | BIT_09_TAP_D2 | Dig out |
| 57 | BIT_10_TAP_D2 | Dig out |
| 58 | BIT_11_TAP_D2 | Dig out |
| 59 | BIT_12_TAP_D2 | Dig out |
| 60 | VSSED/IO | GND |
| 61 | N_CS_CD_1 | Dig in |
| 62 | MISO_CD_1 | Dig out |
| 63 | VDDA | VDDA |
| 64 | VDDD | VDDD |
| 65 | VSSA | GND |
| 66 | VSS_BULK | GND |
| 67 | VSSD | GND |
| 68 | LOAD_PULSE_CD_1 | Dig in |
| 69 | VDDIO | VDDIO |
| 70 | END_ADC_CD_1 | Dig out |
| 71 | VDDA | VDDA |
| 72 | VDD_BULK | VDD_Bulk |
| 73 | VDDD | VDDD |
| 74 | VDDES | VDDES |
| 75 | VSSA | GND |
| 76 | VSS_BULK | GND |
| 77 | VSSD | GND |
| 78 | VDDIO | VDDIO |
| 79 | TEST_MUX_CD_1 | analogue monitor leave n.c. |
| 80 | VDDA | VDDA |
| 81 | VDDD | VDDD |
| 82 | VSSA | GND |
| 83 | VSS_BULK | GND |
| 84 | VSSD | GND |
| 85 | VSSED/IO | GND |
| 86 | PIXEL_CLK_CD_1 | Dig_out |
| 87 | VCLAMP_CD_1 | VDDA |
| 88 | SAMPLE_CD | Dig in |
| 89 | RST_CDS_CD | Dig in |
| 90 | RST_CVC_CD | Dig in |
| 91 | N_CS_CD_2 | Dig in |
| 92 | SCLK_CD_GH | Dig in |
| 93 | MOSI_CD_GH | Dig in |
| 94 | MISO_CD_2 | Dig out |

| | | |
|-----|-----------------|-----------------------------|
| 95 | VDDA | VDDA |
| 96 | VDD_BULK | VDD_Bulk |
| 97 | VDDD | VDDD |
| 98 | VDDES | VDDES |
| 99 | VSSA | GND |
| 100 | VSS_BULK | GND |
| 101 | VSSD | GND |
| 102 | LOAD_PULSE_CD_2 | Dig in |
| 103 | VDDIO | VDDIO |
| 104 | END_ADC_CD_2 | Dig out |
| 105 | VDDA | VDDA |
| 106 | VDDD | VDDD |
| 107 | VSSA | GND |
| 108 | VSSD | GND |
| 109 | VDDIO | VDDIO |
| 110 | TEST_MUX_CD_2 | analogue monitor leave n.c. |
| 111 | VDDA | VDDA |
| 112 | VDD_BULK | VDD_Bulk |
| 113 | VDDD | VDDD |
| 114 | VDDES | VDDES |
| 115 | VSSA | GND |
| 116 | VSS_BULK | GND |
| 117 | VSSD | GND |
| 118 | N_RESET_CD | Dig in |
| 119 | PIXEL_CLK_CD_2 | Dig out |
| 120 | VCLAMP_CD_2 | VDDA |



Note: SCLK and MOSI are connected between connector 2 and connector 4 in the headboard, resulting names are SCLK_CD_GH and MOSI_CD_GH. The user just need to provide to the headboard one pair of this signals to connector 2 or 4 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

12.4.3 Connector 3

| Pin Number | Signal Name | Signal Type |
|------------|-----------------|-----------------------------|
| 1 | N_CS_EF_1 | Dig in |
| 2 | MISO_EF_1 | Dig out |
| 3 | VDDA | VDDA |
| 4 | VDDD | VDDD |
| 5 | VSSA | GND |
| 6 | VSS_BULK | GND |
| 7 | VSSD | GND |
| 8 | LOAD_PULSE_EF_1 | Dig in |
| 9 | VDDIO | VDDIO |
| 10 | END_ADC_EF_1 | Dig out |
| 11 | VDDA | VDDA |
| 12 | VDD_BULK | VDD_Bulk |
| 13 | VDDD | VDDD |
| 14 | VDDES | VDDES |
| 15 | VSSA | GND |
| 16 | VSS_BULK | GND |
| 17 | VSSD | GND |
| 18 | VDDIO | VDDIO |
| 19 | TEST_MUX_EF_1 | analogue monitor leave n.c. |
| 20 | VDDA | VDDA |
| 21 | VDDD | VDDD |
| 22 | VSSA | GND |
| 23 | VSS_BULK | GND |
| 24 | VSSD | GND |
| 25 | VSSES/IO | GND |
| 26 | PIXEL_CLK_EF_1 | Dig out |
| 27 | VCLAMP_EF_1 | VDDA |
| 28 | SAMPLE_EF | Dig in |
| 29 | RST_CDS_EF | Dig in |
| 30 | RST_CVC_EF | Dig in |
| 31 | N_CS_EF_2 | Dig in |
| 32 | SCLK_AB_EF | Dig in |
| 33 | MOSI_AB_EF | dig in |
| 34 | MISO_EF_2 | Dig out |
| 35 | VDDA | VDDA |
| 36 | VDD_BULK | VDD_Bulk |
| 37 | VDDD | VDDD |
| 38 | VDDES | VDDES |
| 39 | VSSA | GND |
| 40 | VSS_BULK | GND |
| 41 | VSSD | GND |
| 42 | LOAD_PULSE_EF_2 | Dig in |
| 43 | VDDIO | VDDIO |
| 44 | END_ADC_EF_2 | Dig out |
| 45 | VDDA | VDDA |
| 46 | VDDD | VDDD |

| | | |
|----|------------------|-----------------------------|
| 47 | VSSA | GND |
| 48 | VSSD | GND |
| 49 | VDDIO | VDDIO |
| 50 | TEST_MUX_EF_2 | analogue monitor leave n.c. |
| 51 | VDDA | VDDA |
| 52 | VDD_BULK | VDD Bulk |
| 53 | VDDD | VDDD |
| 54 | VDDESD | VDDESD |
| 55 | VSSA | GND |
| 56 | VSS_BULK | GND |
| 57 | VSSD | GND |
| 58 | N_RESET_EF | Dig in |
| 59 | PIXEL_CLOCK_EF_2 | Dig out |
| 60 | VCLAMP_EF_2 | VDDA |
| 61 | VSSESD/IO | GND |
| 62 | LVAL_EF_1 | Dig out |
| 63 | BIT_12_TAP_E1 | Dig out |
| 64 | BIT_11_TAP_E1 | Dig out |
| 65 | BIT_10_TAP_E1 | Dig out |
| 66 | BIT_09_TAP_E1 | Dig out |
| 67 | BIT_08_TAP_E1 | Dig out |
| 68 | BIT_07_TAP_E1 | Dig out |
| 69 | BIT_06_TAP_E1 | Dig out |
| 70 | BIT_05_TAP_E1 | Dig out |
| 71 | BIT_04_TAP_E1 | Dig out |
| 72 | BIT_03_TAP_E1 | Dig out |
| 73 | BIT_02_TAP_E1 | Dig out |
| 74 | BIT_01_TAP_E1 | Dig out |
| 75 | BIT_00_TAP_E1 | Dig out |
| 76 | VSSESD/IO | GND |
| 77 | BIT_00_TAP_F1 | Dig out |
| 78 | BIT_01_TAP_F1 | Dig out |
| 79 | BIT_02_TAP_F1 | Dig out |
| 80 | BIT_03_TAP_F1 | Dig out |
| 81 | BIT_04_TAP_F1 | Dig out |
| 82 | BIT_05_TAP_F1 | Dig out |
| 83 | BIT_06_TAP_F1 | Dig out |
| 84 | BIT_07_TAP_F1 | Dig out |
| 85 | BIT_08_TAP_F1 | Dig out |
| 86 | BIT_09_TAP_F1 | Dig out |
| 87 | BIT_10_TAP_F1 | Dig out |
| 88 | BIT_11_TAP_F1 | Dig out |
| 89 | BIT_12_TAP_F1 | Dig out |
| 90 | MAIN_CLK | Dig in |
| 91 | VSSESD/IO | GND |
| 92 | LVAL_EF_2 | Dig out |
| 93 | BIT_12_TAP_E2 | Dig out |
| 94 | BIT_11_TAP_E2 | Dig out |
| 95 | BIT_10_TAP_E2 | Dig out |
| 96 | BIT_09_TAP_E2 | Dig out |

| Pin Number | Signal Name | Signal Type |
|------------|---------------|-------------|
| 97 | BIT_08_TAP_E2 | Dig out |
| 98 | BIT_07_TAP_E2 | Dig out |
| 99 | BIT_06_TAP_E2 | Dig out |
| 100 | BIT_05_TAP_E2 | Dig out |
| 101 | BIT_04_TAP_E2 | Dig out |
| 102 | BIT_03_TAP_E2 | Dig out |
| 103 | BIT_02_TAP_E2 | Dig out |
| 104 | BIT_01_TAP_E2 | Dig out |
| 105 | BIT_00_TAP_E2 | Dig out |
| 106 | VSSESD/IO | GND |
| 107 | BIT_00_TAP_F2 | Dig out |
| 108 | BIT_01_TAP_F2 | Dig out |
| 109 | BIT_02_TAP_F2 | Dig out |
| 110 | BIT_03_TAP_F2 | Dig out |
| 111 | BIT_04_TAP_F2 | Dig out |
| 112 | BIT_05_TAP_F2 | Dig out |
| 113 | BIT_06_TAP_F2 | Dig out |
| 114 | BIT_07_TAP_F2 | Dig out |
| 115 | BIT_08_TAP_F2 | Dig out |
| 116 | BIT_09_TAP_F2 | Dig out |
| 117 | BIT_10_TAP_F2 | Dig out |
| 118 | BIT_11_TAP_F2 | Dig out |
| 119 | BIT_12_TAP_F2 | Dig out |
| 120 | VSSESD/IO | GND |

12.4.4 Connector 4

| Pin Number | Signal Name | Signal Type |
|------------|---------------|---------------|
| 1 | VSSESD/IO | GND |
| 2 | LVAL_GH_1 | Dig out |
| 3 | BIT_12_TAP_G1 | Dig out |
| 4 | BIT_11_TAP_G1 | Dig out |
| 5 | BIT_10_TAP_G1 | Dig out |
| 6 | BIT_09_TAP_G1 | Dig out |
| 7 | BIT_08_TAP_G1 | Dig out |
| 8 | BIT_07_TAP_G1 | Dig out |
| 9 | BIT_06_TAP_G1 | Dig out |
| 10 | BIT_05_TAP_G1 | Dig out |
| 11 | BIT_04_TAP_G1 | Dig out |
| 12 | BIT_03_TAP_G1 | Dig out |
| 13 | BIT_02_TAP_G1 | Dig out |
| 14 | BIT_01_TAP_G1 | Dig out |
| 15 | BIT_00_TAP_G1 | Dig out |
| 16 | VSSESD/IO | GND |
| 17 | BIT_00_TAP_H1 | Dig out |
| 18 | BIT_01_TAP_H1 | Dig out |
| 19 | BIT_02_TAP_H1 | Dig out |
| 20 | BIT_03_TAP_H1 | Dig out |
| 21 | BIT_04_TAP_H1 | Dig out |
| 22 | BIT_05_TAP_H1 | Dig out |
| 23 | BIT_06_TAP_H1 | Dig out |
| 24 | BIT_07_TAP_H1 | Dig out |
| 25 | BIT_08_TAP_H1 | Dig out |
| 26 | BIT_09_TAP_H1 | Dig out |
| 27 | BIT_10_TAP_H1 | Dig out |
| 28 | BIT_11_TAP_H1 | Dig out |
| 29 | BIT_12_TAP_H1 | Dig out |
| 30 | NC | not connected |
| 31 | VSSESD/IO | GND |
| 32 | LVAL_GH_2 | Dig out |
| 33 | BIT_12_TAP_G2 | Dig out |
| 34 | BIT_11_TAP_G2 | Dig out |
| 35 | BIT_10_TAP_G2 | Dig out |
| 36 | BIT_09_TAP_G2 | Dig out |
| 37 | BIT_08_TAP_G2 | Dig out |
| 38 | BIT_07_TAP_G2 | Dig out |
| 39 | BIT_06_TAP_G2 | Dig out |
| 40 | BIT_05_TAP_G2 | Dig out |
| 41 | BIT_04_TAP_G2 | Dig out |
| 42 | BIT_03_TAP_G2 | Dig out |
| 43 | BIT_02_TAP_G2 | Dig out |
| 44 | BIT_01_TAP_G2 | Dig out |
| 45 | BIT_00_TAP_G2 | Dig out |
| 46 | VSSESD/IO | GND |
| 47 | BIT_00_TAP_H2 | Dig out |

| Pin Number | Signal Name | Signal Type |
|------------|-----------------|-----------------------------|
| 48 | BIT_01_TAP_H2 | Dig out |
| 49 | BIT_02_TAP_H2 | Dig out |
| 50 | BIT_03_TAP_H2 | Dig out |
| 51 | BIT_04_TAP_H2 | Dig out |
| 52 | BIT_05_TAP_H2 | Dig out |
| 53 | BIT_06_TAP_H2 | Dig out |
| 54 | BIT_07_TAP_H2 | Dig out |
| 55 | BIT_08_TAP_H2 | Dig out |
| 56 | BIT_09_TAP_H2 | Dig out |
| 57 | BIT_10_TAP_H2 | Dig out |
| 58 | BIT_11_TAP_H2 | Dig out |
| 59 | BIT_12_TAP_H2 | Dig out |
| 60 | VSSED/IO | GND |
| 61 | N_CS_GH_1 | Dig in |
| 62 | MISO_GH_1 | Dig out |
| 63 | VDDA | VDDA |
| 64 | VDDD | VDDD |
| 65 | VSSA | GND |
| 66 | VSS_BULK | GND |
| 67 | VSSD | GND |
| 68 | LOAD_PULSE_GH_1 | Dig in |
| 69 | VDDIO | VDDIO |
| 70 | END_ADC_GH_1 | Dig out |
| 71 | VDDA | VDDA |
| 72 | VDD_BULK | VDD_Bulk |
| 73 | VDDD | VDDD |
| 74 | VDDES | VDDES |
| 75 | VSSA | GND |
| 76 | VSS_BULK | GND |
| 77 | VSSD | GND |
| 78 | VDDIO | VDDIO |
| 79 | TEST_MUX_GH_1 | analogue monitor leave n.c. |
| 80 | VDDA | VDDA |
| 81 | VDDD | VDDD |
| 82 | VSSA | GND |
| 83 | VSS_BULK | GND |
| 84 | VSSD | GND |
| 85 | VSSED/IO | GND |
| 86 | PIXEL_CLK_GH_1 | Dig_out |
| 87 | VCLAMP_GH_1 | VDDA |
| 88 | SAMPLE_GH | Dig in |
| 89 | RST_CDS_GH | Dig in |
| 90 | RST_CVC_GH | Dig in |
| 91 | N_CS_GH_2 | Dig in |
| 92 | SCLK_CD_GH | Dig in |
| 93 | MOSI_CD_GH | Dig in |
| 94 | MISO_GH_2 | Dig out |
| 95 | VDDA | VDDA |

| | | |
|-----|-----------------|-----------------------------|
| 96 | VDD_BULK | VDD_Bulk |
| 97 | VDDD | VDDD |
| 98 | VDDES | VDDES |
| 99 | VSSA | GND |
| 100 | VSS_BULK | GND |
| 101 | VSSD | GND |
| 102 | LOAD_PULSE_GH_2 | Dig in |
| 103 | VDDIO | VDDIO |
| 104 | END_ADC_GH_2 | Dig out |
| 105 | VDDA | VDDA |
| 106 | VDDD | VDDD |
| 107 | VSSA | GND |
| 108 | VSSD | GND |
| 109 | VDDIO | VDDIO |
| 110 | TEST_MUX_GH_2 | analogue monitor leave n.c. |
| 111 | VDDA | VDDA |
| 112 | VDD_BULK | VDD_Bulk |
| 113 | VDDD | VDDD |
| 114 | VDDES | VDDES |
| 115 | VSSA | GND |
| 116 | VSS_BULK | GND |
| 117 | VSSD | GND |
| 118 | N_RESET_GH | Dig in |
| 119 | PIXEL_CLK_GH_2 | Dig out |
| 120 | VCLAMP_GH_2 | VDDA |

12.5 Connector signal assignment for Invar head board DR-6K-7

| Pin Number | Signal Name | |
|------------|---------------------|------------------|
| | Bottom, Connector 1 | Top, Connector 2 |
| 1 | N_CS_AB_1 | GND_D |
| 2 | MISO_AB_1 | LVAL_EF_1 |
| 3 | VDDA | Not connected |
| 4 | VDDD | BIT_11_TAP_A1 |
| 5 | GND_D | BIT_10_TAP_A1 |
| 6 | GND_D | BIT_09_TAP_A1 |
| 7 | GND_A | BIT_08_TAP_A1 |
| 8 | Load_Pulse_AB_1 | BIT_07_TAP_A1 |
| 9 | VDDIO | BIT_06_TAP_A1 |
| 10 | End_ADC_AB_1 | BIT_05_TAP_A1 |
| 11 | VDDA | BIT_04_TAP_A1 |
| 12 | VDD_Bulk | BIT_03_TAP_A1 |
| 13 | VDDD | BIT_02_TAP_A1 |
| 14 | VDDES | BIT_01_TAP_A1 |
| 15 | GND_D | BIT_00_TAP_A1 |
| 16 | GND_D | GND_D |
| 17 | GND_A | Not connected |
| 18 | VDDIO | Not connected |
| 19 | Test_Mux | Not connected |
| 20 | VDDA | Not connected |
| 21 | VDDD | Not connected |
| 22 | GND_D | Not connected |
| 23 | GND_D | Not connected |
| 24 | GND_D | Not connected |
| 25 | GND_A | Not connected |
| 26 | Pixel_Clk_AB_1 | Not connected |
| 27 | Not connected | Not connected |
| 28 | Sample_AB | Not connected |
| 29 | RST_CDS_AB | Not connected |
| 30 | RST_CVC_AB | Not connected |
| 31 | N_CS_AB_2 | GND_D |
| 32 | SCLK_AB_EF | Not connected |
| 33 | MOSI_AB_EF | Not connected |
| 34 | MISO_AB_2 | Not connected |
| 35 | VDDA | Not connected |
| 36 | VDD_BULK | Not connected |
| 37 | VDDD | Not connected |
| 38 | VDDES | Not connected |
| 39 | GND_D | Not connected |
| 40 | GND_D | Not connected |
| 41 | GND_A | Not connected |
| 42 | Load_Pulse_AB_2 | Not connected |

| | | |
|----|----------------|-----------------|
| 43 | VDDIO | Not connected |
| 44 | End_ADC_AB_2 | Not connected |
| 45 | VDDA | Not connected |
| 46 | VDDD | GND_D |
| 47 | GND_D | BIT_00_TAP_F1 |
| 48 | GND_A | BIT_01_TAP_F1 |
| 49 | VDDIO | BIT_02_TAP_F1 |
| 50 | Not connected | BIT_03_TAP_F1 |
| 51 | VDDA | BIT_04_TAP_F1 |
| 52 | VDD_Bulk | BIT_05_TAP_F1 |
| 53 | VDDD | BIT_06_TAP_F1 |
| 54 | VDDES | BIT_07_TAP_F1 |
| 55 | GND_D | BIT_08_TAP_F1 |
| 56 | GND_D | BIT_09_TAP_F1 |
| 57 | GND_A | BIT_10_TAP_F1 |
| 58 | N_Reset_AB | BIT_11_TAP_F1 |
| 59 | Pixel_Clk_AB_2 | Not connected |
| 60 | Not connected | GND_D |
| 61 | GND_D | N_CS_EF_1 |
| 62 | LVAL_AB_1 | MISO_EF_1 |
| 63 | Not connected | Not connected |
| 64 | BIT_00_TAP_B1 | Not connected |
| 65 | BIT_01_TAP_B1 | GND_D |
| 66 | BIT_02_TAP_B1 | GND_D |
| 67 | BIT_03_TAP_B1 | GND_A |
| 68 | BIT_04_TAP_B1 | Load Pulse EF 1 |
| 69 | BIT_05_TAP_B1 | Not connected |
| 70 | BIT_06_TAP_B1 | End ADC EF 1 |
| 71 | BIT_07_TAP_B1 | Not connected |
| 72 | BIT_08_TAP_B1 | Not connected |
| 73 | BIT_09_TAP_B1 | Not connected |
| 74 | BIT_10_TAP_B1 | Not connected |
| 75 | BIT_11_TAP_B1 | GND_D |
| 76 | GND_D | GND_D |
| 77 | BIT_11_TAP_A2 | GND_A |
| 78 | BIT_10_TAP_A2 | Not connected |
| 79 | BIT_09_TAP_A2 | Not connected |
| 80 | BIT_08_TAP_A2 | Not connected |
| 81 | BIT_07_TAP_A2 | Not connected |
| 82 | BIT_06_TAP_A2 | GND_D |
| 83 | BIT_05_TAP_A2 | GND_D |
| 84 | BIT_04_TAP_A2 | GND_D |
| 85 | BIT_03_TAP_A2 | GND_A |
| 86 | BIT_02_TAP_A2 | Pixel_Clk_EF_1 |
| 87 | BIT_01_TAP_A2 | Not connected |
| 88 | BIT_00_TAP_A2 | Sample_EF |
| 89 | Not connected | RST_CDS_EF |
| 90 | Main_Clk | RST_CVC_EF |
| 91 | GND_D | ID_Chip |

| | | |
|-----|---------------|---------------|
| 92 | LVAL_AB_2 | Not connected |
| 93 | Not connected | Not connected |
| 94 | BIT_00_TAP_B2 | Not connected |
| 95 | BIT_01_TAP_B2 | Not connected |
| 96 | BIT_02_TAP_B2 | Not connected |
| 97 | BIT_03_TAP_B2 | Not connected |
| 98 | BIT_04_TAP_B2 | Not connected |
| 99 | BIT_05_TAP_B2 | GND_D |
| 100 | BIT_06_TAP_B2 | GND_D |
| 101 | BIT_07_TAP_B2 | GND_A |
| 102 | BIT_08_TAP_B2 | Not connected |
| 103 | BIT_09_TAP_B2 | Not connected |
| 104 | BIT_10_TAP_B2 | Not connected |
| 105 | BIT_11_TAP_B2 | Not connected |
| 106 | GND_D | 3.3V_Digital |
| 107 | BIT_11_TAP_E1 | GND_D |
| 108 | BIT_10_TAP_E1 | GND_A |
| 109 | BIT_09_TAP_E1 | Not connected |
| 110 | BIT_08_TAP_E1 | Not connected |
| 111 | BIT_07_TAP_E1 | Not connected |
| 112 | BIT_06_TAP_E1 | Not connected |
| 113 | BIT_05_TAP_E1 | Not connected |
| 114 | BIT_04_TAP_E1 | 3.3V_Digital |
| 115 | BIT_03_TAP_E1 | GND_D |
| 116 | BIT_02_TAP_E1 | GND_D |
| 117 | BIT_01_TAP_E1 | GND_A |
| 118 | BIT_00_TAP_E1 | N_Reset_EF |
| 119 | Not connected | Not connected |
| 120 | GND_D | Not connected |

End of Document

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Image Sensors](#) category:

Click to view products by [Ams](#) manufacturer:

Other Similar products are found below :

[KAF-16803-ABA-DD-BA](#) [KAF-4320-AAA-JP-B1](#) [KAF-16200-ABA-CD-B2](#) [KAF-50100-AAA-JD-BA](#) [KAI-0340-FBA-CB-AA-SINGLE](#)
[KAI-11002-ABA-CD-B1](#) [KAI-2020-ABA-CD-BA](#) [KAI-2093-ABA-CB-B2](#) [KAI-2020-ABA-CP-BA](#) [KAI-01150-FBA-FD-BA](#) [KAF-8300-](#)
[AXC-CD-AA](#) [KAI-11002-ABA-CD-B2](#) [KAF-3200-ABA-CD-B2](#) [AR0331SRSC00SUCA0-DPBR](#) [AR0331SRSC00XUEE0-DPBR](#)
[MT9V138C12STC-DP1](#) [KAI-08051-AXA-JP-BA](#) [KLI-8023-RAA-ED-AA](#) [KAF-0402-ABA-CP-B2](#) [KLI-8023-AAA-ED-AA](#) [KAF-16200-](#)
[FXA-CD-B2](#) [KAI-04050-AAA-JP-BA](#) [NOM02A4-AG01G](#) [NOM02A4-AR03G](#) [KAF-1603-AAA-CP-B2](#) [LI-USB30-OS05A20-110H](#)
[NOIX5SN5000B-LTI1](#) [KAF-1001-AAA-CP-B1](#) [NOIV1SE2000A-QDC](#) [KAI-1003-AAA-CR-B2](#) [KAI-0340-FBA-CB-AA-DUAL](#) [KAF-0402-](#)
[ABA-CD-B1](#) [KAI-01050-FBA-JD-BA](#) [AR0237IRSH12SHRA0-DR](#) [OV02659-A47A](#) [AR0132AT6M00XPEA0-DRBR](#)
[DR2X2K7_INVAR_RGB_V6](#) [DR2X4K7_INVAR_RGB_V6](#) [Mira030-1RM2WP](#) [NOIP1SE1300A-QDI](#) [AR0132AT6C00XPEA0-DRBR1](#)
[AR0140AT3C00XUEA0-DPBR2](#) [AR0144CSSC00SUKA0-CPBR1](#) [AR0144CSSC00SUKA0-CPBR2](#) [AR0230CSSC00SUEA0-DPBR2](#)
[AR0238CSSC12SHRA0-DP2](#) [AR0330CM1C00SHAA0-DP2](#) [AR0330CM1C00SHAA0DR](#) [AR0330CM1C00SHAA0-DP1](#)
[AR0521SR2M09SURA0-DP1](#)