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The technical content of this TAOS datasheet is still valid.

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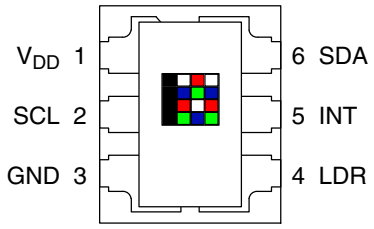
TCS3772
COLOR LIGHT-TO-DIGITAL CONVERTER with PROXIMITY SENSING

TAOS145B – SEPTEMBER 2012

Features

- RGB and Clear Color Sensing and Proximity Detection in a Single Device
- Color Light Sensing with IR-Blocking Filter
  - Programmable Analog Gain and Integration Time
  - 3,800,000:1 Dynamic Range
  - Very High Sensitivity — Ideally Suited for Operation Behind Dark Glass
- Proximity Detection
  - Ambient Light Rejection
  - Programmable Integration Time
  - Current Sink Driver for External IR LED
- Maskable Light and Proximity Interrupt
  - Programmable Upper and Lower Thresholds with Persistence Filter
- Power Management
  - Low Power — 2.5-μA Sleep State
  - 65-μA Wait State withProgrammable Wait State Time from 2.4 ms to > 7 Seconds
- I^2C Fast Mode Compatible Interface
  - Data Rates up to 400 kbit/s
  - Input Voltage Levels Compatible with V_{DD} or 1.8 V Bus
- Register Set and Pin Compatible with the TCS3x71 Series
- Small 2 mm × 2.4 mm Dual Flat No-Lead (FN) Package

PACKAGE FN
DUAL FLAT NO-LEAD
(TOP VIEW)



Package Drawing Not to Scale

Applications

- RGB LED Backlight Control
- Ambient Light Color Temperature Sensing
- Cell Phone Touch Screen Disable
- Mechanical Switch Replacement
- Industrial Process Control
- Medical Diagnostics

End Products and Market Segments

- HDTVs, Mobile Handsets, Tablets, and Portable Media Payers
- Medical and Commercial Instrumentation
- Toys
- Solid State and General Lighting

Description

The TCS3772 device family provides red, green, blue, and clear (RGBC) light sensing and, when coupled with an external IR LED, proximity detection. These devices detect light intensity under a variety of lighting conditions and through a variety of attenuation materials, including dark glass. The proximity detection feature allows a large dynamic range of operation for accurate short distance detection, such as in a cell phone, for detecting when the user positions the phone close to their ear. An internal state machine provides the ability to put the device into a low power state in between proximity and RGBC measurements providing very low average power consumption.

The color sensing feature is useful in applications such as LED RGB backlight control, solid state lighting, reflected LED color sampler, or fluorescent light color temperature detection. With the addition of an IR blocking filter, the device is an excellent ambient light sensor, color temperature monitor, and general purpose color sensor.

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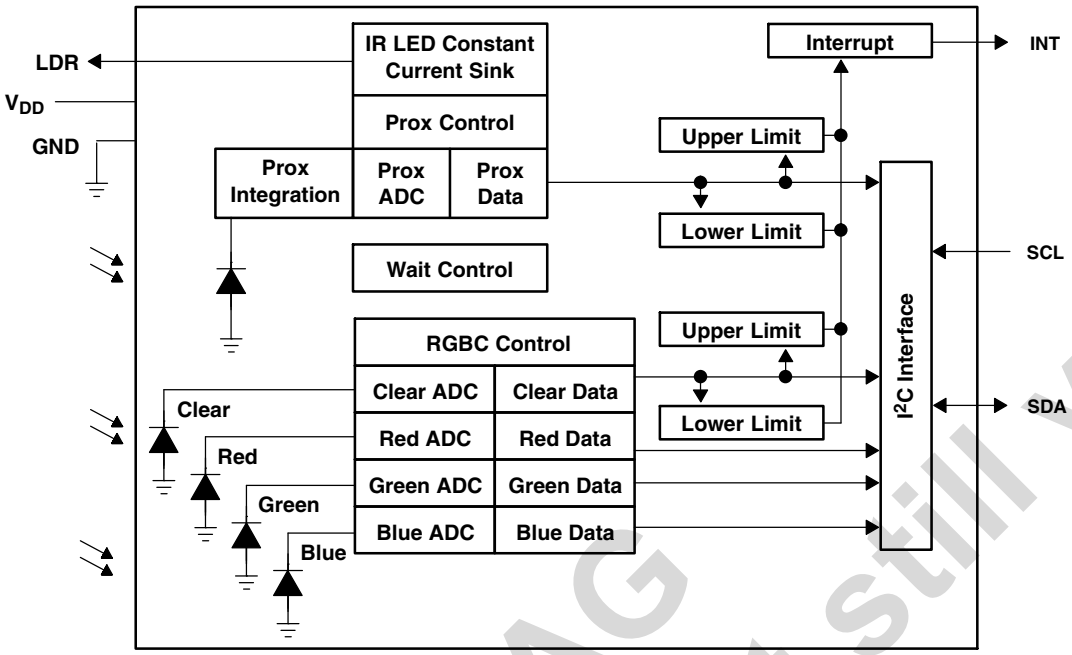
Functional Block Diagram



Detailed Description

The TCS3772 is a next-generation digital color light sensor device containing four integrating analog-to-digital converters (ADCs) that integrate currents from photodiodes. The device contains a 3×4 photodiode array used for color measurements and a 1×4 photodiode array used for proximity measurements. Integration of all color sensing channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the corresponding data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained. Communication with the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller.

The device provides a separate pin for level-style interrupts. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. When interrupts are enabled, an interrupt is generated when the value of a clear channel or proximity conversion is greater than an upper threshold or less than a lower threshold. Once the interrupt is asserted, it remains asserted until cleared by the controlling firmware. In addition, a programmable interrupt persistence filter allows the user to set the number of consecutive clear channel or proximity conversions outside of the threshold region that are necessary to trigger an interrupt. Interrupt thresholds and persistence filter settings are configured independently for both clear and proximity.

Proximity detection requires only a single external IR LED. An internal LED driver can be configured to provide a constant current sink of 12.5 mA, 25 mA, 50 mA, or 100 mA of current. No external current limiting resistor is required. The number of proximity LED pulses can be programmed from 1 to 255 pulses. Each pulse has a 14-µs period.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
GND	3		Power supply ground. All voltages are referenced to GND.
INT	5	O	Interrupt — open drain (active low).
LDR	4	O	LED driver for proximity emitter — open drain.
SCL	2	I	I^2C serial clock input terminal — clock signal for I^2C serial data.
SDA	6	I/O	I^2C serial data I/O terminal — serial data I/O for I^2C .
V_{DD}	1		Supply voltage.

Available Options

DEVICE	ADDRESS	PACKAGE – LEADS	INTERFACE DESCRIPTION	ORDERING NUMBER
TCS37721†	0x39	FN–6	I^2C Vbus = V_{DD} Interface	TCS37721FN
TCS37723†	0x39	FN–6	I^2C Vbus = 1.8 V Interface	TCS37723FN
TCS37725†	0x29	FN–6	I^2C Vbus = V_{DD} Interface	TCS37725FN
TCS37727	0x29	FN–6	I^2C Vbus = 1.8 V Interface	TCS37727FN

† Contact TAOS for availability.

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (Note 1) . . . . . 3.8 V
Input terminal voltage . . . . . –0.5 V to 3.8 V
Output terminal voltage (except LDR) . . . . . –0.5 V to 3.8 V
Output terminal voltage (LDR) . . . . . –0.5 V to 3.8 V
Output terminal current (except LDR) . . . . . –1 mA to 20 mA
Storage temperature range, T_{stg} . . . . . –40°C to 85°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (TCS37721 & TCS37725) (I^2C V_{bus} = V_{DD})	2.7	3	3.6	V
Supply voltage, V_{DD} (TCS37723 & TCS37727) (I^2C V_{bus} = 1.8 V)	2.7	3	3.3	V
Operating free-air temperature, T_A	–30		70	°C

Operating Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	Active — LDR pulses off		235	330	µA
		Wait state		65		
		Sleep state — no I^2C activity		2.5	10	
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		–5		5	µA
I_{LEAK}	Leakage current, LDR pin		–5		5	µA
V_{IH}	SCL, SDA input high voltage	TCS37721 & TCS37725	0.7 V_{DD}			V
		TCS37723 & TCS37727	1.25			
V_{IL}	SCL, SDA input low voltage	TCS37721 & TCS37725			0.3 V_{DD}	V
		TCS37723 & TCS37727			0.54	

Optical Characteristics, V_{DD} = 3 V, T_A = 25°C, AGAIN = 16×, ATIME = 0xF6 (unless otherwise noted) (Note 1)

PARAMETER		TEST CONDITIONS	Red Channel			Green Channel			Blue Channel			Clear Channel			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
R_e	Irradiance responsivity	λ_D = 465 nm Note 2	0%		15%	10%		42%	65%		88%	11.0	13.8	16.6	counts/ µW/ cm^2
		λ_D = 525 nm Note 3	4%		25%	60%		85%	10%		45%	13.2	16.6	20.0	
		λ_D = 615 nm Note 4	80%		110%	0%		14%	5%		24%	15.6	19.5	23.4	

NOTES: 1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the clear channel value.
2. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda$½ = 22 nm.
3. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda$½ = 35 nm.
4. The 615 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 615 nm, spectral halfwidth $\Delta\lambda$½ = 15 nm.

RGBC Characteristics, VDD = 3 V, TA = 25°C, AGAIN = 16×, AEN = 1 (unless otherwise noted)

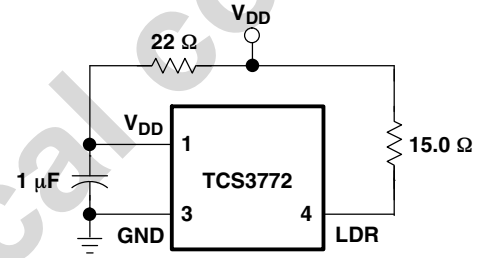
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dark ADC count value	E_e = 0, AGAIN = 60×, ATIME = 0xD6 (100 ms)	0	1	5	counts
ADC integration time step size	ATIME = 0xFF	2.27	2.4	2.56	ms
ADC number of integration steps (Note 5)		1		256	steps
ADC counts per step (Note 5)		0		1024	counts
ADC count value (Note 5)	ATIME = 0xC0 (153.6 ms)	0		65535	counts
Gain scaling, relative to 1× gain setting	4×	3.8	4	4.2	×
	16×	15	16	16.8	
	60×	58	60	63	

NOTE 5: Parameter ensured by design and is not tested.

Proximity Characteristics, V_{DD} = 3 V, T_A = 25°C, PEN = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Supply current	LDR pulse on			3		mA
	ADC conversion time step size	PTIME = 0xFF		2.27	2.4	2.56	ms
	ADC number of integration steps (Note 1)			1		256	steps
	ADC counts per step (Note 1)	PTIME = 0xFF		0		1023	counts
	ADC count value	λ_p = 850 nm, E_e = 770.1 µW/cm^2, PTIME = 0xFB, PPULSE = 1 (Note 3)		1350		1900	counts
	ADC output responsivity	λ_p = 850 nm, PTIME = 0xFF, PPULSE = 1 (Note 3)		0.175	0.211	0.247	counts/ µW/cm^2
	Noise (Notes 1, 2, 3)	E_e = 0, PTIME = 0xFF, PPULSE = 8 (Note 6)			2		% FS
	LED pulse count (Note 1)			0		255	pulses
	LED pulse period				14.0		µs
	LED pulse width — LED on time				6.3		µs
	LED drive current	I_{SINK} sink current @ 1.6 V, LDR pin	PDRIVE = 0	80	106	132	mA
			PDRIVE = 1		50		
			PDRIVE = 2		25		
			PDRIVE = 3		12.5		
	Maximum operating distance (Notes 1, 4, 5)	PDRIVE = 0 (100 mA), PPULSE = 64 Emitter: λ_p = 850 nm, 20° half angle, and 60 mW/sr Object: 16 × 20-inch, 90% reflective Kodak Gray Card (white surface) Optics: Open view (no glass, no optical attenuation)			30		inches

NOTES: 1. Parameter is ensured by design or characterization and is not tested.
2. Proximity noise is defined as one standard deviation of 600 samples.
3. Proximity noise typically increases as $\sqrt{\text{PPULSE}}$
4. Greater operating distances are achievable with appropriate optical system design considerations. See available TAOS application notes for additional information.
5. Maximum operating distance is dependent upon emitter and the reflective properties of the object's surface.
6. Proximity noise test was done using the following circuit:



Wait Characteristics, V_{DD} = 3 V, T_A = 25°C, WEN = 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CHANNEL	MIN	TYP	MAX	UNIT
Wait step size	WTIME = 0xFF		2.27	2.4	2.56	ms
Wait number of steps (Note 7)			1		256	steps

NOTE 7: Parameter ensured by design and is not tested.

AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER†		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	Clock frequency (I^2C only)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0			µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

† Specified by design and characterization; not production tested.

PARAMETER MEASUREMENT INFORMATION

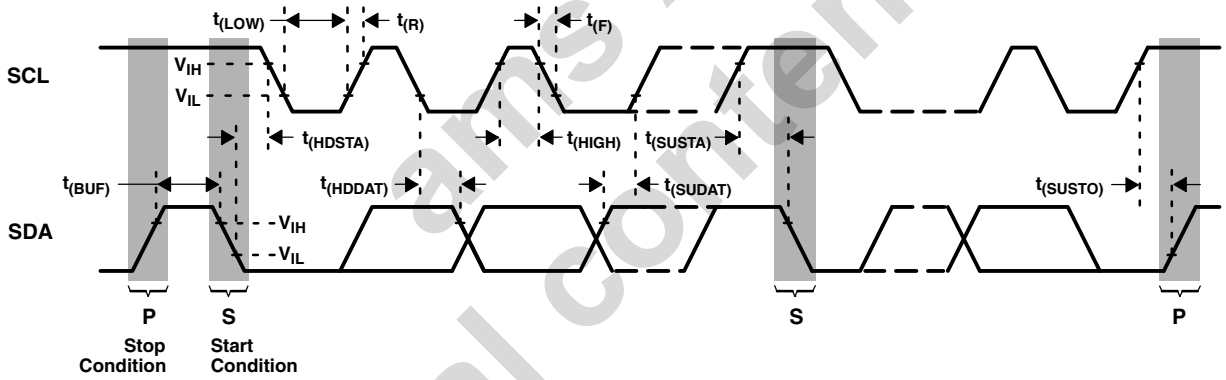


Figure 1. Timing Diagrams

TYPICAL CHARACTERISTICS

PHOTODIODE SPECTRAL RESPONSIVITY
RGBC

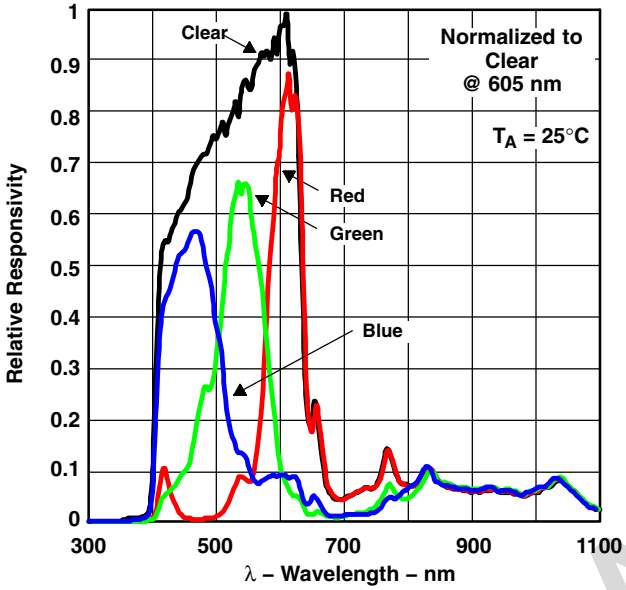


Figure 2

PHOTODIODE SPECTRAL RESPONSIVITY
PROXIMITY

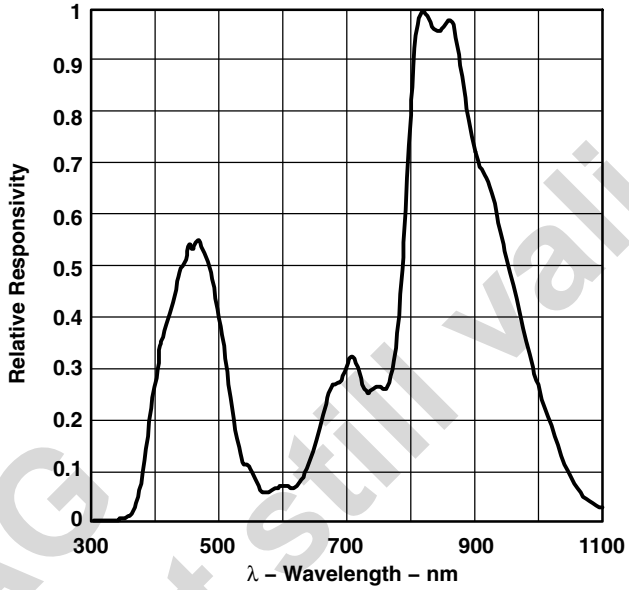


Figure 3

NORMALIZED RESPONSIVITY
vs.
ANGULAR DISPLACEMENT

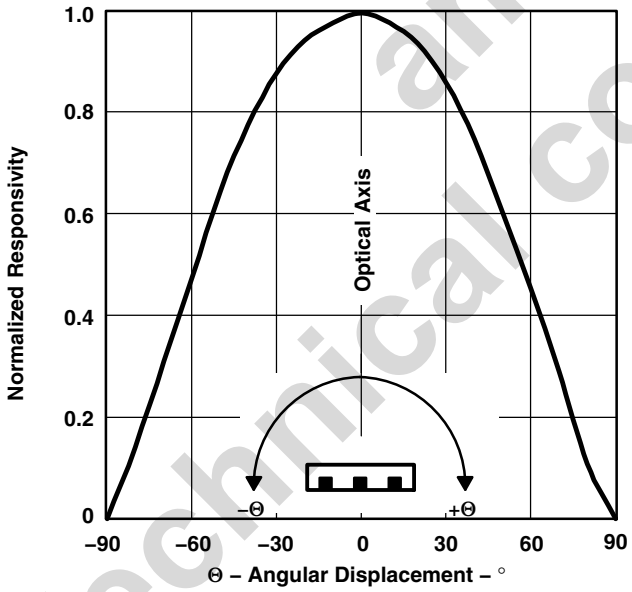


Figure 4

NORMALIZED RESPONSIVITY
vs.
ANGULAR DISPLACEMENT

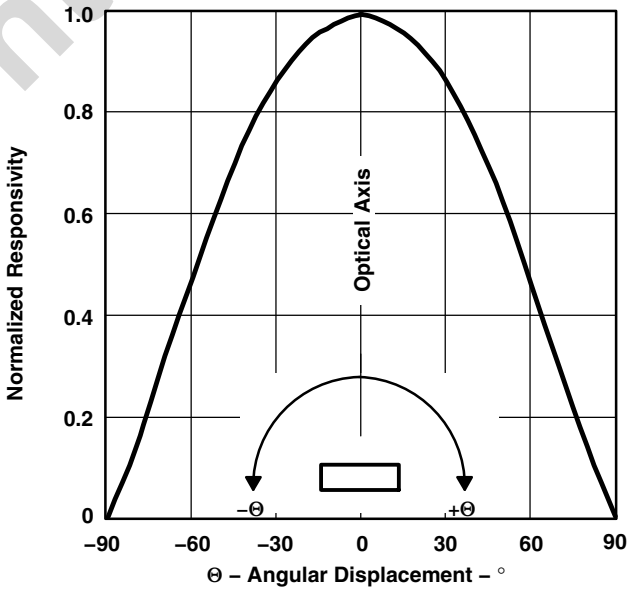


Figure 5

TYPICAL CHARACTERISTICS

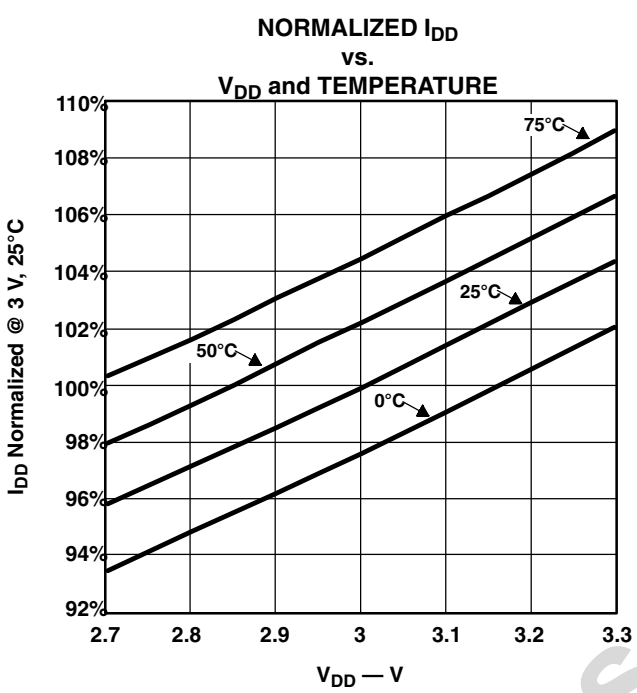


Figure 6

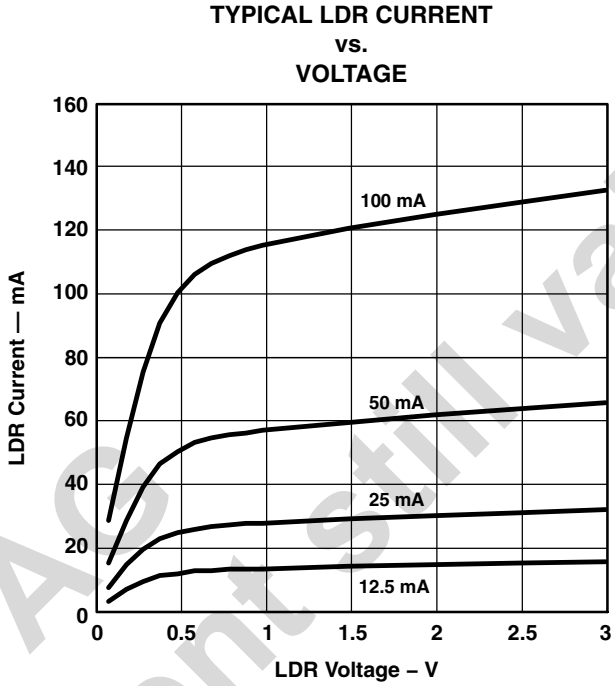


Figure 7

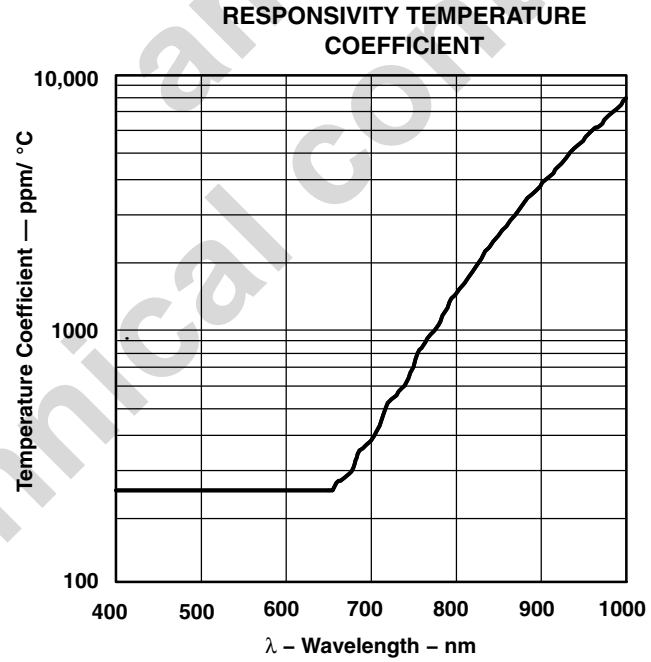


Figure 8

PRINCIPLES OF OPERATION

System State Machine

The TCS3772 provides control of RGBC, proximity detection, and power management functionality through an internal state machine (Figure 9). After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then continue through the Prox, Wait, and RGBC states. If these states are enabled, the device will execute each function. If the PON bit is set to 0, the state machine will continue until all conversions are completed and then go into a low power sleep mode.

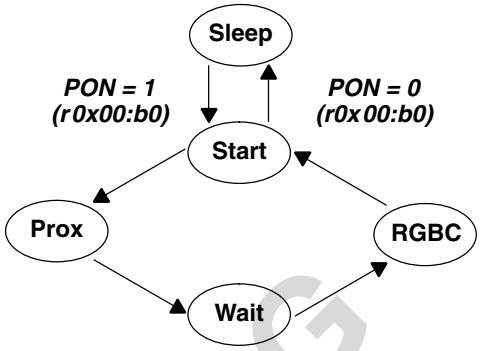


Figure 9. Simplified State Diagram

NOTE: In this document, the nomenclature uses the bit field name in italics followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0, bit 0. This is represented as *PON (r0x00:b0)*.

RGBC Operation

The RGBC engine contains RGBC gain control (AGAIN) and four integrating analog-to-digital converters (ADC) for the RGBC photodiodes. The RGBC integration time (ATIME) impacts both the resolution and the sensitivity of the RGBC reading. Integration of all four channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the color data registers. This data is also referred to as channel count. The transfers are double-buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically moves to the next state in accordance with the configured state machine.

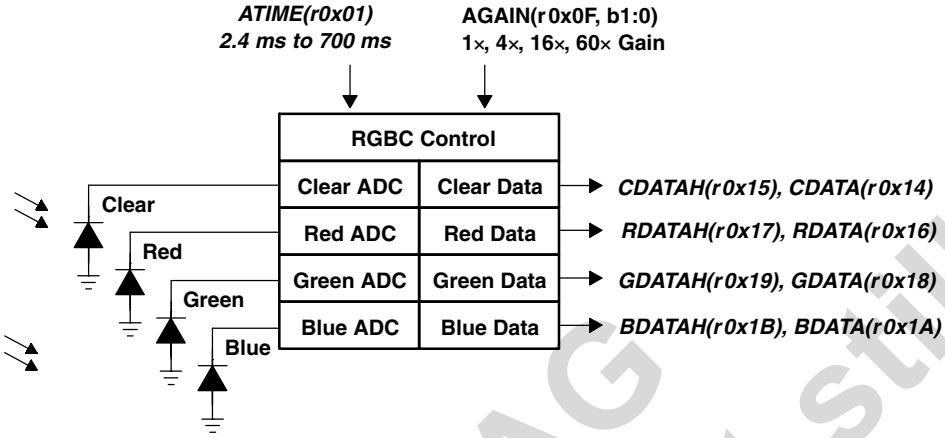


Figure 10. RGBC Operation

The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

ATIME = 256 – Integration Time / 2.4 ms

Inversely, the time can be calculated from the register value as follows:

Integration Time = 2.4 ms × (256 – ATIME)

For example, if a 100-ms integration time is needed, the device needs to be programmed to:

256 – (100 / 2.4) = 256 – 42 = 214 = 0xD6

Conversely, the programmed value of 0xC0 would correspond to:

(256 – 0xC0) × 2.4 = 64 × 2.4 = 154 ms

Proximity Detection

Proximity detection is accomplished by measuring the amount of light energy, generally from an IR LED, reflected off an object to determine its distance. The proximity light source, which is external to the TCS3772 device, is driven by the integrated proximity LED current driver as shown in Figure 6.

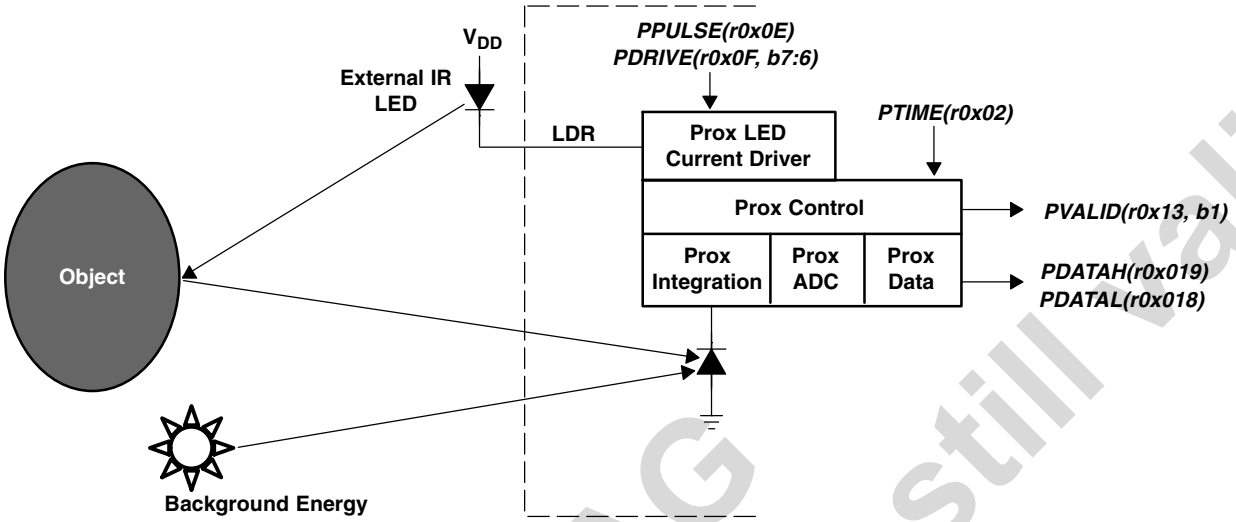


Figure 11. Proximity Detection

The LED current driver, output on the LDR terminal, provides a regulated current sink that eliminates the need for an external current limiting resistor. PDRIVE sets the drive current to 100 mA, 50 mA, 25 mA. To drive an external light source with more than 100 mA or to minimize on-chip ground bounce, LDR can be used to drive an external p-type transistor, which, in turn, drives the light source.

Referring to the Detailed State Machine figure, the LED current driver pulses the external IR LED as shown in Figure 12 during the Prox Accum state. Figure 12 also illustrates that the LED On pulse has a fixed width of 6.3 µs and period of 14.0 µs. So, in addition to setting the proximity drive current, 1 to 255 proximity pulses (PPULSE) can be programmed. When deciding on the number of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of PPULSE.

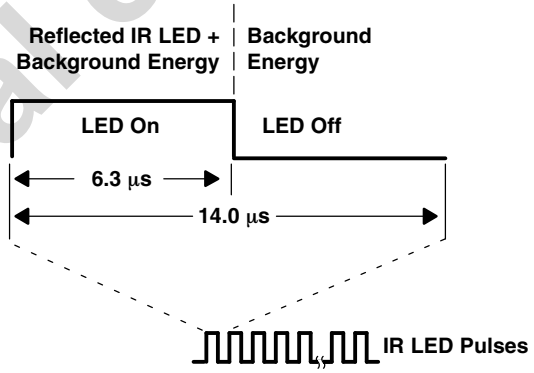


Figure 12. Proximity LED Current Driver Waveform

Figure 11 illustrates light rays emitting from an external IR LED, reflecting off an object, and being absorbed by the proximity photodiode.

Referring again to Figure 12, the reflected IR LED and the background energy is integrated during the LED On time, then during the LED Off time, the integrated background energy is subtracted from the LED On time energy, leaving the external IR LED energy to accumulate from pulse to pulse.

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. ADC scaling is controlled by the proximity ADC conversion time (PTIME) which is programmable from 1 to 256 2.4-ms time units. However, depending on the application, scaling the proximity data will equally scale any accumulated noise. Therefore, in general, it is recommended to leave PTIME at the default value of one 2.4-ms ADC conversion time (0xFF).

Once the first proximity cycle has completed, the proximity valid (PVALID) bit in the Status register will be set and remain set until the proximity detection function is disabled (PEN).

For additional information on using the proximity detection function behind glass and for optical system design guidance, please see available TAOS application notes.

Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity or proximity values outside of a user-defined range. While the interrupt function is always enabled and it's status is available in the status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) or Clear interrupt enable (AIEN) fields in the enable register (0x00).

Four 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level and proximity range. An interrupt can be generated when the Clear data (CDATA) is less than the Clear interrupt low threshold registers (AILTx) or greater than the Clear interrupt high threshold registers (AIHTx). Likewise, an out-of-range proximity interrupt can be generated when the proximity data (PDATA) falls below the proximity interrupt low threshold (PILTx) or exceeds the proximity interrupt high threshold (PIHTx).

It is important to note that the thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range Clear or proximity occurrences before an interrupt is generated. The persistence register (0x0C) allows the user to set the Clear persistence (APERS) and the proximity persistence (PPERS) values. See the persistence register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see command register).

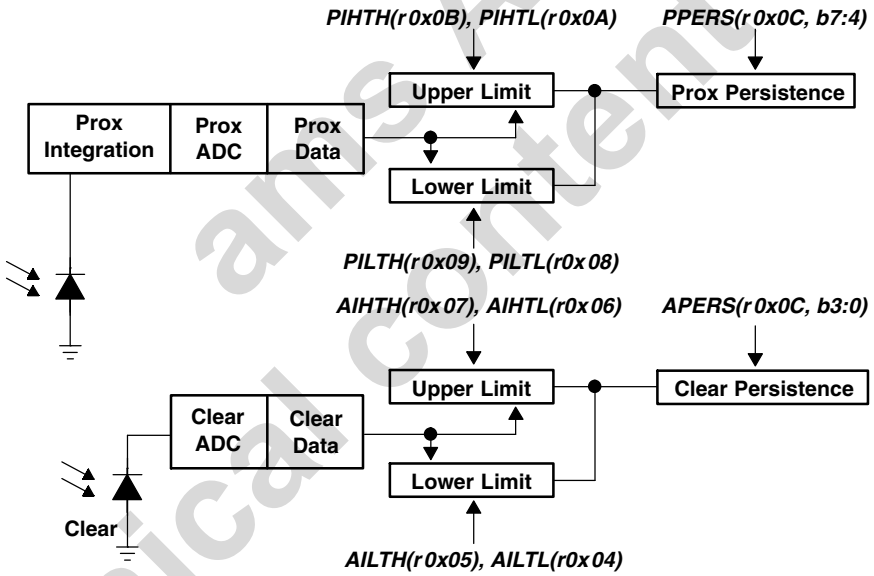


Figure 13. Programmable Interrupt

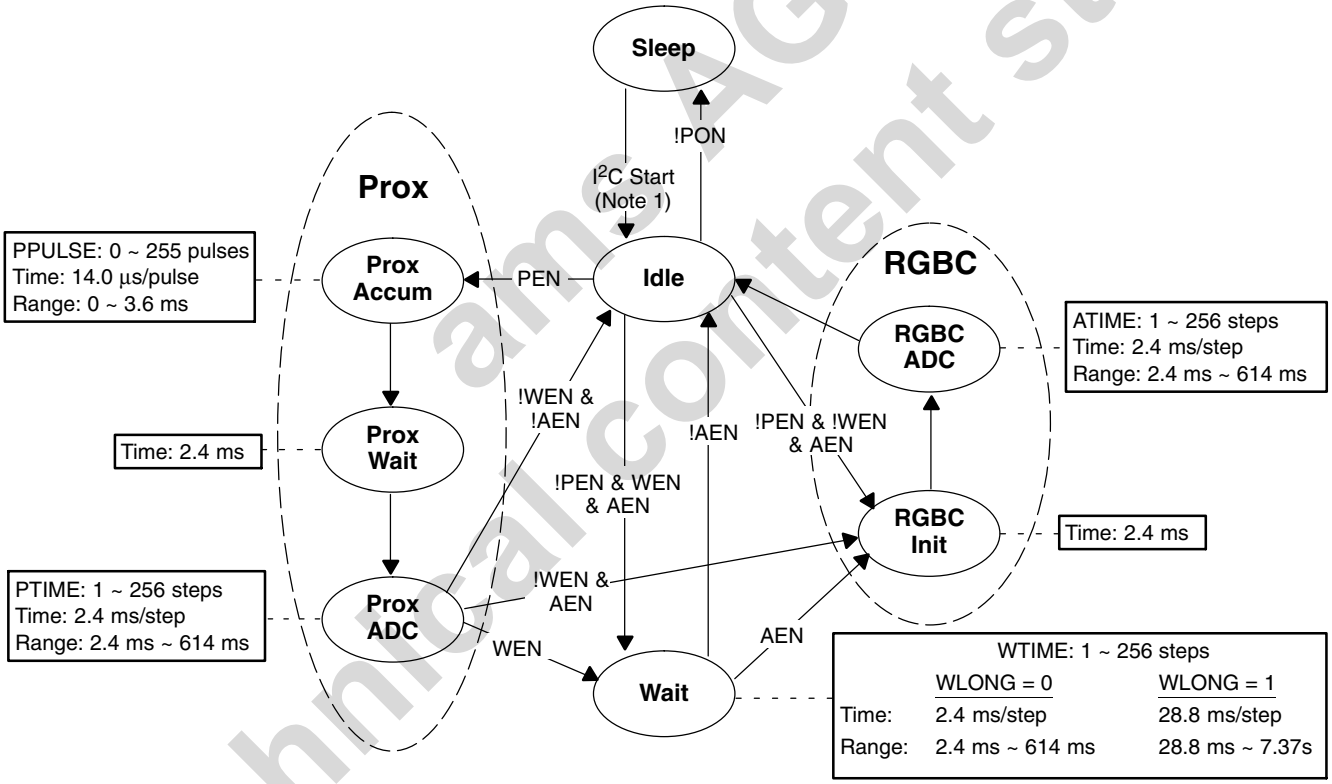
System Timing

The system state machine shown in Figure 9 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features, which affect the state machine cycle time, and provides details to determine system level timing.

When the proximity detection feature is enabled (PEN), the state machine transitions through the Prox Accum, Prox Wait, and Prox ADC states. The Prox Wait time is a fixed 2.4 ms, whereas the Prox Accum time is determined by the number of proximity LED pulses (PPULSE) and the Prox ADC time is determined by the integration time (PTIME). The formulas to determine the Prox Accum and Prox ADC times are given in the associated boxes in Figure 14. If an interrupt is generated as a result of the proximity cycle, it will be asserted at the end of the Prox ADC state.

When the power management feature is enabled (WEN), the state machine will transition in turn to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12× when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 14.

When the RGBC feature is enabled (AEN), the state machine will transition through the RGBC Init and RGBC ADC states. The RGBC Init state takes 2.4 ms, while the RGBC ADC time is dependent on the integration time (ATIME). The formula to determine RGBC ADC time is given in the associated box in Figure 14. If an interrupt is generated as a result of the RGBC cycle, it will be asserted at the end of the RGBC ADC.



Notes: 1. There is a 2.4 ms warm-up delay if PON is enabled. If PON is not enabled, the device will return to the Sleep state as shown.
2. PON, PEN, WEN, and AEN are fields in the Enable register (0x00).

Figure 14. Detailed State Diagram

Power Management

Power consumption can be managed with the Wait state, because the Wait state typically consumes only 65 µA of I_{DD} current. An example of the power management feature is given below. With the assumptions provided in the example, average I_{DD} is estimated to be 186 µA.

Table 1. Power Management

SYSTEM STATE MACHINE STATE	PROGRAMMABLE PARAMETER	PROGRAMMED VALUE	DURATION	TYPICAL CURRENT
Prox Accum	PPULSE	0x04	0.056 ms	
Prox Accum – LED On			0.025 ms (Note 1)	109 mA
Prox Accum – LED Off			0.031 ms (Note 2)	0.235 mA
Prox Wait			2.40 ms	0.235 mA
Prox ADC	PTIME	0xFF	2.40 ms	0.235 mA
Wait	WTIME	0xEE	43.1 ms	0.065 mA
	WLONG	0		
ALS Init			2.40 ms	0.235 mA
ALS ADC	ATIME	0xEE	43.1 ms	0.235 mA

NOTES: 1. Prox Accum – LED On time = 6.3 µs per pulse × 4 pulses = 25.2µs = 0.025 ms
2. Prox Accum – LED Off time = 7.7 µs per pulse × 4 pulses = 30.9µs = 0.031 ms

Average I_{DD} Current = ((0.025 × 109) + (0.031 × 0.235) + (2.40 × 0.235) + (43.1 × 0.065) + (43.1 × 0.263) + (2.40 × 0.235 × 2)) / 93 ≈ 186 µA

Keeping with the same programmed values as the example, Table 2 shows how the average I_{DD} current is affected by the Wait state time, which is determined by WEN, WTIME, and WLONG. Note that the worst-case current occurs when the Wait state is not enabled.

Table 2. Average I_{DD} Current

WEN	WTIME	WLONG	WAIT STATE	AVERAGE I_{DD} CURRENT
0	n/a	n/a	0 ms	289 µA
1	0xFF	0	2.40 ms	279 µA
1	0xEE	0	43.1 ms	186 µA
1	0x00	0	613 ms	82 µA
1	0x00	1	7.36 s	67 µA

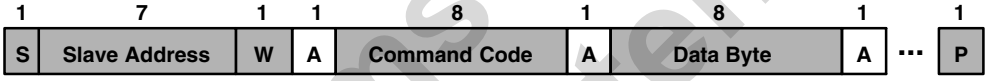
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

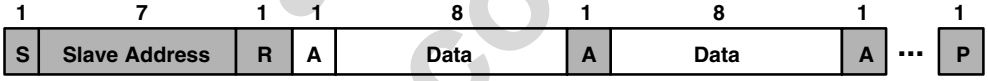
The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 15). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c–bus.org/references/.

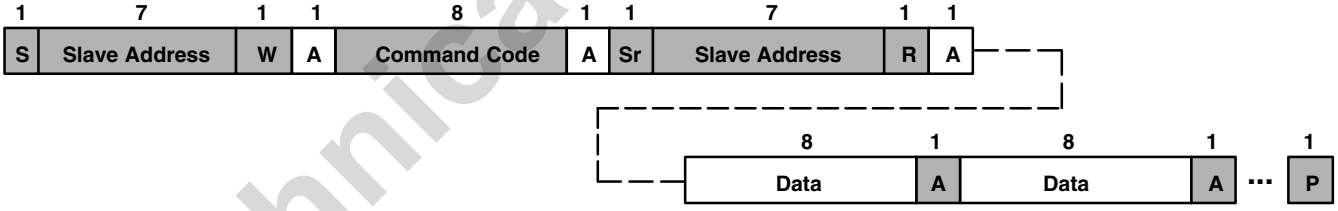
A Acknowledge (0)
N Not Acknowledged (1)
P Stop Condition
R Read (1)
S Start Condition
Sr Repeated Start Condition
W Write (0)
... Continuation of protocol
Master-to-Slave
Slave-to-Master



I²C Write Protocol



I²C Read Protocol



I²C Read Protocol — Combined Format

Figure 15. I²C Protocols

Register Set

The TCS3772 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 3.

Table 3. Register Address

ADDRESS	RESISTER NAME	R/W	REGISTER FUNCTION	RESET VALUE
––	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	RGBC time	0xFF
0x02	PTIME	R/W	Proximity time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	Clear interrupt low threshold low byte	0x00
0x05	AILTH	R/W	Clear interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	Clear interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	Clear interrupt high threshold high byte	0x00
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPULSE	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Gain control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	CDATA	R	Clear ADC data low byte	0x00
0x15	CDATAH	R	Clear ADC data high byte	0x00
0x16	RDATA	R	Red ADC data low byte	0x00
0x17	RDATAH	R	Red ADC data high byte	0x00
0x18	GDATA	R	Green ADC data low byte	0x00
0x19	GDATAH	R	Green ADC data high byte	0x00
0x1A	BDATA	R	Blue ADC data low byte	0x00
0x1B	BDATAH	R	Blue ADC data high byte	0x00
0x1C	PDATA	R	Proximity ADC data low byte	0x00
0x1D	PDATAH	R	Proximity ADC data high byte	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

Table 4. Command Register

	7	6	5	4	3	2	1	0	
COMMAND	**CMD**	**TYPE**			**ADDR/SF**				**Reset 0x00**

FIELD	BITS	DESCRIPTION	
CMD	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**INTEGRATION TIME**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function — See description below
		Byte protocol will repeatedly read the same register with each data access. Block protocol will provide auto-increment function to read successive bytes.	
ADDR/SF	4:0	Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control–status–register for following write and read transactions. The field values listed below apply only to special function commands:	
		FIELD VALUE	**READ VALUE**
		00101	Proximity interrupt clear
		00110	Clear channel interrupt clear
		00111	Proximity and Clear interrupt clear
		other	Reserved — Do not write
		The ALS and Proximity interrupt clear special functions clear any pending interrupt(s) and are self clearing.	

Enable Register (0x00)

The Enable register is used primarily to power the TCS3772 device on and off, and enable functions and interrupts as shown in Table 5.

Table 5. Enable Register

	7	6	5	4	3	2	1	0	
ENABLE	**Reserved**		**PIEN**	**AIEN**	**WEN**	**PEN**	**AEN**	**PON**	**Reset 0x00**

FIELD	BITS	DESCRIPTION
Reserved	7:6	Reserved. Write as 0.
PIEN	5	Proximity interrupt enable. When asserted, permits proximity interrupts to be generated.
AIEN	4	Clear channel interrupt enable. When asserted, permits Clear interrupts to be generated.
WEN	3	Wait enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN	1	RGBC enable. This bit actives the two-channel ADC. Writing a 1 activates RGBC. Writing a 0 disables RGBC.
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator. During reads and writes over the I^2C interface, this bit is temporarily overridden and the oscillator is enabled, independent of the state of PON.

RGBC Time Register (0x01)

The RGBC timing register controls the internal integration time of the RGBC clear and IR channel ADCs in 2.4-ms increments. Upon power up, the RGBC time register is set to 0xFF.

Table 6. RGBC Time Register

FIELD	BITS	DESCRIPTION			
ATIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.4 ms	1024
		0xF6	10	24 ms	10240
		0xD6	42	101 ms	43008
		0xAD	64	154 ms	65535
		0x00	256	614 ms	65535

Proximity Time Register (0x02)

The proximity timing register controls the integration time of the proximity ADC in 2.4 ms increments. Upon power up, the proximity time register is set to 0xFF. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

$$\text{Max Prox Count} = ((256 - \text{PTIME}) \times 1024)) - 1 \quad \text{up to a maximum of } 65535$$

Table 7. Proximity Time Register

FIELD	BITS	DESCRIPTION			
PTIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.4 ms	1023

Wait Time Register (0x03)

Wait time is set 2.4 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number. Upon power up, the wait time register is set to 0xFF.

Table 8. Wait Time Register

FIELD	BITS	DESCRIPTION			
WTIME	7:0	REGISTER VALUE	WAIT TIME	TIME (WLONG = 0)	TIME (WLONG = 1)
		0xFF	1	2.4 ms	0.029 sec
		0xAB	85	204 ms	2.45 sec
		0x00	256	614 ms	7.4 sec

NOTE: The Proximity Wait Time Register should be configured before PEN and/or AEN is/are asserted.

Clear Interrupt Threshold Registers (0x04 – 0x07)

The Clear interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by the clear channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Table 9. Clear Interrupt Threshold Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
AILTL	0x04	7:0	Clear channel low threshold lower byte
AILTH	0x05	7:0	Clear channel low threshold upper byte
AIHTL	0x06	7:0	Clear channel high threshold lower byte
AIHTH	0x07	7:0	Clear channel high threshold upper byte

Proximity Interrupt Threshold Registers (0x08 – 0x0B)

The proximity interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

Table 10. Proximity Interrupt Threshold Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity ADC channel low threshold lower byte
PILTH	0x09	7:0	Proximity ADC channel low threshold upper byte
PIHTL	0x0A	7:0	Proximity ADC channel high threshold lower byte
PIHTH	0x0B	7:0	Proximity ADC channel high threshold upper byte

Persistence Filter Register (0x0C)

The persistence filter register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each integration cycle or if the integration has produced a result that is outside of the values specified by the threshold register for some specified amount of time. Separate filtering is provided for proximity and the clear channel.

Table 11. Persistence Filter Register

	7	6	5	4	3	2	1	0	
PERS	**PPERS**				**APERS**				**Reset 0x00**

FIELD	BITS	DESCRIPTION	
PPERS	7:4	Proximity interrupt persistence. Controls rate of proximity interrupt to the host processor.	
		FIELD VALUE	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every proximity cycle generates an interrupt
		0001	1 proximity value out of range
		0010	2 consecutive proximity values out of range
		...	...
		1111	15 consecutive proximity values out of range
APERS	3:0	Clear Interrupt persistence. Controls rate of Clear channel interrupt to the host processor.	
		FIELD VALUE	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every RGBC cycle generates an interrupt
		0001	1 clear channel value outside of threshold range
		0010	2 clear channel consecutive values out of range
		0011	3 clear channel consecutive values out of range
		0100	5 clear channel consecutive values out of range
		0101	10 clear channel consecutive values out of range
		0110	15 clear channel consecutive values out of range
		0111	20 clear channel consecutive values out of range
		1000	25 clear channel consecutive values out of range
		1001	30 clear channel consecutive values out of range
		1010	35 clear channel consecutive values out of range
		1011	40 clear channel consecutive values out of range
		1100	45 clear channel consecutive values out of range
		1101	50 clear channel consecutive values out of range
		1110	55 clear channel consecutive values out of range
		1111	60 clear channel consecutive values out of range

Configuration Register (0x0D)

The configuration register sets the wait long time.

Table 12. Configuration Register

	7	6	5	4	3	2	1	0	
CONFIG	Reserved						WLONG	Reserved	Reset 0x00

FIELD	BITS	DESCRIPTION
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.

Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that will be transmitted.

Table 13. Proximity Pulse Count Register

	7	6	5	4	3	2	1	0	
PPULSE	PPULSE								Reset 0x00

FIELD	BITS	DESCRIPTION
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block.

Table 14. Control Register

	7	6	5	4	3	2	1	0	
CONTROL	PDRIVE		Reserved				AGAIN		Reset 0x00

FIELD	BITS	DESCRIPTION	
PDRIVE	7:6	Proximity LED Drive Strength.	
		FIELD VALUE	LED STRENGTH
		00	100 mA
		01	50 mA
		10	25 mA
		11	12.5 mA
Reserved	5:2	Reserved. Write bits as 0	
AGAIN	1:0	RGBC Gain Control.	
		FIELD VALUE	RGBC GAIN VALUE
		00	1× gain
		01	4× gain
		10	16× gain
		11	60× gain

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Table 15. ID Register

	7	6	5	4	3	2	1	0	
ID	ID								Reset ID

FIELD	BITS	DESCRIPTION	
ID	7:0	Part number identification	0x40 = TCS37721 & TCS37725
			0x49 = TCS37723 & TCS37727

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Table 16. Status Register

	7	6	5	4	3	2	1	0	
STATUS	Reserved		PINT	AINT	Reserved		PVALID	AVALID	Reset 0x00

FIELD	BIT	DESCRIPTION
Reserved	7:6	Reserved.
PINT	5	Proximity Interrupt.
AINT	4	Clear channel Interrupt.
Reserved	3:2	Reserved.
PVALID	1	Proximity Valid. Indicates that a proximity cycle has completed since PEN was asserted.
AVALID	0	RGBC Valid. Indicates that the RGBC cycle has completed since AEN was asserted.

RGBC Channel Data Registers (0x14 – 0x1B)

Clear, red, green, and blue data is stored as 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with a read word protocol bit set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Table 17. ADC Channel Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
CDATA	0x14	7:0	Clear data low byte
CDATAH	0x15	7:0	Clear data high byte
RDATA	0x16	7:0	Red data low byte
RDATAH	0x17	7:0	Red data high byte
GDATA	0x18	7:0	Green data low byte
GDATAH	0x19	7:0	Green data high byte
BDATA	0x1A	7:0	Blue data low byte
BDATAH	0x1B	7:0	Blue data high byte

Proximity Data Registers (0x1C – 0x1D)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with a read word protocol bit set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Table 18. PDATA Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATA	0x1C	7:0	Proximity data low byte
PDATAH	0x1D	7:0	Proximity data high byte

APPLICATION INFORMATION: HARDWARE

LED Driver Pin with Proximity Detection

In a proximity sensing system, the IR LED can be pulsed by the TCS3772 with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses.

The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LED, the key goal can be meet. Place a 1-µF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LED anode, and a 22-µF capacitor at the output of the LED voltage regulator to supply the 100-mA current surge.

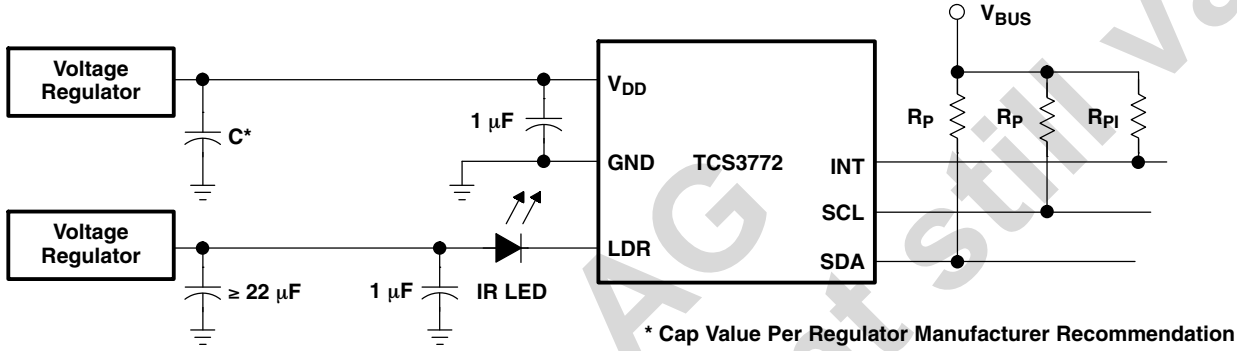


Figure 16. Proximity Sensing Using Separate Power Supplies

If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22-Ω resistor in series with the V_{DD} supply line and a 1-µF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

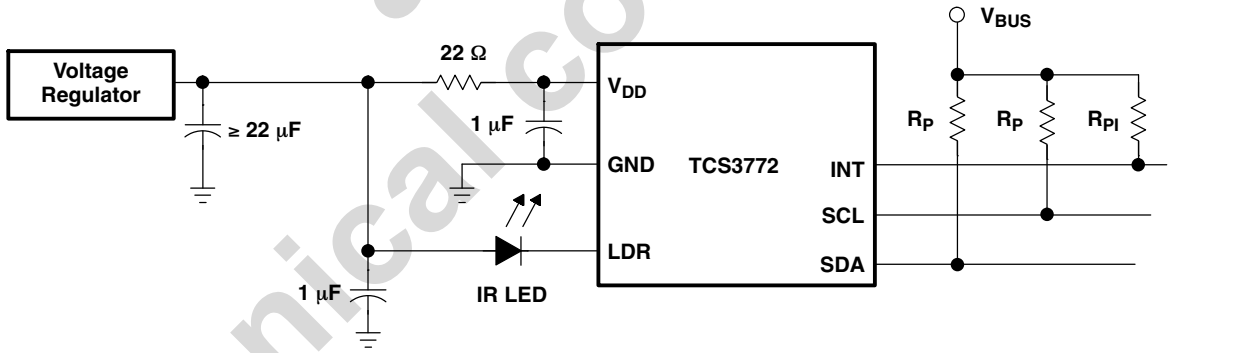


Figure 17. Proximity Sensing Using Single Power Supply

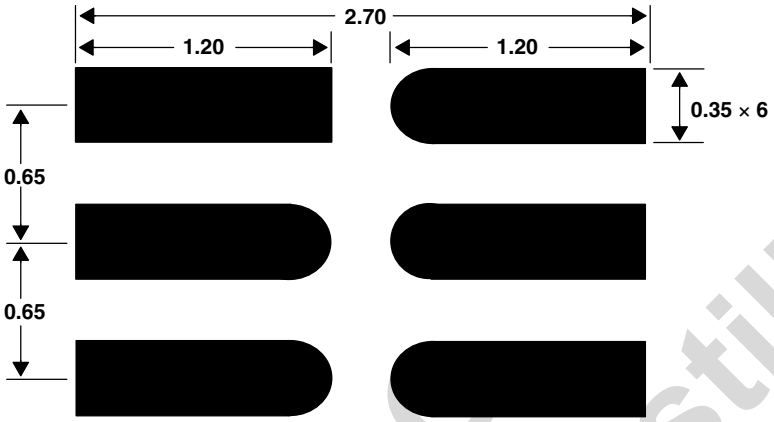
V_{BUS} in the above figures refers to the I^2C bus voltage which is either V_{DD} or 1.8 V. Be sure to apply the specified I^2C bus voltage shown in the Available Options table for the specific device being used.

The I^2C signals and the Interrupt are open-drain outputs and require pull–up resistors. The pull-up resistor (R_P) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The TAOS EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

APPLICATION INFORMATION: HARDWARE

PCB Pad Layout

Suggested land pattern based on the IPC–7351B Generic Requirements for Surface Mount Design and Land Pattern Standard (2010) for the small outline no-lead (SON) package is shown in Figure 18.



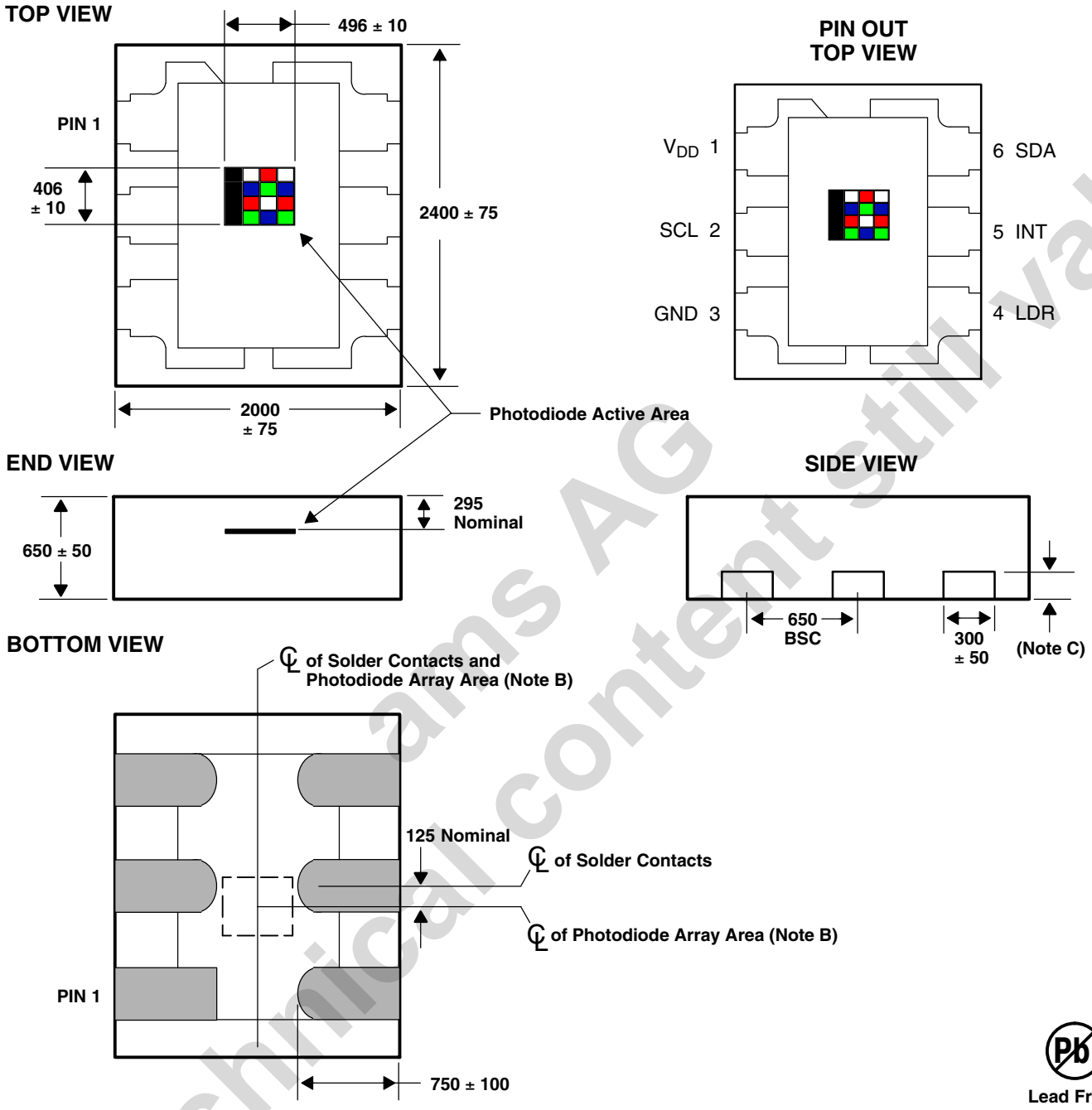
TOP VIEW

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Figure 18. Suggested FN Package PCB Layout

PACKAGE INFORMATION

PACKAGE FN — **Dual Flat No-Lead**



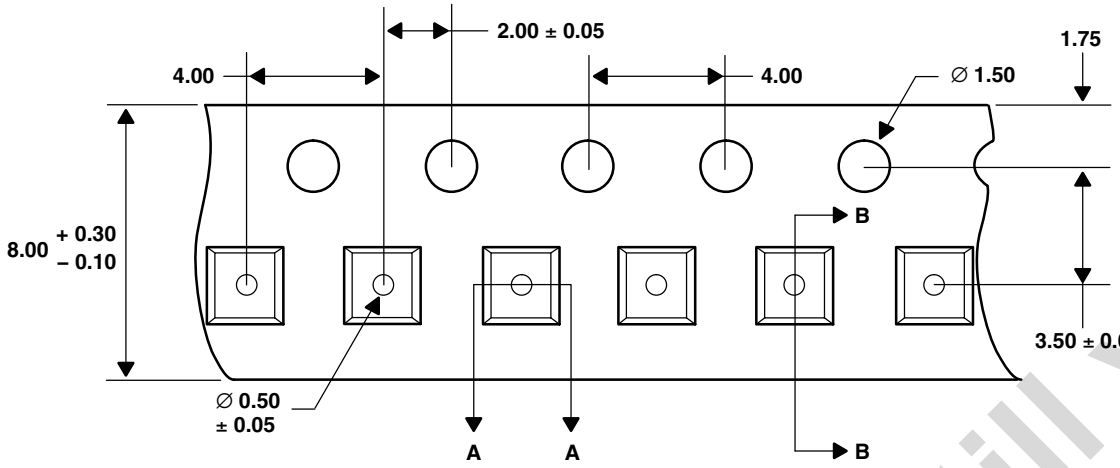
Lead Free

NOTES: A. All linear dimensions are in micrometers.
B. The die is centered within the package within a tolerance of ± 75 µm.
C. Double-Half Etch (DHE) is 97 ± 20 µm. Non-DHE is 203 ± 8 µm.
D. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
E. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
F. This package contains no lead (Pb).
G. This drawing is subject to change without notice.

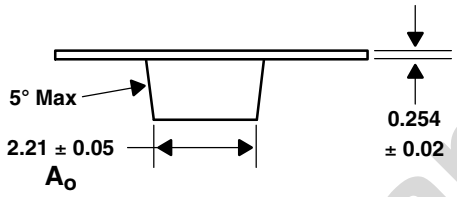
Figure 19. Package FN — Dual Flat No-Lead Packaging Configuration

CARRIER TAPE AND REEL INFORMATION

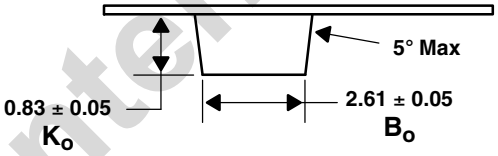
TOP VIEW

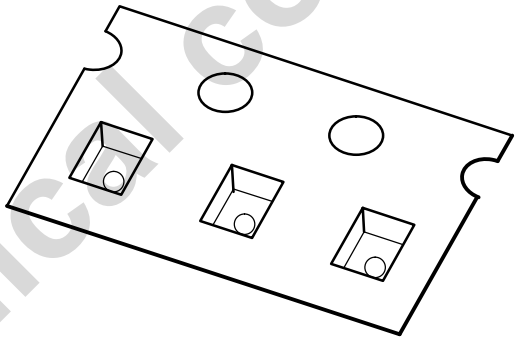


DETAIL A



DETAIL B





NOTES:
A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
D. Each reel is 178 millimeters in diameter and contains 3500 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
G. This drawing is subject to change without notice.

Figure 20. Package FN Carrier Tape

SOLDERING INFORMATION

The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 19. Solder Reflow Profile

PARAMETER	REFERENCE	TCS3772
Average temperature gradient in preheating		2.5°C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T1)	t_1	Max 60 sec
Time above 230°C (T2)	t_2	Max 50 sec
Time above T_{peak} –10°C (T3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/sec

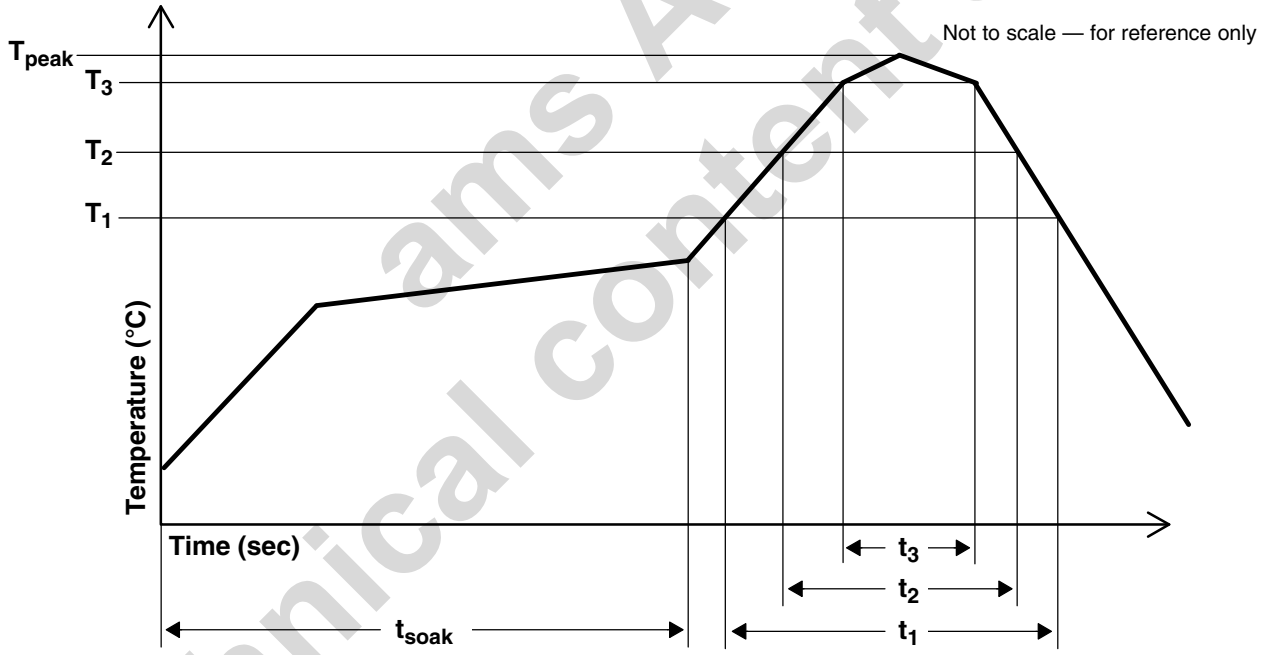


Figure 21. Solder Reflow Profile Graph

STORAGE INFORMATION

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

Shelf Life:	12 months
Ambient Temperature:	< 40°C
Relative Humidity:	< 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The FN package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

Floor Life:	168 hours
Ambient Temperature:	< 30°C
Relative Humidity:	< 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

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