Datasheet

DS000648

TMF8801

Time-of-Flight Sensor

v5-01 • 2020-Apr-28

Abstract

The TMF8801 is a dToF (direct time of flight) optical distance sensor module achieving up to 2500mm target detection distance.

Content Guide

1 General Description

The TMF8801 is a time-of-flight (TOF) sensor in a single modular package with associated VCSEL. The TOF device is based on SPAD, TDC and histogram technology. The device achieves 2500mm detection range.

1.1 Key Benefits & Features

The benefits and features of TMF8801, Time-of-Flight Sensor, are listed below:

Figure 1:
Added Value of Using TMF8801

Benefits	Features
Small footprint fits in the mobile phone bezel	Modular package - 2.2 mm x 3.6 mm x 1.0 mm
Detecting central closest objects	21º FOI
Within 5 % of measurement (accuracy); no multipath and no multiple object problems as for iToF	Time-to-Digital Converter (TDC) Direct Time-of-Flight Measurement
Better accuracy detects reliably closest object Minimum distance 20 mm Maximum distance 2500 mm	Single Photon Avalanche Photodiode (SPAD) Histogram based architecture
No complex calibration	Dynamic cover glass calibration
Compensates for dirt on glass	Reliable Operation under demanding use cases
Improved accuracy over temperature and life	Reference SPAD
Make better decisions	Distance and signal quality reported
Class 1 Eye Safe	Fast VCSEL driver with protection
Longer battery life	27mA power consumption at 30 Hz operation 0.26µA power-down current consumption (EN=0)

1.2 Applications

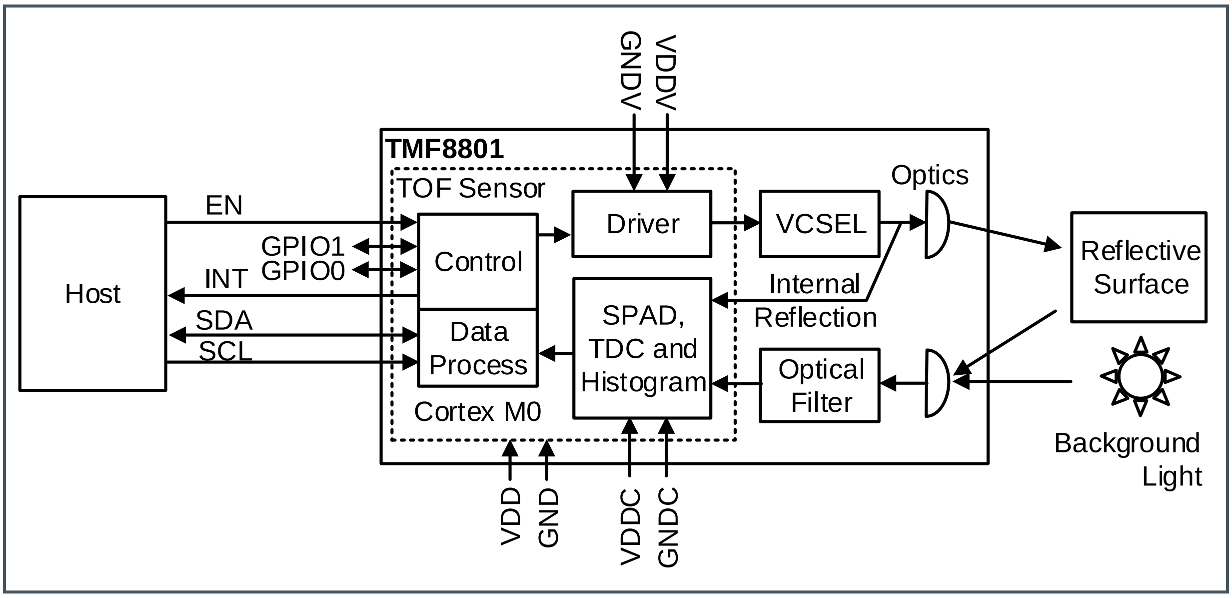
The device is ideal for use in the mobile phone market with applications including:

- Distance measurement for camera autofocus (Laser Detect Autofocus - LDAF)
- Supporting low-power system operation by enabling high-power components (i.e. 3D camera) only when an object is in the detection range
- Presence detection - Object detection
- Collision avoidance

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMF8801



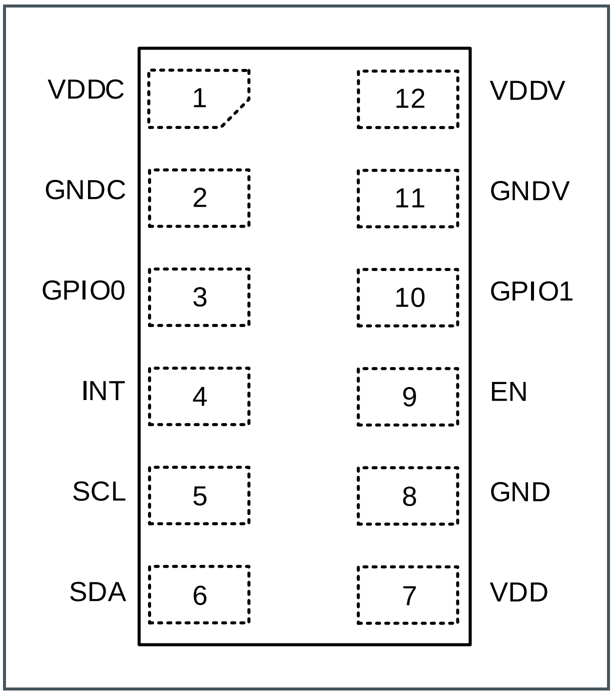
2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
TMF8801-1BM	Optical Module	5-digit tracecode (coded)	Tape & Reel (7'' reels)	500 pcs/reel
TMF8801-1B	Optical Module	5-digit tracecode (coded)	Tape & Reel (13'' reels)	5000 pcs/reel

3 TMF8801 Module Description

3.1 Pin Diagram

Figure 3:
Pin Locations Top Through View (not to scale)



3.2 Pin Description

Figure 4:
Pin Description of TMF8801

Pin Number	Pin Name	Signal Type	Description
1	VDDC	Supply	Charge pump supply voltage (3 V); add a capacitor GRM155R70J104KA01 (0402 X7R 0.1 µF 6.3 V) to GND
2	GNDC	Ground	Charge pump ground; connect all ground pins together
3	GPIO0	I/O	General purpose input/output; default output low; leave open if not used

Pin Number	Pin Name	Signal Type	Description
4	INT	Output	Interrupt. Open-drain output; connect to GND if not used
5	SCL	Input	I²C Serial Clock
6	SDA	I/O	I²C Serial Data
7	VDD	Supply	Chip Supply voltage (3 V); add a capacitor GRM155R70J104KA01 (0402 X7R 0.1 µF 6.3 V) to GND
8	GND	Ground	Chip Ground; connect all ground pins together
9	EN	Input	Enable input active high; setting to low forces the device into shutdown and all memory content is lost; connect to VDD if not used
10	GPIO1	I/O	General purpose input/output; default output low; leave open if not used
11	GNDV	Ground	VCSEL Ground; connect all ground pins together
12	VDDV	Supply	VCSEL Supply voltage (3 V); add a capacitor GRM155R70J104KA01 (0402 X7R 0.1 µF 6.3 V) to GND

(1) SDA, SCL, INT and EN have no diode to any VDD supply. Therefore even with VDD=0 V they do not block the interrupt line or I²C bus.

(2) GPIO0 and GPIO1 are push/pull output and have a diode to VDD; therefore if VDD is not powered, GPIO0 and GPIO1 should not be driven from outside.

4 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5
Absolute Maximum Ratings of TMF8801

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
VDDC, VDDV, VDD	3 V Supply voltage	-0.3	3.6	V	Connect pins VDDC, VDDV, VDD on PCB with very short connections
GNDV, GNDC, GND	Ground	0.0	0.0	V	Connect all GND pins on PCB with very short connections
GPIO0, GPIO1	Digital I/O terminal voltage	-0.3	VDD + 0.3 V max. 3.6 V	V	Protection diode to VDD
INT, SCL, SDA, EN	Digital I/O terminal voltage	-0.3	3.6	V	No protection diodes to any positive supply only to ground
I_SCR	Latch up immunity	± 100		mA	JEDEC JESD78D Nov 2011
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 2000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	± 500		V	JEDEC JESD22-C101F Oct 2013
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	- 40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative Humidity (non-condensing)		85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h with T_{AMB} < 30 °C and < 60 % r.h.

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices."

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

5.1 Recommended Operating Conditions

Device parameters are guaranteed at nominal conditions unless otherwise noted. While the device is operational across the temperature range, functionality will vary with temperature.

Figure 6:
Recommended Operating Conditions of TMF8801

Symbol	Parameter	Min	Typ	Max	Unit	Comment
VDDV, VDDC, VDD	3 V supply voltage	2.7	3	3.3	V	
Temperature Range	Free-air temperature	-30	25	70	°C	Operational

6 Typical Operating Characteristics

Following operating characteristics are measured with calibrated devices with full optical stack including glass and IR ink with >90 % transmissivity. The airgap is set to 0.38 mm. The ambient light is measured on the 1 m x 1 m target. A very diffuse scotch magic tape 810 is used for measurement with smudge.

Figure 7:
350 Lux Fluorescent Light and 18% Grey Card

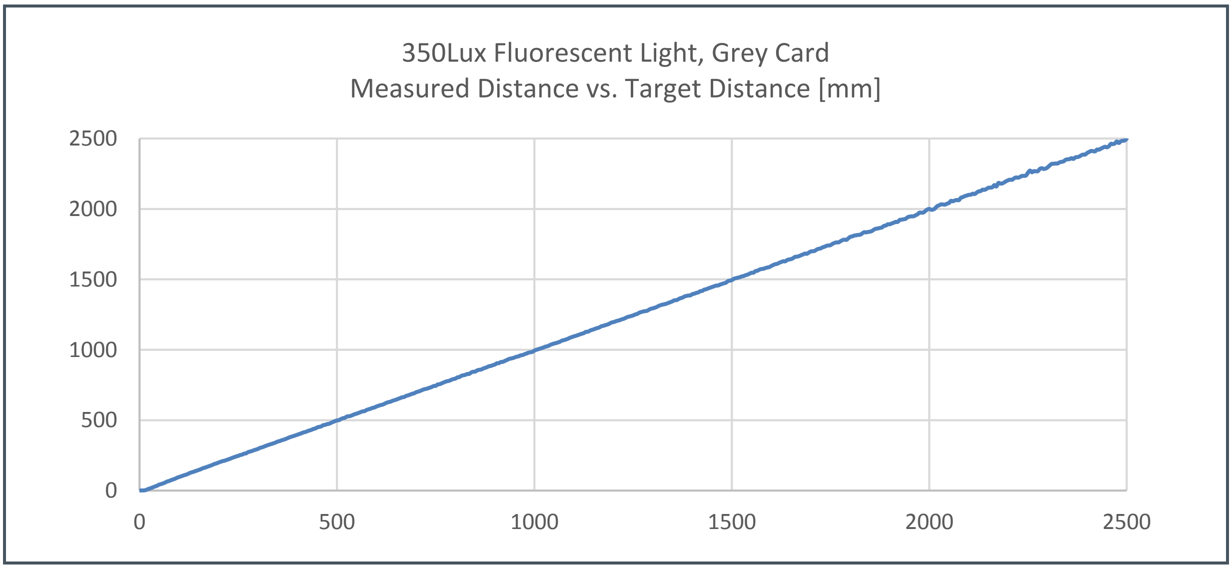


Figure 8:
350 Lux Fluorescent Light, 18% Grey Card and Smudge on Glass

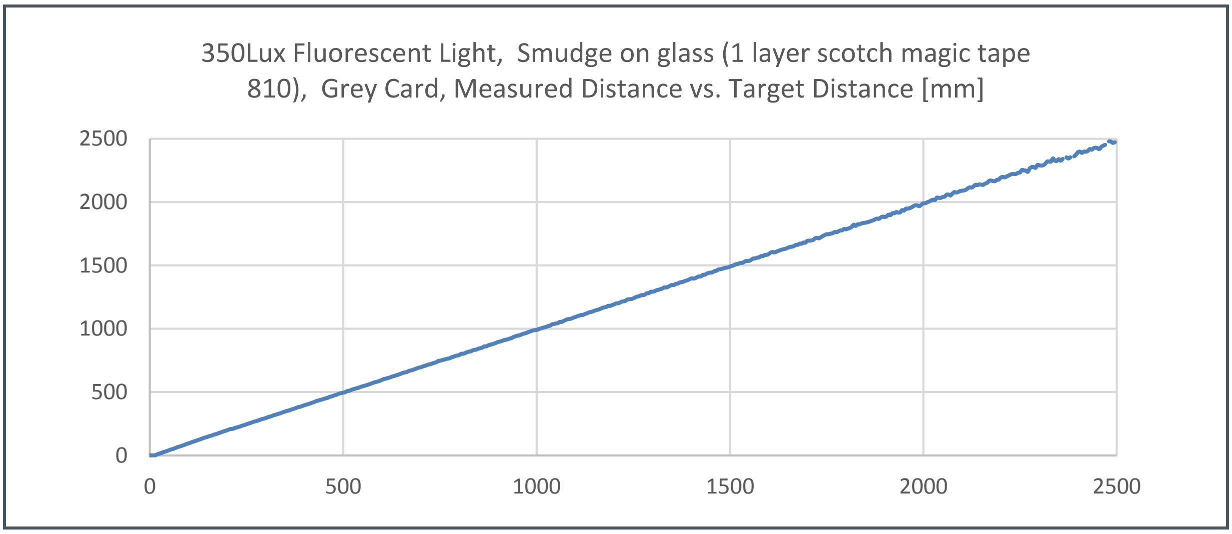


Figure 9:
1.4k Lux Halogen Light and 18% Grey Card

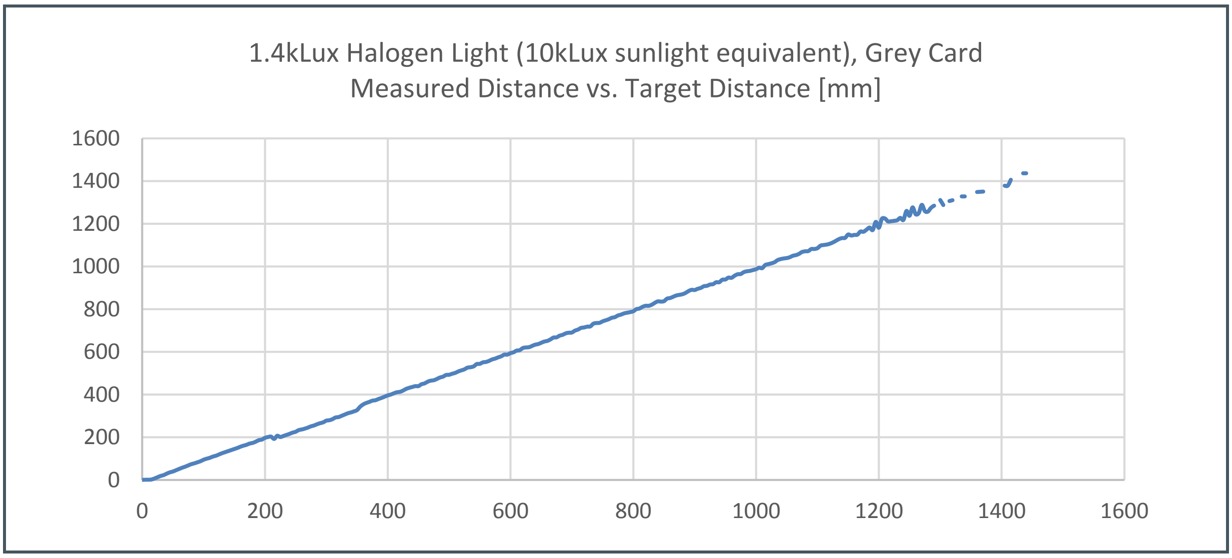


Figure 10:
14k Lux Halogen Light and 18% Grey Card

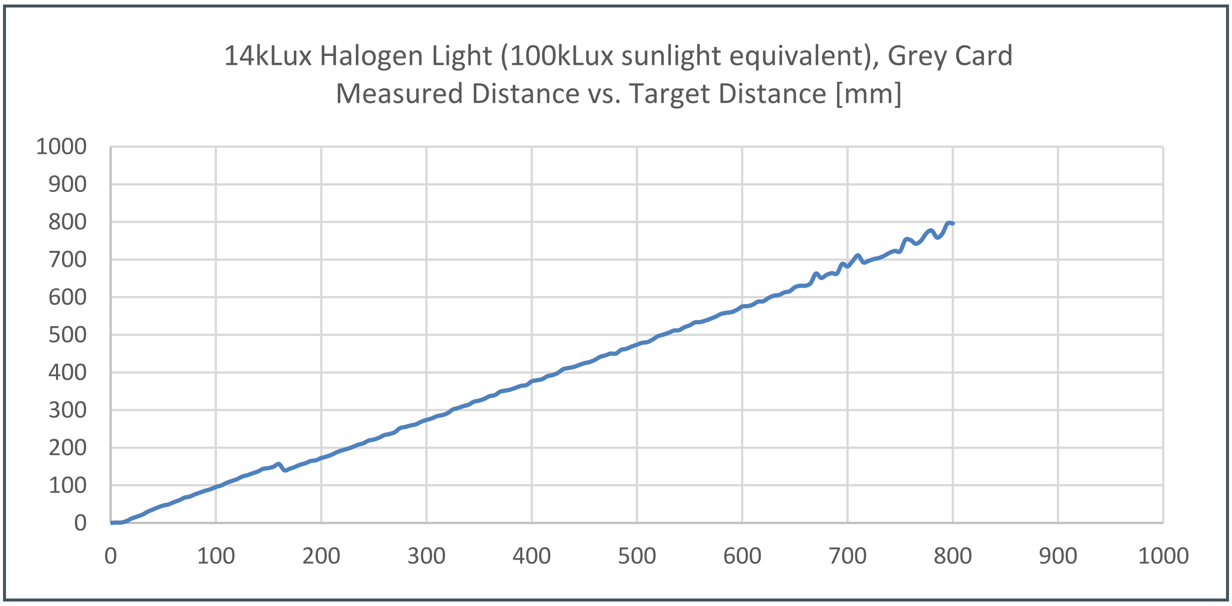
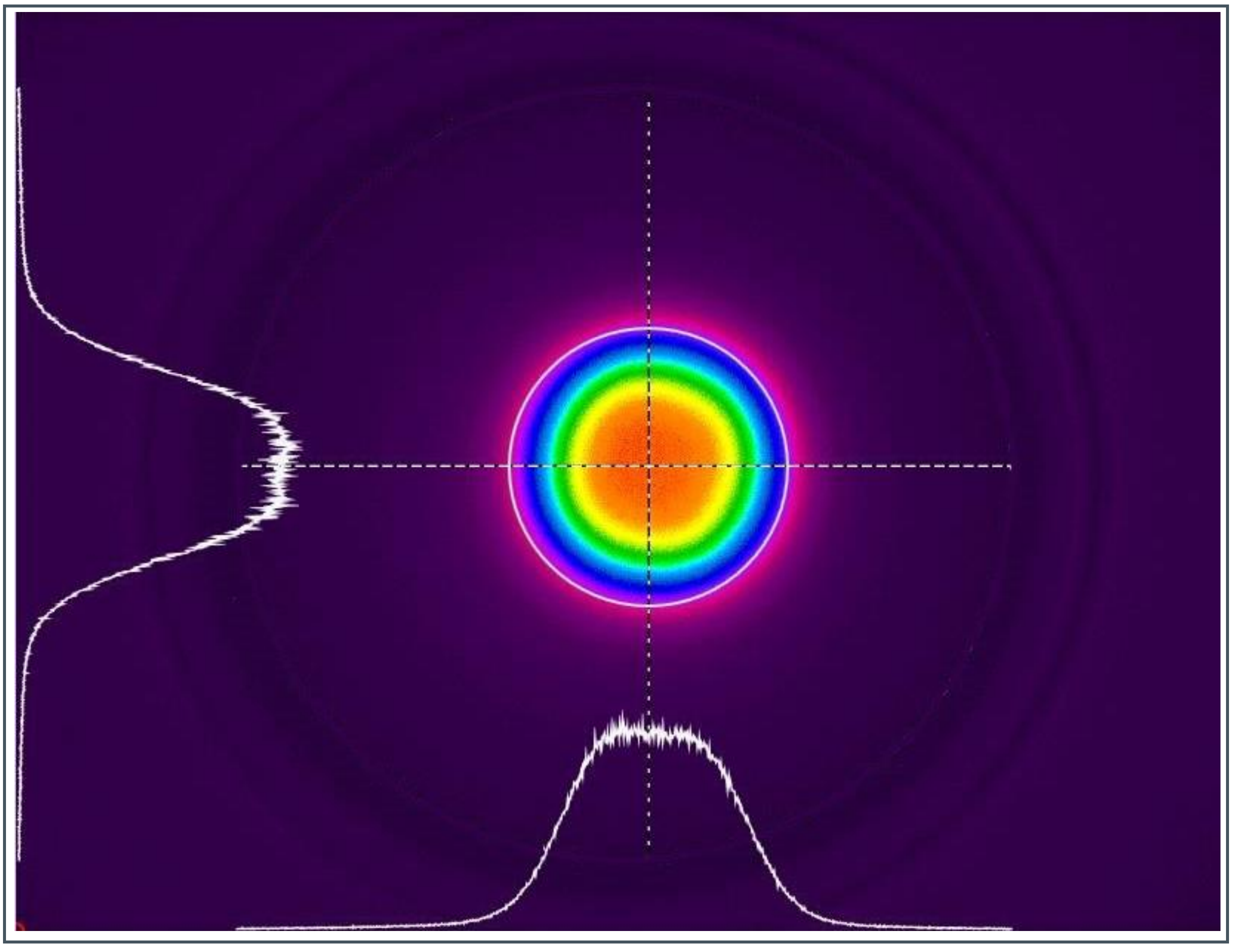


Figure 11:
Field of Illumination of VCSEL (FOI), X-Axis: ±10.4°, Y-Axis: ±10.31°, 1/e²



7 Functional Description

7.1 I²C Protocol

The TMF8801 is controlled by an I²C bus, one interrupt pin and two GPIO pins.

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and standard, fast mode and fast mode plus modes. Read and Write transactions comply with the standard set by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Internal to the device, an 8-bit buffer stores the register address location of the byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESSWRITE, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The default I2C address is 0x41. The address can be changed after power-up. Use the enable pin to enable only one device at a time to provide unique device addresses.

7.2 System Parameters

The on-chip microprocessor is a Cortex M0 µP.

Figure 12:
ARM M0 Parameters

Parameter	Min	Nom	Max	Units	Comment
µP Operating Frequency		5.37	86	MHz	The CPU can operate with the RC oscillator directly or with a 16x PLL; frequency tuning adjusts the default frequency to 4.7MHz
RAM			32	kB	
ROM			32	kB	
Max PLL Frequency		172		MHz	for 5.37MHz RC clock

7.3 I/O

Figure 13:
Typical I/O Level Specification

Symbol	Parameter	Condition	Min	Typ	Max	Units
ILEAK	SDA, SCL, GPIO0/1, EN, INT		-5		5	µA
VIH[1]	SDA, SCL, GPIO0/1, EN		1.26			V
VIL_I2C[1]	SDA, SCL	2.7 V<VDD<2.9 V, <400 kHz I^{2}C speed			0.3	V
		VDD >2.9 V, <400 kHz I^{2}C speed			0.54	
		2.8 V<VDD<3.0 V, <1 MHz I^{2}C speed			0.3	
		VDD>3.0 V, <1 MHz I^{2}C speed			0.54	
VIL	GPIO0/1, EN				0.54	V
VOL	SDA, GPIO0/1, INT	2 mA sink	0		0.36	V
		4 mA sink	0		0.6	V
IDRIVE_H	GPIO0/1	1 V applied on GPIO	3.6			mA
IDRIVE_L	GPIO0/1	1 V applied on GPIO	3.9			mA

(1) The input highlevel VIH and lowlevel VIL is defined to support a pullup supply of 1.8 V ±5 %

7.4 Power Consumption

All current consumption values include silicon process variation. Temperature and voltages are at nominal conditions (23 ºC and 2.8 V).

Figure 14:
Power Consumption

Parameter	Condition	Min	Nom	Max	Units	Comment
I_VDD Powerdown	Enable Pin Low I²C Off	0.02	0.26	1	µA	State: Powerdown
I_VDD Standby CPU Off, RAM On OSC Off, pon=0 I²C Wakeup Only			85		µA	State: Standby
I_VDD Wait CPU Off, RAM On, OSC On 5 MHz I²C On, Timer Wakeup			140		µA	State: Wait
I_VDD Ranging Processing CPU Running at 80 MHz No VCSEL, No TDC			2.7		mA	State: Histogram processing
I_VDD Ranging Active CPU stopped VCSEL_clk_div2=0 (default), TDCs running			32.5		mA	State: Ranging active
I_VDD Ranging Active CPU stopped VCSEL_clk_div2=1, TDCs running			25.2		mA	State: Ranging active
I_VDD Ranging 30 Hz, 33 ms, default settings			27		mA	Average power consumption
Peak VCSEL Current			230		mA	
Max VCSEL Duty Cycle			2		%	

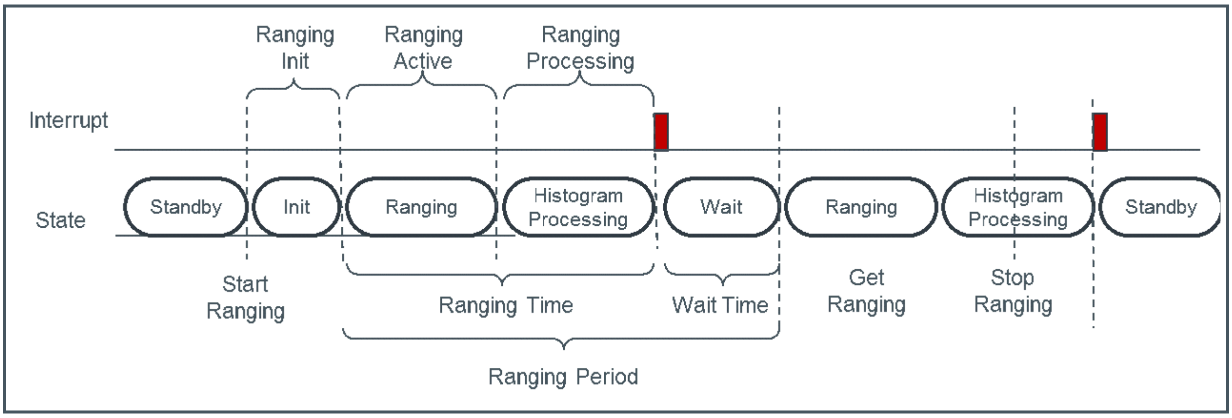
7.5 Timing

7.5.1 Ranging Acquisition Timing

Figure 15:
Ranging Acquisition Timing

Parameter	Min	Nom	Max	Units	Comment
Ranging Time Default Settings		33		ms	Varies with operational mode
Ranging Init (including electrical calibration)		8		ms	Only done on startup and if temperature changed from last calibration
Ranging Period			209	ms	Programmable by the interface

Figure 16:
Ranging Timing Diagram



7.5.2 Reset Pin and Power-Up Timing

Figure 17:
Reset Pin and Power-Up Timing

Parameter	Min	Nom	Max	Units	Comment
Power On (Boot Time)		3		ms	Does not include RAM download time
Enable high to ready for measurement		8		ms	

Parameter	Min	Nom	Max	Units	Comment
Standby to Active Time		<<1		ms	
Active to Standby Time		<<1		ms	
Enable Low to Power Down Time		<<1		ms	

7.6 Algorithm Performance

As the performance of the algorithm is dependent on the ROM version, following section only applies for devices with order code TMF8801-1**B** (and TMF8801-1**B**M), calibrated and in-application oscillator calibration using the reference driver code and patched with the latest software patch from **ams** – contact **ams** to identify latest patch version.

To achieve the full distance of 250 cm, the on chip oscillator needs to be tuned to 4.7 MHz.

The TMF8801 is embedded in the application using a 0.38 mm airgap and a glass with an IR ink with >90 % transmissivity. The glass thickness is 0.5 mm. An additional mask on the opaque ink is implemented according to TMF8801 optical design guide (external document).

7.6.1 Calibration

To achieve the performance described in the next sections, a calibration of the algorithm needs to be performed (command = 0x0A). The TMF8801 shall be embedded in the final application and the cover glass including the IR ink needs to be assembled. The calibration test shall be done in a housing with minimal ambient light and no target within 40 cm in field of view of the TMF8801.

The TMF8801 generates a calibration data set which is permanently stored on the host.

On each power-up of the TMF8801 the calibration data set is sent by I^2C to the TMF8801 prior to execution of any algorithms (commands=0x02 or 0x0B).

7.6.2 Algorithm Timings

The TMF8801 can adjust the number of iterations and detection threshold using registers. A default mode is defined having 900k iterations and threshold=0.

Figure 18:
Algorithm Timings

Parameter	Condition	Min	Nom	Max	Units
Default mode	command=0x02 or 0x03 cmd_data6=0xA3, cmd_data3=0x00, cmd_data1=0x03, cmd_data0=0x84 (900k iterations)		33		ms

7.6.3 Algorithm Performance Parameters

The algorithm reports distance information of the closest object in 1 mm steps.

Using the timings described in 7.6.2 following performance is achieved:

Figure 19:
Object Detection Algorithm Parameters

Parameter	Condition	Min	Nom	Max	Units
Reflectivity of object at 940 nm	Perpendicular to TMF8801	18		90	%
Maximum distance detection, 1.5 m x 1.5 m object	350 lux fluorescent on object, 18% grey card		2500(1)		mm
	360 lux halogen light on object(2), 88% white card		2500(1)		mm
	360 lux halogen light on object(2), 18% grey card		1700		mm
	1400 lux halogen light on object(3), 88% white card		1600		mm
	1400 lux halogen light on object(4), 18% grey card		1250		mm
	14000 lux halogen light on object(4), 18% grey card		600		mm
Minimum distance detection, 18 % grey card, 20 cm x 26 cm			20		mm
Accuracy	Object distance ≥ 200mm		±5		%
	100mm< object distance <200mm		±10		mm
	20mm< object distance <100mm		±15		mm
Transition short to long distance mode			200		mm

(1) To achieve the full distance, the oscillator need to be tuned to 4.7 MHz. Use **ams** reference code to implement clock frequency tuning.
Any target reported above 2500 mm should be considered as no object.
(2) 360 lux halogen light represents 2.5 k sunlight equivalent; light on object only.
(3) 1400 lux halogen light represents 10 k sunlight equivalent; light on object only
(4) 14000 lux halogen light represents 100 k sunlight equivalent; light on object only

7.7 VCSEL

Internal protection ensures no single point of failure will cause the VCSEL to violate the Class 1 Laser Safety.

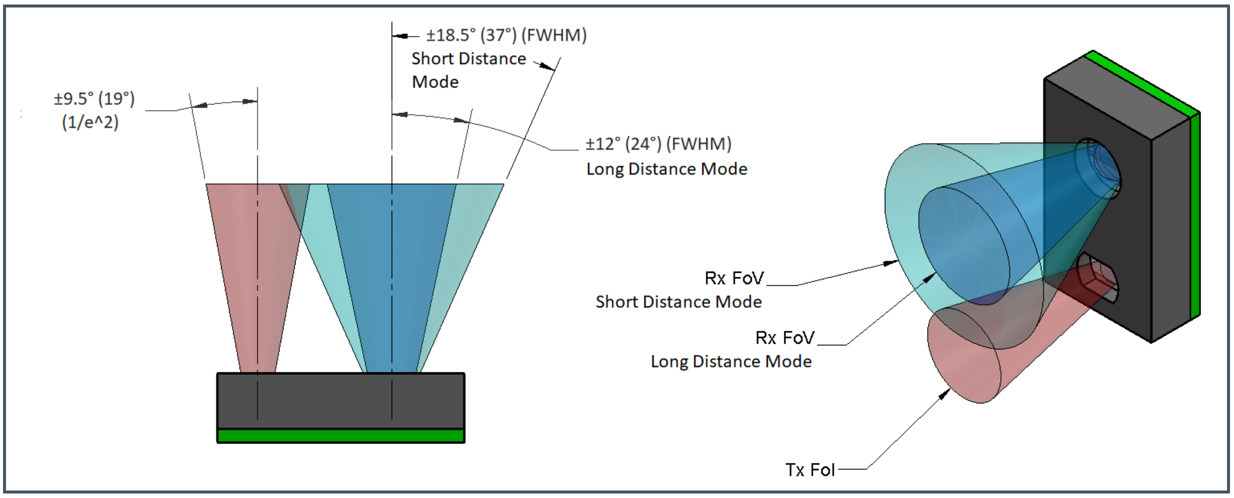
- Laser Safety: Class 1
- VCSEL Pulse Rep Rate: 23 ns (43 MHz; 37.6MHz if clock frequency tuned to 4.7MHz)
  If VCSEL_clk_div=1 the frequency is divided by two.

7.8 Typical Optical Characteristics

- VCSEL Field of Illumination (FOI): 21º full width from 5% of maximum up to maximum
  19º 1/e^2
- TOF Sensor Field of View (FOV): 37º FWHM – for short distances
  24º FWHM – for long distances

The SPAD FoV angular response uses the full TMF8801 SPADs for short distances. The SPAD FoV is reduced when the TMF8801 operates in long distance since the SPAD array is reduced. This helps to improve ambient light tolerance.

Figure 20:
FOI/FOV of TMF8801



7.8.1 Filter Characteristics:

• FWHM	56 nm
• Passband Center Frequency	940 nm
• Min Stopband Frequency	350 nm
• Max Stopband Frequency	1100 nm

8 Register Description

8.1 APPID Register (Address 0x00)

Figure 21:
APPID Register

Addr: 0x00			APPID	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	appid	0	RW	Currently running application: 0xC0 App0 – Measurement application running 0x80 bootloader running

8.2 APPREV_MAJOR Register (Address 0x01)

Figure 22:
APPREV_MAJOR Register

Addr: 0x01			APPREV_MAJOR	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	apprevMajor	0	RW	Application major revision

8.3 APPREQID Register (Address 0x02)

Figure 23:
APPREQID Register

Addr : 0x02			APPREQID	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	appReqid	0	RW	Application that shall be started, set this to 0x80 … bootloader 0xC0 …. App0 – measurement application and wait until register 0x00 (APPID) shows this as application.

8.4 ENABLE Register (Address 0xE0)

Figure 24:
ENABLE Register

Addr: 0xE0			ENABLE	
Field	**Name**	**Rst**	**Type**	**Description**
7	cpu_reset	0	RW_SC	Write a '1' here to reset CPU. This generates global reset, fully resetting CPU and all CPU registers. The bit resets itself, no need to explicitly clear it.
6	cpu_ready	0	RO	CPU is ready to handle I²C - if this bit is zero, then only the registers 0xe0 and above are usable, the memory mapped I²C space is not used. Bit gets set only explicitly by software, therefore a functional and running firmware is necessary for this bit to work.
0	pon	1	R_PUSH	1=activate oscillator 0=ask cpu to go to standby Activating the oscillator is implemented in hardware. Whenever this register is '0' and a '1' is being written, the oscillator is being started and CPU receives a PON1 interrupt. It is implemented in the bootloader to execute a reset at this point, but the application goes to an IDLE state. De-activating the oscillator is a software assisted process. It is important that the CPU powers down all modules properly before turning off the oscillator, therefore this is implemented in firmware. So writing a '0' to this register will trigger an internal CPU interrupt. The firmware, after powering down everything, sets the device into standby state.

8.5 INT_STATUS Register (Address 0xE1)

Figure 25:
INT_STATUS Register

Addr: 0xE1			INT_STATUS	
Field	**Name**	**Rst**	**Type**	**Description**
1	int2	0	R_PUSH1	Raw histogram available interrupt for App0; asserted when a raw histogram can be retrieved from I²C. int2 status. If bis is asserted, and int2_enab is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear int1 condition.

Addr: 0xE1			INT_STATUS	
Field	**Name**	**Rst**	**Type**	**Description**
0	int1	0	R_PUSH1	Object detection interrupt for App0; asserted when a result from object detection is available int1 status. If bis is asserted, and int1_enab is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear int1 condition.

8.6 INT_ENAB Register (Address 0xE2)

Figure 26:
INT_ENAB Register

Addr: 0xE2			INT_ENAB	
Field	**Name**	**Rst**	**Type**	**Description**
1	int2_enab	0	RW	Raw histogram available interrupt for App0; asserted when a raw histogram can be retrieved from I²C. 0=disabled, 1=enabled -> INT output is active if int2 flag is "1"
0	int1_enab	0	RW	Object detection interrupt for App0; asserted when a result from object detection is available 0=disabled, 1=enabled -> INT output is active if int1 flag is "1"

8.7 ID Register (Address 0xE3)

Figure 27:
ID Register

Addr: 0xE3			ID	
Field	**Name**	**Rst**	**Type**	**Description**
5:0	id	0	RO	Chip ID, reads 07h – do not rely on register bits 6 and 7 of this register.

8.8 REVID Register (Address 0xE4)

Figure 28:
REVID Register

Addr: 0xE4			REVID	
Field	**Name**	**Rst**	**Type**	**Description**
2:0	rev_id	0	RO	Chip revision ID

8.9 App0 Registers – appid=0xC0

Following registers are only available if appid=0xC0 (App0):

8.9.1 CMD_DATA9 Register (Address 0x06)

Figure 29:
CMD_DATA9 Register

Addr: 0x06			CMD_DATA9	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data9	0	W	Command data 9 – see COMMAND Register (Address 0x10); for future extension of commands

8.9.2 CMD_DATA8 Register (Address 0x07)

Figure 30:
CMD_DATA8 Register

Addr: 0x07			CMD_DATA8	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data8	0	W	Command data 8 – see COMMAND Register (Address 0x10); for future extension of commands

8.9.3 CMD_DATA7 Register (Address 0x08)

Figure 31:
CMD_DATA7 Register

Addr: 0x08			CMD_DATA7	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data7	0	W	Command data 7 – see COMMAND Register (Address 0x10)

8.9.4 CMD_DATA6 Register (Address 0x09)

Figure 32:
CMD_DATA6 Register

Addr: 0x09			CMD_DATA6	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data6	0	W	Command data 6 – see COMMAND Register (Address 0x10)

8.9.5 CMD_DATA5 Register (Address 0x0A)

Figure 33:
CMD_DATA5 Register

Addr: 0x0A			CMD_DATA5	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data5	0	W	Command data 5 – see COMMAND Register (Address 0x10)

8.9.6 CMD_DATA4 Register (Address 0x0B)

Figure 34:
CMD_DATA4 Register

Addr: 0x0B			CMD_DATA4	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data4	0	W	Command data 4 – see COMMAND Register (Address 0x10)

8.9.7 CMD_DATA3 Register (Address 0x0C)

Figure 35:
CMD_DATA3 Register

Addr: 0x0C			CMD_DATA3	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data3	0	W	Command data 3 – see COMMAND Register (Address 0x10)

8.9.8 CMD_DATA2 Register (Address 0x0D)

Figure 36:
CMD_DATA2 Register

Addr: 0x0D			CMD_DATA2	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data2	0	W	Command data 2 – see COMMAND Register (Address 0x10)

8.9.9 CMD_DATA1 Register (Address 0x0E)

Figure 37:
CMD_DATA1 Register

Addr: 0x0E			CMD_DATA1	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data1	0	W	Command data 1 – see COMMAND Register (Address 0x10)

8.9.10 CMD_DATA0 Register (Address 0x0F)

Figure 38:
CMD_DATA0 Register

Addr: 0x0F			CMD_DATA0	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	cmd_data0	0	W	Command data 0 – see COMMAND Register (Address 0x10)

8.9.11 COMMAND Register (Address 0x10)

Figure 39:
COMMAND Register

<table>
<tr><th colspan="4">Addr: 0x10</th><th colspan="2">COMMAND</th></tr>
<tr><th>Field</th><th>Name</th><th>Rst</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td>7:0</td><td>command</td><td>0</td><td>RW</td><td></td><td>Direct the device to control or select contents of the registers from 0x20...0xDF</td></tr>
<tr><td></td><td></td><td></td><td></td><td>Setting</td><td>Meaning</td></tr>
<tr><td></td><td></td><td></td><td></td><td>0x00</td><td>No command</td></tr>
<tr><td></td><td></td><td></td><td></td><td>0x02</td><td>Set flag to perform target distance measurement with 8 bytes of data containing where including setting of calibration (and algorithm state) configuration.

cmd_data7 = Bit mask which calibration/state data was downloaded from the host to TMF8801 prior to setting this command:
Bits — Definition
0 — dataFactoryCal: When 1 data from register 0x20 onward includes factory calibration
1 — dataAlgState: If set, also set dataFactoryCal=1. Data from register 0x20 onwards includes factory calibration and algorithm state.

cmd_data6… cmd_data0: Identical to command=0x03.</td></tr>
<tr><td></td><td></td><td></td><td></td><td>0x03</td><td>Set flag to perform target distance measurement with 7 bytes of data containing where

cmd_data6 = Bit mask which algorithm is used
Bits — Definition
0 — Set to ‘1’
1 — Set to ‘1’
2 — VCSEL_clk_div2: If set, operates the VCSEL clock at half frequency - see section 7.7 - and doubles the ranging active time where the VCSEL is enabled. It is recommended to use together with spread_spectrum_mode=1.
3 — Reserved; set to 0b.
4 — algImmediateInterrupt – When 1 target distance measurement will immediately report to the host an interrupt of the capturing caused by a GPIO event; when 0, will only report to the host when target distance measurement was finished
5 — When 1 combine the capture of the short and long distance histogram for maximum speed
6 — Reserved; set to 0.
7 — When 1 do not go to standby between measurements (faster measurement times but higher current consumption)</td></tr>
</table>

cmd_data5 = Bits for GPIO control

Bits	Definition
3:0	GPIO0 settings 0 – Input 1 - Input: active low disables collection, immediately abandoning current measurement. Returning to high restarts new measurement 2 - Input: active high disables collection, immediately abandoning current measurement. Returning to low restarts new measurement 3 - Output: VCSEL pulse output – see cmd_data4 4 - Output low (default after startup) 5 - Output high 6:15 – Reserved, do not use
7:4	GPIO1 settings 0 - Input 1 - Input: active low disables collection, immediately abandoning current measurement. Returning to high restarts new measurement 2 - Input: active high disables collection, immediately abandoning current measurement. Returning to low restarts new measurement 3 - Output: VCSEL pulse output – see cmd_data4 4 - Output low (default after startup) 5 - Output high 6:15 – Reserved, do not use

cmd_data4 = If cmd_data5 enables VCSEL pulse output for GPIO0 and/or GPIO1, cmd_data4 sets its timings as follows:

Value	Meaning
0	No signal
1	GPIOx, rises 0 µs time before VCSEL pulse starts
2	GPIOx rises 100 µs before VCSEL pulse
3	GPIOx rises 200 µs before VCSEL pulse and so on

The falling edge of GPIOx happens at the same time the VCSEL stops emitting light.

cmd_data3 = Object detection threshold and spread spectrum mode

Bits	Definition
5:0	Object detection threshold – use 0 as default value
6	spread_spectrum_mode: If set, avoids aliasing of objects into measurement range. Use together with VCSEL_clk_div2=1 otherwise maximum distance is reduced and false objects at far distance can occur.
7	Set to ‘0’

cmd_data2 = repetition_period in mSec, use 0 for single measurement; if the repetition period is set lower than the ranging time for this mode, the TMF8801 runs at it maximum possible speed (best effort approach).

cmd_data1 = Number of iterations, low byte; 1 LSB=1 k

cmd_data0 = Number of iterations, high byte; 1 LSB=1 k*256

Once a measurement is finished, the interrupt is asserted if it is enabled by int1_enab. Additionally the transaction ID tid is updated

<table>
<tr><th colspan="4">Addr: 0x10</th><th colspan="2">COMMAND</th></tr>
<tr><th>Field</th><th>Name</th><th>Rst</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td>0x0A</td><td>Perform factory calibration in the final customer application including cover glass, no ambient light and no target.
The result from the factory calibration is stored from register 0x20 onwards (14 bytes).</td></tr>
<tr><td></td><td></td><td></td><td></td><td>0x0B</td><td>Set flag to download calibration (and algorithm state) configuration to TMF8801

cmd_data0 = Bit mask which calibration/state data was downloaded from the host to TMF8801 prior to setting this command:

Bits — Definition
0 — dataFactoryCal: when 1 data from register 0x20 onward includes factory calibration
1 — dataAlgState: if set, also set dataFactoryCal=1. Data from register 0x20 onwards includes factory calibration and algorithm state.</td></tr>
<tr><td></td><td></td><td></td><td></td><td>0x0F</td><td>Set gpio control setting without actually performing a measurement as commands 0x02 or 0x03 would do:

cmd_data0 = Bits for GPIO control
Bits — Definition
3:0 — GPIO0 settings
0 – Input
1 - Input: active low disables collection, immediately abandoning current measurement. Returning to high restarts new measurement
2 - Input: active high disables collection, immediately abandoning current measurement. Returning to low restarts new measurement
3 - Output: VCSEL pulse output
4 - Output low
5 - Output high
6:15 – Reserved, do not use
7:4 — GPIO1 settings
0 - Input
1 - Input: active low disables collection, immediately abandoning current measurement. Returning to high restarts new measurement
2 - Input: active high disables collection, immediately abandoning current measurement. Returning to low restarts new measurement
3 - Output: VCSEL pulse output
4 - Output low
5 - Output high
6:15 – Reserved, do not use</td></tr>
<tr><td></td><td></td><td></td><td></td><td>0x30</td><td>Enable histogram readout; the internal state machine will stop when a histogram (e.g. calibration) is available and wait for readout by the host. If the selected histogram is readout, the host shall continue the state machine by sending command 0x32

cmd_data3 = Bitmask for the histograms to be readout:
Bit — Definition
0 — Always set to ‘0’
1 — Set to get electrical calibration histograms
2 — Set to get optical calibration histogram</td></tr>
</table>

Addr: 0x10				COMMAND	
Field	**Name**	**Rst**	**Type**	**Description**	
					3 Always set to ‘0’ 4 Set to get short distance histograms 6:5 Always set to ‘00’ 7 Set to get distance measurement histograms. Bin 127 respectively bin 255 is used as scaling factor for this type of histograms. The scaling factor is 0 for no scaling, 1 for 2x, 2 for 4x and so on. **cmd_data2** = Set to 0x00 **cmd_data1** = = Bitmask for pileup correct histograms readout: Bit Definition 0 Set to get pileup corrected distance measurement histograms 1 Set to get pileup corrected sum histogram 2 Set bit 2 to get pileup corrected short distance histogram 7:3 Always set to 0 **cmd_data0** = set to 0x00 Once above bitmask is set, the device is programmed to stop when the histogram is available. Set command=0x04 to actually perform the measurement.
				0x32	After the host has readout the histogram, continue with internal processing.
				0x47	Read out serial number – results see section 0 Serial Number Readout
				0x49	Change the I²C address of TMF8801 **cmd_data0** = Condition if I²C address is changed; program the GPIOs input/output accordingly before using this feature (commands 0x02, 0x03 or 0x0F): Bit Definition 0 mask_gpio0 1 mask_goio1 2 value_gpio0 3 value_gpio1 7:4 always set to 0 The I²C address change is executed only if (mask_gpio1 & GPIO1) << 1 + (mask_gpio0 & GPIO0) == value_gpio1 << 1 + value_gpio0 where GPIO1 and GPIO0 is the current status on pin GPIO1 and pin GPIO0. If this conditional programming is not used, set cmd_data0 to 0x00. **cmd_data1** = New I²C address Bit Definition 0 Set to ‘0’ 7:1 New I²C address to be used

Addr: 0x10				COMMAND	
Field	Name	Rst	Type	Description	
				0x80.. 0x93	Read 1 quarter of one histogram - copy histogram bits[4:2] to select TDC0…TDC4, quarter bits[1:0] into 0x20..0x9f NOTE: At the end of the transaction of read a quarter, the contents of the registers from 0x20-0x9F will be automatically updated, and the contents of registers REGISTER_CONTENTS and TID will be updated NOTE: At the end of a TDC, the TDC number will also auto increment.
				0xFF	Stop whatever you are doing as soon as possible and reenter the idle state. The current state will not be interrupted and will require leaving the current state processing to take effect. This command will stop continuous measurement.

8.9.12 PREVIOUS Register (Address 0x11)

Figure 40:
PREVIOUS Register

Addr: 0x11			PREVIOUS	
Field	Name	Rst	Type	Description
7:0	previousCommand	0	RO	Previous command that was executed (or current if continues mode is selected)

8.9.13 APPREV_MINOR Register (Address 0x12)

Figure 41:
APPREV_MINOR Register

Addr: 0x12			APPREV_MINOR	
Field	Name	Rst	Type	Description
7:0	appRevMinor	0	RO	Application minor revision

8.9.14 APPREV_PATCH Register (Address 0x13)

Figure 42:
APPREV_PATCH Register

Addr: 0x13			APPREV_PATCH	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	appRevPatch	0	RO	Application patch number

8.9.15 STATUS Register (Address 0x1D)

Figure 43:
STATUS Register

Addr: 0x1D			STATUS	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	status	0	RO	Current status or current general operation Reading — Meaning 00h-0Fh — OK 10h-FFh — Error

8.9.16 REGISTER_CONTENTS Register (Address 0x1E)

Figure 44:
REGISTER_CONTENTS Register

Addr: 0x1E			REGISTER_CONTENTS	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	register_contents	0	RO	Current contents of the I²C RAM from 0x20 to 0xEF ; the coding is as follows: Reading — Meaning 0Ah — Calibration data 47h — Serial number 55h — Results for commands 0x02/0x03 and 0x04

Addr: 0x1E			REGISTER_CONTENTS	
Field	Name	Rst	Type	Description
			80h-93h	Raw histogram data where 80h = TDC0, bin 0…63 81h = TDC0, bin 64…127 82h = TDC0, bin 128..195 83h = TDC0, bin 196..255 84h = TDC1, bin 0…63 … 93h = TDC4, bin 196…255

8.9.17 TID Register (Address 0x1F)

Figure 45:
TID Register

Addr: 0x1F			TID	
Field	Name	Rst	Type	Description
7:0	tid	0	RO	Unique transaction ID, changes with every update of register map by TOF

8.9.18 Object Detection Results – If Register register_contents = 0x55 (commands 0x02, 0x03 or 0x04)

RESULT_NUMBER Register (Address 0x20)

Figure 46:
RESULT_NUMBER Register

Addr: 0x20			RESULT_NUMBER	
Field	Name	Rst	Type	Description
7:0	result_num	0	RO	Result number, incremented every time there is a unique answer

RESULT_INFO Register (Address 0x21)

Figure 47:
RESULT_INFO Register

Addr: 0x21		RESULT_INFO		
Field	**Name**	**Rst**	**Type**	**Description**
5:0	reliability	0	RO	Reliability of object - valid range 0..63 where 63 is best
7:6	measStatus	0	RO	When algImmediateInterrupt == 1 Will indicate the status of the measurement: Reading / Meaning 0 – Short distance capture interrupted, using previous short distance only result 1 – Short distance capture interrupted, using previous short and long distance result 2 – Long distance capture interrupted, result is from short distance algorithm only 3 – Complete result (short and long distance algorithm) When algImmediateInterrupt == 0 Will indicate the status of the measurement: Reading / Meaning 0 – Measurement was not interrupted 1 – Reserved 2 – Measurement was interrupted (delay) by GPIO interrupt 3 – Reserved

DISTANCE_PEAK_0 Register (Address 0x22)

Figure 48:
DISTANCE_PEAK_0 Register

Addr: 0x22		DISTANCE_PEAK_0		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	distance_peak[7:0]	0	RO	Distance to the peak in [mm] of the object, least significant byte

DISTANCE_PEAK_1 Register (Address 0x23)

Figure 49:
DISTANCE_PEAK_1

Addr: 0x23			DISTANCE_PEAK_1	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	distance_peak[15:8]	0	RO	Distance to the peak in [mm] of the object, most significant byte

The sys clock registers is a running timer information – this value is counting up (and wraps around to 0 again) as long as the internal clock is running. As it is derived from the internal RC oscillator and distance information is depending on its accuracy, it can be used to correct an algorithm result by comparing this clock with a more accurate clock inside the host. It is recommended to use several measurement cycles for this clock correction.

For correctly updating of these registers by TMF8801, an I²C blockread starting from address 0x1D until 0x27 shall be done.

SYS_CLOCK_0 Register (Address 0x24)

Figure 50:
SYS_CLOCK_0 Register

Addr: 0x24			SYS_CLOCK_0	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	sys_clock[7:0]	0	RO	System clock/time stamp in units of 0.2 µs

SYS_CLOCK_1 Register (Address 0x25)

Figure 51:
SYS_CLOCK_1 Register

Addr: 0x25			SYS_CLOCK_1	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	sys_clock[15:8]	0	RO	System clock/time stamp in units of 0.2 µs

SYS_CLOCK_2 Register (Address 0x26)

Figure 52:
SYS_CLOCK_2 Register

Addr: 0x26			SYS_CLOCK_2	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	sys_clock[23:16]	0	RO	System clock/time stamp in units of 0.2 µs

SYS_CLOCK_3 Register (Address 0x27)

Figure 53:
SYS_CLOCK_3 Register

Addr: 0x27			SYS_CLOCK_3	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	sys_clock[31:24]	0	RO	System clock/time stamp in units of 0.2 µs

Algorithm state information is captured in the next registers. To allow resume of operation after power-off, algorithm state can be stored temporarily inside the host and once after power-on of TMF8801 restored to resume operation.

STATE_DATA_0 Register (Address 0x28)

Figure 54:
STATE_DATA_0 Register

Addr: 0x28			STATE_DATA_0	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_0	0	RO	Algorithm state data

STATE_DATA_1 Register (Address 0x29)

Figure 55:
STATE_DATA_1 Register

Addr: 0x29			STATE_DATA_1	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_1	0	RO	Algorithm state data

STATE_DATA_2 Register (Address 0x2A)

Figure 56:
STATE_DATA_2 Register

Addr: 0x2A			STATE_DATA_2	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_2	0	RO	Algorithm state data

STATE_DATA_3 Register (Address 0x2B)

Figure 57:
STATE_DATA_3 Register

Addr: 0x2B			STATE_DATA_3	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_3	0	RO	Algorithm state data

STATE_DATA_4 Register (Address 0x2C)

Figure 58:
STATE_DATA_4 Register

Addr: 0x2C			STATE_DATA_4	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_4	0	RO	Algorithm state data

STATE_DATA_5 Register (Address 0x2D)

Figure 59:
STATE_DATA_5 Register

Addr: 0x2D			STATE_DATA_5	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_5	0	RO	Algorithm state data

STATE_DATA_6 Register (Address 0x2E)

Figure 60:
STATE_DATA_6 Register

Addr: 0x2E			STATE_DATA_6	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_6	0	RO	Algorithm state data

STATE_DATA_7 Register (Address 0x2F)

Figure 61:
STATE_DATA_7 Register

Addr: 0x2F			STATE_DATA_7	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_7	0	RO	Algorithm state data

STATE_DATA_8_XTALK_MSB Register (Address 0x30)

Figure 62:
STATE_DATA_8 Register

Addr: 0x30			STATE_DATA_8_XTALK_MSB	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	xtalk_msb	0	RO	Crosstalk peak value MSB byte; only valid with minimal ambient light and no target within 40 cm in field of view of the TMF8801

STATE_DATA_9_XTALK_LSB Register (Address 0x31)

Figure 63:
STATE_DATA_9 Register

Addr: 0x31			STATE_DATA_9_XTALK_LSB	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	xtalk_lsb	0	RO	Crosstalk peak value LSB byte; only valid with minimal ambient light and no target within 40 cm in field of view of the TMF8801

STATE_DATA_10_TJ Register (Address 0x32)

Figure 64:
STATE_DATA_10_TEMPERATURE Register

Addr: 0x32			STATE_DATA_10_TJ	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	temperature	0	RO	8 bit signed integer of the TMF8801 sensor DIE junction temperature in ºCelsius (e.g. “25” means 25ºC)

Reference hits and object hits are used for information purposes of the target object and are only reported if a target is detected with the distance algorithm.

REFERENCE_HITS_0 Register (Address 0x33)

Figure 65:
REFERENCE_HITS_0 Register

Addr: 0x33			REFERENCE_HITS_0	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	reference_hits[7:0]	0	RO	Sum of the reference SPADs hits during the distance measurement; zero if no object is detected or distance algorithm is not used

REFERENCE_HITS_1 Register (Address 0x34)

Figure 66:
REFERENCE_HITS_1 Register

Addr: 0x34			REFERENCE_HITS_1	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	reference_hits[15:8]	0	RO	Sum of the reference SPADs hits during the distance measurement; zero if no object is detected or distance algorithm is not used

REFERENCE_HITS_2 Register (Address 0x35)

Figure 67:
REFERENCE_HITS_2 Register

Addr: 0x35			REFERENCE_HITS_2	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	reference_hits[23:16]	0	RO	Sum of the reference SPADs hits during the distance measurement; zero if no object is detected or distance algorithm is not used

REFERENCE_HITS_3 Register (Address 0x36)

Figure 68:
REFERENCE_HITS_3 Register

Addr: 0x36		REFERENCE_HITS_3		
Field	Name	Rst	Type	Description
7:0	reference_hits[31:24]	0	RO	Sum of the reference SPADs hits during the distance measurement; zero if no object is detected or distance algorithm is not used

OBJECT_HITS_0 Register (Address 0x37)

Figure 69:
OBJECT_HITS_0 Register

Addr: 0x37		OBJECT_HITS_0		
Field	Name	Rst	Type	Description
7:0	object_hits[7:0]	0	RO	Sum of the object SPADs hits during the distance measurement; zero if no object is detected or distance algorithm is no used

OBJECT_HITS_1 Register (Address 0x38)

Figure 70:
OBJECT_HITS_1 Register

Addr: 0x38		OBJECT_HITS_1		
Field	Name	Rst	Type	Description
7:0	object_hits[15:8]	0	RO	Sum of the object SPADs hits during the distance measurement; zero if no object is detected or distance algorithm is no used

OBJECT_HITS_2 Register (Address 0x39)

Figure 71:
OBJECT_HITS_2 Register

Addr: 0x39		OBJECT_HITS_2		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	object_hits[23:16]	0	RO	Sum of the object SPADs hits during the distance measurement; zero if no object is detected or distance algorithm is no used

OBJECT_HITS_3 Register (Address 0x3A)

Figure 72:
OBJECT_HITS_3 Register

Addr: 0x3A		OBJECT_HITS_3		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	object_hits[31:24]	0	RO	Sum of the object SPADs hits during the distance measurement; zero if no object is detected or distance algorithm is no used

8.9.19 Calibration and Algorithm State Data Exchange

These registers shall be pre-loaded by the host before command=0x02 or 0x0B is executed

FACTORY_CALIB_0 Register (Address 0x20)

Figure 73:
FACTORY_CALIB_0 Register

Addr: 0x20		FACTORY_CALIB_0		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_0	0	RW	Factory calibration data Bits [3:0] are format revision Bits [7:4] are bits [3:0] of crosstalk measurement

FACTORY_CALIB_1 Register (Address 0x21)

Figure 74:
FACTORY_CALIB_1 Register

Addr: 0x21			FACTORY_CALIB_1	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_1	0	RW	Factory calibration data Bits [11:4] of crosstalk measurement

FACTORY_CALIB_2 Register (Address 0x22)

Figure 75:
FACTORY_CALIB_2 Register

Addr: 0x22			FACTORY_CALIB_2	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_2	0	RW	Factory calibration data Bits [19:12] of crosstalk measurement

FACTORY_CALIB_3 Register (Address 0x23)

Figure 76:
FACTORY_CALIB_3 Register

Addr: 0x23			FACTORY_CALIB_3	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_3	0	RW	Factory calibration data

FACTORY_CALIB_4 Register (Address 0x24)

Figure 77:
FACTORY_CALIB_4 Register

Addr: 0x24			FACTORY_CALIB_4	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_4	0	RW	Factory calibration data

FACTORY_CALIB_5 Register (Address 0x25)

Figure 78:
FACTORY_CALIB_5 Register

Addr: 0x25			FACTORY_CALIB_5	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_5	0	RW	Factory calibration data

FACTORY_CALIB_6 Register (Address 0x26)

Figure 79:
FACTORY_CALIB_6 Register

Addr: 0x26			FACTORY_CALIB_6	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_6	0	RW	Factory calibration data

FACTORY_CALIB_7 Register (Address 0x27)

Figure 80:
FACTORY_CALIB_7 Register

Addr: 0x27			FACTORY_CALIB_7	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_7	0	RW	Factory calibration data

FACTORY_CALIB_8 Register (Address 0x28)

Figure 81:
FACTORY_CALIB_8 Register

Addr: 0x28			FACTORY_CALIB_8	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_8	0	RW	Factory calibration data

FACTORY_CALIB_9 Register (Address 0x29)

Figure 82:
FACTORY_CALIB_9 Register

Addr: 0x29			FACTORY_CALIB_9	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_9	0	RW	Factory calibration data

FACTORY_CALIB_10 Register (Address 0x2A)

Figure 83:
FACTORY_CALIB_10 Register

Addr: 0x2A			FACTORY_CALIB_10	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_10	0	RW	Factory calibration data

FACTORY_CALIB_11 Register (Address 0x2B)

Figure 84:
FACTORY_CALIB_11 Register

Addr: 0x2B			FACTORY_CALIB_11	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_11	0	RW	Factory calibration data

FACTORY_CALIB_12 Register (Address 0x2C)

Figure 85:
FACTORY_CALIB_12 Register

Addr: 0x2C			FACTORY_CALIB_12	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_12	0	RW	Factory calibration data

FACTORY_CALIB_13 Register (Address 0x2D)

Figure 86:
FACTORY_CALIB_13 Register

Addr: 0x2D			FACTORY_CALIB_13	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	factory_calib_13	0	RW	Factory calibration data

If algorithm state data is sent to TMF8801 following registers shall be pre-loaded by the host before command=0x02 or 0x0B is executed.

Information

If only algorithm state data and no calibration data is sent to TMF8801, pre-load algorithm state data starting from address 0x20 instead of 0x2E.

STATE_DATA_WR_0 Register (Address 0x2E)

Figure 87:
STATE_DATA_WR_0 Register

Addr: 0x2E			STATE_DATA_WR_0	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_0	0	RW	Algorithm state data

STATE_DATA_WR_1 Register (Address 0x2F)

Figure 88:
STATE_DATA_WR_1 Register

Addr: 0x2F			STATE_DATA_WR_1	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_1	0	RW	Algorithm state data

STATE_DATA_WR_2 Register (Address 0x30)

Figure 89:
STATE_DATA_WR_2 Register

Addr: 0x30			STATE_DATA_WR_2	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_2	0	RW	Algorithm state data

STATE_DATA_WR_3 Register (Address 0x31)

Figure 90:
STATE_DATA_WR_3 Register

Addr: 0x31			STATE_DATA_WR_3	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_3	0	RW	Algorithm state data

STATE_DATA_WR_4 Register (Address 0x32)

Figure 91:
STATE_DATA_WR_4 Register

Addr: 0x32			STATE_DATA_WR_4	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_4	0	RW	Algorithm state data

STATE_DATA_WR_5 Register (Address 0x33)

Figure 92:
STATE_DATA_WR_5 Register

Addr: 0x33			STATE_DATA_WR_5	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_5	0	RW	Algorithm state data

STATE_DATA_WR_6 Register (Address 0x34)

Figure 93:
STATE_DATA_WR_6 Register

Addr: 0x34			STATE_DATA_WR_6	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_6	0	RW	Algorithm state data

STATE_DATA_WR_7 Register (Address 0x35)

Figure 94:
STATE_DATA_WR_7 Register

Addr: 0x35			STATE_DATA_WR_7	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_7	0	RW	Algorithm state data

STATE_DATA_WR_8 Register (Address 0x36)

Figure 95:
STATE_DATA_WR_8 Register

Addr: 0x36			STATE_DATA_WR_8	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_8	0	RW	Algorithm state data

STATE_DATA_WR_9 Register (Address 0x37)

Figure 96:
STATE_DATA_WR_9 Register

Addr: 0x37			STATE_DATA_9	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_9	0	RW	Algorithm state data

STATE_DATA_WR_10 Register (Address 0x38)

Figure 97:
STATE_DATA_WR_10 Register

Addr: 0x38			STATE_DATA_WR_10	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	state_data_wr_10	0	RW	Algorithm state data

8.9.20 Raw Histogram Output – If Register register_contents=0x80…0x93

HISTOGRAM_START Register (Address 0x20)

Figure 98:
HISTOGRAM_START Register

Addr: 0x20			HISTOGRAM_START	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	hist_start	0	RW	Quarter of histogram first byte

…all bytes until…

HISTOGRAM_END Register (Address 0x9F)

Figure 99:
HISTOGRAM_END Register

Addr: 0x9F			HISTOGRAM_END	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	hist_end	0	RW	Quarter of histogram last byte

8.9.21 Serial Number Readout – If Register register_contents=0x47

SERIAL_NUMBER_0 Register (Address 0x28)

Figure 100:
SERIAL_NUMBER_0 Register

Addr: 0x28			SERIAL_NUMBER_0	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	serial_number_0	0	RW	Serial number byte 0

SERIAL_NUMBER_1 Register (Address 0x29)

Figure 101:
SERIAL_NUMBER_1 Register

Addr: 0x29			SERIAL_NUMBER_1	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	serial_number_1	0	RW	Serial number byte 1

IDENTIFICATION_NUMBER_0 (Address 0x2A)

Figure 102:
IDENTIFICATION_NUMBER_0 Register

Addr: 0x2A			IDENTIFICATION_NUMBER_0	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	identification_number_0	0	RW	Identification number byte 0

IDENTIFICATION_NUMBER_1 (Address 0x2B)

Figure 103:
IDENTIFICATION_NUMBER_1 Register

Addr: 0x2B			IDENTIFICATION_NUMBER_1	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	identification_number_1	0	RW	Identification number byte 1

The binary concatenated number of serial_number_0: serial_number_1: identification_number_0: identification_number_1 registers result in a unique number.

8.10 Bootloader Registers – appid=0x80

Following registers are only available if appid=0x80 (Bootloader):

8.10.1 BL_CMD_STAT (Address 0x08)

Figure 104:
BL_CMD_STAT Register

Addr: 0x08			BL_CMD_STAT	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	bl_cmd_stat	0	RW	Write: Bootloader Command – see section Bootloader Commands Read: Bootloader Status – anything else than 0x00 means an error

8.10.2 BL_SIZE (Address 0x09)

Figure 105:
BL_SIZE Register

Addr: 0x09			BL_SIZE	
Field	**Name**	**Rst**	**Type**	**Description**
6:0	bl_size	0	RW	Data size in bytes

8.10.3 BL_DATA (Address 0x0A-0x8A)

Figure 106:
BL_DATA Register

Addr: 0x0A-0x8A			BL_DATA	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	bl_data0 … bl_data127	0	RW	Up to 128 data bytes for bootloader commands

8.10.4 BL_CSUM (Address 0x8B)

Figure 107:
BL_CSUM Register

Addr: 0x8B			BL_CSUM	
Field	**Name**	**Rst**	**Type**	**Description**
7:0	bl_csum	0	RW	Checksum for Sum(Command + Data Size + Data itself) XOR 0xFF

8.10.5 Bootloader Commands

The following commands (bl_cmd_stat) are supported by the bootloader:

Command	Value	Meaning
RAMREMAP_RESET	0x11	Remap RAM to Address 0 and Reset
DOWNLOAD_INIT	0x14	Initialize for RAM download from host to TMF8801

Command	Value	Meaning
W_RAM	0x41	Write RAM Region (Plain = not encoded into e.g. Intel Hex Records)
ADDR_RAM	0x43	Set the read/write RAM pointer to a given address

RAMREMAP_RESET = Execute Program Downloaded to RAM

This command remaps the RAM to address 0 and performs a System reset (see also command RESET).

Command is performed immediately without any delay.

After this the application that is located in RAM will be running. If there is no valid application you will need to do a HW reset (toggle enable pin or power cycle).

Figure 108:
RAMREMAP_RESET

Address	Value	Meaning
BL_CMD_STAT	0x11	REMAP RAM to 0 and RESET
BL_SIZE	0	No parameters
BL_CSUM	0xEE	

DOWNLOAD_INIT

This command is used to initialize the download HW for secure devices.

Figure 109:
DOWNLOAD_INIT

Address	Value	Meaning
BL_CMD_STAT	0x14	Initialize the HW for download from host to TMF8801 RAM
BL_SIZE	1	
BL_DATA0	0..0xFF	Seed
BL_CSUM	0..0xFF	

W_RAM

This command writes the given data to a defined RAM region. Note that the RAM pointer has first to be set by the command ADDR_RAM. After the command is successfully executed the RAM pointer will point to the first byte after the written region.

Figure 110:
W_RAM

Address	Value	Meaning
BL_CMD_STAT	0x41	Write to main RAM
BL_SIZE	0..0x80	Number of bytes to be written
BL_DATA0	0..0xFF	1^{st} byte to be written
BL_DATA1	0..0xFF	2^{nd} byte to be written
…		
BL_DATA127	0..0xFF	128^{th} byte to be written (only if size was 0x80)
BL_CSUM	0..0xFF	The CSUM comes immediately after the data.

ADDR_RAM

This command is to specify the RAM pointer location for the next R_RAM or W_RAM command.

Figure 111:
ADDR_RAM

Address	Value	Meaning
BL_CMD_STAT	0x43	Specify the address of the next RAM read or write.
BL_SIZE	2	
BL_DATA0	0..0xFF	LSB of address in RAM
BL_DATA1	0..0xFF	MSB of address in RAM
BL_CSUM	0..0xFF	

9 Application Information

9.1 SPAD Options

9.1.1 Signal SPADs

Firmware can enable/disable SPADs in the array as needed.

Figure 112:
Signal SPADs

	Min	Nom	Max	Comment
1x SPADS			72	
10x Attenuated SPADs			16	
100x Attenuated SPADs			16	

Physically there are 4x32=128 signal SPADs, but SPADs with too high dark count rate are disabled during production test. There are four TDCs (TDC1…TDC4) connected to the output of the SPADs. Each of the TDCs is connected to an array of 32 SPADs (SPADs with too high dark count rate are disabled). In distance mode the number of SPADs are reduced to typ. 40 SPADs to limit the FOV of the TMF8801.

9.1.2 Reference SPADs

Figure 113:
Reference SPADs

	Min	Nom	Max	Comment
100x Attenuated SPADs			9	

Due to the high light intensity form the VCSEL which is located very close to the reference SPADs and has no optical barrier like the signal SPADs only highly attenuated SPADs are used. Physically there are 12 reference SPADs, but SPADs with too high dark count rate are disabled during production test. There is one TDC (TDC0) connected to the output of the SPADs.

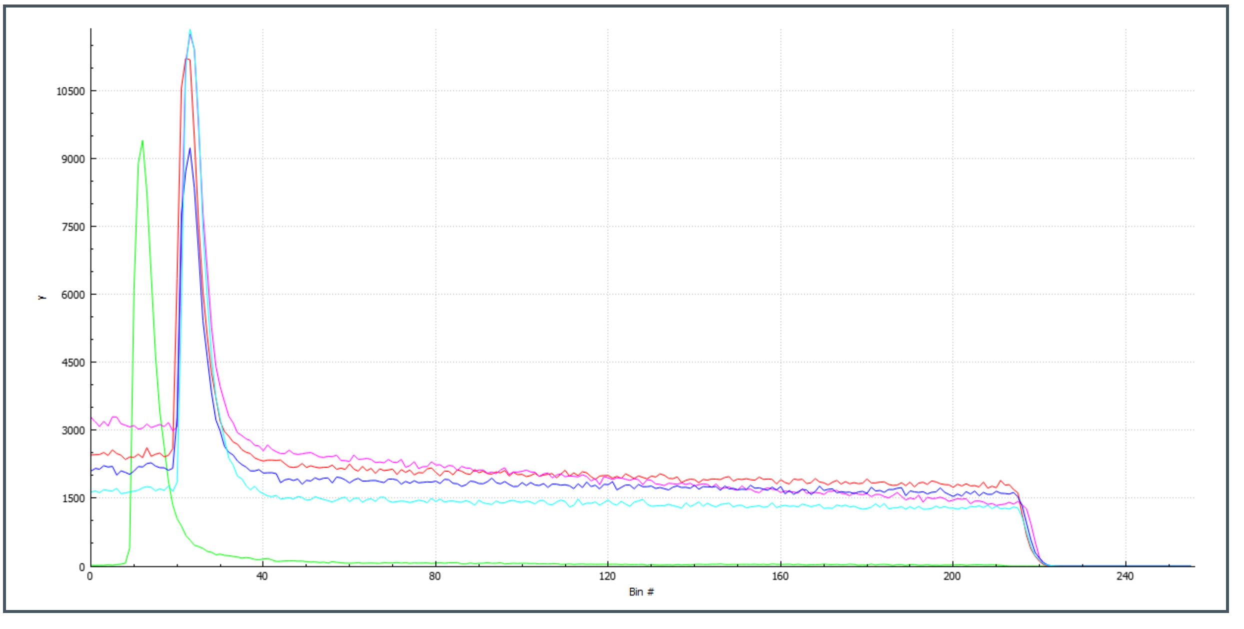
9.2 Reference SPAD, TDC and Histogram

There is an internal reference SPAD with associated TDC and histogram. This is used to determine the start time of each pulse. The reference SPAD is processed during calibration. The reference channel processing occurs internal to the device with no user interaction required.

All histograms can be processed inside the TMF8801 and/or readout through the I²C interface. As the readout is constrained by the I²C speed and the I²C bus utilization (TMF8801 can support I²C speed up to 1 MHz), it is recommended to readout the histograms only for debugging purposes.

Figure 114 shows a histogram obtained from TMF8801. The x-axis is scaled in bins, where the nominal bin size is 100 ps per bin and each TDC has 256 bins. The y-axis is scaled in counts represented by 16-bit values. The green line shows the reference histogram from TDC0 and its peak marks the reference or zero distance. The other four lines (blue, cyan, red and violet) are the histograms obtained from TDC1 to TDC4. A target at 20 cm is used to generate the peak around bin 25.

Figure 114:
Histogram

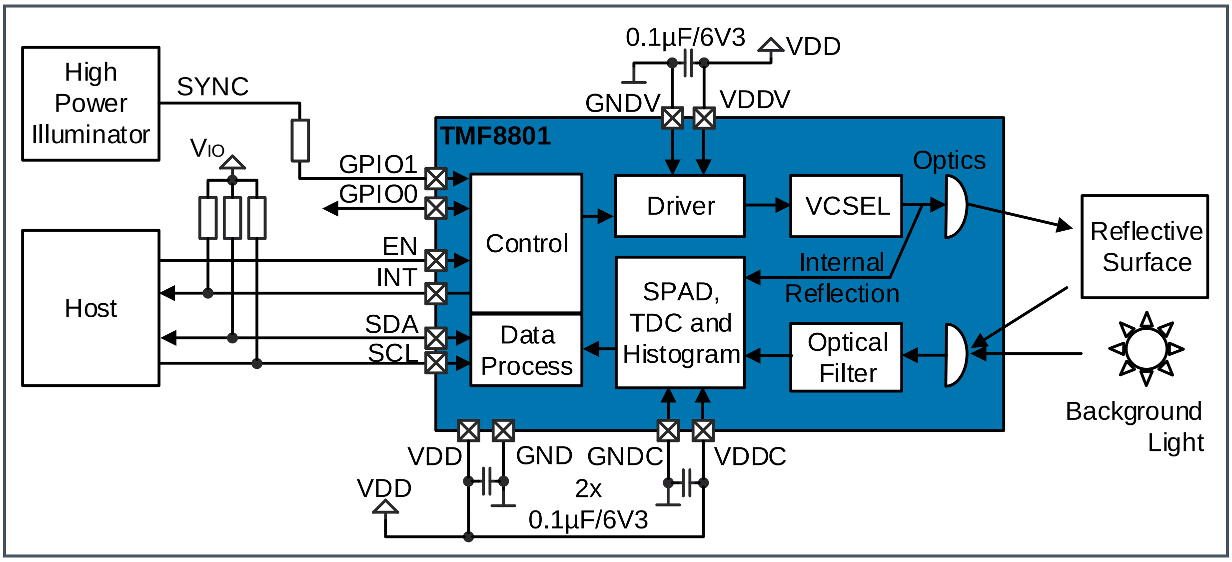


(1) The above histogram is used for general device information only. The actual histogram differ due to different bin size and modes used.

9.3 Schematic

The TMF8801 needs only 3 small 0402 external capacitors for operation:

Figure 115:
TMF8801 Application Schematic



The SYNC signal connected to GPIO1 can be used to immediately interrupt the TMF8801 VCSEL operation if the high power illuminator is operating. It needs to be ensured that SYNC does not exceed the VDD supply of TMF8801 as otherwise an internal protection diode will start conducting. The VCSEL operation is controlled by setting cmd_data5 of command=0x02 or 0x03 according (see App0 registers). On SYNC assertion, the VCSEL is immediately switched off (typically after 10 µs), on SYNC de-assertion the VCSEL operation is resumed within >100 µs.

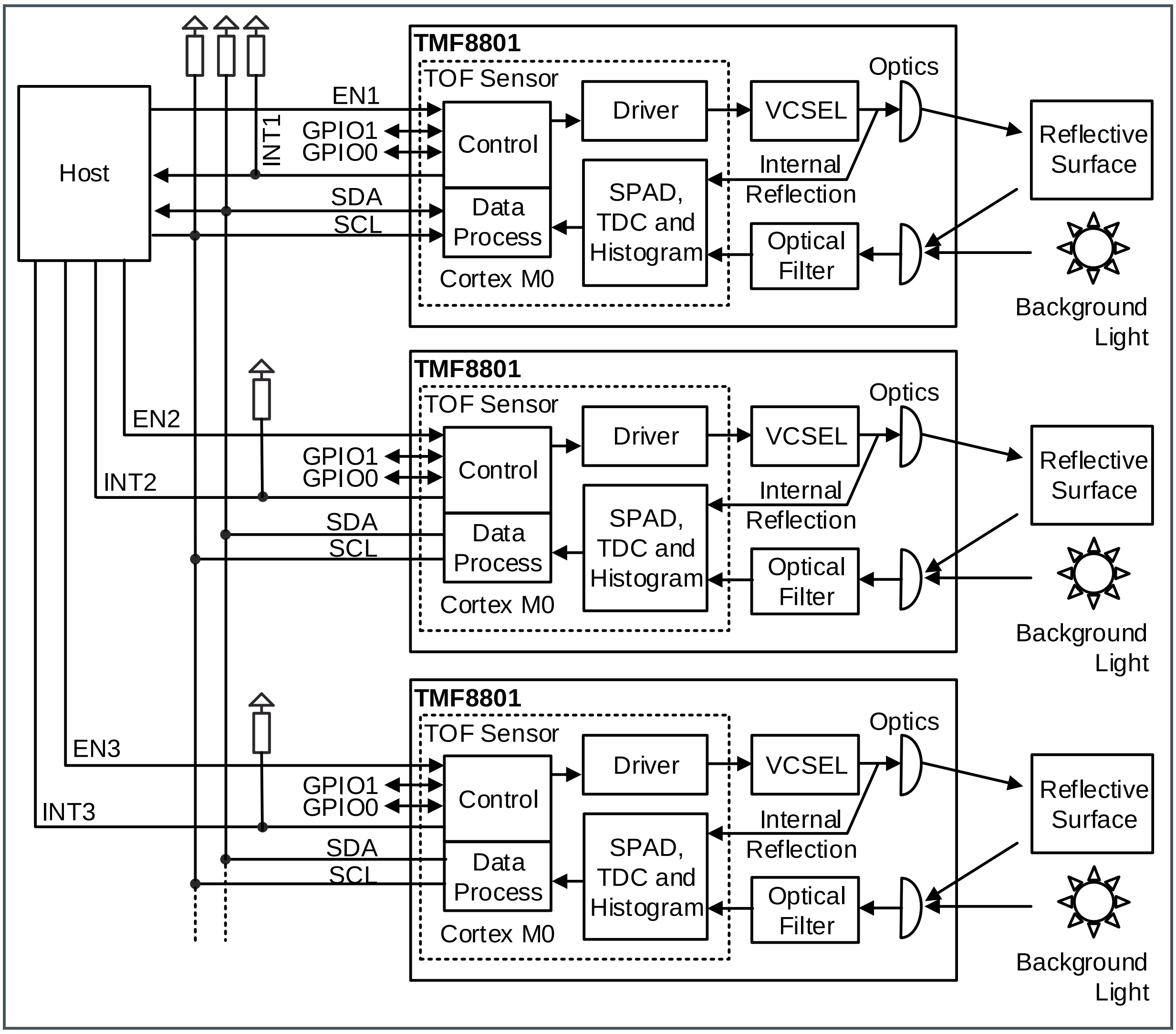
GPIO0 can be used as a general GPIO output signal.

The signals INT/SDA/SCL need an external pullup resistor to the VIO supply (typically 1.8 V).

9.3.1 Operating Several TMF8801 on a Single I²C Bus

Several TMF8801 devices can share a single I²C bus if there are dedicated enable (EN) connections to each of these devices.

Figure 116:
Sharing a Single I²C Bus for Operating Several TMF8801s



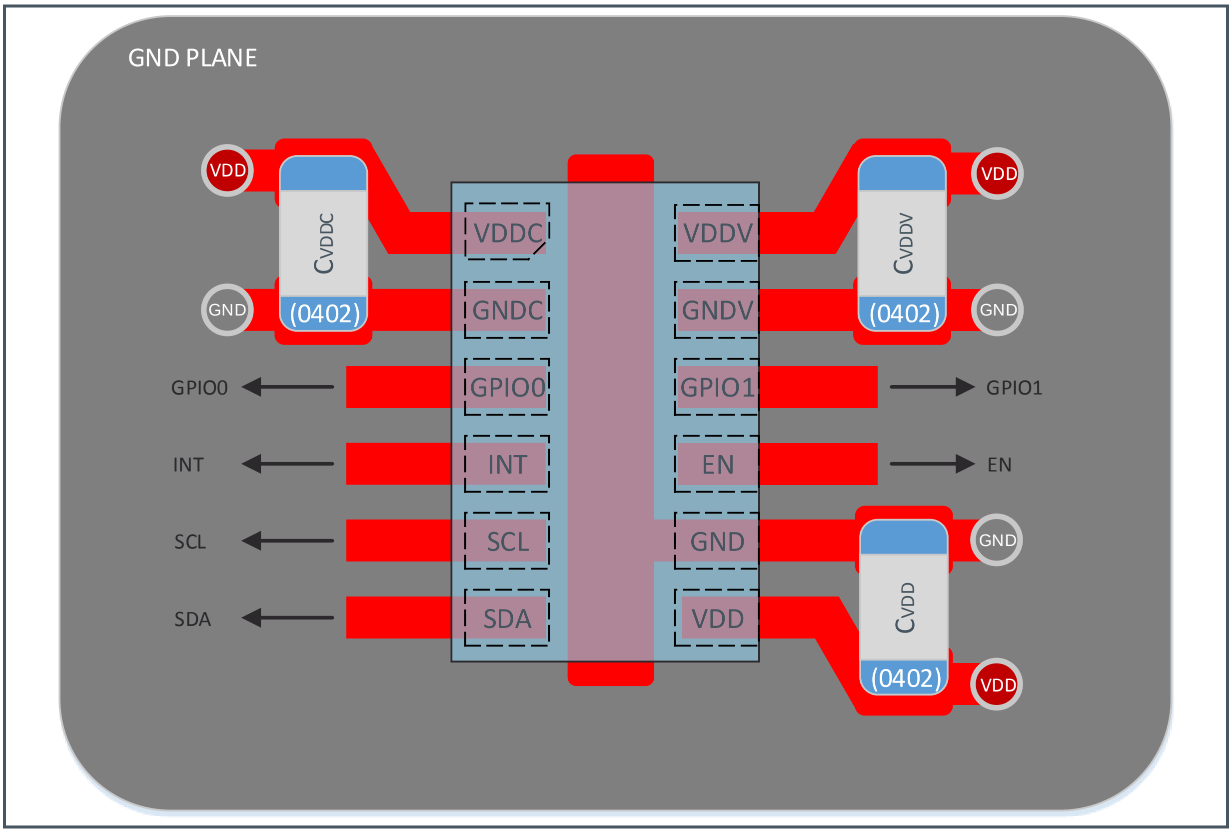
The procedure to initialize the devices to different I²C addresses is as follows:

1. Set EN1=0, EN2=0, EN3=0 (reset all devices)
2. Set EN1=1
3. Upload firmware patch to first TMF8801
4. Reprogram I²C address for first TMF8801 using command=0x49 where cmd_data0=0 and cmd_data1=I²C address for first TMF8801

5. Set EN2=1
6. Upload firmware patch to second TMF8801
7. Reprogram I²C address for second TMF8801 using command=0x49 where cmd_data0=0 and cmd_data1=I²C address for second TMF8801
8. Set EN3=1
9. Upload firmware patch to third TMF8801
10. Reprogram I²C address for third TMF8801 using command=0x49 where cmd_data0=0 and cmd_data1=I²C address for third TMF8801
11. If there are further devices, repeat last three steps accordingly.

9.4 PCB Layout

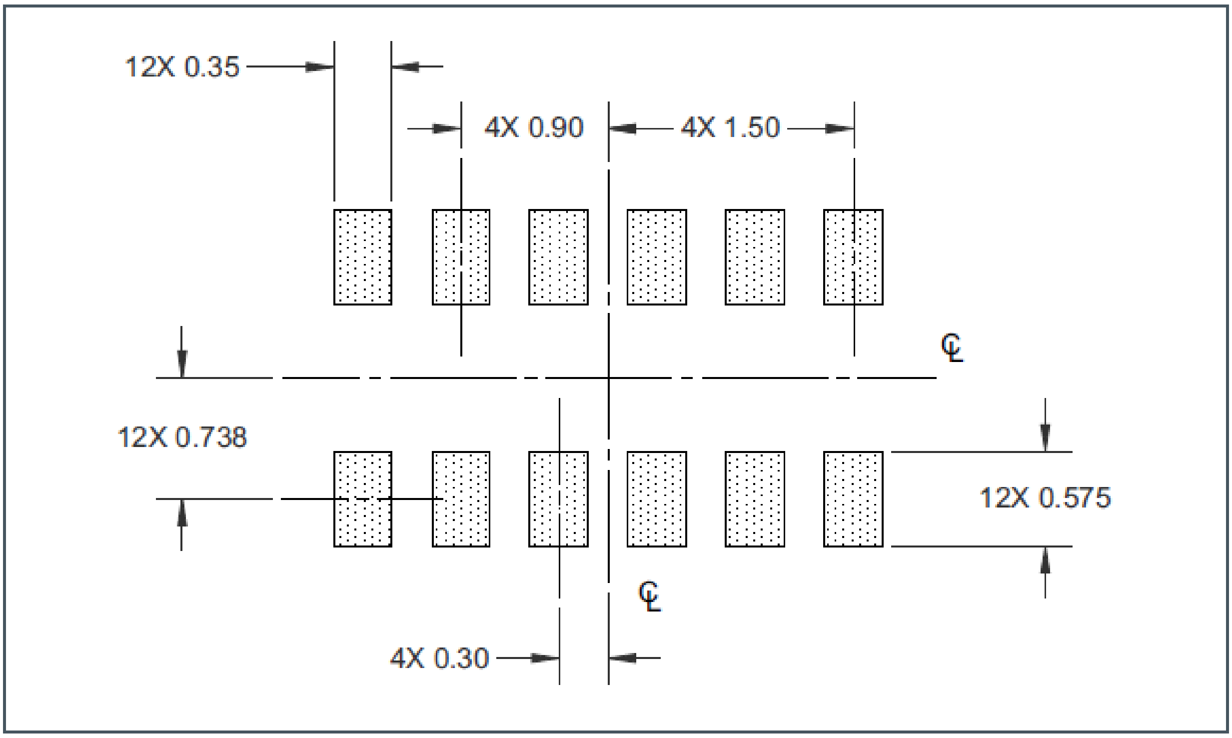
Figure 117:
PCB Layout Recommendation



Use GRM155R70J104KA01 (0402 X7R 0.1 µF 6.3 V) or capacitors with same or better performance for CVDDC, CVDD and CVDDV.

9.5 PCB Pad Layout

Figure 118:
PCB Pad Layout

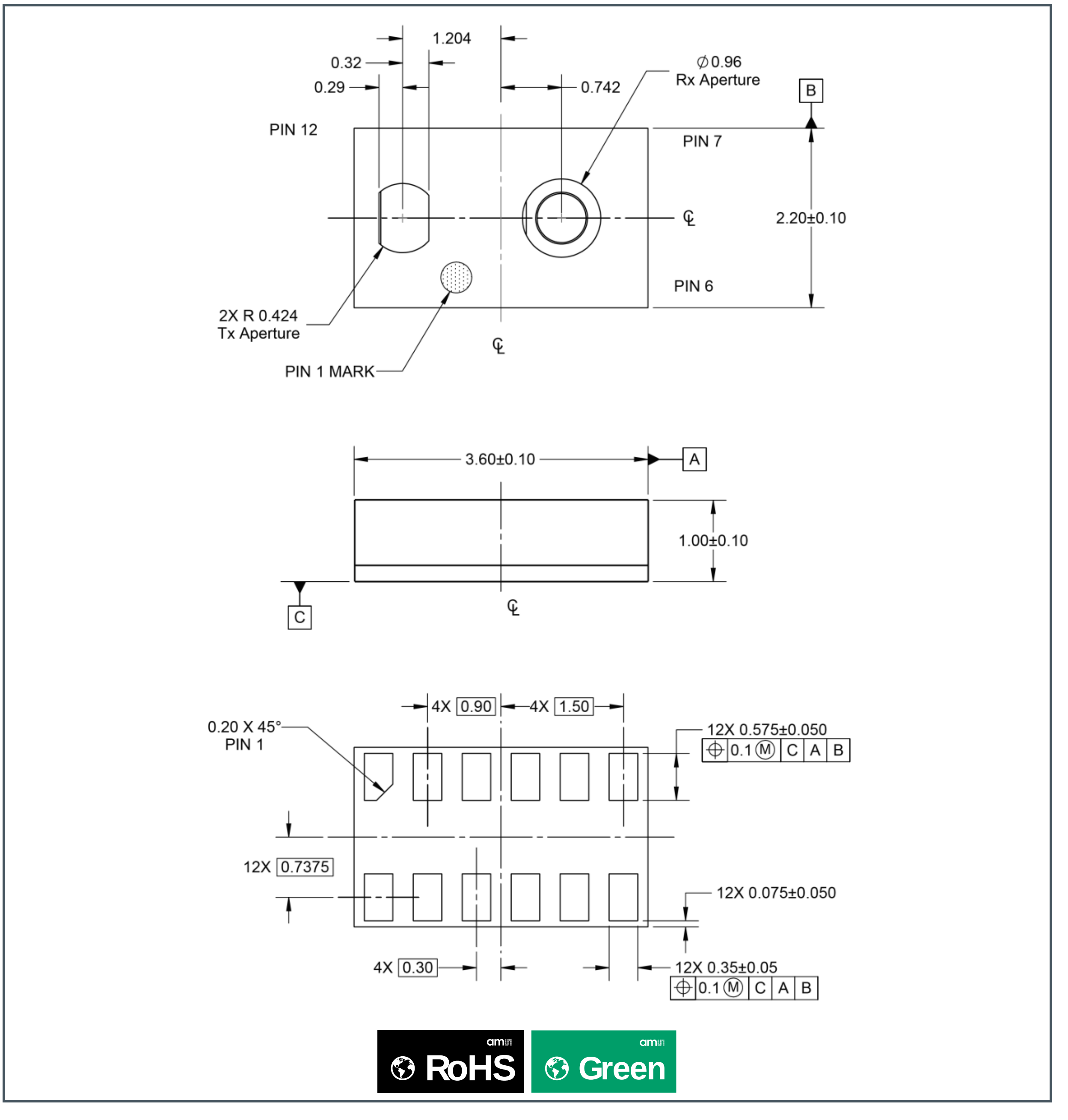


(1) All linear dimensions are in millimeters.
(2) Dimension tolerances are 0.05 mm unless otherwise noted.
(3) This drawing is subject to change without notice.

Use the PCB pad layout as a recommendation only. The actual pad layout shall be optimized for the customer production line.

10 Package Drawings & Markings

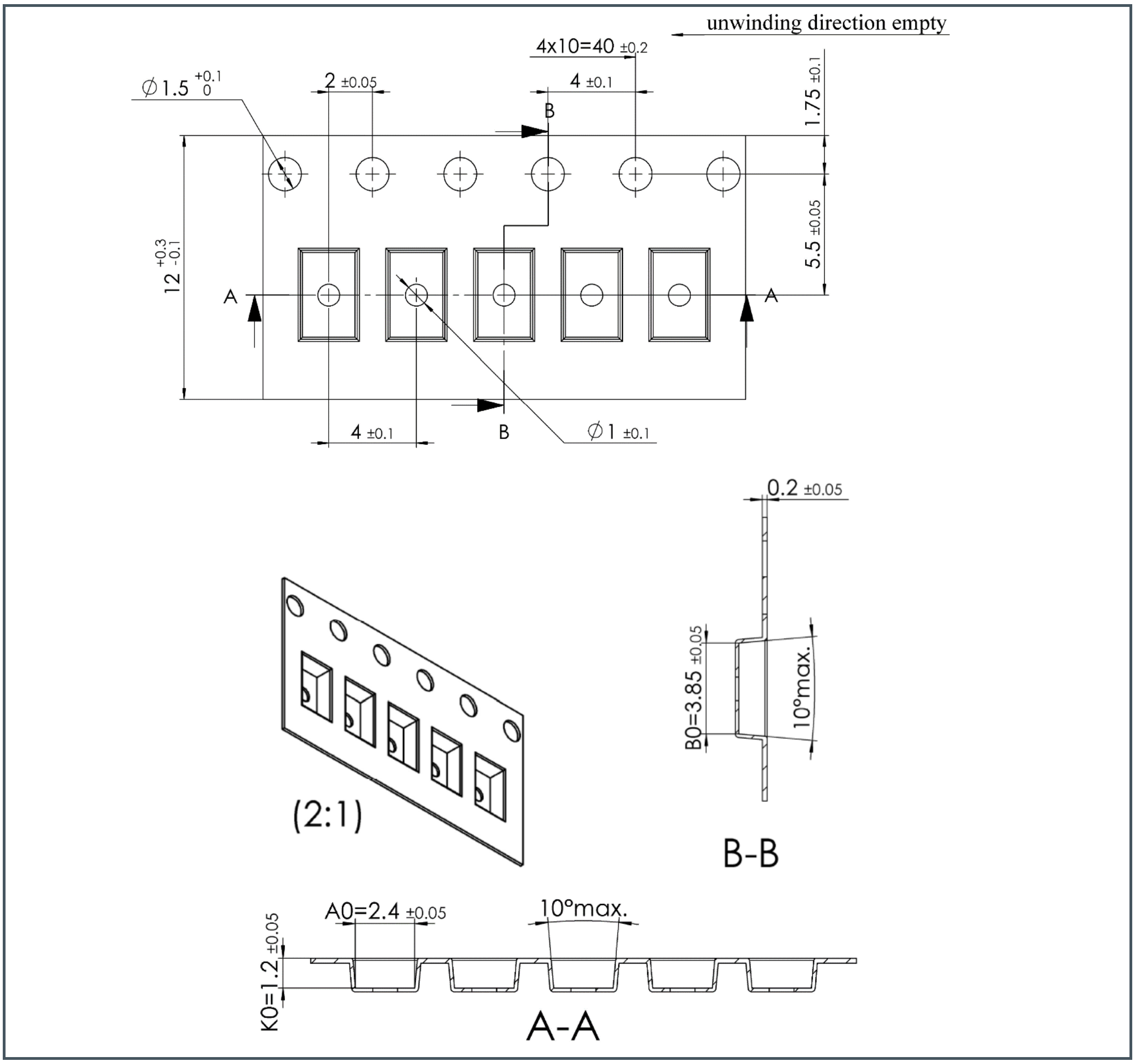
Figure 119:
Package Drawing



(1) All linear dimensions are in millimeters.
(2) Contact finish is Au/Ni.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.
(5) 5-digit tracecode is only on bottom side of the package.

11 Tape & Reel Information

Figure 120:
Tape and Reel Drawing



(1) All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
(2) The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
(3) Symbols on drawing A0, B0, and K0 are defined in ANSI EIA Standard 481-B 2001.
(4) There are two reel sizes available (see section Ordering Information)
 i) 7'' reels: Each reel is 7 inch in diameter and contains 500 parts.
 ii) 13'' reels: Each reel is 13 inch in diameter and contains 5000 parts.
(5) **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
(6) In accordance with EIA standard, device pin 1 is located next to sprocket holes in the tape.
(7) This drawing is subject to change without notice.

12 Soldering & Storage Information

12.1 Soldering Information

The package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 121:
Solder Reflow Profile Graph

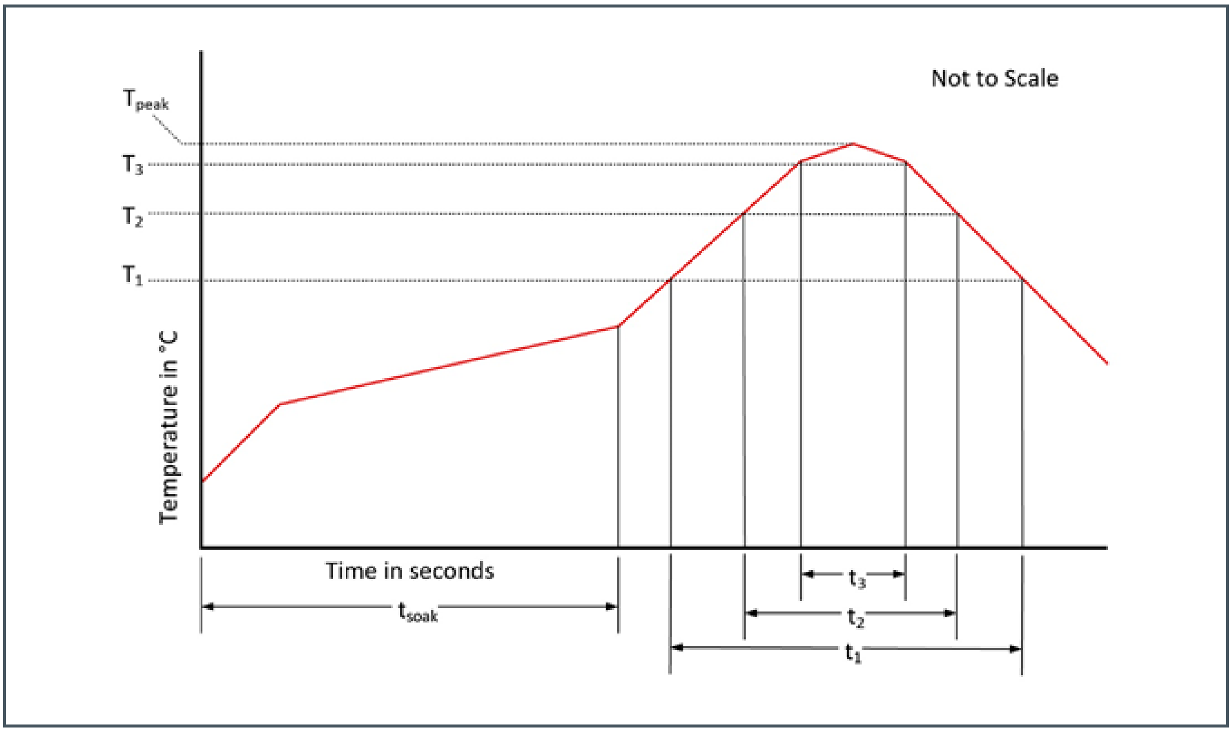


Figure 122:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s

Parameter	Reference	Device
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max −5 °C/s

12.2 Storage Information

12.2.1 Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40 °C
- Relative Humidity: <90 %

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30 °C
- Relative Humidity: <60 %

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50 °C for 12 hours.

13 Laser Eye Safety

The TMF8801 is designed to meet the Class 1 laser safety limits including single faults in compliance with IEC / EN 60825-1:2014. This applies to the stand-alone device and the included software supplied by **ams**. In an end application system environment, the system may need to be tested to ensure it remains compliant. The system must not include any additional lens to concentrate the laser light or parameters set outside of the recommended operating conditions. Use outside of the recommended condition or any physical modification to the module during development could result in hazardous levels of radiation exposure.

14 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v5-01	Page
Added detailed explanation for soldering profile.	64

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

15 Legal Information

RoHS Compliant & ams Green Statement

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ams Green (RoHS compliant and no Sb/Br/Cl): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material) and do not contain Chlorine (Cl not exceed 0.1% by weight in homogeneous material).

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