

# TSL2540

## ALS, Light-to-Digital Sensor

### General Description

The TSL2540 is a very-high sensitivity light-to-digital converter that transforms light intensity into a digital signal output capable of direct I<sup>2</sup>C interface. The ALS sensor features 2 output channels, a visible channel and an IR channel. The visible channel has a photodiode with a UV and IR blocking filter whereas the IR channel has a photodiode with an IR pass filter. Each channel has a dedicated data converter producing a 16-bit output. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance to control a display backlight.

*Ordering Information and Content Guide appear at end of datasheet.*

### Key Benefits & Features

The benefits and features of TSL2540, ALS, Light-to-Digital Sensor are listed below:

**Figure 1:**  
Added Value of Using TSL2540

Benefits	Features
<ul style="list-style-type: none"> <li>• Single device integrated optical solution</li> </ul>	<ul style="list-style-type: none"> <li>• 2.0mm x 2.0mm x 0.5mm</li> <li>• Power management features</li> <li>• I<sup>2</sup>C fast mode interface compatible</li> </ul>
<ul style="list-style-type: none"> <li>• Accurate ambient light sensing</li> </ul>	<ul style="list-style-type: none"> <li>• Photopic ambient light sense (ALS)</li> <li>• UV / IR blocking filter</li> <li>• Programmable gain and integration time</li> </ul>
<ul style="list-style-type: none"> <li>• Reduced power consumption</li> </ul>	<ul style="list-style-type: none"> <li>• 1.8V power supply with 1.8V I<sup>2</sup>C bus</li> </ul>

### Applications

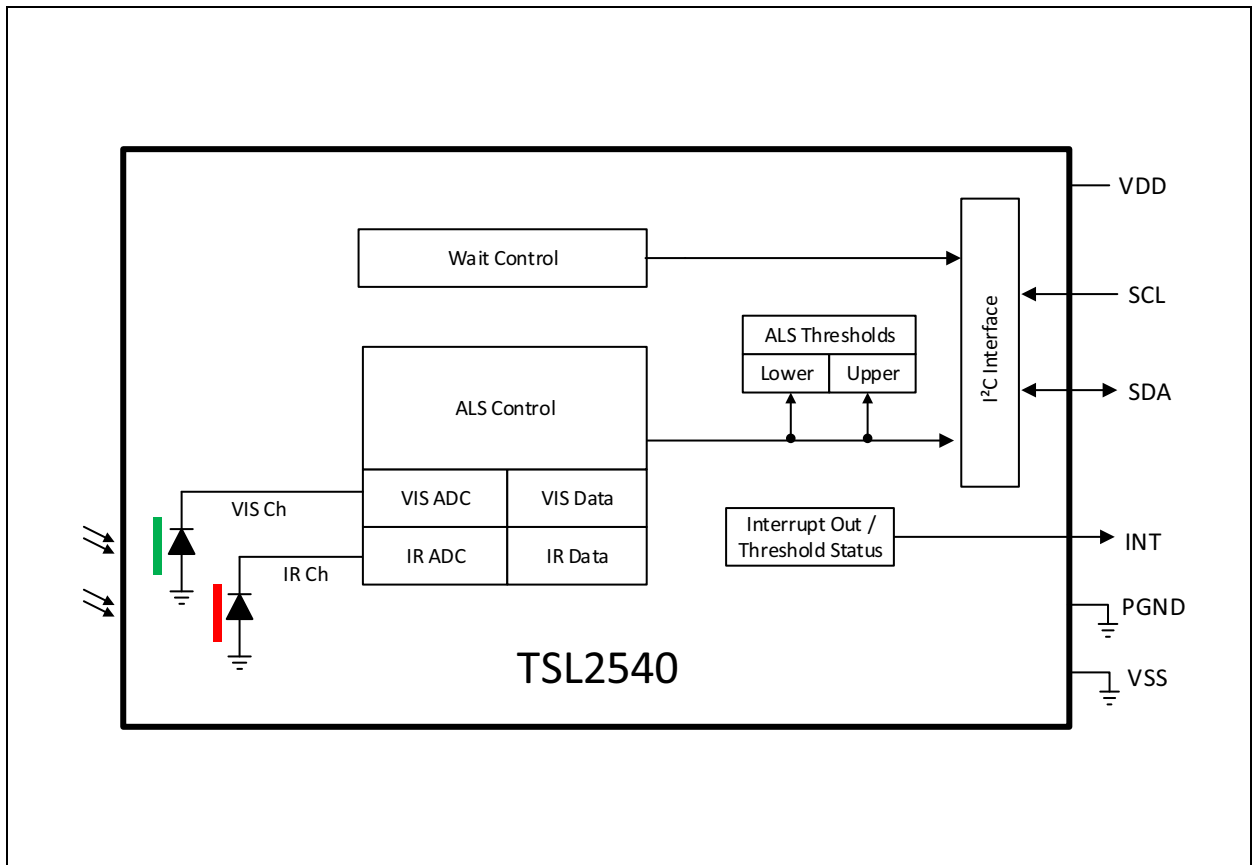
The TSL2540 applications include:

- Ambient light sensing
- Display backlight control

### Block Diagram

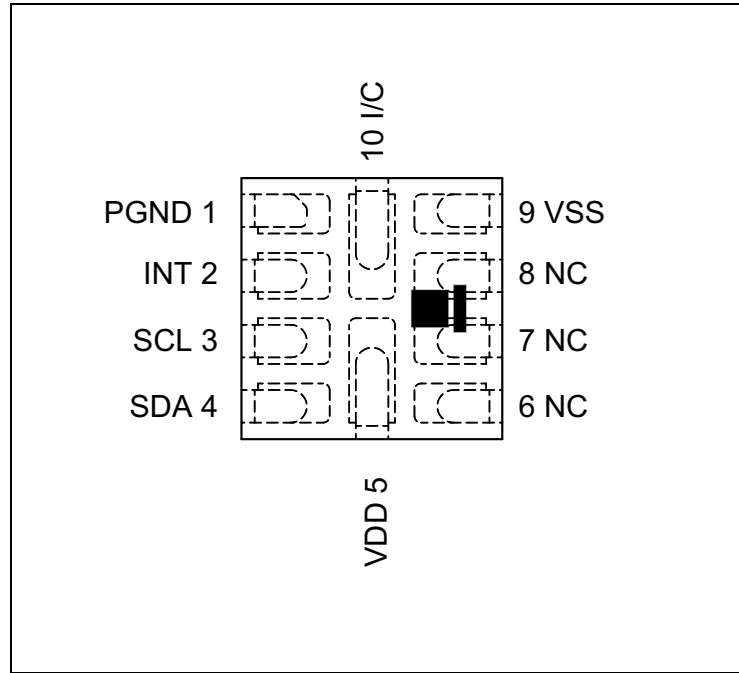
The functional blocks of this device are shown below:

**Figure 2:**  
Functional Blocks of TSL2540



## Pin Assignment

**Figure 3:**  
Pin Diagram of TSL2540



**Figure 4:**  
Pin Description of TSL2540 (10-Pin QFN)

Pin Number	Pin Name	Description
1	PGND	Power ground
2	INT	Interrupt. Open drain output (active low)
3	SCL	I <sup>2</sup> C serial clock input terminal
4	SDA	I <sup>2</sup> C serial data I/O terminal
5	VDD	Supply voltage
6	NC	No connection
7	NC	No connection
8	NC	No connection
9	VSS	Ground. All voltages are referenced to VSS
10	I/C	Internal connection. Connect to ground or leave floating

## Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**  
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
$V_{DD}$	Supply voltage	-0.3	2.2	V	All voltages are with respect to GND
$V_{IO}$	Digital I/O terminal voltage	-0.3	3.6	V	INT, SCL and SDA
$I_{out}$	Output terminal current	-1	20	mA	INT and SDA
$T_{strg}$	Storage temperature range	-40	85	°C	
$I_{SCR}$	Input current (latch up immunity) JEDEC JESD78D	± 100		mA	Class II
$ESD_{HBM}$	Electrostatic discharge HBM JS-001-2014	± 2000		V	
$ESD_{CDM}$	Electrostatic discharge CDM JEDEC JESD22-C101F	± 500		V	

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 6:**  
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD}$	Supply voltage	1.7	1.8	2.0	V
	Supply voltage accuracy, $V_{DD}$ total error including transients	-3		3	%
$T_A$	Operating free-air temperature <sup>(1)</sup>	-30		85	°C

**Note(s):**

1. While the device is operational across the temperature range, performance will vary with temperature. Specifications are stated at 25°C unless otherwise noted.

**Figure 7:**  
Operating Characteristics,  $V_{DD} = 1.8V$ ,  $T_A = 25^\circ C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$f_{OSC}$	Oscillator frequency			8.107		MHz
$I_{DD}$	Supply current	Active ALS State (PON=AEN=1) <sup>(1)</sup>	50	90	150	$\mu A$
		Idle State (PON=1,AEN=0) <sup>(2)</sup>		30	60	
		Sleep State <sup>(3)</sup>		0.7	5	
$V_{OL}$	INT, SDA output low voltage	6mA sink current			0.6	V
$I_{LEAK}$	Leakage current, INT, SCL and SDA		-5		5	$\mu A$
$V_{IH}$	SCL, SDA input high voltage <sup>(4)</sup>		1.26			V
$V_{IL}$	SCL, SDA input low voltage				0.54	V
$T_{Active}$	Time from power-on to ready to receive I <sup>2</sup> C commands			1.5		ms

**Note(s):**

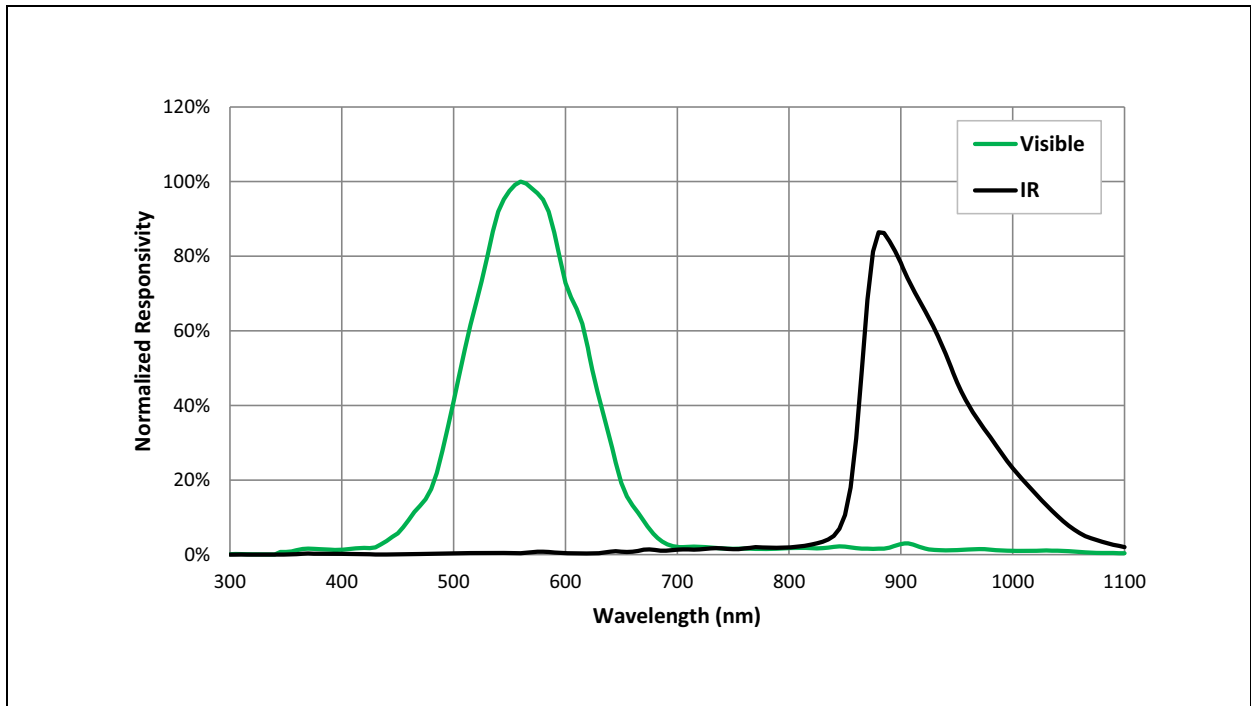
1. This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
2. Idle state occurs when PON=1 and all functions are not enabled.
3. Sleep state occurs when PON = 0 and I<sup>2</sup>C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
4. Digital pins: SDA, SCL, INT, are tolerant to a communication voltage up to 3.4V.

## Typical Operating Characteristics

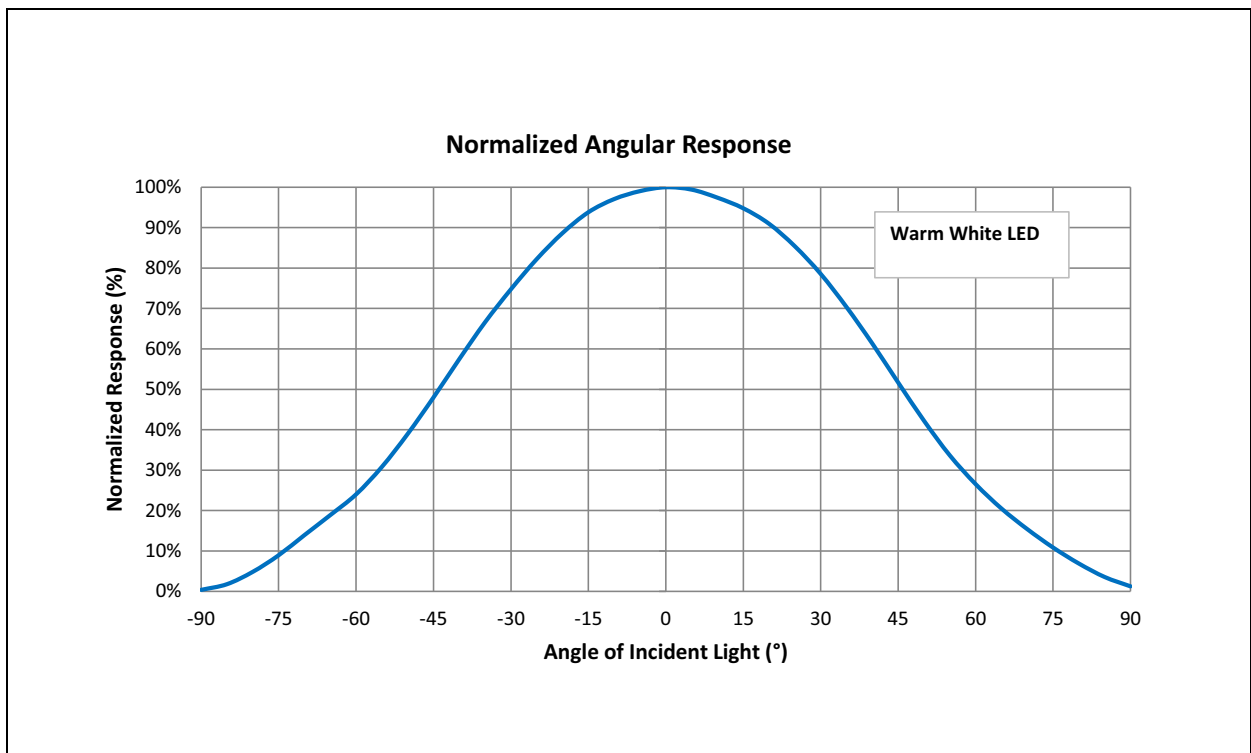
Figure 8:  
ALS Operating Characteristics,  $V_{DD} = 1.8V$ ,  $T_A = 25^\circ C$

Parameter	Conditions	Min	Typ	Max	Units
Integration time step size		2.68	2.78	2.90	ms
Number of integration steps		1		256	steps
Dark ADC count value	$E_e = 0 \mu W/cm^2$ ; AGAIN = 64x; ATIME = 100ms (0x23)	0	1	3	counts
$R_e$ Irradiance responsivity  Settings: AGAIN = 16x ATIME = 400ms	<b>Visible Channel</b>				
	White LED, 2700K	309	363	417	counts/ ( $\mu W/cm^2$ )
	<b>IR Channel</b>				
	$\lambda_D = 950 \text{ nm LED}$		352		counts/ ( $\mu W/cm^2$ )
Gain scaling, relative to 1x gain setting	AGAIN = 4x		4		x
	AGAIN = 16x		16		
	AGAIN = 64x		67		
	AGAIN = 128x		140		
ADC noise	AGAIN = 16x		0.005		% full scale

**Figure 9:**  
Spectral Responsivity



**Figure 10:**  
ALS Responsivity vs Angular Displacement



## Detailed Description

### Ambient Light Sensing

The ALS reception signal path begins as photodiodes receive filtered light and ends with the 16-bit results in the VISDATA<sub>L/H</sub> and IRDATA<sub>L/H</sub> registers. The visible channel's photodiode is filtered with a UV and IR filter to receive only visible light. The IR channel's photodiode is filtered to receive only IR. Signals from the photodiodes simultaneously accumulate for a period of time set by the value in ATIME before the results are available. Gain is adjustable from 1x to 128x to facilitate operation over a wide range of lighting conditions. Custom Lux equations can be created for specific applications and system designs.

### I<sup>2</sup>C Characteristics

The device uses I<sup>2</sup>C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes with a chip address of 0x39. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I<sup>2</sup>C bus is released).

During consecutive Read transactions, the future/repeated I<sup>2</sup>C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

#### ***I<sup>2</sup>C Write Transaction***

A Write transaction consists of a START, CHIP-ADDRESS<sub>WRITE</sub>, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9<sup>th</sup> clock pulse) the slave places an ACKNOWLEDGE/NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

#### ***I<sup>2</sup>C Read Transaction***

A Read transaction consists of a START, CHIP-ADDRESS<sub>WRITE</sub>, REGISTER-ADDRESS, START, CHIP-ADDRESS<sub>READ</sub>, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9<sup>th</sup> clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Alternately, if the previous I<sup>2</sup>C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without "re"-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESS<sub>READ</sub>, DATA BYTE(S), and STOP. Following all but



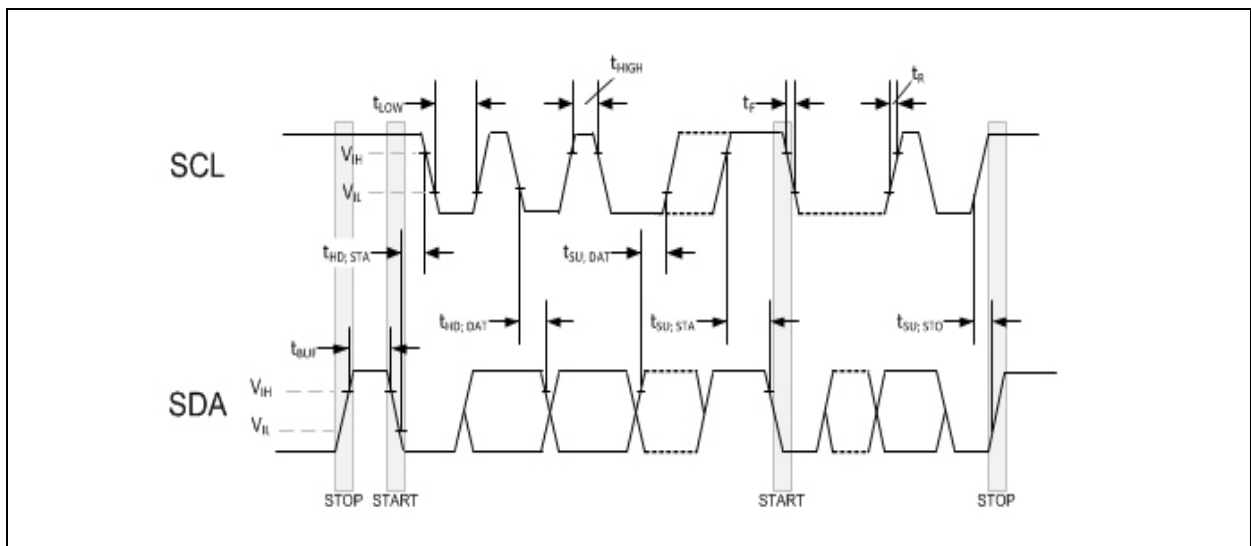
the final byte the master places an ACK on the bus (9<sup>th</sup> clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I<sup>2</sup>C bus protocol was developed by Philips (now NXP). For a complete description of the I<sup>2</sup>C protocol, please review the NXP I<sup>2</sup>C design specification at:

[www.i2c-bus.org/references/](http://www.i2c-bus.org/references/)

### Timing Diagrams

**Figure 11:**  
I<sup>2</sup>C Timing

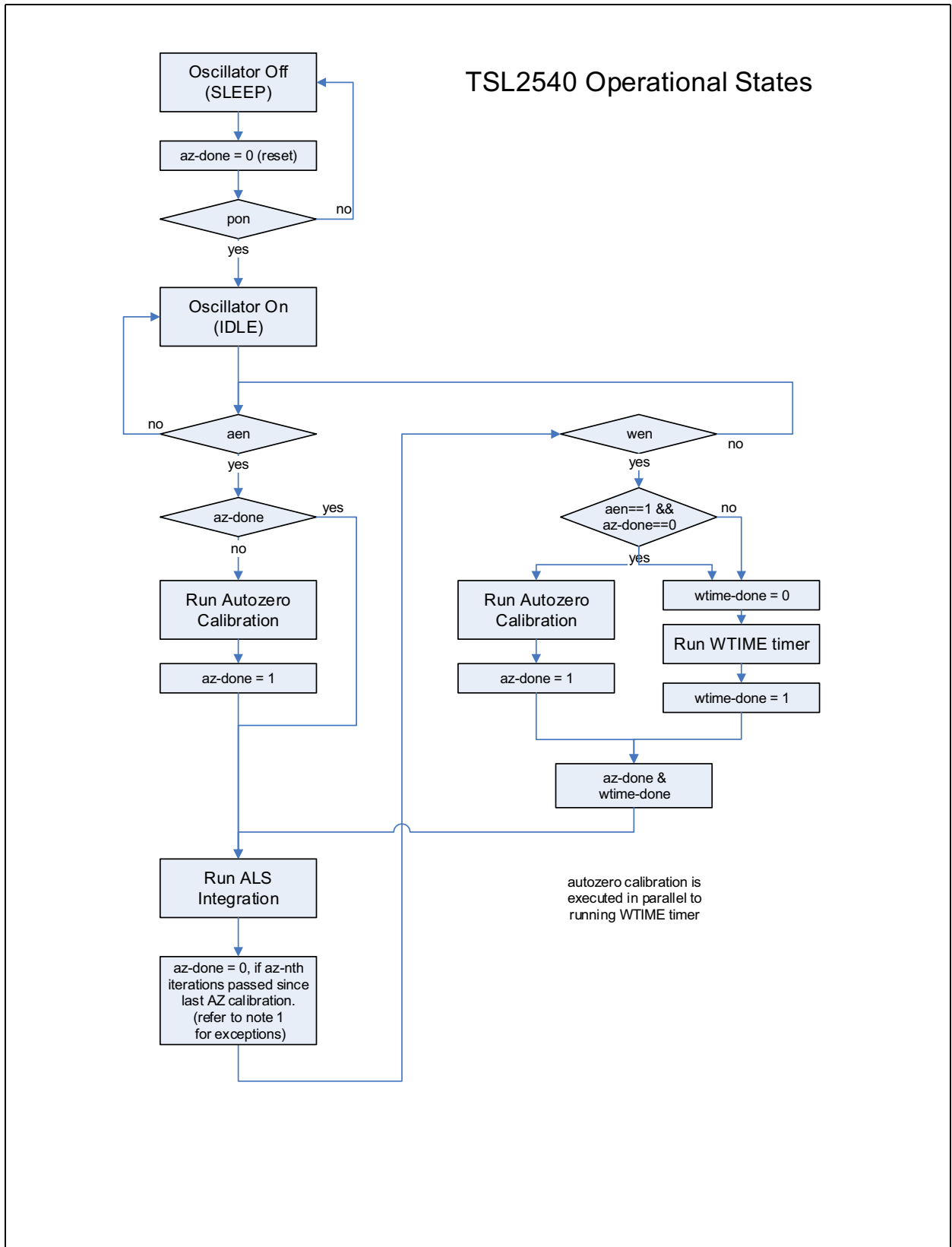


### Principles of Operation

#### System State Machine

An internal state machine provides system control of the ALS and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low power Sleep state. When a write on I<sup>2</sup>C bus to the Enable register (0x80) PON bit is set, the device transitions to the Idle state. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until the ALS function is enabled. Once enabled, the device will execute the ALS and Wait states in sequence as indicated in Figure 12. Upon completion, the device will automatically begin a new ALS-Wait cycle as long as PON and AEN remain enabled. If the ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I<sup>2</sup>C command is received clearing the interrupts in the STATUS register. See Interrupts for additional information.

Figure 12:  
Detailed State Diagram



**Note(s):**

1. An I<sup>2</sup>C write to az-nth-iteration register, except of the value 00h (disable-az), resets az-done independent of actual cntrl-state. In consequence, a new autozero calibration will be started in advance to the next ALS integration cycle.

## Register Description

**Figure 13:**  
**Register Overview**

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and functions	0x00
0x81	ATIME	R/W	ALS integration time	0x00
0x83	WTIME	R/W	Wait time	0x00
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x8C	PERS	R/W	ALS interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration register zero	0x80
0x90	CFG1	R/W	Configuration register one	0x00
0x91	REVID	R	Revision ID	0x61
0x92	ID	R	Device ID	0xE4
0x93	STATUS	R	Device status register	0x00
0x94	VISDATA L	R	Visible channel data low byte	0x00
0x95	VISDATA H	R	Visible channel data high byte	0x00
0x96	IRDATA L	R	IR channel data low byte	0x00
0x97	IRDATA H	R	IR channel data high byte	0x00
0x9E	REVID2	R	Auxiliary ID	REVID2
0x9F	CFG2	R/W	Configuration register two	0x04
0xAB	CFG3	R/W	Configuration register three	0x0C
0xD6	AZ_CONFIG	R/W	Autozero configuration	0x7F
0xDD	INTENAB	R/W	Interrupt enables	0x00

### Register Access:

- R = Read Only
- W = Write Only
- R/W = Read or Write
- SC = Self Clearing after access

## Detailed Register Description

### *Enable Register (Address 0x80)*

**Figure 14:**  
Enable Register

Addr: 0x80		Enable		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0000	RW	Reserved.
3	WEN	0	RW	This bit activates the wait feature. Active high.
2	Reserved	0	RW	Reserved.
1	AEN	0	RW	This bit activates the ALS function. Active high. *Set AEN=1 and PON=1 in the same command to ensure auto-zero function is run prior to the first measurement.
0	PON	0	RW	This field activates the internal oscillator and ADC channels. Active high.

Before activating AEN, preset each applicable operating mode registers and bits.

**ATIME Register (Address 0x81)****Figure 15:  
ATIME Register**

Addr: 0x81		ATIME					
Bit	Bit Name	Default	Access	Bit Description			
7:0	ATIME	0x00	RW	ALS value that specifies the integration time in 2.81ms intervals. 0x00 indicates 2.8ms. The maximum ALS value depends on the integration time. For every 2.81ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.8ms.			
				<b>Value</b>	<b>Integration Cycles</b>	<b>Integration Time</b>	<b>Maximum ALS Value</b>
				0x00	1	2.8ms	1023
				0x01	2	5.6ms	2047
				...	...	...	...
				0x3F	64	180ms	65535
				...	...	...	...
				0xFF	256	721ms	65535

The ATIME register controls the integration time of the ALS ADCs. The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.8ms nominal rate. Loading 0x00 will generate a 2.8ms integration time, loading 0x01 will generate a 5.6ms integration time, and so forth. The RC oscillator runs at 8MHz nominal rate. This gets divided by 11 to generate the integration clock of 727kHz. One count in ATIME (nominal 2.8ms) are 2.81ms. This is 2048 integration clock cycles:  $125\text{ns} * 11 * 8 * 256 = 2.81\text{ms}$ .

**WTIME Register (Address 0x83)**

**Figure 16:**  
WTIME Register

Addr: 0x83		WTIME				
Bit	Bit Name	Default	Access	Bit Description		
7:0	WTIME	0x00	RW	Value that specifies the wait time between ALS cycles in 2.81ms increments.		
				<b>Value</b>	<b>Increments</b>	<b>Wait Time</b>
				0x00	1	2.8ms (33.8ms)
				0x01	2	5.6ms (67.6ms)
				...	...	...
				0x3F	64	180ms (2.16s)
				...	...	...
				0xFF	256	721ms (8.65s)

The wait timer is implemented using a down counter.  
 Wait time = (value + 1) x 2.8ms. If WLONG is enabled then  
 Wait time = (value + 1) x 2.8ms x 12.

**AILTL Register (Address 0x84)**

**Figure 17:**  
AILTL Register

Addr: 0x84		AILTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	AILTL	0x00	RW	This register sets the low byte of the LOW ALS threshold.

The Visible (Vis) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

***AILTH Register (Address 0x85)*****Figure 18:**  
**AILTH Register**

Addr: 0x85		AILTH		
Bit	Bit Name	Default	Access	Bit Description
7:0	AILTH	0x00	RW	This register sets the high byte of the LOW ALS threshold.

The Visible (Vis) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is below the AILTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.

When setting the 16-bit ALS threshold AILTL must be written first, immediately followed by AILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

***AIHTL Register (Address 0x86)*****Figure 19:**  
**AIHTL Register**

Addr: 0x86		AIHTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	AIHTL	0x00	RW	This register sets the low byte of the HIGH ALS threshold.

The Visible (Vis) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.

The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert. When setting the 16-bit ALS threshold AIHTL must be written first, immediately followed by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

### AIHTH Register (Address 0x87)

Figure 20:  
AIHTH Register

Addr: 0x87		AIHTH		
Bit	Bit Name	Default	Access	Bit Description
7:0	AIHTH	0x00	RW	This register sets the high byte of the HIGH ALS threshold.

The Visible (Vis) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.

The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.

When setting the 16-bit ALS threshold AIHTL must be written first, immediately follow by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.



**PERS Register (Address 0x8C)****Figure 21:**  
**PERS Register**

Addr: 0x8C		PERS			
Bit	Bit Name	Default	Access	Bit Description	
7:4	Reserved	0000	RW	Reserved.	
3:0	APERS	0000	RW	This register sets the ALS persistence filter.	
				0	Every ALS cycle
				1	Any value outside ALS thresholds
				2	2 consecutive ALS values out of range
				3	3 consecutive ALS values out of range
				4	5 consecutive ALS values out of range
				5	10 consecutive ALS values out of range
				6	15 consecutive ALS values out of range
				7	20 consecutive ALS values out of range
				...	...
				13	50 consecutive ALS values out of range
				14	55 consecutive ALS values out of range
				15	60 consecutive ALS values out of range

The frequency of consecutive visible channel results outside of threshold limits are counted; this count value is compared against the APERS value. If the counter is equal to the APERS setting an interrupt is asserted. Any time a clear channel result is inside the threshold values the counter is cleared.

**CFG0 Register (Address 0x8D)**
**Figure 22:**  
**CFG0 Register**

Addr: 0x8D		CFG0		
Bit	Bit Name	Default	Access	Bit Description
7:3	Reserved	10000	RW	This field must be set to the default value.
2	WLONG	0	RW	When Wait Long is asserted the wait period as set by WTIME is increased by a factor of 12.
1:0	Reserved	00	RW	This field must be set to the default value.

The wait timer is implemented using a down counter.  
 Wait time = (value + 1) x 2.8ms. If WLONG is enabled then  
 Wait time = (value + 1) x 2.8ms x 12.

**CFG1 Register (Address 0x90)****Figure 23:**  
CFG1 Register

Addr: 0x90		CFG1			
Bit	Bit Name	Default	Access	Bit Description	
7:2	Reserved	000000	RW	Reserved.	
1:0	AGAIN	00	RW	This field sets the gain of the ALS sensor.	
				<b>Value</b>	<b>ALS Gain</b>
				0	1x
				1	4x
				2	16x
				3	64x

**REVID Register (Address 0x91)****Figure 24:**  
REVID Register

Addr: 0x91		REVID		
Bit	Bit Name	Default	Access	Bit Description
7:3	Reserved	01100	RO	Reserved.
2:0	REV_ID	001	RO	Device revision number.

**ID Register (Address 0x92)**

**Figure 25:**  
ID Register

Addr: 0x92		ID		
Bit	Bit Name	Default	Access	Bit Description
7:2	ID	111001	RO	Device type identification.
1:0	Reserved	00	RO	Reserved.

**Status Register (Address 0x93)**

**Figure 26:**  
Status Register

Addr: 0x93		Status Register		
Bit	Bit Name	Default	Access	Bit Description
7	ASAT	0	R, SC	The Analog Saturation flag signals that the ALS results may be unreliable due to saturation of the AFE.
6:5	Reserved	00	R, SC	Reserved.
4	AINT	0	R, SC	The ALS Interrupt flag indicates that ALS results (visible channel) have exceeded thresholds and persistence settings.
3	CINT	0	R, SC	The Calibration Interrupt flag indicates that calibration has completed.
2:0	Reserved	000	R, SC	Reserved.

All flags in this register can be cleared by setting the bit high. Alternatively, if the CFG3.int\_read\_clear bit is set, then simply reading this register automatically clears all eight flags.

**VISDATAL Register (Address 0x94)**

**Figure 27:**  
VISDATAL Register

Addr: 0x94		VISDATAL		
Bit	Bit Name	Default	Access	Bit Description
7:0	VISDATAL	0x00	RO	This register contains the low byte of the 16-bit visible channel data.

**VISDATAH Register (Address 0x95)****Figure 28:**  
VISDATAH Register

Addr: 0x95		VISDATAH		
Bit	Bit Name	Default	Access	Bit Description
7:0	VISDATAH	0x00	RO	This register contains the high byte of the 16-bit visible channel data.

**IRDATAL Register (Address 0x96)****Figure 29:**  
IRDATAL Register

Addr: 0x96		IRDATAL		
Bit	Bit Name	Default	Access	Bit Description
7:0	IRDATAL	0x00	RO	This register contains the low byte of the 16-bit IR channel data.

**IRDATAH Register (Address 0x97)****Figure 30:**  
IRDATAH Register

Addr: 0x97		IRDATAH		
Bit	Bit Name	Default	Access	Bit Description
7:0	IRDATAH	0x00	RO	This register contains the high byte of the 16-bit IR channel data.

**REVID2 Register (Address 0x9E)****Figure 31:**  
REVID2 Register

Addr: 0x9E		REVID2		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0000	RO	Reserved.
3:0	REVID2	000x	RO	Auxiliary identification (0000 or 0001)

**CFG2 Register (Address 0x9F)**

**Figure 32:**  
CFG2 Register

Addr: 0x9F		CFG2		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	000	RW	Reserved.
4	AGAINMAX	0	RW	This bit adjusts the overall ALS gain factor. See <a href="#">Figure 33</a> for recommended settings and corresponding overall ALS gain factor.
3	Reserved	0	RW	Reserved.
2	AGAINL	1	RW	This bit adjusts the overall ALS gain factor. See <a href="#">Figure 33</a> for recommended settings and corresponding overall ALS gain factor.
1:0	Reserved	00	RW	Reserved.

The ALS gain can be adjusted by setting the two AGAIN bits as well as the AGAINMAX and AGAINL bits which yields an overall range from ½x to 128x.

**Figure 33:**  
AGAIN Range

AGAIN[1]	AGAIN[0]	AGAINMAX	AGAINL	Overall ALS Gain
0	0	0	0	½
0	0	0	1	1
0	1	0	1	4
1	0	0	1	16
1	1	0	1	64
1	1	1	1	128

**CFG3 Register (Address 0xAB)****Figure 34:**  
**CFG3 Register**

Addr: 0xAB		CFG3					
Bit	Bit Name	Default	Access	Bit Description			
7	INT_READ_CLEAR	0	RW	If the Interrupt-Clear-by-Read bit is set, then all flag bits in the STATUS register will be reset whenever the STATUS register is read over I <sup>2</sup> C.			
6:5	Reserved	10	RW	Reserved.			
4	SAI	0	RW	The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pin assertion.			
				<b>PON</b>	<b>SAI</b>	<b>INT</b>	<b>Oscillator</b>
				0	X	X	OFF
				1	0	X	ON
				1	1	1	ON
1	1	0	OFF				
3:0	Reserved	1100	RW	Reserved.			

The SAI bit sets the device operational mode following the completion of an ALS cycle. If AINT and AIEN are both set or if PINT and PIEN are both set, causing an interrupt on the INT pin, and the SAI bit is set, then the oscillator will deactivate. The Device will appear as if PON = 0, however, PON will read as 1. The device can only be reactivated (oscillator enabled) by clearing the interrupts in the STATUS register.

**AZ\_CONFIG Register (Address 0xD6)**
**Figure 35:**  
**AZ\_CONFIG Register**

Addr: 0xD6		AZ_CONFIG		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0	RW	Reserved.
6:0	AZ_NTH_ITERATION	1111111	RW	Run autozero automatically before every n <sup>th</sup> ALS cycle (00h = never, n = every n <sup>th</sup> ALS cycle, and 7Fh = only before the first ALS cycle).

**INTENAB Register (Address 0xDD)**
**Figure 36:**  
**INTENAB Register**

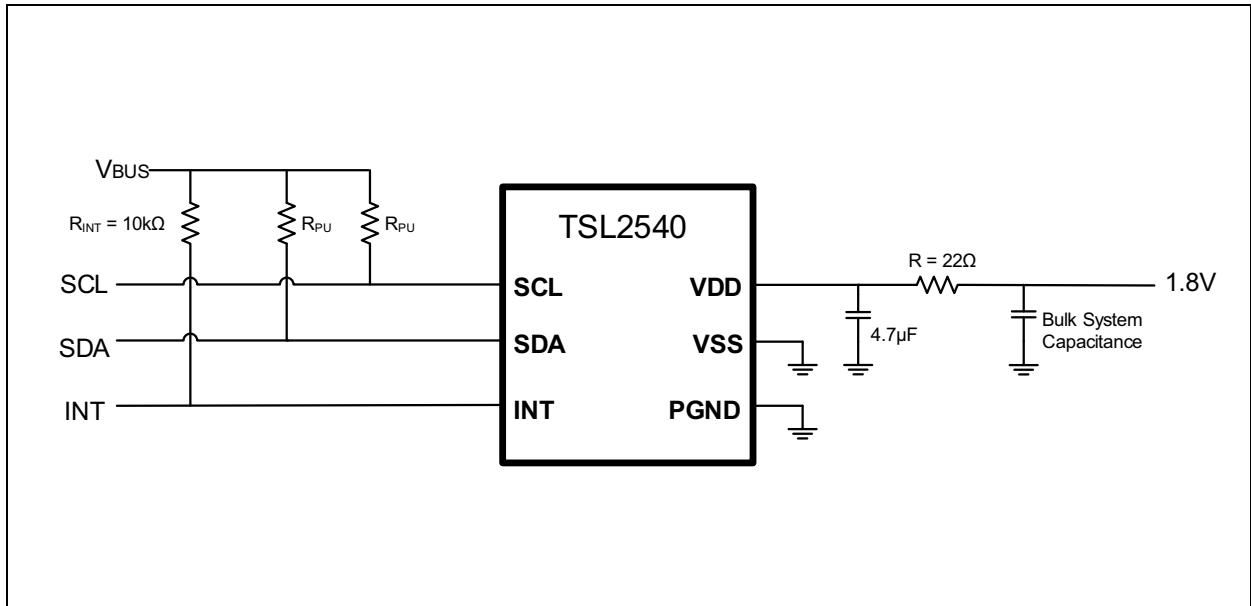
Addr: 0xDD		INTENAB		
Bit	Bit Name	Default	Access	Bit Description
7	ASIEN	0	RW	ALS Saturation Interrupt Enable.
6:5	Reserved	00	RW	Reserved.
4	AIEN	0	RW	ALS Interrupt Enable.
3:0	Reserved	0000	RW	Reserved.



## Application Information

### Schematic

**Figure 37:**  
Typical Applications Circuit

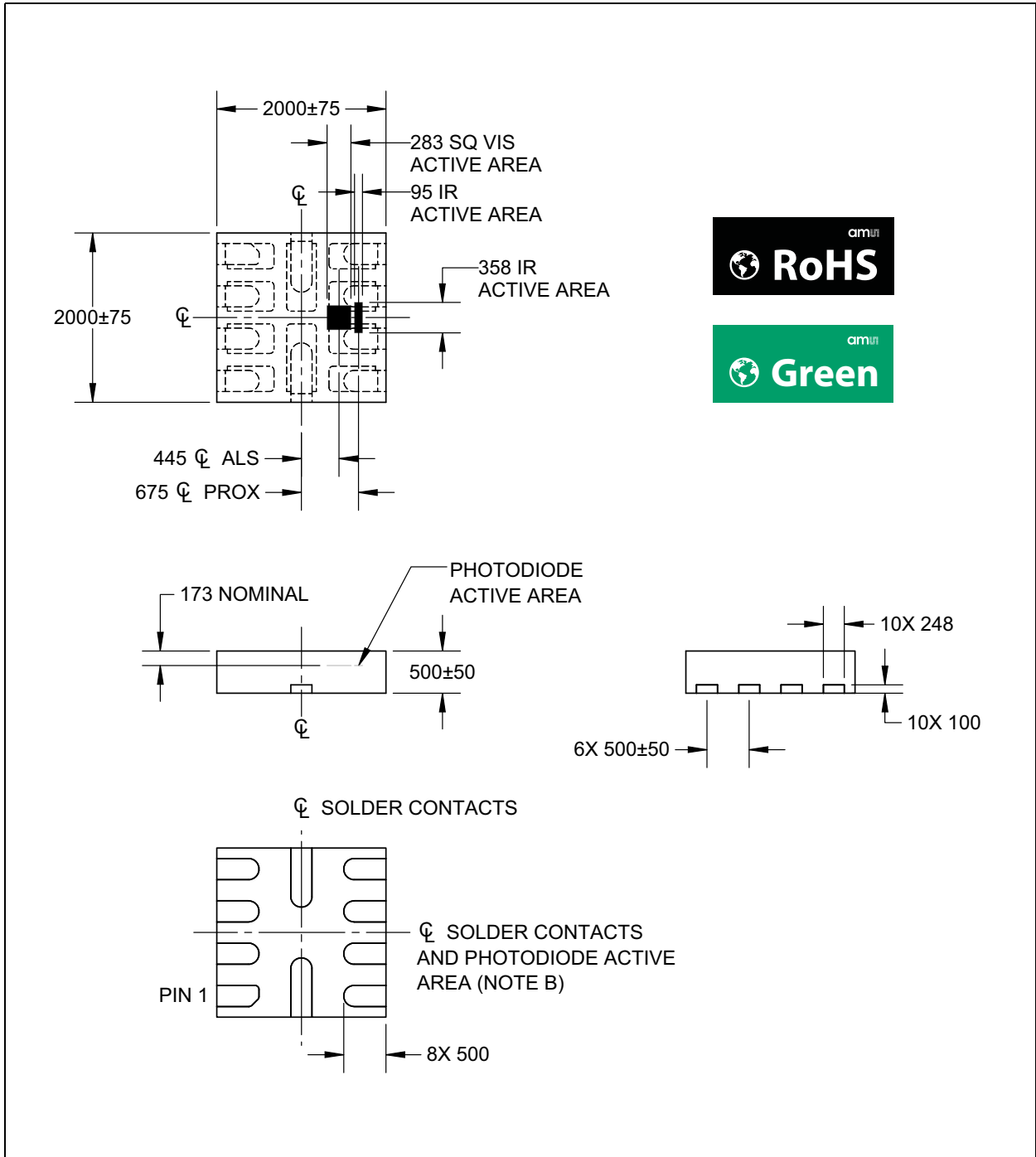


**Note(s):**

1. The value of the I<sup>2</sup>C pull up resistors R<sub>PU</sub> should be based on the 1.8V bus voltage, system bus speed and trace capacitance.
2. The bulk capacitor can affect the stability of a regulated supply output and should be chosen with the regulator characteristics in mind.
3. VSS and PGND should be connected to the same solid ground plane as close to the device as possible.

Package Drawings & Markings

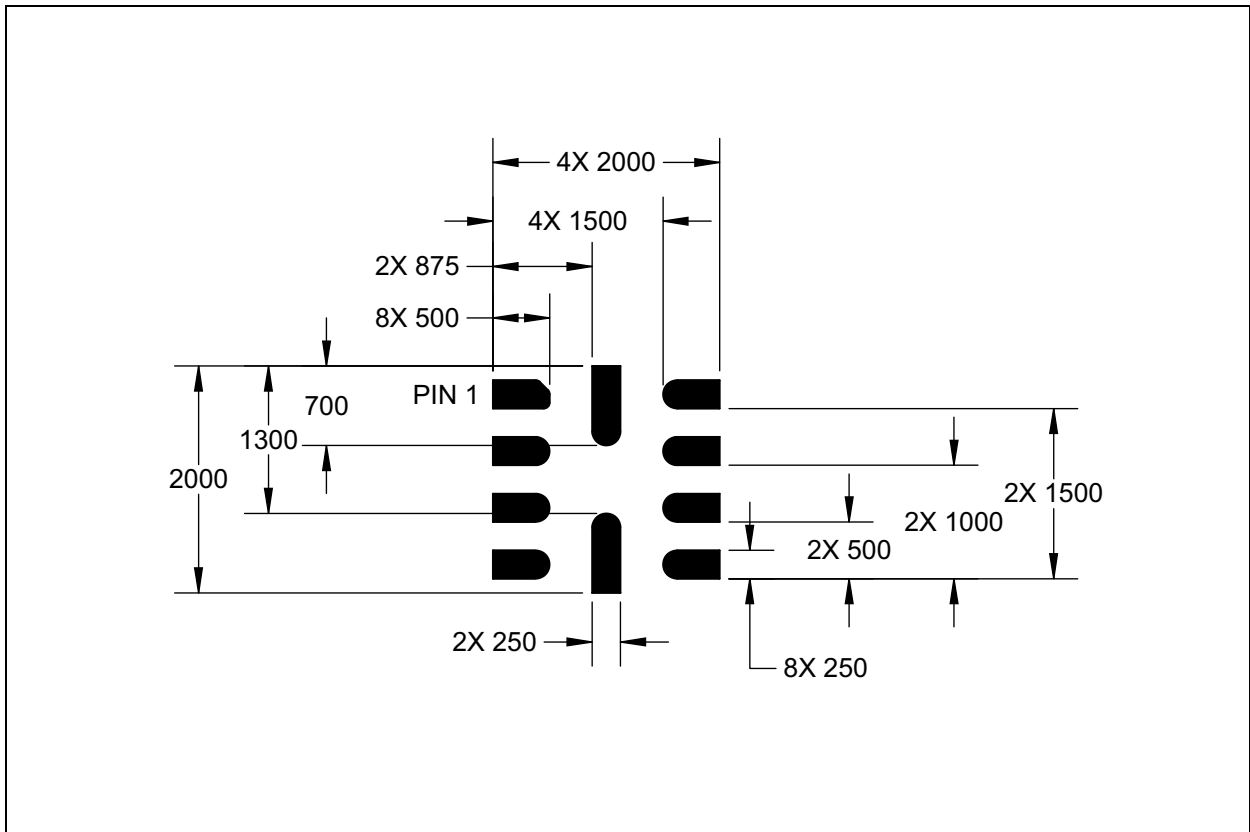
Figure 38:  
Package Drawing



Note(s):

1. All linear dimensions are in micrometers. Dimension tolerance is  $\pm 20 \mu\text{m}$  unless otherwise stated.
2. The die is centered vertically within the package within a tolerance of  $\pm 75 \mu\text{m}$ .
3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is Copper Alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

**Figure 39:**  
**Recommended PCB Pad Layout**

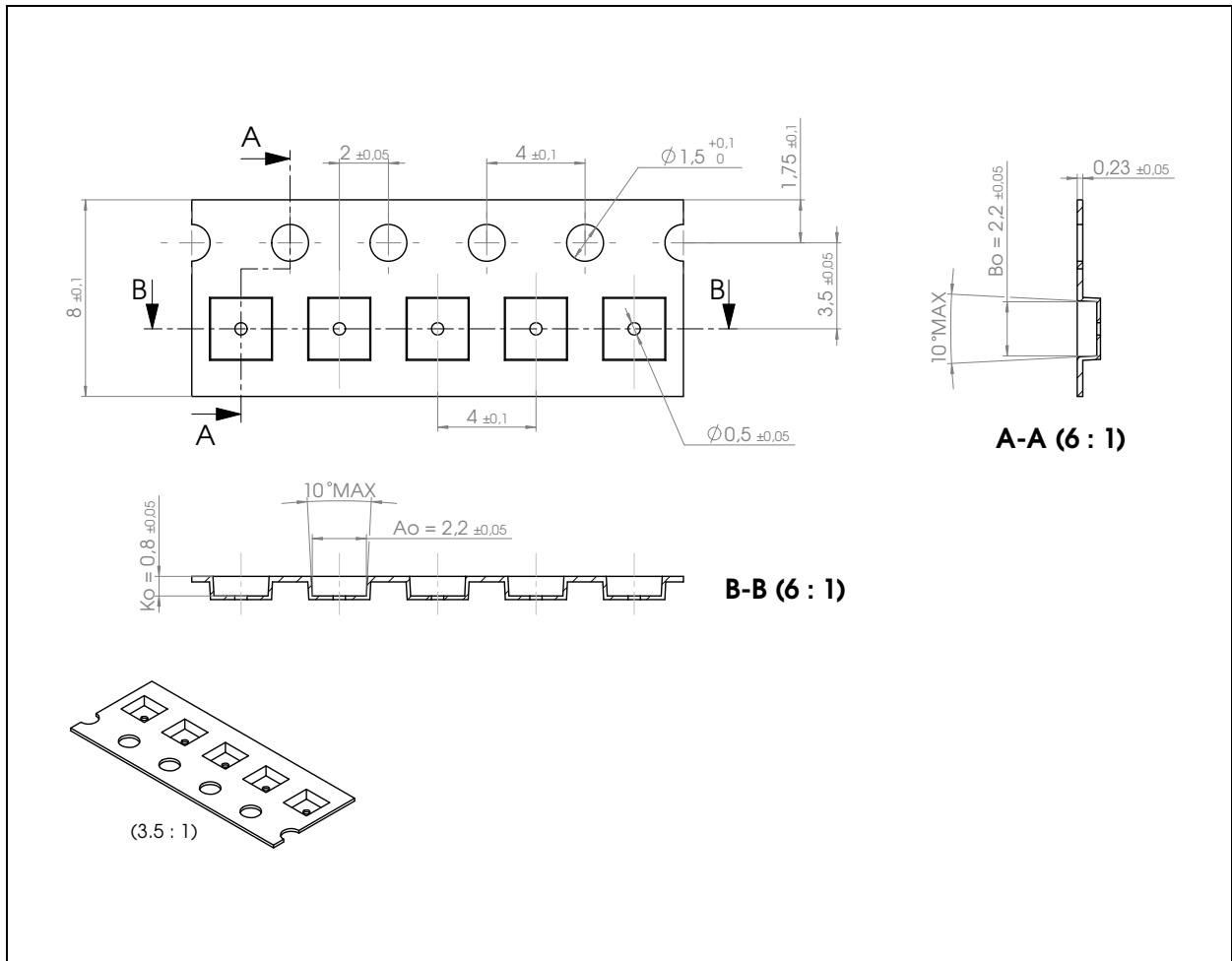


**Note(s):**

1. All dimensions are in micrometers.
2. Dimension tolerances are 50µm unless otherwise noted.
3. This drawing is subject to change without notice.

## Tape & Reel Information

Figure 40:  
Tape and Reel Information



**Note(s):**

1. All linear dimensions are in millimeters.
2. For missing tolerances and dimensions, refer to EIA-481.

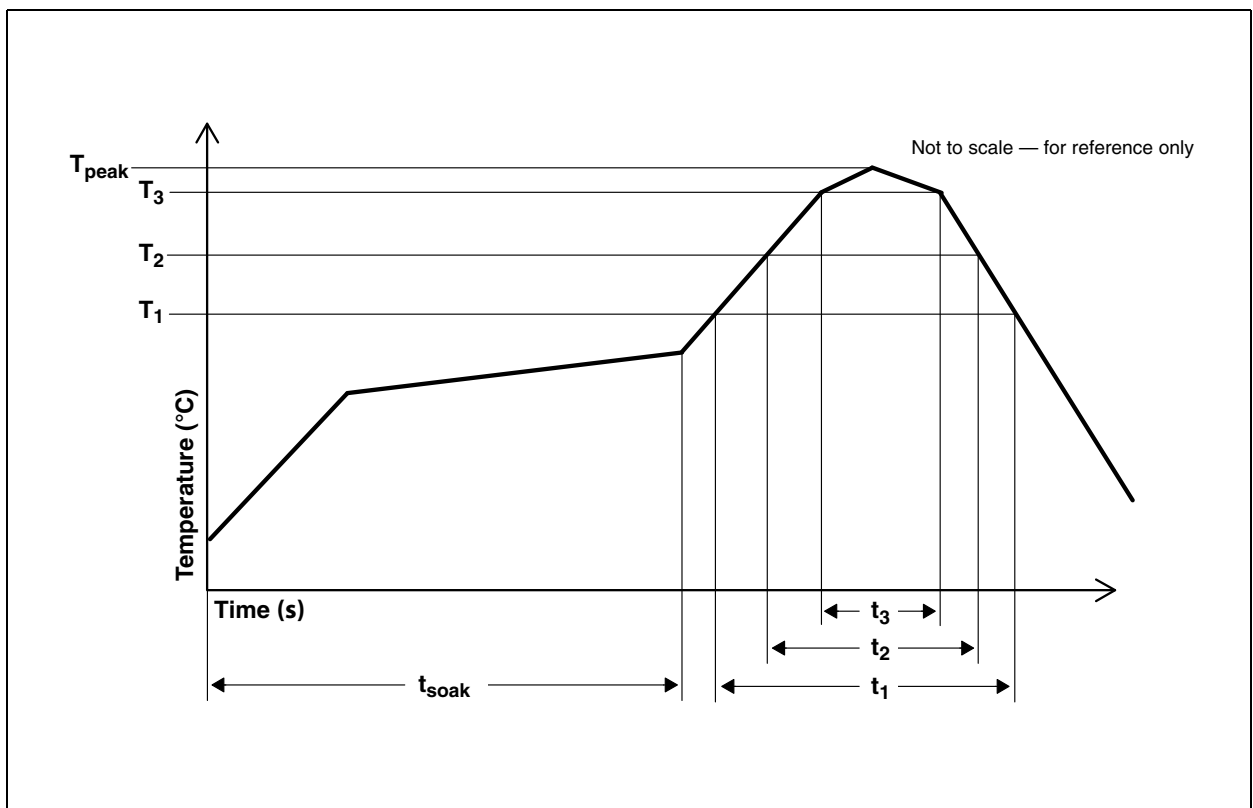
## Soldering & Storage Information

The QFN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

**Figure 41:**  
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	$t_{SOAK}$	2 to 3 minutes
Time above 217°C ( $T_1$ )	$t_1$	Max 60s
Time above 230°C ( $T_2$ )	$t_2$	Max 50s
Time above $T_{peak} - 10^\circ\text{C}$ ( $T_3$ )	$t_3$	Max 10s
Peak temperature in reflow	$T_{peak}$	260°C
Temperature gradient in cooling		Max - 5°C/s

**Figure 42:**  
Solder Reflow Profile Graph



## Storage Information

Moisture Sensitivity Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

## Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

## Floor Life

The QFN package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

## Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

## Ordering & Contact Information

**Figure 43:**  
Ordering Information

Ordering Code	I <sup>2</sup> C Bus	I <sup>2</sup> C Address	Delivery Form	Delivery Quantity
TSL25403	1.8V	39h	Tape and Reel	10000 pcs/reel
TSL25403M	1.8V	39h	Tape and Reel	1000 pcs/reel

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Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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## Revision Information

Changes from 1-02 (2019-Jan-10) to current revision 1-03 (2019-Mar-20)	Page
Updated figure 8	6
Updated text under “System State Machine”	9
Updated figure 13	11
Updated figure 31	21
Updated text under figure 34	23

**Note(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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