GaAs MMIC 5 WATT T/R SWITCH DC - 3 GHz

RoHS✓ EARTH FRIENDLY

Designer's Kit Available

Typical Applications

The HMC574MS8 / HMC574MS8E is ideal for:

- Cellular/3G Infrastructure
- Private Mobile Radio Handsets
- WLAN, WiMAX & WiBro
- Automotive Telematics
- Test Equipment

Features

Low Insertion Loss: 0.3 dB

High Third Order Intercept: +65 dBm

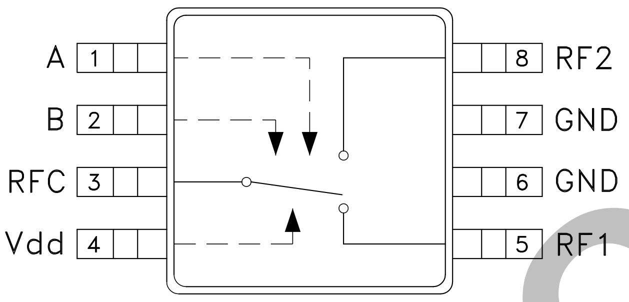
Isolation: 30 dB

Single Positive Supply: +3 to +8V

SMT Package: MSOP8

Included in the HMC-DK005 Designer's Kit

Functional Diagram



General Description

The HMC574MS8 & HMC574MS8E are low-cost SPDT switches in 8-lead MSOP packages for use in transmit/receive applications which require very low distortion at high incident power levels. The device can control signals from DC to 3 GHz and is especially suited for Cellular/3G infrastructure, WiMAX and WiBro applications with only 0.3 dB typical insertion loss. The design provides 5 watt power handling performance and +65 dBm third order intercept at +8 Volt bias. RF1 and RF2 are reflective shorts when "Off".

Electrical Specifications, T_A = +25° C, Vctl = 0/+5 Vdc, Vdd = +5 Vdc (Unless Otherwise Stated), 50 Ohm System

Parameter		Frequency	Min.	Typ.	Max.	Units
Insertion Loss		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		0.25 0.3 0.4 0.5	0.5 0.6 0.7 0.8	dB dB dB dB
Isolation		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz	26 24 21 16	30 28 25 20		dB dB dB dB
Return Loss		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		35 25 18 16		dB dB dB dB
Input Power for 1dB Compression	Vctl = 0/+3V Vctl = 0/+5V Vctl = 0/+8V	0.5 - 3.0 GHz	33 35 37	36 38 39		dBm dBm dBm
Input Third Order Intercept (Two-tone Input Power = +27 dBm Each Tone)	Vctl = 0/+3V Vctl = 0/+5V Vctl = 0/+8V	0.5 - 3.0 GHz		55 63 65		dBm dBm dBm
Switching Characteristics	 tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 3.0 GHz		 80 120		 ns ns

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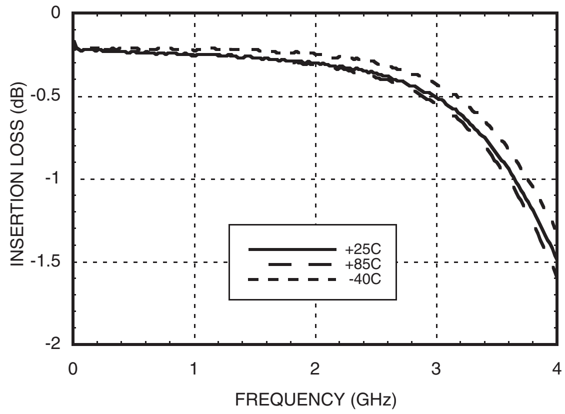
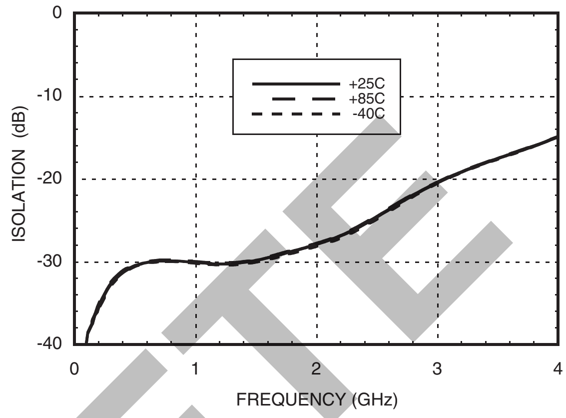
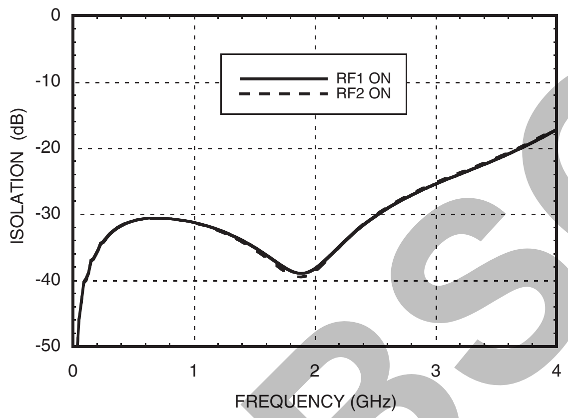
Insertion Loss



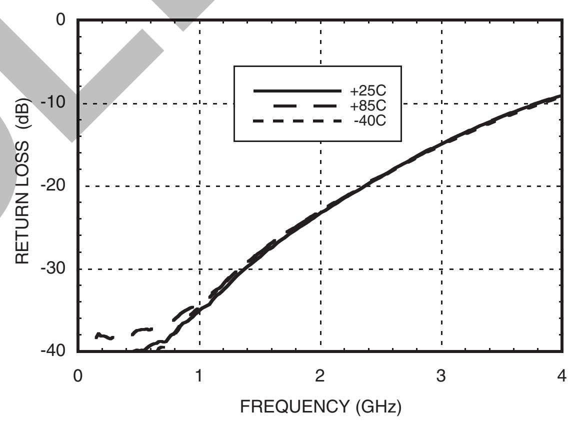
Isolation Between RFC & RF1/RF2



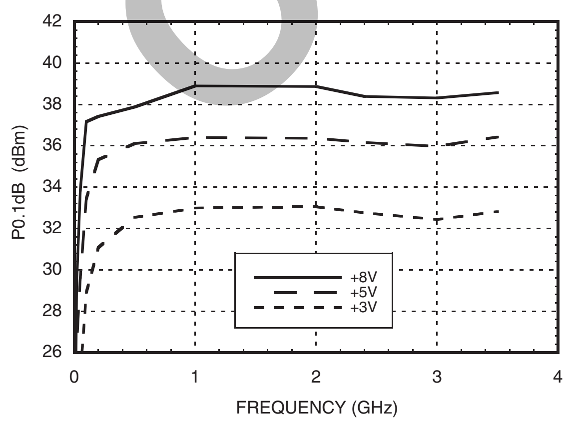
RF1 to RF2 Isolation



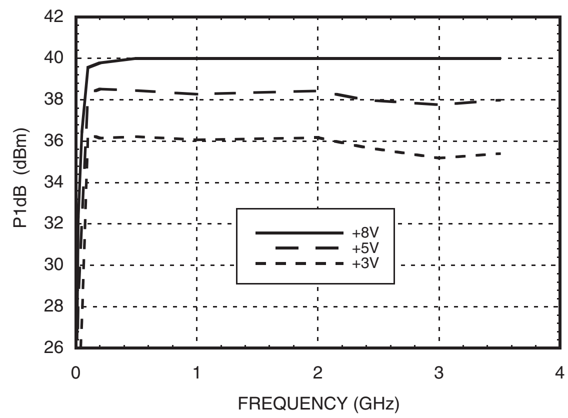
Return Loss



Input P0.1dB vs. Vdd



Input P1dB vs. Vdd



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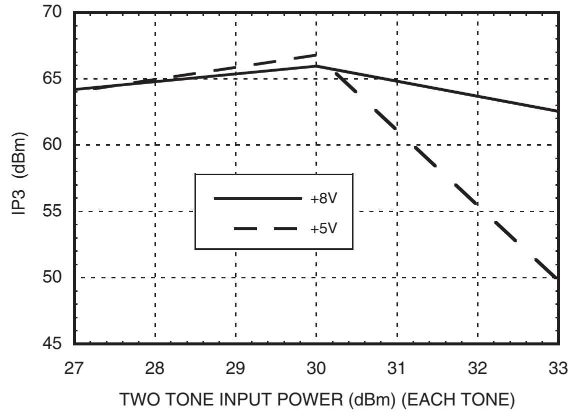
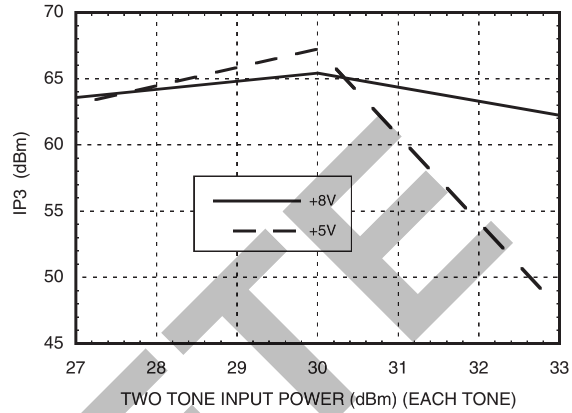
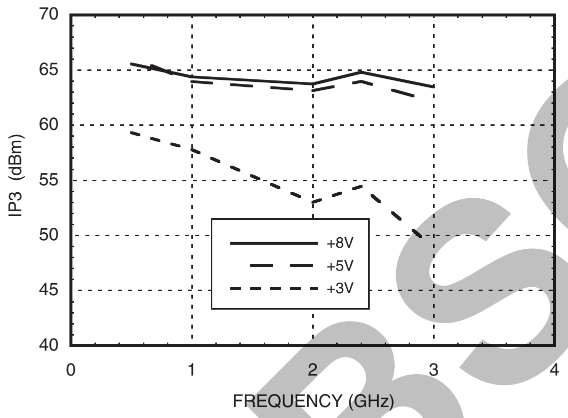
Input IP3 vs. Input Power @ 900 MHz



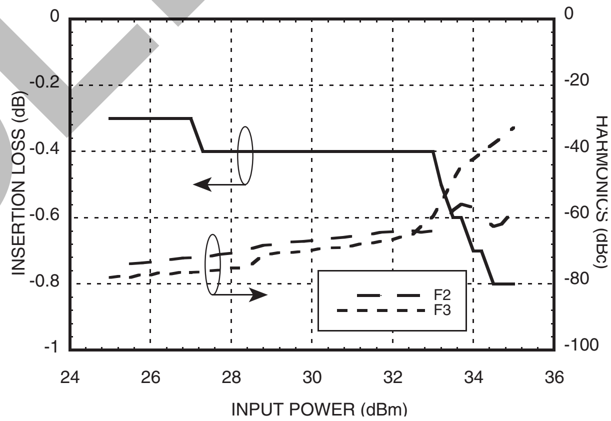
Input IP3 vs. Input Power @ 1900 MHz



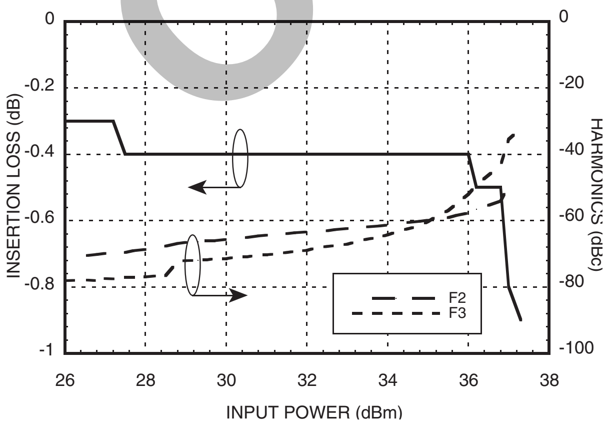
Input Third Order Intercept



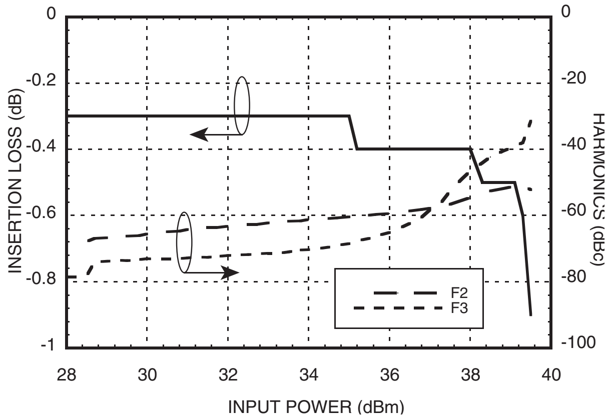
2nd & 3rd Harmonics @ 900 MHz Vdd = +3 Volts



2nd & 3rd Harmonics @ 900 MHz Vdd = +5 Volts



2nd & 3rd Harmonics @ 900 MHz Vdd = +8 Volts



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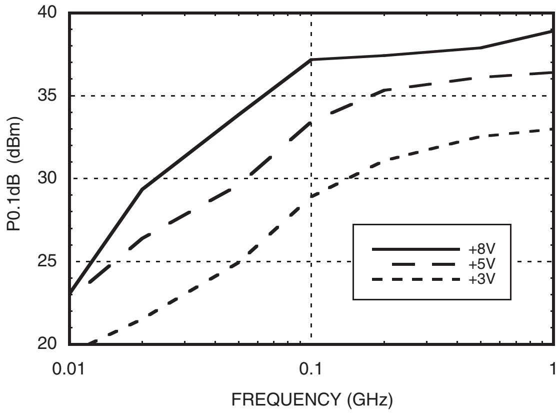
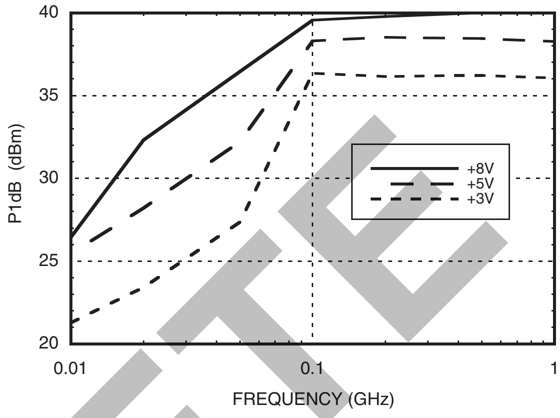
Input P0.1dB vs. Vdd



Input P1dB vs. Vdd



OBSOLETE

Absolute Maximum Ratings

Max. Input Power V_{dd} = 0/+8V	0.5 - 2.5 GHz	39 dBm
Bias Voltage Range (Vdd)		-0.2 to +10 Vdc
Control Voltage Range (A & B)		-0.2 to +Vdd Vdc
Hot Switching Power Level V_{dd} = +8V		39 dBm
Channel Temperature		150 °C
Continuous Pdiss (T= + 85 °C) (derate 10 mW/°C above 85 °C)		0.65W
Thermal Resistance		100 °C/W
Storage Temperature		-65 to +150 °C
Operating Temperature		-40 to +85 °C
ESD Sensitivity (HBM)		Class 1A

DC Blocks are required at ports RFC, RF1 and RF2

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Bias Voltage & Current

Vdd (Vdc)	Typical Idd (µA)
+3	2
+5	10
+8	40

Control Voltages

State	Bias Condition
Low	0 to +0.2 Vdc @ 10 µA Typical
High	Vdd ± 0.2 Vdc @ 10 µA Typical

Truth Table

Control Input (Vctl)		Signal Path State	
A	B	RFC to RF1	RFC to RF2
High	Low	Off	On
Low	High	On	Off

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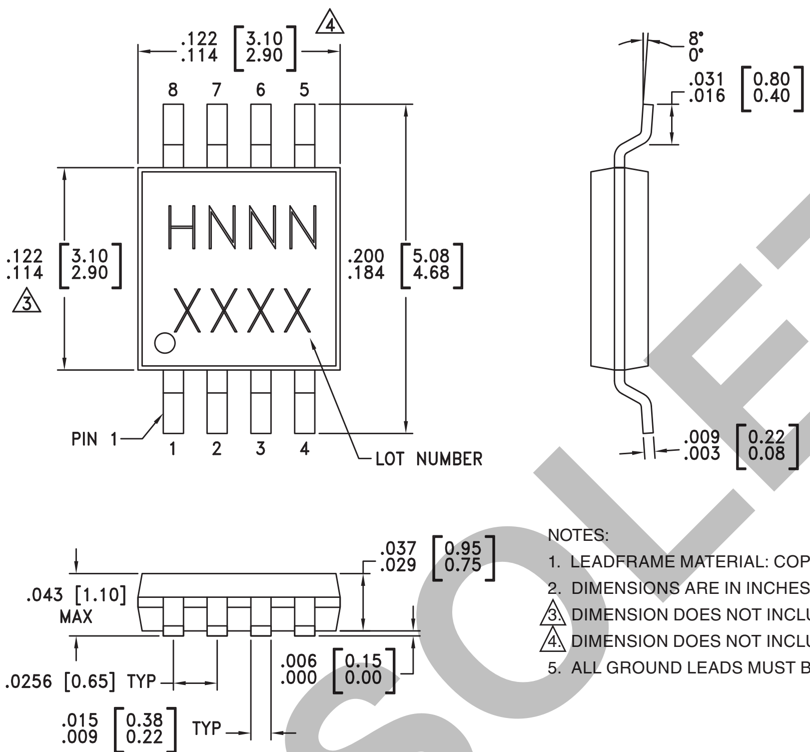
Outline Drawing



NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC574MS8	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H574 XXXX
HMC574MS8E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H574 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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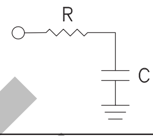
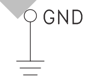
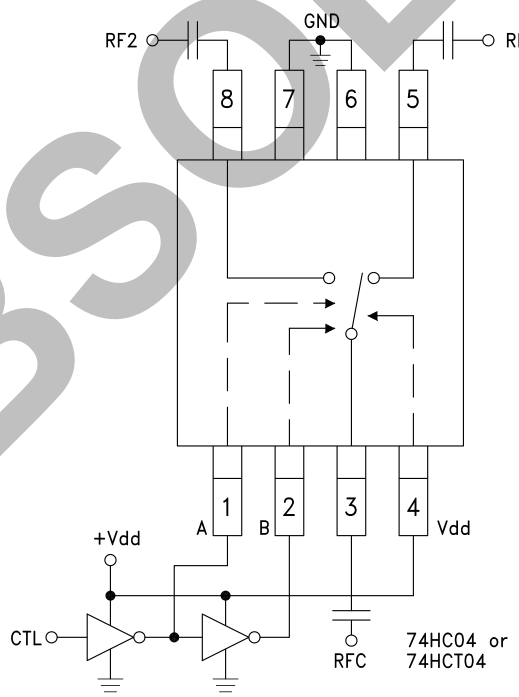
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	A	See truth table and control voltage table.	
2	B	See truth table and control voltage table.	
3, 5, 8	RFC, RF1, RF2	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required.	
4	Vdd	Supply Voltage.	
6, 7	GND	This pin must be connected to RF/DC ground.	

Typical Application Circuit



Notes:

1. Set logic gate and switch Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of +3 to +8 Volts applied to the CMOS logic gates and to pin 4 of the RF switch.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with Vdd set to +8V. The switch will operate properly (but at lower RF power capability) at bias voltages down to +3V.

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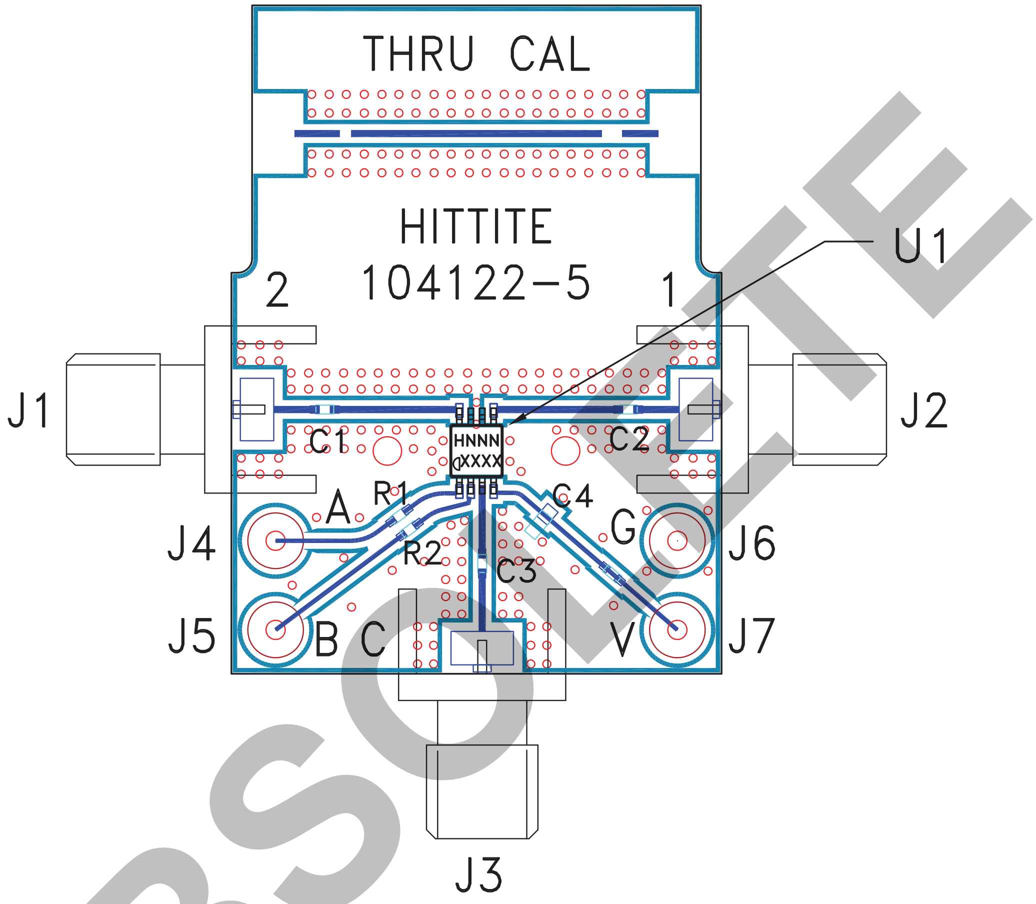
Evaluation Circuit Board



List of Materials for Evaluation PCB 104124 [1]

Item	Description
J1 - J3	PCB Mount SMA RF Connector
J4 - J7	DC Pin
C1 - C3	100 pF capacitor, 0402 Pkg.
C4	10,000 pF capacitor, 0603 Pkg.
R1, R2	100 Ohm resistor, 0402 Pkg.
U1	HMC574MS8 / HMC574MS8E T/R Switch
PCB [2]	104122 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 ohm impedance and the package ground leads and package bottom should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.

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