HMC700LP4 / 700LP4E

v11.0411

8 GHz 16-Bit Fractional-N PLL

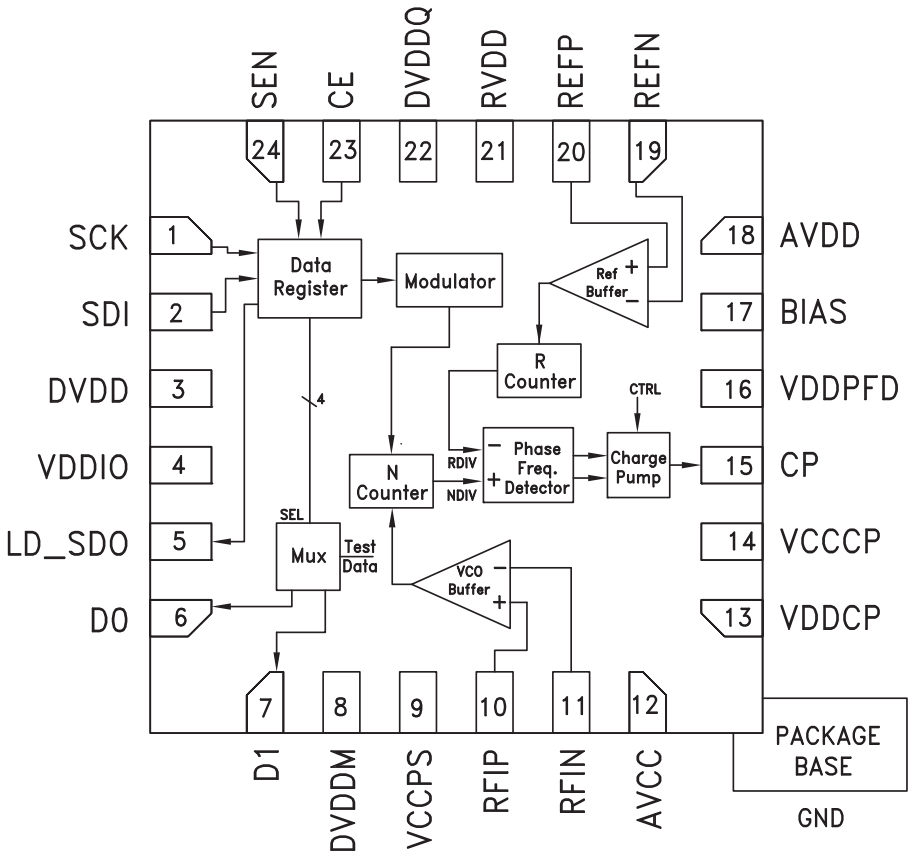
Features

- 8 GHz, 16 bit prescaler
- Fractional or Integer Modes
- Ultra Low Phase Noise
  6 GHz; 50 MHz Ref.
  -103 / -108 dBc/Hz @ 20 kHz
  (Frac / Integer)
  Figure of Merit (FOM)
  -221 / -226 dBc/Hz (Frac / Integer)
- 24 bit step size resolution, 3 Hz typ
- 200 MHz, 14bit reference path input
- Direct FSK Modulation Mode
- Cycle Slip Prevention
- Read / Write Serial Port, Chip ID
- 24 Lead 4x4mm SMT Package: 16mm²

Typical Applications

- Base Stations for Mobile Radio
- WiMAX
- Test & Measurement
- CATV Equipment
- Phased Array Applications
- Simple FSK Links
- DDS Replacement

Functional Diagram



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General Description

The HMC700LP4(E) is a SiGe BiCMOS fractional-N PLL. The PLL includes a very low noise digital phase frequency detector (PFD), and a precision controlled charge pump.

The fractional PLL features an advanced delta-sigma modulator design that allows both ultra-fine step sizes and very low spurious products. Spurious outputs are low enough to eliminate the need for costly Direct Digital Synthesis (DDS) references in many applications.

The HMC700LP4(E) phase-frequency detector (PFD) features cycle slip prevention (CSP) technology that allows faster frequency hopping times.

Ultra low in-close phase noise and low spurious also permit architectures with wider loop bandwidths for faster frequency hopping and low micro-phonics. FSK mode allows the synthesizer to be used as a simple low cost direct FM transmitter source.

Recommended level >500mVpp. With 250mVpp phase noise degradation may occur.

Electrical Specifications, VDDCP, VCCCP = 5V; RVDD, AVDD, DVDDM, VDDPFD, DVDD, VDDIO, DVDDQ, VCCPS, AVCC = 3.3V ±5%; AGND = DGND = 0V

Parameter	Conditions	Min	Typ	Max	Units
RF Input Characteristics					
Max RF Input Frequency (3.3V)		8	9		GHz
Min RF Input Frequency			100	200	MHz
RF Input Sensitivity	AC coupling only. Recommended range -10 to -5dBm. Operation with higher levels, up to +7dBm is allowable, but phase noise degradation may occur.	-10		0	dBm
RF Input Level Differential	AC coupling only.	-16		+6	dBm
16 bit divider (Integer)	N Divide ratio, 2^{16} + 31	32		65,567	
16 bit divider (fractional)	2^{16}-1	36		65,535	
REF Input Characteristics					
Max Ref Input Frequency (3.3V)		200			MHz
Min Ref Input Frequency				200	kHz
Ref Input Sensitivity	AC coupling only. Recommended level >500mVpp. With 250mVpp phase noise degradation may occur.	250		3000	mVpp
Ref Input Level Differential	AC coupling only	250		5000	mVpp
14 bit Ref Divider Range		1		16,383	
Phase Detector					
Phase Detector Frequency (Frac)			50	70	MHz
Phase Detector Frequency (Integ)		0.2		100	MHz

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Parameter	Conditions	Min	Typ	Max	Units
Charge Pump					
Max Output Current			2		mA
Min Output Current			500		µA
Charge Pump Noise	Input referred, 50 MHz ref, 20 kHz		-145		dBc/Hz
Logic Inputs					
VIH Input High Voltage		VDDIO-0.4		VDDIO	V
VIL Input Low Voltage		0		0.4	V
Logic Outputs					
VOH Input High Voltage		VDDIO-0.4		VDDIO	V
VOL Input Low Voltage		0		0.4	V
Serial Port Max Clock			50		MHz
Power Supplies					
RVDD, AVDD, VDDPFD, AVCC, VCCPS - Analog supply	AVDD should equal DVDD	2.7	3.3	3.4	V
DVDD, DVDDM, DVDDQ, VDDIO – Digital Supply	All must be equal	2.7	3.3	3.4	V
VDDCP, VCCCP Charge Pump Supplies	VCCCP and VDDCP must be equal	4.5	5	5.5	V
Total Current Consumption (5V)	6 GHz operation		5.5	7	mA
Total Current Consumption (3V)	6 GHz operation		90	110	mA
Power Down Current			1	10	µA
Bias Reference Voltage	Measured with 10 G Ohm Meter	1.880	1.920	1.960	V
Phase Noise					
6 GHz VCO, Integer Mode	20kHz offset, 50 MHz fPFD		-108		dBc/Hz
6 GHz VCO, Fractional Mode	20kHz offset, 50 MHz fPFD		-103		dBc/Hz

Absolute Maximum Ratings

Nominal 3V Supplies to GND	-0.3V to +3.6V
Nominal 3V Digital Supply to 3V Analog Supply	-0.3V to +0.3V
Nominal 5V Supply to GND	-0.3V to +5.8V
VCO Divider Input Single-Ended	+7 dBm
VCO Divide Input Differential	+13 dBm
Maximum Junction Temperature	+125 °C
Continuous Power Diss. (T= 85° C) (Derate 51 mW/°C above 85°C	3.3 W
Thermal Resistance (R1) (junction to ground paddle)	19.7 °C/W
Reflow Soldering	
Peak Temperature Time at Peak Temperature	260 °C 40 Sec
Operating Temperature	-40 °C to +85 °C
Storage Temperature Range	-65 °C to +125 °C
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Pin Descriptions

Pin Number	Function	Description
1	SCK	Serial port clock input
2	SDI	Serial port data input
3	DVDD	Power supply pin for internal digital circuitry. Nominally 3V
4	VDDIO	Power Supply for digital I/O driver
5	LD_SDO	Lock Detect, Main Serial Data Output or VCO Serial Port Data Out
6	D0	GPO Output Bit 0, VCO Serial Port LE when in VCO Serial Port Mode
7	D1	GPO Output Bit 1, VCO Serial Port Clock when in VCO Serial Port Mode
8	DVDDM	Digital Power Supply for M-Counter, Nominally 3V
9	VCCPS	Analog Power Supply for Prescaler, Nominally 3V
10	RFIP	Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.
11	RFIN	Complementary Input to the RF Prescaler. For single-ended input this point must be decoupled to the ground plane with a ceramic bypass capacitor, typically 100 pF.
12	AVCC	Analog Power supply pin for the RF Section. A decoupling capacitor to the ground plane should be placed as close as possible to this pin. Nominally 3V
13	VDDCP	+5V Power Supply for charge pump digital section
14	VCCCP	+5V Power Supply for the charge pump analog section
15	CP	Charge pump output
16	VDDPFD	Analog Power supply for the phase frequency detector, Nominally 3V
17	BIAS [1]	External bypass decoupling for precision bias circuits, 1.920V ±20 mV [1]
18	AVDD	Analog Power supply for analog ref paths, Nominally 3V
19	REFN	Reference input (Negative or decoupled)
20	REFP	Reference input (Positive)
21	RVDD	Ref path supply
22	DVDDQ	Digital supply for Substrate, Nominally 3V
23	CE	Chip Enable
24	SEN	Serial port latch enable input

[1] NOTE: BIAS ref voltage cannot drive an external load. Must be measured with 10GOhm meter such as Agilent 34410A, typical 10Mohm DVM will read erroneously.

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Figure 1.

Typical Phase Noise Plots

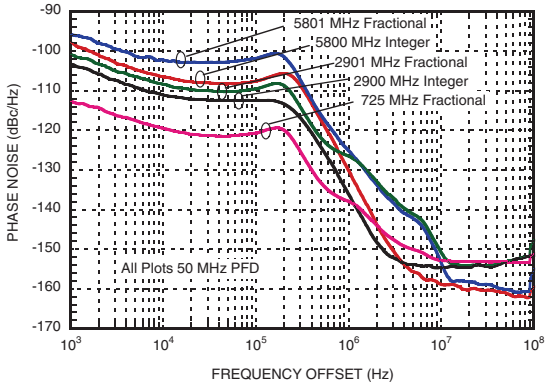


Figure 2.

Comparison of Low PFD Integer Mode w/ High PFD Fractional at 1 GHz

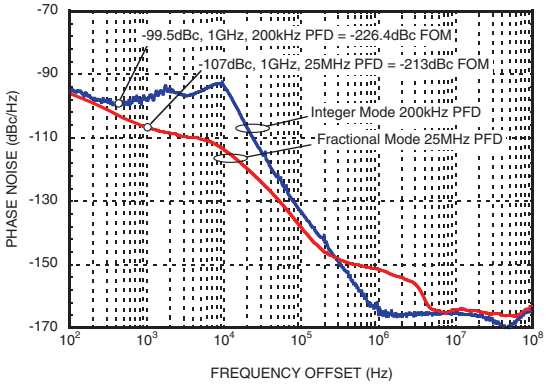


Figure 3.

Typical Phase Noise Performance vs. Charge Pump Output Voltage

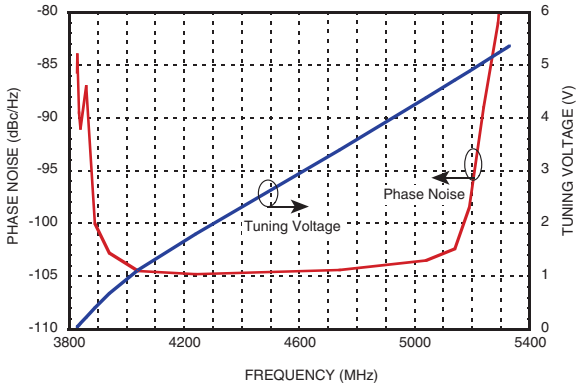


Figure 4.

RF Divider Sensitivity vs. Frequency, Mode and Temperature, +3.3V

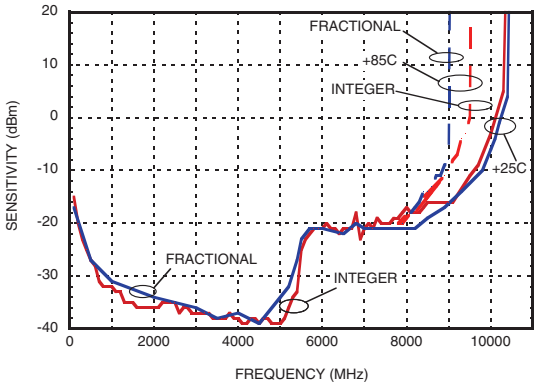


Figure 5.

Example of Cycle Slip Prevention for Frequency Hop from 5200 to 3950 MHz

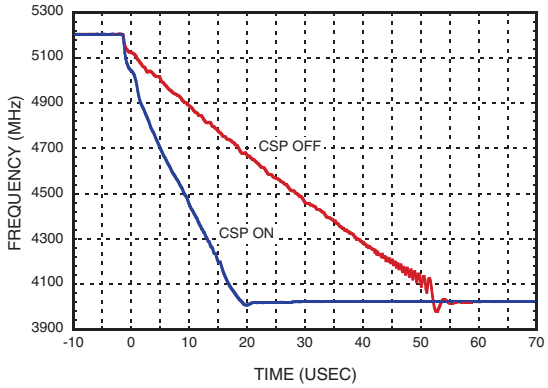
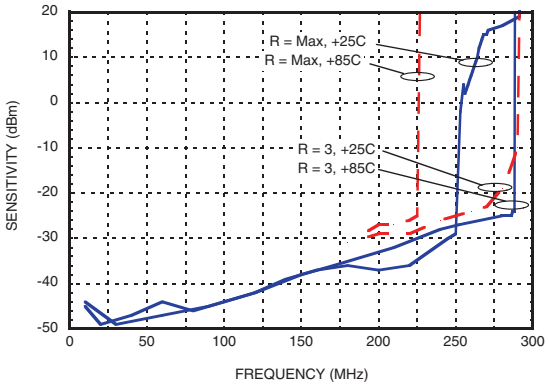


Figure 6.

Typical Reference Sensitivity vs. Frequency, 3.3V



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Theory of Operation

The HMC700LP4(E) is targeted for ultra low phase noise applications. The synthesizer has been designed with very low noise reference path, phase detector and charge pump.

External VCO

The HMC700LP4(E) is targeted for ultra low phase noise applications with an external VCO. The synthesizer charge pump can operate with the charge pump supply as high as 5.5 Volts. The charge pump output at the varactor tuning port, normally can maintain low noise performance to within 500mV of either ground or the upper supply voltage (see example (figure 3)

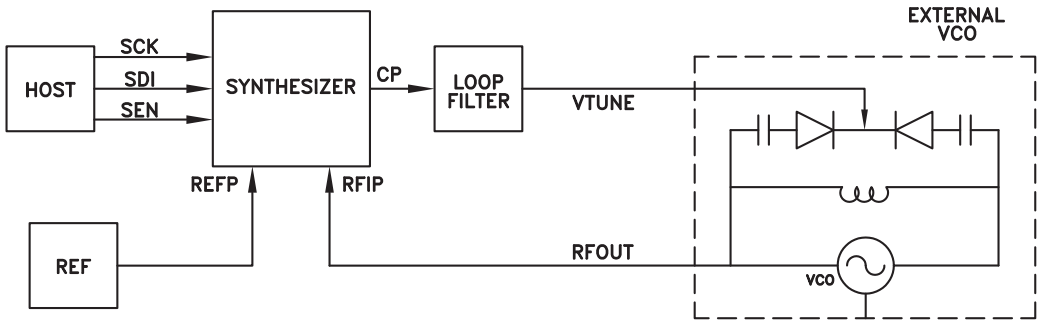

Figure 7. HMC700LP4(E) Synthesizer with External VCO

High Performance Low Spurious Operation

The HMC700LP4(E) has been designed for the best phase noise possible in an integrated synthesizer. Spurious signals in a synthesizer can occur in any mode of operation and can come from a number of sources. In general spurious can be the result of interference that gets through the loop filter and modulates the input tuning port of the VCO directly. It can also result from interference that modulates the VCO indirectly through power supplies, ground, or output ports, or bypasses the loop filter due to poor isolation of the filter. It can also simply add to the output of the synthesizer.

Interference is always present at multiples of the PFD frequency, and the input reference frequency. Depending upon the mode of operation of the synthesizer spurious may also occur at integer sub-multiples of the reference frequency. If the fractional mode of operation is used the difference between the VCO frequency and the nearest harmonic of the reference, will also create what are referred to as integer boundary spurs.

The synthesizer necessarily contains digital circuitry to control the prescaler. The circuitry mostly operates at the PFD frequency. There is more circuitry active in fractional mode, hence more full switching CMOS is used and the potential for interference is greater.

The HMC700LP4(E) has been designed and tested for low spurious performance in either integer or fractional mode of operation. Reference spurious levels are typically below -100 dBc, and in-band fractional boundary spurious are typically below integrated phase noise, frequency planning can improve spurious performance in many cases.

Reference spurious levels of below -100 dBc require superb board isolation of power supplies, isolation of the VCO from the digital switching of the synthesizer, isolation of the VCO load from the synthesizer and isolation of the crystal from the VCO. Typical board layout, evaluation boards and application information are available for low spurious operation. Operation with lower levels of isolation in the application circuit board from those recommended by Hittite may result in higher spurious levels.

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Reference Input Stage

The reference input provides the path from the external reference source to the phase detector. The input stage of the reference path is shown in Figure 8. HMC700LP4(E) is a DC coupled, common emitter differential NPN buffer. Input pins have 1.8V bias on them. Expected input is full swing 3V CMOS. Slightly degraded phase noise performance may result with quasi sine or sine inputs. Input reference should have a noise floor better than -155 dBc/Hz at 50MHz to avoid degradation of the input reference path. The input reference path phase noise floor is approximately equivalent to -155 dBc/Hz. This input should be well isolated from the VCO for best spurious performance in fractional mode.

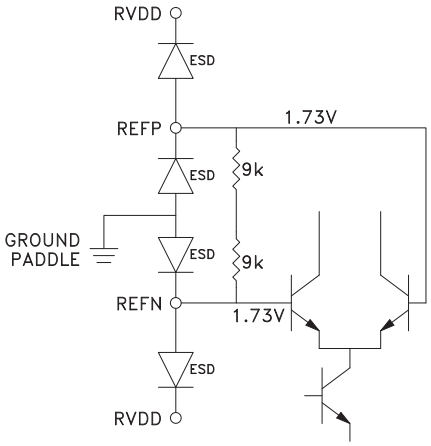

Figure 8. Reference Path Input Stage

Ref Path 'R' Divider

The reference path "R" divider is based on a 14 bit counter and can divide input signals of up to 220 MHz input by values from 1 to 16,383 and is controlled by rdiv (Table 9).

RF Input Stage

The RF input stage provides the path from the external VCO to the phase detector via the fractional divider. The RF input path is rated to operate nominally from 100 MHz to 8 GHz. The HMC700LP4(E) RF input stage is a differential common emitter stage with DC coupling, and is protected by ESD diodes as shown in Figure 9. The RF Input stage is internally matched from a single ended 50 ohm source above about 3.5 GHz, with the complimentary input grounded. If a better match is required at low frequency a simple shunt 50ohm resistor can be used external to the package.

The RF input stage has excellent sensitivity (see figure 4). Excessive drive levels can result in more coupling and spurious products in fractional mode. -10 dBm is a recommended drive level.

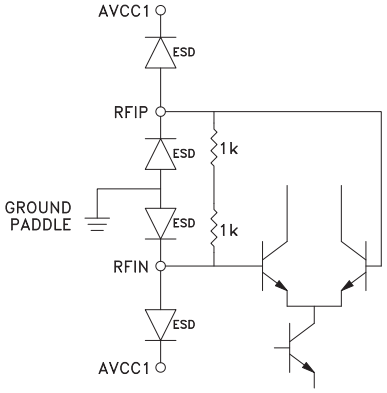

Figure 9. RF Input Stage

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RF Path 'N' Divider

The main RF path divider is capable of average divide ratios between 2^{16}-1 (65,535) and 36 in fractional mode, and 2^{16} + 31 (65,567) to 32 in integer mode.

Charge Pump and Phase Frequency Detector

The Phase Frequency Detector or PFD has two inputs, one from the reference path divider and one from the RF path divider. When in lock these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. We refer to the frequency of operation of the PFD as f_{PFD}. Most formula related to step size, delta-sigma modulation, timers etc., are functions of the operating frequency of the PFD, f_{PFD}. The PFD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians input phase difference.

PFD Test Functions

Phase detector registers are mainly used in test. *pfd_phase_sel* in Table 18 reverses the polarity of the phase detector, to allow for negative slope VCO or inverting op-amp in the loop filter.

pfd_up_en in Table 18 allows masking of the PFD up output, which effectively prevents the charge pump from pumping up.

pfd_dn_en in Table 18 allows masking of the PFD down output, which effectively prevents the charge pump from pumping down.

De-asserting both *pfd_up_en* and *pfd_dn_en* effectively tri-states the charge pump while leaving all other functions operating internally.

PFD Jitter and Lock Detect Background

In normal phase locked operation the divided VCO signal arrives at the phase detector in phase with the divided crystal signal, known as the PFD reference signal. Despite the fact that the device is in lock, the phase of the VCO signal and the PFD reference signal vary in time due to the phase noise of the reference and VCO oscillators, the loop bandwidth used and the presence of fractional modulation or not. The total integrated noise from the VCO normally dominates the variations in the two arrival times at the phase detector in integer mode.

If we wish to detect if the VCO is in lock or not we need to distinguish between normal phase jitter when in lock and phase jitter when not in lock.

First, we need to understand what is the jitter of the synthesizer, measured at the phase detector in integer or fractional modes.

The standard deviation of the arrival time of the VCO signal, or the jitter, in integer mode may be estimated with a simple approximation if we assume that the locked VCO has a constant phase noise, $\Phi^2(f_0)$, at offsets less than the loop 3 dB bandwidth and a 20 dB per decade rolloff at greater offsets. The simple locked VCO phase noise approximation is shown in Figure 10.

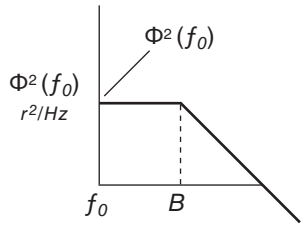

Figure 10. Synthesizer Phase Noise & Jitter

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PFD Jitter and Lock Detect Background (Continued)

With this simplification the total integrated VCO phase noise, ϕ^2, in rads^2 at the phase detector is given by

$$\phi^2 = \phi^2(f_o)B\pi/N^2 \quad \text{(EQ 1)}$$

where
B is the 3 dB corner frequency of the closed loop PLL

N is the division ratio of the prescaler

Since the simple integral of (EQ 1) is just a product of constants, we can easily do the integral in the log domain. For example if the VCO phase noise inside the loop is -100 dBc/Hz at 10 kHz offset and the loop bandwidth is 100 kHz, and the division ratio is 100, then the integrated phase noise at the phase detector, in dB, is given by:

$$\phi^2_{dB} = 10\log(\phi^2(f_0)B\pi/N^2) = -100 + 50 + 5 - 40 = 85\text{dBrads}^2$$

or equivalently, $\phi = 10^{-85/20} = 56.2$ urads = 3.22 milli-degrees rms.

While the phase noise reduces by a factor of 20logN after division to the reference, due to the increased period of the PFD reference signal, the jitter is constant.

The rms jitter from the phase noise is then given by $T_{jpn} = T_{PFD}\phi/2\pi$

In this example if the PFD reference was 50MHz, T_{PFD} = 20nsec, and hence T_{jpn} = 0.179 psec.

A normal 3 sigma peak-to-peak variation in the arrival time therefore would be $\pm 3T_{jpn} = \pm 0.759$ psec.

If the synthesizer was in fractional mode, the fractional modulation of the VCO divider will dominate the jitter. The exact standard deviation of the divided VCO signal will vary based upon the modulator type chosen, however a typical modulator will vary by about ±3 division ratios, ±4 division ratios, worst case.

If, for example a nominal VCO at 5 GHz is divided by 100 to equal the PFD reference at 50 MHz, then the worst case division ratios will vary by 100 ±4. Hence the peak variation in the arrival times caused by ΔΣ modulation of the fractional synthesizer at the reference will be

$$T_{j\Delta\Sigma pk} = \pm T_{vco} \cdot (N_{max} - N_{min})/2 \quad \text{(EQ 2)}$$

If we note that the distribution of the delta sigma modulation is approximately Gaussian, we could approximate $T_{j\Delta\Sigma pk}$ as a 3 sigma jitter, and hence we could estimate the rms jitter of the ΔΣ modulator as about 1/3 of $T_{j\Delta\Sigma pk}$ or about 266 psec in this example.

Hence the total rms jitter T_j, expected from the delta sigma modulation plus the phase noise of the VCO would be given by the rms sum, where

$$T_j = \sqrt{T_{jpn}^2 + \left(\frac{T_{j\Delta\Sigma pk}}{3}\right)^2} \quad \text{(EQ 3)}$$

In this example the jitter contribution of the phase noise calculated previously would add only 0.18psec more jitter at the reference, hence we see that the jitter at the phase detector is totally dominated by the fractional modulation.

Hence, we have to expect about ±800 psec of normal variation in the phase detector arrival times when in fractional mode. In addition, lower VCO frequencies with high PFD reference frequencies will have much larger variations. For example a 1GHz VCO operating at near the minimum nominal divider ratio of 36, would according to (EQ 2) exhibit about ±4 nsec of peak variation at the phase detector, under normal operation.

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PFD Jitter and Lock Detect Background *(Continued)*

In summary, the lock detect circuit must not interpret fractional modulation or normal phase noise related jitter as being out of lock, while at the same time declaring loss of lock when truly out of lock.

PFD Lock Detect

lkd_enable in Table 14 enables the lock detect functions of the HMC700LP4(E).

The Lock Detect circuit in the HMC700LP4(E) places a one shot window around the reference. The one shot window may be generated by either an analog one shot circuit or a digital one shot based upon an internal ring oscillator. Clearing *ringosc_oneshot_sel* (Table 14) will result in a fixed analog based nominal 10 nsec window, as shown in Figure 11. Setting *ringosc_oneshot_sel* will result in a variable length widow based upon a high frequency internal ring oscillator. The ring oscillator frequency is controlled by *ringosc_cfg*. The resulting lock detect window period is then generated by the number of ring oscillator periods defined in *oneshot_duration*, both in (Table 14).

wincnt_max in Table 14 defines the number of consecutive counts of the divided VCO that must land inside the lock detect window to declare lock. If for example we set *wincnt_max* = 1000 , then the VCO arrival would have to occur inside the ±10 nsec widow 1000 times in a row to be declared locked, which results in a Lock Detect Flag high. A single occurrence outside of the window will result in an out of lock, i.e. Lock Detect Flag low. Once low, the Lock Detect Flag will stay low until the wincnt_max =1000 condition is met again.

The Lock Detect Flag is output to LD_SDO pin according to *pfd_LD_opEn* (Table 18) or to the internal SPI read only register if *locked = 1* (Table 21). Setting *pfd_LD_opEn* will display the Lock Detect Flag on LD_SDO except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin, and returns to the Lock Detect Flag after the read is completed. Timing of the Lock Detect and Serial Data Out functions are shown in Figure 11.

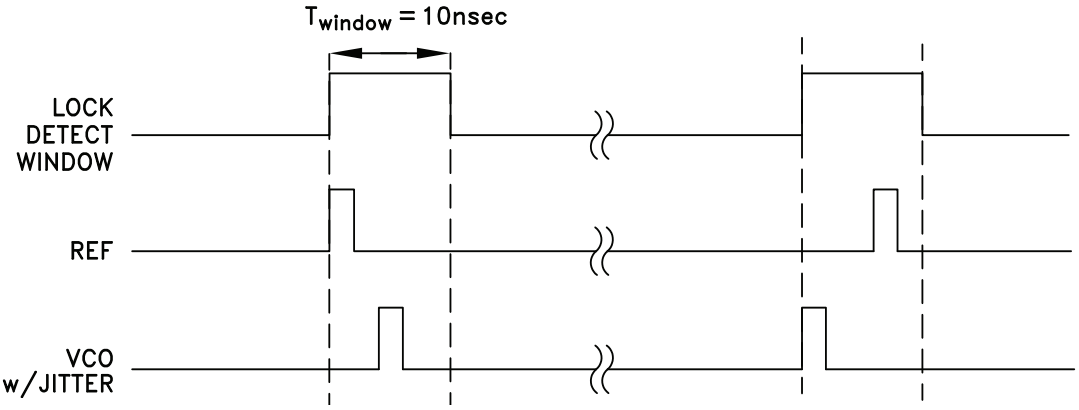

Figure 11. Normal Lock Detect Window

When operating in fractional mode the linearity of the charge pump and phase detector are much more critical than in integer mode. The phase detector linearity is worse when operated with zero phase offset. Hence in fractional mode it is necessary to offset the phase of the PFD reference and the VCO at the phase detector. In such a case, for example with an offset delay, as shown in Figure 12, the VCO arrival will always occur after the reference. The lock detect circuit can accommodate a fixed offset delay by setting *lkd_win_asym_enable and win_asym_up_sel* in Table 14. Similarly the offset can be in advance of the reference by clearing *lkd_win_asym_up_sel* while leaving *lkd_win_asym_enable* set both in Table 14. There are certain conditions, such as operating near the supply limits of the charge pump which make it advantageous to use advanced or delayed phase offset, hence both are available.

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PFD Lock Detect *(Continued)*

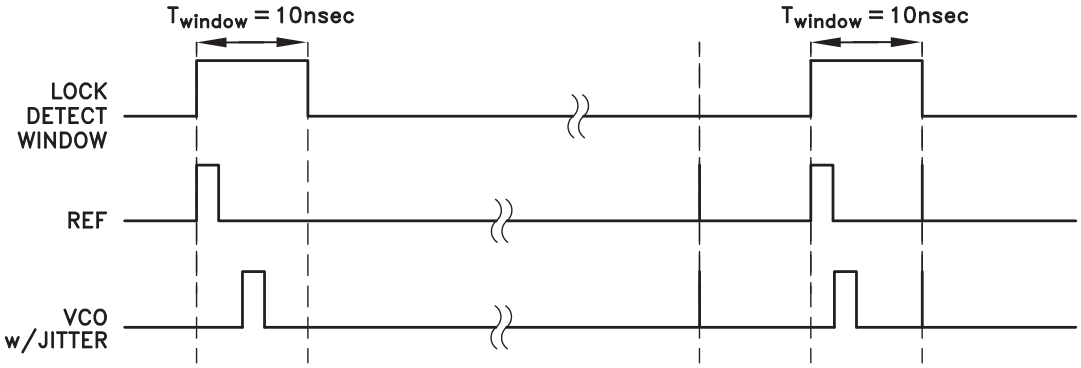

Figure 12. Delayed Lock Detect Window

Cycle Slip Prevention (CSP)

When the VCO is not yet locked to the reference, the instantaneous frequencies of the two paths are different, and the phase difference of the two paths at the PFD varies rapidly over a range much greater than ±2π radians. Since the gain of the PFD varies linearly with phase up to ±2π, the gain of a conventional PFD will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. The charge on the loop filter small cap may actually discharge slightly during the low gain portion of the cycle. This can make the VCO frequency actually reverse temporarily during locking. This phenomena is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically as shown in the red curve in Figure 13, and increases the time to lock to a value far greater than that predicted by normal small signal Laplace analysis.

The HMC700LP4(E) PFD features an ability to virtually eliminate cycle slipping during acquisition. When enabled, the Cycle Slip Prevention (CSP) feature essentially holds the PFD gain at maximum until such time as the frequency difference is near zero. Cycle Slip Prevention, allows faster lock times as shown in Figure 13. The use of the cycle slip feature is enabled with *csp_enable (see* Table 14*)* .

The Cycle Slip Prevention feature may be optimized for a given set of PLL dynamics by adjusting the PFD sensitivity to cycle slipping. This is achieved by *adjusting csp_corr_magn* in Table 13.

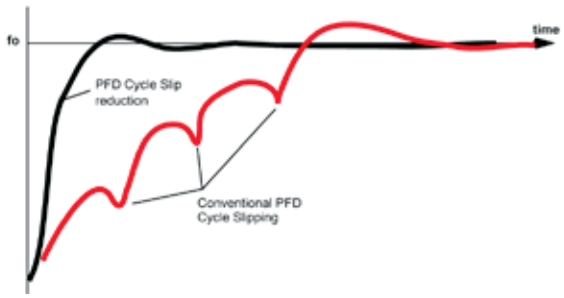

Figure 13. Cycle Slip Prevention (CSP)

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Charge Pump Gain

A simplified diagram of the charge pump is shown in Figure 14. Charge pump up and down gains are set by *cp_UPcurrent_sel* and *cpDNcurrent_sel* respectively (Table 16). Each of the UP and DN charge pumps consist of two 500uA current sources and one 1000uA current source. The current gain of the pump in radians/Amp is equal to the gain setting of this register divided by 2π. For example if both *cp_UPcurrent_sel* and *cpDNcurrent_sel* are set to '010' the output current of each pump will be 1mA and the phase detector gain Kp = 1mA/2π radians, or 159uA/rad.

Charge Pump Gain Trim

Each of the UP and DN pumps may be trimmed to more precise values to improve current source matching or to allow finer control of pump gain. The pump trim controls are 4bits, binary weighted for UP and DN, in *cp_UPtrim_sel* and *cp_DNtrim_sel* respectively (Table 16). LSB weight is 7µA, maximum trim is 105µA.

Charge Pump Phase Offset

Ideally the phase detector operates with zero offset, that is, the divided reference signal and the divided VCO signal arrive at the phase detector inputs at exactly the same time. In some modes of operation, such as fractional mode, charge pump linearity and ultimately, phase noise, is better if the VCO and reference inputs are operated with a phase offset. Normally integer mode of operation is best with no phase offset. A phase offset is implemented by adding a constant DC leakage to one of the charge pumps. DC leakage may be added to the UP or DN pumps using *chp_UPoffset_sel* or *chp_DNoffset_sel*. These are 3 bit registers with 55µA LSB. Maximum offset is 385uA.

For best spectral performance in Fractional Mode the leakage current should be programmed to: Required Leakage Current (uA) = (4E-9 + 4xTvco) x Fcomparison (Hz) x CP current (uA)

Charge Pump Operation Near the Rail

It should be noted that the charge pump is a non-ideal device. Phase locked operation with the tuning voltage very near the positive charge pump supply voltage or very near ground will degrade the phase noise performance of the synthesizer. Exactly how close to the supply limits that one should operate is a question of margin needed for the application in question and user judgement. Figure 3. gives some idea of the typical performance near the supply limits. It should be noted that if operation is necessary very near the supply limits, for example less than 500mV from the supply limit, then it is recommended to operate with a DC leakage that leaks in the direction of the supply. For example, if the charge pump supply is 5.5V and locked operation is required with a VCO tune voltage of 5.2V, then operating with UP leakage on the charge pump will improve operation in this region. Similarly if phase locked operation is needed, with a VCO tune voltage of say 300mV, then operating with DN leakage is recommended.

As an example, if the main pump gain was set at 1mA, an offset of 385uA would represent a phase offset of about (385/1000)*360 = 138degrees. Normally it is sufficient to offset the pump by just slightly larger than the delta sigma excursions for best phase noise. Best spurious operation usually occurs with DN offset with non-inverting loop filters and UP offset with inverting loop filters.

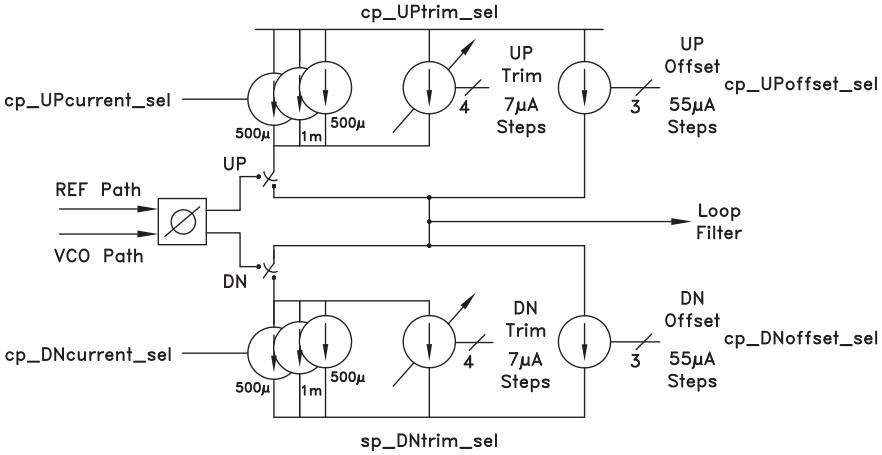

Figure 14. Charge Pump Gain & Offset Control

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Fractional Mode

Fractional Frequency Tuning

The HMC700LP4(E) synthesizer in fractional mode can achieve frequencies at fractional multiples of the reference. The output frequency of the synthesizer is given by

$$f_{vco} = \frac{f_{xtal}}{R} N_{int} + \frac{f_{xtal} \cdot N_{frac}}{R \cdot 2^{24}} = f_{int} + f_{frac} \quad \text{(EQ 4)}$$

Where	
N_{int}	is the integer division ratio, an integer number between 36 and 65,567 (see intg Table 10)
N_{frac}	is the fractional part, a number from 1 to 2^{24} see frac Table 11
R	is the reference path division ratio, see rdiv Table 9
f_{xtal}	is the frequency of the reference oscillator input
f_{PFD}	is the PFD operating frequency f_{xtal}/R
As an Example	
f_{xtal}	= 50 MHz
R	= 1
f_{PFD}	= 50 MHz
N_{int}	= 45
N_{frac}	= 1

$$f_{vco} = \frac{50e6}{1} 45 + \frac{50e6 \cdot 1}{1 \cdot 2^{24}} = 2.3GHz + 2.98Hz \quad \text{(EQ 5)}$$

In this example the output frequency of 2,300,000,002.98 Hz is achieved by programming the 10 bit binary value of 46d =2Eh = 0000 0000 0010 1110 into *intg* in Table 13.

Similarly the 24 bit binary value of the fractional word is written into *frac* in Table 11,

16,777,215d = FFF FFFh = 1111 1111 1111 1111 1111 1111

1d = 000 001h = 0000 0000 0000 0000 0000 0001

Example 2: Set the output to 4.600 025 GHz using a 100 MHz reference, R=2.

Find the nearest integer value, N_{int}, N_{int} = 92, f_{int} = 4.600 000 GHz

This leaves the fractional part to be f_{frac} =25 kHz

$$N_{frac} = \frac{2^{24} \cdot R \cdot f_{frac}}{f_{xtal}} = \frac{2^{24} \cdot 2 \cdot 25e3}{100e6} = 8389 \quad \text{(EQ 6)}$$

Since N_{frac} must be an integer number, the actual fractional frequency will be 4,600,025,001.17Hz, an error of 1.17Hz or 0.00025ppm.

Here we program the 16 bit Nint = 92d = 5Ch = 0000 0000 0101 1100 and

The 24 bit Nfrac = 8389d = 20C5h = 0000 0010 0000 1100 0101

In addition to the above frequency programming words, the fractional mode must be enabled by setting *frac_rstb* and *buff_rstb* Table 13. Other DSM configuration registers should be set to the recommended register values.

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FSK Modulation

The HMC700LP4(E) is capable of a simple binary Frequency Shift Keying (FSK) modulation. The internal modulation is unshaped FSK. The loop bandwidth of the synthesizer must be fixed by the user to achieve symbol shaping as required.

When the FSK mode of operation is enabled, via *fsk_enable* (Table 13), and SEN is held low, the synthesizer will output binary FSK frequency hops in response to data input on the SDI pin. When SEN is set, the FSK modulation will stop and return to f_0. SCK must not be toggled when transmitting data in FSK mode.

FSK modulation is normally defined by a deviation, Δf, and a modulation rate, f_m. The deviation is defined as the difference between the frequency transmitted when input data is 0, f_0, and the frequency transmitted when the input data is 1, f_1.

f_o is the frequency programmed in the frequency registers as was defined in (EQ 4), that is:

$$f_0 = \frac{f_{ref}}{R} N_{int} + \frac{f_{ref} \cdot N_{frac}}{R \cdot 2^{24}} = f_{int} + f_{frac} \quad \text{(EQ 7)}$$

f_1 is the fractional frequency achieved by adding the value in the seed register to the value in the frac register, that is:

$$f_1 = \frac{f_{ref}}{R} N_{int} + \frac{f_{ref} \cdot (N_{frac} + N_{seed})}{R \cdot 2^{24}} = f_{int} + f_{frac} + f_{seed} \quad \text{(EQ 8)}$$

Where

N_{int} is the integer division ratio, an integer number between 36 and 65,567 (see integer register)

N_{frac} is the fractional part, a number from 1 to 2^{24}

N_{seed} is the seed part, a number from 1 to 2^{24}

R is the reference path division ratio

f_{ref} is the frequency of the external reference input

In this case the deviation Δf is given simply by

$$\Delta f = f_1 - f_0 = f_{seed} \quad \text{(EQ 9)}$$

FSK data bits on SDI will be latched into the synthesizer on the falling edge of the divided reference rate, f_{PFD}. If for example R=1, and f_{ref} = 50 MHz, the input FSK data would be oversampled every 20nsec on the falling edge of the input reference.

The f_m rate of the FSK data is simply the inverse of twice the period of the data bits. For example, if the data bit period is 1msec the fm rate is 500 Hz.

If an unshaped binary FSK is desired, the closed loop bandwidth of the synthesizer should be larger than the f_m rate by a sufficient margin. For practical FSK transmissions the f_m rate is limited by the radio link budget, channel spectral emission restrictions and practical closed loop bandwidths of the fractional synthesizer.

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Integer Mode

The HMC700LP4(E) synthesizer is capable of operating in integer mode. In integer mode the synthesizer step size is fixed to that of the PFD frequency, f_{PFD}. Integer mode typically has the lower phase noise for a given PFD operating frequency, than fractional mode. The advantage is usually of the order of 4 to 6 dB. Integer mode, however, often requires a lower PFD frequency to meet step size requirements. The fractional mode advantage is that higher PFD frequencies can be used, hence lower phase noise can often be realized in fractional mode.

Integer Frequency Tuning

In integer mode the digital ΔΣ modulator is shut off and the division ratio of the prescaler is set at a fixed value. To run in integer mode clear *frac_rstb* and *buffrstb* Table 13. Then program the integer portion of the frequency as explained by (EQ 4), ignoring the fractional part.

VCO Divider Register Buffering

The VCO divider registers inside the HMC700LP4E are not double buffered. As soon as either the integer (Reg 3) or fractional (Reg 4) VCO divider register is programmed the new value takes effect. Under certain conditions, this can present a momentary mis-load of the internal VCO divider which can take several milliseconds to clear. In time sensitive frequency settling applications a specific programming sequence is required to avoid this delay. This delay arises only when the upper 11 bits of the 16 bit VCO divider (Reg 3) are all changing state such that none of the bits remain as a 1.

In time sensitive applications the following programming sequence should be used.

For Fractional Mode:

Write Register 5 = 0h (zero the Seed);
Write Register 4 = 0h (zero the Fractional divide value);
Write Register 3 to the 'intermediate' integer divide value;
Write Register 3 to the final integer divide value;
Write Register 5 = 50894Ch (or any other non-zero value);
Write Register 4 to the final fractional divide value;

For Integer Mode:

Write Register 3 to the 'intermediate' integer divide value;
Write Register 3 to the final integer divide value;

The 'intermediate' VCO Divider register value (Register 3) must have a '1' in the upper 11 bits (lower 5 bits do not matter) that does not change when going from the starting value to the intermediate value and then from the intermediate value to the final value.

A simple algorithm to calculate a suitable interim value is to 'OR' the Register 3 Start value with the Register 3 Final value. For example, if you are going from 74h to 80h the 'OR'ed value would be F4h. This behaviour is not present on other Hittite Microwave PLL devices.

Soft Reset and Power on Reset

The HMC700LP4(E) features a hardware Power on Reset (POR). All chip registers will be reset to default states approximately 250us after power up. The SPI registers may also be soft reset by an SPI write to strobe register *rst_swrst* (Table 7)

Power Down Mode

Chip Power Down is done by deasserting Chip Enable, CE, pin 23 (Low = Disabled). This will result in all analog functions and internal clocks disabled. Current consumption will typically drop below 10µA in Power Down state. During Power Down, the serial register writes will still operate, however, serial data output is disabled so Read operations will not work.

It is possible to control Power Down Mode from the serial port register *rst_chipen_from_spi* by clearing *rst_chipen_pin_select* (Table 8).

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It is also possible to leave various blocks on when in Power Down (see Table 8), including:

a. Digital Clocks
b. Internal bias reference sources
c. PFD block
d. Charge Pump Block
e. Reference Path buffer
f. VCO Path buffer
g. Digital I/O Test pads

Chip Identification

The version of the synthesizer is described in *Table 6*. Version information may be read from the synthesizer by reading the content of *chip_ID* in Reg 00h.

SERIAL PORT

Typical serial port operation can be run with SCK at speeds up to 50MHz.

Serial Port WRITE Operation

Table 4. Timing Characteristics

Parameter	Conditions	Min	Typ	Max	Units
t_1	SEN to SCK Setup Time	8			nsec
t_2	SDI to SCK Setup Time	5			nsec
t_3	SDI to SCK Setup Time	5			nsec
tsck	SCK period	20			nsec
t_4	SCK High Duration	8			nsec
t_5	SCK Low Duration	8			nsec
t_6	SEN High Duration	640			nsec
t_7	SEN Low Duration	20			nsec

A typical WRITE cycle is shown in Figure 15.

a. The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCK.
b. The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI low initiates the Write cycle (/WR).
c. Host places the six address bits on the next six falling edges of SCK, MSB first.
d. Slave registers the address bits in the next six rising edges of SCK (2-7).
e. Host places the 24 data bits on the next 24 falling edges of SCK, MSB first .
f. Slave registers the data bits on the next 24 rising edges of SCK (8-31).
g. SEN is de-asserted on the 32nd falling edge of SCK.
h. The 32nd falling edge of SCK completes the cycle.

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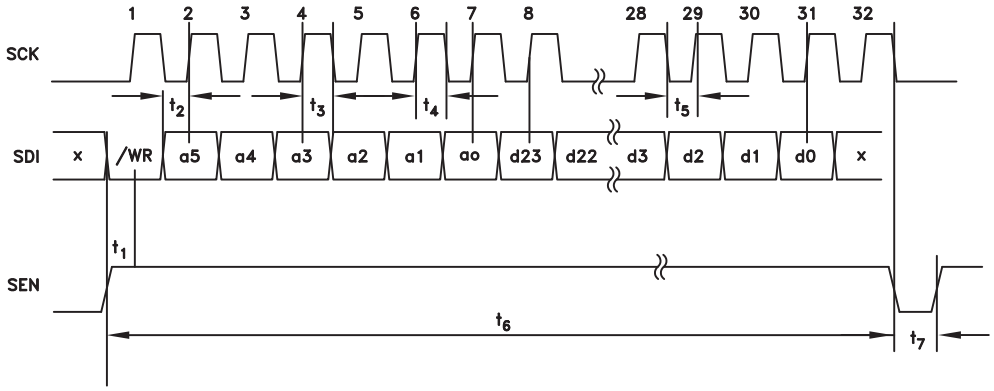

Figure 15. Serial Port Timing Diagram - Write Serial Port WRITE Operation

Serial Port READ Operation

A typical READ cycle is shown in Figure 16.

a. The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCK. Note: The Lock Detect function is multiplexed onto the LD_SDO pin. It is suggested that lock detect (LD) only be considered valid when SEN is low. In fact LD will not toggle until the first active data bit toggles on LD_SDO, and will be restored immediately after the trailing edge of the LSB of serial data out as shown in Figure 15.

b. The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI high initiates the READ cycle (RD).

c. Host places the six address bits on the next six falling edges of SCK, MSB first.

d. Slave registers the address bits on the next six rising edges of SCK (2-7).

e. Slave switches from Lock Detect and places the requested 24 data bits on SD_LDO on the next 24 rising edges of SCK (8-31), MSB first .

f. Host registers the data bits on the next 24 falling edges of SCK (8-31).

g. Slave restores Lock Detect on the 32nd rising edge of SCK.

h. SEN is de-asserted on the 32nd falling edge of SCK.

i. The 32nd falling edge of SCK completes the READ cycle.

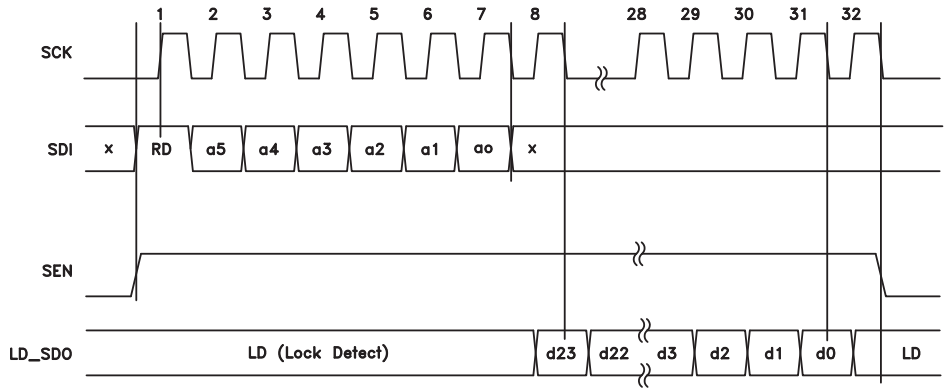

Figure 16. Serial Port Timing Diagram - READ Serial Port Operation

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General Purpose Output (GPO) Pins

The HMC700LP4(E) also supports a simple two pin GPO bus implemented on pins D1 and D0. GPO operation requires that GPO output pads be enabled via *gpio_pads_en* (Table 15). Two bit arbitrary data may be written to the GPO outputs via register *gpo_test*, when *gpo_select* is first set to 10d (Table 20). Other test waveforms, described in Table 20, may be output to the GPO pins according to the value written to *gpo_select*. If the GPO outputs are not used, and it is desirable that they are as quiet as possible then the GPO pads should be disabled via *gpio_pads_en* (Table 15) and *gpo_select* set to a value that has a static source, such as 10d.

Register Map

Note: For Read Operations from register 00h, it is Read Only containing the chip ID. Current Hittite synthesizer chip IDs are shown in Table 6.

Table 6. Reg00h ID (Read Only) Register

Bit	Name	Width	Default	Description
[23:0]	chip_ID	24	478708h or 485901	Part Number, Description HMC700LP4, 16-Bit 5.5V

For write operations to register 00h, it is a Write Only strobe register as defined in Table 7.

Table 7. Reg00h RST Strobe Register

Bit	Name	Width	Default	Description
[0]	rst_swrst	1	n/a	Strobe (WRITE ONLY) generates soft reset. Resets all digital and registers to default states.

Table 8. Reg 01h RST Register

Bit	Name	Width	Default	Description
[0]	rst_chipen_pin_select	1	1	1 = Chip enable via CE pin, CE (Pin 23) enables chip. CE low puts chip in power down. 0 = Chip enable via SPI (rst_chipen_from_spi), CE Pin is ignored
[1]	rst_chipen_from_spi	1	0	1= Chip Enable when rst_chipen_pin_select = 0 0= Power Down when rst_chipen_pin_select = 0 see Power Down Mode description and csp_enable Reg07 <20> If rst_chipen_pin_select =1 this register is ignored
[2]	rst_chipen_digclks_keep_on	1	0	keeps digital clocks on when chip is Power Down from any source
[3]	rst_chipen_bias_keep_on	1	0	keeps chip internal bias generators on when chip is Power Down from any source
[4]	rst_chipen_pfd_keep_on	1	0	keeps internal PFD block on when chip is Power Down from any source
[5]	rst_chipen_chp_keep_on	1	0	keeps internal Charge Pump block on when chip is Power Down from any source
[6]	rst_chipen_refbuf_keep_on	1	0	keeps reference path buffer on when chip is Power Down from any source
[7]	rst_chipen_vcobuf_keep_on	1	0	keeps VCO path RF buffer on when chip is Power Down from any source
[8]	rst_chipen_dig_io_keep_on	1	0	keeps digital IO pins on when chip is Power Down from any source
[9]	rst_chipen_rdiv_fe_sync	1	0	Tri-states the PFD on the next falling edge of the ref clock and also puts the chip to sleep

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Table 9. Reg 02h REFDIV Register

Bit	Name	Width	Default	Description
[13:0]	rdiv	14	1	Reference Divider 'R' Value (EQ 4) 00h - illegal 01h - divide-by-1 (bypass) 10h - divide-by-2 11h - divide-by-3 etc ... 3FFFh - divide-by-16, 383 The reference divider is controlled by several bits in register 8. See register 8 description for details.

Table 10. Reg 03h Frequency Register - Integer Part

Bit	Name	Width	Default	Description	
[15:0]	intg	16	C8h	VCO Divider Integer part, used in all modes, see (EQ 4)	
				Fractional Mode min 36d max 2^16 -1 = 65,535d	**Integer Mode** min 32d max 2^16+31 = 65,567d

Table 11. Reg 04h Frequency - Fractional Part Register

Bit	Name	Width	Default	Description	
[23:0]	frac	24	0	VCO Divider Fractional part (24 bit unsigned) see section Fractional Frequency Tuning	
				Used in Fractional Mode only **min 0d** **max 2^24-1**	

Table 12. Reg 05h SD Seed Register

Bit	Name	Width	Default	Description
[23:0]	seed	24	0	**Fractional Mode**: Seeds fractional modulator **FSK Mode**: Sets f1 in FSK mode when fsk_enable=1 (see section FSK Modulation)

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Table 13. Reg 06h SD CFG Register

Bit	Name	Width	Default	Description
[7:0]	reserved		87h	
[9:8]	order	2	2h	Select the Modulator Type 0 - not used 1 - not used 2 - Type B 3 - Type A
[10]	frac_rstb	1	1	0 holds the frac core in reset reset is used for integer mode or integer mode with CSP
[11]	buff_rstb	1	1	0 holds the frac core buffers in reset reset is used with frac_rstb=0 for integer mode, no CSP
[12]	bypass_mode	1	0	1 fractional modulator output is ignored, but fractional modulator continues to be clocked, used to test the isolation of the digital fractional modulator from the VCO output in integer mode
[13]	autoseed_mode	1	1	loads the seed whenever the frac register is written
[14]	reserved	1	0	Must be kept at 0
[15]	fsk_enable	1	0	enables the FSK mode of operation and FSK input on SDI pin, (see section FSK Modulation)
[16]	reserved	1	0	
[17]	clkrq_refdiv_sel	1	0	selects the SD clock source 1 = reference divider clock 0 = VCO divider clock (recommended)
[18]	clkrq_invert_clk	1	1	inverts the selected sd clock
[19]	sd_spare_out	1	0	spare
[23:20]	csp_corr_magn	4	8h	CSP magnitude correction (see section Cycle Slip Prevention (CSP)) 0000 low magnitude 1111 high magnitude sign of the correction is determined automatically by the CSP state machine

Note: To Enable Frac Mode:

Set Reg 6 [12:10]= 011

Also, Reg 9[9:7] or Reg 9[4:2] must be adjusted to mitigate spurs in frac mode (Dn or Up Leakage)

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Table 14. Reg 07h LKD/CSP Register

Bit	Name	Width	Default	Description
[9:0]	wincnt_max	10	250	lock detect window sets the number of consecutive counts of divided VCO that must land inside the Lock Detect Window to declare LOCK
[10]	lkd_enable	1	1	enables internal lock detect function, Note output to Lock Detect Flag on *LD_SDO* as per Figure 13 controlled by *pfd_LD_opEn*, *Reg 0Bh PFD* Register
[11]	lkd_winasym_enable	1	0	asymmetrical window enables lock detect window to only lag or only lead the divided reference signal at the PFD, see Figure 9
[12]	lkd_win_asym_up_sel	1	0	1 selects lead window when lkd_winasym_enable=1 0 selects lag window when lkd_winasym_enable=1
[13]	ringosc_oneshot_sel	1	0	1 ring osc based one shot for lock detection mode 0 nominal 20nsec analog one shot for lock detection mode
[16:14]	oneshot_duration	3	0	duration of the ringosc based oneshot pulse in lock detection mode
[18:17]	ringosc_cfg	2	0	Lock Detect ringosc frequency trim “00” fastest “11” slowest
[19]	ringosc_mode	1	0	force ringosc ON
[20]	csp_enable	1	1	cycle slip prevention (CSP) enable

See section PFD Lock Detect for more information about this register.

Table 15. Reg 08h Analog EN Register

Bit	Name	Width	Default	Description
[0]	bias_en	1	1	enables main chip bias reference
[1]	cp_en	1	1	charge pump enable
[2]	pfd_en	1	1	pfd enable
[3]	refbuf_en		1	reference path buffer enable. Set to 1 for normal operation.
[4]	vcobuf_en	1	1	vco path RF buffer enable
[5]	gpio_pads_en	1	1	gpio pads enable, Pins D0 and D1 required for use of GPO port or VCO Serial Port
[6]	sdo_pad_en	1	1	LD_SDO pad driver enable (Pin 5) required for use of Lock Detect, Serial Port Read Operation or VCO Serial Port operation
[7]	vcodiv_digclk_en	1	1	vco divider output clk to digital enable
[8]	vcodiv_en	1	1	enable vco divider
[9]	reserved	1	0	
[10]	vcodiv_dutycyc_mode	1	0	vcodiv duty cycle mode stretches the VCO divider output when N>32
[11]	reserved	1	0	Set to 0 for normal operation
[12]	rdiv_ref_to_dig_en	1	1	reference input applied to digital when set to 1, non-divided reference signal is fed to digital (required for normal operation)
[13]	rdiv_refdiv_to_dig_en	1	1	reference divider applied to digital, when set to 1, divided reference signal is fed to digital (required for normal operation)

Charge Pump control register. see Figure 14

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Table 16. Reg 09h CP Register

Bit	Name	Width	Default	Description
[1:0]	Reserved set them to 0	2	0	
[4:2]	cp_UPoffset_sel	3	0	Charge Pump UP Offset Control 55uA/step 000 = 0uA 001 = 55uA 010 = 110uA ... 111 = 385uA
[6:5]	Reserved Set them to 0	2	0	
[9:7]	cp_DNoffset_sel	3	0	Charge Pump DN Offset Control 55uA/step 000 = 0uA 001 = 55uA 010 = 110uA ... 111 = 385uA
[13:10]	cfg cp_UPtrim_sel	4	0	Charge Pump UP Current Trim 7uA/step 0000 = 0uA 0001 = 7uA 0010 = 14uA 0100 = 28uA 1000 = 56uA 1111 = 105uA
[17:14]	cp_DNtrim_sel	4	0	Charge Pump DN Current Trim 7uA/step 0000 = 0uA 0001 = 7uA 0010 = 14uA 0100 = 28uA 1000 = 56uA 1111 = 105uA
[20:18]	cp_UPcurrent_sel	3	0	Charge Pump UP MAIN Current Control 500uA step 000 tristate if PFD also disabled 001 500uA 010 1000uA 011 1500uA 100 2000uA 101 2000uA 110 2000uA 111 2000uA
[23:21]	cp_DNcurrent_sel	3	0	Charge Pump UP MAIN Current Control 500uA step 000 tristate if PFD also disabled 001 500uA 010 1000uA 011 1500uA 100 2000uA 101 2000uA 110 2000uA 111 2000uA

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Table 17. Reg 0Ah CP Op Amp Register

Bit	Name	Width	Default	Description
[1:0]	cp_opamp_bias_sel	2	0	Charge Pump Internal Op-Amp bias select 00 - 540 µA 01 - 689 µA 10 - 943 µA 11 - 1503 µA Enabled with Chg Pump enable Note: this circuit affects internal charge pump operation and linearity. Default setting is recommended. Enabled with Reg08h[1] cp_en

Table 18. Reg 0Bh PFD Register

Bit	Name	Width	Default	Description
[2:0]	pfd_del_sel	3	0	sets PFD reset path delay. Recommended value 010 When in Integer mode, Reg B Bits [2:0] should not be 000 because it doesn't ensure sufficient 'on' time for the CP at 50MHz. This isn't an issue in Fractional Mode;
[3]	pfd_phase_sel	1	0	Swaps the PFD inputs 1 negative VCO tuning slope 0 positive VCO tuning slope
[4]	pfd_up_en	1	1	enables the PFD UP output according to state of pfd_mute_when_locked_enable, see *Reg0B<9>*
[5]	pfd_dn_en	1	1	enables the PFD DN output according to state of pfd_mute_when_locked_enable, see *Reg0B<9>*
[6]	pfd_LD_opEn	1	1	pfd Lock Detect Output Enable, enables Lock Detect flag output to LD_SDO pin
[7]	pfd_pullup_ctrl	1	0	Forces PFD UP output on
[8]	pfd_puldn_ctrl	1	0	Forces PFD DN output on
[9]	pfd_mute_when_locked_ enable	1	0	1: if set: when locked disables UP if pfd_up_en=0 when locked disables DN if pfd_dn_en=0 when NOT locked, allows both UP and DN to be active and ignores pdf_up_en and pfd_dn_en 0: if clear, pfd_dn_en and pfd_up_en enable UP and DN outputs at all times
[10]	spare0	1	0	reserved
[11]	spare1	1	1	reserved

Table 19. Reg 0Ch VCO SPI Register

Bit	Name	Width	Default	Description
[9:0]	vcospi_vco_data	10	0	data register contents, when written automatically outputs this data via VCO SPI when to_gpo_sdo=1 *Reg09<7>*

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Table 20. Reg 0Dh GPO_SPI_RDIV Register

Bit	Name	Width	Default	Description
[3:0]	gpo_select	4	10d	Test signals selected here are output to gpo pins when *gpo_pads_en=1* (Table 15) D1 & D0 0: clk_vcodiv & clk_refdiv 1: pfd_up & pfd_dn 2: refOut & refDivOut 3: seed_stb_sypulse_test & frac_stb_sypulse_test 4: intg_inbuff_enable_test & clk_sd 5: oneshot_trigg_test & oneshot_pulse_test 6: '0' & ringosc_test 7: csp_corr_add & csp_corr_sub 8: pfd_sat_refdiv & pfd_sat_vcodiv 9: (csp_corr_add or csp_corr_sub) & pfd_sat_rstb 10: gpo_test , see Reg0D<5:4> 11: not used 12: not used 13: not used 14: not used 15: not used
[5:4]	gpo_test	2	0	data written to this register is output to D0 and D1 pins when gpo_select = 10d
[6]	refclkdiv4	1	0	1: sel ref divby4 for clocking the vco_spi 0: sel ref divby1 for clocking the vco_spi
[7]	to_gpo_sdo	1	0	enable the automatic output of vcospi_vco_data to LD_SDO Output VCO_SPI clock to D1 (see *Reg0D<6>*) Output VCO_SPI EN to D0

Table 21. Reg 0Fh LD State Register (Read Only)

Bit	Name	Width	Default	Description
[0]	locked	1	0	Read only Lock Detect flag, 1 when locked

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v11.0411

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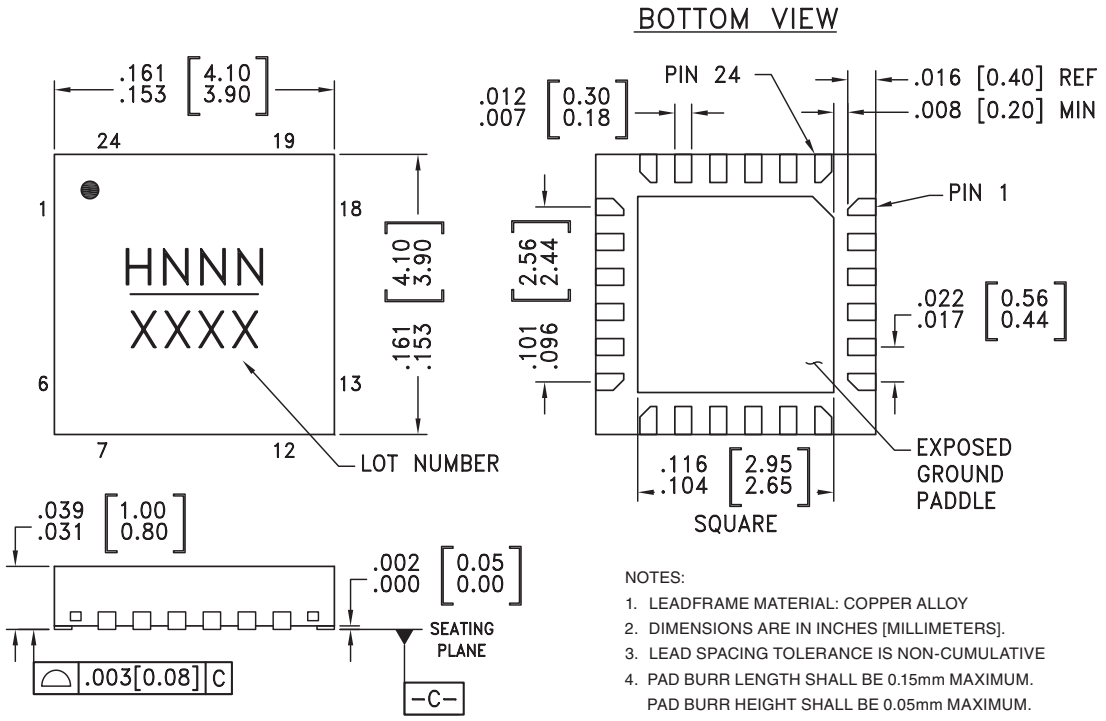
Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC700LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H700 XXXX
HMC700LP4(E)	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H700 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Evaluation PCB

Please reference HMC700LP4 Product Note for information on Evaluation PCB kit and List of Materials.

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