ANALOG DEVICES

HMC713MS8 / 713MS8E

v06.0412

RoHS EARTH FRIENDLY

54 dB, LOGARITHMIC DETECTOR / CONTROLLER, 45 - 2700 MHz

Typical Applications

The HMC713MS8(E) is ideal for:

- Cellular Infrastructure
- WiMAX, WiBro & LTE/4G
- Power Monitoring & Control Circuitry
- Receiver Signal Strength Indication (RSSI)
- Automatic Gain & Power Control
- Military, ECM & Radar

Features

Wide Dynamic Range: up to 54 dB

High Accuracy:
±1 dB with 54 dB Range Up To 2.7 GHz

Fast Output Response Time

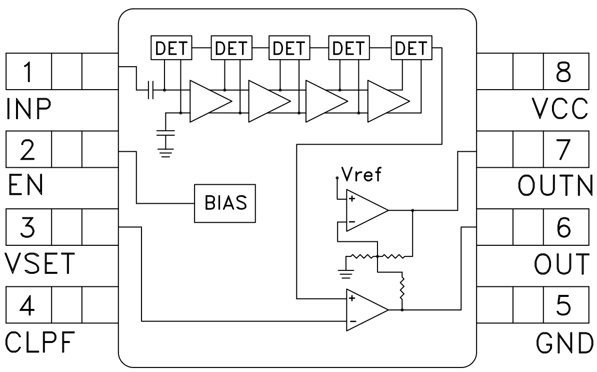
Supply Voltage: +2.7 to +5.5V

Power-Down Mode

Excellent Stability over Temperature

MSOP-8 SMT Package: 14.8 mm²

Functional Diagram



General Description

The HMC713MS8(E) Logarithmic Detector/Controller is ideal for converting RF signals with frequencies in the 45 MHz to 2700 MHz range, to a proportional DC voltage at its output. The HMC713MS8(E) employs a successive compression technology which delivers 54 dB of dynamic range with high conversion accuracy over a wide input frequency range. As the input signal is increased, successive amplifiers move into saturation one by one creating an accurate approximation of the logarithm function. The outputs of a series of detectors are summed, converted into voltage domain and buffered to drive the OUT output. For detection mode, the OUT pin is connected to the VSET input and will provide a nominal logarithmic slope of 17 mV/dB and an intercept of -68 dBm. The HMC713MS8(E) can also be used in the controller mode where an external voltage is applied to the VSET pin to create an AGC or APC feedback loop.

Electrical Specifications, T_A = +25 °C, Vcc= +3V [1]

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	45	100	900	1900	2200	2700	MHz
±3 dB Dynamic Range	60	61	61	62	62	68	dB
±3 dB Dynamic Range Center	-26	-28	-28	-30	-31	-27	dBm
±1 dB Dynamic Range	53	54	54	54	53	59	dB
OUT Slope	17.3	17.3	17.2	17.1	17.1	17.2	mV/dB
OUT Intercept	-68	-68	-69	-71	-72	-70	dBm
Variation of OUT with Temperature from -40°C to +85°C @ -20 dBm Input	-0.8	-1	-0.9	-0.5	-0.6	-0.5	dB

[1] Detector mode measurements; OUT (Pin 6) is shorted to VSET (Pin 3) through an RC network.

Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Down (EN) Interface					
Voltage Range for Normal Mode		0.8 x Vcc			V
Voltage Range for Powerdown Mode				0.2 x Vcc	V
Threshold Voltage			Vcc/2		V
Power Supply (Vcc)					
Operating Voltage Range			2.7 - 5.5		V
Supply Current in Normal Mode			17		mA
Supply Current in Power Down Mode			0.3		mA
OUT Interface					
Rise Time	CLPF= 0, No Power to -10 dBm, 10% - 90%		24		ns
Fall Time	CLPF= 0, -10 dBm to No Power, 90% - 10%		70		ns
Output Video BW	3 dB reduction in demodulated output voltage		16		MHz
Voltage Range	Closed Loop (Eval Board Setup)		0.2 - 1.2		V
Voltage Range	Open Loop		0.1 to (Vcc -0.1)		V
Current Drive Source / Sink			3.5 / 0.51		mA
OUTN Interface					
Current Drive Source / Sink			3.6 / 0.47		mA
OUTN Interface					
Output Voltage Range			0.2 - 2.1		V
RF Input					
Input Return Loss (S11)	F= 50 MHz to 2.5 GHz Z_0= 50Ω, See plot		10		dB
VSET Interface					
Input Impedance			1		MΩ
Input Voltage Range	Eval Board		0.2 - 1.2		V
Low Frequency Gain	VSET to OUT		64		dB
Open Loop Corner Frequency			11		kHz

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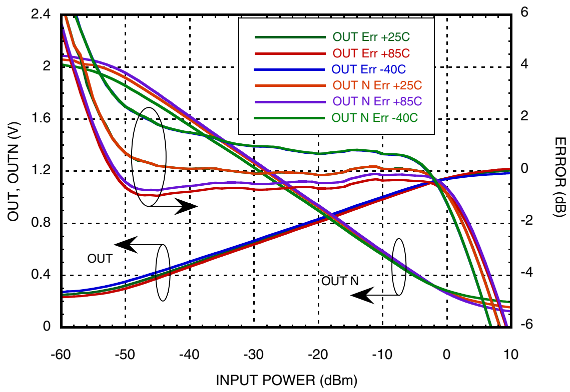
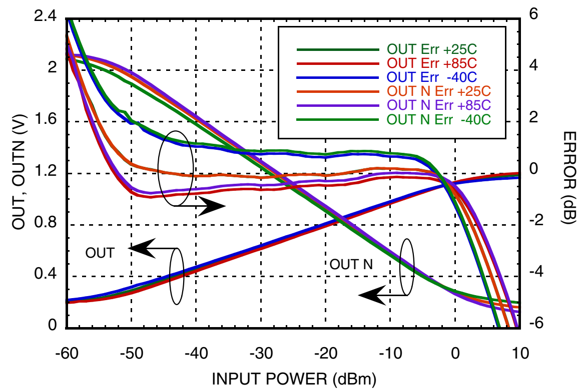
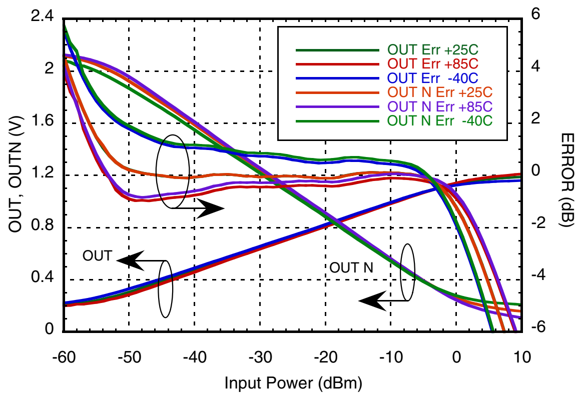
Output Voltage & Error vs. Input Power, Fin = 45 MHz



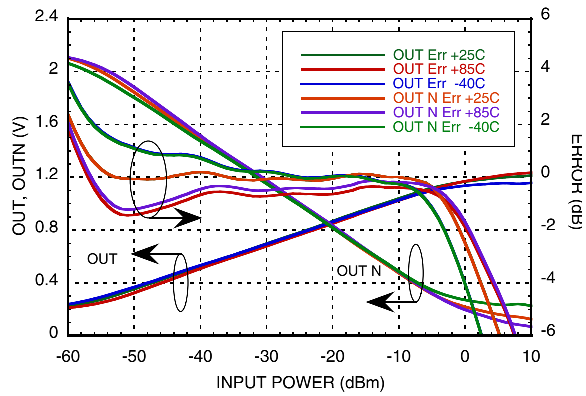
Output Voltage & Error vs. Input Power, Fin = 100 MHz



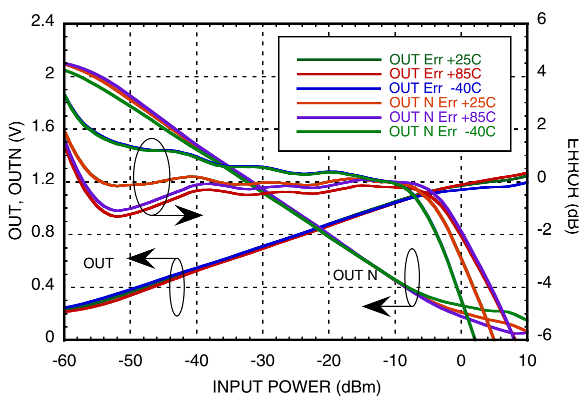
Output Voltage & Error vs. Input Power, Fin = 900 MHz



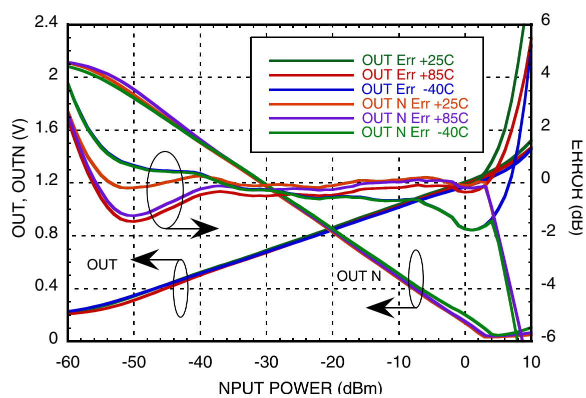
Output Voltage & Error vs. Input Power, Fin = 1900 MHz



Output Voltage & Error vs. Input Power, Fin = 2200 MHz

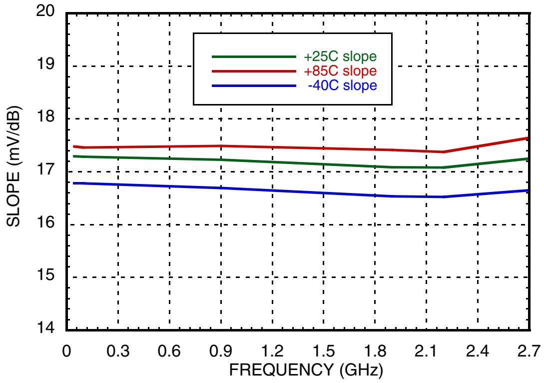


Output Voltage & Error vs. Input Power, Fin = 2700 MHz

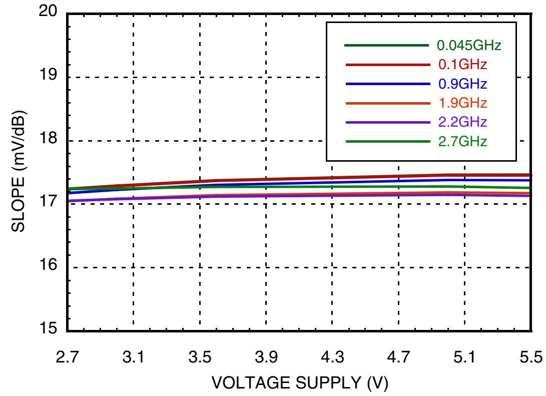


Unless otherwise noted: Vcc= +3V, T_A = +25 °C

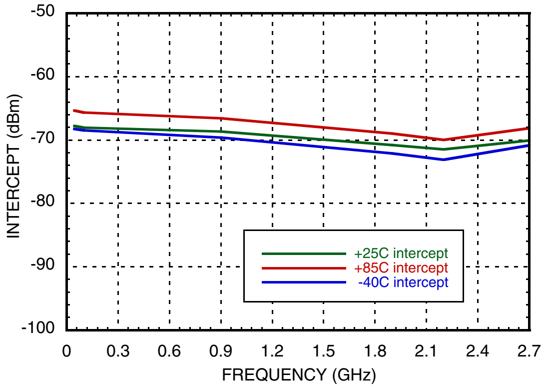
OUT Slope vs. Frequency



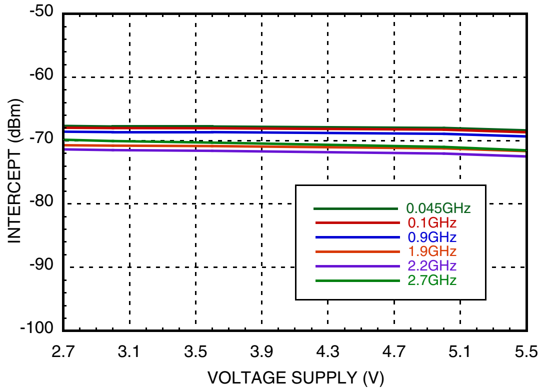
OUT Slope vs. Supply Voltage



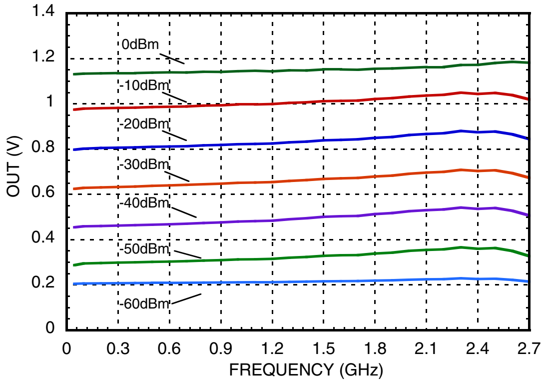
OUT Intercept vs. Frequency



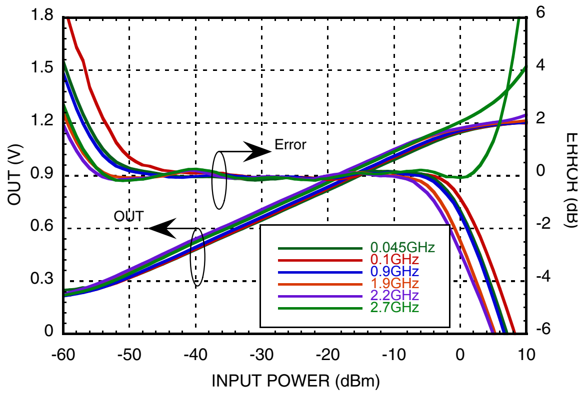
OUT Intercept vs. Supply Voltage



OUT vs. Frequency & Input Power



OUT Voltage & Error vs. Frequency



Unless otherwise noted: Vcc= +3V, T_A = +25 °C

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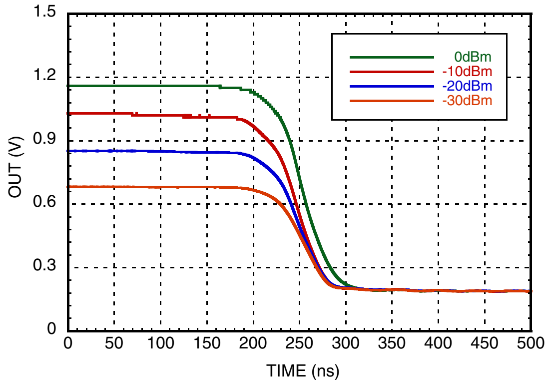
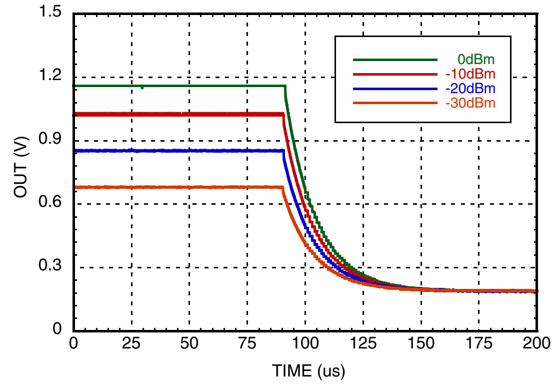
54 DB, LOGARITHMIC DETECTOR / CONTROLLER, 45 - 2700 MHz

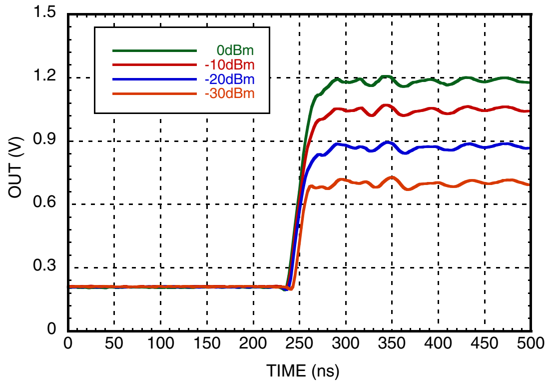
Output Response
Fall Time @ 900 MHz, C1 = Open



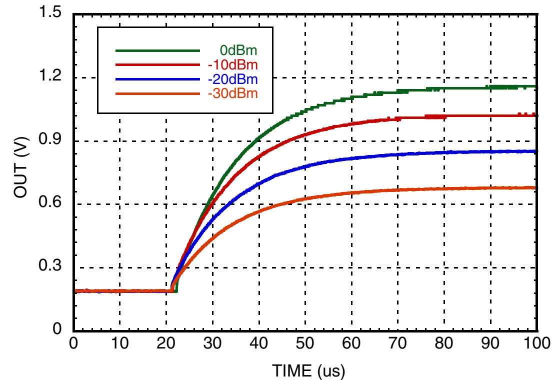
Output Response
Fall Time @ 900 MHz, C1 = 10nF



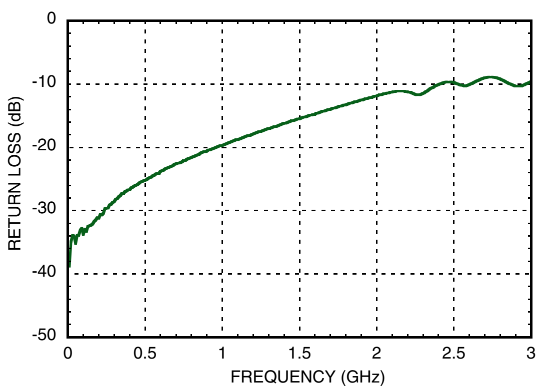
Output Response
Rise Time @ 900 MHz, C1 = Open



Output Response
Rise Time @ 900 MHz, C1 = 10nF



Input Return Loss



Unless otherwise noted: Vcc= +3V, T_A = +25 °C

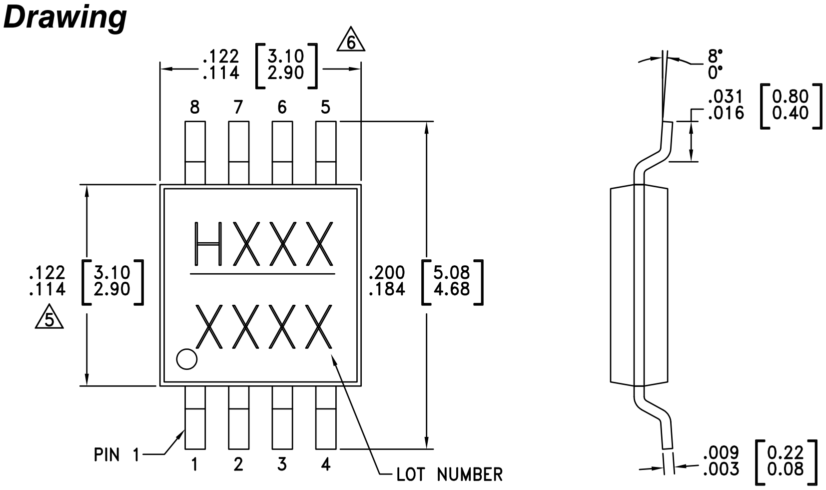
54 DB, LOGARITHMIC DETECTOR / CONTROLLER, 45 - 2700 MHz

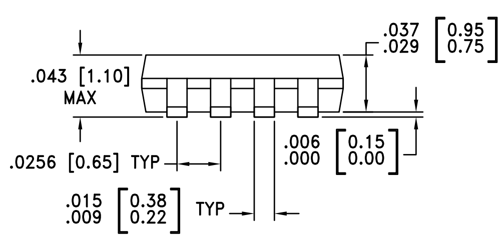
Absolute Maximum Ratings

Vcc	0 to +5.6V
EN	0 to +5.6V
VSET	0 to +5.6V
OUT Output Current	5 mA
OUTN Output Current	5 mA
RF Input Power	12 dBm
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 5.43 mW/°C above 85°C)	0.22 Watts
Thermal Resistance (R_{th}) (junction to lead)	184 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing





NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD MATERIAL: COPPER ALLOY
3. LEAD PLATING: 100% MATTE TIN
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
7. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

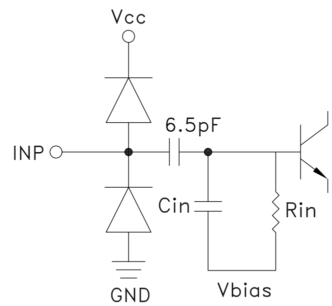
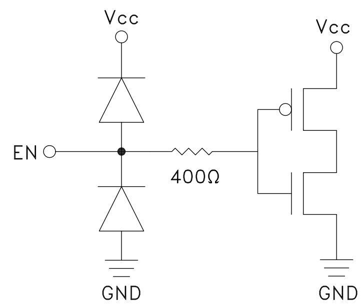
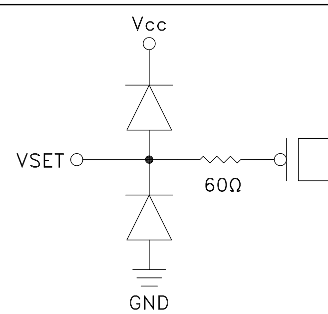
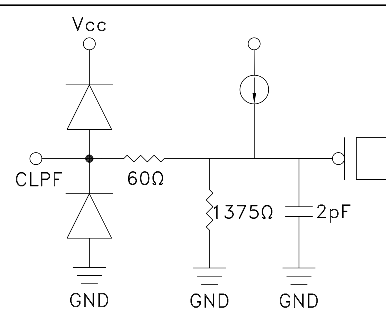
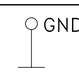
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC713MS8	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H713 XXXX
HMC713MS8E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H713 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

54 DB, LOGARITHMIC DETECTOR / CONTROLLER, 45 - 2700 MHz

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	INP	RF input pin.	
2	EN	Enable pin. Apply VEN >0.8 x Vcc for normal operation. Apply VEN <0.2xVcc to disable the HMC713MS8E and reduce supply current to 0.3mA. To ensure proper start-up apply the power-up sequence shown in the “Power-Up Timing Diagram” attached to the application circuit.	
3	VSET	Set point input for controller mode. Connect to OUT with the resistor network shown in evaluation board drawing for detector mode.	
4	CLPF	Connection for ground referenced external lowpass filter capacitor.	
5	GND	Device ground.	

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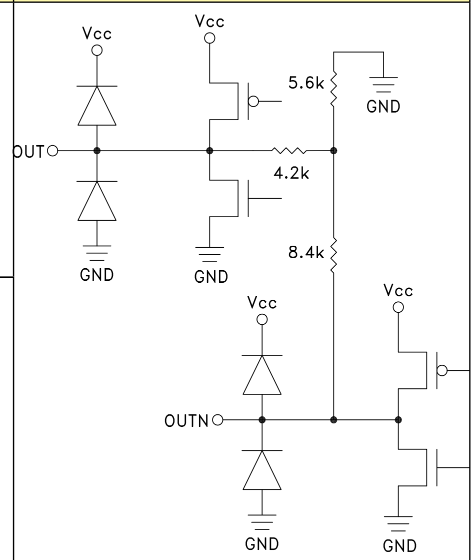
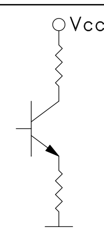
Pin Descriptions (Continued)

<table>
<tr><th>Pin Number</th><th>Function</th><th>Description</th><th>Interface Schematic</th></tr>
<tr><td>6</td><td>OUT</td><td>Logarithmic output that converts the input power to a DC level in controller mode. Output voltage increases with increasing amplitude</td><td rowspan="2">
</td></tr>
<tr><td>7</td><td>OUTN</td><td>Inverted logarithmic output.
OUTN= 2.55 - 2 x OUT</td></tr>
<tr><td>8</td><td>Vcc</td><td>Bias Supply.
Connect supply voltage to all this pin with appropriate filtering.</td><td>
</td></tr>
</table>

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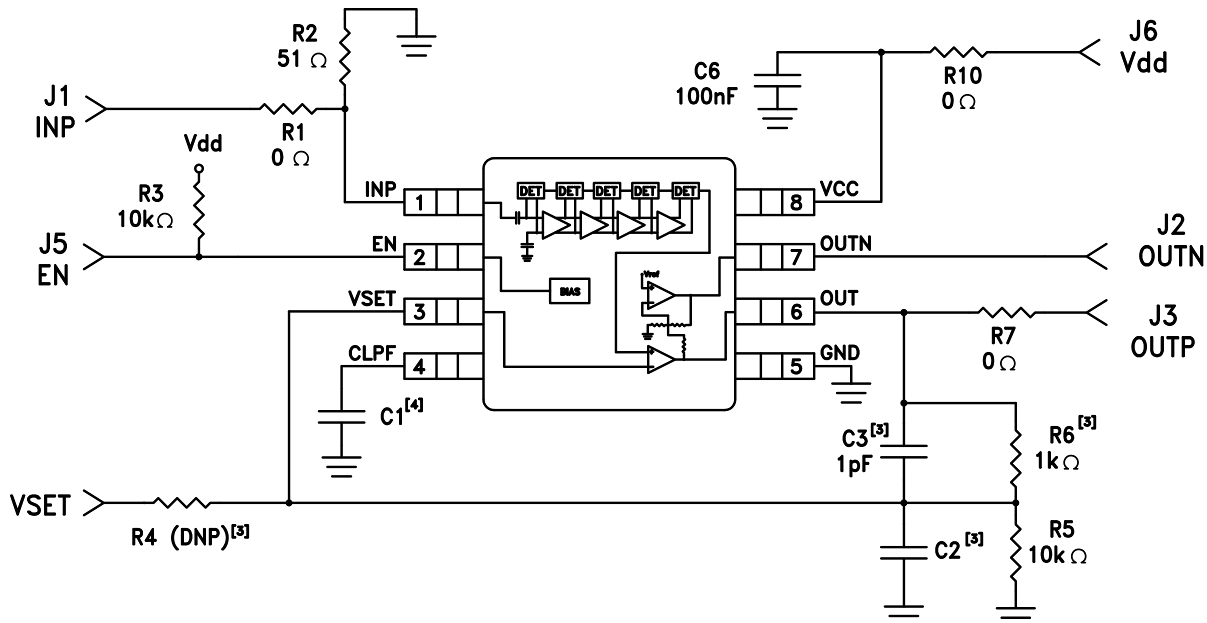
Application & Evaluation PCB Schematic



Notes

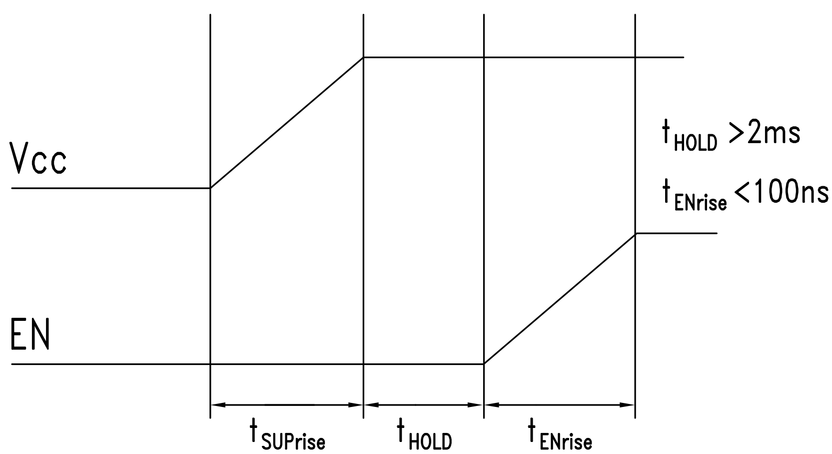
Note 1: The HMC713MS8(E) evaluation board is pre-assembled for single-ended input, and detector/RSSI mode.

Note 2: For detector mode, connect high impedance volt meter to the OUT / OUTN port.

Note 3: For controller mode, remove R6 & C3 and install 1k Ω resistor (R4) and 100pF capacitor (C2), then make appropriate connection to OUT and VSET. In controller mode, the OUT / OUTN output can be used to drive a variable gain amplifier, or a variable attenuator, either directly or through a buffer or microcontroller. VSET should be connected to an external supply, typically between +0.2 and +1.2V.

Note 4: An external capacitance C1 can be connected to CLPF port for additional filtering of OUT and OUTN outputs..

Power-Up Timing Diagram



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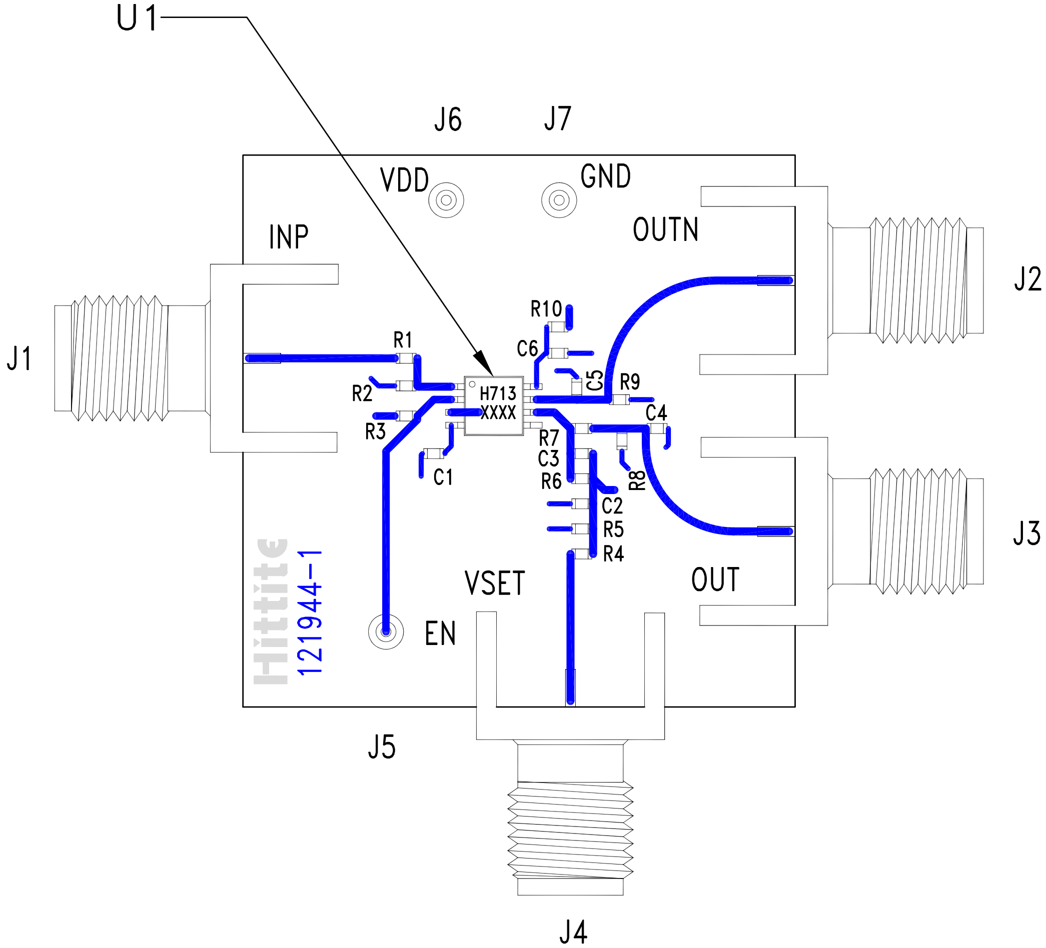
54 DB, LOGARITHMIC DETECTOR / CONTROLLER, 45 - 2700 MHz

Evaluation PCB



List of Materials for Evaluation PCB 121947 [1]

Item	Description
J1 - J3	PC Mount SMA Connector
J5 - J7	DC Pin
C3	1 pF Capacitor, 0402 Pkg.
C6	0.1 µF Capacitor, 0402 Pkg.
R1, R7, R10	0Ω Resistor, 0402 Pkg.
R2	51Ω Resistor, 0402 Pkg.
R3, R5	10k Resistor, 0402 Pkg.
R6	1k Resistor, 0402 Pkg.
U1	HMC713MS8(E) Logarithmic Detector / Controller
PCB [2]	121944 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.