

GaAs pHEMT MMIC LOW NOISE AMPLIFIER, 5 - 10 GHz



Typical Applications

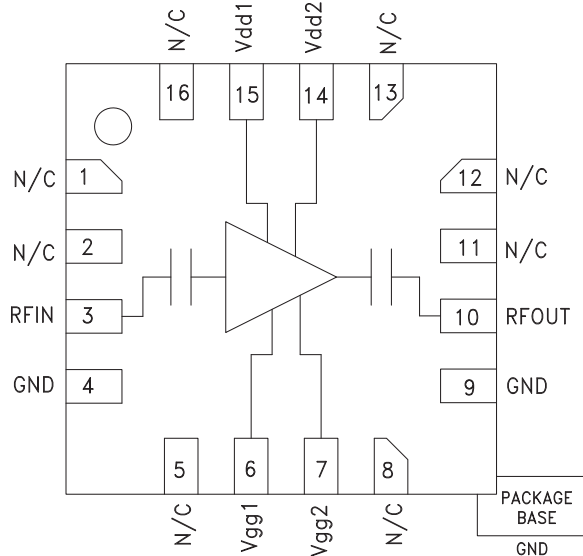
This HMC902LP3E is ideal for:

- Point-to-Point Radios
- Point-to-Multi-Point Radios
- Military & Space
- Test Instrumentation

Features

- Low Noise Figure: 1.8 dB
- High Gain: 19 dB
- High P1dB Output Power: 16 dBm
- Single Supply: +3.5 V @ 80 mA
- Output IP3: +28 dBm
- 50 Ohm matched Input/Output
- 16 Lead 3x3mm SMT Package: 9mm²

Functional Diagram



General Description

The HMC902LP3E is a GaAs MMIC Low Noise Amplifier housed in a leadless 3x3 mm plastic surface mount package. The amplifier operates between 5 and 10 GHz, providing 19 dB of small signal gain, 1.8 dB noise figure, and output IP3 of +28 dBm, while requiring only 80 mA from a +3.5V supply. The P1dB output power of +16 dBm enables the LNA to function as a LO driver for balanced, I/Q or image reject mixers. The HMC902LP3E also features I/Os that are DC blocked and internally matched to 50 Ohms, making it ideal for high capacity microwave radios and C-Band VSAT applications.

Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{dd1} = V_{dd2} = +3.5\text{V}$, $I_{dd} = 80\text{ mA}$ [2]

| Parameter | Min. | Typ. | Max. | Units |
|--|------|--------|------|---------|
| Frequency Range | | 5 - 10 | | GHz |
| Gain [1] | 17 | 19.5 | | dB |
| Gain Variation over Temperature | | 0.01 | | dB / °C |
| Noise Figure [1] | | 1.8 | 2.2 | dB |
| Input Return Loss | | 12 | | dB |
| Output Return Loss | | 15 | | dB |
| Output Power for 1 dB Compression [1] | | 16 | | dBm |
| Saturated Output Power (P _{sat}) [1] | | 17.5 | | dBm |
| Output Third Order Intercept (IP3) | | 28 | | dBm |
| Supply Current (I _{dd}) (V _{dd} = 3.5V, set V _{gg2} = 0V, V _{gg1} = 0V Typ.) | | 80 | 110 | mA |

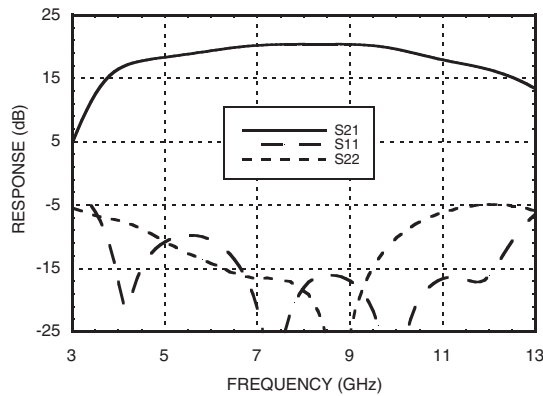
[1] Board loss removed from gain, power and noise figure measurement.

[2] V_{gg1} = V_{gg2} = open for normal, self-biased operation.

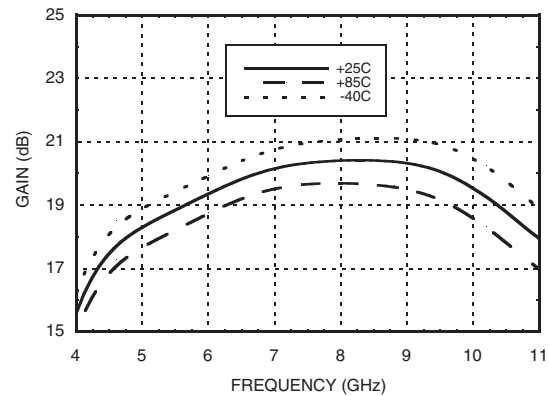


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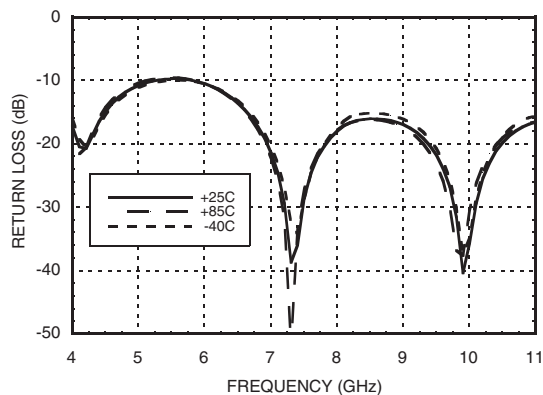
Broadband Gain & Return Loss [1]



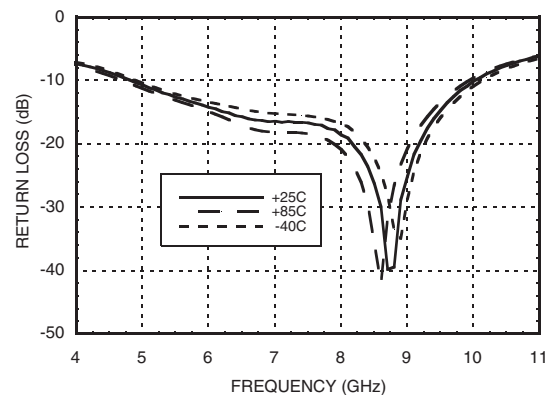
Gain vs. Temperature [1]



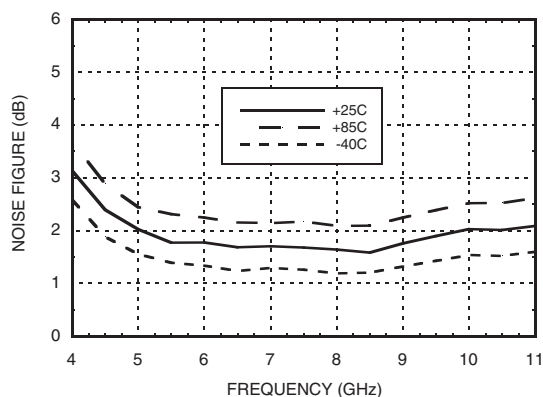
Input Return Loss vs. Temperature



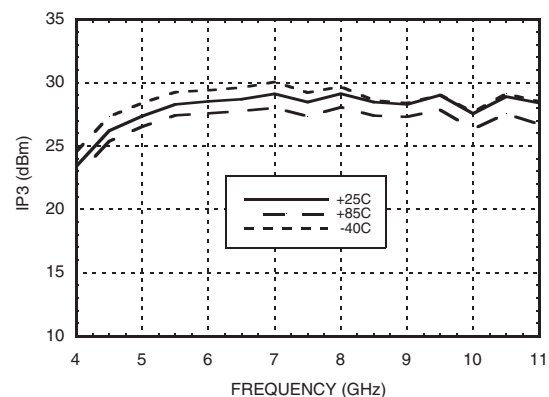
Output Return Loss vs. Temperature



Noise Figure vs. Temperature [1]



Output IP3 vs. Temperature

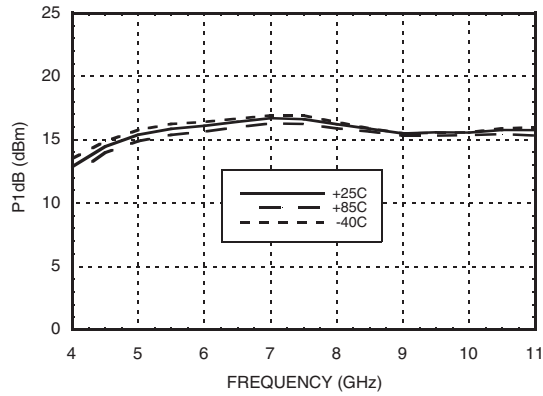


[1] Board loss removed from gain, power and noise figure measurement.

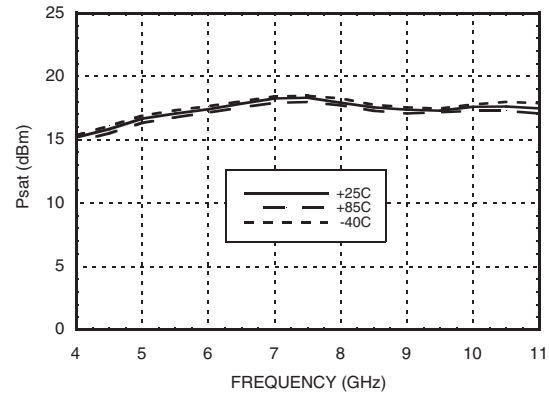


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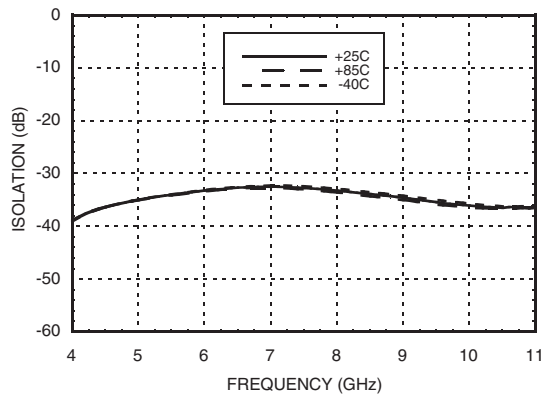
P1dB vs. Temperature [1]



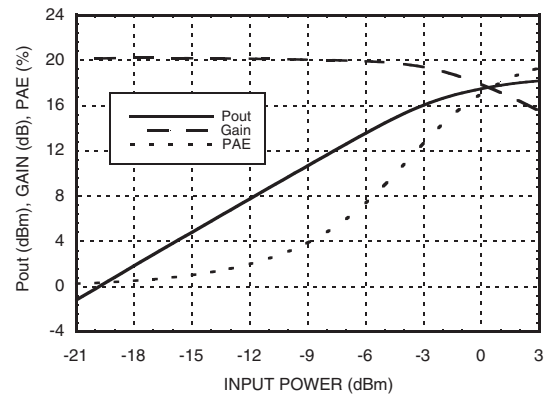
Psat vs. Temperature [1]



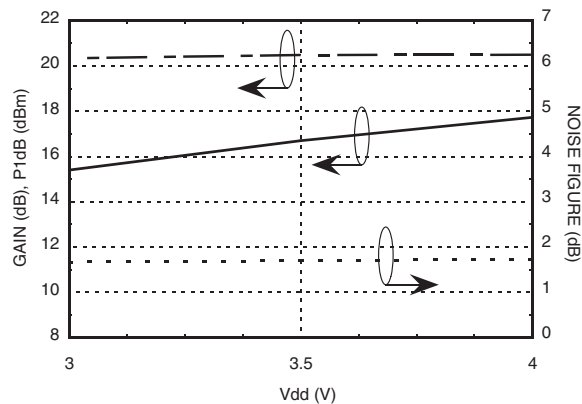
Reverse Isolation vs. Temperature



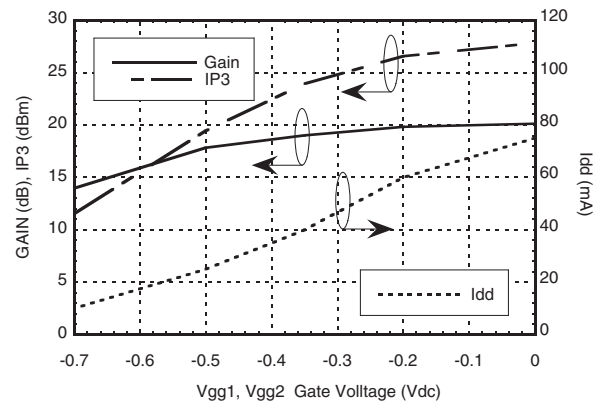
Power Compression @ 7 GHz [1]



Gain, Noise Figure & Power vs. Supply Voltage @ 7 GHz [1]



Gain, Output IP3 & Idd vs. Gate Voltage @ 7 GHz [2][3]



[1] Board loss removed from gain, power and noise figure measurement.

[2] Board loss removed from gain measurement

[3] Data taken at Vdd1 = Vdd2 = 3V

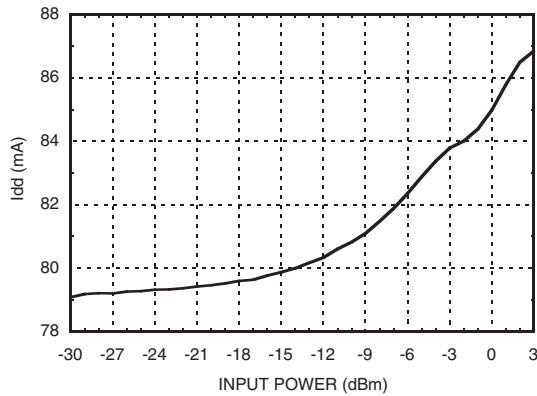
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Current vs. Input Power @ 7 GHz



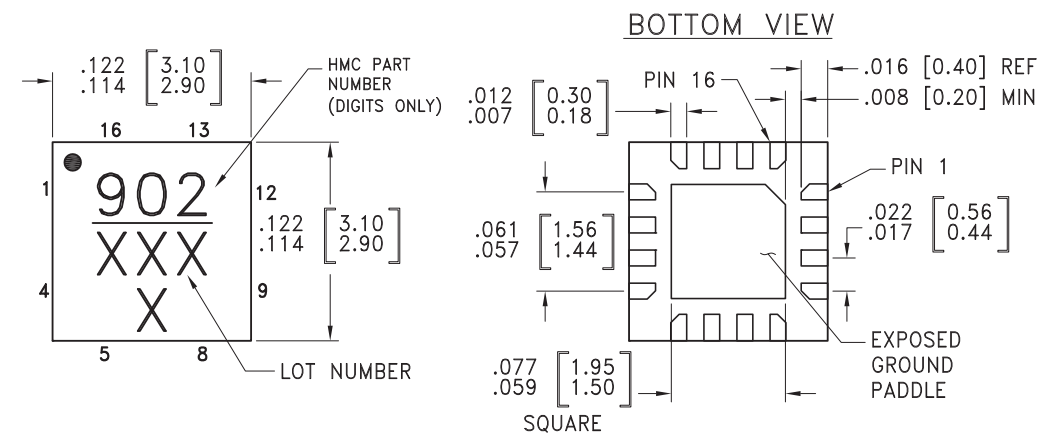
Absolute Maximum Ratings

| | |
|--|----------------|
| Drain Bias Voltage | +4.5V |
| RF Input Power | +10 dBm |
| Gate Bias Voltage, V _{gg1} | -0.8V to +0.2V |
| Gate Bias Voltage, V _{gg2} | -0.8V to +0.2V |
| Channel Temperature | 150 °C |
| Continuous P _{diss} (T = 85 °C) (derate 7 mW/°C above 85 °C) | 0.45 W |
| Thermal Resistance (Channel to ground paddle) | 143.8 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



- NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
 2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
 3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN
 4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
 5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
 6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
 7. PACKAGE WARP SHALL NOT EXCEED 0.05mm
 8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
 9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

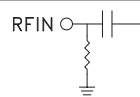

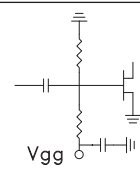
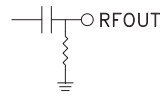
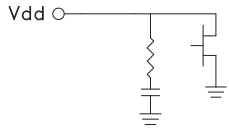
| Part Number | Package Body Material | Lead Finish | Package Marking ^[1] |
|-------------|--|------------------------------|--------------------------------|
| HMC902LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn ^[2] | 902 XXXX |

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

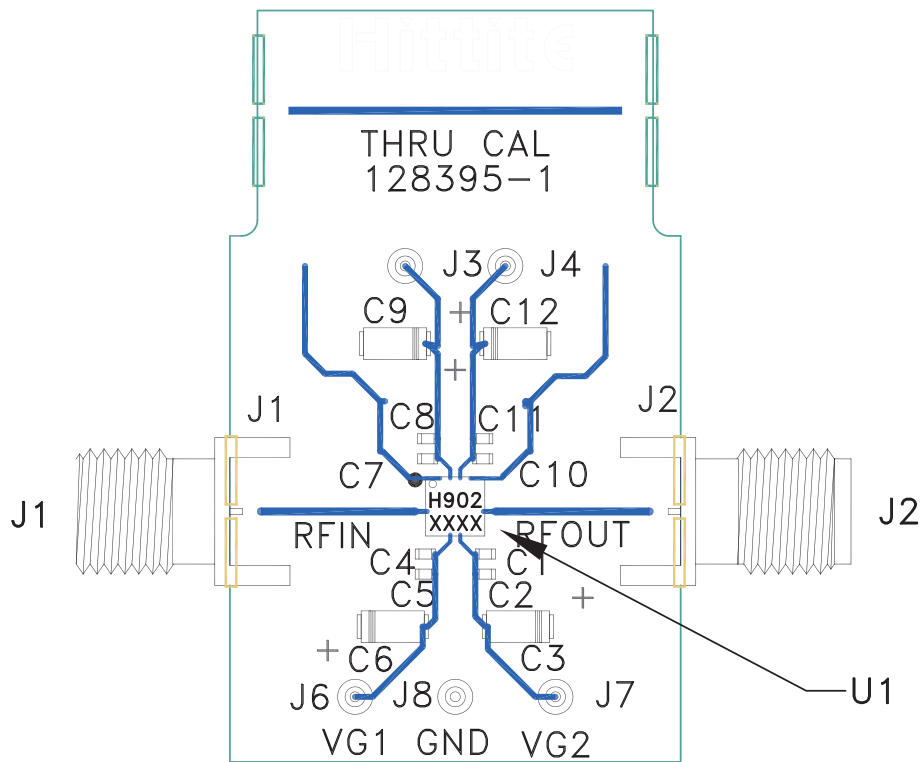
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AMPLIFIER, 5 - 10 GHz**

7
AMPLIFIERS - LOW NOISE - SMT
Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|----------------------------|------------|---|---|
| 1, 2, 5, 8, 11 - 13, 16 | N/C | The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally. | |
| 3 | RFIN | This pin is AC coupled and matched to 50 Ohms |  |
| 4, 9 | GND | Package bottom has exposed metal ground paddle that must be connected to RF/DC ground. |  |
| 6, 7 | Vgg1, Vgg2 | Optional gate control for amplifier. If left open, the amplifier will run self-biased at standard current. Negative voltage applied will reduce drain current. External capacitors required, see application circuits herein. |  |
| 10 | RFOUT | This pin is AC coupled and matched to 50 Ohms |  |
| 14, 15 | Vdd2, Vdd1 | Power supply voltage for the amplifier. See assembly for required external components. |  |



Evaluation PCB



List of Material for Evaluation PCB 129787 [1]

| Item | Description |
|-----------------|-----------------------------|
| J1, J2 | SMA Connector |
| J3, J4, J6 - J8 | DC Pins |
| C1, C4, C7, C10 | 100 pF Capacitor, 0402 Pkg. |
| C2, C5, C8, C11 | 10 KpF Capacitor, 0402 Pkg. |
| C3, C6, C9, C12 | 4.7 μF Capacitor, Tantalum |
| U1 | HMC902LP3E Amplifier |
| PCB [2] | 128395 Evaluation PCB |

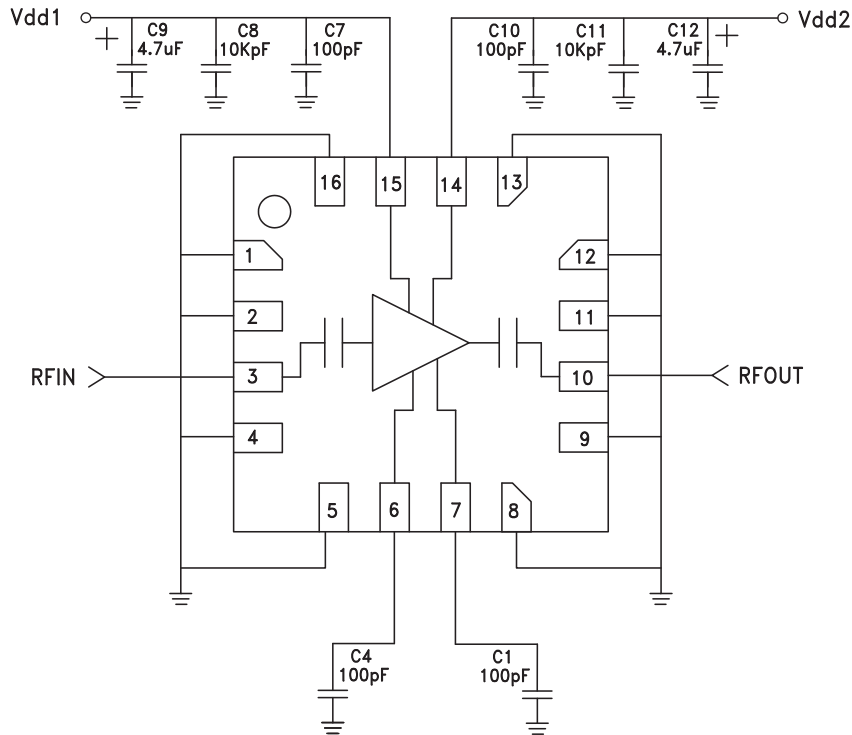
[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

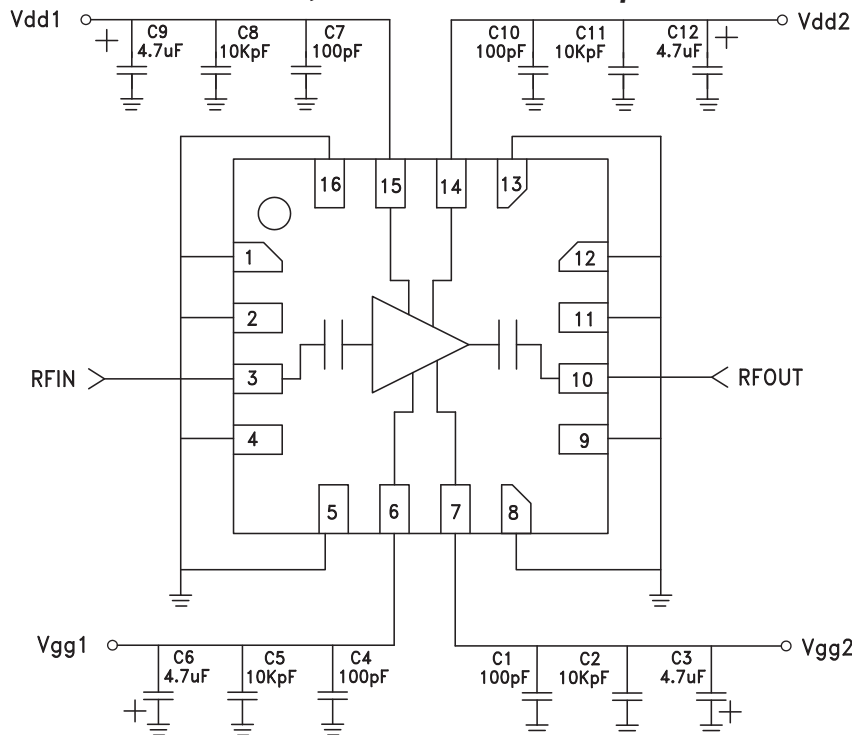
The circuit board used in this application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.



Application Circuit - Standard (Self-Biased) Operation



Application Circuit - Gate Control, Reduced Current Operation



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**Notes:**

v00.0210

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AMPLIFIER, 5 - 10 GHz****7****AMPLIFIERS - LOW NOISE - SMT**

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