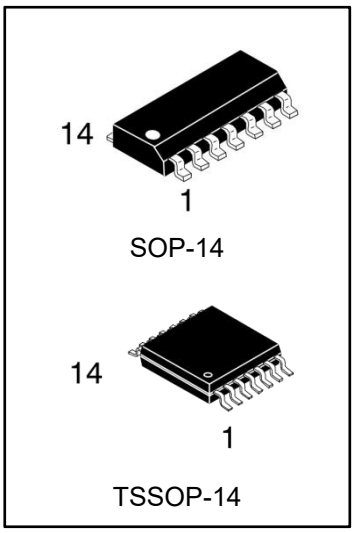
Quad 2−Input NAND Gate with Schmitt−Trigger Inputs

High−Performance Silicon−Gate CMOS

FEATURES

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements as Defined by JEDEC Standard No. 7A
- ESD Performance:
  HBM > 2000 V;
  Machine Model > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These are Pb−Free Device



ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC132DRG	SOP-14	74HC132	REEL	2500pcs/reel
74HC132PWRG	TSSOP-14	HC132	REEL	2500pcs/reel

GENERAL DESCRIPTION

The 74HC132 is identical in pinout to the LS132. The device nputs are compatible with standard CMOS outputs; with pull−up resistors, they are compatible with LSTTL outputs.
The HC132 can be used to enhance noise immunity or to square up slowly changing waveforms.

PIN CONFIGURATION

SOP-14/TSSOP-14

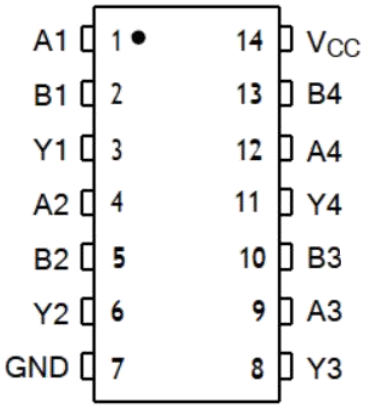
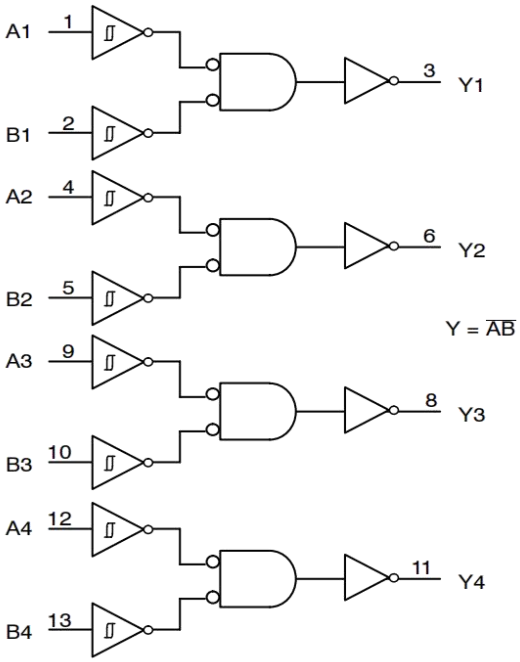


Figure 1. Pin Assignment



PIN 14 =V_{CC};

PIN 7 = GND

Figure 2. Logic Diagram

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		-0.5 to +7.0	V
V_{IN}	Digital Input Voltage		-0.5 to +7.0	V
V_{OUT}	DC Output Voltage	Output in 3−State High or Low State	-0.5 to +7.0 -0.5toVCC +0.5	V
I_{IK}	Input Diode Current		-20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, VCC and GND Pins		±75	mA
I_{GND}	DC Ground Current per Ground Pin		±75	mA
T_{STG}	Storage Temperature Range		-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		245	°C
T_J	Junction Temperature Under Bias		+125	°C
θ_{JA}	Thermal Resistance	14−SOP 14−TSSOP	125 170	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOP TSSOP	500 450	mW
M_{SL}	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2)	>2000 >200	V
$I_{Latchup}$	Latchup Performance	Above VCC and Below GND at 85°C (Note 3)	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.Tested to EIA/JESD22−A114−A.

2.Tested to EIA/JESD22−A115−A.

3.Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+85	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	–	NoLimt (Note5)	ns

4.When V_{IN} ~ 0.5 V_{CC}, I_{CC} >> quiescent current.

5.Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	VCC (V)	Guaranteed Limit		Unit
				-40°C to 25°C	≤85°C	
VT+max	Maximum Positive Going Input Threshold Voltage (Figure 5)	V_{OUT} = 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	V
VT+min	Minimum Positive−Going Input Threshold Voltage (Figure 5)	V_{OUT} = 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	1.0 2.3 3.0	0.95 2.25 2.95	V
VT−max	Maximum Negative−Going Input Threshold Voltage (Figure 5)	V_{OUT} = VCC – 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	0.9 2.0 2.6	0.95 2.05 2.65	V
VT−min	Minimum Negative−Going Input Threshold Voltage (Figure 5)	V_{OUT} = V_{CC} – 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	V
VHmax (Note 7)	Maximum Hysteresis Voltage (Figure 5)	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	1.2 2.25 3.0	1.2 2.25 3.0	V
VHmin (Note 7)	Minimum Hysteresis Voltage (Figure 5)	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	0.2 0.4 0.5	0.2 0.4 0.5	V
V_{OH}	Minimum High−Level Output Voltage	V_{IN} ≤ VT−min or VT+max $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	V
		VIN ≤ −VT−min or VT+max |IOUT| ≤ 4.0 mA |IOUT| ≤ 5.2 mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	

V_{OL}	Maximum Low−Level Output Voltage	V_{IN} ≥VT+max $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	V
		VIN≥ VT+max$\|I_{OUT}\|$ ≤ 4.0 mA $\|I_{OUT}\|$ ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	
I_{IN}	Maximum Input Leakage Current	V_{IN} = V_{CC} or GND	6.0	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0	2.0	20	μA

6.$V_H$min > (V_T+min) — (V_T−max); $V_H$max = (V_T+max) + (V_T−min).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	VCC (V)	Guaranteed Limit		Unit
			-40°C to 25°C	≤85°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 3 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	ns
C_{in}	Maximum Input Capacitance	—	10	10	pF
C_{PD}	Power Dissipation Capacitance(per Gate)(Note 10)	Typical@25°C,VCC=5.0V 24			pF

Used to determine the no−load dynamic power consumption: P_D = C_{PD} V_{CC}^2f + I_{CC} V_{CC}

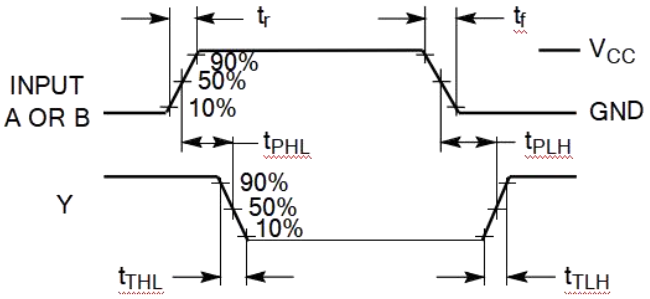
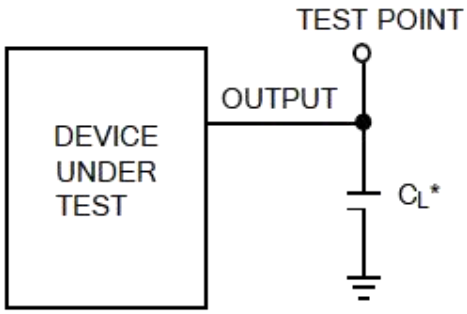
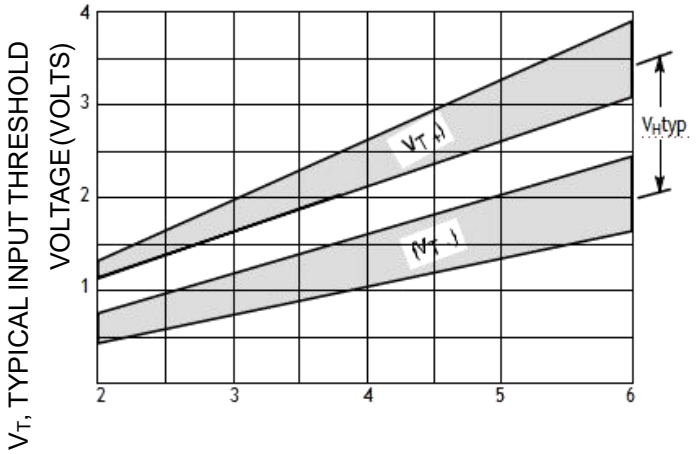


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

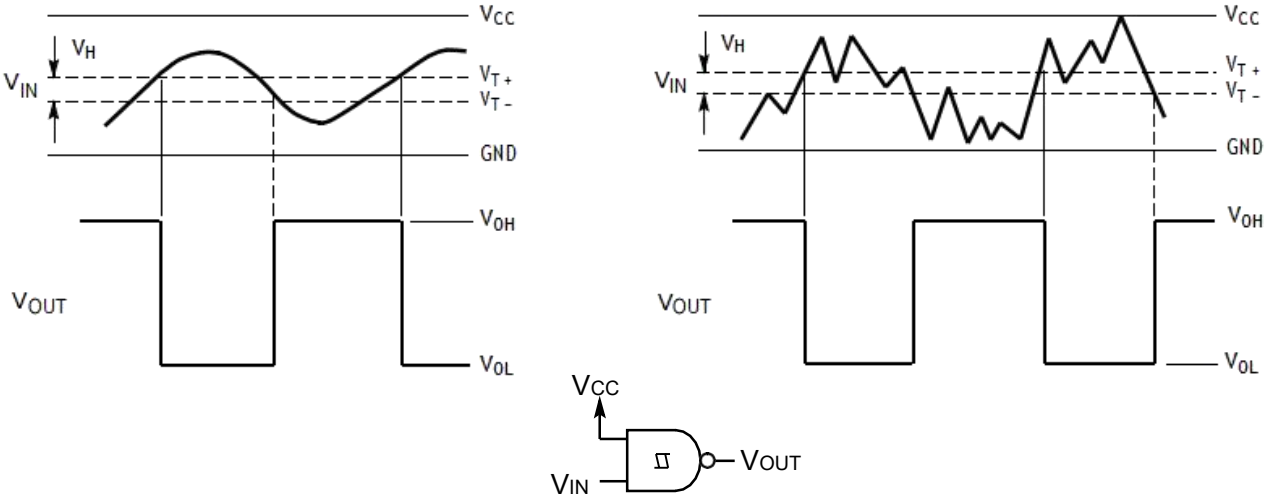
Figure 4. Test Circuit



V_{CC},POWER SUPPLY VOLTAE (VOLTS)

VHtyp = (VT + typ) − (VT − typ)

Figure 5. Typical Input Threshold, VT+, VT− Versus Power Supply Voltage



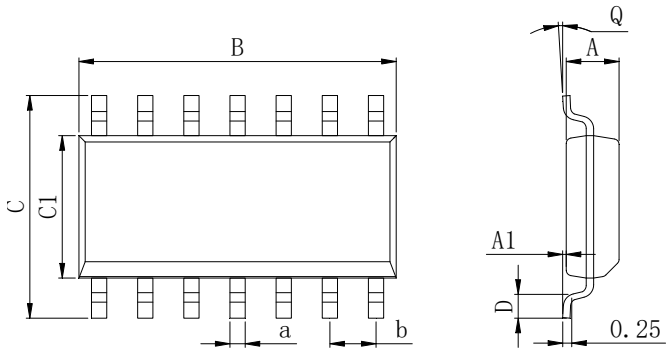
(A)A SCHMITT TRIGGER SQUARES UP INPUTS WITH SLOW RISE AND FALL TIMES

(B) A SCHMITT TRGGER OFFERS MAXIMUM NOSISE IMMUNITY

FIgure6.Typical Schmitt-Trigger Applications

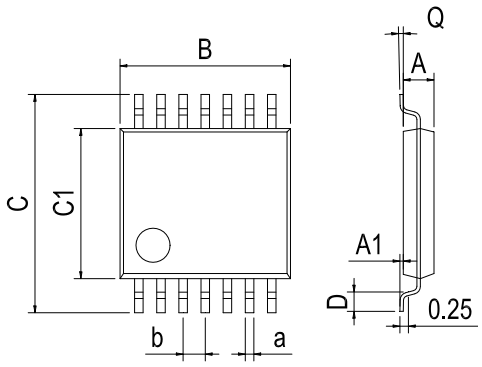
PHYSICAL DIMENSIONS

SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

REVISION HISTORY

DATE	REVISION	PAGE
2020-3-1	New	1-9
2023-7-21	Update Lead Temperature、Update encapsulation type	3、1

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