Multichannel 96 kHz Codec

Data Sheet

AD1836A

FEATURES

- 5 V multichannel audio system
- Accepts 16-/18-/20-/24-bit data
- Supports 24-bit and 96 kHz sample rate
- Multibit Σ-Δ modulators with data directed scrambling
- Differential output for optimum performance
- ADCs: –92 dB THD + N, 105 dB SNR and dynamic range
- DACs: –95 dB THD + N, 108 dB SNR and dynamic range
- On-chip volume control with "auto-ramp" function
- Programmable gain amplifier for ADC input
- Hardware and software controllable clickless mute
- Digital de-emphasis processing
- Supports 256 × f_S, 512 × f_S, or 768 × f_S master clock
- Power-down mode plus soft power-down mode
- Flexible serial data port with right justified, left justified, I²S compatible, and DSP serial port modes
- TDM interface mode supports 8 in/8 out using a single SHARC® SPORT
- 52-lead MQFP (PQFP) plastic package

APPLICATIONS

- Home theater systems
- Automotive audio systems
- DVD recorders
- Set-top boxes
- Digital audio effects processors

PRODUCT OVERVIEW

The AD1836A is a high performance, single-chip codec that provides three stereo DACs and two stereo ADCs using Analog Devices, Inc., patented multibit Σ-Δ architecture. An SPI® port is included, allowing a microcontroller to adjust volume and many other parameters. The AD1836A operates from a 5 V supply, with provision for a separate output supply to interface with low voltage external circuitry. The AD1836A is available in a 52-lead MQFP (PQFP) package.

FUNCTIONAL BLOCK DIAGRAM

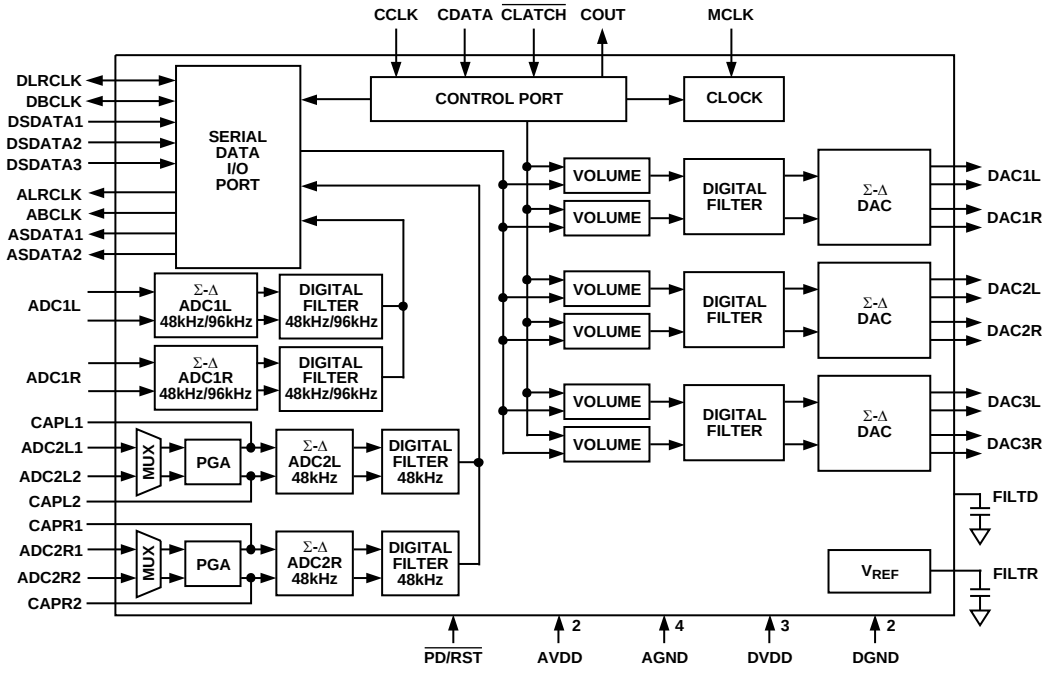

Figure 1.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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8/03—Revision 0: Initial Version

AD1836A—SPECIFICATIONS

Table 1. Test conditions, unless otherwise noted. Performance of all channels is identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).

Parameter	Rating
Supply Voltages (AVDD, DVDD)	5 V
Ambient Temperature	25°C
Master Clock	12.288 MHz (48 kHz f_S, 256 × f_S Mode)
Input Signal	1.000 kHz, 0 dBFS (Full Scale)
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	24 Bits
Load Capacitance (Digital Output)	100 pF
Load Impedance (Digital Output)	2.5 kΩ
Input Voltage HI	2.4 V
Input Voltage LO	0.8 V

Table 2. Analog Performance

Parameter		Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS	ADC Resolution (all ADCs)		24		Bits
	Dynamic Range (20 Hz to 20 kHz, –60 dB Input)[1, 2]				
	No Filter (RMS), AD1836AAS	97	102		dB
	With A-Weighted Filter (RMS), AD1836AAS	100	105		dB
	No Filter (RMS), AD1836ACS	94	99		dB
	With A-Weighted Filter (RMS), AD1836ACS	97	102		dB
	Total Harmonic Distortion + Noise (–1 dBFS)[1]		–92	–83	dB
	Full-Scale Input Voltage (Differential)		2.18 (6.16)		V rms (V pp)
	Gain Error	–5.0		+5.0	%
	Interchannel Gain Mismatch	–0.1		+0.1	dB
	Offset Error	–10	0	+10	mV
	Gain Drift		100		ppm/°C
	Interchannel Isolation		–110		dB
	Programmable Input Gain		12		dB
	Gain Step Size		3		dB
	CMRR, Direct Input, 100 mV RMS, 1 kHz		–77	–63	dB
	CMRR, Direct Input, 100 mV RMS, 20 kHz		–72	–60	dB
	CMRR, PGA Differential Input, 100 mV RMS, 1 kHz		–57	–39	dB
	CMRR, PGA Differential Input, 100 mV RMS, 20 kHz		–57	–39	dB
	Input Resistance	10			kΩ
	Input Capacitance			15	pF
	Common-Mode Input Volts		2.25		V
DIGITAL-TO-ANALOG CONVERTERS	Dynamic Range (20 Hz to 20 kHz, –60 dB Input)[1, 2]				
	No Filter (RMS), AD1836AAS	102	105		dB
	With A-Weighted Filter (RMS), AD1836AAS	105	108		dB
	No Filter (RMS), AD1836ACS	99	102		dB
	With A-Weighted Filter (RMS), AD1836ACS	102	105		dB
	Total Harmonic Distortion + Noise (0 dBFS)[1]		–95	–85	dB
	Full-Scale Output Voltage (Differential)		2.0 (5.6)		V rms (V pp)
	Gain Error	–6.0		+6.0	%
	Interchannel Gain Mismatch	–0.3		+0.3	dB
	Offset Error	15	55	95	mV
	Gain Drift		150		ppm/°C
	Interchannel Isolation		–110		dB
	Interchannel Phase Deviation		±0.1		Degrees
	Volume Control Step Size (1023 Linear Steps)		0.098		%
	Volume Control Range (Max Attenuation)		60		dB
	Max Attenuation		–100		dB
	De-emphasis Gain Error			±0.1	dB
	Output Resistance at Each Pin		115		Ω
	V_{REF} (FILTR), Common-Mode Output	2.2	2.25	2.3	V

[1] Total harmonic distortion + noise and dynamic range typical specifications are for two channels active, max/min are all channels active.
[2] Measured with Audio Precision System Two Cascade in rms mode. Averaging mode will show approximately 2 dB better performance.

Table 3. Digital I/O

Parameter	Min	Typ	Max	Unit
Input Voltage HI (V_{IH})	2.2			V
Input Voltage LO (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 2.4 V)			10	µA
Input Leakage (I_{IL} @ V_{IL} = 0.8 V)			10	µA
High Level Output Voltage (V_{OH}) I_{OH} = 2 mA	ODVDD – 0.4			V
Low Level Output Voltage (V_{OL}) I_{OL} = 2 mA			0.5	V
Input Capacitance			20	pF

Table 4. Power Supplies

Parameter		Min	Typ	Max	Unit
Supplies	Voltage, DVDD and AVDD	4.75	5	5.25	V
	Voltage, ODVDD	3.0	3.3/5	5.25	V
	Analog Current		108		mA
	Analog Current—Power-Down		47		mA
	Digital Current		78		mA
	Digital Current—Power-Down		1.5		mA
Dissipation	Operation—Both Supplies		930		mW
	Operation—Analog Supplies		540		mW
	Operation—Digital Supplies		390		mW
	Power-Down—Both Supplies		243		mW
Power Supply Rejection Ratio	1 kHz 300 mV p-p Signal at Analog Supply Pins		–60		dB
	20 kHz 300 mV p-p Signal at Analog Supply Pins		–50		dB

Table 5. Temperature Range

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	–40		+85	°C Ambient
	–40		+110	°C Case
Storage	–65		+150	°C

Table 6. Digital Filter @ 44.1 kHz

Parameter		Min	Typ	Max	Unit
ADC DECIMATION FILTER	Pass Band		20		kHz
	Pass-Band Ripple		±0.0001		dB
	Transition Band		22		kHz
	Stop Band		24		kHz
	Stop-Band Attenuation		120		dB
	Group Delay		990.20		µs
DAC INTERPOLATION FILTER	Pass Band		20		kHz
	Pass-Band Ripple		±0.01		dB
	Transition Band		22		kHz
	Stop Band		24		kHz
	Stop-Band Attenuation		70		dB
	Group Delay		446.35		µs

Table 7. Timing Specifications

Parameter			Comments	Min	Max	Unit
MASTER CLOCK AND RESET	t_{MH}	MCLK High	512 × f_S Mode	18		ns
	t_{ML}	MCLK Low	512 × f_S Mode	18		ns
	t_{MCLK}	MCLK Period	512 × f_S Mode	36		ns
	f_{MCLK}	MCLK Frequency	512 × f_S Mode		27	MHz
	t_{PDR}	$\overline{\text{PD/RST}}$ Low		5		ns
	t_{PDRR}	$\overline{\text{PD/RST}}$ Recovery	Reset to Active Output	4500		t_{MCLK}
SPI PORT	t_{CHH}	CCLK High		10		ns
	t_{CHL}	CCLK Low		10		ns
	t_{CDS}	CDATA Setup	To CCLK Rising	5		ns
	t_{CDH}	CDATA Hold	From CCLK Rising	5		ns
	t_{CLS}	$\overline{\text{CLATCH}}$ Setup	To CCLK Rising	5		ns
	t_{CLH}	$\overline{\text{CLATCH}}$ Hold	From CCLK Falling	5		ns
	t_{CODE}	COUT Enable	From CCLK Falling		10	ns
	t_{COD}	COUT Delay	From CCLK Falling		10	ns
	t_{COH}	COUT Hold	From CCLK Falling	0		ns
	t_{COTS}	COUT Three-State	From CCLK Falling		10	ns
DAC SERIAL PORT (Normal Modes)	t_{DBH}	DBCLK High		15		ns
	t_{DBL}	DBCLK Low		15		ns
	f_{DB}	DBCLK Frequency		64 × f_S		ns
	t_{DLS}	DLRCLK Setup	To DBCLK Rising	0		ns
	t_{DLH}	DLRCLK Hold	From DBCLK Rising	10		ns
	t_{DDS}	DSDATA Setup	To DBCLK Rising	0		ns
	t_{DDH}	DSDATA Hold	From DBCLK Rising	20		ns
DAC SERIAL PORT (Packed 128 Mode, Packed 256 Mode)	t_{DBH}	DBCLK High		15		ns
	t_{DBL}	DBCLK Low		15		ns
	f_{DB}	DBCLK Frequency		256 × f_S		ns
	t_{DLS}	DLRCLK Setup	To DBCLK Rising	0		ns
	t_{DLH}	DLRCLK Hold	From DBCLK Rising	10		ns
	t_{DDS}	DSDATA Setup	To DBCLK Rising	0		ns
	t_{DDH}	DSDATA Hold	From DBCLK Rising	20		ns
ADC SERIAL PORT (Normal Modes)	t_{ABD}	ABCLK Delay	From MCLK Transition, 256 × f_S Mode		15	ns
			From MCLK Rising, 512 × f_S Mode			
	t_{ALS}	LRCLK Skew	From ABCLK Falling	−2	+2	ns
	t_{ABDD}	ASDATA Delay	From ABCLK Falling		5	ns
ADC SERIAL PORT (Packed 128 Mode, Packed 256 Mode)	t_{ABD}	ABCLK Delay	From MCLK Transition, 256 × f_S Mode		15	ns
			From MCLK Rising, 512 × f_S Mode			
	t_{ALS}	LRCLK Skew	From ABCLK Falling	−2	+2	ns
	t_{ABDD}	ASDATA Delay	From ABCLK Falling		5	ns
ADC SERIAL PORT (TDM Packed AUX)	t_{ABD}	ABCLK Delay	From MCLK Transition, 256 × f_S Mode		15	ns
			From MCLK Rising, 512 × f_S Mode			
	t_{ALS}	LRCLK Skew	From ABCLK Falling	−2	+2	ns
	t_{ABDD}	ASDATA Delay	From ABCLK Falling		5	ns
	t_{DDS}	DSDATA1 Hold	To ABCLK Rising	0		ns
	t_{DDH}	DSDATA1 Hold	From ABCLK Rising	7		ns
AUXILIARY INTERFACE	t_{AXDS}	AAUXDATA Setup	To AUXBCLK Rising	7		ns
	t_{AXDH}	AAUXDATA Hold	From AUXBCLK Rising	10		ns
	t_{DXDD}	DAUXDATA Delay	From AUXBCLK Falling		25	ns

Table 7. Timing Specifications (Continued)

Parameter			Comments	Min	Max	Unit
AUXILIARY INTERFACE (Master Mode)	t_{XBD}	AUXBCLK Delay	From MCLK Transition, 256 × f_S Mode		15	ns
			From MCLK Rising, 512 × f_S Mode			
	t_{XLS}	AUXLRCLK Skew	From AUXBCLK Falling	−3	+3	ns
AUXILIARY INTERFACE (Slave Mode)	t_{XBH}	AUXBCLK High		60		ns
	t_{XBL}	AUXBCLK Low		60		ns
	f_{XB}	AUXBCLK Frequency		64 × f_S		ns
	t_{DLS}	AUXLRCLK Setup	To AUXBCLK Rising	5		ns
	t_{DLH}	AUXLRCLK Hold	From AUXBCLK Rising	15		ns

ABSOLUTE MAXIMUM RATINGS

Table 8. AD1836A Absolute Maximum Ratings

Parameter	Min	Max	Unit
Analog (AVDD)	–0.3	+6	V
Digital (DVDD)	–0.3	+6	V
Input Current (Except Supply Pins)		±20	mA
Analog Input Voltage (Signal Pins)	–0.3	AVDD + 0.3	V
Digital Input Voltage (Signal Pins)	–0.3	DVDD + 0.3	V
Ambient Temperature (Operating)	–40	+85	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 9. Package Characteristics

Parameter	Min	Typ	Max	Unit
θ_{JA} (Thermal Resistance [Junction to Ambient])		45		°C/W
θ_{JC} (Thermal Resistance [Junction to Case])		18		°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND PIN FUNCTIONAL DESCRIPTIONS

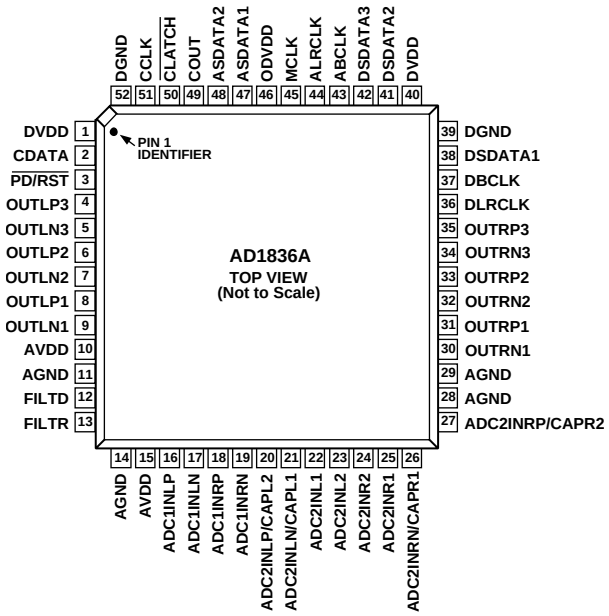


Figure 2. 52-Lead MQFP

Table 10. Pin Function Descriptions—52-Lead MQFP

Pin No.	In/Out	Mnemonic	Description
1	I	DVDD	Digital Power Supply. Connect to digital 5 V supply.
2	I	CDATA	Serial Control Input.
3	I	$\overline{\text{PD/RST}}$	Power-Down Reset (Active Low).
4	O	OUTLP3	DAC 3 Left Positive Output.
5	O	OUTLN3	DAC 3 Left Negative Output.
6	O	OUTLP2	DAC 2 Left Positive Output.
7	O	OUTLN2	DAC 2 Left Negative Output.
8	O	OUTLP1	DAC 1 Left Positive Output.
9	O	OUTLN1	DAC 1 Left Negative Output.
10	I	AVDD	Analog Power Supply. Connect to analog 5 V.
11	I	AGND	Analog Ground.
12	I	FILTD	Filter Capacitor Connection. Bypass with 10 µF||100 nF to AGND.
13	I	FILTR	Voltage Reference Filter Capacitor Connection. Bypass with 10 µF||100 nF to AGND.
14	I	AGND	Analog Ground.
15	I	AVDD	Analog Power Supply. Connect to analog 5 V supply.
16	I	ADC1INLP	ADC1 Left Positive Input.
17	I	ADC1INLN	ADC1 Left Negative Input.
18	I	ADC1INRP	ADC1 Right Positive Input.
19	I	ADC1INRN	ADC1 Right Negative Input.
20	I	ADC2INLP/CAPL2	ADC2 Left Positive Input (Direct Mode)/ADC2 Left Decoupling Cap (MUX/PGA and PGA Differential Mode).
21	I	ADC2INLN/CAPL1	ADC2 Left Negative Input (Direct Mode)/ADC2 Left Decoupling Capacitor (MUX/PGA and PGA Differential Mode).
22	I	ADC2INL1	ADC2 Left Input 1 (MUX/PGA Mode)/Left Positive Input (PGA Differential Mode).
23	I	ADC2INL2	ADC2 Left Input 2 (MUX/PGA Mode)/Left Negative Input (PGA Differential Mode).
24	I	ADC2INR2	ADC2 Right Input 2 (MUX/PGA Mode)/Right Negative Input (PGA Differential Mode).
25	I	ADC2INR1	ADC2 Right Input 1 (MUX/PGA Mode)/Right Positive Input (PGA Differential Mode).
26	I	ADC2INRN/CAPR1	ADC2 Right Negative Input (Direct Mode)/ADC2 Right Decoupling Capacitor (MUX/PGA and PGA Differential Mode).

Pin No.	In/Out	Mnemonic	Description
27	I	ADC2INRP/CAPR2	ADC2 Right Positive Input (Direct Mode)/ADC2 Right Decoupling Capacitor (MUX/PGA and PGA Differential Mode).
28	I	AGND	Analog Ground.
29	I	AGND	Analog Ground.
30	O	OUTRN1	DAC 1 Right Negative Output.
31	O	OUTRP1	DAC 1 Right Positive Output.
32	O	OUTRN2	DAC 2 Right Negative Output.
33	O	OUTRP2	DAC 2 Right Positive Output.
34	O	OUTRN3	DAC 3 Right Negative Output.
35	O	OUTRP3	DAC 3 Right Positive Output.
36	I/O	DLRCLK	LR Clock for DACs.
37	I/O	DBCLK	Bit Clock for DACs.
38	I	DSDATA1	DAC Input 1 (Input to DAC 1 L and R).
39	I	DGND	Digital Ground.
40	I	DVDD	Digital Power Supply. Connect to digital 5 V supply.
41	I	DSDATA2	DAC Input 2 (Input to DAC 2 L and R).
42	I	DSDATA3	DAC Input 3 (Input to DAC 3 L and R).
43	O	ABCLK	Bit Clock for ADCs.
44	O	ALRCLK	LR Clock for ADCs.
45	I	MCLK	Master Clock Input.
46	I	ODVDD	Digital Output Driver Power Supply. Connect to 3.3 V or 5 V logic supply.
47	O	ASDATA1	ADC Serial Data Output 1 (ADC 1 L and R).
48	O	ASDATA2	ADC Serial Data Output 2 (ADC 2 L and R).
49	O	COUT	Output for Control Data.
50	I	$\overline{\text{CLATCH}}$	Latch Input for Control Data.
51	I	CCLK	Control Clock Input for Control Data.
52	I	DGND	Digital Ground.

FUNCTIONAL OVERVIEW

ADCs

There are four ADC channels in the AD1836A configured as two independent stereo pairs. One stereo pair is the primary ADC and has fully differential inputs. The second pair can be programmed to operate in one of three possible input modes (programmed via SPI ADC Control Register 3). The ADC section may also operate at a sample rate of 96 kHz with only the two primary channels active. The ADCs include an on-board digital decimation filter with 120 dB stop-band attenuation and linear phase response, operating at an over-sampling ratio of 128 (for 4-channel 48 kHz operation) or 64 (for 2-channel 96 kHz operation).

The primary ADC pair should be driven from a differential signal source for best performance. The input pins of the primary ADC connect directly to the internal switched capacitors. To isolate the external driving op amp from the "glitches" caused by the internal switched capacitors, each input pin should be isolated by using a series-connected external 100 Ω resistor together with a 1 nF capacitor connected from each input to ground. This capacitor must be of high quality, for example, ceramic NPO or polypropylene film.

The secondary input pair can operate in one of three modes:

- Direct differential inputs (driven the same way as the primary ADC inputs described above).
- PGA mode with differential inputs. In this mode, the PGA amplifier can be programmed using the SPI port to give an input gain of 0 dB to 12 dB in steps of 3 dB. External capacitors are used after the PGA to supply filtering for the switched capacitor inputs.
- Single-ended MUX/PGA mode. In this mode, two single-ended stereo inputs are provided that can be selected using the SPI port. Input gain can be programmed from 0 dB to 12 dB in steps of 3 dB. External capacitors are used to supply filtering for the switched capacitor inputs.

Peak level information for each ADC may be read from the SPI port through Registers 12 to 15. The data is supplied as a 10-bit word with a maximum range of 0 dB to –60 dB and a resolution of 1 dB. The registers hold peak information until read; after reading, the registers are reset so that new peak information can be acquired. Refer to the register descriptions for the details on this format.

A digital high-pass filter can be switched in line with the ADCs under SPI control to remove residual dc offsets. It has a 1.3 Hz, 6 dB per octave cutoff at a 44.1 kHz sample rate. The cutoff frequency will scale directly with sample frequency. Note that it does not remove these offsets from the peak level measurement.

The voltage at the V_{REF} pin, FILTR (~2.25 V), can be used to bias external op amps that buffer the input signals. See the Power Supply and Voltage Reference section.

DACs

The AD1836A has six DAC channels arranged as three independent stereo pairs, with six fully differential analog outputs for improved noise and distortion performance. Each channel has its own independently programmable attenuator, adjustable in 1024 linear steps. Digital inputs are supplied through three serial data input pins (one for each stereo pair) and a common frame (DLRCLK) and bit (DBCLK) clock. Alternatively, one of the "packed data" modes may be used to access all six channels on a single TDM data pin.

Each set of differential output pins sits at the dc level of V_{REF} and swings ±1.4 V for a 0 dB digital input signal. A single op amp third order external low-pass filter is recommended to remove high frequency noise present on the output pins, as well as to provide differential-to-single-ended conversion. Note that the use of op amps with low slew rate or low bandwidth may cause high frequency noise and tones to fold down into the audio band; care should be exercised in selecting these components.

The voltage at the V_{REF} pin, FILTR (~2.25 V), can be used to bias the external op amps that buffer the output signals. See the Power Supply and Voltage Reference section.

CLOCK SIGNALS

The master clock frequency can be selected for 256, 512, or 768 times the sample rate. The default at power-up is 256 × f_S. For operation at 96 kHz, the master clock frequency should stay at the same absolute frequency. For example, if the AD1836A is programmed in 256 × f_S, 48 kHz mode, the frequency of the master clock would be 256 × 48 kHz = 12.288 MHz. If the AD1836A is then switched to 96 kHz operation (via writing to the SPI port), the frequency of the master clock should remain at 12.288 MHz (which is now 128 × f_S).

The internal clock used in the AD1836A is 512 × f_S (48 kHz mode) or 256 × f_S (96 kHz mode). A clock doubler is used to generate this internal master clock from the external clock in the 256 × f_S and 768 × f_S modes.

To maintain the highest performance possible, it is recommended that the clock jitter of the master clock signal be limited to less than 300 ps rms, measured using the edge-to-edge technique. Even at these levels, extra noise or tones may appear in the DAC outputs if the jitter spectrum contains large spectral peaks. It is highly recommended that an independent crystal oscillator generate the master clock. In addition, it is especially important that the clock signal should not be passed

through an FPGA or other large digital chip before being applied to the AD1836A. In most cases, this will induce clock jitter due to the fact that the clock signal is sharing common power and ground connections with other unrelated digital output signals.

The six DAC channels use a common serial bit clock to clock in the serial data and a common left-right framing clock. The four ADC channels output a common serial bit clock and a left-right framing clock. The clock signals are all synchronous with the sample rate.

RESET AND POWER-DOWN

Reset will power down the chip and set the control registers to their default settings. After reset is de-asserted, an initialization routine will run inside the AD1836A to clear all memories to zero. This initialization lasts for approximately 4500 MCLKs.

The power-down bit in the DAC Control Register 1 and ADC Control Register 1 will power down the respective digital section. The analog circuitry does not power down. All other register settings are retained.

To avoid possible synchronization problems, if MCLK is 512 f_S or 768 f_S, the clock rate should be set in ADC Control Register 3 within the first 3072 MCLK cycles after reset, or DLRCLK and DBCLK should be withheld until after the internal initialization completes (see above).

SERIAL CONTROL PORT

The AD1836A has an SPI compatible control port that permits programming the internal control registers for the ADCs and DACs and for reading the ADC signal level from the internal peak detectors. The DAC output levels may be independently programmed by means of an internal digital attenuator adjustable in 1024 linear steps.

The SPI control port is a 4-wire serial control port. The format is similar to the Motorola SPI format except the input data-word is 16 bits wide. The maximum serial bit clock frequency is 8 MHz and may be completely asynchronous to the sample rate of the ADCs and DACs. Figure 3 shows the format of the SPI signal.

All control registers are write-only. They cannot be read back. The ADC peak registers are read-only. They are reset to zero each time they are read and are updated at the next sample time.

Due to an anomaly in the SPI interface, when a write to a DAC control register follows after a read or a write to an ADC register, it may not be executed properly. Any such write should be performed twice.

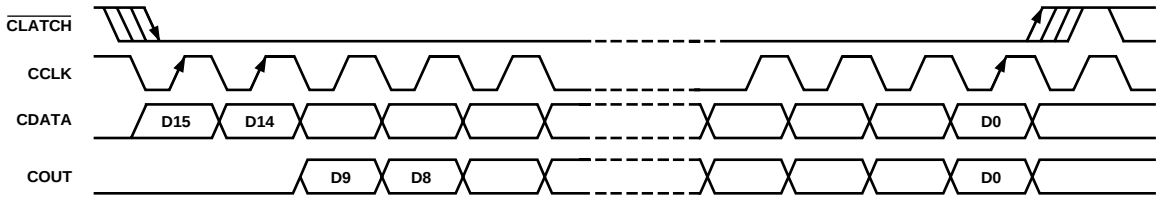


Figure 3. Format of SPI Signal

POWER SUPPLY AND VOLTAGE REFERENCE

The AD1836A is designed for 5 V supplies. Separate power supply pins are provided for the analog and digital sections. These pins should be bypassed with 100 nF ceramic chip capacitors, as close to the pins as possible, to minimize noise pickup. A bulk aluminum electrolytic capacitor of at least 22 μF should also be provided on the same PC board as the codec. For critical applications, improved performance will be obtained with separate supplies for the analog and digital sections. If this is not possible, it is recommended that the analog and digital supplies be isolated by means of a ferrite bead in series with each supply. It is important that the analog supply be as clean as possible.

For ease in interfacing to various logic families, the digital output drivers are supplied from the ODVDD pin. For CMOS logic, this should be connected to the 5 V digital supply. For 3.3 V logic, it should be connected to the 3.3 V supply. For TTL levels, it can be tied to either. All digital inputs are compatible with TTL and CMOS levels.

The internal voltage reference V_{REF} is brought out on Pin 13 (FILTR) and should be bypassed as close as possible to the chip, with a parallel combination of 10 μF and 100 nF. The reference voltage may be used to bias external op amps to the common-mode voltage of the input and output signal pins. The current drawn should be limited to less than 50 μA. This source can be connected directly to op amp inputs but should be buffered if it is required to drive resistive networks.

The FILTD pin should be connected to an external grounded capacitor. This pin is used to reduce the noise of the internal DAC bias circuitry, thereby reducing the DAC output noise. In some cases, this capacitor may be eliminated with little effect on performance.

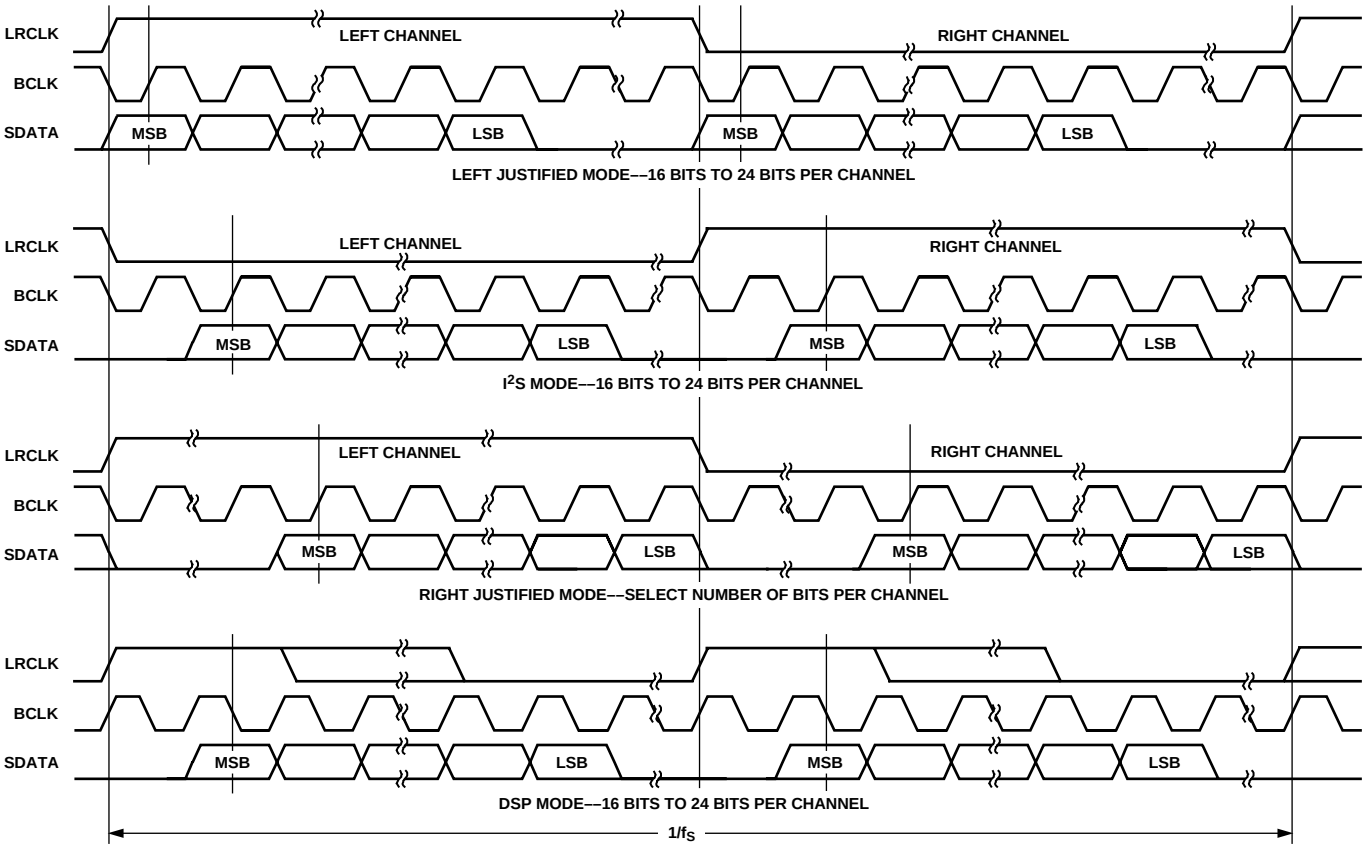
SERIAL DATA PORTS—DATA FORMAT

The ADC serial data output mode defaults to the popular I^2S format, where the data is delayed by 1 BCLK interval from the edge of the LRCLK. By programming Bits 8 and 9 in ADC Control Register 2, the serial mode can be changed to right justified (RJ), left justified DSP (DSP), left justified (LJ), Packed Mode 128, or Packed Mode 256. In the RJ mode, it is necessary to set Bits 6 and 7 to define the width of the data-word.

The DAC serial data input mode defaults to I^2S. By programming Bits 5, 6, and 7 in DAC Control Register 1, the mode can be changed to RJ, DSP, LJ, Packed Mode 128, or Packed Mode 256. The word width defaults to 24 bits but can be changed by programming Bits 3 and 4 in DAC Control Register 1. The packed modes accept six channels of data at the DSDATA1 input pin, which is routed independently to each of the six internal DACs.

A special "auxiliary mode" is provided to allow two external stereo ADCs and one external stereo DAC to be interfaced with the AD1836A to provide 8 in/8 out operation. In addition, this mode supports glueless interface to a single SHARC DSP serial port, allowing a SHARC DSP to access all eight channels of analog I/O. In this special mode, many pins are redefined; see Table 11 for a list of redefined pins. Two versions of this mode are available. In the master mode, the AD1836A provides the LRCLK and BCLK signals for the external ADCs and DAC. In the slave mode, external ADC1 provides the LRCLK and BCLK signals (which must be divided down properly from the external master clock), and the AD1836A will sync to these external clocks. In the absence of the external ADC clocks in slave mode, the ALRCLK and ABCLK outputs of the AD1836A (TDM frame sync and bit clock) will default to be the same as in master mode. See Figure 9 through Figure 11 for details of these modes. Figure 12 shows the internal signal flow diagram of the auxiliary mode.

The following figures show the serial mode formats.



NOTES
1. DSP MODE DOES NOT IDENTIFY CHANNEL
2. LRCLK NORMALLY OPERATES AT f_S EXCEPT FOR DSP MODE WHICH IS $2 \times f_S$
3. BCLK FREQUENCY IS NORMALLY $64 \times$ LRCLK BUT MAY BE OPERATED IN BURST MODE

Figure 4. Stereo Serial Modes

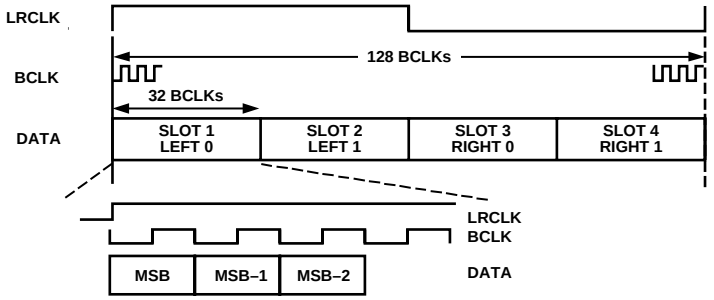


Figure 5. ADC Packed Mode 128

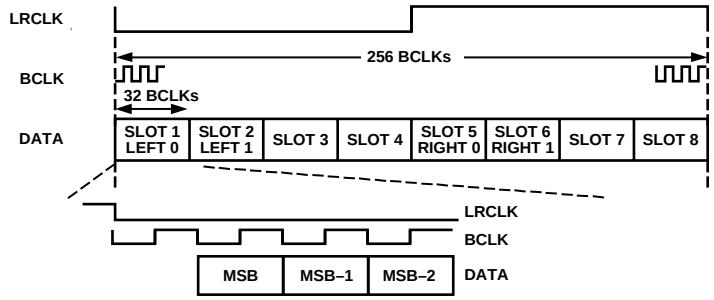


Figure 6. ADC Packed Mode 256

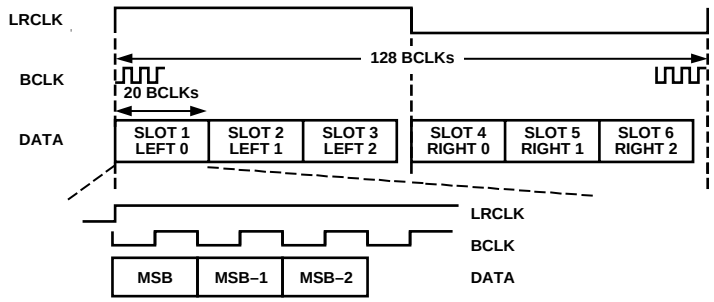


Figure 7. DAC Packed Mode 128

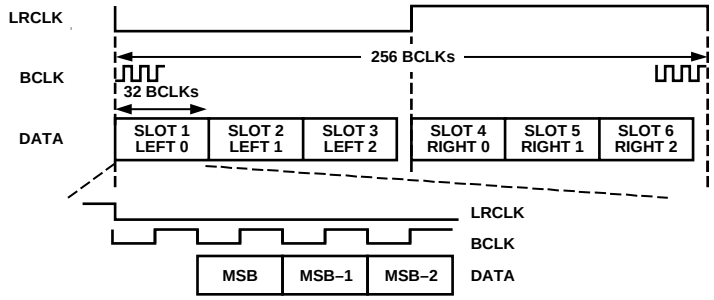
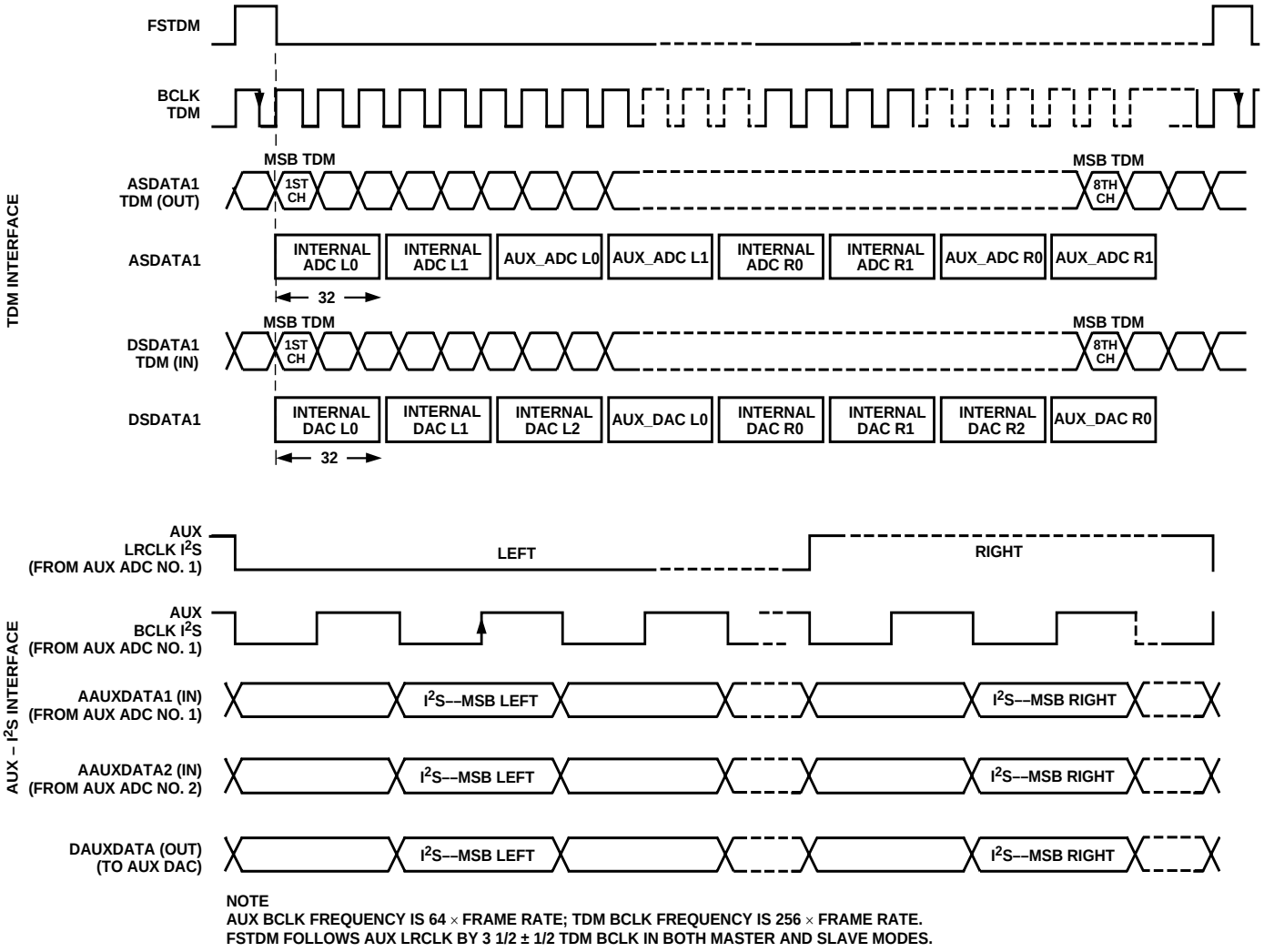


Figure 8. DAC Packed Mode 256



NOTE
AUX BCLK FREQUENCY IS 64 × FRAME RATE; TDM BCLK FREQUENCY IS 256 × FRAME RATE.
FSTDM FOLLOWS AUX LRCLK BY 3 1/2 ± 1/2 TDM BCLK IN BOTH MASTER AND SLAVE MODES.

Figure 9. AUX Mode Timing (Note that the Clocks Are Not to Scale)

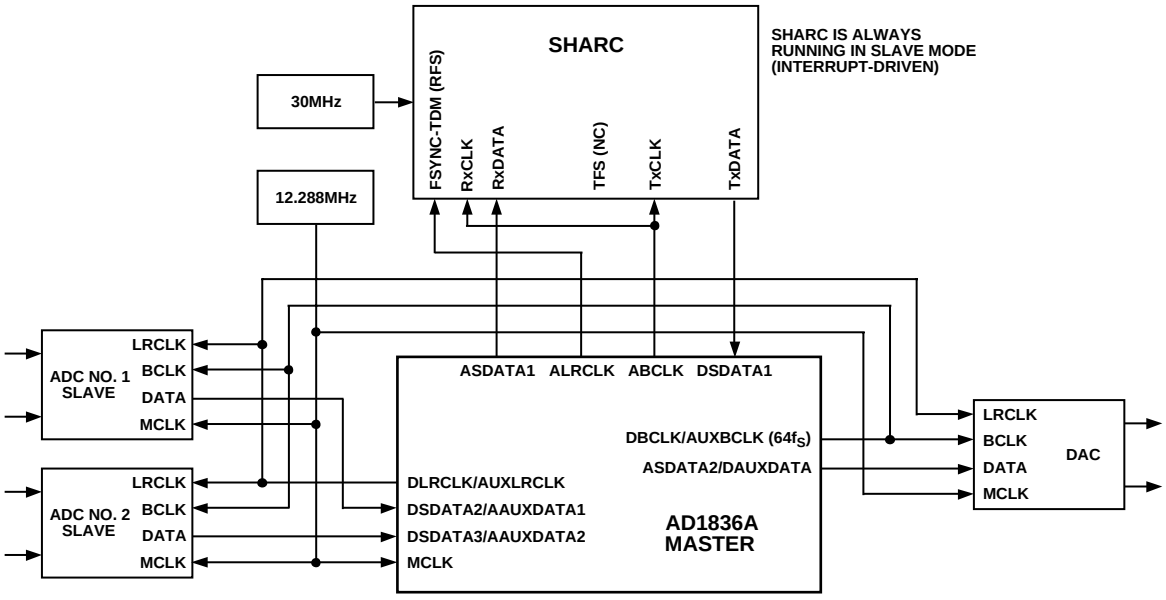


Figure 10. AUX Mode Connection to SHARC (Master Mode)

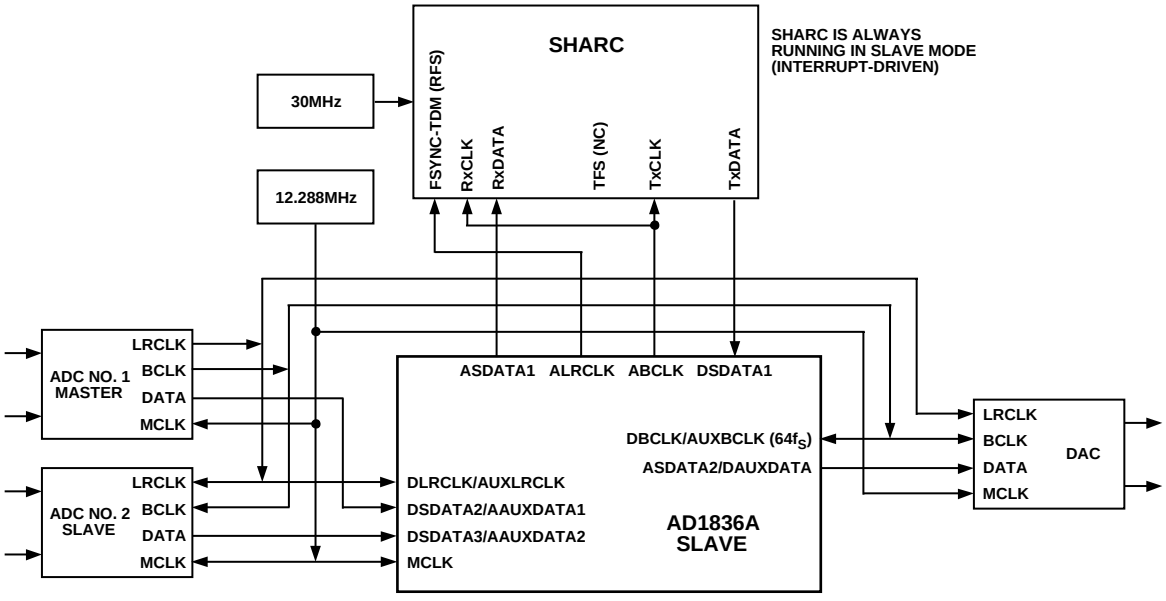


Figure 11. AUX Mode Connection to SHARC (Slave Mode)

Table 11. Pin Function Changes in AUX Mode

Pin Name (I²S/AUX Mode)	I²S Mode	AUX Mode
ASDATA1(O)	I²S Data Out, Internal ADC1	TDM Data Out, to SHARC
ASDATA2(O)/DAUXDATA(O)	I²S Data Out, Internal ADC2	AUX—I²S Data Out (to External DAC)
DSDATA1(I)	I²S Data In, Internal DAC1	TDM Data In, from SHARC
DSDATA2(I)/AAUXDATA(I)	I²S Data In, Internal DAC2	AUX—I²S Data In 1 (to External ADC)
DSDATA3(I)/AAUXDATA2(I)	I²S Data In, Internal DAC3	AUX—I²S Data In 2 (to External ADC)
ALRCLK(O)	LRCLK for Internal ADC1, ADC2	TDM Frame Sync Out, to SHARC
ABCLK(O)	BCLK for Internal ADC1, ADC2	TDM BCKL Out, to SHARC
DLRCLK(I)/AUXLRCLK(I/O)	LRCLK In/Out Internal DACs	AUX LRCLK In/Out, Driven by External IRCLK from ADC (in slave mode). In master mode, driven by internal MCLK/512.
DBCLK(I)/AUXBCLK(I/O)	BCLK In/Out Internal DACs	AUX BCLK In/Out, Driven by External BCLK from ADC (in slave mode). In master mode, driven by internal MCLK/8.

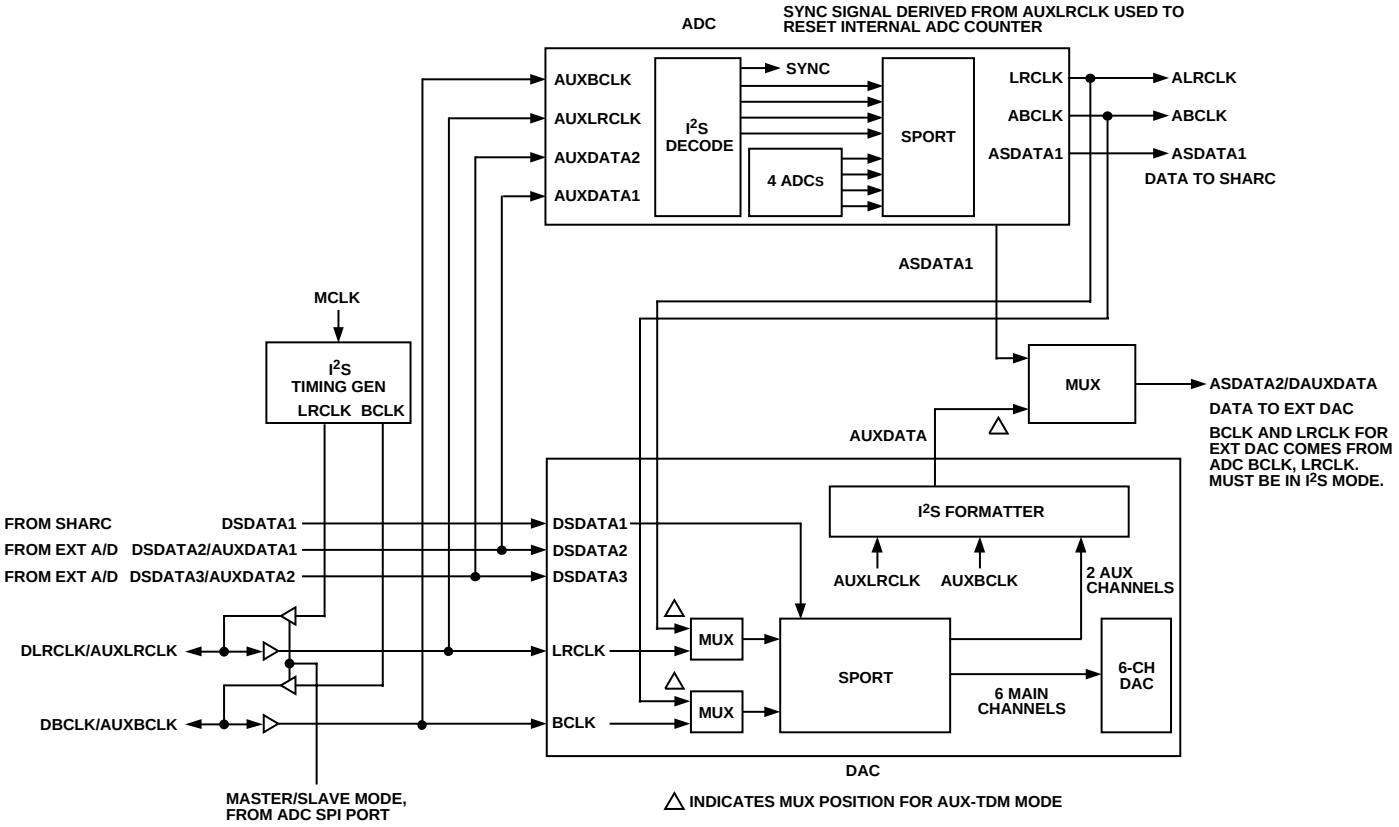


Figure 12. Extended TDM Mode (Internal Flow Diagram)

SPI CONTROL REGISTERS

Note that all control registers default to zero at power-up.

Table 12. Serial SPI Word Format

Register Address	Read/Write	Reserved	Data Field
15:12	**11**	**10**	**9:0**
4 Bits	1 = Read 0 = Write	0	10 Bits

Table 13. Register Addresses and Functions

Register Address				RD/WR	Reserved	Function
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bits 9:0**
0	0	0	0	0	0	DAC Control 1
0	0	0	1	0	0	DAC Control 2
0	0	1	0	0	0	DAC1L Volume
0	0	1	1	0	0	DAC1R Volume
0	1	0	0	0	0	DAC2L Volume
0	1	0	1	0	0	DAC2R Volume
0	1	1	0	0	0	DAC3L Volume
0	1	1	1	0	0	DAC3R Volume
1	0	0	0	0	0	ADC1L—Peak Level (Read-Only)
1	0	0	1	0	0	ADC1R—Peak Level (Read-Only)
1	0	1	0	0	0	ADC2L—Peak Level (Read-Only)
1	0	1	1	0	0	ADC2R—Peak Level (Read-Only)
1	1	0	0	0	0	ADC Control 1
1	1	0	1	0	0	ADC Control 2
1	1	1	0	0	0	ADC Control 3
1	1	1	1	0	0	Reserved

Table 14. DAC Control Register 1

Packed Mode: Eight channels are "packed" in DSDATA1 serial input. Packed Mode 128: Refer to Figure 7. Packed Mode 256: Refer to Figure 8.

Address	RD/WR	Reserved	Function					
			De-emphasis	Serial Mode	Data-Word Width	Power-Down	Interpolator Mode	Reserved
15, 14, 13, 12	**11**	**10**	**9, 8**	**7, 6, 5**	**4, 3**	**2**	**1**	**0**
0000	0	0	00 = None 01 = 44.1 kHz 10 = 32.0 kHz 11 = 48.0 kHz	000 = I²S 001 = RJ 010 = DSP 011 = LJ 100 = Packed Mode 256 101 = Packed Mode 128 110 = Reserved 111 = Reserved	00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = Reserved	0 = Normal 1 = PWRDWN	0 = 8× (48 kHz) 1 = 4× (96 kHz)	0

Table 15. DAC Control Register 2

Address	RD/WR	Reserved	DAC Mute					
			DAC3R	DAC3L	DAC2R	DAC2L	DAC1R	DAC1L
15, 14, 13, 12	**11**	**10, 9, 8, 7, 6**	**5**	**4**	**3**	**2**	**1**	**0**
0001	0	00000	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute

Table 16. DAC Volume Registers

Address	RD/WR	Reserved	Function
			Volume
15, 14, 13, 12	**11**	**10**	**9:0**
0010: DAC1L 0011: DAC1R 0100: DAC2L 0101: DAC2R 0110: DAC3L 0111: DAC3R	0	0	0 to 1023 in 1024 Linear Steps

Table 17. ADC Control Register 1

Address	RD/WR	Reserved	Function				
			Filter	Power-Down	Sample Rate	Left Gain	Right Gain
15, 14, 13, 12	**11**	**10, 9**	**8**	**7**	**6**	**5, 4, 3**	**2, 1, 0**
1100	0	00	0 = DC 1 = High Pass	0 = Normal 1 = PWRDWN	0 = 48 kHz 1 = 96 kHz	000 = 0 dB 001 = 3 dB 010 = 6 dB 011 = 9 dB 100 = 12 dB 101 = Reserved 110 = Reserved 111 = Reserved	000 = 0 dB 001 = 3 dB 010 = 6 dB 011 = 9 dB 100 = 12 dB 101 = Reserved 110 = Reserved 111 = Reserved

Table 18. ADC Control Register 2

Packed Mode: Eight channels are "packed" in ASDATA1 serial output. Packed Mode 128: Refer to Figure 5. Packed Mode 256: Refer to Figure 6. Packed Mode AUX: Refer to Figure 9 to Figure 11. Note that Packed AUX mode affects the entire chip, including the DAC serial mode.

Address	RD/WR	Reserved	Master/Slave AUX Mode	SOUT Mode	Word Width	ADC Mute			
						ADC2R	ADC2L	ADC1R	ADC1L
15, 14, 13, 12	**11**	**10**	**9**	**8, 7, 6**	**5, 4**	**3**	**2**	**1**	**0**
1101	0	0	0 = Slave 1 = Master	000 = I²S 001 = RJ 010 = DSP 011 = LJ 100 = Packed Mode 256 101 = Packed Mode 128 110 = Packed Mode AUX	00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = Reserved	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute

Table 19. ADC Control Register 3

When changing clock mode, other SPI bits that are written during the same SPI transaction may be lost. Therefore, it is recommended that these be set separately.

				Function					
Address	**RD/WR**	**Reserved**	**Clock Mode**	**Left Differential I/P Select**	**Right Differential I/P Select**	**Left MUX/PGA Enable**	**Left MUX I/P Select**	**Right MUX/PGA Enable**	**Right MUX I/P Select**
15, 14, 13, 12	**11**	**10, 9, 8**	**7, 6**	**5**	**4**	**3**	**2**	**1**	**0**
1110	0	000	00 = 256 × f_S 01 = 512 × f_S 10 = 768 × f_S	0 = Differential PGA Mode 1 = PGA/MUX Mode (Single-Ended Input)	0 = Differential PGA Mode 1 = PGA/MUX Mode (Single-Ended Input)	0 = Direct 1 = MUX/PGA	0 = I/P 0 1 = I/P 1	0 = Direct 1 = MUX/PGA	0 = I/P 0 1 = I/P 1

Table 20. ADC Peak Level Data Registers

			Peak Level Data (10 Bits)	
Address	**RD/WR**	**Reserved**	**6 Data Bits**	**4 Fixed Bits**
15, 14, 13, 12	**11**	**10**	**9:4**	**3:0**
1000 = ADC1L 1001 = ADC1R 1010 = ADC2L 1011 = ADC2R	1	0	000000 = 0.0 dBFS 000001 = –1.0 dBFS 000010 = –2.0 dBFS 000011 = –3.0 dBFS 111100 = –60 dBFS Min	0000 The 4 LSBs are always zero.

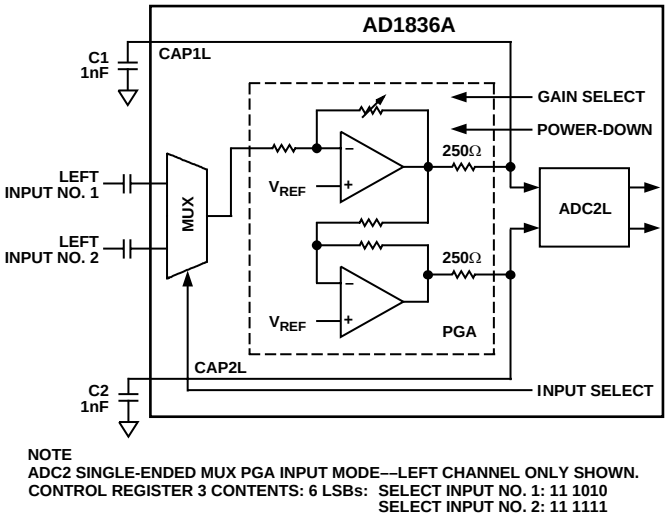


Figure 13. Single-Ended MUX/PGA Mode

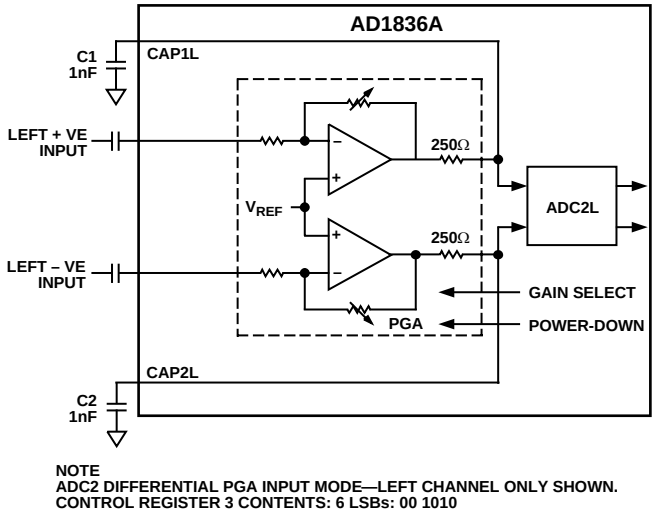


Figure 14. Differential PGA Mode

OUTLINE DIMENSIONS

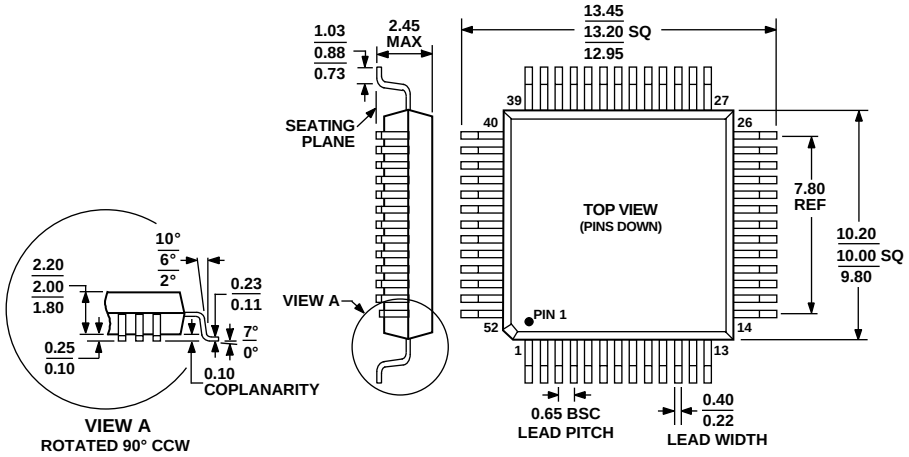


Figure 15. 52-Lead Plastic Quad Flat Package [MQFP]
(S-52-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Package	Package Description	Package Option
AD1836AASZ	–40°C to +85°C	52-Lead MQFP	S-52-1
AD1836AASZRL	–40°C to +85°C	52-Lead MQFP, 13" Tape and Reel	S-52-1
AD1836ACSZ	–40°C to +85°C	52-Lead MQFP	S-52-1

[1] Z = RoHS Compliant Part.

NOTES

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