18-Bit, 2 MSPS Precision, Differential SAR ADC

Known Good Die

AD4003-KGD

FEATURES

- **Throughput: 2 MSPS**
- **INL: ±1.0 LSB (±3.8 ppm) maximum**
- **Guaranteed 18-bit no missing codes**
- **Low power**
  - **9.5 mW at 2 MSPS, 4.9 mW at 1 MSPS, 2.4 mW at 500 kSPS (VDD only)**
  - **80 µW at 10 kSPS, 16 mW at 2 MSPS (total)**
- **SNR: 100.5 dB typical at 1 kHz, V_{REF} = 5 V; 99 dB typical at 100 kHz**
- **THD: −123 dB typical at 1 kHz, V_{REF} = 5 V; −100 dB typical at 100 kHz**
- **Ease of use features reduce system power and complexity**
  - **Input overvoltage clamp circuit**
  - **Reduced nonlinear input charge kickback**
  - **High-Z mode**
  - **Long acquisition phase**
  - **Input span compression**
  - **Fast conversion time allows low SPI clock rates**
  - **SPI-programmable modes, read/write capability, status word**
- **Differential analog input range: ±V_{REF}**
  - **0 V to V_{REF} with V_{REF} from 2.4 V to 5.1 V**
- **Single 1.8 V supply operation with 1.71 V to 5.5 V logic interface**
- **SAR architecture: no latency/pipeline delay, valid first conversion**
- **First conversion accurate**
- **Guaranteed operation: −40°C to +125°C**
- **SPI-/QSPI-/MICROWIRE-/DSP-compatible serial interface**
- **Ability to daisy chain multiple ADCs and busy indicator**

APPLICATIONS

- **Automatic test equipment**
- **Machine automation**
- **Medical equipment**
- **Battery-powered equipment**
- **Precision data acquisition systems**

GENERAL DESCRIPTION

The AD4003-KGD is a low noise, low power, high speed, 18-bit, precision successive approximation register (SAR) analog-to-digital converter (ADC). The AD4003-KGD offers a 2 MSPS throughput. The AD4003-KGD incorporates ease of use features that reduce signal chain power consumption and complexity, and enable higher channel density. The high-Z mode, coupled with a long acquisition phase, eliminates the need for a dedicated high power, high speed ADC driver. Eliminating this ADC driver broadens the range of low power, precision amplifiers that can drive this ADC directly, while still achieving optimum performance. The input span compression feature enables the ADC driver amplifier and the ADC to operate off common supply rails without a negative supply, yet preserves the full ADC code range. The low serial peripheral interface (SPI) clock rate requirement reduces the digital input/output power consumption, broadens processor options, and simplifies the task of sending data across digital isolation.

Operating from a 1.8 V supply, the AD4003-KGD has a ±V_{REF} fully differential input range, with V_{REF} ranging from 2.4 V to 5.1 V, and consumes 16 mW at 2 MSPS with a minimum SCK rate of 75 MHz in turbo mode. The AD4003-KGD achieves ±1.0 LSB integral nonlinearity (INL) error maximum and guarantees no missing codes at 18 bits with 100.5 dB typical signal-to-noise ratio (SNR) for 1 kHz inputs. The reference voltage is applied externally and can be set independently of the supply voltage.

The SPI-compatible, serial interface features seven modes, including the ability, using the SDI input, to daisy-chain several ADCs on a single 3-wire bus and provides an optional busy indicator. The AD4003-KGD uses a simple SPI interface for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, set to the host logic level. By using the VIO supply, the AD4003-KGD is compatible with 1.8 V, 2.5 V, 3 V, and 5 V logic.

Additional application and technical information can be found in the AD4003/AD4007/AD4011 data sheet. Known Good Die (KGD): these die are fully guaranteed to data sheet specifications.

FUNCTIONAL BLOCK DIAGRAM

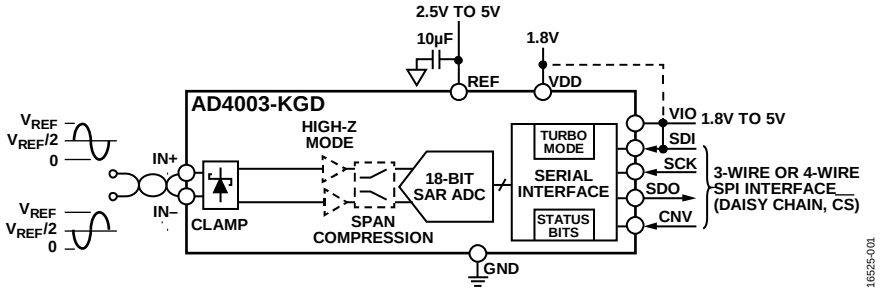

Figure 1.

Rev. 0 Document Feedback

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Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

6/2018—Revision 0: Initial Version

SPECIFICATIONS

VDD = 1.71 V to 1.89 V; VIO = 1.71 V to 5.5 V; V_{REF} = 5 V; all specifications T_{MIN} to T_{MAX}, high-Z mode disabled, span compression disabled, turbo mode enabled, and sampling frequency (f_S) = 2 MSPS, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	IN+ voltage (V_{IN+}) − IN− voltage (V_{IN-})	$-V_{REF}$		$+V_{REF}$	V
	Span compression enabled	$-V_{REF} \times 0.8$		$+V_{REF} \times 0.8$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to GND	−0.1		$V_{REF} + 0.1$	V
	Span compression enabled	$0.1 \times V_{REF}$		$0.9 \times V_{REF}$	V
Common-Mode Input Range		$V_{REF}/2 - 0.125$	$V_{REF}/2$	$V_{REF}/2 + 0.125$	V
Common-Mode Rejection Ratio (CMRR)	f_{IN} = 500 kHz		68		dB
Analog Input Current	Acquisition phase, T = 25°C		0.3		nA
	High-Z mode enabled, converting dc input at 2 MSPS		1		µA
THROUGHPUT					
Complete Cycle		500			ns
Conversion Time		270	290	320	ns
Acquisition Phase[1]		290			ns
Throughput Rate[2]		0		2	MSPS
Transient Response[3]			250		ns
DC ACCURACY					
No Missing Codes		18			Bits
Integral Nonlinearity Error		−1.0	±0.4	+1.0	LSB
		−3.8	±1.52	+3.8	ppm
Differential Nonlinearity (DNL) Error		−0.75	±0.3	+0.75	LSB
Transition Noise			0.8		LSB
Zero Error		−7		+7	LSB
Zero Error Drift[4]		−0.21		+0.21	ppm/°C
Gain Error		−26	±3	+26	LSB
Gain Error Drift[4]		−1.23		+1.23	ppm/°C
Power Supply Sensitivity	VDD = 1.8 V ± 5%		1.5		LSB
1/f Noise	Bandwidth = 0.1 Hz to 10 Hz		6		µV p-p
AC ACCURACY					
Dynamic Range			101		dB
Total RMS Noise			31.5		µV rms
f_{IN} = 1 kHz, −0.5 dBFS, V_{REF} = 5 V					
SNR		99	100.5		dB
Spurious-Free Dynamic Range (SFDR)			122		dB
Total Harmonic Distortion (THD)			−123		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)		98.5	100		dB
Oversampled Dynamic Range	Oversampling ratio (OSR) = 256, V_{REF} = 5 V		122		dB
f_{IN} = 1 kHz, −0.5 dBFS, V_{REF} = 2.5 V					
SNR		93.5	94.5		dB
SFDR			122		dB
THD			−119		dB
SINAD		93	94		dB
f_{IN} = 100 kHz, −0.5 dBFS, V_{REF} = 5 V					
SNR			99		dB
THD			−100		dB
SINAD			96.5		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{IN} = 400 kHz, −0.5 dBFS, V_{REF} = 5 V					
SNR			91.5		dB
THD			−94		dB
SINAD			90		dB
−3 dB Input Bandwidth			10		MHz
Aperture Delay			1		ns
Aperture Jitter			1		ps rms
REFERENCE					
Voltage Range, V_{REF}		2.4		5.1	V
Current	2 MSPS		1.1		mA
INPUT OVERVOLTAGE CLAMP					
IN+/IN− Current, I_{IN+}/I_{IN-}	V_{REF} = 5 V			50	mA
	V_{REF} = 2.5 V			50	mA
V_{IN+}/V_{IN-} at Maximum I_{IN+}/I_{IN-}	V_{REF} = 5 V		5.4		V
	V_{REF} = 2.5 V		3.1		V
V_{IN+}/V_{IN-} Clamp On/Off Threshold	V_{REF} = 5 V	5.25	5.4		V
	V_{REF} = 2.5 V	2.68	2.8		V
Deactivation Time			360		ns
REF Current at Maximum I_{IN+}/I_{IN-}	$V_{IN+}/V_{IN-} > V_{REF}$		100		µA
DIGITAL INPUTS					
Logic Levels					
Input Low Voltage, V_{IL}	VIO > 2.7 V	−0.3		+0.3 × VIO	V
	VIO ≤ 2.7 V	−0.3		+0.2 × VIO	V
Input High Voltage, V_{IH}	VIO > 2.7 V	0.7 × VIO		VIO + 0.3	V
	VIO ≤ 2.7 V	0.8 × VIO		VIO + 0.3	V
Input Low Current, I_{IL}		−1		+1	µA
Input High Current, I_{IH}		−1		+1	µA
Input Pin Capacitance			6		pF
DIGITAL OUTPUTS					
Data Format		Serial 18 bits, twos complement			
Pipeline Delay		Conversion results available immediately after completed conversion			
Output Low Voltage, V_{OL}	I_{SINK} = 500 µA			0.4	V
Output High Voltage, V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		1.71	1.8	1.89	V
VIO		1.71		5.5	V
Standby Current	VDD = 1.8 V, VIO = 1.8 V, T = 25°C		1.6		µA
Power Dissipation, P_{DISS}	VDD = 1.8 V, VIO = 1.8 V, V_{REF} = 5 V				
	10 kSPS, high-Z mode disabled		80		µW
	500 kSPS, high-Z mode disabled		4	4.7	mW
	1 MSPS, high-Z mode disabled		8	9.3	mW
	2 MSPS, high-Z mode disabled		16	18.5	mW
	500 kSPS, high-Z mode enabled		5	6.2	mW
	1 MSPS, high-Z mode enabled		10	12.3	mW
	2 MSPS, high-Z mode enabled		20	24.5	mW
VDD Only	500 kSPS, high-Z mode disabled		2.4		mW
	1 MSPS, high-Z mode disabled		4.9		mW
	2 MSPS, high-Z mode disabled		9.5		mW
REF Only	500 kSPS, high-Z mode disabled		1.4		mW
	1 MSPS, high-Z mode disabled		2.8		mW
	2 MSPS, high-Z mode disabled		5.5		mW
VIO Only	500 kSPS, high-Z mode disabled		0.1		mW
	1 MSPS, high-Z mode disabled		0.4		mW
	2 MSPS, high-Z mode disabled		1.0		mW

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Energy per Conversion			8		nJ/ sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+125	°C

[1] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS.
[2] A throughput rate of 2 MSPS can only be achieved with turbo mode enabled and a minimum SCK rate of 75 MHz. Refer to Table 4 for the maximum achievable throughput for different modes of operation.
[3] Transient response is the time required for the ADC to acquire a full-scale input step to ±1 LSB accuracy.
[4] The minimum and maximum values are guaranteed by characterization, but not production tested.

TIMING SPECIFICATIONS

VDD = 1.71 V to 1.89 V; VIO = 1.71 V to 5.5 V; V_{REF} = 5 V; all specifications T_{MIN} to T_{MAX}, high-Z mode disabled, span compression disabled, turbo mode enabled, and sampling frequency f_S = 2 MSPS.

Table 2. Digital Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION TIME—CNV RISING EDGE TO DATA AVAILABLE	t_{CONV}	270	290	320	ns
ACQUISITION PHASE[1]	t_{ACQ}	290			ns
TIME BETWEEN CONVERSIONS	t_{CYC}	500			ns
CNV PULSE WIDTH ($\overline{CS}$ MODE)[2]	t_{CNVH}	10			ns
SCK PERIOD ($\overline{CS}$ MODE)[3]	t_{SCK}				
VIO > 2.7 V		9.8			ns
VIO > 1.7 V		12.3			ns
SCK PERIOD (DAISY-CHAIN MODE)[4]	t_{SCK}				
VIO > 2.7 V		20			ns
VIO > 1.7 V		25			ns
SCK LOW TIME	t_{SCKL}	3			ns
SCK HIGH TIME	t_{SCKH}	3			ns
SCK FALLING EDGE TO DATA REMAINS VALID DELAY	t_{HSDO}	1.5			ns
SCK FALLING EDGE TO DATA VALID DELAY	t_{DSDO}				
VIO > 2.7 V				7.5	ns
VIO > 1.7 V				10.5	ns
CNV OR SDI LOW TO SDO D17 MOST SIGNIFICANT BIT (MSB) VALID DELAY ($\overline{CS}$ MODE)	t_{EN}				
VIO > 2.7 V				10	ns
VIO > 1.7 V				13	ns
CNV RISING EDGE TO FIRST SCK RISING EDGE DELAY	t_{QUIET1}	190			ns
LAST SCK FALLING EDGE TO CNV RISING EDGE DELAY[5]	t_{QUIET2}	60			ns
CNV OR SDI HIGH OR LAST SCK FALLING EDGE TO SDO HIGH IMPEDANCE ($\overline{CS}$ MODE)	t_{DIS}			20	ns
SDI VALID SETUP TIME FROM CNV RISING EDGE	$t_{SSDICNV}$	2			ns
SDI VALID HOLD TIME FROM CNV RISING EDGE ($\overline{CS}$ MODE)	$t_{HSDICNV}$	2			ns
SCK VALID HOLD TIME FROM CNV RISING EDGE (DAISY-CHAIN MODE)	$t_{HSCKCNV}$	12			ns
SDI VALID SETUP TIME FROM SCK RISING EDGE (DAISY-CHAIN MODE)	$t_{SSDISCK}$	2			ns
SDI VALID HOLD TIME FROM SCK RISING EDGE (DAISY-CHAIN MODE)	$t_{HSDISCK}$	2			ns

[1] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS.
[2] For turbo mode, t_{CNVH} must match the t_{QUIET1} minimum.
[3] A throughput rate of 2 MSPS can only be achieved with turbo mode enabled and a minimum SCK rate of 75 MHz. Refer to Table 4 for the maximum achievable throughput for different modes of operation.
[4] A 50% duty cycle is assumed for SCK.

Table 3. Register Read/Write Timing

Parameter	Symbol	Min	Typ	Max	Unit
READ/WRITE OPERATION					
CNV Pulse Width[1]	t_{CNVH}	10			ns
SCK Period	t_{SCK}				
VIO > 2.7 V		9.8			ns
VIO > 1.7 V		12.3			ns
SCK Low Time	t_{SCKL}	3			ns
SCK High Time	t_{SCKH}	3			ns
READ OPERATION					
CNV Low to SDO D17 MSB Valid Delay	t_{EN}				
VIO > 2.7 V				10	ns
VIO > 1.7 V				13	ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	1.5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO > 2.7 V				7.5	ns
VIO > 1.7 V				10.5	ns
CNV Rising Edge to SDO High Impedance	t_{DIS}			20	ns
CNV RISING EDGE TO FIRST SCK RISING EDGE DELAY	t_{QUIET1}	190			ns
WRITE OPERATION					
SDI Valid Setup Time from SCK Rising Edge	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Rising Edge	$t_{HSDISCK}$	2			ns
CNV Rising Edge to SCK Edge Hold Time	$t_{HCNVSCK}$	0			ns
CNV Falling Edge to SCK Active Edge Setup Time	$t_{SCNVSCK}$	6			ns

[1] For turbo mode, t_{CNVH} must match the t_{QUIET1} minimum.

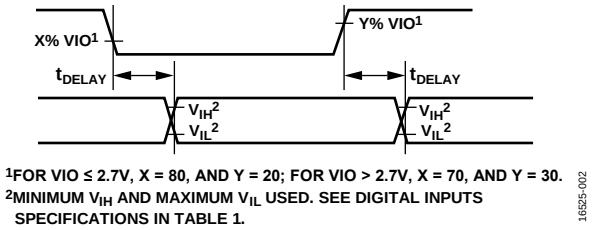

Figure 2. Voltage Levels for Timing

Table 4. Achievable Throughput for Different Modes of Operation

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
THROUGHPUT, $\overline{CS}$ MODE					
3-Wire and 4-Wire Turbo Mode	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			2	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			2	MSPS
3-Wire and 4-Wire Turbo Mode and Six Status Bits	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			2	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			1.78	MSPS
3-Wire and 4-Wire Mode	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			1.75	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			1.62	MSPS
3-Wire and 4-Wire Mode and Six Status Bits	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			1.59	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			1.44	MSPS

ABSOLUTE MAXIMUM RATINGS

Note that the input overvoltage clamp cannot sustain the overvoltage condition for an indefinite amount of time.

Table 5.

Parameter	Rating
Analog Inputs	
IN+, IN− to GND	−0.3 V to V_{REF} + 0.4 V or ± 130 mA[1]
Supply Voltage	
REF, VIO to GND	−0.3 V to +6.0 V
VDD to GND	−0.3 V to +2.1 V
VDD to VIO	−6 V to +2.4 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature	−40°C to +125°C
Junction Temperature	150°C
Electrostatic Discharge (ESD) Ratings	
Human Body Model (HBM)	4 kV
Machine Model	200 V
Field Induced Charged Device Model	1.25 kV

[1] Current condition tested over a 10 ms time interval.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

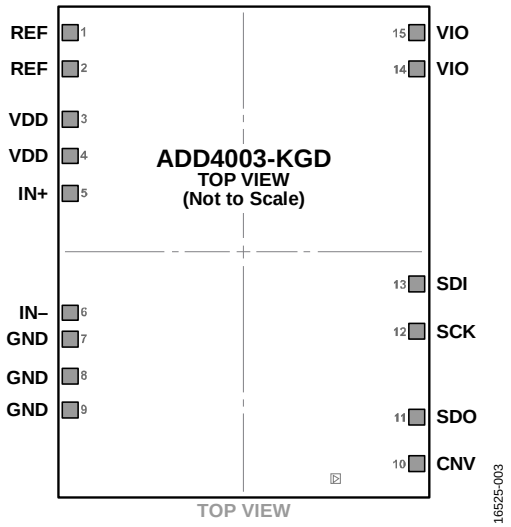

Figure 3. Pad Configuration

Table 6. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
1	−747.675	+996.855	REF	Reference Input Voltage. The VREF range is 2.4 V to 5.1 V. This pin is referred to the GND pin and must be decoupled closely to the GND pin with a 10 µF X7R ceramic capacitor.
2	−747.675	+823.805	REF	Reference Input Voltage. The VREF range is 2.4 V to 5.1 V. This pin is referred to the GND pin and must be decoupled closely to the GND pin with a 10 µF X7R ceramic capacitor.
3	−750	+607.545	VDD	1.8 V Power Supply. The VDD range is 1.71 V to 1.89 V. Bypass VDD to GND with a 0.1 µF ceramic capacitor.
4	−750	+442.715	VDD	1.8 V Power Supply. The VDD range is 1.71 V to 1.89 V. Bypass VDD to GND with a 0.1 µF ceramic capacitor.
5	−744.365	+272.19	IN+	Differential Positive Analog Input.
6	−744.365	−260.63	IN−	Differential Negative Analog Input.
7	−745.845	−382.055	GND	Power Supply Ground.
8	−745.845	−546.885	GND	Power Supply Ground.
9	−745.845	−702.35	GND	Power Supply Ground.
10	+747.78	−942.43	CNV	Convert Input. This input has multiple functions. On its leading edge, this input initiates the conversions and selects the interface mode of the device: daisy-chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In daisy-chain mode, the data is read when CNV is high.
11	+747.78	−733.54	SDO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
12	+747.78	−345.685	SCK	Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.
13	+747.78	−132.405	SDI	Serial Data Input. This input provides multiple features. This input selects the interface mode of the ADC as follows: daisy-chain mode is selected if SDI is low during the CNV rising edge. In daisy-chain mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 18 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled. With CNV low, the device can be programmed by clocking in a 16-bit word on SDI on the rising edge of SCK.
14	+747.675	+832.805	VIO	Input/Output Interface Digital Power. Nominally, this pin is at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). Bypass VIO to GND with a 0.1 µF ceramic capacitor.
15	+747.675	+996.855	VIO	Input/Output Interface Digital Power. Nominally, this pin is at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). Bypass VIO to GND with a 0.1 µF ceramic capacitor.

OUTLINE DIMENSIONS

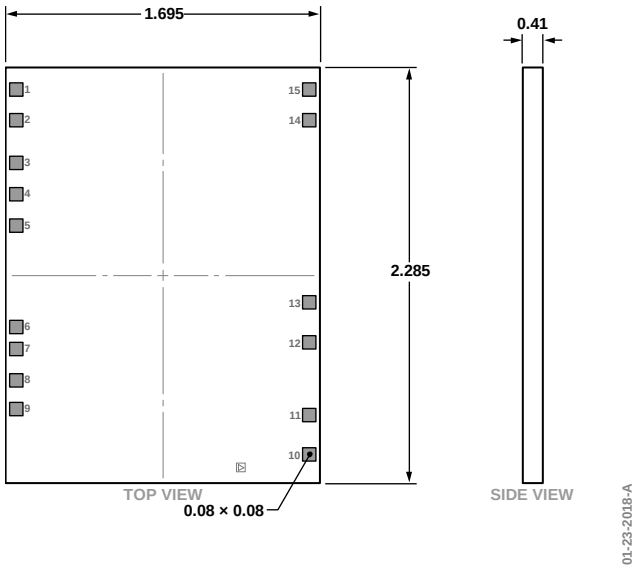

Figure 4. 15-Pad Bare Die [CHIP]
(C-15-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 7. Die Specifications

Parameter	Value	Unit
Chip Size	1695 × 2205	µm
Scribe Line Width	80 × 80	µm
Die Size	1695 × 2285	µm maximum
Thickness	410	µm
Bond Pad	70 × 70	µm maximum
Bond Pad Composition	AlCu (0.5%)	%
Backside	Standard assembly die attach	N/A
Passivation	Oxynitride	N/A

Table 8. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy adhesive
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Bond pin five first

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD4003-KGD-WP	−40°C to +125°C	15-Pad Bare Die [CHIP]	C-15-1

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