Single-Channel, 1024-Position, Digital Rheostat with I²C Interface and 50-TP Memory

AD5175

FEATURES

Single-channel, 1024-position resolution
10 kΩ nominal resistance
50-times programmable (50-TP) wiper memory
Rheostat mode temperature coefficient: 35 ppm/°C
2.7 V to 5.5 V single-supply operation
±2.5 V to ±2.75 V dual-supply operation for ac or bipolar operations
I²C-compatible interface
Wiper setting and memory readback
Power on refreshed from memory
Resistor tolerance stored in memory
Thin LFCSP, 10-lead, 3 mm × 3 mm × 0.8 mm package
Compact MSOP, 10-lead 3 mm × 4.9 mm × 1.1 mm package

APPLICATIONS

Mechanical rheostat replacements
Op-amp: variable gain control
Instrumentation: gain, offset adjustment
Programmable voltage to current conversions
Programmable filters, delays, time constants
Programmable power supply
Sensor calibration

FUNCTIONAL BLOCK DIAGRAM

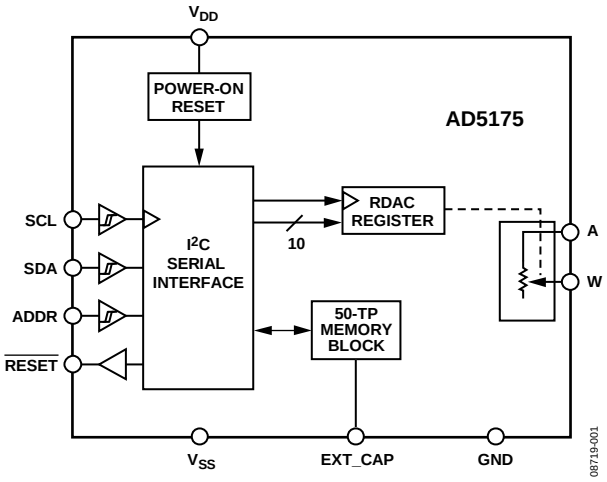

Figure 1.

GENERAL DESCRIPTION

The AD5175 is a single-channel, 1024-position digital rheostat that combines industry leading variable resistor performance with nonvolatile memory (NVM) in a compact package.

This device supports both dual-supply operation at ±2.5 V to ±2.75 V and single-supply operation at 2.7 V to 5.5 V, and offers 50-times programmable (50-TP) memory.

The AD5175 device wiper settings are controllable through the I²C–compatible digital interface. Unlimited adjustments are allowed before programming the resistance value into the 50-TP memory. The AD5175 does not require any external voltage supply to facilitate fuse blow and there are 50 opportunities for permanent programming. During 50-TP activation, a permanent blow fuse command freezes the resistance position (analogous to placing epoxy on a mechanical rheostat).

The AD5175 is available in a 3 mm × 3mm 10-lead LFCSP package and in a 10-lead MSOP package. The part is guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

Rev. A

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3/10—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V; −40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution			10			Bits
Resistor Integral Nonlinearity[2, 3]	R-INL	$\|V_{DD} - V_{SS}\|$ = 3.6 V to 5.5 V	−1		+1	LSB
		$\|V_{DD} - V_{SS}\|$ = 3.3 V to 3.6 V	−1		+1.5	LSB
		$\|V_{DD} - V_{SS}\|$ = 2.7 V to 3.3 V	−2.5		+2.5	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−1		+1	LSB
Nominal Resistor Tolerance				±15		%
Resistance Temperature Coefficient[4, 5]		Code = full scale		35		ppm/°C
Wiper Resistance		Code = zero scale		35	70	Ω
RESISTOR TERMINALS						
Terminal Voltage Range[4, 6]	V_{TERM}		V_{SS}		V_{DD}	V
Capacitance A[4]		f = 1 MHz, measured to GND, code = half scale		90		pF
Capacitance W[4]		f = 1 MHz, measured to GND, code = half scale		40		pF
Common-Mode Leakage Current[4]		$V_A = V_W$			50	nA
DIGITAL INPUTS						
Input Logic[4]						
High	V_{INH}		2.0			V
Low	V_{INL}				0.8	V
Input Current	I_{IN}			±1		µA
Input Capacitance[4]	C_{IN}			5		pF
DIGITAL OUTPUT						
Output Voltage[4]						
High	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{DD}	V_{DD} − 0.1			V
Low	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{DD}				
		V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V			0.4	V
		V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V			0.6	V
Tristate Leakage Current			−1		+1	µA
Output Capacitance[4]				5		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range			±2.5		±2.75	V
Supply Current						
Positive	I_{DD}				1	µA
Negative	I_{SS}		−1			µA
50-TP Store Current[4, 7]						
Positive	$I_{DD\_OTP\_STORE}$			4		mA
Negative	$I_{SS\_OTP\_STORE}$			−4		mA
50-TP Read Current[4, 8]						
Positive	$I_{DD\_OTP\_READ}$				500	µA
Negative	$I_{SS\_OTP\_READ}$		−500			µA
Power Dissipation[9]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND			5.5	µW
Power Supply Rejection Ratio[4]	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = ±5 V ± 10%	−50	−55		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[4, 10]						
Bandwidth		−3 dB, R_{AW} = 5 kΩ, Terminal W, see Figure 23		700		kHz
Total Harmonic Distortion		V_A = 1 V rms, f = 1 kHz, R_{AW} = 5 kΩ		−90		dB
Resistor Noise Density		R_{WB} = 5 kΩ, T_A = 25°C, f = 10 kHz		13		nV/√Hz

[1] Typical specifications represent average readings at 25°C, V_{DD} = 5 V, and V_{SS} = 0 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from the ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] The maximum current in each code is defined by $I_{AW} = (V_{DD} - 1)/R_{AW}$.
[4] Guaranteed by design and not subject to production test.
[5] See Figure 8 for more details.
[6] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[7] Different from operating current; the supply current for the fuse program lasts approximately 55 ms.
[8] Different from operating current; the supply current for the fuse read lasts approximately 500 ns.
[9] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
[10] All dynamic characteristics use V_{DD} = +2.5 V, V_{SS} = −2.5 V.

INTERFACE TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

		Limit at T_{MIN}, T_{MAX}			
Parameter	Conditions[1]	Min	Max	Unit	Description
f_{SCL}[2]	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	Serial clock frequency
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	t_{HIGH}, SCL high time
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	t_{LOW}, SCL low time
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	$t_{SU;DAT}$, data setup time
t_4	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	$t_{HD;DAT}$, data hold time
t_5	Standard mode	4.7		µs	$t_{SU;STA}$, set-up time for a repeated start condition
	Fast mode	0.6		µs	$t_{SU;STA}$, set-up time for a repeated start condition
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6		µs	$t_{HD;STA}$, hold time (repeated) start condition
	High speed mode	160		ns	$t_{HD;STA}$, hold time (repeated) start condition
t_7	Standard mode	4.7		µs	t_{BUF}, bus free time between a stop and a start condition
	Fast mode	1.3		µs	t_{BUF}, bus free time between a stop and a start condition
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	$t_{SU;STO}$, setup time for a stop condition
t_9	Standard mode		1000	ns	t_{RDA}, rise time of the SDA signal
	Fast mode		300	ns	t_{RDA}, rise time of the SDA signal
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of the SDA signal
	Fast mode		300	ns	t_{FDA}, fall time of the SDA signal
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of the SCL signal
	Fast mode		300	ns	t_{RCL}, rise time of the SCL signal
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of the SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	t_{RCL1}, rise time of the SCL signal after a repeated start condition and after an acknowledge bit
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of the SCL signal
	Fast mode		300	ns	t_{FCL}, fall time of the SCL signal
t_{13}	$\overline{\text{RESET}}$ pulse time	20		ns	Minimum $\overline{\text{RESET}}$ low time
t_{SP}[3]	Fast mode	0	50	ns	Pulse width of the spike is suppressed
t_{EXEC}[4, 5]		500		ns	Command execute time

Parameter	Conditions[1]	Limit at T_{MIN}, T_{MAX} Min	Max	Unit	Description
$t_{RDAC\_R\text{-}PERF}$			2	µs	RDAC register write command execute time (R-Perf mode)
t_{RDAC_NORMAL}			600	ns	RDAC register write command execute time (normal mode)
t_{MEMORY_READ}			6	µs	Memory readback execute time
$t_{MEMORY\_PROGRAM}$			350	ms	Memory program time
t_{RESET}			600	µs	Reset 50-TP restore time
$t_{POWER\text{-}UP}$[6]			2	ms	Power-on 50-TP restore time

[1] Maximum bus capacitance is limited to 400 pF.
[2] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.
[3] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns for fast mode.
[4] Refer to $t_{RDAC\_R\text{-}PERF}$ and t_{RDAC_NORMAL} for RDAC register write operations.
[5] Refer to t_{MEMORY_READ} and $t_{MEMORY\_PROGRAM}$ for memory commands operations.
[6] Maximum time after $V_{DD} - V_{SS}$ is equal to 2.5 V.

Shift Register and Timing Diagrams

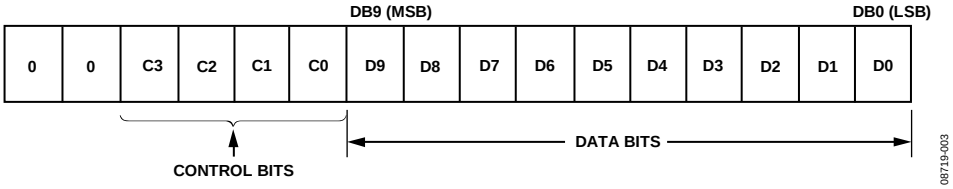

Figure 2. Shift Register Content

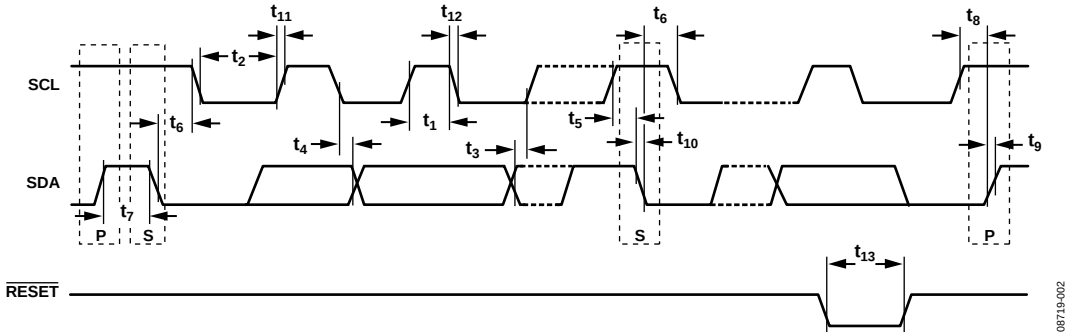

Figure 3. 2-Wire I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
V_{SS} to GND	+0.3 V to −7.0 V
V_{DD} to V_{SS}	7 V
V_A, V_W to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
Digital Input and Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
EXT_CAP to V_{SS}	7 V
I_A, I_W	
Pulsed[1]	
Frequency > 10 kHz	±6 mA/d[2]
Frequency ≤ 10 kHz	±6 mA/√d[2]
Continuous	±6 mA
Operating Temperature Range[3]	−40°C to +125°C
Maximum Junction Temperature (T_J Maximum)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A and W terminals at a given resistance.
[2] Pulse duty factor.
[3] Includes programming of 50-TP memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is defined by JEDEC specification JESD-51 and the value is dependent on the test board and test environment.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead LFCSP	50	3	°C/W
10-Lead MSOP	135[1]	N/A	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec airflow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

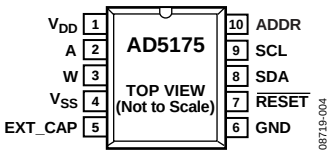

Figure 4. MSOP Pin Configuration

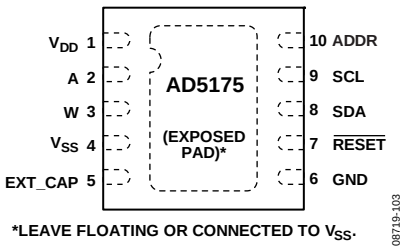

Figure 5. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
2	A	Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$.
3	W	Wiper Terminal of RDAC. $V_{SS} \le V_W \le V_{DD}$.
4	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
5	EXT_CAP	External Capacitor. Connect a 1 µF capacitor between EXT_CAP and V_{SS}. This capacitor must have a voltage rating of ≥7 V.
6	GND	Ground Pin, Logic Ground Reference.
7	$\overline{\text{RESET}}$	Hardware Reset Pin. Refreshes the RDAC register with the contents of the 50-TP memory register. Factory default loads midscale until the first 50-TP wiper memory location is programmed. $\overline{\text{RESET}}$ is active low. Tie $\overline{\text{RESET}}$ to V_{DD} if not used.
8	SDA	Serial Data Line. This pin is used in conjunction with the SCL line to clock data into or out of the 16-bit input registers. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
9	SCL	Serial Clock Line. This pin is used in conjunction with the SDA line to clock data into or out of the 16-bit input registers.
10	ADDR	Tristate Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 6).
EPAD	Exposed Pad	Leave floating or connected to V_{SS}

TYPICAL PERFORMANCE CHARACTERISTICS

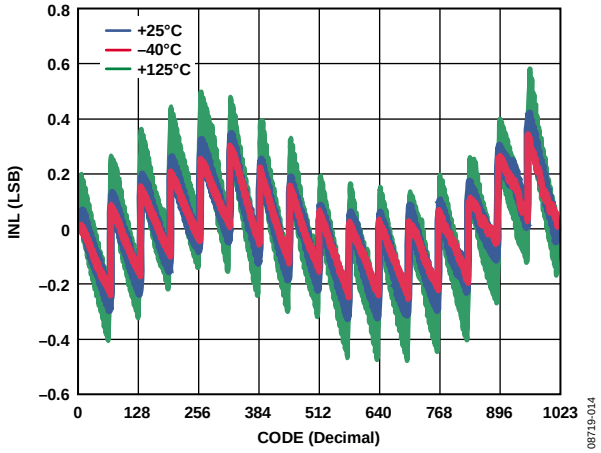

Figure 6. R-INL in Normal Mode vs. Code vs. Temperature

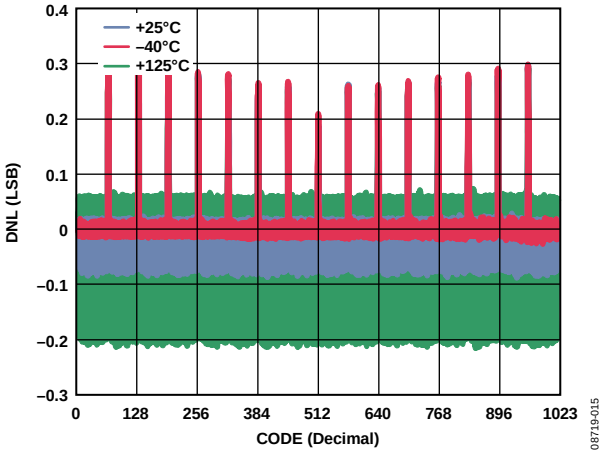

Figure 7. R-DNL in Normal Mode vs. Code vs. Temperature

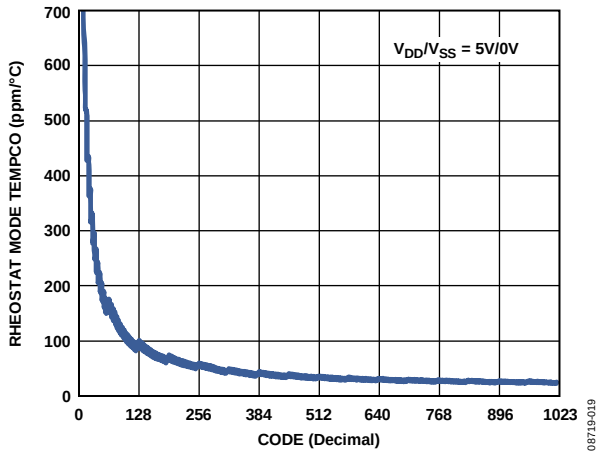

Figure 8. Tempco $\Delta R_{WA}/\Delta T$ vs. Code

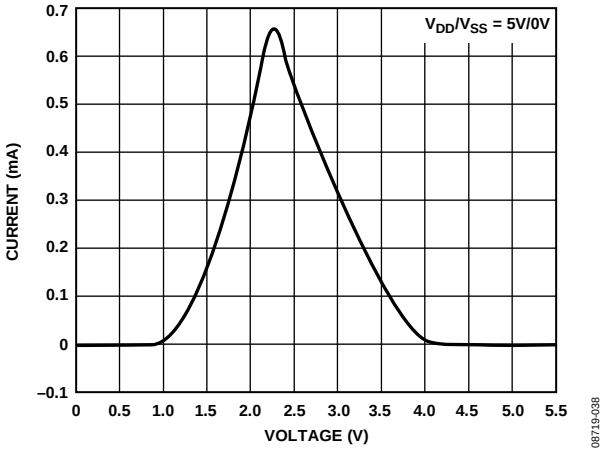

Figure 9. Supply Current (I_{DD}) vs. Digital Input Voltage

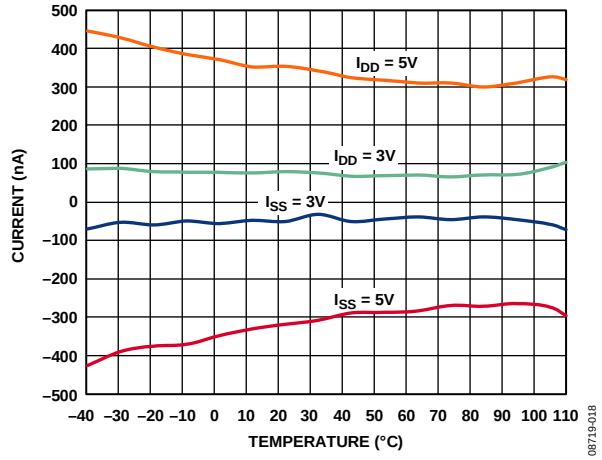

Figure 10. Supply Current (I_{DD}, I_{SS}) vs. Temperature

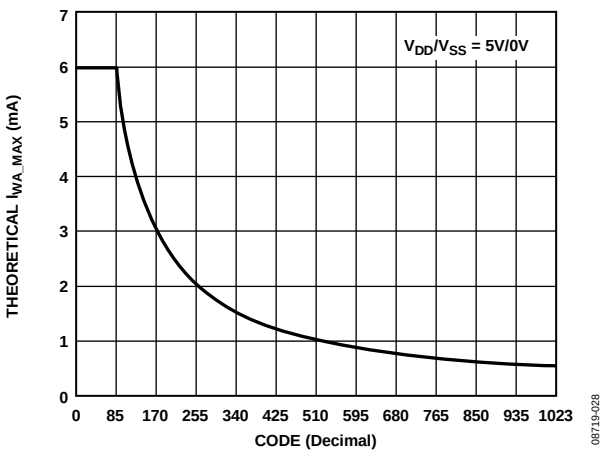

Figure 11. Theoretical Maximum Current vs. Code

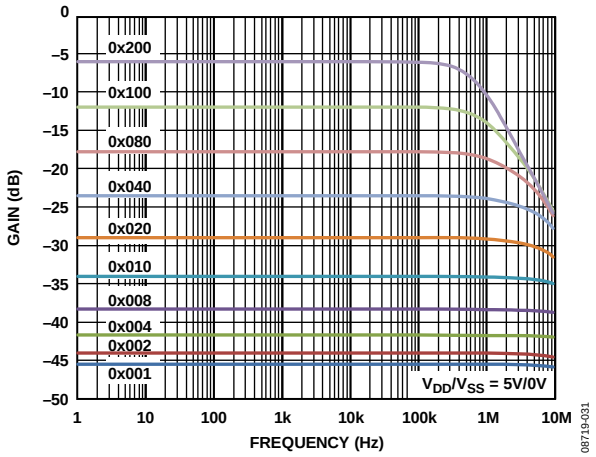

Figure 12. Bandwidth vs. Frequency vs. Code

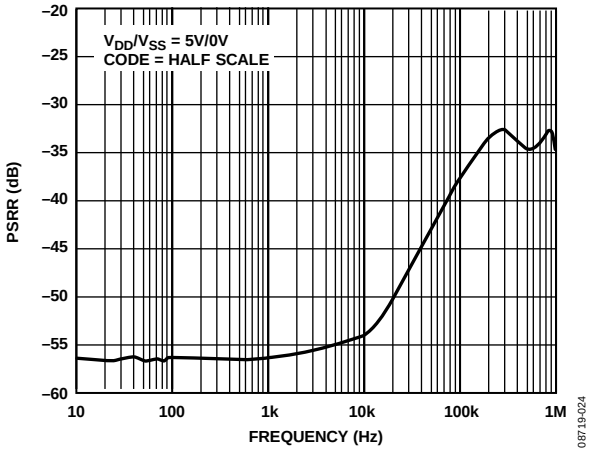

Figure 15. PSRR vs. Frequency

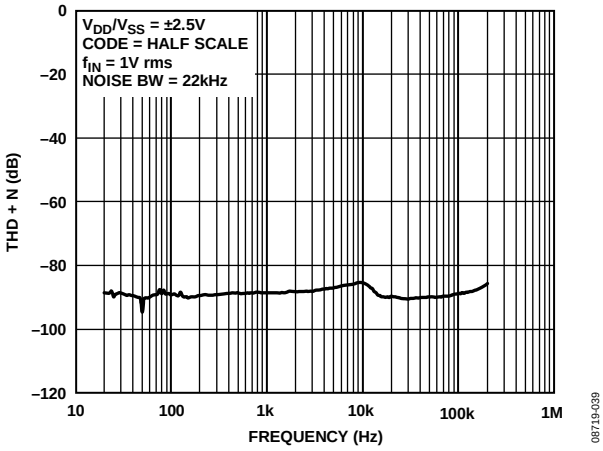

Figure 13. THD + N vs. Frequency

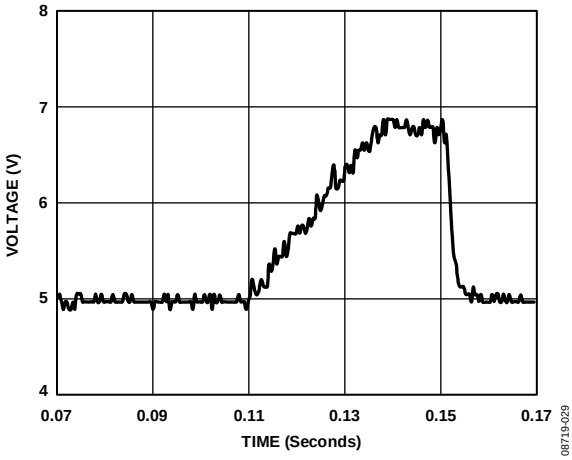

Figure 16. V_{EXT_CAP} Waveform While Writing Fuse

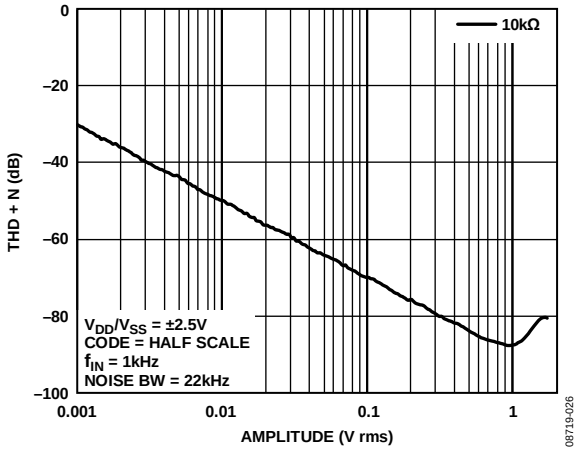

Figure 14. THD + N vs. Amplitude

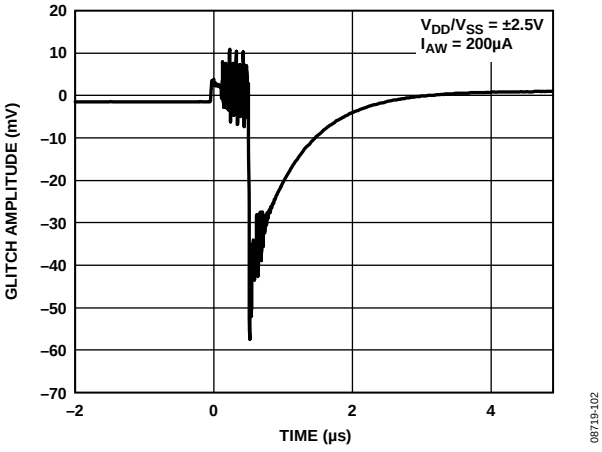

Figure 17. Maximum Glitch Energy

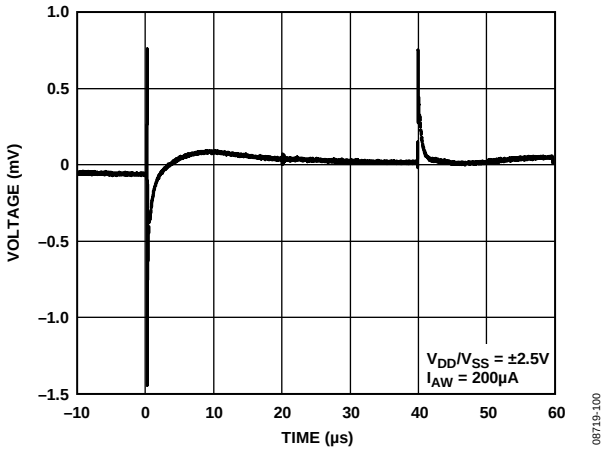

Figure 18. Digital Feedthrough

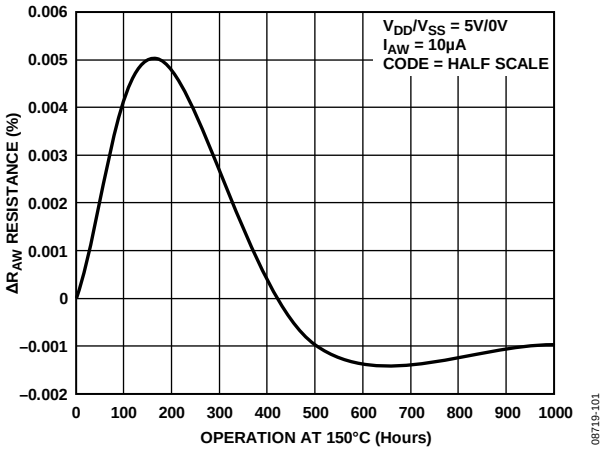

Figure 19. Long-Term Drift Accelerated Average by Burn-In

TEST CIRCUITS

Figure 20 to Figure 24 define the test conditions used in the Specifications section.

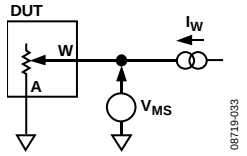

Figure 20. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

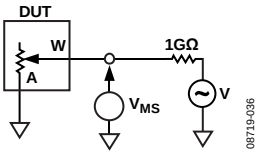

Figure 23. Gain vs. Frequency

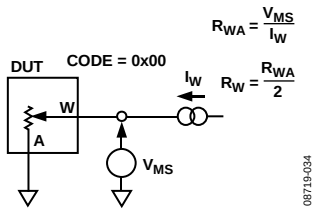

Figure 21. Wiper Resistance

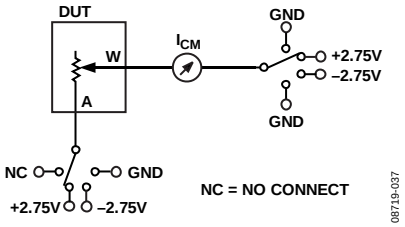

Figure 24. Common Leakage Current

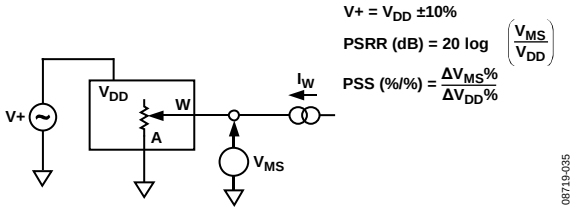

Figure 22. Power Supply Sensitivity (PSS, PSRR)

THEORY OF OPERATION

The AD5175 is designed to operate as a true variable resistor for analog signals within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The RDAC register contents determine the resistor wiper position. The RDAC register acts as a scratchpad register, which allows unlimited changes of resistance settings. The RDAC register can be programmed with any position setting using the I²C interface. When a desirable wiper position is found, this value can be stored in a 50-TP memory register. Thereafter, the wiper position is always restored to that position for subsequent power-up. The storing of 50-TP data takes approximately 350 ms; during this time, the AD5175 is locked and does not acknowledge any new command thereby preventing any changes from taking place. The acknowledge bit can be polled to verify that the fuse program command is complete.

SERIAL DATA INTERFACE

The AD5175 has a 2-wire I²C-compatible serial interface. It can be connected to an I²C bus as a slave device under the control of a master device; see Figure 3 for a timing diagram of a typical write sequence.

The AD5175 supports standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

The AD5175 has a 7-bit slave address. The five MSBs are 01011 and the two LSBs are determined by the state of the ADDR pin. The facility to make hardwired changes to ADDR allows the user to incorporate up to three of these devices on one bus, as outlined in Table 6.

The 2-wire serial bus protocol operates as follows: The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The next byte is the address byte, which consists of the 7-bit slave address and a R/$\overline{W}$ bit. The slave device corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.

Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse, that is, the SDA line remains high. The master then brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

SHIFT REGISTER

For the AD5175, the shift register is 16 bits wide, as shown in Figure 2. The 16-bit word consists of two unused bits, which should be set to 0, followed by four control bits and 10 RDAC data bits, and data is loaded MSB first (Bit D9). The four control bits determine the function of the software command (Table 7). Figure 25 shows a timing diagram of a typical AD5175 write sequence.

The command bits (Cx) control the operation of the digital potentiometer and the internal 50-TP memory. The data bits (Dx) are the values that are loaded into the decoded register.

Table 6. Device Address Selection

ADDR Pin	A1	A0	7-Bit I²C Device Address
GND	1	1	0101111
V_{DD}	0	0	0101100
NC (No Connection)[1]	1	0	0101110

[1] Not available in bipolar mode. $V_{SS} < 0$ V.

WRITE OPERATION

It is possible to write data for the RDAC register or the control register. When writing to the AD5175, the user must begin with a start command followed by an address byte ($R/\overline{W} = 0$), after which the AD5175 acknowledges that it is prepared to receive data by pulling SDA low.

Two bytes of data are then written to the RDAC, the most significant byte followed by the least significant byte; both of these data bytes are acknowledged by the AD5175. A stop condition follows. The write operations for the AD5175 are shown in Figure 25.

A repeated write function gives the user flexibility to update the device a number of times after addressing the part only once, as shown in Figure 26.

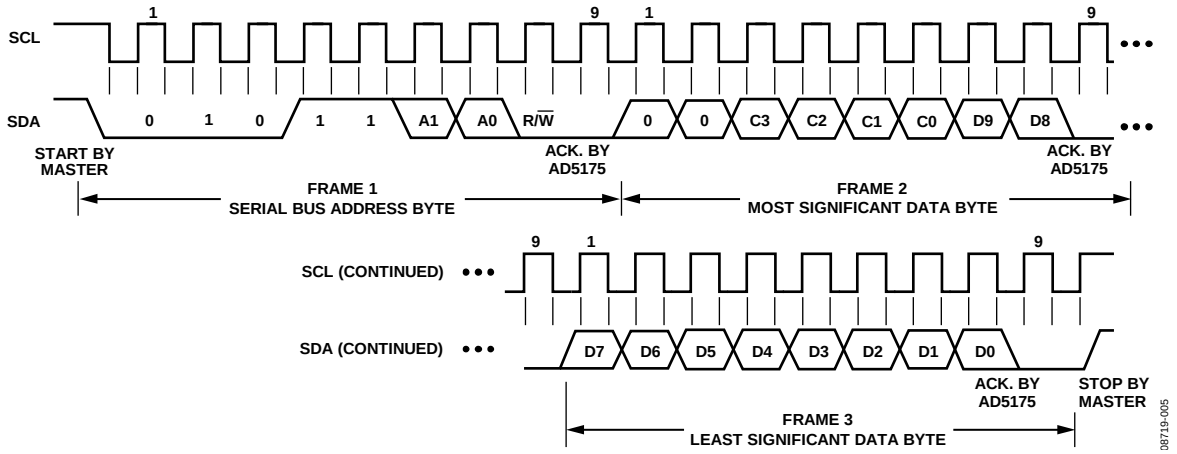

Figure 25. Write Command

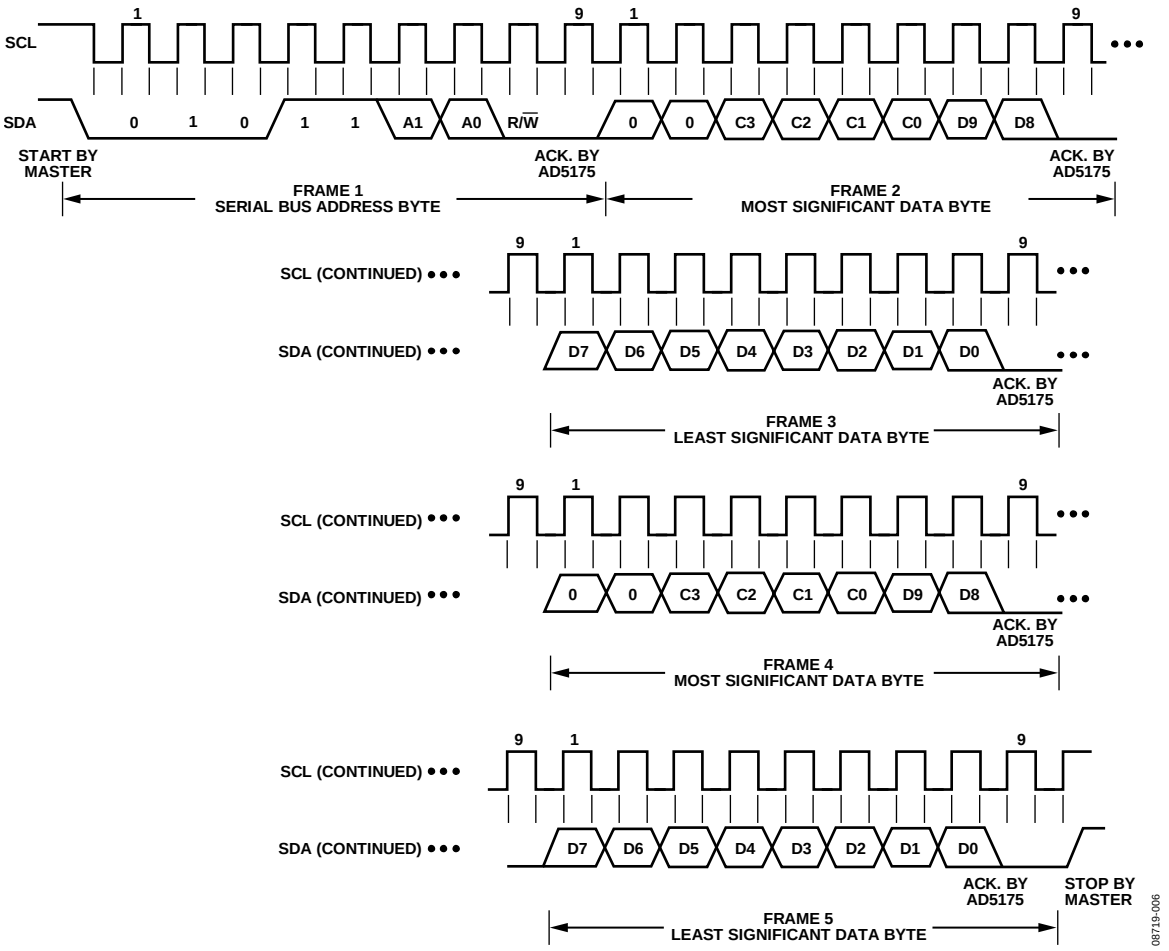

Figure 26. Multiple Write

READ OPERATION

When reading data back from the AD5175, the user must first issue a readback command to the device, this begins with a start command followed by an address byte ($R/\overline{W} = 0$), after which the AD5175 acknowledges that it is prepared to receive data by pulling SDA low.

Two bytes of data are then written to the AD5175, the most significant byte followed by the least significant byte; both of these data bytes are acknowledged by the AD5175. A stop condition follows. These bytes contain the read instruction, which enables readback of the RDAC register, 50-TP memory, or the control register. The user can then read back the data beginning with a start command followed by an address byte ($R/\overline{W} = 1$), after which the device acknowledges that it is prepared to transmit data by pulling SDA low. Two bytes of data are then read from the device, as shown in Figure 27. A stop condition follows. If the master does not acknowledge the first byte, the second byte is not transmitted by the AD5175.

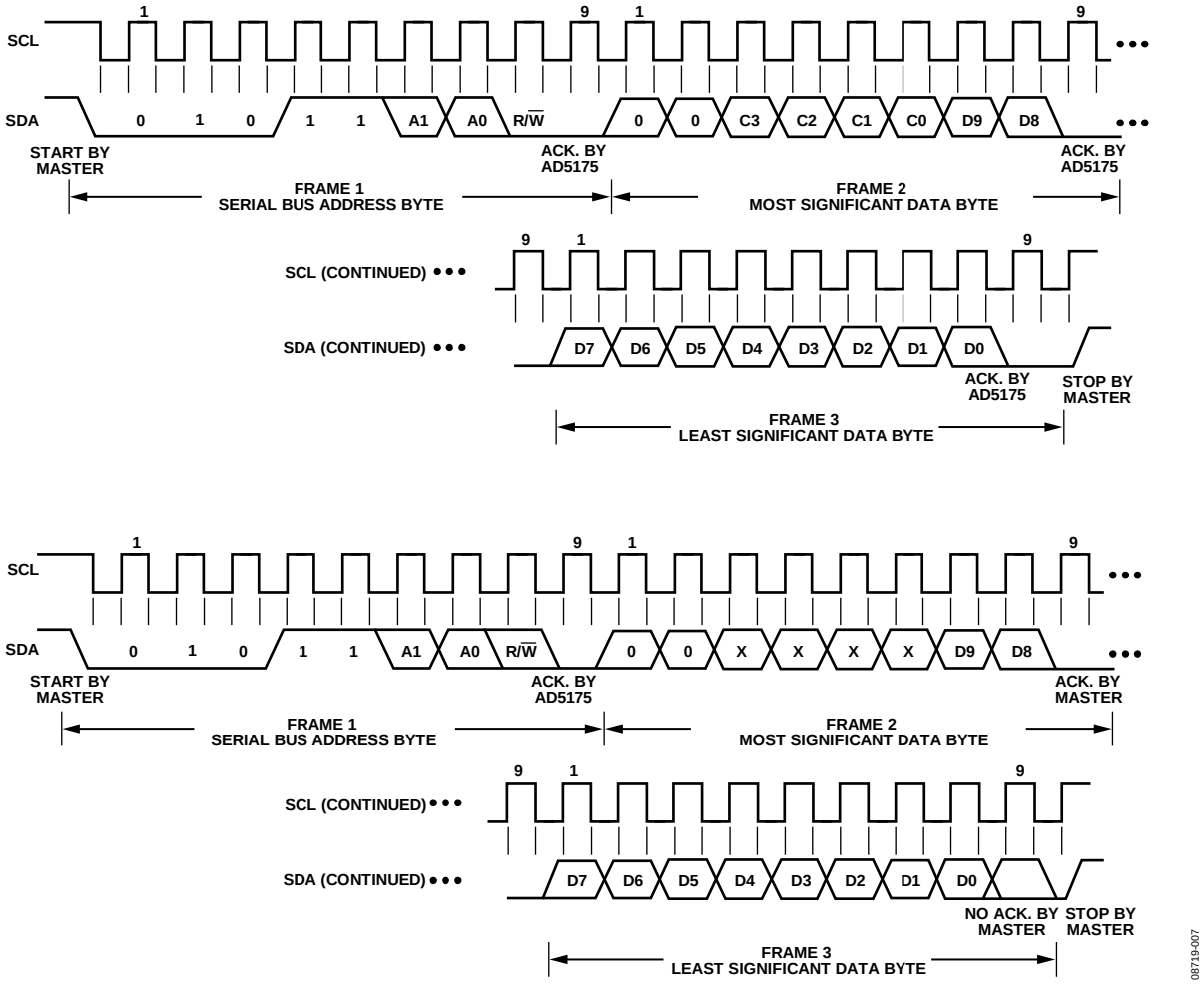

Figure 27. Read Command

RDAC REGISTER

The RDAC register directly controls the position of the digital rheostat wiper. For example, when the RDAC register is loaded with all 0s, the wiper is connected to Terminal A of the variable resistor. It is possible to both write to and read from the RDAC register using the I²C interface. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

50-TP MEMORY BLOCK

The AD5175 contains an array of 50-TP programmable memory registers, which allow the wiper position to be programmed up to 50 times. Table 11 shows the memory map. Command 3 in Table 7 programs the contents of the RDAC register to memory. The first address to be programmed is Location 0x01, see Table 11, and the AD5175 increments the 50-TP memory address for each subsequent program until the memory is full. Programming data to 50-TP consumes approximately 4 mA for 55 ms, and takes approximately 350 ms to complete, during which time the shift register is locked preventing any changes from taking place. Bit C2 of the control register in Table 10 can be polled to verify that the fuse program command was successful. No change in supply voltage is required to program the 50-TP memory; however, a 1 µF capacitor on the EXT_CAP pin is required as shown in Figure 29.

Prior to 50-TP activation, the AD5175 presets to midscale on power-up. It is possible to read back the contents of any of the 50-TP memory registers through the I²C interface by using Command 5 in Table 7. The lower six LSB bits, D0 to D5 of the data byte, select which memory location is to be read back. A binary encoded version address of the most recently programmed wiper memory location can be read back using Command 6 in Table 7. This can be used to monitor the spare memory status of the 50-TP memory block.

WRITE PROTECTION

On power-up, serial data input register write commands for both the RDAC register and the 50-TP memory registers are disabled. The RDAC write protect bit (Bit C1) of the control register (see Table 9 and Table 10), is set to 0 by default. This disables any change of the RDAC register content regardless of the software commands, except that the RDAC register can be refreshed from the 50-TP memory using the software reset, Command 4, or through the hardware by the $\overline{\text{RESET}}$ pin. To enable programming of the variable resistor wiper position (programming the RDAC register), the write protect bit (Bit C1) of the control register must first be programmed. This is accomplished by loading the serial data input register with Command 7 (see Table 7). To enable programming of the 50-TP memory block, Bit C0 of the control register, which is set to 0 by default, must first be set to 1.

Table 7. Command Operation Truth Table

Command Number	Command[DB13:DB10]				Data[DB9:DB0][1]										Operation
	C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP: do nothing.
1	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1	D	Write contents of serial register data to RDAC.
2	0	0	1	0	X	X	X	X	X	X	X	X	X	X	Read contents of RDAC wiper register.
3	0	0	1	1	X	X	X	X	X	X	X	X	X	X	Store wiper setting: store RDAC setting to 50-TP.
4	0	1	0	0	X	X	X	X	X	X	X	X	X	X	Software reset: refresh RDAC with the last 50-TP memory stored value.
5[2]	0	1	0	1	X	X	X	X	D5	D4	D3	D2	D1	D0	Read contents of 50-TP from the SDO output in the next frame.
6	0	1	1	0	X	X	X	X	X	X	X	X	X	X	Read address of the last 50-TP programmed memory location.
7[3]	0	1	1	1	X	X	X	X	X	X	X	X	D1	D0	Write contents of the serial register data to the control register.
8	1	0	0	0	X	X	X	X	X	X	X	X	X	X	Read contents of the control register.
9	1	0	0	1	X	X	X	X	X	X	X	X	X	D0	Software shutdown. D0 = 0; normal mode. D0 = 1; shutdown mode.

[1] X is don't care.
[2] See Table 11 for the 50-TP memory map.
[3] See Table 10 for bit details.

Table 8. Write and Read to RDAC and 50-TP Memory

DIN	SDO[1]	Action
0x1C03	0xXXXX	Enable update of wiper position and 50-TP memory contents through digital interface.
0x0500	0x1C03	Write 0x100 to the RDAC register, wiper moves to ¼ full-scale position.
0x0800	0x0500	Prepare data read from RDAC register.
0x0C00	0x100	Stores RDAC register content into 50-TP memory. 16-bit word appears out of SDO, where the last 10-bits contain the contents of the RDAC Register 0x100.
0x1800	0x0C00	Prepare data read of the last programmed 50-TP memory monitor location.
0x0000	0xXX19	NOP Instruction 0 sends a 16-bit word out of SDO, where the six LSBs (that is, the last 6 bits) contain the binary address of the last programmed 50-TP memory location, for example, 0x19 (see Table 11).
0x1419	0x0000	Prepares data read from Memory Location 0x19.
0x2000	0x0100	Prepare data read from the control register. Sends a 16-bit word out of SDO, where the last 10-bits contain the contents of Memory Location 0x19.
0x0000	0xXXXX	NOP Instruction 0 sends a 16-bit word out of SDO, where the last four bits contain the contents of the control register. If Bit C2 = 1, fuse program command successful.

[1] X is don't care.

Table 9. Control Register Bit Map

DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	C2	0	C1	C0

Table 10. Control Register Description

Bit Name	Description
C0	50-TP program enable 0 = 50-TP program disabled (default) 1 = enable device for 50-TP program
C1	RDAC register write protect 0 = wiper position frozen to value in OTP memory (default)[1] 1 = allow update of wiper position through a digital interface
C2	50-TP memory program success bit 0 = fuse program command unsuccessful (default) 1 = fuse program command successful

[1] Wiper position is frozen to the last value programmed in the 50-TP memory. Wiper freezes to midscale if 50-TP memory has not been previously programmed.

Table 11. Memory Map

	Data Byte[DB9:DB0][1]										
Command Number	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register Contents
5	X	X	X	0	0	0	0	0	0	0	Reserved
	X	X	X	0	0	0	0	0	0	1	1st programmed wiper location (0x01)
	X	X	X	0	0	0	0	0	1	0	2nd programmed wiper location (0x02)
	X	X	X	0	0	0	0	0	1	1	3rd programmed wiper location (0x03)
	X	X	X	0	0	0	0	1	0	0	4th programmed wiper location (0x04)
	…	…	…	…	…	…	…	…	…	…	…
	X	X	X	0	0	0	1	0	1	0	10th programmed wiper location (0xA)
	…	…	…	…	…	…	…	…	…	…	…
	X	X	X	0	0	1	0	1	0	0	20th programmed wiper location (0x14)
	…	…	…	…	…	…	…	…	…	…	…
	X	X	X	0	0	1	1	1	1	0	30th programmed wiper location (0x1E)
	…	…	…	…	…	…	…	…	…	…	…
	X	X	X	0	1	0	1	0	0	0	40th programmed wiper location (0x28)
	…	…	…	…	…	…	…	…	…	…	…
	X	X	X	0	1	1	0	0	1	0	50th programmed wiper location (0x32)
	…	…	…	…	…	…	…	…	…	…	…
	X	X	X	0	1	1	1	0	0	1	MSB resistance tolerance (0x39)
	X	X	X	0	1	1	1	0	1	0	LSB resistance tolerance (0x3A)

[1] X is don't care.

50-TP MEMORY WRITE-ACKNOWLEDGE POLLING

After each write operation to the 50-TP registers, an internal write cycle begins. The I²C interface of the device is disabled. To determine if the internal write cycle is complete and the I²C interface is enabled, interface polling can be executed. I²C interface polling can be conducted by sending a start condition followed by the slave address and the write bit. If the I²C interface responds with an acknowledge (ACK), the write cycle is complete and the interface is ready to proceed with further operations. Otherwise, I²C interface polling can be repeated until it completes.

RESET

The AD5175 can be reset through software by executing Command 4 (see Table 7) or through hardware on the low pulse of the $\overline{\text{RESET}}$ pin. The reset command loads the RDAC register with the contents of the most recently programmed 50-TP memory location. The RDAC register loads with midscale if no 50-TP memory location has been previously programmed. Tie $\overline{\text{RESET}}$ to V_{DD} if the $\overline{\text{RESET}}$ pin is not used.

SHUTDOWN MODE

The AD5175 can be shut down by executing the software shutdown command, Command 9 (see Table 7), and setting the LSB to 1. This feature places the RDAC in a zero-power-consumption state where Terminal A is disconnected from the wiper terminal. It is possible to execute any command from Table 7 while the AD5175 is in shutdown mode. The part can be taken out of shutdown mode by executing Command 9 and setting the LSB to 0, or by issuing a software or hardware reset.

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices, Inc., has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5175 employs a three-stage segmentation approach, as shown in Figure 28. The AD5175 wiper switch is designed with the transmission gate CMOS topology.

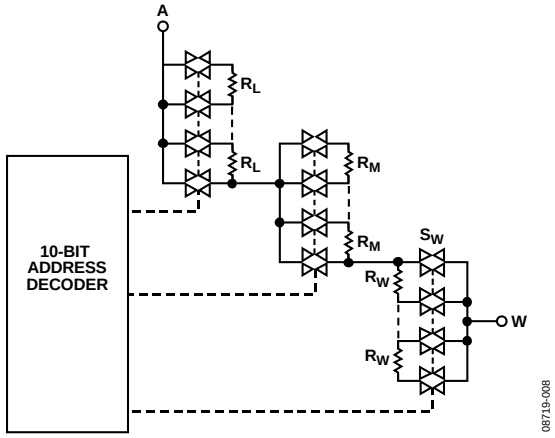

Figure 28. Simplified RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance between Terminal W and Terminal A, R_{WA}, is available in 10 kΩ and has 1024-tap points accessed by the wiper terminal. The 10-bit data in the RDAC latch is decoded to select one of the 1024 possible wiper settings. As a result, the general equation for determining the digitally programmed output resistance between the W terminal and A terminal is

$$R_{WA}(D) = \frac{D}{1024} \times R_{WA} \quad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 10-bit RDAC register.

R_{WA} is the end-to-end resistance.

In the zero-scale condition, a finite total wiper resistance of 120 Ω is present. Regardless of which setting the part is operating in, take care to limit the current between the A terminal to W terminal, and W terminal to B terminal, to the maximum continuous current of ±6 mA, or the pulse current specified in Table 3. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Calculate the Actual End-to-End Resistance

The resistance tolerance is stored in the internal memory during factory testing. The actual end-to-end resistance can, therefore, be calculated (which is valuable for calibration, tolerance matching, and precision applications).

The resistance tolerance in percentage is stored in fixed-point format, using a 16-bit sign magnitude binary. The sign bit(0 = negative and 1 = positive) and the integer part is located in Address 0x39, as shown in Table 11. Address 0x3A contains the fractional part, as shown in Table 12.

That is, if the data readback from Address 0x39 is 0000001010 and data from Address 0x3A is 0010110000, then the end-to-end resistance can be calculated as follows.

For Memory Location 0x39,

DB[9:8]: XX = don't care

DB[7]: 0 = negative

DB[6:0]: 0001010 = 10

For Memory Location 0x3A,

DB[9:8]: XX = don't care

DB[7:0]: 10110000 = $176 \times 2^{-8} = 0.6875$

Therefore, tolerance = −10.6875% and R_{WA} (1023)= 8.931 kΩ.

EXT_CAP CAPACITOR

A 1 µF capacitor to V_{SS} must be connected to the EXT_CAP pin (see Figure 29) on power-up and throughout the operation of the AD5175.

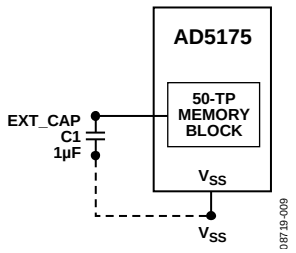

Figure 29. EXT_CAP Hardware Setup

TERMINAL VOLTAGE OPERATING RANGE

The positive V_{DD} and negative V_{SS} power supplies of the AD5175 define the boundary conditions for proper 2-terminal digital resistor operation. Supply signals present on Terminal A and Terminal W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 30).

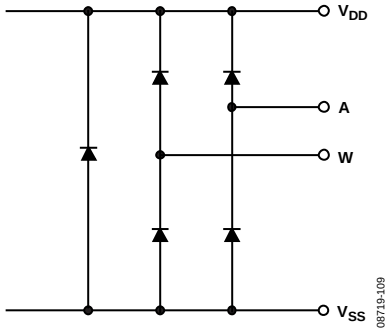

Figure 30. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5175 is primarily used as a digital ground reference. To minimize the digital ground bounce, join the AD5175 ground terminal remotely to the common ground. The digital input control signals to the AD5175 must be referenced to the device ground pin (GND) and satisfy the logic level defined in the Specifications section. An internal level shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD}, regardless of the digital input level.

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A and Terminal W (see Figure 30), it is important to power V_{DD}/V_{SS} first before applying any voltage to Terminal A and Terminal W; otherwise, the diode is forward-biased such that V_{DD}/V_{SS} are powered unintentionally. The ideal power-up sequence is V_{SS}, GND, V_{DD}, digital inputs, V_A, and V_W. The order of powering V_A, V_W, and digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

As soon as V_{DD} is powered, the power-on preset activates, which first sets the RDAC to midscale and then restores the last programmed 50-TP value to the RDAC register.

Table 12. End-to-End Resistance Tolerance Bytes

	Data Byte[1]									
Memory Map Address	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0x39	X	X	Sign	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0x3A	X	X	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

[1] X is don't care.

OUTLINE DIMENSIONS

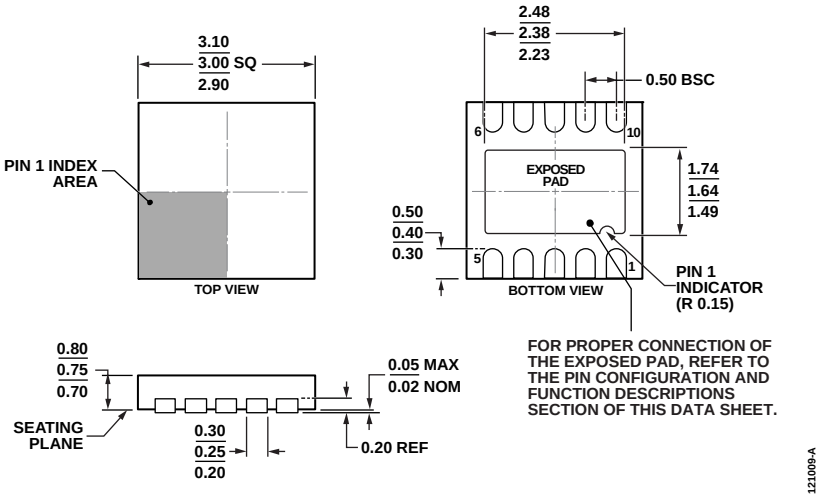

Figure 31. 10-Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

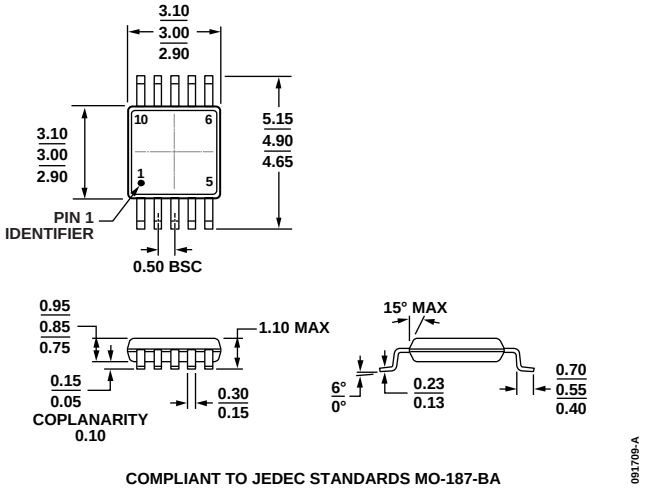

Figure 32. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AB} (kΩ)	Resolution	Temperature Range	Package Description	Package Option	Branding
AD5175BRMZ-10	10	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DDR
AD5175BRMZ-10-RL7	10	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DDR
AD5175BCPZ-10-RL7	10	1,024	−40°C to +125°C	10-Lead LFCSP_WD	CP-10-9	DEG

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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