32-Channel, 3 V/5 V, Single-Supply, 12-Bit, *dense*DAC

Data Sheet **AD5383**

FEATURES

- Guaranteed monotonic
- INL error: ±1 LSB max
- On-chip 1.25 V/2.5 V, 10 ppm/°C reference
- Temperature range: −40°C to +85°C
- Rail-to-rail output amplifier
- Power-down mode
- Package type: 100-lead LQFP (14 mm × 14 mm)
- User Interfaces
  - Parallel
  - Serial (SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible, featuring data readback)
  - I²C-compatible
- Robust 6.5 kV HBM and 2 kV FICDM ESD rating

INTEGRATED FUNCTIONS

- Channel monitor
- Simultaneous output update via $\overline{\text{LDAC}}$
- Clear function to user-programmable code
- Amplifier boost mode to optimize slew rate
- User programmable offset and gain adjust
- Toggle mode enables square wave generation
- Thermal monitor

APPLICATIONS

- Variable optical attenuators (VOA)
- Level setting (ATE)
- Optical microelectro-mechanical systems (MEMS)
- Control systems
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

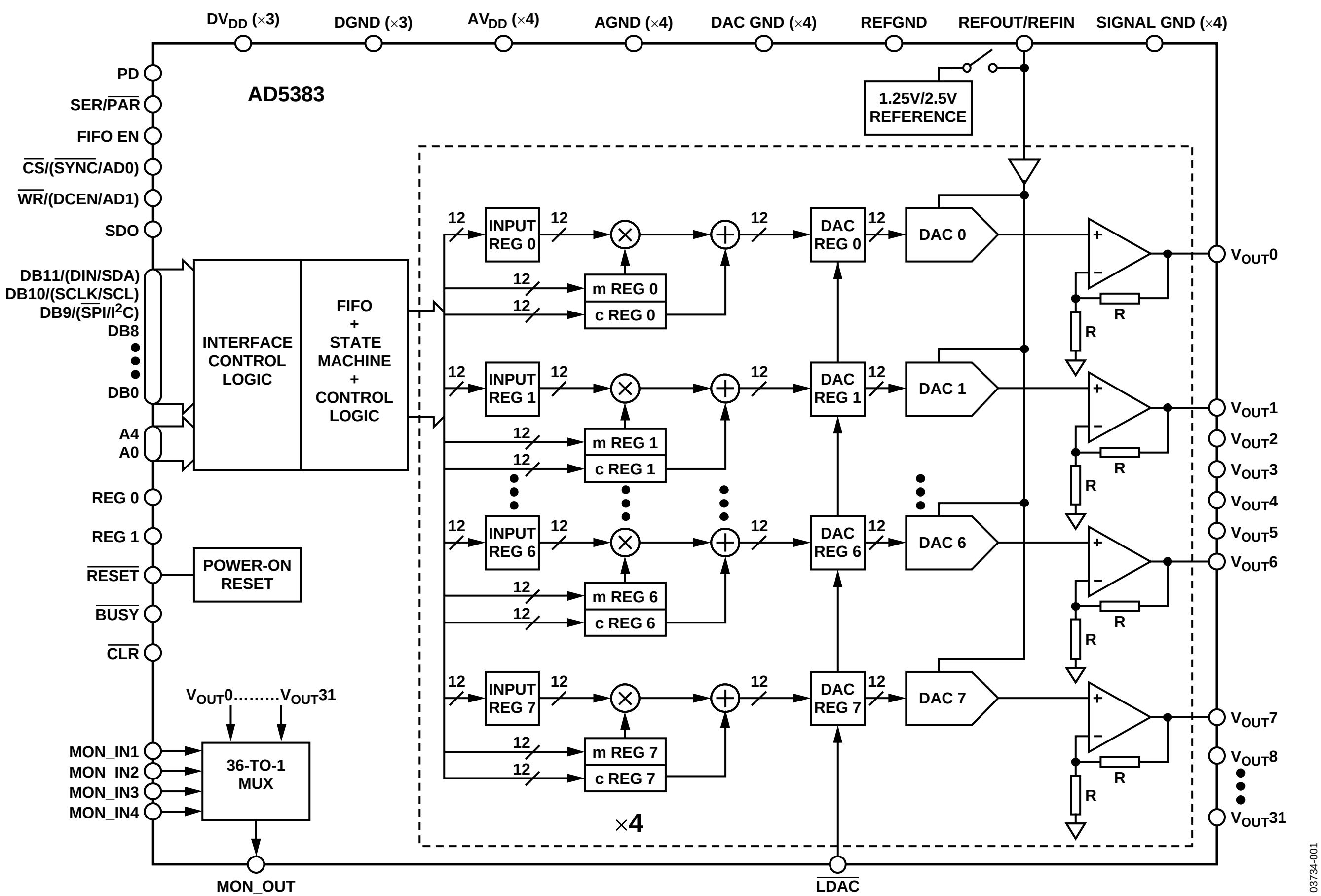


Figure 1.

Rev. D Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

5/14—Rev. C to Rev. D

10/12—Rev. B to Rev. C

4/10—Rev. A to Rev. B

3/05—Rev. 0 to Rev. A

5/04—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5383 is a complete, single-supply, 32-channel, 12-bit *dense*DAC® available in a 100-lead LQFP package. All 32 channels have an on-chip output amplifier with rail-to-rail operation. The AD5383 includes a programmable internal 1.25 V/2.5 V, 10 ppm/°C reference; an on-chip channel monitor function that multiplexes the analog outputs to a common MON_OUT pin for external monitoring; and an output amplifier boost mode that allows optimization of the amplifier slew rate. The AD5383 features

- Double-buffered parallel interface with a 20 ns $\overline{\text{WR}}$ pulse width.
- SPI-/QSPI-/MICROWIRE-/DSP-compatible serial interface with interface speeds in excess of 30 MHz.
- I^2C-compatible interface that supports a 400 kHz data transfer rate.

An input register followed by a DAC register provides double buffering, allowing the DAC outputs to be updated independently or simultaneously using the $\overline{\text{LDAC}}$ input.

Each channel has a programmable gain and offset adjust register that allows the user to fully calibrate any DAC channel. With boost off, power consumption is typically 0.25 mA/channel.

SPECIFICATIONS

AD5383-5 SPECIFICATIONS

AV_{DD} = 4.5 V to 5.5 V; DV_{DD} = 2.7 V to 5.5 V, AGND = DGND = 0 V; external REFIN = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	AD5383-5[1]	Unit	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	
Relative Accuracy[2] (INL)	±1	LSB max	
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic over temperature
Zero-Scale Error	4	mV max	
Offset Error	±4	mV max	Measured at Code 8 in the linear region
Offset Error TC	±5	µV/°C typ	
Gain Error	±0.05	% FSR max	At 25°C
	±0.06	% FSR max	T_{MIN} to T_{MAX}
Gain Temperature Coefficient[3]	2	ppm FSR/°C typ	
DC Crosstalk[3]	1	LSB max	
REFERENCE INPUT/OUTPUT			
Reference Input[3]			
Reference Input Voltage	2.5	V	±1% for specified performance, AV_{DD} = 2 × REFIN + 50 mV
DC Input Impedance	1	MΩ min	Typically 100 MΩ
Input Current	±1	µA max	Typically ±30 nA
Reference Range	1 to V_{DD}/2	V min/max	
Reference Output[4]			Enabled via CR8 in the AD5383 control register, CR10 selects the reference voltage
Output Voltage	2.495/2.505	V min/max	At ambient; optimized for 2.5 V operation; CR10 = 1
	1.22/1.28	V min/max	1.25 V reference selected; CR10 = 0
Reference TC	±10	ppm/C	Temperature range: 25°C to 85°C
	±15	ppm/C	Temperature range: −40°C to +85°C
OUTPUT CHARACTERISTICS[3]			
Output Voltage Range[2]	0/AV_{DD}	V min/max	
Short-Circuit Current	40	mA max	
Load Current	±1	mA max	
Capacitive Load Stability			
R_L = ∞	200	pF max	
R_L = 5 kΩ	1000	pF max	
DC Output Impedance	0.6	Ω max	
MONITOR PIN			
Output Impedance	1	kΩ typ	
Three-State Leakage Current	100	nA typ	
LOGIC INPUTS (EXCEPT SDA/SCL)[3]			DV_{DD} = 2.7 V to 5.5 V
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage			
DV_{DD} > 3.6 V	0.8	V max	
DV_{DD} ≤ 3.6 V	0.6	V max	
Input Current	±1	µA max	Total for all pins; T_A = T_{MIN} to T_{MAX}
Pin Capacitance	10	pF max	

Parameter	AD5383-5[1]	Unit	Test Conditions/Comments
LOGIC INPUTS (SDA, SCL ONLY)			
V_{IH}, Input High Voltage	0.7 × DV_{DD}	V min	SMBus compatible at DV_{DD} < 3.6 V
V_{IL}, Input Low Voltage	0.3 × DV_{DD}	V max	SMBus compatible at DV_{DD} < 3.6 V
I_{IN}, Input Leakage Current	±1	µA max	
V_{HYST}, Input Hysteresis	0.05 × DV_{DD}	V min	
C_{IN}, Input Capacitance	8	pF typ	
Glitch Rejection	50	ns max	Input filtering suppresses noise spikes of less than 50 ns
LOGIC OUTPUTS ($\overline{BUSY}$, SDO)[3]			
V_{OL}, Output Low Voltage	0.4	V max	DV_{DD} = 5 V ± 10%, sinking 200 µA
V_{OH}, Output High Voltage	DV_{DD} − 1	V min	DV_{DD} = 5 V ± 10%, sourcing 200 µA
V_{OL}, Output Low Voltage	0.4	V max	DV_{DD} = 2.7 V to 3.6 V, sinking 200 µA
V_{OH}, Output High Voltage	DV_{DD} − 0.5	V min	DV_{DD} = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current	±1	µA max	SDO only
High Impedance Output Capacitance	5	pF typ	SDO only
LOGIC OUTPUT (SDA)[3]			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 3 mA
	0.6	V max	I_{SINK} = 6 mA
Three-State Leakage Current	±1	µA max	
Three-State Output Capacitance	8	pF typ	
POWER REQUIREMENTS			
AV_{DD}	4.5/5.5	V min/max	
DV_{DD}	2.7/5.5	V min/max	
Power Supply Sensitivity[3]			
ΔMidscale/ΔAV_{DD}	−85	dB typ	
AI_{DD}	0.375	mA/channel max	Outputs unloaded, boost off; 0.25 mA/channel typ
	0.475	mA/channel max	Outputs unloaded, boost on; 0.325 mA/channel typ
DI_{DD}	1	mA max	V_{IH} = DV_{DD}, V_{IL} = DGND
AI_{DD} (Power-Down)	20	µA max	Typically 200 nA
DI_{DD} (Power-Down)	20	µA max	Typically 3 µA
Power Dissipation	65	mW max	Outputs unloaded, boost off, AV_{DD} = DV_{DD} = 5 V

[1] AD5383-5 is calibrated using an external 2.5 V reference. Temperature range for all versions: −40°C to +85°C.
[2] Accuracy guaranteed from V_{OUT} = 10 mV to AV_{DD} − 50 mV.
[3] Guaranteed by characterization, not production tested.
[4] Default on the AD5383-5 is 2.5 V. Programmable to 1.25 V via CR10 in the AD5383 control register; operating the AD5383-5 with a 1.25 V reference leads to degraded accuracy specifications.

AD5383-3 SPECIFICATIONS

AV_{DD} = 2.7 V to 3.6 V; DV_{DD} = 2.7 V to 5.5 V, AGND = DGND = 0 V; external REFIN = 1.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	AD5383-3[1]	Unit	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	
Relative Accuracy[2] (INL)	±1	LSB max	
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic over temperature
Zero-Scale Error	4	mV max	
Offset Error	±4	mV max	Measured at Code 32 in the linear region
Offset Error TC	±5	µV/°C typ	
Gain Error	±0.05	% FSR max	At 25°C
	±0.1	% FSR max	T_{MIN} to T_{MAX}
Gain Temperature Coefficient[3]	2	ppm FSR/°C typ	
DC Crosstalk[3]	1	LSB max	
REFERENCE INPUT/OUTPUT			
Reference Input[3]			
Reference Input Voltage	1.25	V	±1% for specified performance
DC Input Impedance	1	MΩ min	Typically 100 MΩ
Input Current	±1	µA max	Typically ±30 nA
Reference Range	1 to AV_{DD}/2	V min/max	
Reference Output[4]			Enabled via CR8 in the AD5383 control register, CR10 selects the reference voltage
Output Voltage	1.245/1.255	V min/max	At ambient; optimized for 1.25 V operation; CR10 = 0
	2.47/2.53	V min/max	2.5 V reference enabled; CR10 = 1
Reference TC	±10	ppm/°C max	Temperature range: +25°C to +85°C
	±15	ppm/°C max	Temperature range: −40°C to +85°C
OUTPUT CHARACTERISTICS[3]			
Output Voltage Range[2]	0/AV_{DD}	V min/max	
Short-Circuit Current	40	mA max	
Load Current	±1	mA max	
Capacitive Load Stability			
R_L = ∞	200	pF max	
R_L = 5 kΩ	1000	pF max	
DC Output Impedance	0.6	Ω max	
MONITOR PIN			
Output Impedance	1	kΩ typ	
Three-State Leakage Current	100	nA typ	
LOGIC INPUTS (EXCEPT SDA/SCL)[3]			DV_{DD} = 2.7 V to 3.6 V
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage			
DVDD > 3.6 V	0.8	V max	
DVDD ≤ 3.6 V	0.6	V max	
Input Current	±1	µA max	Total for all pins; T_A = T_{MIN} to T_{MAX}
Pin Capacitance	10	pF max	
LOGIC INPUTS (SDA, SCL ONLY)			
V_{IH}, Input High Voltage	0.7 × DV_{DD}	V min	SMBus-compatible at DV_{DD} < 3.6 V
V_{IL}, Input Low Voltage	0.3 × DV_{DD}	V max	SMBus-compatible at DV_{DD} < 3.6 V
I_{IN}, Input Leakage Current	±1	µA max	
V_{HYST}, Input Hysteresis	0.05 × DV_{DD}	V min	
C_{IN}, Input Capacitance	8	pF typ	
Glitch Rejection	50	ns max	Input filtering suppresses noise spikes of less than 50 ns

Parameter	AD5383-3[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS (BUSY, SDO)[3]			
V_{OL}, Output Low Voltage	0.4	V max	Sinking 200 µA
V_{OH}, Output High Voltage	DV_{DD} – 0.5	V min	Sourcing 200 µA
High Impedance Leakage Current	±1	µA max	SDO only
High Impedance Output Capacitance	5	pF typ	SDO only
LOGIC OUTPUT (SDA)[3]			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 3 mA
	0.6	V max	I_{SINK} = 6 mA
Three-State Leakage Current	±1	µA max	
Three-State Output Capacitance	8	pF typ	
POWER REQUIREMENTS			
AV_{DD}	2.7/3.6	V min/max	
DV_{DD}	2.7/5.5	V min/max	
Power Supply Sensitivity[3]			
ΔMidscale/ΔAV_{DD}	−85	dB typ	
AI_{DD}	0.375	mA/channel max	Outputs unloaded, boost off; 0.25 mA/channel typ
	0.475	mA/channel max	Outputs unloaded, boost on; 0.325 mA/channel typ
DI_{DD}	1	mA max	$V_{IH} = DV_{DD}$, V_{IL} = DGND.
AI_{DD} (Power-Down)	20	µA max	Typically 200 nA
DI_{DD} (Power-Down)	20	µA max	Typically 1 µA
Power Dissipation	39	mW max	Outputs unloaded, boost off; $AV_{DD} = DV_{DD}$ = 3 V

[1] AD5383-3 is calibrated using an external 1.25 V reference. Temperature range is −40°C to +85°C.
[2] Accuracy guaranteed from V_{OUT} = 10 mV to AV_{DD} − 50 mV.
[3] Guaranteed by characterization, not production tested.
[4] Default on the AD5383-3 is 1.25 V. Programmable to 2.5 V via CR10 in the AD5383 control register; operating the AD5383-3 with a 2.5 V reference leads to degraded accuracy specifications and limited input code range.

AC CHARACTERISTICS[1]

AV_{DD} = 4.5 V to 5.5 V or 2.7 V to 3.6 V; DV_{DD} = 2.7 V to 5.5 V; AGND = DGND = 0 V.

Table 3.

Parameter	All	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time[2]			¼ scale to ¾ scale change settling to ±1 LSB
	3	µs typ	Boost mode off, CR9 = 0
	8	µs max	Boost mode off, CR9 = 0
Slew Rate[2]	1.5	V/µs typ	Boost mode off, CR9 = 0
	2.5	V/µs typ	Boost mode on, CR9 = 1
Digital-to-Analog Glitch Energy	12	nV-s typ	
Glitch Impulse Peak Amplitude	15	mV typ	
DAC-to-DAC Crosstalk	1	nV-s typ	See Terminology section
Digital Crosstalk	0.8	nV-s typ	
Digital Feedthrough	0.1	nV-s typ	Effect of input bus activity on DAC output under test
Output Noise 0.1 Hz to 10 Hz	15	µV p-p typ	External reference, midscale loaded to DAC
	40	µV p-p typ	Internal reference, midscale loaded to DAC
Output Noise Spectral Density			
At 1 kHz	150	nV/√Hz typ	
At 10 kHz	100	nV/√Hz typ	

[1] Guaranteed by design and characterization, not production tested.
[2] The slew rate can be programmed via the current boost control bit (CR9) in the AD5383 control register.

TIMING CHARACTERISTICS

SERIAL INTERFACE TIMING

DV_{DD} = 2.7 V to 5.5 V; AV_{DD} = 4.5 V to 5.5 V or 2.7 V to 3.6 V; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5[4]	13	ns min	24th SCLK falling edge to $\overline{SYNC}$ falling edge
t_6[4]	33	ns min	Minimum $\overline{SYNC}$ low time
t_7	10	ns min	Minimum $\overline{SYNC}$ high time
t_{7A}	140	ns min	Minimum $\overline{SYNC}$ high time in readback mode
t_8	5	ns min	Data setup time
t_9	4.5	ns min	Data hold time
t_{10}[4]	36	ns max	24th SCLK falling edge to $\overline{BUSY}$ falling edge
t_{11}	670	ns max	$\overline{BUSY}$ pulse width low (single channel update)
t_{12}[4]	20	ns min	24th SCLK falling edge to $\overline{LDAC}$ falling edge
t_{13}	20	ns min	$\overline{LDAC}$ pulse width low
t_{14}	100/2000	ns min/max	$\overline{BUSY}$ rising edge to DAC output response time
t_{15}	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LDAC}$ falling edge
t_{16}	100/2000	ns min/max	$\overline{LDAC}$ falling edge to DAC output response time
t_{17}	3	µs typ	DAC output settling time; boost mode off
t_{18}	20	ns min	$\overline{CLR}$ pulse width low
t_{19}	40	µs max	$\overline{CLR}$ pulse activation time
t_{20}[5]	30	ns max	SCLK rising edge to SDO valid
t_{21}[5]	5	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_{22}[5]	8	ns min	$\overline{SYNC}$ rising edge to SCLK rising edge
t_{23}	20	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of V_{CC}) and are timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, Figure 4, and Figure 5.
[4] Standalone mode only.
[5] Daisy-chain mode only.

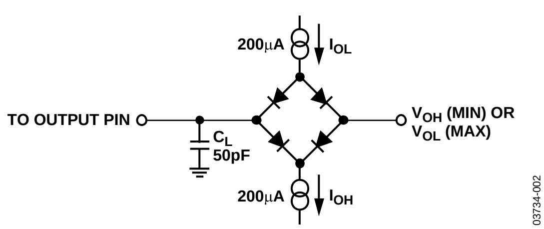


Figure 2. Load Circuit for SDO Timing Diagram (Serial Interface, Daisy-Chain Mode)

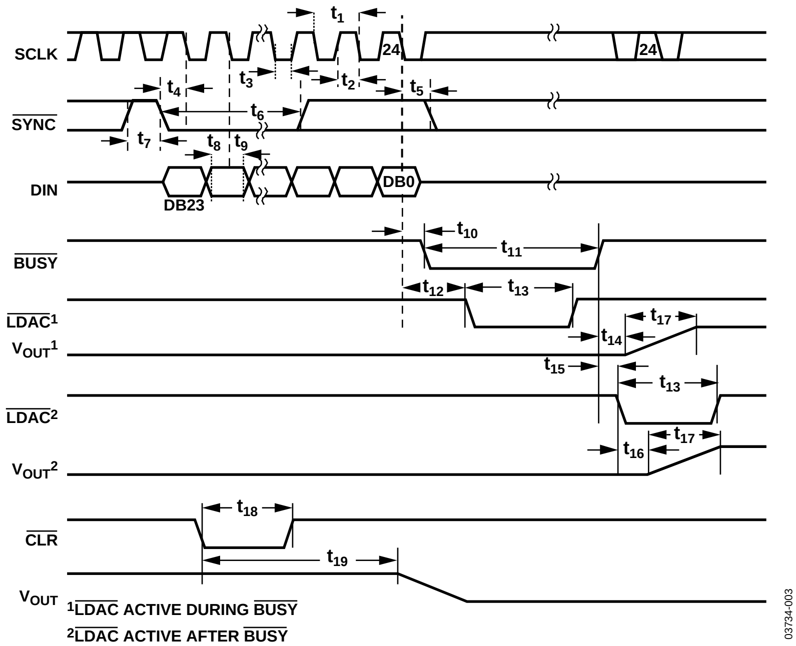


Figure 3. Serial Interface Timing Diagram (Standalone Mode)

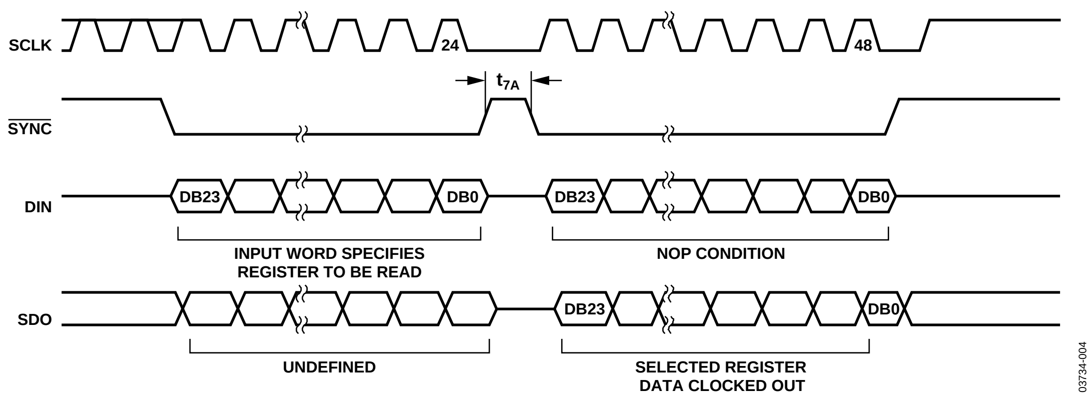


Figure 4. Serial Interface Timing Diagram (Data Readback Mode)

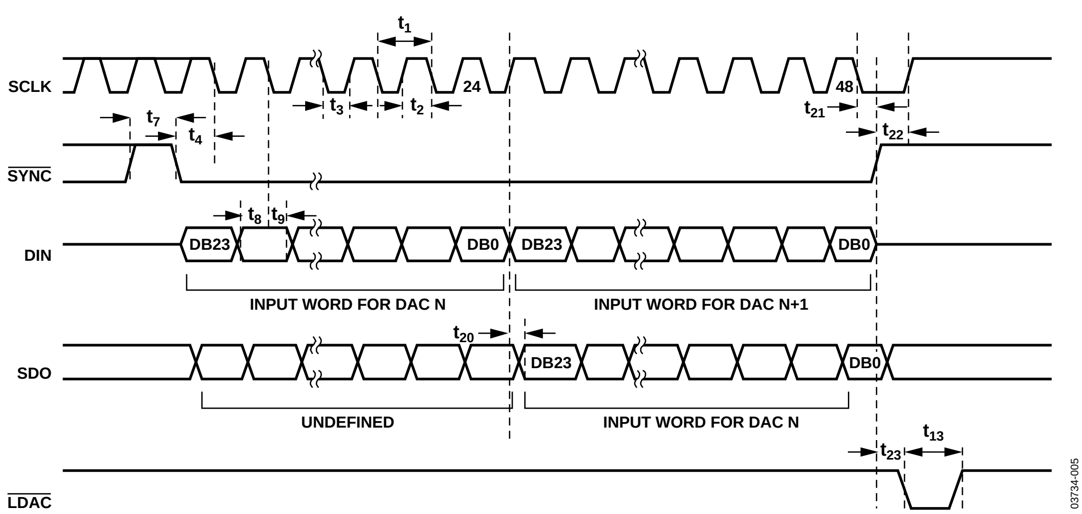


Figure 5. Serial Interface Timing Diagram (Daisy-Chain Mode)

I²C SERIAL INTERFACE TIMING

DV_{DD} = 2.7 V to 5.5 V; AV_{DD} = 4.5 V to 5.5 V or 2.7 V to 3.6 V; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	μs min	SCL cycle time
t_2	0.6	μs min	t_{HIGH}, SCL high time
t_3	1.3	μs min	t_{LOW}, SCL low time
t_4	0.6	μs min	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU,DAT}$, data setup time
t_6[3]	0.9	μs max	$t_{HD,DAT}$, data hold time
	0	μs min	$t_{HD,DAT}$, data hold time
t_7	0.6	μs min	$t_{SU,STA}$, setup time for repeated start
t_8	0.6	μs min	$t_{SU,STO}$, stop condition setup time
t_9	1.3	μs min	t_{BUF}, bus free time between a STOP and a START condition
t_{10}	300	ns max	t_R, rise time of SCL and SDA when receiving
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS-compatible)
t_{11}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS-compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	20 + 0.1 C_b[4]	ns min	t_F, fall time of SCL and SDA when transmitting
C_b	400	pF max	Capacitive load for each bus line

[1] Guaranteed by design and characterization, not production tested.
[2] See Figure 6.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[4] C_b is the total capacitance, in pF, of one bus line. t_R and t_F are measured between 0.3 DV_{DD} and 0.7 DV_{DD}.

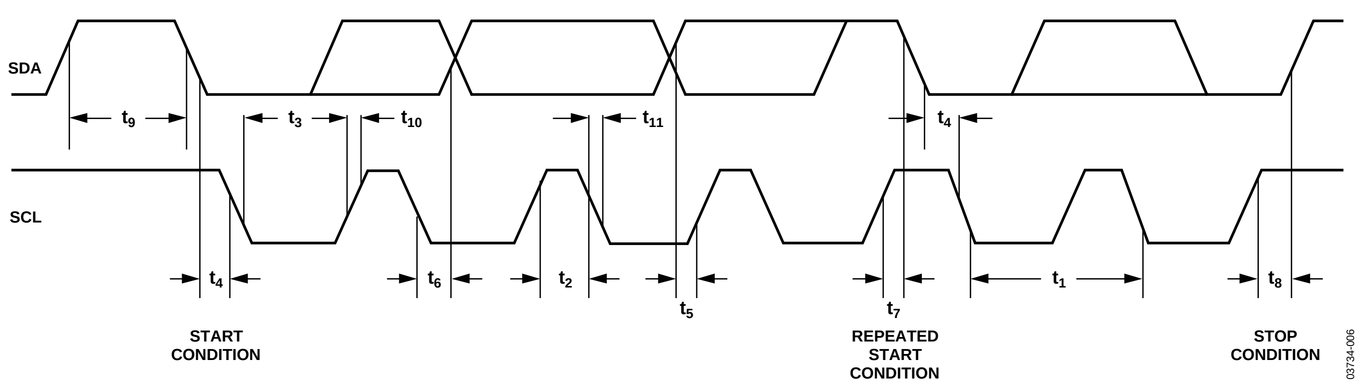


Figure 6. I²C-Compatible Serial Interface Timing Diagram

PARALLEL INTERFACE TIMING

DV_{DD} = 2.7 V to 5.5 V; AV_{DD} = 4.5 V to 5.5 V or 2.7 V to 3.6 V; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 6.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_0	4.5	ns min	REG0, REG1, address to $\overline{WR}$ rising edge setup time
t_1	4.5	ns min	REG0, REG1, address to $\overline{WR}$ rising edge hold time
t_2	20	ns min	$\overline{CS}$ pulse width low
t_3	20	ns min	$\overline{WR}$ pulse width low
t_4	0	ns min	$\overline{CS}$ to $\overline{WR}$ falling edge setup time
t_5	0	ns min	$\overline{WR}$ to $\overline{CS}$ rising edge hold time
t_6	4.5	ns min	Data to $\overline{WR}$ rising edge setup time
t_7	4.5	ns min	Data to $\overline{WR}$ rising edge hold time
t_8	20	ns min	$\overline{WR}$ pulse width high
t_9[4]	700	ns min	Minimum $\overline{WR}$ cycle time (single-channel write)
t_{10}[4]	30	ns max	$\overline{WR}$ rising edge to $\overline{BUSY}$ falling edge
t_{11}[4, 5]	670	ns max	$\overline{BUSY}$ pulse width low (single-channel update)
t_{12}	30	ns min	$\overline{WR}$ rising edge to $\overline{LDAC}$ falling edge
t_{13}	20	ns min	$\overline{LDAC}$ pulse width low
t_{14}	100/2000	ns min/max	$\overline{BUSY}$ rising edge to DAC output response time
t_{15}	20	ns min	$\overline{LDAC}$ rising edge to $\overline{WR}$ rising edge
t_{16}	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LDAC}$ falling edge
t_{17}	100/2000	ns min/max	$\overline{LDAC}$ falling edge to DAC output response time
t_{18}	8	µs max	DAC output settling time
t_{19}	20	ns min	$\overline{CLR}$ pulse width low
t_{20}	40	µs max	$\overline{CLR}$ pulse activation time

1 Guaranteed by design and characterization, not production tested.
2 All input signals are specified with t_R = t_R = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.
3 See Figure 7.
4 See Figure 29.
5 Measured with the load circuit of Figure 2.

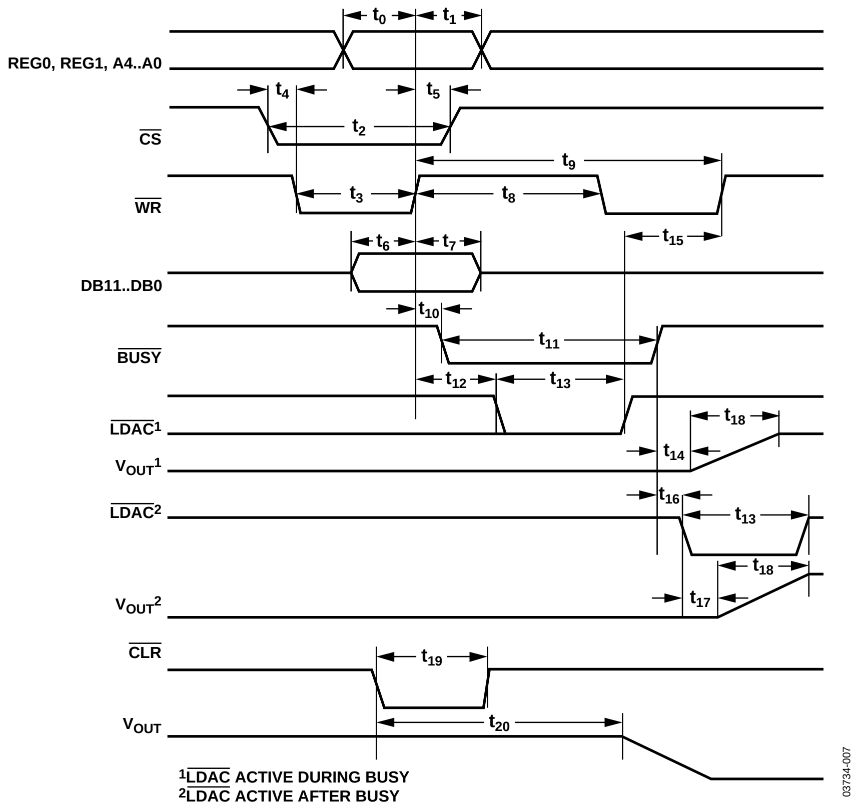


Figure 7. Parallel Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted[1].

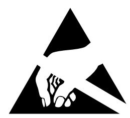
Table 7.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{DD} + 0.3 V
SDA/SCL to DGND	−0.3 V to +7 V
Digital Outputs to DGND	−0.3 V to DV_{DD} + 0.3 V
REFIN/REFOUT to AGND	−0.3 V to AV_{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
V_{OUT}x to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
MON_IN Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
MON_OUT to AGND	−0.3 V to AV_{DD} + 0.3 V
ESD	
HBM	6.5 kV
FICDM	2 kV
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Max)	150°C
100-Lead LQFP Package	
θ_{JA} Thermal Impedance	44°C/W
Reflow Soldering	
Peak Temperature	230°C

[1] Transient currents of up to 100 mA will not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

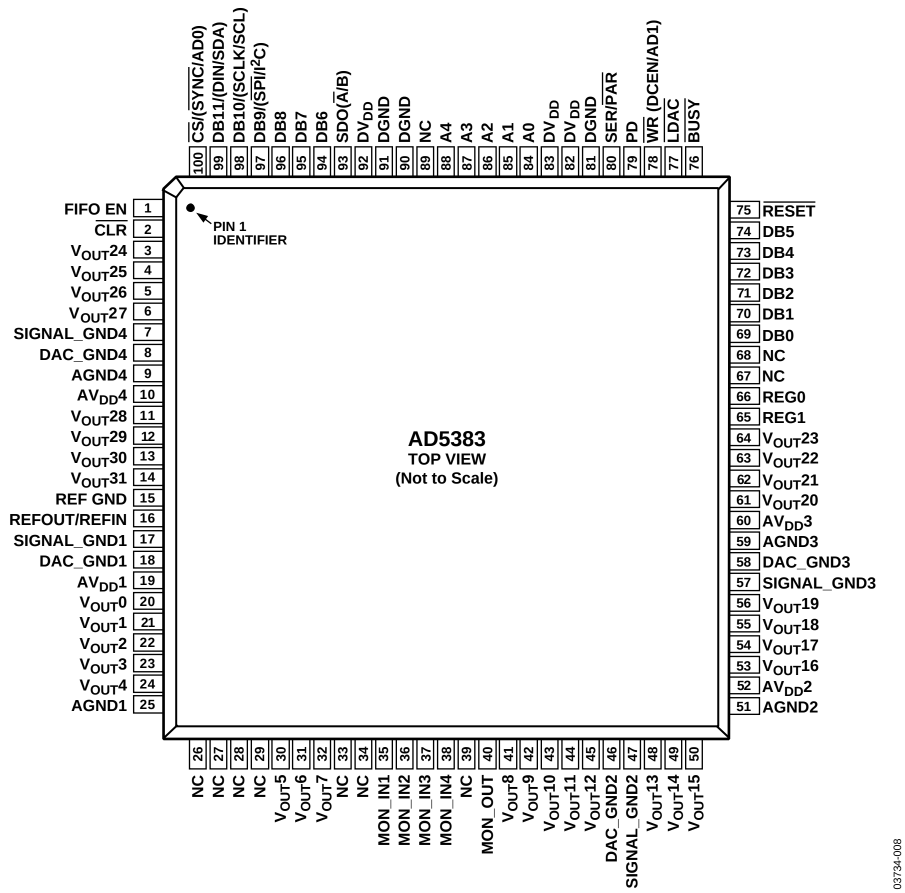


Figure 8. 100-Lead LQFP Pin Configuration

Table 8. Pin Function Descriptions

Mnemonic	Function
$V_{OUT}x$	Buffered Analog Outputs for Channel x. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
SIGNAL_GND(1 to 4)	Analog Ground Reference Points for Each Group of Eight Output Channels. All SIGNAL_GND pins are tied together internally and should be connected to the AGND plane as close as possible to the AD5383.
DAC_GND(1 to 4)	Each Group of Eight Channels Contains a DAC_GND Pin. This is the ground reference point for the internal 12-bit DAC. These pins should be connected to the AGND plane.
AGND(1 to 4)	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. All AGND pins should be connected externally to the AGND plane.
AV_{DD}(1 to 4)	Analog Supply Pins. Each group of eight channels has a separate AV_{DD} pin. These pins are connected together internally and should be decoupled with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor. Operating range for the AD5383-5 is 4.5 V to 5.5 V; operating range for the AD5383-3 is 2.7 V to 3.6 V.
DGND	Ground for All Digital Circuitry.
DV_{DD}	Logic Power Supply. Guaranteed operating range is 2.7 V to 5.5 V. It is recommended that these pins be decoupled with 0.1 µF ceramic and 10 µF tantalum capacitors to DGND.
REF GND	Ground Reference Point for the Internal Reference.
REFOUT/REFIN	The AD5383 Contains a Common REFOUT/REFIN Pin. When the internal reference is selected, this pin is the reference output. If the application requires an external reference, it can be applied to this pin and the internal reference can be disabled via the control register. The default for this pin is a reference input.
MON_OUT	MON_OUT Monitor Output Pin. When the monitor function is enabled, this output acts as the output of a 36-to-1 channel multiplexer that can be programmed to multiplex one of Channels 0 to 31or any of the monitor input pins (MON_IN1 to MON_IN4) to the MON_OUT pin. The MON_OUT pin's output impedance is typically 500 Ω, and is intended to drive a high input impedance like that exhibited by SAR ADC inputs.

Mnemonic	Function
MON_INx	MON_IN Monitor Input Pins. The AD5383 contains four monitor input pins that allow the user to connect input signals within the maximum ratings of the device to these pins for monitoring purposes. Any of the signals applied to the MON_IN pins along with the 32 output channels can be switched to the MON_OUT pin via software. An external ADC, for example, can be used to monitor these signals.
SER/PAR	Interface Select Input. This pin allows the user to select whether the serial or parallel interface is used. If it is tied high, the serial interface mode is selected and Pin 97 (SPI/I^{2}C) is used to determine if the interface mode is SPI or I^{2}C. Parallel interface mode is selected when SER/PAR is low.
CS/(SYNC/AD0)	Parallel Interface Mode. This pin acts as chip select input (level sensitive, active low). When low, the AD5383 is selected. Serial Interface Mode. This is the frame synchronization input signal for the serial clocks before the addressed register is updated. I^{2}C Mode. This pin acts as a hardware address pin used in conjunction with AD1 to determine the software address for the device on the I^{2}C bus.
WR/(DCEN/AD1)	Multifunction Pin. In parallel interface mode, this pin acts as write enable. In serial interface mode, this pin acts as a daisy-chain enable in SPI mode, and as a hardware address pin in I^{2}C mode. Parallel Interface Write Input (Edge Sensitive). The rising edge of WR is used in conjunction with CS low and the address bus inputs to write to the selected device registers. Serial Interface. Daisy-chain select input (level sensitive, active high). When high, this signal is used in conjunction with SER/PAR high to enable the SPI serial interface daisy-chain mode. I^{2}C Mode. This pin acts as a hardware address pin used in conjunction with AD0 to determine the software address for this device on the I^{2}C bus.
DB11 to DB0	Parallel Data Bus. DB11 is the MSB and DB0 is the LSB of the input data-word on the AD5383.
A4 to A0	Parallel Address Inputs. A4 to A0 are decoded to address one of the 40 input channels of the AD5383. Used in conjunction with the REG1 and REG0 pins to determine the destination register for the input data.
REG1, REG0	Register Pins. In parallel interface mode, REG1 and REG0 are used in decoding the destination registers for the input data. REG1 and REG0 are decoded to address the input data register, offset register, or gain register for the selected channel and are also used to decide the special function registers.
SDO/(A/B)	Serial Data Output in Serial Interface Mode. Three-stateable CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK, and is valid on the falling edge of SCLK. When operating in parallel interface mode, this pin acts as the A or B data register select when writing data to the data registers of the AD5383 with toggle mode selected (see the Toggle Mode Function section). In toggle mode, the LDAC is used to switch the output between the data contained in the A and B data registers. All DAC channels contain two data registers. In normal mode, Data Register A is the default for data transfers.
BUSY	Digital CMOS Output. BUSY goes low during internal calculations of the data (x2) loaded to the DAC data register. During this time, the user can continue writing new data to the x1, c, and m registers in parallel mode (these are stored in a FIFO), but no further updates to the DAC registers and DAC outputs can take place. If LDAC is taken low while BUSY is low, this event is stored. BUSY also goes low during power-on reset, and when the BUSY pin is low. During this time, the interface is disabled and any events on LDAC are ignored. A CLR operation also brings BUSY low.
LDAC	Load DAC Logic Input (Active Low). If LDAC is taken low while BUSY is inactive (high), the contents of the input registers are transferred to the DAC registers and the DAC outputs are updated. If LDAC is taken low while BUSY is active and internal calculations are taking place, the LDAC event is stored and the DAC registers are updated when BUSY goes inactive However any events on LDAC during power-on reset or on RESET are ignored.
CLR	Asynchronous Clear Input. The CLR input is falling edge sensitive. When CLR is activated, all channels are updated with the data contained in the CLR code register. BUSY is low for a duration of 35 µs while all channels are being updated with the CLR code.
RESET	Asynchronous Digital Reset Input (Falling Edge Sensitive). The function of this pin is equivalent to that of the power-on reset generator. When this pin is taken low, the state machine initiates a reset sequence to digitally reset the x1, m, c, and x2 registers to their default power-on values. This sequence typically takes 270 µs. The falling edge of RESET initiates the RESET process and BUSY goes low for the duration, returning high when RESET is complete. While BUSY is low, all interfaces are disabled and all LDAC pulses are ignored. When BUSY returns high, the part resumes normal operation and the status of the RESET pin is ignored until the next falling edge is detected.

Mnemonic	Function
PD	Power Down (Level Sensitive, Active High). PD is used to place the device in low power mode where the device consumes 2 μA analog supply current and 20 μA digital supply current. In power-down mode, all internal analog circuitry is placed in low power mode, and the analog output is configured as a high impedance output or will provide a 100 kΩ load to ground, depending on how the power-down mode is configured. The serial interface remains active during power-down.
FIFO EN	FIFO Enable (Level Sensitive, Active High). When connected to DV_{DD}, the internal FIFO is enabled, allowing the user to write to the device at full speed. FIFO is only available in parallel interface mode. The status of the FIFO EN pin is sampled on power-up, and also following a CLEAR or RESET, to determine if the FIFO is enabled. In either serial or I^2C interface modes, the FIFO EN pin should be tied low.
DB9/($\overline{SPI}$/I^2C)	Multifunction Input Pin. In parallel interface mode, this pin acts as DB9 of the parallel input data-word. In serial interface mode, this pin acts as serial interface mode select. When serial interface mode is selected (SER/$\overline{PAR}$ = 1) and this input is low, SPI mode is selected. In SPI mode, DB12 is the serial clock (SCLK) input and DB11 is the serial data (DIN) input. When serial interface mode is selected (SER/$\overline{PAR}$ = 1) and this input is high I^2C mode is selected. In this mode, DB12 is the serial clock (SCL) input and DB11 is the serial data (SDA) input.
DB10/(SCLK/SCL)	Multifunction Input Pin. In parallel interface mode, this pin acts as DB10 of the parallel input data-word. In serial interface mode, this pin acts as a serial clock input. Serial Interface Mode. In serial interface mode, data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 50 MHz. I^2C Mode. In I^2C mode, this pin performs the SCL function, clocking data into the device. The data transfer rate in I^2C mode is compatible with both 100 kHz and 400 kHz operating modes.
DB11/(DIN/SDA)	Multifunction Data Input Pin. In parallel interface mode, this pin acts as DB11 of the parallel input data-word. Serial Interface Mode. In serial interface mode, this pin acts as the serial data input. Data must be valid on the falling edge of SCLK. I^2C Mode. In I^2C mode, this pin is the serial data pin (SDA) operating as an open-drain input/output.
NC	No Connect. The user is advised not to connect any signal to these pins.

TERMINOLOGY

Relative Accuracy

Relative accuracy, or endpoint linearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error, and is expressed in LSB.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error

Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register. Ideally, with all 0s loaded to the DAC and m = all 1s, $c = 2^{n-1}$

$$V_{OUT(Zero\text{-}Scale)} = 0\ V$$

Zero-scale error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal), expressed in mV. It is mainly due to offsets in the output amplifier.

Offset Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) in the linear region of the transfer function, expressed in mV. Offset error is measured on the AD5383-5 with Code 32 loaded into the DAC register, and on the AD5383-3 with Code 64.

Gain Error

Gain Error is specified in the linear region of the output range between V_{OUT} = 10 mV and V_{OUT} = AV_{DD} − 50 mV. It is the deviation in slope of the DAC transfer characteristic from the ideal and is expressed in %FSR with the DAC output unloaded.

DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC at midscale in response to a full-scale code (all 0s to all 1s, and vice versa) and output change of all other DACs. It is expressed in LSB.

DC Output Impedance

DC output impedance is the effective output source resistance. It is dominated by package lead resistance.

Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change, and is measured from the $\overline{\text{BUSY}}$ rising edge.

Digital-to-Analog Glitch Energy

Digital-to-analog glitch energy is the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one DAC due to both the digital change and to the subsequent analog output change at another DAC. The victim channel is loaded with midscale. DAC-to-DAC crosstalk is specified in nV-s.

Digital Crosstalk

The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.

Digital Feedthrough

When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the V_{OUT} pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density

Output noise spectral density is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hertz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in nV/√Hz in a 1 Hz bandwidth at 10 kHz.

TYPICAL PERFORMANCE CHARACTERISTICS

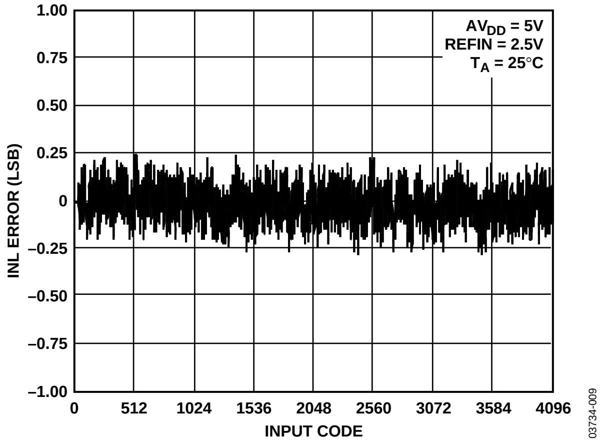


Figure 9. Typical AD5383-5 INL Plot

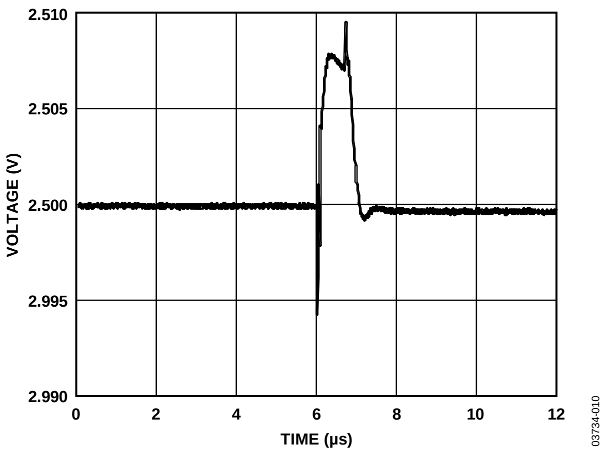


Figure 10. AD5383-5 Glitch Impulse

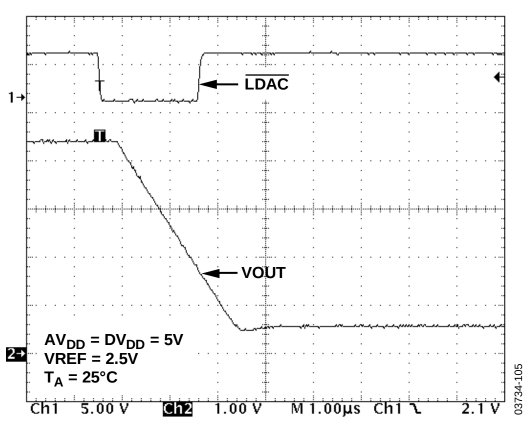


Figure 11. Slew Rate with Boost Off

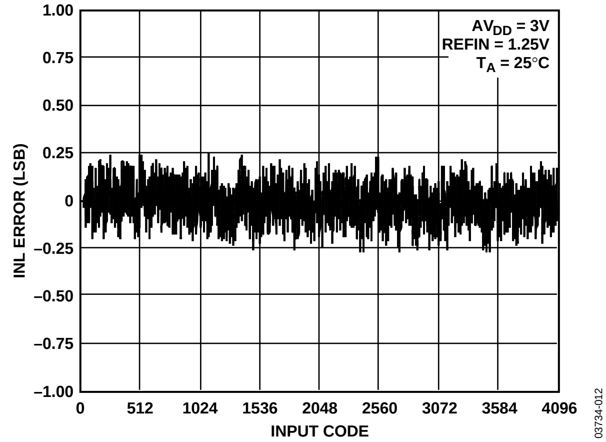


Figure 12. Typical AD5383-3 INL Plot

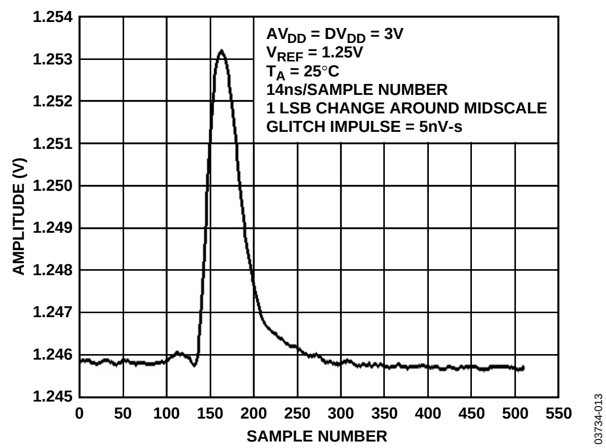


Figure 13. AD5383-3 Glitch Impulse

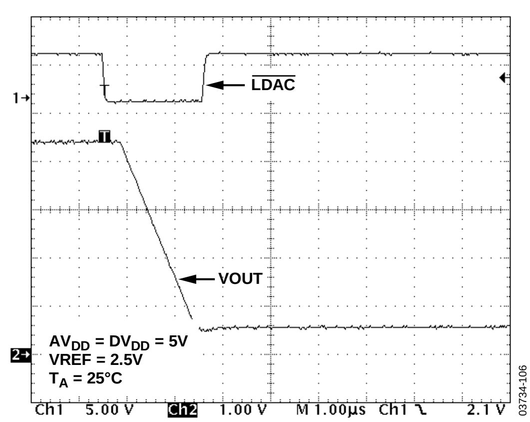


Figure 14. Slew Rate with Boost On

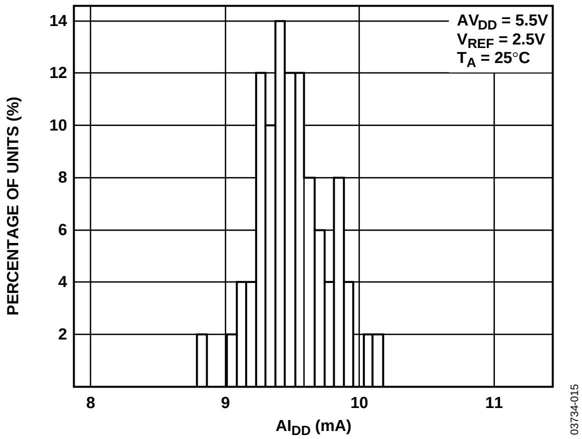


Figure 15. AI_{DD} Histogram

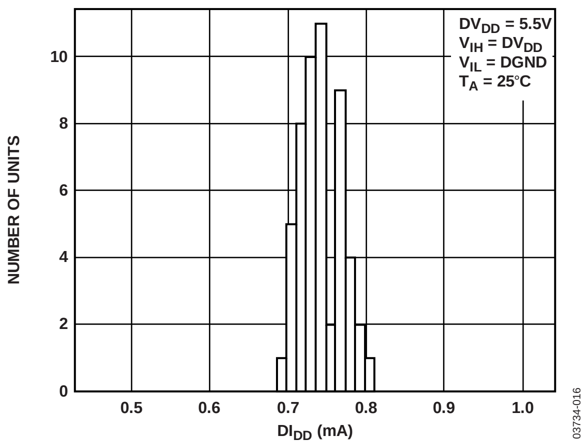


Figure 16. DI_{DD} Histogram

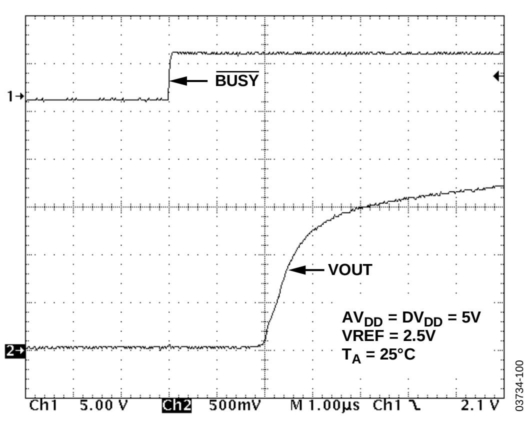


Figure 17. Exiting Soft Power-Down

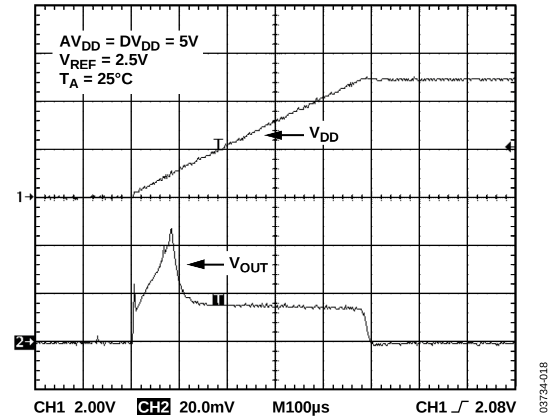


Figure 18. Power-Up Transient

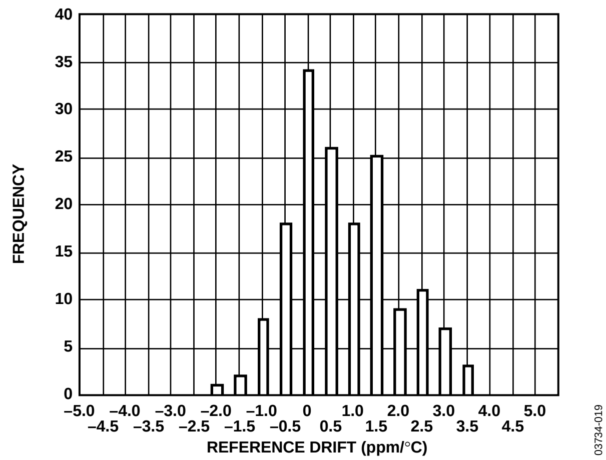


Figure 19. REFOUT Temperature Coefficient

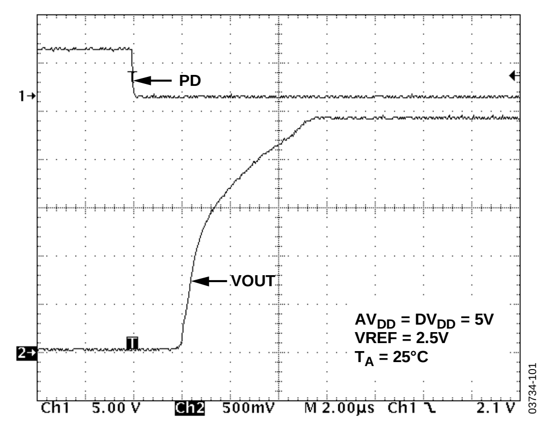


Figure 20. Exiting Hardware Power-Down

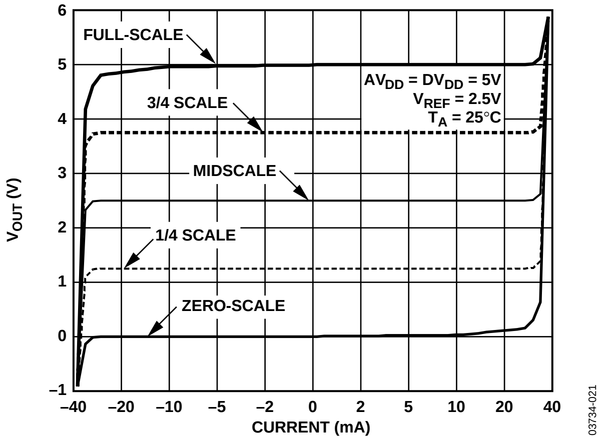


Figure 21. AD5383-5 Output Amplifier Source and Sink Capability

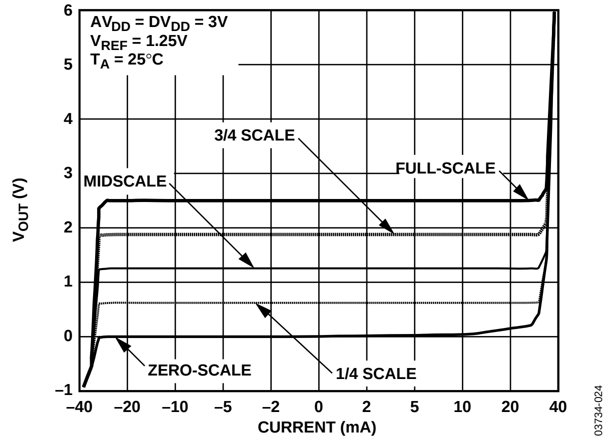


Figure 24. AD5383-3 Output Amplifier Source and Sink Capability

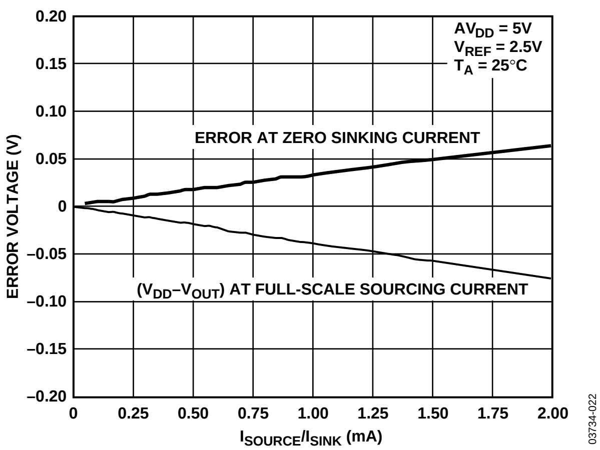


Figure 22. Headroom at Rails vs. Source/Sink Current

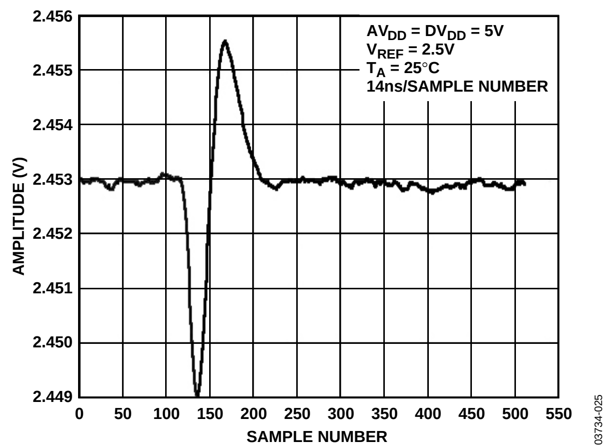


Figure 25. Adjacent Channel DAC-to-DAC Crosstalk

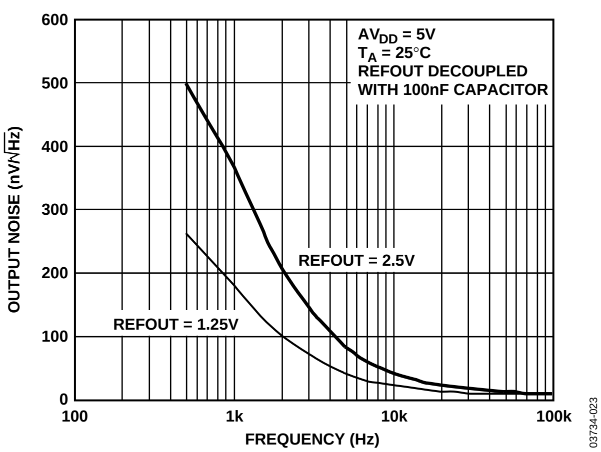


Figure 23. REFOUT Noise Spectral Density

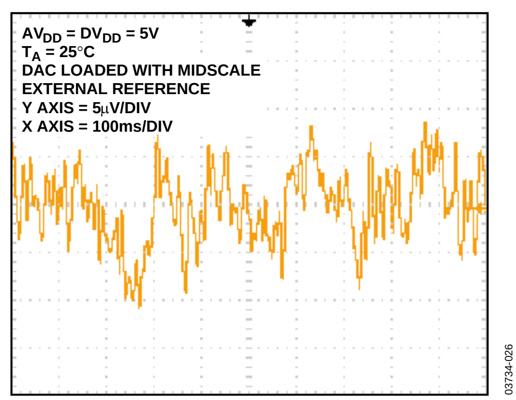


Figure 26. 0.1 Hz to 10 Hz Noise Plot

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE—GENERAL

The AD5383 is a complete, single-supply, 32-channel voltage output DAC that offers 12-bit resolution. The part is available in a 100-lead LQFP package and features both a parallel and a serial interface. This product includes an internal, software selectable, 1.25 V/2.5 V, 10 ppm/°C reference that can be used to drive the buffered reference inputs; alternatively, an external reference can be used to drive these inputs. Internal/external reference selection is via the CR8 bit in the control register; CR10 selects the reference magnitude if the internal reference is selected. All channels have an on-chip output amplifier with rail-to-rail output capable of driving 5 kΩ in parallel with a 200 pF load.

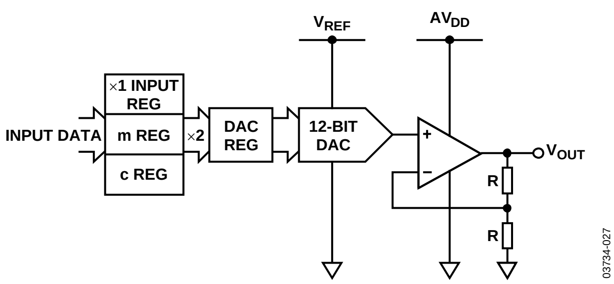


Figure 27. Single-Channel Architecture

The architecture of a single DAC channel consists of a 12-bit resistor-string DAC followed by an output buffer amplifier operating at a gain of 2. This resistor-string architecture guarantees DAC monotonicity. The 12-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed to the output amplifier. Each channel on these devices contains independent offset and gain control registers that allow the user to digitally trim offset and gain. These registers give the user the ability to calibrate out errors in the complete signal chain, including the DAC, using the internal m and c registers, which hold the correction factors. All channels are double buffered, allowing synchronous updating of all channels using the $\overline{LDAC}$ pin. Figure 27 shows a block diagram of a single channel on the AD5383. The digital input transfer function for each DAC can be represented as

$$x2 = [(m + 2)/ 2^n \times x1] + (c - 2^{n-1})$$

where:

$x2$ = the data-word loaded to the resistor string DAC.

$x1$ = the 12-bit data-word written to the DAC input register.

m = the gain coefficient (default is 0xFFE). The gain coefficient is written to the 11 most significant bits (DB11 to DB1) and the LSB (DB0) is 0.

n = DAC resolution (n = 12 for AD5383).

c = the12-bit offset coefficient (default is 0x800).

The complete transfer function for these devices can be represented as

$$V_{OUT} = 2 \times V_{REF} \times x2/2^n$$

where $x2$ is the data-word loaded to the resistor string DAC. V_{REF} is the internal reference voltage or the reference voltage externally applied to the DAC REFOUT/REFIN pin. For specified performance, an external reference voltage of 2.5 V is recommended for the AD5383-5 and 1.25 V for the AD5383-3.

DATA DECODING

The AD5383 contains a 12-bit data bus, DB11 to DB0. Depending on the value of REG1 and REG0 (see Table 9), this data is loaded into the addressed DAC input registers, offset (c) registers, or gain (m) registers. The format data, offset (c), and gain (m) register contents are shown in Table 10 to Table 12.

Table 9. Register Selection

REG1	REG0	Register Selected
1	1	Input Data Register (x1)
1	0	Offset Register (c)
0	1	Gain Register (m)
0	0	Special Function Registers (SFRs)

Table 10. DAC Data Format (REG1 = 1, REG0 = 1)

DB11 to DB0			DAC Output (V)
1111	1111	1111	$2\ V_{REF} \times (4095/4096)$
1111	1111	1110	$2\ V_{REF} \times (4094/4096)$
1000	0000	0001	$2\ V_{REF} \times (2049/4096)$
1000	0000	0000	$2\ V_{REF} \times (2048/4096)$
0111	1111	1111	$2\ V_{REF} \times (2047/4096)$
0000	0000	0001	$2\ V_{REF} \times (1/4096)$
0000	0000	0000	0

Table 11. Offset Data Format (REG1 = 1, REG0 = 0)

DB11 to DB0			Offset (LSB)
1111	1111	1111	+2048
1111	1111	1110	+2047
1000	0000	0001	+1
1000	0000	0000	0
0111	1111	1111	−1
0000	0000	0001	−2047
0000	0000	0000	−2048

Table 12. Gain Data Format (REG1 = 0, REG0 = 1)

DB11 to DB1			Gain Factor
1111	1111	1110	1
1011	1111	1110	0.75
0111	1111	1110	0.5
0011	1111	1110	0.25
0000	0000	0000	0

ON-CHIP SPECIAL FUNCTION REGISTERS (SFR)

The AD5383 contains a number of special function registers (SFRs), as outlined in Table 13. SFRs are addressed with REG1 = REG0 = 0 and are decoded using Address Bit A4 to Address Bit A0.

Table 13. SFR Register Functions (REG1 = 0, REG0 = 0)

R/$\overline{W}$	A4	A3	A2	A1	A0	Function
X	0	0	0	0	0	NOP (No Operation)
0	0	0	0	0	1	Write CLR Code
0	0	0	0	1	0	Soft CLR
0	0	1	0	0	0	Soft Power-Down
0	0	1	0	0	1	Soft Power-Up
0	0	1	1	0	0	Control Register Write
1	0	1	1	0	0	Control Register Read
0	0	1	0	1	0	Channel Monitor
0	0	1	1	1	1	Soft Reset

SFR COMMANDS

NOP (No Operation)

REG1 = REG0 = 0, A4 to A0 = 00000

Performs no operation but is useful in serial readback mode to clock out data on D_{OUT} for diagnostic purposes. $\overline{BUSY}$ pulses low during a NOP operation.

Write CLR Code

REG1 = REG0 = 0, A4 to A0 = 00001
DB11 to DB0 = contain the CLR data

Bringing the $\overline{CLR}$ line low or exercising the soft clear function loads the contents of the DAC registers with the data contained in the user configurable $\overline{CLR}$ register, and sets $V_{OUT}0$ to $V_{OUT}31$ accordingly. This can be very useful for setting up a specific output voltage in a clear condition. It is also beneficial for calibration purposes; the user can load full scale or zero scale to the clear code register and then issue a hardware or software clear to load this code to all DACs, removing the need for individual writes to each DAC. Default on power-up is all zeros.

Soft CLR

REG1 = REG0 = 0, A4 to A0 = 00010
DB11 to DB0 = don't care

Executing this instruction performs the CLR, which is functionally the same as that provided by the external $\overline{CLR}$ pin. The DAC outputs are loaded with the data in the CLR code register. It takes 35 µs to fully execute the SOFT CLR, as indicated by the $\overline{BUSY}$ low time.

Soft Power-Down

REG1 = REG0 = 0, A4 to A0 = 01000
DB11 to DB0 = don't care

Executing this instruction performs a global power-down feature that puts all channels into a low power mode that reduces the analog supply current to 2 µA max, and the digital current to 20 µA. In power-down mode, the output amplifier can be configured as a high impedance output or provide a 100 kΩ load to ground. The contents of all internal registers are retained in power-down mode. No register can be written to while in power-down.

Soft Power-Up

REG1 = REG0 = 0, A4 to A0 = 01001
DB11 to DB0 = don't care

This instruction is used to power up the output amplifiers and the internal reference. The time to exit power-down is 8 µs. The hardware power-down and software function are internally combined in a digital OR function.

Soft RESET

REG1 = REG0 = 0, A4 to A0 = 01111
DB11 to DB0 = don't care

This instruction is used to implement a software reset. All internal registers are reset to their default values, which correspond to m at full-scale and c at zero scale. The contents of the DAC registers are cleared, setting all analog outputs to 0 V. The soft reset activation time is 135 µs. Only perform a soft reset when the AD5383 is not in power-down mode.

Table 14. Control Register Contents

MSB											LSB
CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

Control Register Write/Read

REG1 = REG0 = 0, A4 to A0 = 01100, $R/\overline{W}$ status determines if the operation is a write ($R/\overline{W}$ = 0) or a read ($R/\overline{W}$ = 1). DB11 to DB0 contains the control register data.

Control Register Contents

CR11: Power-Down Status. This bit is used to configure the output amplifier state in power-down.

CR11 = 1. Amplifier output is high impedance (default on power-up).

CR11 = 0. Amplifier output is 100 kΩ to ground.

CR10: REF Select. This bit selects the operating internal reference for the AD5383. CR12 is programmed as follows:

CR10 = 1: Internal reference is 2.5 V (AD5383-5 default), the recommended operating reference for AD5383-5.

CR10 = 0: Internal reference is 1.25 V (AD5383-3 default), the recommended operating reference for AD5383-3.

CR9: Current Boost Control. This bit is used to boost the current in the output amplifier, thereby altering its slew rate. This bit is configured as follows:

CR9 = 1: Boost Mode On. This maximizes the bias current in the output amplifier, optimizing its slew rate but increasing the power dissipation.

CR9 = 0: Boost Mode Off (default on power-up). This reduces the bias current in the output amplifier and reduces the overall power consumption.

CR8: Internal/External Reference. This bit determines if the DAC uses its internal reference or an externally applied reference.

CR8 = 1: Internal Reference Enabled. The reference output depends on data loaded to CR10.

CR8 = 0: External Reference Selected (default on power up).

CR7: Channel Monitor Enable (see Channel Monitor Function).

CR7= 1: Monitor Enabled. This enables the channel monitor function. After a write to the monitor channel in the SFR register, the selected channel output is routed to the MON_OUT pin.

CR7 = 0: Monitor Disabled (default on power-up). When the monitor is disabled, the MON_OUT pin is three-stated.

CR6: Thermal Monitor Function. This function is used to monitor the internal die temperature of the AD5383 when enabled. The thermal monitor powers down the output amplifiers when the temperature exceeds 130°C. This function can be used to protect the device in cases where power dissipation may be exceeded if a number of output channels are simultaneously short-circuited. A soft power-up will re-enable the output amplifiers if the die temperature has dropped below 130°C.

CR6 = 1: Thermal Monitor Enabled.

CR6 = 0: Thermal Monitor Disabled (default on power-up).

CR5 and CR4: Don't Care.

CR3 to CR0: Toggle Function Enable. This function allows the user to toggle the output between two codes loaded to the A and B registers for each DAC. Control Register Bits CR3 to CR0 are used to enable individual groups of eight channels for operation in toggle mode. A Logic 1 written to any bit enables a group of channels; a Logic 0 disables a group. $\overline{LDAC}$ is used to toggle between the two registers. Logic 1 enables a group of channels; Logic 0 disables a group of channels.

Table 15.

CR Bit	Group	Channels
CR3	3	24 to 31
CR2	2	16 to 23
CR1	1	8 to 15
CR0	0	0 to 7

Channel Monitor Function

REG1 = REG0 = 0, A4 to A0 = 01010

DB11 to DB6 = Contain data to address the monitored channel.

A channel monitor function is provided on the AD5383. This feature, which consists of a multiplexer addressed via the interface, allows any channel output or signals connected to the MON_IN pins to be routed to the MON_OUT pin for monitoring using an external ADC. The channel monitor function must be enabled in the control register before any channels are routed to MON_OUT. On the AD5383, DB11 to DB6 contain the channel address for the monitored channel. Selecting Channel Address 63 three-states MON_OUT.

Table 16. Channel Monitor Decoding

REG1	REG0	A4	A3	A2	A1	A0	DB11	DB10	DB9	DB8	DB7	DB6	DB5 to DB0	MON_OUT
0	0	0	1	0	1	0	0	0	0	0	0	0	X	$V_{OUT}0$
0	0	0	1	0	1	0	0	0	0	0	0	1	X	$V_{OUT}1$
0	0	0	1	0	1	0	0	0	0	0	1	0	X	$V_{OUT}2$
0	0	0	1	0	1	0	0	0	0	0	1	1	X	$V_{OUT}3$
0	0	0	1	0	1	0	0	0	0	1	0	0	X	$V_{OUT}4$
0	0	0	1	0	1	0	0	0	0	1	0	1	X	$V_{OUT}5$
0	0	0	1	0	1	0	0	0	0	1	1	0	X	$V_{OUT}6$
0	0	0	1	0	1	0	0	0	0	1	1	1	X	$V_{OUT}7$
0	0	0	1	0	1	0	0	0	1	0	0	0	X	$V_{OUT}8$
0	0	0	1	0	1	0	0	0	1	0	0	1	X	$V_{OUT}9$
0	0	0	1	0	1	0	0	0	1	0	1	0	X	$V_{OUT}10$
0	0	0	1	0	1	0	0	0	1	0	1	1	X	$V_{OUT}11$
0	0	0	1	0	1	0	0	0	1	1	0	0	X	$V_{OUT}12$
0	0	0	1	0	1	0	0	0	1	1	0	1	X	$V_{OUT}13$
0	0	0	1	0	1	0	0	0	1	1	1	0	X	$V_{OUT}14$
0	0	0	1	0	1	0	0	0	1	1	1	1	X	$V_{OUT}15$
0	0	0	1	0	1	0	0	1	0	0	0	0	X	$V_{OUT}16$
0	0	0	1	0	1	0	0	1	0	0	0	1	X	$V_{OUT}17$
0	0	0	1	0	1	0	0	1	0	0	1	0	X	$V_{OUT}18$
0	0	0	1	0	1	0	0	1	0	0	1	1	X	$V_{OUT}19$
0	0	0	1	0	1	0	0	1	0	1	0	0	X	$V_{OUT}20$
0	0	0	1	0	1	0	0	1	0	1	0	1	X	$V_{OUT}21$
0	0	0	1	0	1	0	0	1	0	1	1	0	X	$V_{OUT}22$
0	0	0	1	0	1	0	0	1	0	1	1	1	X	$V_{OUT}23$
0	0	0	1	0	1	0	0	1	1	0	0	0	X	$V_{OUT}24$
0	0	0	1	0	1	0	0	1	1	0	0	1	X	$V_{OUT}25$
0	0	0	1	0	1	0	0	1	1	0	1	0	X	$V_{OUT}26$
0	0	0	1	0	1	0	0	1	1	0	1	1	X	$V_{OUT}27$
0	0	0	1	0	1	0	0	1	1	1	0	0	X	$V_{OUT}28$
0	0	0	1	0	1	0	0	1	1	1	0	1	X	$V_{OUT}29$
0	0	0	1	0	1	0	0	1	1	1	1	0	X	$V_{OUT}30$
0	0	0	1	0	1	0	0	1	1	1	1	1	X	$V_{OUT}31$
0	0	0	1	0	1	0	1	0	0	0	0	0	X	Undefined
0	0	0	1	0	1	0	1	0	0	0	0	1	X	Undefined
0	0	0	1	0	1	0	1	0	0	0	1	0	X	MON_IN1
0	0	0	1	0		0	1	0	0	0	1	1	X	MON_IN2
0	0	0	1	0	1	0	1	0	0	1	0	0	X	MON_IN3
0	0	0	1	0	1	0	1	0	0	1	0	1	X	MON_IN4
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
0	0	0	1	0	1	0	1	1	1	1	1	0	X	Undefined
0	0	0	1	0	1	0	1	1	1	1	1	1	X	Three-State

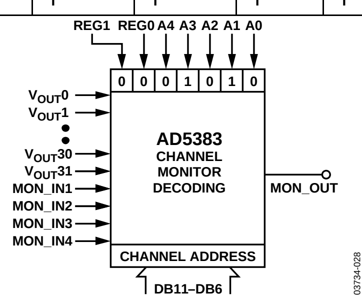


Figure 28. Channel Monitor Decoding

HARDWARE FUNCTIONS

RESET FUNCTION

Bringing the $\overline{\text{RESET}}$ line low resets the contents of all internal registers to their power-on reset state. $\overline{\text{RESET}}$ is a negative edge-sensitive input. The default corresponds to m at full scale and to c at zero scale. The contents of the DAC registers are cleared, setting $V_{OUT}0$ to $V_{OUT}31$ to 0 V. This sequence takes 270 µs max. The falling edge of $\overline{\text{RESET}}$ initiates the reset process; $\overline{\text{BUSY}}$ goes low for the duration, returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled and all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{BUSY}}$ returns high, the part resumes normal operation and the status of the $\overline{\text{RESET}}$ pin is ignored until the next falling edge is detected. Only perform a soft reset when the AD5383 is not in power-down mode.

ASYNCHRONOUS CLEAR FUNCTION

Bringing the $\overline{\text{CLR}}$ line low clears the contents of the DAC registers to the data contained in the user-configurable CLR register and sets $V_{OUT}0$ to $V_{OUT}31$ accordingly. This function can be used in system calibration to load zero scale and full-scale to all channels. The execution time for a CLR is 32 µs.

$\overline{\text{BUSY}}$ AND $\overline{\text{LDAC}}$ FUNCTIONS

$\overline{\text{BUSY}}$ is a digital CMOS output that indicates the status of the AD5383. The value of x2, the internal data loaded to the DAC data register, is calculated each time the user writes new data to the corresponding x1, c, or m registers. During the calculation of x2, the $\overline{\text{BUSY}}$ output goes low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the x1, m, or c registers, but no DAC output updates can take place. The DAC outputs are updated by taking the $\overline{\text{LDAC}}$ input low. If $\overline{\text{LDAC}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LDAC}}$ event is stored and the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. The user may hold the $\overline{\text{LDAC}}$ input permanently low, in which case the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. $\overline{\text{BUSY}}$ also goes low during power-on reset and when a falling edge is detected on the $\overline{\text{RESET}}$ pin. During this time, all interfaces are disabled and any events on $\overline{\text{LDAC}}$ are ignored. The AD5383 contains an extra feature whereby a DAC register is not updated unless its x2 register has been written to since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the x2 registers. However, the AD5383 will only update the DAC register if the x2 data has changed, thereby removing unnecessary digital crosstalk.

FIFO OPERATION IN PARALLEL MODE

The AD5383 contains a FIFO to optimize operation when operating in parallel interface mode. The FIFO Enable (level sensitive, active high) is used to enable the internal FIFO. When connected to DV_{DD}, the internal FIFO is enabled, allowing the user to write to the device at full speed. FIFO is only available in parallel interface mode. The status of the FIFO EN pin is sampled on power-up, and after a $\overline{\text{CLR}}$ or $\overline{\text{RESET}}$, to determine if the FIFO is enabled. In either serial or I^2C interface modes, FIFO EN should be tied low. Up to 128 successive instructions can be written to the FIFO at maximum speed in parallel mode. When the FIFO is full, any further writes to the device are ignored. Figure 29 shows a comparison between FIFO mode and non-FIFO mode in terms of channel update time. Figure 29 also outlines digital loading time.

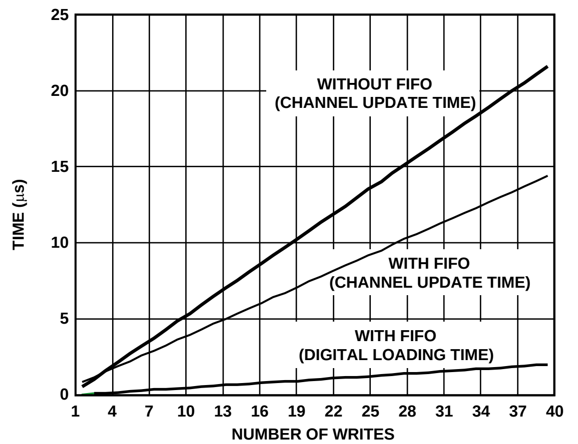


Figure 29. Channel Update Rate (FIFO vs. Non-FIFO)

POWER-ON RESET

The AD5383 contains a power-on reset generator and state machine. The power-on reset resets all registers to a predefined state and configures the analog outputs as high impedance. The $\overline{\text{BUSY}}$ pin goes low during the power-on reset sequencing, preventing data writes to the device.

POWER-DOWN

The AD5383 contains a global power-down feature that puts all channels into a low power mode and reduces the analog power consumption to 2 µA maximum and digital power consumption to 20 µA maximum. In power-down mode, the output amplifier can be configured as high impedance output or provide a 100 kΩ load to ground. The contents of all internal registers are retained in power-down mode. When exiting power-down, the settling time of the amplifier will elapse before the outputs settle to their correct values.

INTERFACES

The AD5383 contains both parallel and serial interfaces. Furthermore, the serial interface can be programmed to be SPI-, DSP-, MICROWIRE-, or I²C-compatible. The SER/PAR pin selects parallel and serial interface modes. In serial mode, the SPI/I²C pin is used to select DSP, SPI, MICROWIRE, or I²C interface mode.

The devices use an internal FIFO memory to allow high speed successive writes in parallel interface mode. The user can continue writing new data to the device while write instructions are being executed. The BUSY signal indicates the current status of the device, going low while instructions in the FIFO are being executed. In parallel mode, up to 128 successive instructions can be written to the FIFO at maximum speed. When the FIFO is full, any further writes to the device are ignored.

To minimize both the power consumption of the device and the on-chip digital noise, the active interface only powers up fully when the device is being written to, that is, on the falling edge of WR or the falling edge of SYNC.

DSP-, SPI-, MICROWIRE-COMPATIBLE SERIAL INTERFACES

The serial interface can be operated with a minimum of three wires in standalone mode or four wires in daisy-chain mode. Daisy-chaining allows many devices to be cascaded together to increase system channel count. The SER/PAR pin must be tied high and the SPI/I²C pin (Pin 97) should be tied low to enable the DSP-/SPI-/MICROWIRE-compatible serial interface. In serial interface mode, the user does not need to drive the parallel input data pins. The serial interface's control pins are:

SYNC, DIN, SCLK—Standard 3-wire interface pins.
DCEN—Selects standalone mode or daisy-chain mode.
SDO—Data out pin for daisy-chain mode.

Figure 3 and Figure 5 show timing diagrams for a serial write to the AD5383 in standalone and daisy-chain modes. The 24-bit data-word format for the serial interface is shown in Table 17.

A/B. When toggle mode is enabled, this pin selects whether the data write is to the A or B register. With toggle disabled, this bit should be set to zero to select the A data register.

R/W is the read or write control bit.

A4 to A0 address the input channels.

REG1 and REG0 select the register to which data is written, as shown in Table 9.

DB11 to DB0 contain the input data-word.

X is a don't care condition.

Standalone Mode

By connecting the DCEN (daisy-chain enable) pin low, standalone mode is enabled. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of SYNC starts the write cycle and resets a counter that counts the number of serial clocks to ensure that the correct number of bits are shifted into the serial shift register. Any further edges on SYNC, except for a falling edge, are ignored until 24 bits are clocked in. Once 24 bits have been shifted in, the SCLK is ignored. In order for another serial transfer to take place, the counter must be reset by the falling edge of SYNC.

Table 17. 40-Channel, 12-Bit DAC Serial Input Register Configuration

MSB ... LSB

A/B	R/W	0	A4	A3	A2	A1	A0	REG1	REG0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	X	X

Daisy-Chain Mode

For systems that contain several devices, the SDO pin may be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines.

By connecting the DCEN (daisy-chain enable) pin high, daisy-chain mode is enabled. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the DIN input on the next device in the chain, a multidevice interface is constructed. Twenty-four clock pulses are required for each device in the system. Therefore, the total number of clock cycles must equal 24N, where N is the total number of AD538x devices in the chain.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This latches the input data in each device in the daisy-chain and prevents any further data from being clocked into the input shift register.

If $\overline{\text{SYNC}}$ is taken high before 24 clocks are clocked into the part, this is considered a bad frame and the data is discarded.

The serial clock may be either a continuous or a gated clock. A continuous SCLK source can only be used if $\overline{\text{SYNC}}$ can be held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

Readback Mode

Readback mode is invoked by setting the R/$\overline{\text{W}}$ bit = 1 in the serial input register write. With R/$\overline{\text{W}}$ = 1, Bits A4 to A0, in association with Bits REG1 and REG0, select the register to be read. The remaining data bits in the write sequence are don't cares. During the next SPI write, the data appearing on the SDO output will contain the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. Figure 30 shows the readback sequence. For example, to read back the m register of Channel 0 on the AD5383, the following sequence should be implemented. First, write 0x404XXX to the AD5383 input register. This configures the AD5383 for read mode with the m register of Channel 0 selected. Note that Data Bits DB11 to DB0 are don't cares. Follow this with a second write, a NOP condition, 0x000000. During this write, the data from the m register is clocked out on the D_{OUT} line, that is, data clocked out will contain the data from the m register in Bits DB11 to DB0, and the top 10 bits contain the address information as previously written. In readback mode, the $\overline{\text{SYNC}}$ signal must frame the data. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of the SCLK signal. If the SCLK idles high between the write and read operations of a readback operation, the first bit of data is clocked out on the falling edge of $\overline{\text{SYNC}}$.

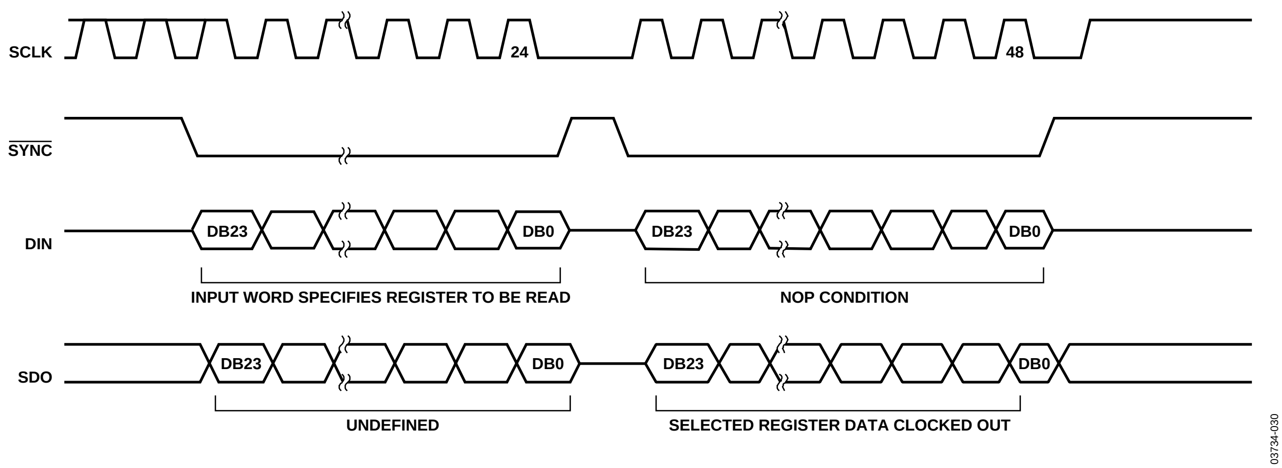


Figure 30. Serial Readback Operation

I^{2}C SERIAL INTERFACE

The AD5383 features an I^{2}C-compatible, 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the AD5383 and the master at rates up to 400 kHz. Figure 6 shows the 2-wire interface timing diagram that incorporates three different modes of operation. In selecting the I^{2}C operating mode, first configure serial operating mode (SER/$\overline{\text{PAR}}$ = 1) and then select I^{2}C mode by configuring the $\overline{\text{SPI}}$/I^{2}C pin to a Logic 1. The device is connected to the I^{2}C bus as a slave device (that is, no clock is generated by the AD5383). The AD5383 has a 7-bit slave address 10101 (AD1) (AD0). The 5 MSBs are hard-coded and the 2 LSBs are determined by the state of the AD1 and AD0 pins. The facility to hardware-configure AD1 and AD0 allows four of these devices to be configured on the bus.

I^{2}C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals that configure START and STOP conditions. Both SDA and SCL are pulled high by the external pull-up resistors when the I^{2}C bus is not busy.

START and STOP Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the AD5383. The STOP condition frees the bus. If a repeated START condition (Sr) is generated instead of a STOP condition, the bus remains active.

Repeated START Conditions

A repeated START (Sr) condition may indicate a change of data direction on the bus. Sr may be used when the bus master is writing to several I^{2}C devices and wants to maintain control of the bus.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data-word. ACK is always generated by the receiving device. The AD5383 devices generate an ACK when receiving an address or data by pulling SDA low during the ninth clock period. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication.

AD5383 Slave Addresses

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave address. When idle, the AD5383 waits for a START condition followed by its slave address. The LSB of the address word is the read/write (R/$\overline{\text{W}}$) bit. The AD5383 is a receive-only device; when communicating with the AD5383, R/$\overline{\text{W}}$ = 0. After receiving the proper address 10101 (AD1) (AD0), the AD5383 issues an ACK by pulling SDA low for one clock cycle.

The AD5383 has four different user-programmable addresses determined by the AD1 and AD0 bits.

Write Operation

There are three specific modes in which data can be written to the AD5383 DAC.

4-Byte Mode

When writing to the AD5383 DACs, the user must begin with an address byte (R/$\overline{\text{W}}$ = 0) after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte; this addresses the specific channel in the DAC to be addressed and is also acknowledged by the DAC. Two bytes of data are then written to the DAC, as shown in Figure 31. A STOP condition follows. This allows the user to update a single channel within the AD5383 at any time and requires four bytes of data to be transferred from the master.

3-Byte Mode

In 3-byte mode, the user can update more than one channel in a write sequence without having to write the device address byte each time. The device address byte is only required once; subsequent channel updates require the pointer byte and the data bytes. In 3-byte mode, the user begins with an address byte (R/$\overline{\text{W}}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte. This addresses the specific channel in the DAC to be addressed and is also acknowledged by the DAC. This is then followed by the two data bytes. REG1 and REG0 determine the register to be updated.

If a STOP condition does not follow the data bytes, another channel can be updated by sending a new pointer byte followed by the data bytes. This mode only requires three bytes to be sent to update any channel once the device has been initially addressed, and reduces the software overhead in updating the AD5383 channels. A STOP condition at any time exits this mode. Figure 32 shows a typical configuration.

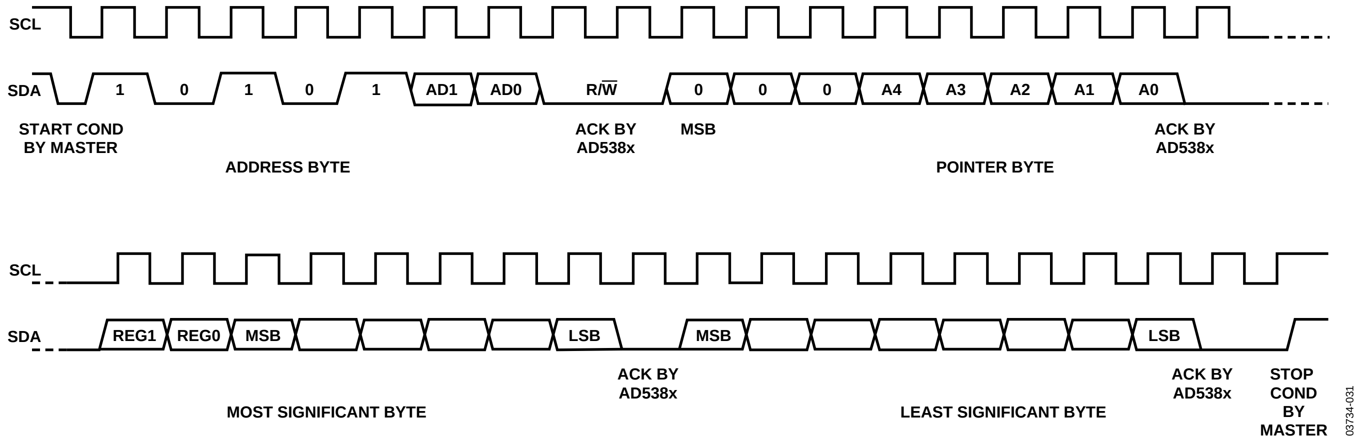


Figure 31. 4-Byte, I²C Write Operation

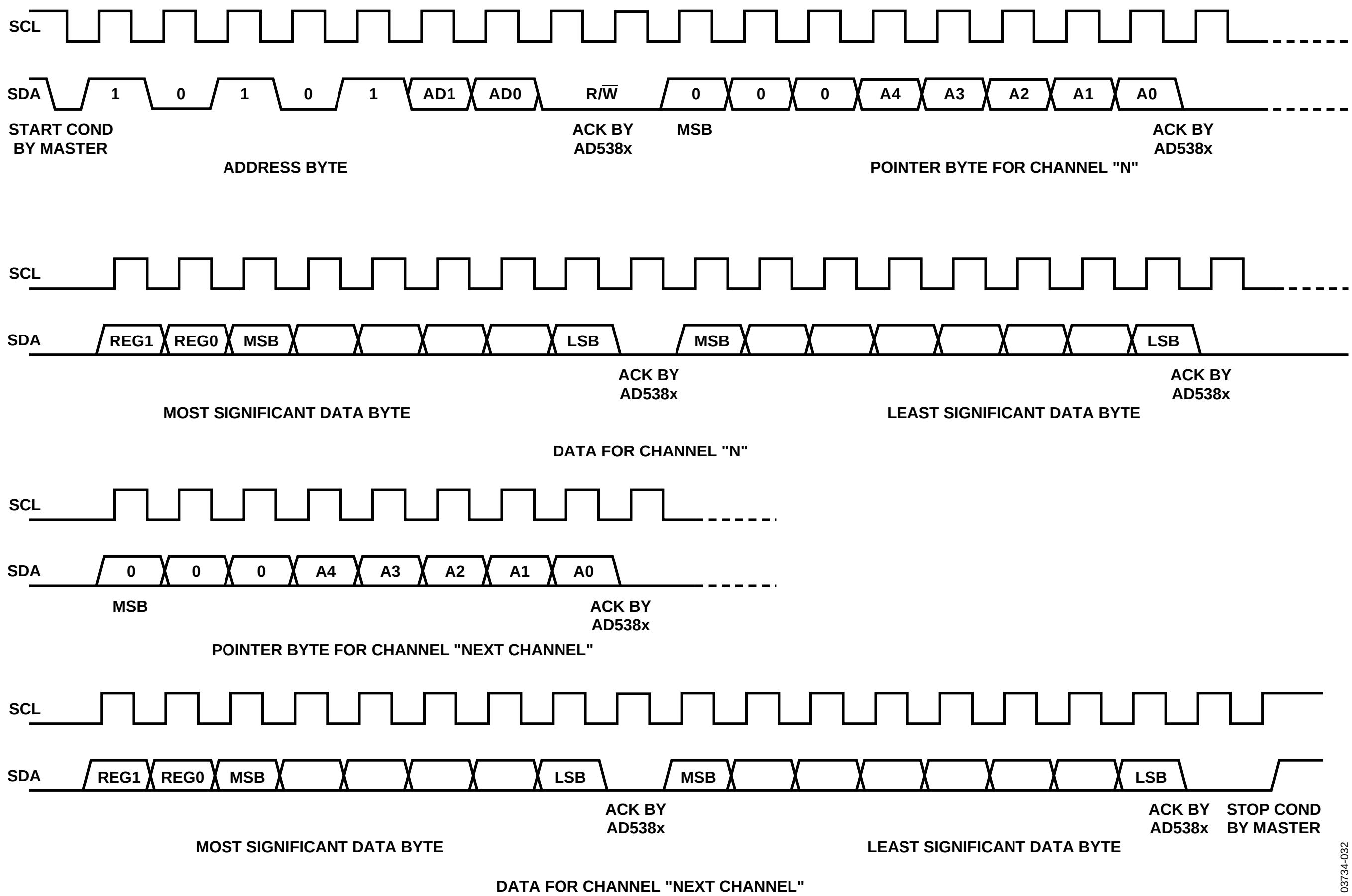


Figure 32. 3-Byte, I²C Write Operation

2-Byte Mode

Following initialization of 2-byte mode, the user can sequentially update channels. The device address byte is only required once, and the address pointer is configured for auto-increment or burst mode.

The user must begin with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte is followed by a specific pointer byte (0xFF) that initiates the burst mode of operation. The address pointer initializes to Channel 0, the data following the pointer is loaded to Channel 0, and the address pointer automatically increments to the next address.

The REG0 and REG1 bits in the data byte determine which register is updated. In this mode, following the initialization, only the two data bytes are required to update a channel. The channel address automatically increments from Address 0 to Channel 31 and then returns to the normal 3-byte mode of operation. This mode allows transmission of data to all channels in one block and reduces the software overhead in configuring all channels. A STOP condition at any time exits this mode. Toggle mode is not supported in 2-byte mode. Figure 33 shows a typical configuration.

PARALLEL INTERFACE

The SER/$\overline{PAR}$ pin must be tied low to enable the parallel interface and disable the serial interfaces. Figure 7 shows the timing diagram for a parallel write. The parallel interface is controlled by the $\overline{CS}$, $\overline{WR}$, REG0, REG1, A4 to A0, and DB11 to DB0 pins.

$\overline{CS}$ Pin

Active low device select pin.

$\overline{WR}$ Pin

On the rising edge of $\overline{WR}$, with $\overline{CS}$ low, the addresses on Pin A4 to Pin A0 are latched; data present on the data bus is loaded into the selected input registers.

REG0, REG1 Pins

The REG0 and REG1 pins determine the destination register of the data being written to the AD5383. See Table 9.

Pins A4 to A0

Each of the 32 DAC channels can be addressed individually.

Pins DB11 to DB0

The AD5383 accepts a straight 12-bit parallel word on DB11 to DB0, where DB11 is the MSB and DB0 is the LSB.

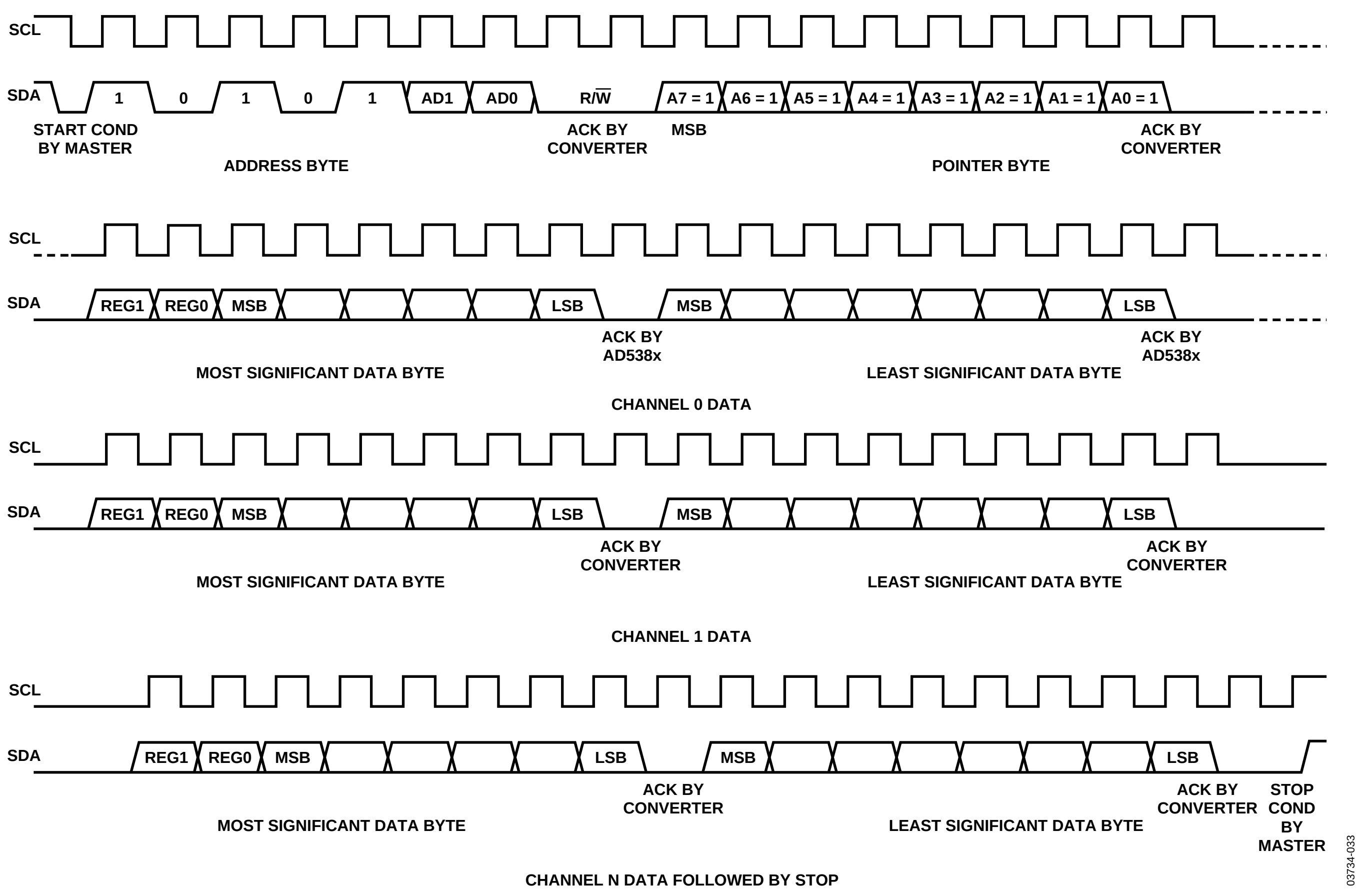


Figure 33. 2-Byte, I²C Write Operation

MICROPROCESSOR INTERFACING

Parallel Interface

The AD5383 can be interfaced to a variety of 16-bit microcontrollers or DSP processors. Figure 35 shows the AD5383 family interfaced to a generic 16-bit microcontroller/DSP processor. The lower address lines from the processor are connected to A0 to A4 on the AD5383. The upper address lines are decoded to provide a $\overline{\text{CS}}$, $\overline{\text{LDAC}}$ signal for the AD5383. The fast interface timing of the AD5383 allows direct interface to a wide variety of microcontrollers and DSPs, as shown in Figure 35.

AD5383 to MC68HC11

The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1), the clock polarity bit (CPOL) = 0, and the clock phase bit (CPHA) = 1. The SPI is configured by writing to the SPI control register (SPCR)—see the *68HC11 User Manual*. SCK of the 68HC11 drives the SCLK of the AD5383, the MOSI output drives the serial data line (DIN) of the AD5383, and the MISO input is driven from DOUT. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5383, the $\overline{\text{SYNC}}$ line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle.

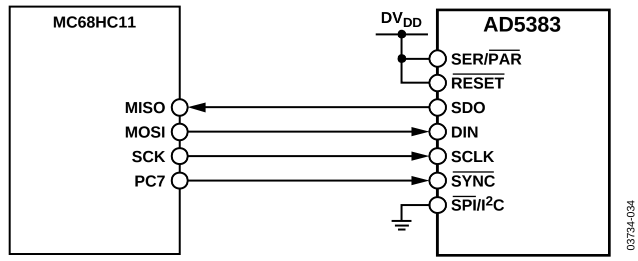


Figure 34. AD5383-to-MC68HC11 Interface

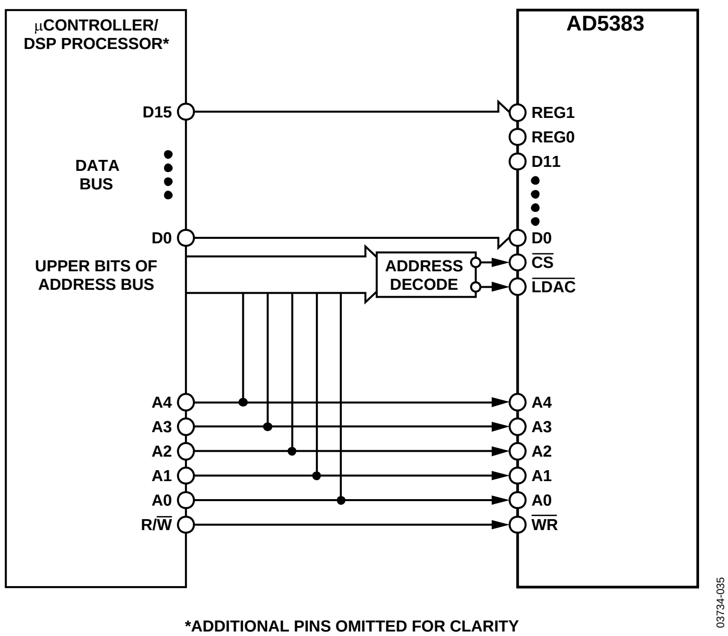


Figure 35. AD5383-to-Parallel Interface

AD5383 to PIC16C6x/7x

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit = 0. This is done by writing to the synchronous serial port control register (SSPCON). See the *PIC16/17 Microcontroller User Manual*. In this example I/O, Port RA1 is being used to pulse SYNC and enable the serial port of the AD5383. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive read/write operations may be needed depending on the mode. Figure 36 shows the connection diagram.

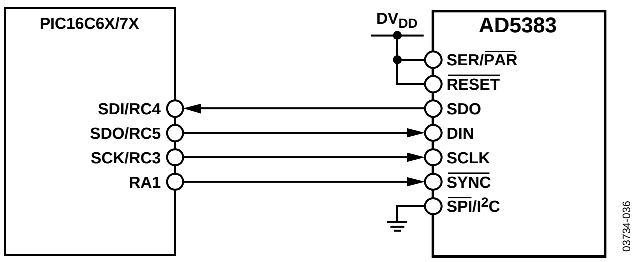


Figure 36. AD5383-to-PIC16C6x/7x Interface

AD5383 to 8051

The AD5383 requires a clock synchronized to the serial data. Therefore, the 8051 serial interface must be operated in Mode 0. In this mode, serial data enters and exits through RxD, and a shift clock is output on TxD. Figure 37 shows how the 8051 is connected to the AD5383. Because the AD5383 shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. The AD5383 requires its data to be MSB first. Since the 8051 outputs the LSB first, the transmit routine must take this into account.

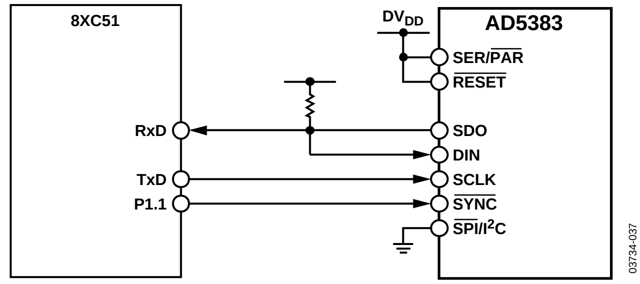
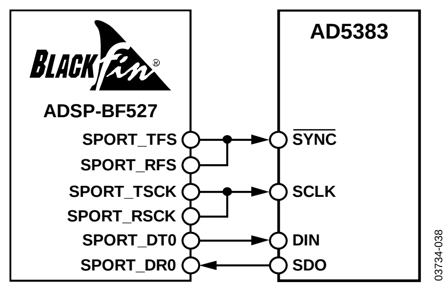


Figure 37. AD5383-to-8051 Interface

AD5383 to ADSP-BF527

Figure 38 shows a serial interface between the AD5383 and the ADSP-BF527. The ADSP-BF527 should be set up to operate in SPORT transmit alternate framing mode. The ADSP-BF527 SPORT is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.



* ADDITIONAL PINS OMITTED FOR CLARITY

Figure 38. AD5383 to ADSP-BF527 Interface

APPLICATIONS INFORMATION

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5383 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5383 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only, a star ground point established as close to the device as possible.

For supplies with multiple pins (AV_{DD}, DV_{DD}), these pins should be tied together. The AD5383 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible and ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

The power supply lines of the AD5383 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the DIN and SCLK lines will help reduce crosstalk between them (this is not required on a multilayer board because there will be a separate ground plane, but separating the lines will help). It is essential to minimize noise on the V_{IN} and REFIN lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A micro-strip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

POWER SUPPLY SEQUENCING

For proper operation of the AD5383, apply DV_{DD} first and then AV_{DD} either simultaneously or within 10 ms of DV_{DD}. This sequence ensures that the power-on reset circuitry sets the registers to their default values and keeps the analog outputs at 0 V until a valid write operation takes place. When AV_{DD} cannot be applied within 10 ms of DV_{DD}, issue a hardware reset. This triggers the power-on reset circuitry and loads the default register values. In cases where the initial power supply has the same or a lower voltage than the second power supply, a Schottky diode can be used to temporarily supply power until the second power supply turns on. Table 18 lists the power supply sequences and the recommended diode connections. Alternatively, a load switch such as the ADP196 can be used to delay the first power supply until the second power supply turns on. Figure 41 shows a typical configuration using the ADP196. In this case, the AV_{DD} is applied first. This voltage does not appear at the AV_{DD} pin of the AD5383 until the DV_{DD} is applied and brings the EN pin high. The result is that the AV_{DD} and the DV_{DD} are both applied to the AD5383 at the same time.

Table 18. Power Supply Sequencing

First Power Supply	Second Power Supply	Recommended Operation
AV_{DD} = 3 V	DV_{DD} ≥ 3 V	See Figure 39
DV_{DD} = 3 V	AV_{DD} ≥ 3 V	See Figure 40
AV_{DD} = DV_{DD}	DV_{DD} = AV_{DD}	See Figure 39; this operation assumes separate analog and digital supplies
DV_{DD} = AV_{DD}	AV_{DD} = DV_{DD}	See Figure 40; this operation assumes separate analog and digital supplies
AV_{DD} = 5 V	DV_{DD} = 3 V	See Figure 41
DV_{DD} = 5 V	AV_{DD} = 3 V	Hardware reset or see Figure 42

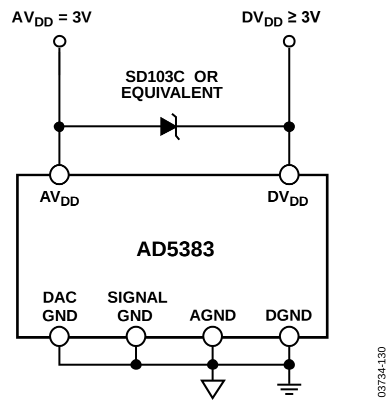


Figure 39. AV_{DD} First, Followed by DV_{DD}

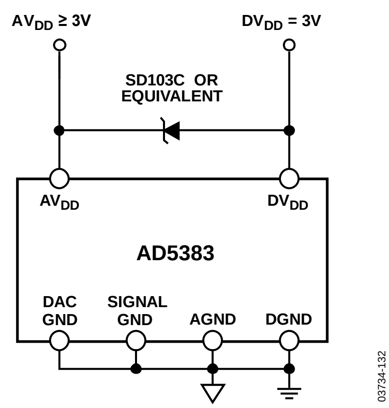


Figure 40. DV_{DD} First, Followed by AV_{DD}

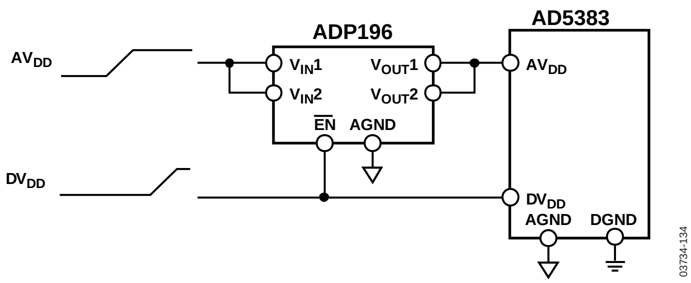


Figure 41. DV_{DD} Power Supply Controlled by a Load Switch

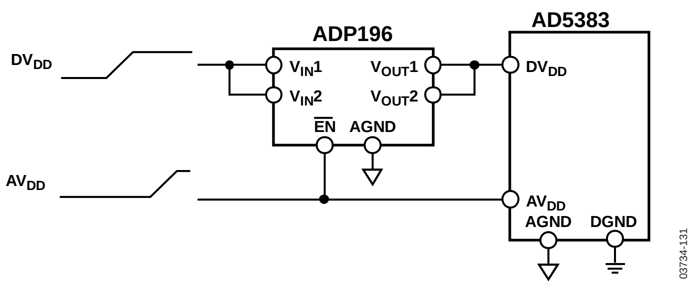


Figure 42. AV_{DD} Power Supply Controlled by a Load Switch

TYPICAL CONFIGURATION CIRCUIT

Figure 43 shows a typical configuration for the AD5383-5 when configured for use with an external reference. In the circuit shown, all AGND, SIGNAL_GND, and DAC_GND pins are tied together to a common AGND. AGND and DGND are connected together at the AD5383 device. On power-up, the AD5383 defaults to external reference operation. All AV_{DD} lines are connected together and driven from the same 5 V source. It is recommended to decouple close to the device with a 0.1 µF ceramic and a 10 µF tantalum capacitor. In this application, the reference for the AD5383-5 is provided externally from either an ADR421 or ADR431 2.5 V reference. Suitable external references for the AD5383-3 include the ADR3412 1.2 V reference. The reference should be decoupled at the REFOUT/ REFIN pin of the device with a 0.1 µF capacitor.

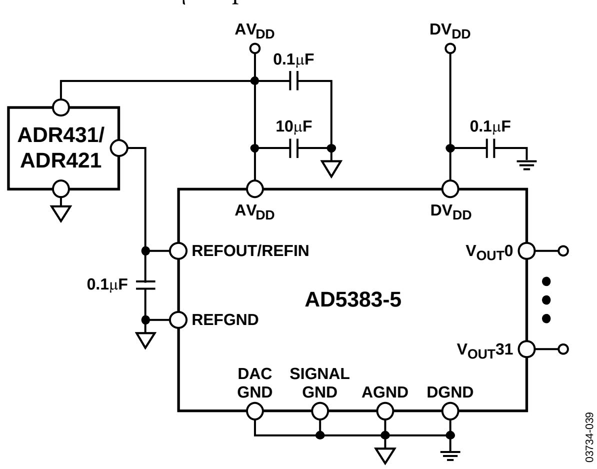


Figure 43. Typical Configuration with External Reference

Figure 44 shows a typical configuration when using the internal reference. On power-up, the AD5383 defaults to an external reference; therefore, the internal reference needs to be configured and turned on via a write to the AD5383 control register. Control Register Bit CR10 allows the user to choose the reference value; Bit CR 8 is used to select the internal reference. It is recommended to use the 2.5 V reference when AV_{DD} = 5 V, and the 1.25 V reference when AV_{DD} = 3 V.

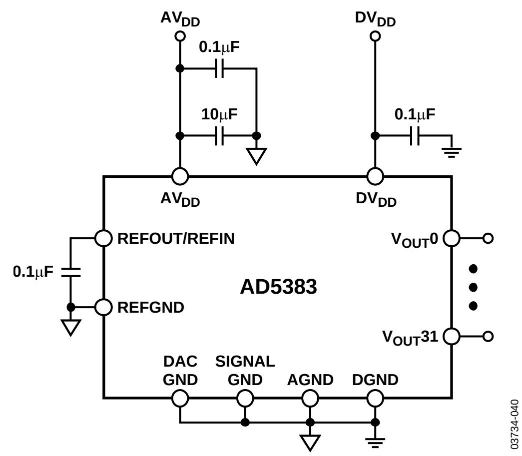


Figure 44. Typical Configuration with Internal Reference

Digital connections have been omitted for clarity. The AD5383 contains an internal power-on reset circuit with a 10 ms brownout time. If the power supply ramp rate exceeds 10 ms, the user should reset the AD5383 as part of the initialization process to ensure the calibration data gets loaded correctly into the device.

CHANNEL MONITOR FUNCTION

The AD5383 contains a channel monitor function that consists of a multiplexer addressed via the interface, allowing any channel output to be routed to this pin for monitoring using an external ADC. The channel monitor function must be enabled in the control register before any channels are routed to MON_OUT. Table 16 contains the decoding information needed to route any channel to MON_OUT. To three-state MON_OUT, select Channel Address 63. Figure 45 shows a typical monitoring circuit using a 12-bit SAR ADC in a 6-lead SOT-23 package. The controller output port selects the channel to be monitored, and the input port reads the converted data from the ADC.

TOGGLE MODE FUNCTION

The toggle mode function allows an output signal to be generated using the $\overline{\text{LDAC}}$ control signal that switches between two DAC data registers. This function is configured using the SFR control register as follows. A write with REG1 = REG0 = 0 and A4 to A0 = 01100 specifies a control register write. The toggle mode function is enabled in groups of eight channels using Bit CR3 to Bit CR0 in the control register. See the AD5383 Control Register Write/Read section. Figure 46 shows a block diagram of toggle mode implementation. Each of the 32 DAC channels on the AD5383 contain an A and B data register. Note that the B registers can only be loaded when toggle mode is enabled. The sequence of events when configuring the AD5383 for toggle mode is:

1. Enable toggle mode for the required channels via the control register.
2. Load data to A registers.
3. Load data to B registers.
4. Apply $\overline{\text{LDAC}}$.

The $\overline{\text{LDAC}}$ is used to switch between the A and B registers in determining the analog output. The first $\overline{\text{LDAC}}$ configures the output to reflect data in the A registers. This mode offers significant advantages if the user wants to generate a square wave at the output of all 32 channels, as might be required to drive a liquid crystal-based variable optical attenuator. In this case, the user writes to the control register and enables the toggle function by setting CR3 to CR2 = 1, thus enabling the four groups of eight for toggle mode operation. The user must then load data to all 32 A and B registers. Toggling $\overline{\text{LDAC}}$ sets the output values to reflect the data in the A and B registers. The frequency of the $\overline{\text{LDAC}}$ determines the frequency of the square wave output.

Toggle mode is disabled via the control register. The first $\overline{\text{LDAC}}$ following the disabling of the toggle mode updates the outputs with the data contained in the A registers.

THERMAL MONITOR FUNCTION

The AD5383 contains a temperature shutdown function to protect the chip in case multiple outputs are shorted. The short circuit current of each output amplifier is typically 40 mA. Operating the AD5383 at 5 V results in power dissipation of 200 mW per shorted amplifier. With five channels shorted, this amounts to an extra watt of power dissipation. For the 100-lead LQFP, the θ_{JA} is typically 44°C/W.

The thermal monitor is enabled by the user via CR6 in the control register. The output amplifiers on the AD5383 are automatically powered down if the die temperature exceeds approximately 130°C. After a thermal shutdown has occurred, the user can re-enable the part by executing a soft power-up if the temperature has dropped below 130°C or by turning off the thermal monitor function via the control register.

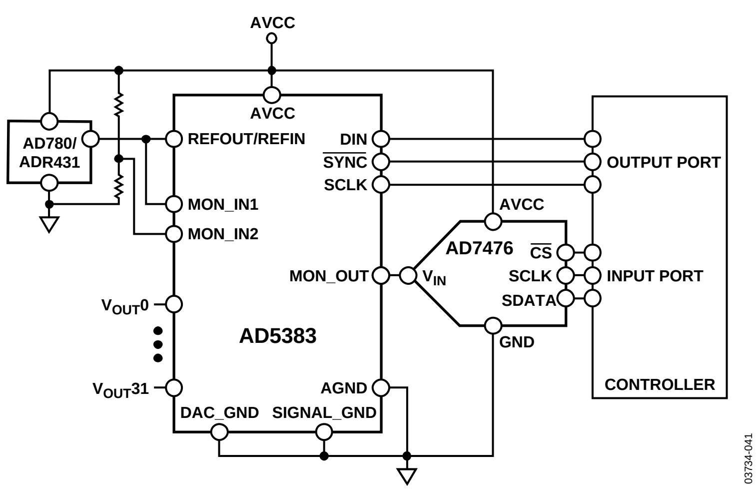


Figure 45. Typical Channel Monitoring Circuit

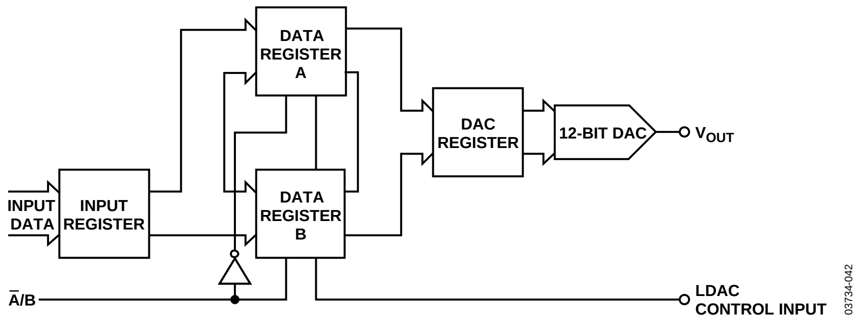


Figure 46. Toggle Mode Function

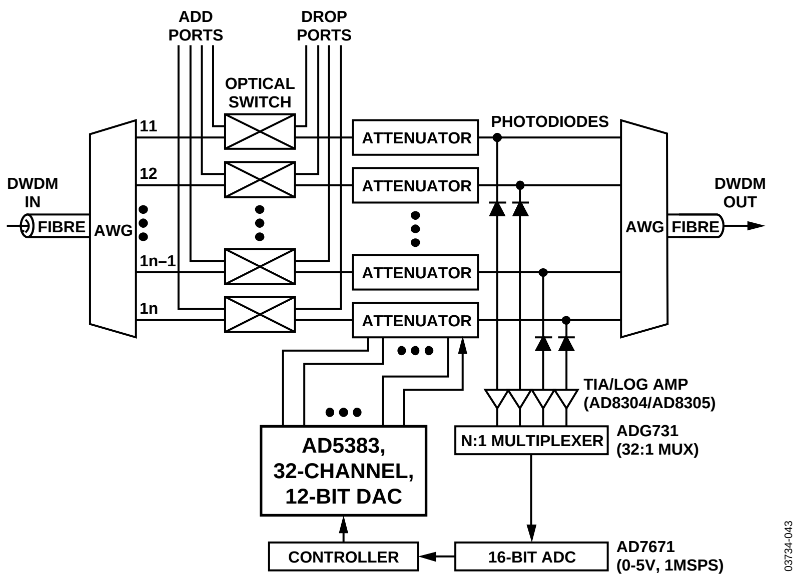


Figure 47. OADM Using the AD5383 as Part of an Optical Attenuator

OPTICAL ATTENUATORS

Based on its high channel count, high resolution, monotonic behavior, and high level of integration, the AD5383 is ideally targeted at optical attenuation applications used in dynamic gain equalizers, variable optical attenuators (VOA), and optical add-drop multiplexers (OADM). In these applications, each wavelength is individually extracted using an arrayed wave guide; its power is monitored using a photodiode, transimpedance amplifier and ADC in a closed-loop control system. The AD5383 controls the optical attenuator for each wavelength, ensuring that the power is equalized in all wavelengths before being multiplexed onto the fiber. This prevents information loss and saturation from occurring at amplification stages further along the fiber.

UTILIZING THE FIFO

The AD5383 FIFO mode optimizes total system update rates in applications where a large number of channels need to be updated. FIFO mode is only available when parallel interface mode is selected. The FIFO EN pin is used to enable the FIFO. The status of FIFO EN is sampled during the initialization sequence. Therefore, the FIFO status can only be changed by resetting the device. In a telescope that provides for the cancellation of atmospheric distortion, for example, a large number of channels need to be updated in a short period of time. In such systems, as many as 320 channels need to be updated within 25 µs to 30 µs. 320 channels require the use of 10 AD5383s. With FIFO mode enabled, the data write cycle time is 40 ns; therefore, each group consisting of 32 channels can be fully loaded in 1.28 µs. In FIFO mode, a complete group of 32 channels updates in 11.5 µs. The time taken to update all 320 channels is 11.5 µs + 9 × 1.28 µs = 23 µs. Figure 48 shows the FIFO operation scheme.

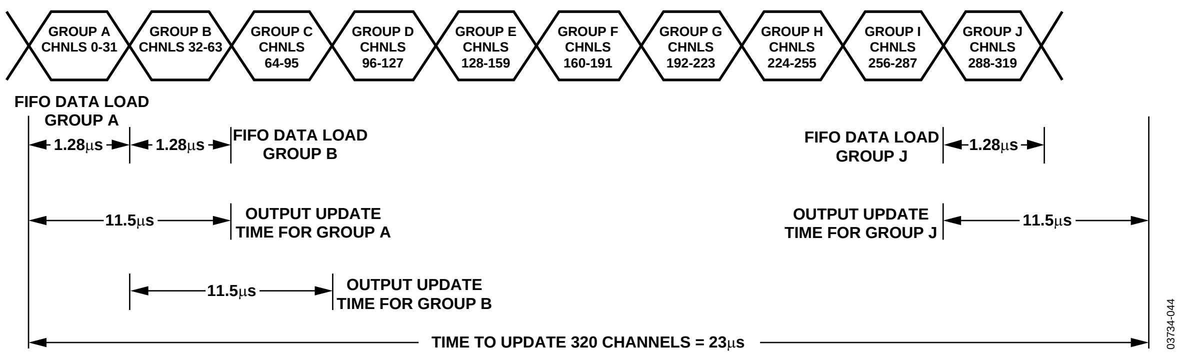


Figure 48. Using FIFO Mode 320 Channels Updated in Under 25 µs

OUTLINE DIMENSIONS

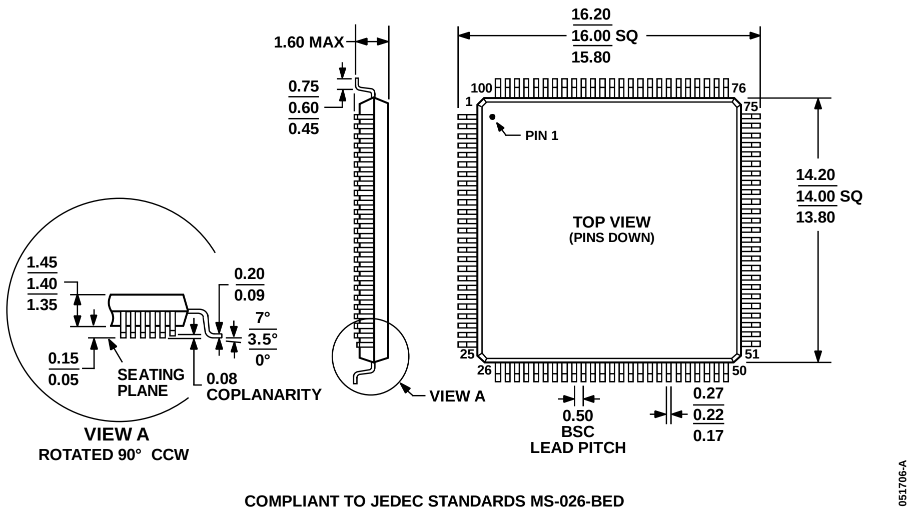


Figure 49. 100-Lead Low Profile Quad Flat Package [LQFP]
(ST-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution	Temperature Range	AV_{DD} Range	Output Channels	Linearity Error	Package Description	Package Option
AD5383BSTZ-3	12 Bits	−40°C to +85°C	2.7 V to 3.6 V	32	±1 LSB	100-Lead LQFP	ST-100-1
AD5383BSTZ-5	12 Bits	−40°C to +85°C	4.5 V to 5.5 V	32	±1 LSB	100-Lead LQFP	ST-100-1

[1] Z = RoHS Compliant Part.

NOTES

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D03734-0-5/14(D)