Dual, 16-/12-Bit *nano*DAC+ with 2 ppm/°C Reference, SPI Interface

Data Sheet

AD5689R/AD5687R

FEATURES

High relative accuracy (INL): ±2 LSB maximum at 16 bits
Low drift 2.5 V reference: 2 ppm/°C typical
Tiny package: 3 mm × 3 mm, 16-lead LFCSP
TUE: ±0.1% of FSR maximum
Offset error: ±1.5 mV maximum
Gain error: ±0.1% of FSR maximum
High drive capability: 20 mA, 0.5 V from supply rails
User-selectable gain of 1 or 2 (GAIN pin)
Reset to zero scale or midscale (RSTSEL pin)
1.8 V logic compatibility
50 MHz SPI with readback or daisy chain
Low glitch: 0.5 nV-sec
Low power: 3.3 mW at 3 V
2.7 V to 5.5 V power supply
−40°C to +105°C temperature range
AEC-Q100 qualified for automotive applications

APPLICATIONS

Optical transceivers
Base station power amplifiers
Process control (PLC I/O cards)
Industrial automation
Data acquisition systems

GENERAL DESCRIPTION

The AD5689R/AD5687R members of the *nano*DAC+™ family are low power, dual, 16-/12-bit buffered voltage output digital-to-analog converters (DACs). The devices include a 2.5 V, 2 ppm/°C internal reference (enabled by default) and a gain select pin giving a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). The devices operate from a single 2.7 V to 5.5 V supply, are guaranteed monotonic by design, and exhibit less than 0.1% FSR gain error and 1.5 mV offset error performance. Both devices are available in a 3 mm × 3 mm LFCSP and a TSSOP package.

The AD5689R/AD5687R also incorporate a power-on reset circuit and a RSTSEL pin that ensure that the DAC outputs power up to zero scale or midscale and remain there until a valid write takes place. Each part contains a per channel power-down feature that reduces the current consumption of the device to 4 µA at 3 V while in power-down mode.

The AD5689R/AD5687R use a versatile serial peripheral interface (SPI) that operates at clock rates up to 50 MHz. Both devices contain a V_{LOGIC} pin that is intended for 1.8 V/3 V/5 V logic.

FUNCTIONAL BLOCK DIAGRAM

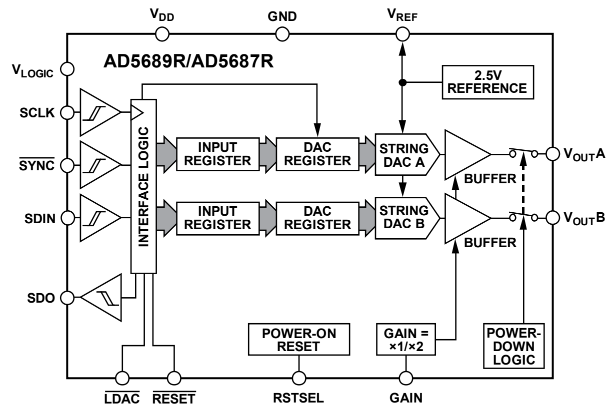

Figure 1.

Table 1. Dual *nano*DAC+ Devices

Interface	Reference	16-Bit	12-Bit
SPI	Internal	AD5689R	AD5687R
	External	AD5689	AD5687
I²C	Internal		AD5697R

PRODUCT HIGHLIGHTS

1. High Relative Accuracy (INL).
   AD5689R (16-bit): ±2 LSB maximum
   AD5687R (12-bit): ±1 LSB maximum
2. Low Drift 2.5 V On-Chip Reference.
   2 ppm/°C typical temperature coefficient
   5 ppm/°C maximum temperature coefficient
3. Two Package Options.
   3 mm × 3 mm, 16-lead LFCSP
   16-lead TSSOP

Rev. C Document Feedback

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2/2013—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. R_L = 2 kΩ; C_L = 200 pF.

Table 2.

Parameter	A Grade[1] Min	A Grade[1] Typ	A Grade[1] Max	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[2]								
AD5689R								
Resolution	16			16			Bits	
Relative Accuracy		±2	±8		±1	±2	LSB	Gain = 2
		±2	±8		±1	±3		Gain = 1
					±1	±3		AD5689RWBCPZ-RL7, Gain = 2
					±1	±4		AD5689RWBCPZ-RL7, Gain = 1
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design
AD5687R								
Resolution	12			12			Bits	
Relative Accuracy		±0.12	±2		±0.12	±1	LSB	
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design
Zero-Code Error		0.4	4		0.4	1.5	mV	All 0s loaded to DAC register
Offset Error		+0.1	±4		+0.1	±1.5	mV	
Full-Scale Error		+0.01	±0.2		+0.01	±0.1	% of FSR	All 1s loaded to DAC register
Gain Error		±0.02	±0.2		±0.02	±0.1	% of FSR	
Total Unadjusted Error		±0.01	±0.25		±0.01	±0.1	% of FSR	External reference; gain = 2; TSSOP
			±0.25			±0.2	% of FSR	Internal reference; gain = 1; TSSOP
Offset Error Drift[3]		±1			±1		µV/°C	
Gain Temperature Coefficient[3]		±1			±1		ppm	Of FSR/°C
DC Power Supply Rejection Ratio[3]		0.15			0.15		mV/V	DAC code = midscale; V_{DD} = 5 V ± 10%
DC Crosstalk[3]								
		±2			±2		µV	Due to single channel, full-scale output change
		±3			±3		µV/mA	Due to load current change
		±2			±2		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{REF}	0		V_{REF}	V	Gain = 1
	0		2 × V_{REF}	0		2 × V_{REF}	V	Gain = 2, see Figure 31
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 1 kΩ
Resistive Load[4]	1			1			kΩ	
Load Regulation		80			80		µV/mA	5 V ± 10%, DAC code = midscale; −30 mA ≤ I_{OUT} ≤ 30 mA
		80			80		µV/mA	3 V ± 10%, DAC code = midscale; −20 mA ≤ I_{OUT} ≤ 20 mA
Short-Circuit Current[5]		40			40		mA	
Load Impedance at Rails[6]		25			25		Ω	See Figure 31
Power-Up Time		2.5			2.5		µs	Coming out of power-down mode; V_{DD} = 5 V

Parameter	A Grade[1] Min	Typ	Max	B Grade[1] Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE OUTPUT								
Output Voltage[7]	2.4975		2.5025	2.4975		2.5025	V	At ambient
Reference Temperature Coefficient[8, 9]		5	20		2	5	ppm/°C	See the Long-Term Temperature Drift section
Output Impedance[3]		0.04			0.04		Ω	
Output Voltage Noise[3]		12			12		μV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density[3]		240			240		nV/√Hz	At ambient; f = 10 kHz, C_L = 10 nF
Load Regulation Sourcing[3]		20			20		μV/mA	At ambient
Load Regulation Sinking[3]		40			40		μV/mA	At ambient
Output Current Load Capability[3]		±5			±5		mA	V_{DD} ≥ 3 V
Line Regulation[3]		100			100		μV/V	At ambient
Thermal Hysteresis[3]		125			125		ppm	First cycle
		25			25		ppm	Additional cycles
LOGIC INPUTS[3]								
Input Current			±2			±2	μA	Per pin
Input Low Voltage (V_{INL})			0.3 × V_{LOGIC}			0.3 × V_{LOGIC}	V	
Input High Voltage (V_{INH})	0.7 × V_{LOGIC}			0.7 × V_{LOGIC}			V	
Pin Capacitance		2			2		pF	
LOGIC OUTPUTS (SDO)[3]								
Output Low Voltage (V_{OL})			0.4			0.4	V	I_{SINK} = 200 μA
Output High Voltage (V_{OH})	V_{LOGIC} − 0.4			V_{LOGIC} − 0.4			V	I_{SOURCE} = 200 μA
Floating State Output Capacitance		4			4		pF	
POWER REQUIREMENTS								
V_{LOGIC}	1.62		5.5	1.62		5.5	V	
I_{LOGIC}			3			3	μA	
V_{DD}	2.7		5.5	2.7		5.5	V	Gain = 1
V_{DD}	V_{REF} + 1.5		5.5	V_{REF} + 1.5		5.5	V	Gain = 2
I_{DD}								V_{IH} = V_{DD}, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V
Normal Mode[10]		0.59	0.7		0.59	0.7	mA	Internal reference off
		1.1	1.3		1.1	1.3	mA	Internal reference on, at full scale
All Power-Down Modes[11]		1	4		1	4	μA	−40°C to +85°C
			6			6	μA	−40°C to +105°C

[1] Temperature range for A and B grades: −40°C to +105°C.
[2] DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV; it exists only when V_{REF} = V_{DD} with gain = 1 or when $V_{REF}/2$ = V_{DD} with gain = 2. Linearity is calculated using a reduced code range of 256 to 65,280 (AD5689R) and 12 to 4080 (AD5687R).
[3] Guaranteed by design and characterization; not production tested.
[4] Channel A can have an output current of up to 30 mA. Similarly, Channel B can have an output current of up to 30 mA, up to a junction temperature of 110°C.
[5] V_{DD} = 5 V. The devices include current limiting that is intended to protect them during temporary overload conditions. Junction temperature may be exceeded during current limit, but operation above the specified maximum operation junction temperature can impair device reliability.
[6] When drawing a load current at either rail, the output voltage headroom, with respect to that rail, is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 31).
[7] Initial accuracy presolder reflow is ±750 μV; output voltage includes the effects of preconditioning drift. See the Internal Reference Setup section.
[8] Reference is trimmed and tested at two temperatures and is characterized from −40°C to +105°C.
[9] Reference temperature coefficient is calculated as per the box method. See the Terminology section for more information.
[10] Interface inactive. Both DACs active. DAC outputs unloaded.
[11] Both DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; 1.8 V − 10% ≤ V_{LOGIC} ≤ 5 V + 10%; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Guaranteed by design and characterization; not production tested.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
Output Voltage Settling Time					
AD5689R		5	8	µs	¼ to ¾ scale settling to ±2 LSB
AD5687R		5	7	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		0.8		V/µs	
Digital-to-Analog Glitch Impulse		0.5		nV-sec	1 LSB change around major carry
Digital Feedthrough		0.13		nV-sec	
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		0.2		nV-sec	
DAC to DAC Crosstalk		0.3		nV-sec	
Total Harmonic Distortion (THD)[3]		−80		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Output Noise Spectral Density (NSD)		300		nV/√Hz	DAC code = midscale, 10 kHz; gain = 2
Output Noise		6		µV p-p	0.1 Hz to 10 Hz
Signal-to-Noise Ratio (SNR)		90		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Spurious Free Dynamic Range (SFDR)		83		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Signal-to-Noise-and-Distortion Ratio (SINAD)		80		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz

[1] See the Terminology section.
[2] Temperature range is −40°C to +105°C, typical at 25°C.
[3] Digitally generated sine wave at 1 kHz.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; V_{REF} = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1]	Symbol	1.62 V ≤ V_{LOGIC} < 2.7 V Min	1.62 V ≤ V_{LOGIC} < 2.7 V Max	2.7 V ≤ V_{LOGIC} ≤ 5.5 V Min	2.7 V ≤ V_{LOGIC} ≤ 5.5 V Max	Unit
SCLK Cycle Time	t_1	20		20		ns
SCLK High Time	t_2	10		10		ns
SCLK Low Time	t_3	10		10		ns
SYNC to SCLK Falling Edge Setup Time	t_4	15		10		ns
Data Setup Time	t_5	5		5		ns
Data Hold Time	t_6	5		5		ns
SCLK Falling Edge to SYNC Rising Edge	t_7	10		10		ns
Minimum SYNC High Time	t_8	20		20		ns
SYNC Rising Edge to SYNC Rising Edge (DAC Register Updates)	t_9	870		830		ns
SYNC Falling Edge to SCLK Fall Ignore	t_{10}	16		10		ns
LDAC Pulse Width Low	t_{11}	15		15		ns
SYNC Rising Edge to LDAC Rising Edge	t_{12}	20		20		ns
SYNC Rising Edge to LDAC Falling Edge	t_{13}	30		30		ns
LDAC Falling Edge to SYNC Rising Edge	t_{14}	840		800		ns
Minimum Pulse Width Low	t_{15}	30		30		ns
Pulse Activation Time	t_{16}	30		30		ns
Power-Up Time[2]		4.5		4.5		μs

[1]Guaranteed by design and characterization; not production tested.
[2] Time to exit power-down to normal mode of AD5689R/AD5687R operation, SYNC rising edge to 90% of DAC midscale value, with output unloaded.

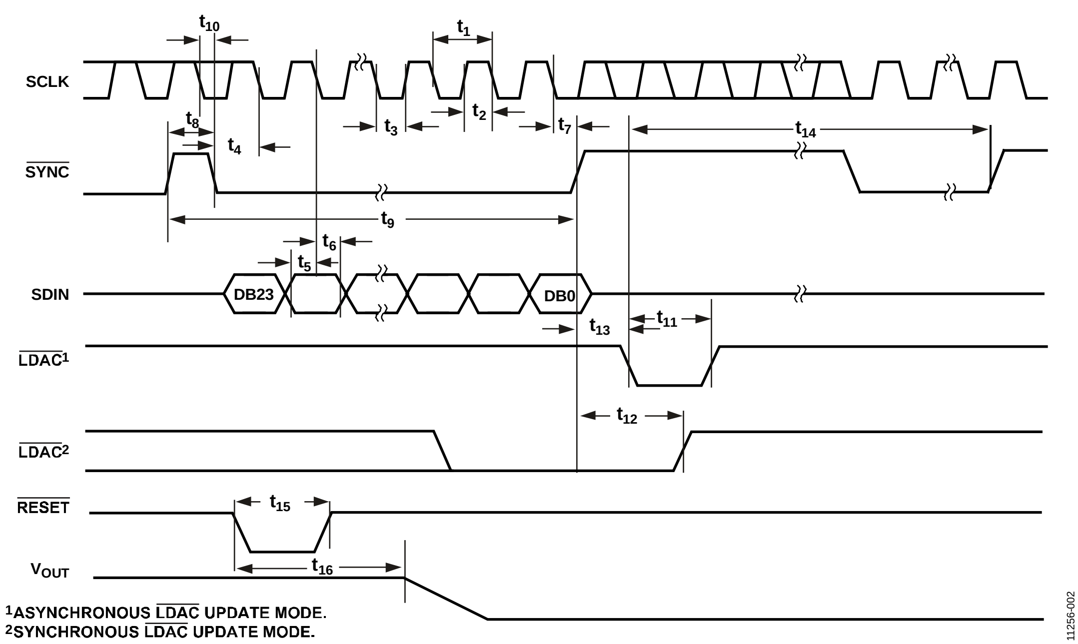


Figure 2. Serial Write Operation

DAISY-CHAIN AND READBACK TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 4 and Figure 5. V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; V_{REF} = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. V_{DD} = 2.7 V to 5.5 V.

Table 5.

		1.62 V ≤ V_{LOGIC} < 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		
Parameter[1]	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCLK Cycle Time	t_1	66		40		ns
SCLK High Time	t_2	33		20		ns
SCLK Low Time	t_3	33		20		ns
$\overline{\text{SYNC}}$ to SCLK Falling Edge	t_4	33		20		ns
Data Setup Time	t_5	5		5		ns
Data Hold Time	t_6	5		5		ns
SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	t_7	15		10		ns
Minimum $\overline{\text{SYNC}}$ High Time	t_8	60		30		ns
SDO Data Valid from SCLK Rising Edge	t_9		45		30	ns
$\overline{\text{SYNC}}$ Rising Edge to SCLK Rising Edge	t_{10}	15		10		ns
$\overline{\text{SYNC}}$ Rising Edge to SDO Disable	t_{11}	60		60		ns

[1] Guaranteed by design and characterization; not production tested.

Circuit and Timing Diagrams

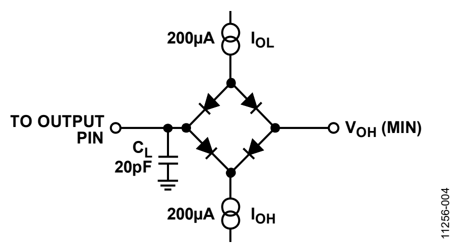


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

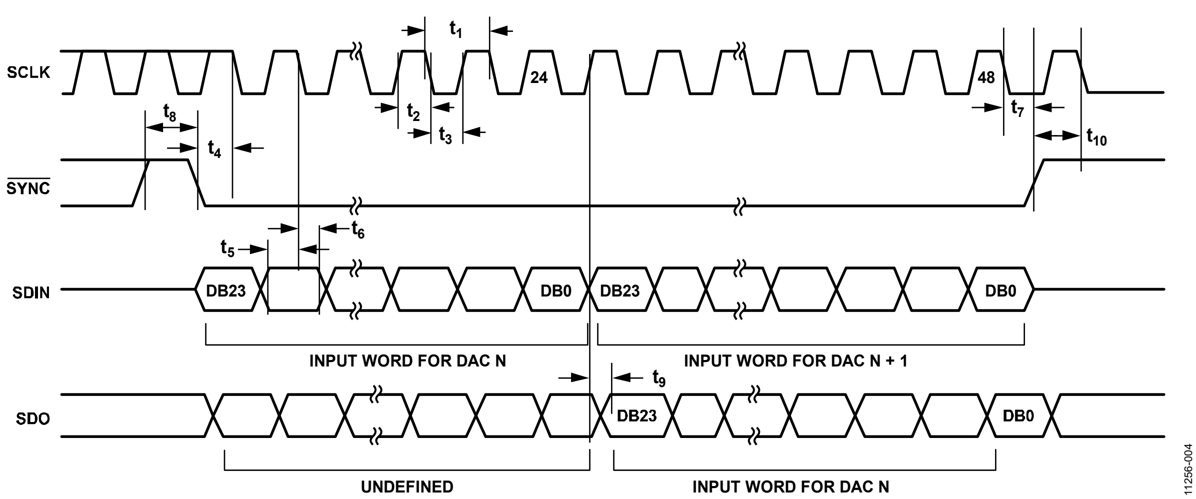


Figure 4. Daisy-Chain Timing Diagram

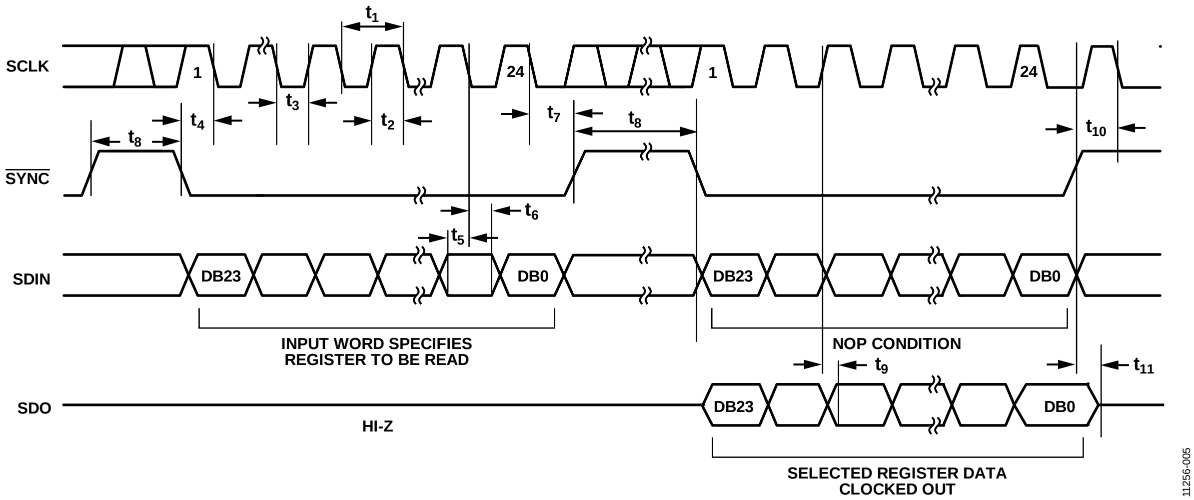


Figure 5. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C
16-Lead TSSOP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	112.6°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	70°C/W
Reflow Soldering Peak Temperature, Pb Free (J-STD-020)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

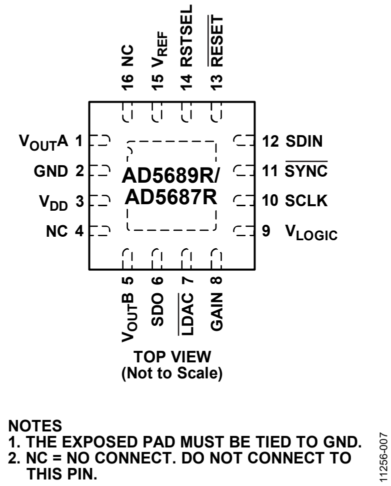


Figure 6. 16-Lead LFCSP Pin Configuration

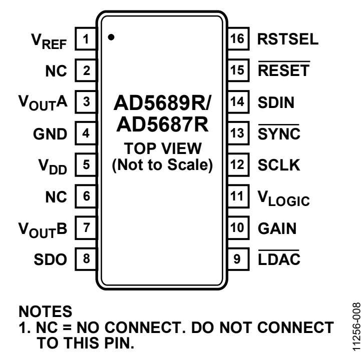


Figure 7. 16-Lead TSSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
LFCSP	TSSOP	Mnemonic	Description
1	3	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	4	GND	Ground Reference Point for All Circuitry on the AD5689R/AD5687R.
3	5	V_{DD}	Power Supply Input. The AD5689R/AD5687R can be operated from 2.7 V to 5.5 V. Decouple the supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	6	NC	No Connect. Do not connect to this pin.
5	7	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
6	8	SDO	Serial Data Output. SDO can be used to daisy-chain a number of AD5689R/AD5687R devices together, or it can be used for readback. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
7	9	$\overline{LDAC}$	$\overline{LDAC}$ can be operated in two modes: asynchronous and synchronous. Pulsing this pin low allows either or both DAC registers to be updated if the input registers have new data; both DAC outputs can be updated simultaneously. This pin can also be tied permanently low.
8	10	GAIN	Gain Select. When this pin is tied to GND, both DACs output a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, both DACs output a span of 0 V to 2 × V_{REF}.
9	11	V_{LOGIC}	Digital Power Supply. The voltage on this pin ranges from 1.62 V to 5.5 V.
10	12	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
11	13	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data is transferred in on the falling edges of the next 24 clocks.
12	14	SDIN	Serial Data Input. This device has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	15	$\overline{RESET}$	Asynchronous Reset Input. The $\overline{RESET}$ input is falling edge sensitive. When $\overline{RESET}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{RESET}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin. If this pin is forced low at power-up, the power-on reset (POR) circuit does not initialize the device correctly until this pin is released.
14	16	RSTSEL	Power-On Reset Select. Tying this pin to GND powers up both DACs to zero scale. Tying this pin to V_{LOGIC} powers up both DACs to midscale.
15	1	V_{REF}	Reference Voltage. The AD5689R/AD5687R have a common reference pin. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference output.
16	2	NC	No Connect. Do not connect to this pin.
17	N/A	EPAD	Exposed Pad. The exposed pad must be tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

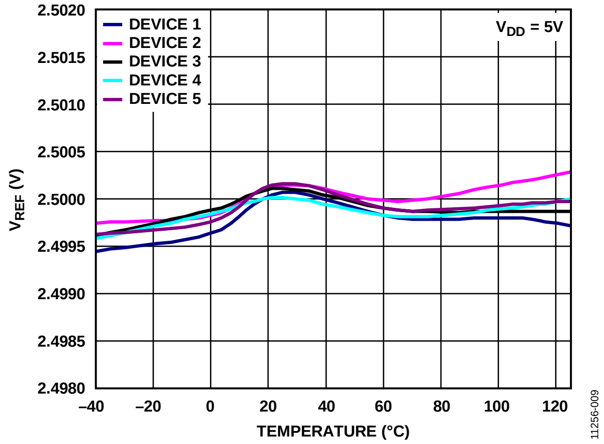


Figure 8. Internal Reference Voltage vs. Temperature (Grade B)

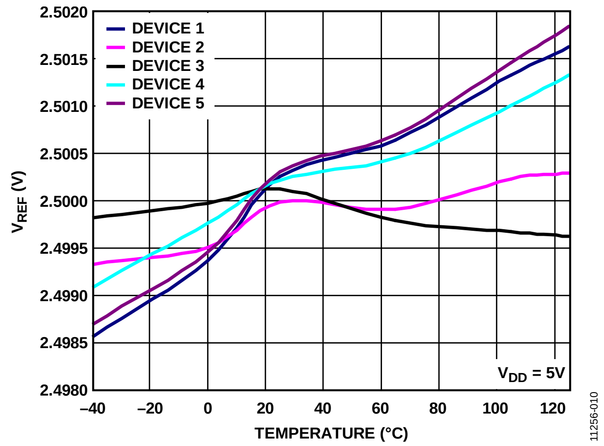


Figure 9. Internal Reference Voltage vs. Temperature (Grade A)

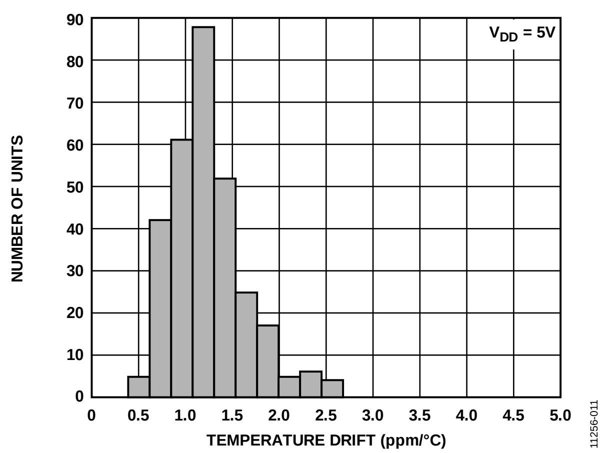


Figure 10. Reference Output Temperature Drift Histogram

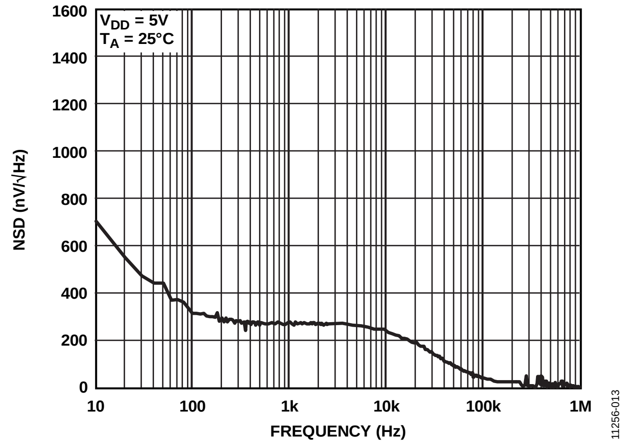


Figure 11. Internal Reference Noise Spectral Density vs. Frequency

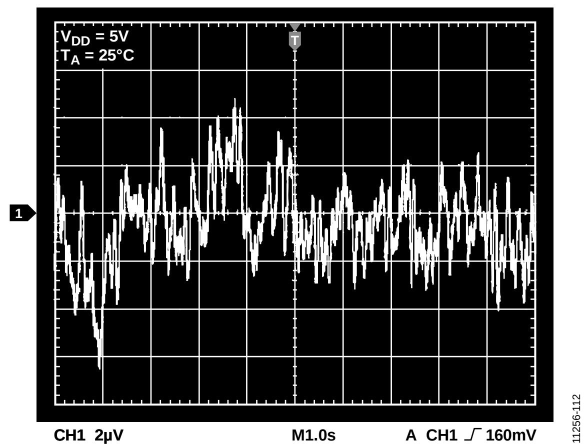


Figure 12. Internal Reference Noise, 0.1 Hz to 10 Hz

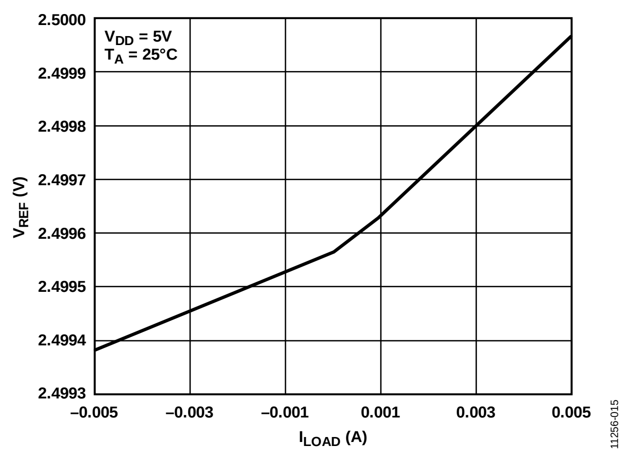


Figure 13. Internal Reference Voltage vs. Load Current

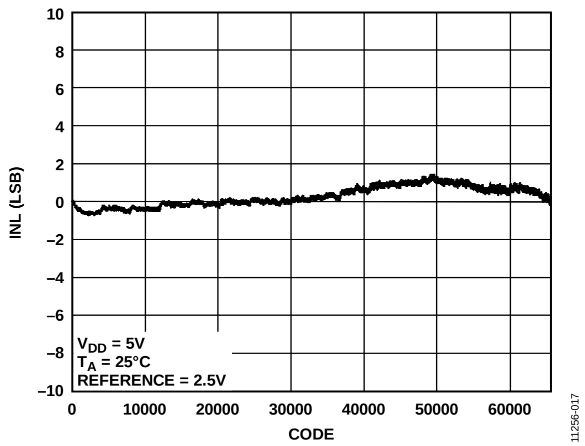


Figure 14. AD5689R Integral Nonlinearity (INL) vs. Code

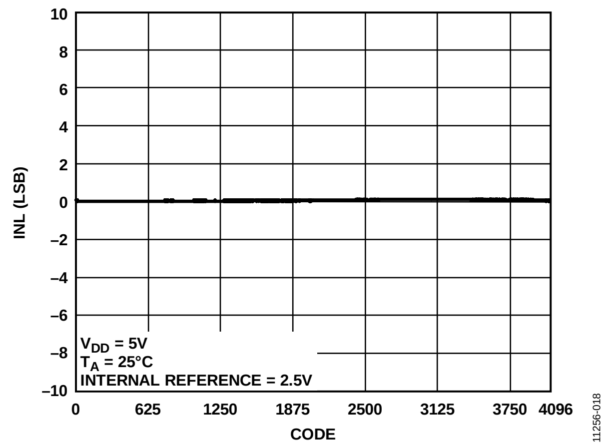


Figure 17. AD5687R INL vs. Code

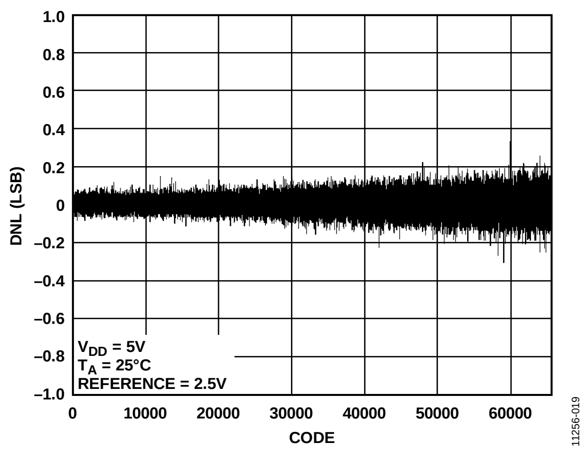


Figure 15. AD5689R Differential Nonlinearity (DNL) vs. Code

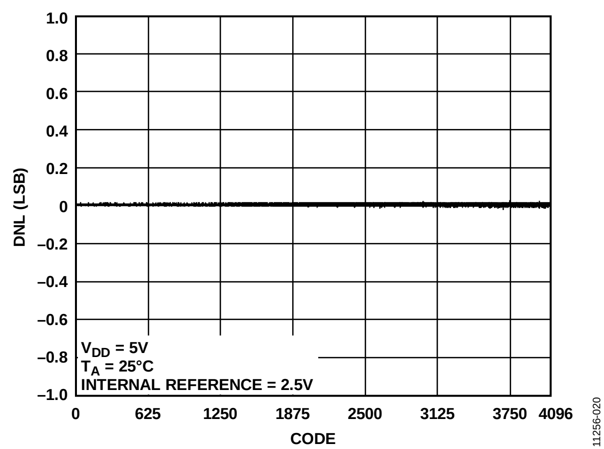


Figure 18. AD5687R DNL vs. Code

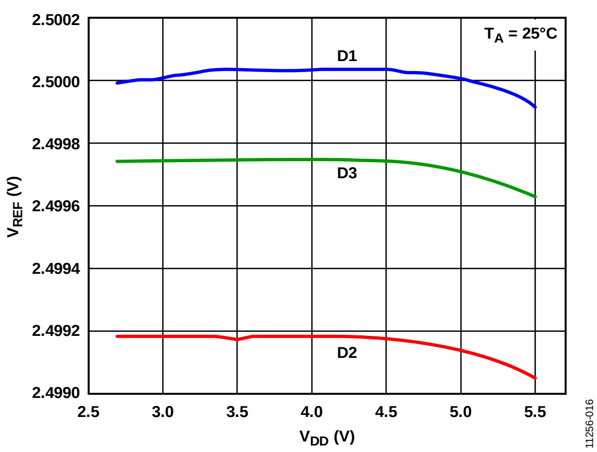


Figure 16. Internal Reference Voltage vs. Supply Voltage

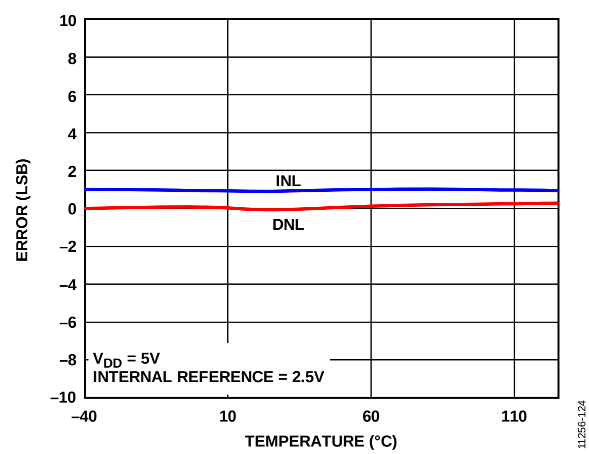


Figure 19. INL Error and DNL Error vs. Temperature

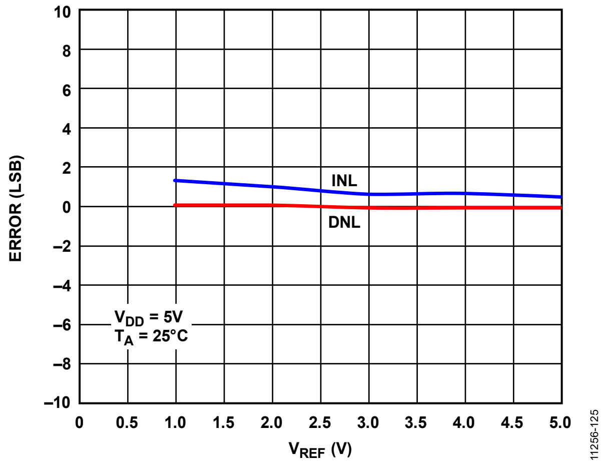


Figure 20. INL Error and DNL Error vs. V_{REF}

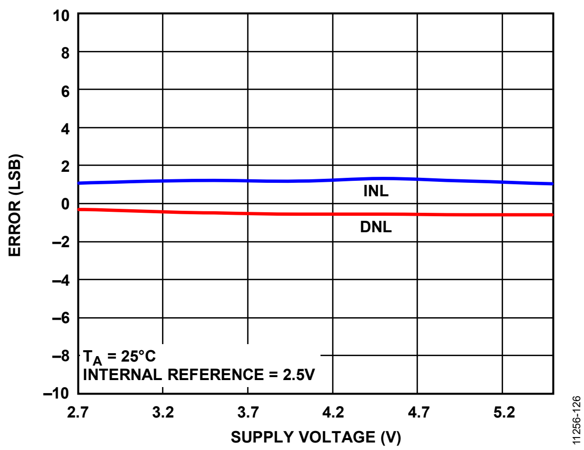


Figure 21. INL Error and DNL Error vs. Supply Voltage

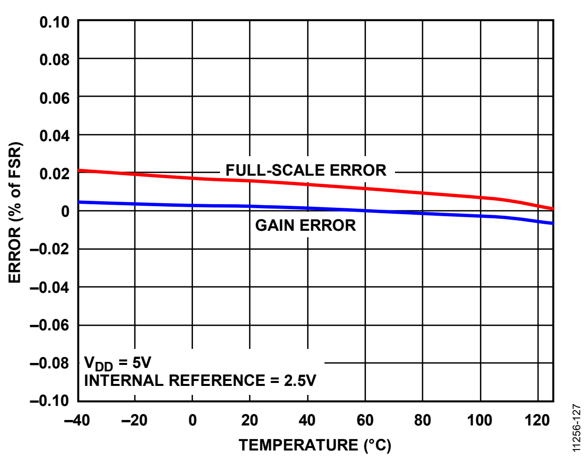


Figure 22. Gain Error and Full-Scale Error vs. Temperature

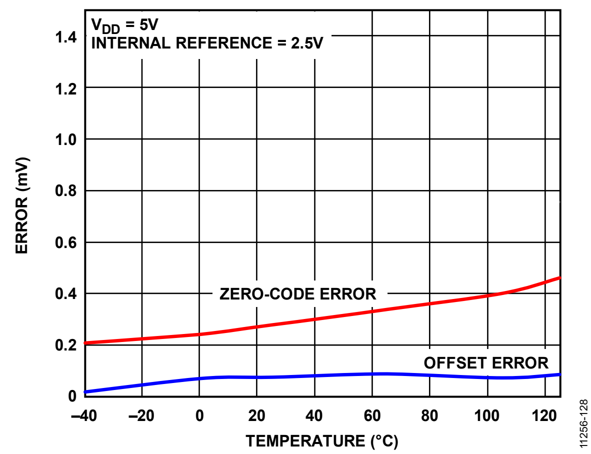


Figure 23. Zero-Code Error and Offset Error vs. Temperature

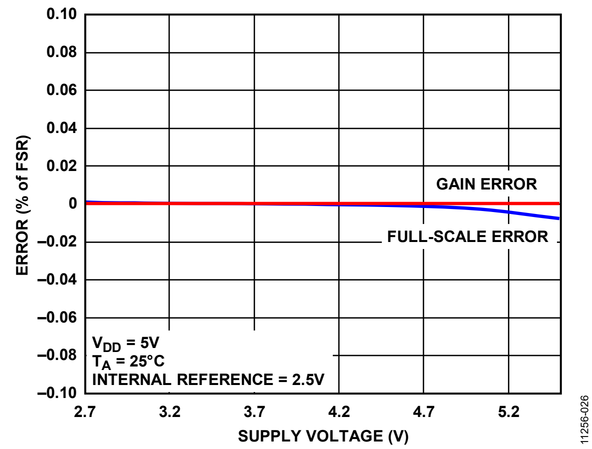


Figure 24. Gain Error and Full-Scale Error vs. Supply

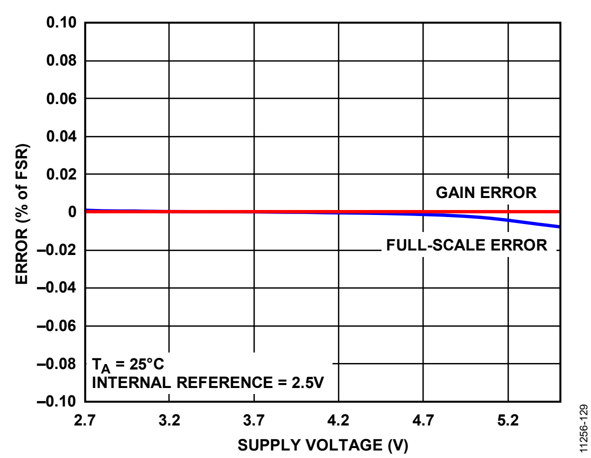


Figure 25. Zero-Code Error and Offset Error vs. Supply Voltage

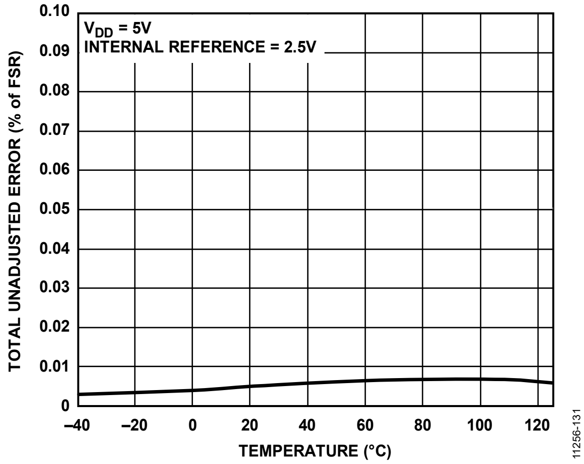


Figure 26. Total Unadjusted Error (TUE) vs. Temperature

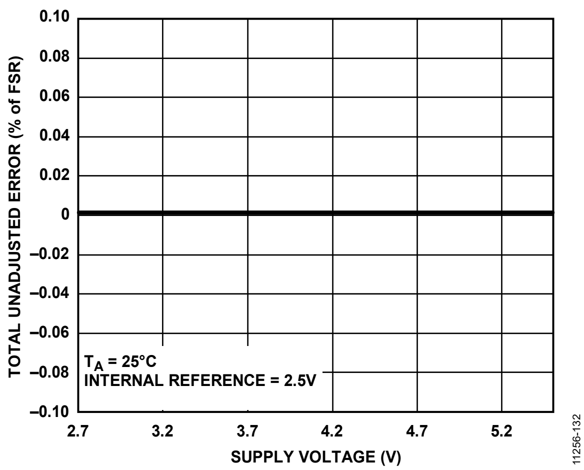


Figure 27. TUE vs. Supply, Gain = 1

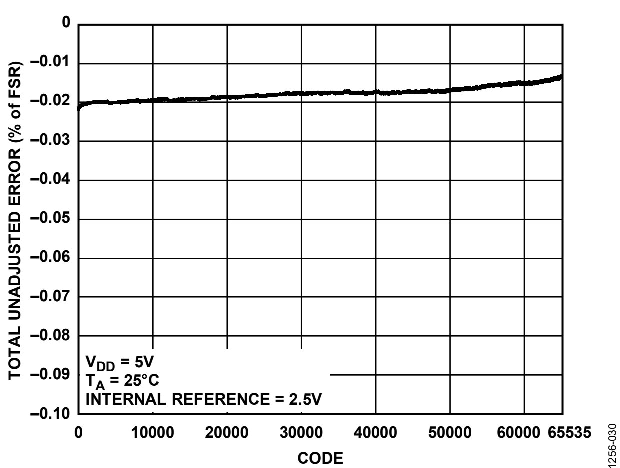


Figure 28. TUE vs. Code

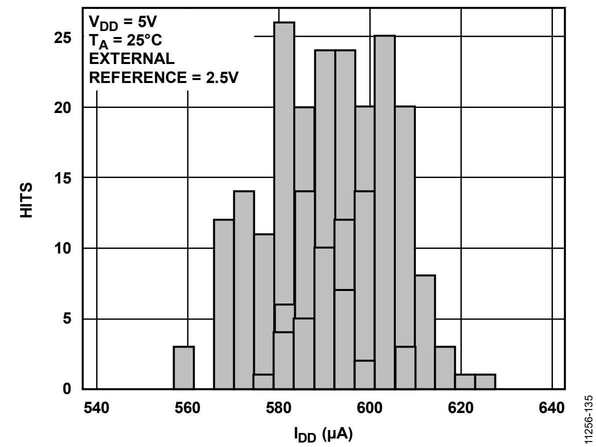


Figure 29. I_{DD} Histogram with External Reference, V_{DD} = 5 V

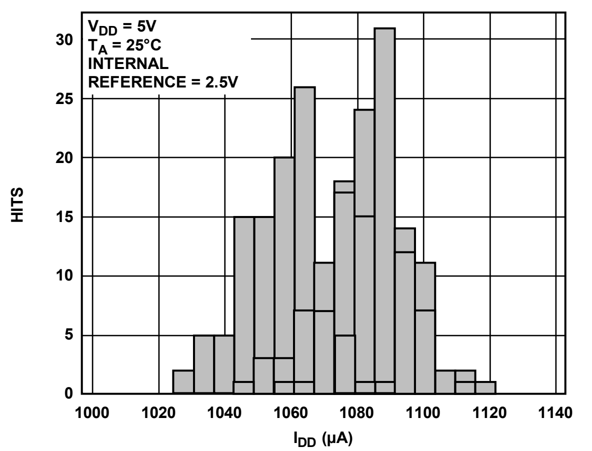


Figure 30. I_{DD} Histogram with Internal Reference, V_{REF} = 2.5 V, Gain = 2

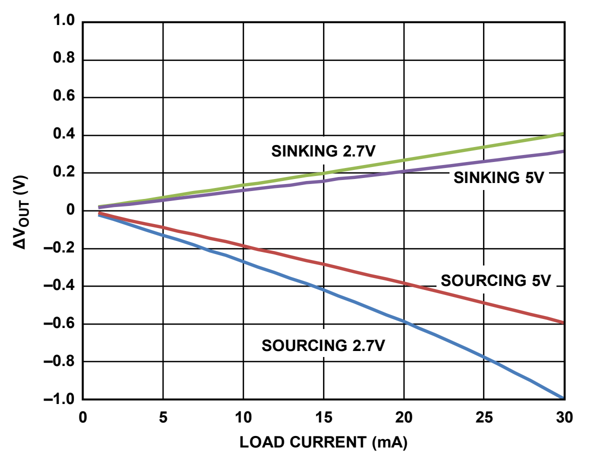


Figure 31. Headroom/Footroom vs. Load Current

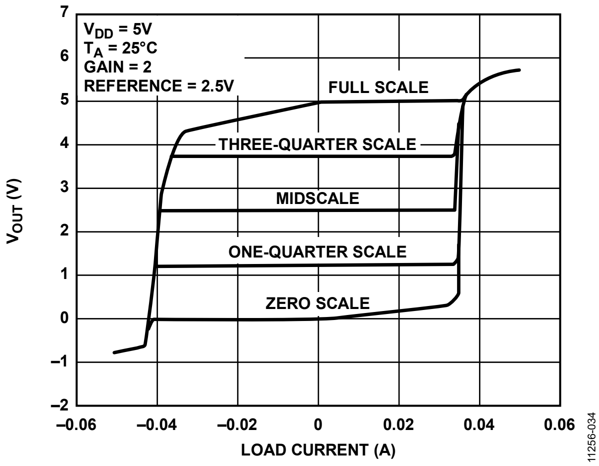


Figure 32. Source and Sink Capability at 5 V, Gain = 2

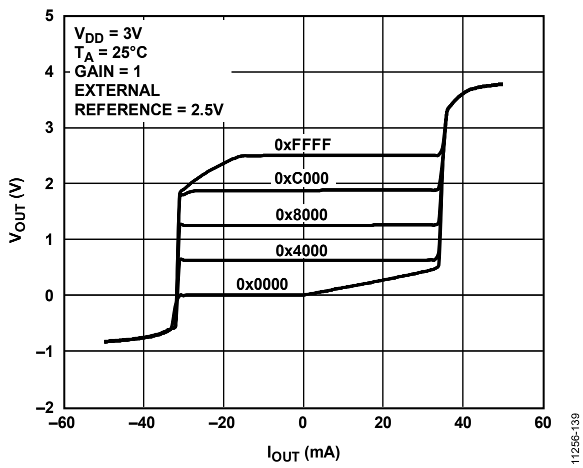


Figure 33. Source and Sink Capability at 3 V, Gain = 1

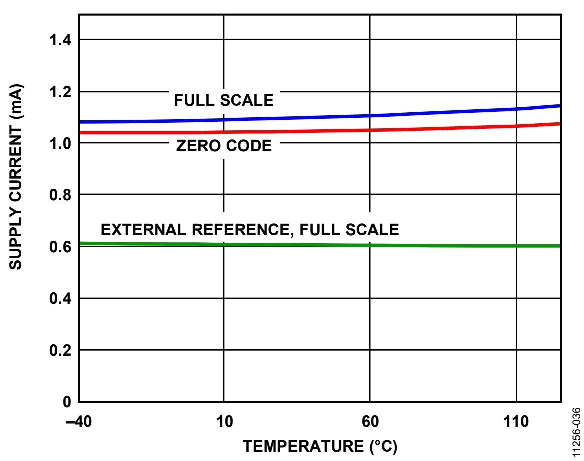


Figure 34. Supply Current vs. Temperature

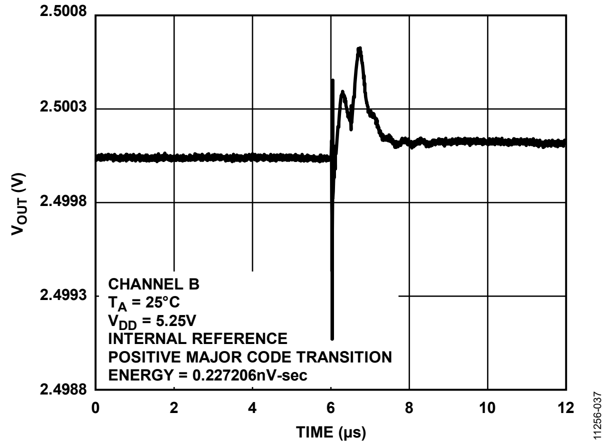


Figure 35. Digital-to-Analog Glitch Impulse

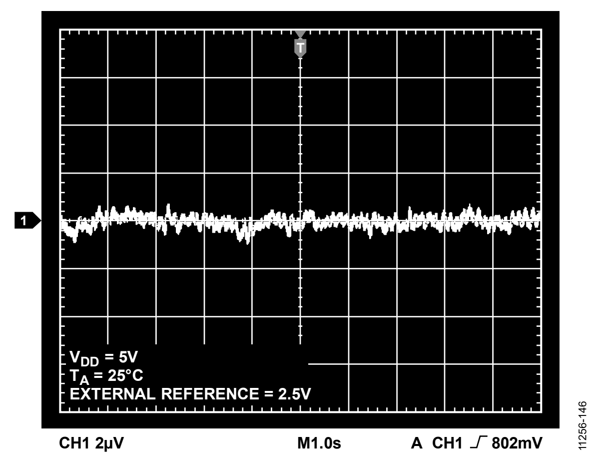


Figure 36. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

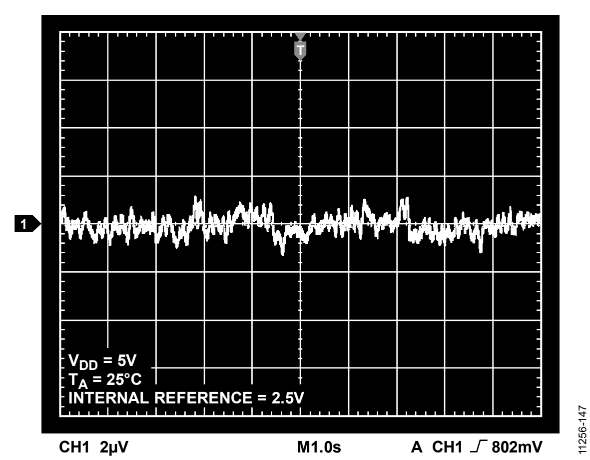


Figure 37. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

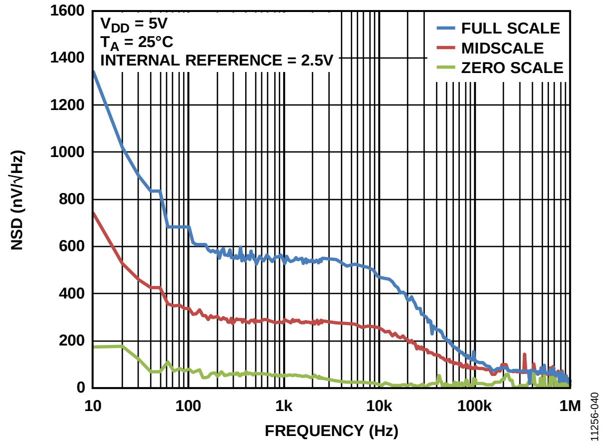


Figure 38. Noise Spectral Density (NSD)

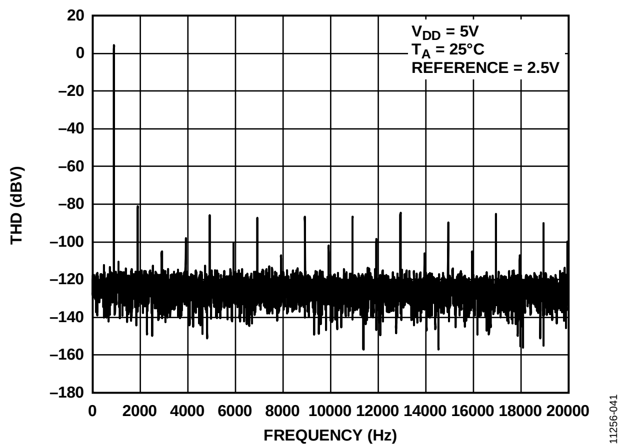


Figure 39. Total Harmonic Distortion at 1 kHz

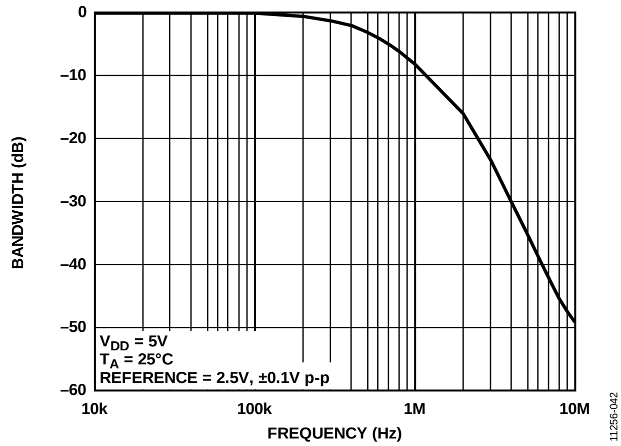


Figure 40. Multiplying Bandwidth, External Reference = 2.5 V, ±0.1 V p-p, 10 kHz to 10 MHz

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Typical INL vs. code plots are shown in Figure 14 and Figure 17.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL vs. code plots are shown in Figure 15 and Figure 18.

Zero-Code Error
Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the device because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature is shown in Figure 23.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range (% of FSR). A plot of full-scale error vs. temperature is shown in Figure 22.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal and is expressed as % of FSR.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Gain Temperature Coefficient
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the device with Code 512 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. It is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of $\overline{SYNC}$.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 35).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Noise Spectral Density (NSD)
NSD is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured, in nV/√Hz, by loading the DAC to midscale and measuring noise at the output. A noise spectral density plot is shown in Figure 38.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and expressed in nV-sec.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then execute a software LDAC and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and the attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows;

$$TC = \left[\frac{V_{REFmax} - V_{REFmin}}{V_{REFnom} \times TempRange} \right] \times 10^6$$

where:

V_{REFmax} is the maximum reference output measured over the total temperature range.

V_{REFmin} is the minimum reference output measured over the total temperature range.

V_{REFnom} is the nominal reference output voltage, 2.5 V.

TempRange is the specified temperature range of −40°C to +105°C.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTERS

The AD5689R/AD5687R are dual 16-/12-bit, serial input, voltage output DACs with an internal reference. The parts operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5689R/AD5687R in a 24-bit word format via a 3-wire serial interface. The devices incorporate a power-on reset circuit to ensure that the DAC output powers up to a known output state. The AD5689R/AD5687R also have a software power-down mode that reduces the typical current consumption to 4 µA.

TRANSFER FUNCTION

The internal reference is on by default. To use an external reference, only a nonreference option is available. Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by the following equation:

$$V_{OUT} = V_{REF} \times Gain\left[\frac{D}{2^N}\right]$$

where:
Gain is the output amplifier gain and is set to 1 by default. It can be set to ×1 or ×2 using the gain select pin. When the GAIN pin is tied to GND, both DACs output a span from 0 V to V_{REF}. If the GAIN pin is tied to V_{LOGIC}, both DACs output a span of 0 V to 2 × V_{REF}.
D is the decimal equivalent of the binary code that is loaded to the DAC register as follows: 0 to 4,095 for the 12-bit device and 0 to 65,535 for the 16-bit device.
N is the DAC resolution.

DAC ARCHITECTURE

The DAC architecture consists of a string DAC followed by an output amplifier. Figure 41 shows a block diagram of the DAC architecture.

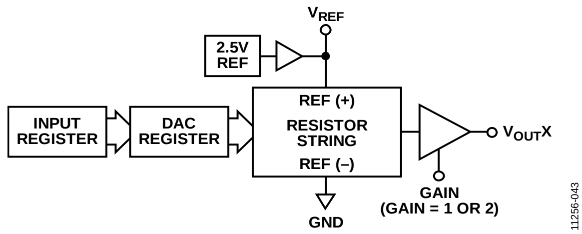


Figure 41. Single DAC Channel Architecture Block Diagram

The resistor string structure is shown in Figure 42. It is a string of resistors, each of Value R. The code loaded to the DAC register determines the node on the string where the voltage is to be tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

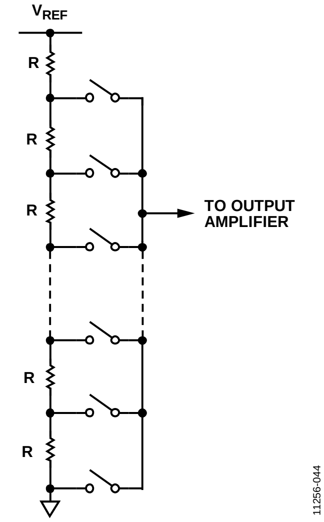


Figure 42. Resistor String Structure

Internal Reference

The AD5689R/AD5687R on-chip reference is on at power-up but can be disabled via a write to a control register. See the Internal Reference Setup section for details.

The AD5689R/AD5687R have a 2.5 V, 2 ppm/°C reference, giving a full-scale output of 2.5 V or 5 V, depending on the state of the GAIN pin. The internal reference associated with the device is available at the V_{REF} pin. This buffered reference is capable of driving external loads of up to 10 mA.

Output Amplifiers

The output buffer amplifier can generate rail-to-rail voltages on the output, which gives an output range of 0 V to V_{DD}. The actual range depends on the value of V_{REF}, the GAIN pin, the offset error, and the gain error. The GAIN pin selects the gain of the output, as follows:

- If the GAIN pin is tied to GND, both DAC outputs have a gain of 1, and the output range is 0 V to V_{REF}.
- If the GAIN pin is tied to V_{LOGIC}, both DAC outputs have a gain of 2, and the output range is 0 V to 2 × V_{REF}.

These amplifiers are capable of driving a load of 1 kΩ in parallel with 2 nF to GND. The slew rate is 0.8 V/µs with a ¼ to ¾ scale settling time of 5 µs.

SERIAL INTERFACE

The AD5689R/AD5687R have a 3-wire serial interface (SYNC, SCLK, and SDIN) that is compatible with SPI, QSPI™, and MICROWIRE® interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence. The AD5689R/AD5687R contain an SDO pin that allows the user to daisy-chain multiple devices together (see the Daisy-Chain Operation section) or read back data.

Input Shift Register

The input shift register of the AD5689R/AD5687R is 24 bits wide, and data is loaded MSB first (DB23). The first four bits are the command bits, C3 to C0 (see Table 9), followed by the 4-bit DAC address bits, composed of DAC B, DAC A, and two don't care bits that must be set to 0 (see Table 8). Finally, the data-word completes the input shift register.

The data-word comprises 16-bit or 12-bit input code, followed by zero don't care bits (for the AD5689R) or four don't care bits (for the AD5687R), as shown in Figure 43 and Figure 44, respectively). These data bits are transferred to the input shift register on the 24 falling edges of SCLK and updated on the rising edge of SYNC.

Commands can be executed on individual DAC channels or on both DAC channels, depending on the address bits selected.

Table 8. Address Commands

Address (n)				
DAC B	**0**	**0**	**DAC A**	**Selected DAC Channel**
0	0	0	1	DAC A
1	0	0	0	DAC B
1	0	0	1	DAC A and DAC B

Table 9. Command Definitions

Command				
C3	**C2**	**C1**	**C0**	**Description**
0	0	0	0	No operation
0	0	0	1	Write to Input Register n (dependent on LDAC)
0	0	1	0	Update DAC Register n with contents of Input Register n
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Hardware LDAC mask register
0	1	1	0	Software reset (power-on reset)
0	1	1	1	Internal reference setup register
1	0	0	0	Set up DCEN register (daisy-chain enable)
1	0	0	1	Set up readback register (readback enable)
1	0	1	0	Reserved
…	…	…	…	Reserved
1	1	1	1	No operation in daisy-chain mode

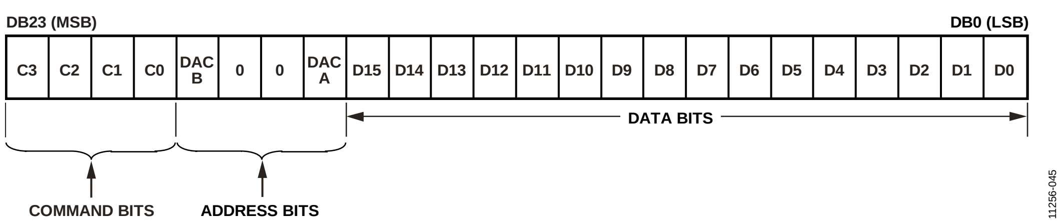


Figure 43. AD5689R Input Shift Register Content

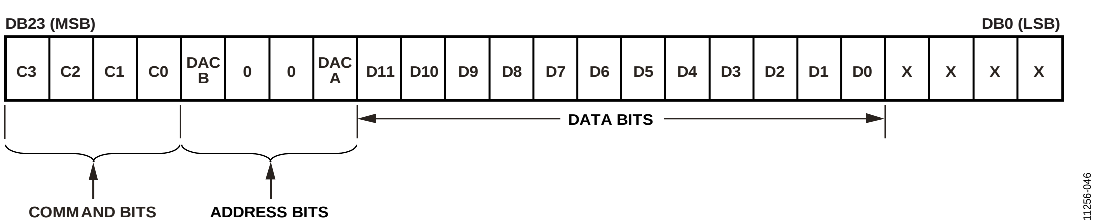


Figure 44. AD5687R Input Shift Register Content

STANDALONE OPERATION

The write sequence begins by bringing the SYNC line low. Data from the SDIN line is clocked into the 24-bit input shift register on the falling edge of SCLK. After the last of 24 data bits is clocked in, SYNC is brought high. The programmed function is then executed; that is, an LDAC-dependent change in DAC register contents and/or a change in the mode of operation occurs. If SYNC is taken high at a clock before the 24th clock, it is considered a valid frame and invalid data may be loaded to the DAC. SYNC must be brought high for a minimum of 20 ns (single channel, see t_8 in Figure 2) before the next write sequence so that a falling edge of SYNC can initiate the next write sequence. Idle SYNC at the rails between write sequences for an even lower power operation of the part. The SYNC line is kept low for 24 falling edges of SCLK, and the DAC is updated on the rising edge of SYNC.

When the data has been transferred into the input register of the addressed DAC, both DAC registers and outputs can be updated by taking LDAC low while the SYNC line is high.

WRITE AND UPDATE COMMANDS

Write to Input Register n (Dependent on LDAC)

Command 0001 allows the user to write to the dedicated input register of each DAC individually. When LDAC is low, the input register is transparent (if not controlled by the LDAC mask register).

Update DAC Register n with Contents of Input Register n

Command 0010 loads the DAC registers/outputs with the contents of the input registers selected and updates the DAC outputs directly.

Write to and Update DAC Channel n (Independent of LDAC)

Command 0011 allows the user to write to the DAC registers and update the DAC outputs directly.

DAISY-CHAIN OPERATION

For systems that contain several DACs, the SDO pin can be used to daisy-chain several devices together. SDO is enabled through a software executable daisy-chain enable (DCEN) command. Command 1000 is reserved for this DCEN function (see Table 9). Daisy-chain mode is enabled by setting Bit DB0 in the DCEN register. The default setting is standalone mode, where DB0 (LSB) = 0. Table 10 shows how the state of the bit corresponds to the mode of operation of the device.

Table 10. Daisy-Chain Enable (DCEN) Register

DB0 (LSB)	Description
0	Standalone mode (default)
1	DCEN mode

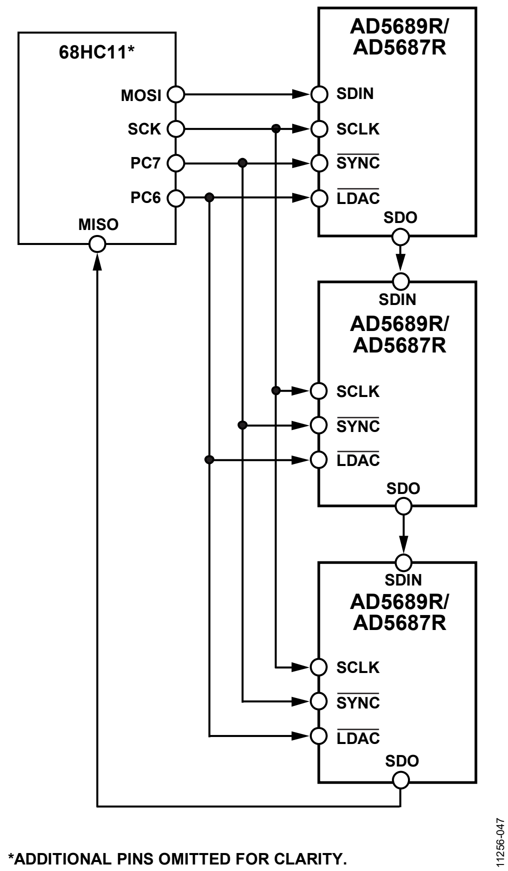


Figure 45. Daisy-Chaining Multiple AD5689R/AD5687R Devices

The SCLK pin is continuously applied to the input shift register when SYNC is low. If more than 24 clock pulses are applied, the data ripples out of the input shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the SDIN input on the next DAC in the chain, a daisy-chain interface is constructed. Each DAC in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where N is the total number of devices that are updated. If SYNC is taken high at a clock that is not a multiple of 24, it is considered a valid frame, and invalid data may be loaded to the DAC. When the serial transfer to all devices is complete, SYNC is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be continuous or a gated clock. A continuous SCLK source can be used only if SYNC can be held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and SYNC must be taken high after the final clock to latch the data.

READBACK OPERATION

Readback mode is invoked through a software executable readback command. If the SDO output is disabled via the daisy-chain mode disable bit in the control register, it is automatically enabled for the duration of the read operation, after which it is disabled again. Command 1001 is reserved for the readback function in when DCEN is enable. This command, in association with selecting one of the address bits, DAC B or DAC A, selects the register to be read. Note that only one DAC register can be selected during readback. The remaining three address bits (which include the two don't care bits) must be set to Logic 0. The remaining data bits in the write sequence are ignored. If more than one address bit is selected or no address bit is selected, DAC Channel A is read back by default. During the next SPI write, the data that appears on the SDO output contains the data from the previously addressed register.

For example, to read back the DAC register for Channel A, implement the following sequence:

1. Write 0x900000 to the AD5689R/AD5687R input register. This setting configures the part for read mode with the Channel A DAC register selected. Note that all data bits, DB15 to DB0, are don't care bits.
2. Follow this write operation with a second write, a nop operation, 0x000000 (0xF00000 in daisy-chain mode). During this write, the data from the register is clocked out on the SDO line. DB23 to DB20 contain undefined data, and the last 16 bits contain the DB19 to DB4 DAC register contents.

POWER-DOWN OPERATION

The AD5689R/AD5687R contain three separate power-down modes. Command 0100 controls the power-down function (see Table 9). These power-down modes are software-programmable by setting eight bits, Bit DB7 to Bit DB0, in the input shift register. There are two bits associated with each DAC channel. Table 11 explains how the state of the two bits corresponds to the mode of operation of the device.

Either or both DACs (DAC B, DAC A) can be powered down to the selected mode by setting the corresponding bits. See Table 12 for the contents of the input shift register during the power-down/power-up operation.

Table 11. Modes of Operation

Operating Mode	PDx1	PDx0
Normal Operation Mode	0	0
Power-Down Modes		
1 kΩ to GND	0	1
100 kΩ to GND	1	0
Three-State	1	1

When both Bit PDx1 and Bit PDx0 (where x is the channel that is selected) in the input shift register are set to 0, the parts work normally, with a normal power consumption of 4 mA at 5 V. However, for the three power-down modes of the AD5689R/AD5687R, the supply current falls to 4 µA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This switchover has the advantage that the output impedance of the part is known while the part is in power-down mode. The three power-down options are as follows:

- The output is connected internally to GND through a 1 kΩ resistor.
- The output is connected internally to GND through a 100 kΩ resistor.
- The output is left open-circuited (three-state).

The output stage is illustrated in Figure 46.

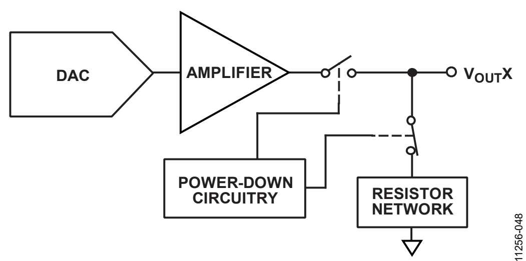


Figure 46. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down, and the DAC register can be updated while the device is in power-down mode. The time that is required to exit power-down is typically 4.5 µs for V_{DD} = 5 V.

To further reduce the current consumption, the on-chip reference can be powered off (see the Internal Reference Setup section).

Table 12. 24-Bit Input Shift Register Contents of Power-Down/Power-Up Operation[1]

DB23 (MSB)	DB22	DB21	DB20	DB19 to DB16	DB15 to DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)
0	1	0	0	X	X	PDB1	PDB0	1	1	1	1	PDA1	PDA0
Command bits (C3 to C0)				Address bits; don't care		Power-down, select DAC B		Set to 1		Set to 1		Power-down, select DAC A	

[1] X = don't care.

LOAD DAC (HARDWARE LDAC PIN)

The AD5689R/AD5687R DACs have double buffered interfaces consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers. Updates to the DAC register are controlled by the LDAC pin.

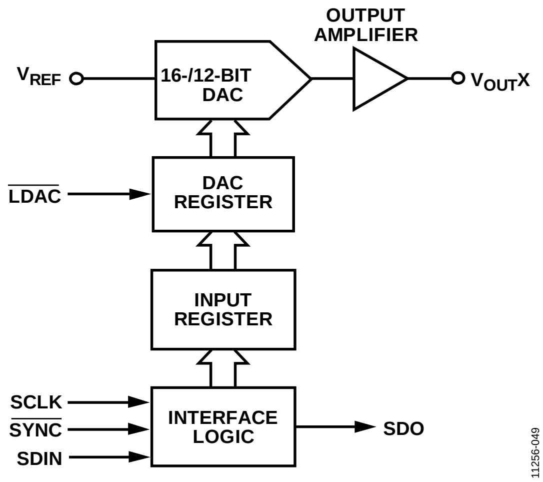


Figure 47. Simplified Diagram of Input Loading Circuitry for a Single DAC

Instantaneous DAC Updating (LDAC Held Low)

LDAC is held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the rising edge of SYNC, and then the output begins to change (see Table 14 and Table 15).

Deferred DAC Updating (LDAC Pulsed Low)

LDAC is held high while data is clocked into the input register using Command 0001. Both DAC outputs are asynchronously updated by taking LDAC low after SYNC is taken high. The update then occurs on the falling edge of LDAC.

LDAC MASK REGISTER

Command 0101 is reserved for a software LDAC mask function, which allows the address bits to be ignored. A write to the DAC, using Command 0101, loads the 4-bit LDAC mask register (DB3 to DB0). The default setting for each channel is 0; that is, the LDAC pin works normally. Setting the selected bit to 1 forces the DAC channel to ignore transitions on the LDAC pin, regardless of the state of the hardware LDAC pin. This flexibility is useful in applications where the user wishes to select which channels respond to the LDAC pin.

The LDAC mask register gives the user extra flexibility and control over the hardware LDAC pin (see Table 13). Setting an LDAC bit (DB3, DB0) to 0 for a DAC channel means that the update of this channel is controlled by the hardware LDAC pin.

Table 13. LDACOverwrite Definition

Load LDAC Register		
LDAC Bits (DB3, DB0)	LDAC Pin	LDAC Operation
0	1 or 0	Determined by the LDAC pin.
1	X[1]	DAC channels update and override the LDAC pin. DAC channels see the LDAC pin as set to 1.

[1] X = don't care.

Table 14. 24-Bit Input Shift Register Contents for LDAC Operation[1]

DB23 (MSB)	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB4	DB3	DB2	DB1	DB0 (LSB)
0	1	0	1	X	X	X	X	X	DAC B	0	0	DAC A
Command bits (C3 to C0)				Address bits, don't care				Don't care	Setting the LDAC bit to 1 overrides the LDAC pin			

[1] X = don't care.

Table 15. Write Commands and LDAC Pin Truth Table[1]

Command	Description	Hardware LDAC Pin State	Input Register Contents	DAC Register Contents
0001	Write to Input Register n (dependent on LDAC)	V_{LOGIC}	Data update	No change (no update)
		GND[2]	Data update	Data update
0010	Update DAC Register n with contents of Input Register n	V_{LOGIC}	No change	Updated with input register contents
		GND	No change	Updated with input register contents
0011	Write to and update DAC Channel n	V_{LOGIC}	Data update	Data update
		GND	Data update	Data update

[1] A high-to-low hardware LDAC pin transition always updates the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the LDAC mask register.
[2] When the LDAC pin is permanently tied low, the LDAC mask bits are ignored.

HARDWARE RESET ($\overline{RESET}$)

$\overline{RESET}$ is an active low reset that allows the outputs to be cleared to either zero scale or midscale. The clear code value is user selectable via the power-on reset select pin (RSTSEL). $\overline{RESET}$ must be kept low for a minimum amount of time to complete the operation (see Figure 2). When the $\overline{RESET}$ signal is returned high, the output remains at the cleared value until a new value is programmed. The outputs cannot be updated with a new value while the $\overline{RESET}$ pin is low. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function (see Table 9). Any events on $\overline{LDAC}$ during a power-on reset are ignored. If the $\overline{RESET}$ pin is pulled low at power-up, the device does not initialize correctly until the pin is released.

RESET SELECT PIN (RSTSEL)

The AD5689R/AD5687R contain a power-on reset circuit that controls the output voltage during power-up. When the RSTSEL pin is connected low (to GND), the output powers up to zero scale. Note that this is outside the linear region of the DAC. When the RSTSEL pin is connected high (to V_{LOGIC}), $V_{OUT}X$ powers up to midscale. The output remains powered up at this level until a valid write sequence is sent to the DAC.

To ensure that the RSTSEL pin functions correctly, a power sequence must be followed. Power up V_{LOGIC} first, before V_{DD}; otherwise, V_{OUT} remains at zero scale.

INTERNAL REFERENCE SETUP

Command 0111 is reserved for setting up the internal reference (see Table 9). By default, the on-chip reference is on at power-up. To reduce the supply current, this reference can be turned off by setting the software-programmable bit, DB0, as shown in Table 17. Table 16 shows how the state of the bit corresponds to the mode of operation.

Table 16. Reference Setup Register

Internal Reference Setup Register (DB0)	Action
0	Reference on (default)
1	Reference off

SOLDER HEAT REFLOW

As with all IC reference voltage circuits, the reference value experiences a shift induced by the soldering process. Analog Devices, Inc., performs a reliability test, called precondition, that mimics the effect of soldering a device to a board. The output voltage specification that is listed in Table 2 includes the effect of this reliability test.

Figure 48 shows the effect of solder heat reflow (SHR) as measured through the reliability test (precondition).

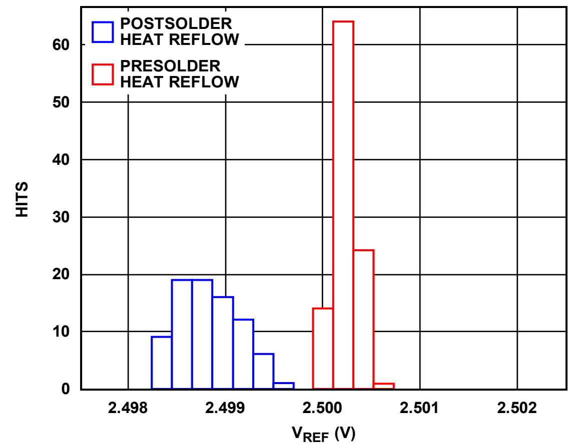


Figure 48. SHR Reference Voltage Shift

LONG-TERM TEMPERATURE DRIFT

Figure 49 shows the change in the V_{REF} (ppm) value after 1000 hours at 25°C ambient temperature.

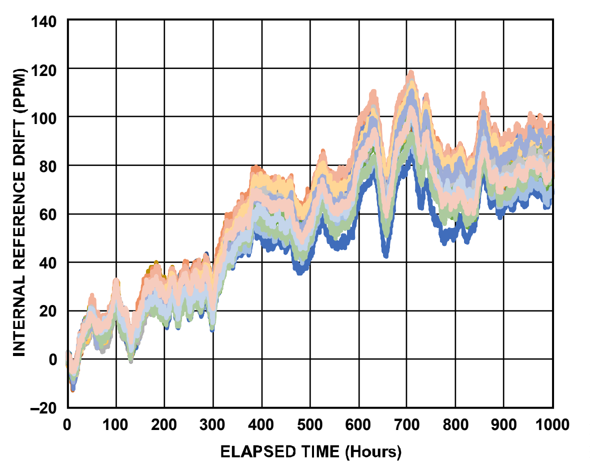


Figure 49. Reference Drift Through to 1000 Hours

Table 17. 24-Bit Input Shift Register Contents for Internal Reference Setup Command[1]

DB23 (MSB)	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB1	DB0 (LSB)
0	1	1	1	X	X	X	X	X	1 or 0
Command bits (C3 to C0)				Address bits (A3 to A0)				Don't care	Reference setup register

[1] X = don't care.

THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, to hot, and then back to ambient.

Thermal hysteresis data is shown in Figure 50. It is measured by sweeping the temperature from ambient to −40°C, next to +105°C, and then returning to ambient. The V_{REF} delta is then measured between the two ambient measurements and shown in blue in Figure 50. The same temperature sweep and measurements are immediately repeated and the results are shown in red in Figure 50.

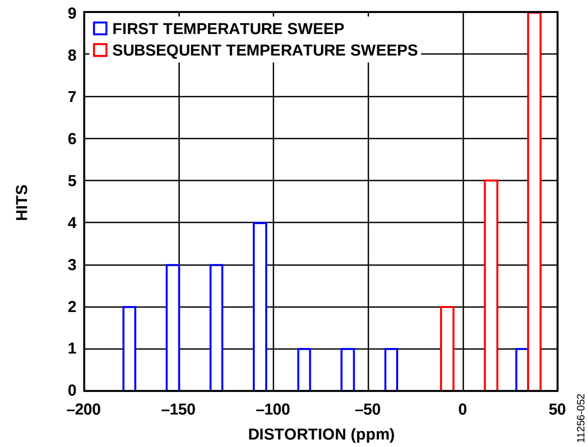


Figure 50. Thermal Hysteresis

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5689R/AD5687R is achieved via a serial bus using a standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 3-wire or 4-wire interface consisting of a clock signal, a data signal, and a synchronization signal. Each device requires a 24-bit data-word with data valid on the rising edge of $\overline{\text{SYNC}}$.

AD5689R/AD5687R TO ADSP-BF531 INTERFACE

The SPI interface of the AD5689R/AD5687R is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 51 shows the AD5689R/AD5687R connected to an Analog Devices Blackfin® DSP. The Blackfin has an integrated SPI port that connects directly to the SPI pins of the AD5689R/AD5687R.

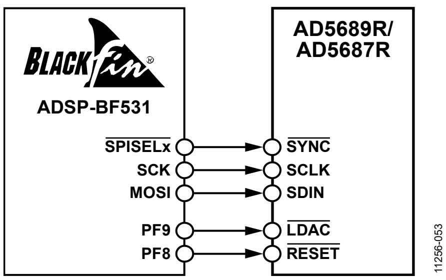


Figure 51. ADSP-BF531 Interface to the AD5689R/AD5687R

AD5689R/AD5687R TO SPORT INTERFACE

The Analog Devices ADSP-BF527 has one SPORT serial port. Figure 52 shows how one SPORT interface can be used to control the AD5689R/AD5687R.

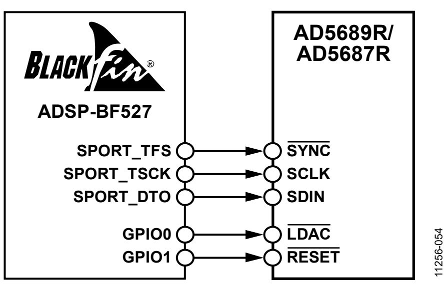


Figure 52. SPORT Interface to the AD5689R/AD5687R

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the PCB on which the AD5689R/AD5687R are mounted so that the AD5689R/AD5687R lie on the analog plane.

Provide the AD5689R/AD5687R with ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply, located as close to the package as possible, ideally right up against the device. The 10 μF capacitor is of the tantalum bead type. Use a 0.1 μF capacitor with low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where there are many devices on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

Each AD5689R or AD5687R has an exposed paddle beneath the device. Connect this paddle to the GND supply for the part. For optimum performance, use special considerations to design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, solder the exposed paddle on the bottom of the package to the corresponding thermal land paddle on the PCB. Design thermal vias into the PCB land paddle area to further improve heat dissipation.

The GND plane on the device can be increased (as shown in Figure 53) to provide a natural heat sinking effect.

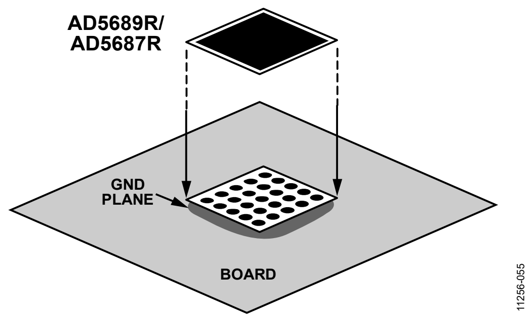


Figure 53. Paddle Connection to Board

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The *i*Coupler® products from Analog Devices provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5689R/AD5687R makes these parts ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 54 shows a 4-channel isolated interface to the AD5689R/AD5687R using an ADuM1400. For additional information, visit www.analog.com/icouplers.

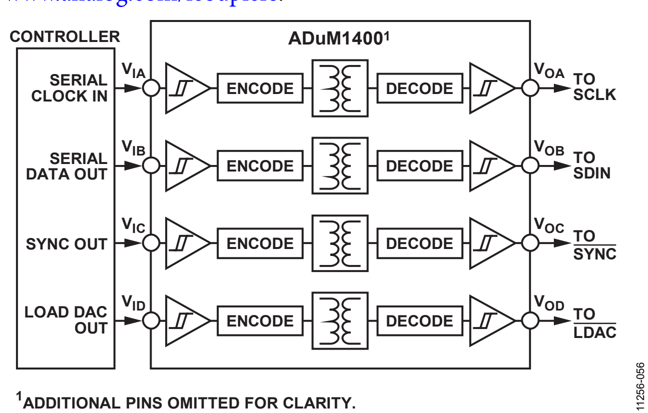
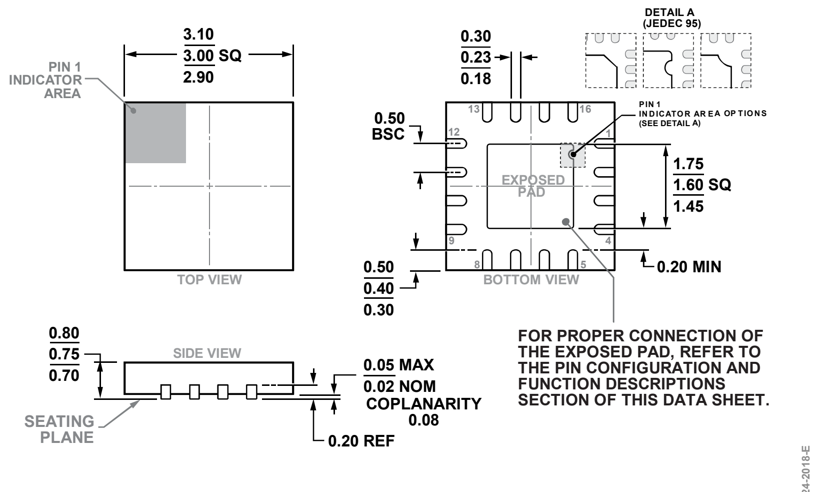


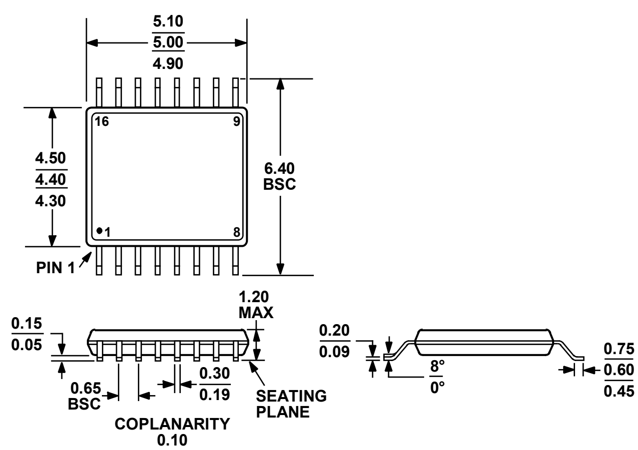
Figure 54. Isolated Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6

Figure 55. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 56. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Resolution	Temperature Range	Accuracy	Reference Tempco (ppm/°C)	Package Description	Package Option	Marking Code
AD5689RACPZ-RL7	16 Bits	−40°C to +105°C	±8 LSB INL	±5 (typ)	16-Lead LFCSP_WQ	CP-16-22	DLU
AD5689RBCPZ-RL7	16 Bits	−40°C to +105°C	±2 LSB INL	±5 (max)	16-Lead LFCSP_WQ	CP-16-22	DL2
AD5689RWBCPZ-RL7	16 Bits	−40°C to +105°C	±3 LSB INL	±5 (max)	16-Lead LFCSP_WQ	CP-16-22	DNN
AD5689RARUZ	16 Bits	−40°C to +105°C	±8 LSB INL	±5 (typ)	16-Lead TSSOP	RU-16	
AD5689RARUZ-RL7	16 Bits	−40°C to +105°C	±8 LSB INL	±5 (typ)	16-Lead TSSOP	RU-16	
AD5689RBRUZ	16 Bits	−40°C to +105°C	±2 LSB INL	±5 (max)	16-Lead TSSOP	RU-16	
AD5689RBRUZ-RL7	16 Bits	−40°C to +105°C	±2 LSB INL	±5 (max)	16-Lead TSSOP	RU-16	
AD5687RBCPZ-RL7	12 Bits	−40°C to +105°C	±1 LSB INL	±5 (max)	16-Lead LFCSP_WQ	CP-16-22	DL1
AD5687RBRUZ	12 Bits	−40°C to +105°C	±1 LSB INL	±5 (max)	16-Lead TSSOP	RU-16	
AD5687RBRUZ-RL7	12 Bits	−40°C to +105°C	±1 LSB INL	±5 (max)	16-Lead TSSOP	RU-16	
EVAL-AD5687RSDZ					Evaluation Board		
EVAL-AD5689RSDZ					Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] W = Qualified for automotive applications.

AUTOMOTIVE PRODUCTS

The AD5689RWBCPZ-RL7 model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

D11256-0-10/19(C)