Internally Trimmed Precision IC Multiplier

Data Sheet

AD632

FEATURES

Pretrimmed to ±0.5% maximum 4-quadrant error
All inputs (X, Y, and Z) differential, high impedance for $[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$ transfer function
Scale-factor adjustable to provide up to ×10 gain
Low noise design: 90 mV rms, 10 Hz to 10 kHz
Low cost, monolithic construction
Excellent long-term stability

APPLICATIONS

High quality analog signal processing
Differential ratio and percentage computations
Algebraic and trigonometric function synthesis
Accurate voltage controlled oscillators and filters

FUNCTIONAL BLOCK DIAGRAM

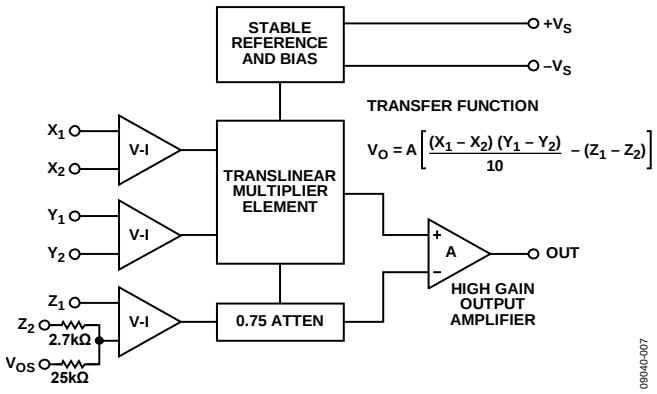


Figure 1.

GENERAL DESCRIPTION

The AD632 is an internally trimmed monolithic four-quadrant multiplier/divider. The AD632B has a maximum multiplying error of ±0.5% without external trims.

Excellent supply rejection, low temperature coefficients, and long-term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions. The simplicity and flexibility of use provide an attractive alternative approach to the solution of complex control functions.

The AD632 is pin-for-pin compatible with the industry standard AD532 but with improved specifications and a fully differential high impedance Z input. The AD632 is capable of providing gains of up to ×10, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD632 can be effectively employed as a variable gain differential input amplifier with high common-mode rejection. The effectiveness of the variable gain capability is enhanced by the inherent low noise of the AD632 at 90 μV rms.

PRODUCT HIGHLIGHTS

1. Guaranteed performance over temperature.
2. The AD632A and AD632B are specified for maximum multiplying errors of ±1.0% and ±0.5% of full scale, respectively, at +25°C and are rated for operation from −25°C to +85°C.
3. Maximum multiplying errors of ±2.0% (AD632S) and ±1.0% (AD632T) are guaranteed over the extended temperature range of −55°C to +125°C.
4. High reliability.
5. The AD632S and AD632T series are available with MIL-STD-883 Level B screening.
6. All devices are available in either the hermetically sealed TO-100 metal can or ceramic DIP package.

Rev. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

5/13—Rev. C to Rev. D

Changes to Table 1 3
Changes to Ordering Guide 11

12/11—Rev. B to Rev. C

Updated Format ..... Universal
Added Figure 1, Renumbered Sequentially 1
Deleted Chip Dimensions and Pad Layout Section 5
Changes to Figure 3 and Figure 4 6
Added Table 3 and Table 4 6
Changes to the Operations as a Divider Section 9
Updated Outline Dimensions 10

4/10—Rev. A to Rev. B

Changes to Pin Configurations and Product Highlights Sections 1
Changes to Thermal Characteristics Section 3
Updated Outline Dimensions 6
Changes to Ordering Guide 6

SPECIFICATIONS

@ +25°C, V_S = ±15 V, R ≥ 2 kΩ, unless otherwise noted. Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Table 1.

Parameter	AD632A Min	AD632A Typ	AD632A Max	AD632B Min	AD632B Typ	AD632B Max	AD632S Min	AD632S Typ	AD632S Max	AD632T Min	AD632T Typ	AD632T Max	Units
MULTIPLIER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$		
Total Error[1] (−10 V ≤ X, Y ≤ +10 V)			**±1.0**			**±0.5**			**±1.0**			**±0.5**	%
T_A = Min to Max		**±1.5**			**±1.0**				**±2.0**			**±1.0**	%
Total Error vs. Temperature		±0.022			±0.015				**±0.02**			**±0.01**	%/°C
Scale Factor Error (SF = 10,000 V Nominal)[2]		±0.25			±0.1			±0.25			±0.1		%
Temperature Coefficient of Scaling Voltage		±0.02			**±0.01**			±0.2				**±0.005**	%/°C
Supply Rejection (±15 V ± 1 V)		±0.01			±0.01			±0.01			±0.01		%
Nonlinearity													
X (X = 20 V p-p, Y = 10 V)		±0.4			±0.2	±0.3		±0.4			±0.2	±0.3	%
Y (Y = 20 V p-p, X = 10 V)		±0.2			±0.1	±0.1		±0.2			±0.1	±0.1	%
Feedthrough[3]													
X (Y Nulled, X = 20 V p-p 50 Hz)		±0.3			±0.15	±0.3		±0.3			±0.15	±0.3	%
Y (X Nulled, Y = 20 V p-p 50 Hz)		±0.01			±0.01	±0.1		±0.01			±0.01	±0.1	%
Output Offset Voltage		±5	**±30**		±2	±15		±5	**±30**		±2	±15	mV
Output Offset Voltage Drift		200			100				**500**			**300**	µV/°C
DYNAMICS													
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000 pF)		50			50			50			50		kHz
Slew Rate (V_{OUT} 20 p-p)		20			20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20 V)		2			2			2			2		µs
NOISE													
Noise Spectral Density													
SF = 10 V		0.8			0.8			0.8			0.8		µV/√Hz
SF = 3 V[4]		0.4			0.4			0.4			0.4		µV/√Hz
Wideband Noise													
A = 10 Hz to 5 MHz		1.0			1.0			1.0			1.0		mV/rms
P = 10 Hz to 10 kHz		90			90			90			90		µV/rms
OUTPUT													
Output Voltage Swing	**±11**			**±11**			**±11**			**±11**			V
Output Impedance (f ≤ 1 kHz)		0.1			0.1			0.1			0.1		Ω
Output Short-Circuit Current (R_L = 0, T_A = Min to Max)		30			30			30			30		mA
Amplifier Open-Loop Gain (f = 50 Hz)		70			70			70			70		dB
INPUT AMPLIFIERS (X, Y, and Z)[5]													
Signal Voltage Range (Differential or Common-Mode Operating Diff.)		±10	±12		±10	±12		±10	±12		±10	±12	V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z		200			100				500			300	µV/°C
CMRR	**60**	80		**70**	90		**60**	80		**70**	90		dM
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1			0.1			0.1		µA
Differential Resistance		10			10			10			10		MΩ

Parameter	AD632A Min	AD632A Typ	AD632A Max	AD632B Min	AD632B Typ	AD632B Max	AD632S Min	AD632S Typ	AD632S Max	AD632T Min	AD632T Typ	AD632T Max	Units
DIVIDER PERFORMANCE													
Transfer Function($X_1 > X_2$)		$10\text{V}\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\text{V}\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\text{V}\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\text{V}\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1]													
(X = 10 V, −10 V ≤ Z ≤ +10 V)		±0.75			±0.35			±0.75			±0.35		%
(X = 1 V, −1 V ≤ Z ≤ +1 V)		±2.0			±1.0			±2.0			±1.0		%
(0.1 V ≤ X ≤ 10 V, −10 V ≤ Z ≤ 10 V)		±2.5			±1.0			±2.5			±1.0		%
SQUARER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)^2}{10\text{V}}+Z_2$			$\frac{(X_1-X_2)^2}{10\text{V}}+Z_2$			$\frac{(X_1-X_2)^2}{10\text{V}}+Z_2$			$\frac{(X_1-X_2)^2}{10\text{V}}+Z_2$		
Total Error (−10 V ≤ X ≤ 10 V)		±0.6			±0.3			±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE													
Transfer Function, ($Z_1 \le Z_2$)		$\sqrt{10\text{V}(Z_2-Z_1)+X_2}$			$\sqrt{10\text{V}(Z_2-Z_1)+X_2}$			$\sqrt{10\text{V}(Z_2-Z_1)+X_2}$			$\sqrt{10\text{V}(Z_2-Z_1)+X_2}$		
Total Error[1] (1 V ≤ Z ≤ 10 V)		±1.0			±0.5			±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS													
Supply Voltage													
Rated Performance		±15			±15			±15			±15		V
Operating	±8		**±18**	±8		**±18**	±8		**±22**	±8		**±22**	V
Supply Current													
Quiescent		4	**6**		4	6		4	**6**		4	6	mA

[1] Figures given are percent of full-scale, ±10 V (that is, 0.01% = 1 mV).
[2] Can be reduced to 3 V using an external resistor between $-V_S$ and SF.
[3] Irreducible component due to nonlinearity: excludes effect of offsets.
[4] Using an external resistor adjusted to give a value of SF = 3 V.
[5] See the functional block diagram (Figure 1) for definition of sections.

ABSOLUTE MAXIMUM RATINGS

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 2. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead TO-100	150	25	°C/W
14-Lead SBDIP	95	25	°C/W

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

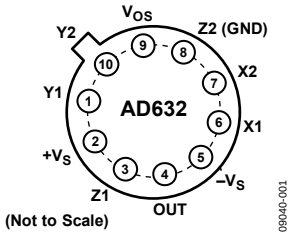


Figure 2. Pin Configuration, H-Package, TO-100

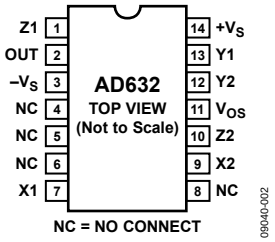


Figure 3. Pin Configuration, D-Package, SBDIP

Table 3. Pin Function Descriptions, 10-Pin TO-100

Pin No.	Mnemonic	Description
1	Y1	Y Multiplicand Noninverting Input.
2	$+V_S$	Positive Supply Voltage.
3	Z1	Summing Node Noninverting Input.
4	OUT	Product.
5	$-V_S$	Negative Supply Voltage.
6	X1	X Multiplicand Noninverting Input.
7	X2	X Multiplicand Inverting Input.
8	Z2	Summing Node Inverting Input.
9	V_{OS}	Offset Voltage Adjustment.
10	Y2	Y Multiplicand Inverting Input.

Table 4. Pin Function Descriptions, 14-Lead SBDIP

Pin No.	Mnemonic	Description
1	Z1	Summing Node Noninverting Input.
2	OUT	Product.
3	$-V_S$	Negative Supply Voltage.
4, 5, 6, 8	NC	No Connection. Do not connect to this pin.
7	X1	X Multiplicand Noninverting Input.
9	X2	X Multiplicand Noninverting Input.
10	Z2	Summing Node Inverting Input.
11	V_{OS}	Offset Voltage Adjustment.
12	Y2	Y Multiplicand Inverting Input.
13	Y1	Y Multiplicand Noninverting Input.
14	$+V_S$	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

Typical @ 25°C with ±V_S = 15 V.

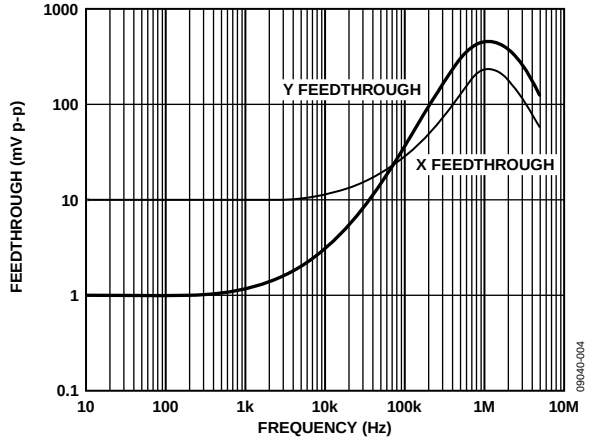


Figure 4. AC Feedthrough vs. Frequency

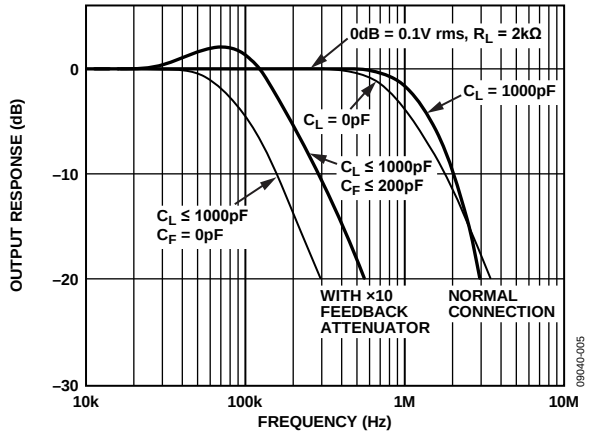


Figure 5. Frequency Response as a Multiplier

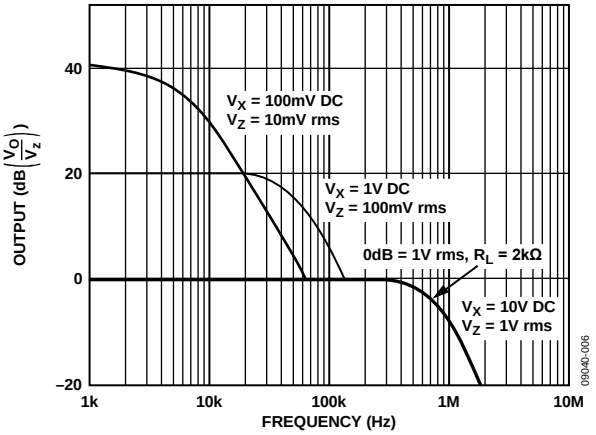


Figure 6. Frequency Response vs. Divider Denominator Input Voltage

OPERATION AS A MULTIPLIER

Figure 7 shows the basic connection for multiplication. Note that the circuit meets all specifications without trimming.

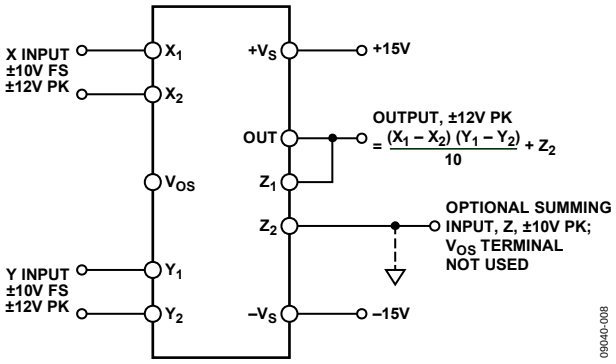


Figure 7. Basic Multiplier Connection

When needed, the user can reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30 mV range required) to the X or Y input. Figure 4 shows the typical ac feedthrough with this adjustment mode. Note that the feedthrough of the Y input is a factor of 10 lower than that of the X input and is to be used for applications where null suppression is critical.

The Z_2 terminal of the AD632 can be used to sum an additional signal into the output. In this mode, the output amplifier behaves as a voltage follower with a 1 MHz small signal bandwidth and a 20 V/µs slew rate. Always reference this terminal to the ground point of the driven system, particularly if this is remote. Likewise, reference the differential inputs to their respective signal common potentials to realize the full accuracy of the AD632.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator, as shown in Figure 8. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80 kHz without the peaking capacitor, C_F. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications.

Feedback attenuation also retains the capability for adding a signal to the output. Signals can be applied to the Z terminal, where they are amplified by −10, or to the common ground connection where they are amplified by −1. Input signals can also be applied to the lower end of the 2.7 kΩ resistor, giving a gain of +9.

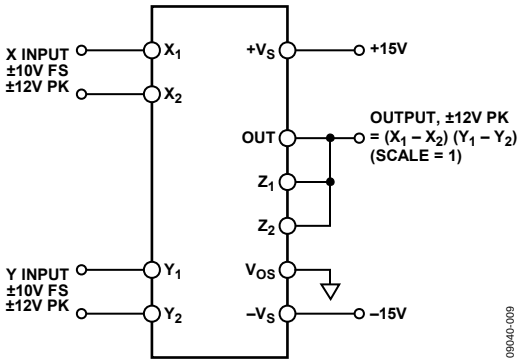


Figure 8. Connections for Scale Factor of Unity

OPERATION AS A DIVIDER

Figure 9 shows the connection required for division. Unlike earlier products, the AD632 provides differential operation on both the numerator and the denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in Figure 6.

The accuracy of the AD632 B-model is sufficient to maintain a 1% error over a 10 V to 1 V denominator range.

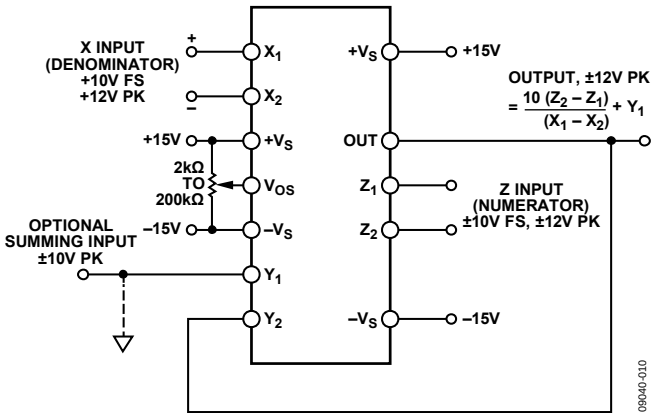
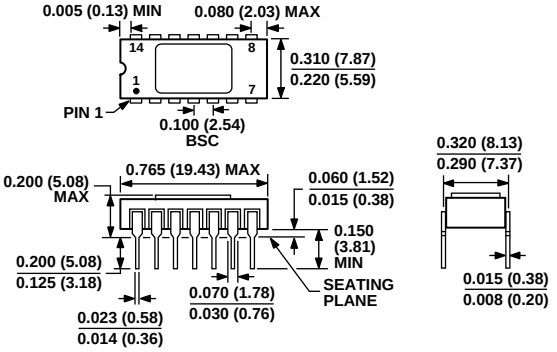


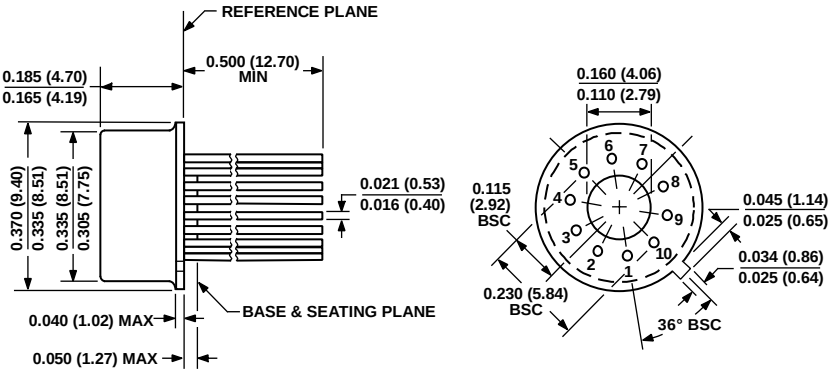
Figure 9. Basic Divider Connection

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 10. 14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP] (D-14)
Dimensions shown in inches and (millimeters)



DIMENSIONS PER JEDEC STANDARDS MO-006-AF
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022306-A

Figure 11. 10-Pin Metal Header Package [TO-100] (H-10)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD632AD	−25°C to +85°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD632ADZ	−25°C to +85°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD632AHZ	−25°C to +85°C	10-Pin Metal Header Package [TO-100]	H-10
AD632BD	−25°C to +85°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD632BDZ	−25°C to +85°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD632BHZ	−25°C to +85°C	10-Pin Metal Header Package [TO-100]	H-10
AD632SD	−55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD632SH	−55°C to +125°C	10-Pin Metal Header Package [TO-100]	H-10
AD632SH/883B	−55°C to +125°C	10-Pin Metal Header Package [TO-100]	H-10
AD632TD	−55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD632TD/883B	−55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD632TH	−55°C to +125°C	10-Pin Metal Header Package [TO-100]	H-10
AD632TH/883B	−55°C to +125°C	10-Pin Metal Header Package [TO-100]	H-10

[1] Z = RoHS Compliant Part.

NOTES

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