135 MHz BW IF Diversity Receiver

Data Sheet

AD6679

FEATURES

- Parallel LVDS (DDR) outputs
- In-band SFDR = 82 dBFS at 340 MHz (500 MSPS)
- In-band SNR = 67.8 dBFS at 340 MHz (500 MSPS)
- 1.1 W total power per channel at 500 MSPS (default settings)
- Noise density = −153 dBFS/Hz at 500 MSPS
- 1.25 V, 2.50 V, and 3.3 V dc supply operation
- Flexible input range
  - 1.46 V p-p to 2.06 V p-p (2.06 V p-p nominal)
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient automatic gain control (AGC) implementation
- Noise shaping requantizer (NSR) option for main receiver function
- Variable dynamic range (VDR) option for digital predistortion (DPD) function
- 2 integrated wideband digital processors per channel
  - 12-bit numerically controlled oscillator (NCO), up to
    - 4 cascaded half-band filters
- Differential clock inputs
- Integer clock divide by 1, 2, 4, or 8
- Energy saving power-down modes
- Small signal dither

APPLICATIONS

- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE, LTE-A
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

GENERAL DESCRIPTION

The AD6679 is a 135 MHz bandwidth mixed-signal intermediate frequency (IF) receiver. It consists of two, 14-bit, 500 MSPS analog-to-digital converters (ADCs) and various digital signal processing blocks consisting of four wideband DDCs, an NSR, and VDR monitoring. It has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of sampling wide bandwidth analog signals of up to 2 GHz. The AD6679 is optimized for wide input bandwidth, high sampling rates, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

FUNCTIONAL BLOCK DIAGRAM

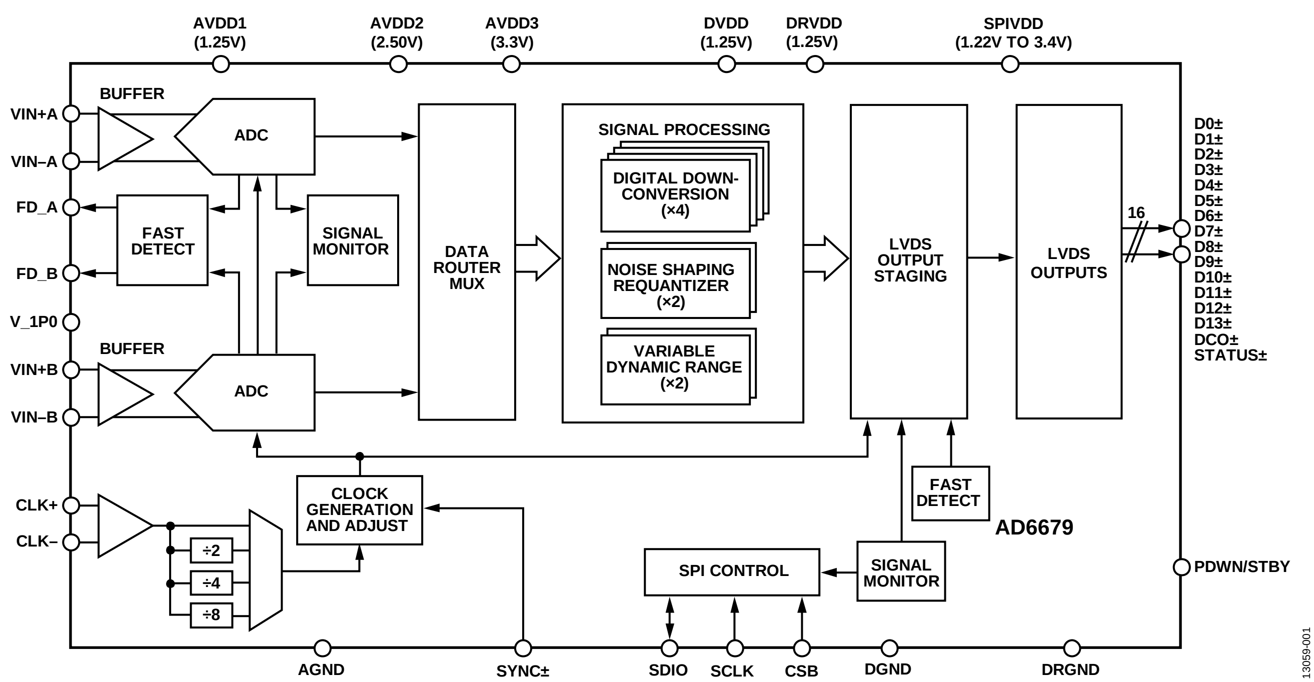


Figure 1.

Rev. B

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support
www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

4/16—Rev. A to Rev. B

Changes to Table 4 ... 8
Changes to Table 5 and Figure 3 ... 9
Changes to Figure 4 Caption ... 10
Changes to Figure 5 Caption ... 11
Changes to Figure 6 Caption ... 12
Changes to Figure 7 Caption ... 13
Changes to Figure 8 Caption ... 14
Changes to Figure 10 ... 16
Changes to Table 6 ... 18
Changes to Input Clock Divider Section ... 34
Added Virtual Converter Mapping Section and Table 12; Renumbered Sequentially ... 36
Added Figure 60; Renumbered Sequentially ... 37
Changes to Table 35 ... 62
Changes to Datapath Soft Reset Section ... 69
Changes to Table 41 ... 70

9/15—Rev. 0 to Rev. A

Changes to General Description Section ... 3
Changes to Figure 12 ... 18
Changes to Figure 13 ... 20
Changes to Figure 14 ... 22
Changes to ADC Test Modes ... 63

5/15—Revision 0: Initial Version

The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four DDCs through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 12-bit frequency translator (NCO) and up to four half-band decimation filters.

Each ADC output is connected internally to an NSR block. The integrated NSR circuitry allows improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes, selectable via the serial port interface (SPI). With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6679 supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining a 9-bit output resolution.

Each ADC output is also connected internally to a VDR block. This optional mode allows full dynamic range for defined input signals. Inputs that are within a defined mask (based on DPD applications) pass unaltered. Inputs that violate this defined mask result in the reduction of the output resolution.

With VDR, the dynamic range of the observation receiver is determined by a defined input frequency mask. For signals falling within the mask, the outputs are presented at the maximum resolution allowed. For signals exceeding defined power levels within this frequency mask, the output resolution is truncated. This mask is based on DPD applications and supports tunable real IF sampling, and zero IF or complex IF receive architectures.

Operation of the AD6679 between the DDC, NSR, and VDR modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD6679 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly reduce the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD6679 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal that the ADC digitized.

The output data is routed directly to the one external 14-bit LVDS output port, supporting double data rate (DDR) formatting. An external data clock and a clock status bit are offered for data capture flexibility.

The AD6679 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V capable 3-wire SPI.

The AD6679 is available in a Pb-free, 196-ball BGA_ED, and is specified over the −40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth IF sampling of signals up to 2 GHz.
2. Buffered inputs with programmable input termination eases filter design and implementation.
3. Four integrated wideband decimation filters and NCO blocks support multiband receivers.
4. Flexible SPI controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection and signal monitoring.
6. Programmable fast overrange detection.
7. 12 mm × 12 mm, 196-ball BGA_ED.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference (V_{REF}), A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.3	0	+0.3	% FSR
Offset Matching	Full		0	0.3	% FSR
Gain Error	Full	−6.5	0	+6.5	% FSR
Gain Matching	Full		0	5.0	% FSR
Differential Nonlinearity (DNL)	Full	−0.6	±0.5	+0.7	LSB
Integral Nonlinearity (INL)	Full	−4.5	±2.5	+5.0	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±3		ppm/°C
Gain Error	Full		−39		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Voltage	Full		1.0		V
INPUT REFERRED NOISE					
V_{REF} = 1.0 V	25°C		2.04		LSB rms
ANALOG INPUTS					
Differential Input Voltage Range (Internal V_{REF} = 1.0 V)	Full	1.46	2.06	2.06	V p-p
Common-Mode Voltage (V_{CM})	Full		2.05		V
Differential Input Capacitance[1]	Full		1.5		pF
Analog Full Power Bandwidth	Full		2		GHz
POWER SUPPLY					
AVDD1	Full	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	V
DVDD	Full	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	V
SPIVDD	Full	1.22	1.8	3.4	V
I_{AVDD1}	Full		464	503	mA
I_{AVDD2}	Full		396	455	mA
I_{AVDD3}[2]	Full		89	100	mA
I_{DVDD} (Default SPI—NSR Mode)	Full		141	164	mA
I_{DVDD} (VDR Mode)	Full		117	138	mA
I_{DRVDD}[3]	Full		110	123	mA
I_{SPIVDD}	Full		5	6	mA
POWER CONSUMPTION					
Total Power Dissipation					
Default SPI—NSR Mode[3]	Full		2.2	2.37	W
VDR Mode[3]	Full		2.16	2.34	W
Power-Down Dissipation	Full		0.71		W
Standby[4]	Full		1.4		W

[1] Differential capacitance is measured between the VIN+x and VIN−x pins (x = A, B).
[2] AVDD3 current changes based on the Buffer Control 1 setting (see Figure 46).
[3] Parallel interleaved LVDS mode. The power dissipation on DRVDD changes with the output data mode used.
[4] Standby can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE	Full		2.06		V p-p
NOISE DENSITY[2]	Full		−153		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		68.9		dBFS
f_{IN} = 170 MHz	Full	67.5	68.6		dBFS
f_{IN} = 340 MHz	25°C		67.8		dBFS
f_{IN} = 450 MHz	25°C		67.3		dBFS
f_{IN} = 765 MHz	25°C		63.9		dBFS
f_{IN} = 985 MHz	25°C		62.8		dBFS
f_{IN} = 1950 MHz	25°C		59.0		dBFS
NSR Enabled (21% Bandwidth (BW) Mode)					
f_{IN} = 10 MHz	25°C		75.0		dBFS
f_{IN} = 170 MHz	25°C		74.8		dBFS
f_{IN} = 340 MHz	25°C		74.0		dBFS
f_{IN} = 450 MHz	25°C		73.1		dBFS
f_{IN} = 765 MHz	25°C		69.7		dBFS
f_{IN} = 985 MHz	25°C		68.1		dBFS
f_{IN} = 1950 MHz	25°C		64.6		dBFS
NSR Enabled (28% BW Mode)					
f_{IN} = 10 MHz	25°C		72.4		dBFS
f_{IN} = 170 MHz	25°C		72.3		dBFS
f_{IN} = 340 MHz	25°C		71.6		dBFS
f_{IN} = 450 MHz	25°C		71.0		dBFS
f_{IN} = 765 MHz	25°C		67.7		dBFS
f_{IN} = 985 MHz	25°C		66.8		dBFS
f_{IN} = 1950 MHz	25°C		63.1		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		68.7		dBFS
f_{IN} = 170 MHz	Full	67	68.5		dBFS
f_{IN} = 340 MHz	25°C		67.6		dBFS
f_{IN} = 450 MHz	25°C		67.2		dBFS
f_{IN} = 765 MHz	25°C		63.8		dBFS
f_{IN} = 985 MHz	25°C		62.5		dBFS
f_{IN} = 1950 MHz	25°C		58.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		11.1		Bits
f_{IN} = 170 MHz	Full	10.8	10.9		Bits
f_{IN} = 340 MHz	25°C		10.8		Bits
f_{IN} = 450 MHz	25°C		10.8		Bits
f_{IN} = 765 MHz	25°C		10.3		Bits
f_{IN} = 985 MHz	25°C		10.1		Bits
f_{IN} = 1950 MHz	25°C		9.5		Bits

Parameter[1]	Temperature	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR), SECOND OR THIRD HARMONIC[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		83		dBFS
f_{IN} = 170 MHz	Full	76	85		dBFS
f_{IN} = 340 MHz	25°C		82		dBFS
f_{IN} = 450 MHz	25°C		86		dBFS
f_{IN} = 765 MHz	25°C		81		dBFS
f_{IN} = 985 MHz	25°C		76		dBFS
f_{IN} = 1950 MHz	25°C		69		dBFS
WORST OTHER (EXCLUDING SECOND OR THIRD HARMONIC)[3]					
VDR Mode (Input Mask Not Triggered)					
f_{IN} = 10 MHz	25°C		−93		dBFS
f_{IN} = 170 MHz	Full		−94		dBFS
f_{IN} = 340 MHz	25°C		−90		dBFS
f_{IN} = 450 MHz	25°C		−92		dBFS
f_{IN} = 765 MHz	25°C		−89		dBFS
f_{IN} = 985 MHz	25°C		−89		dBFS
f_{IN} = 1950 MHz	25°C		−85		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD)[3], A_{IN1} AND A_{IN2} = −7.0 dBFS					
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz	25°C		−88		dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C		−87		dBFS
CROSSTALK[4]	25°C		95		dB
FULL POWER BANDWIDTH	25°C		2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (30 MHz).
[3] See Table 11 for the recommended settings for full-scale voltage and buffer control settings.
[4] Crosstalk is measured at 185 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYSTEM REFERENCE INPUTS (SYNC+, SYNC−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full		0.8 × SPIVDD		V
Logic 0 Voltage	Full	0	0.2 × SPIVDD		V
Input Resistance	Full		30		kΩ

Parameter	Temperature	Min	Typ	Max	Unit
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	Full		0.8 × SPIVDD		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full		0.2 × SPIVDD		V
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8	SPIVDD		V
Logic 0 Voltage	Full	0	0		V
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (D0± to D13±, A Dx/Dy± and B Dx/Dy±, DATA0± to DATA7±, DCO±, OVR±, FCO±, and STATUS±)					
Logic Compliance	Full		LVDS		
ANSI Mode					
Differential Output Voltage (V_{OD})	Full	230	350	430	mV
Output Offset Voltage (V_{OS})	Full	0.58	0.70	0.85	V
Reduced Swing Mode					
Differential Output Voltage (V_{OD})	Full	120	200	235	mV
Output Offset Voltage (V_{OS})	Full	0.59	0.70	0.83	V

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, 1.0 V internal reference, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK					
Clock Rate (at CLK+/CLK− Pins)	Full	0.3		4	GHz
Sample Rate					
Maximum[1]	Full	500			MSPS
Minimum[2]	Full	250			MSPS
Clock Pulse Width					
High	Full	1000			ps
Low	Full	1000			ps
LVDS DATA OUTPUT					
Data Propagation Delay (t_{PD})[3]	Full		2.225		ns
DCO± Propagation Delay (t_{DCO})[3]	Full		2.2		ns
DCO± to Data Skew—Rising Edge Data (t_{SKEWR})[3]	Full	−150	−25	+100	ps
DCO± to Data Skew—Falling Edge Data (t_{SKEWF})[3]	Full	−150	−25	+100	ps
DCO± and Data Duty Cycle	Full	44	50	56	%
FCO± Propagation Delay (t_{FCO})[4]	Full		2.2		ns
DCO± to FCO± Skew (t_{FRAME})[4]	Full	−150	−25	+100	ps
DCO Output Frequency	Full			500	MHz
Output Date Rate	Full			1000	Mbps
LATENCY					
Pipeline Latency	Full		33		Clock cycles
NSR Latency[5]	Full		8		Clock cycles
NSR HB Filter Latency[5]	Full		24		Clock cycles
VDR Latency[5]	Full		8		Clock cycles
HB1 Filter Latency[5]	Full		50		Clock cycles
HB1 + HB2 Filter Latency[5]	Full		101		Clock cycles
HB1 + HB2 + HB3 Filter Latency[5]	Full		217		Clock cycles
HB1 + HB2 + HB3 + HB4 Filter Latency[5]	Full		433		Clock cycles
Fast Detect Latency	Full		28		Clock cycles

Parameter	Temperature	Min	Typ	Max	Unit
Wake-Up Time[6]					
Standby	25°C		1		ms
Power-Down[6]	25°C			4	ms
APERTURE					
Aperture Delay (t_A)	Full		530		ps
Aperture Uncertainty (Jitter, t_J)	Full		55		fs rms
Out of Range Recovery Time	Full		1		Clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 300 MSPS with L = 2 or L = 1.
[3] This specification is valid for parallel interleaved, channel multiplexed, and byte mode output modes.
[4] This specification is valid for byte mode output mode only.
[5] Add this value to the pipeline latency specification to achieve total latency through the AD6679.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode or standby mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK± to SYNC± TIMING REQUIREMENTS					
t_{SU_SR}	Device clock to SYNC± setup time		117		ps
t_{H_SR}	Device clock to SYNC± hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 3				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK is in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK is in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 3)	10			ns

Timing Diagrams

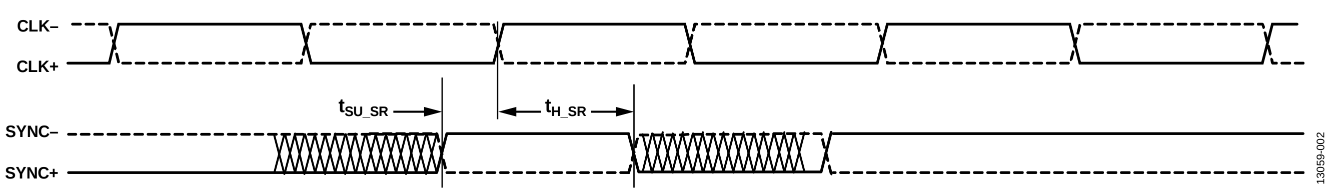


Figure 2. SYNC± Setup and Hold Timing

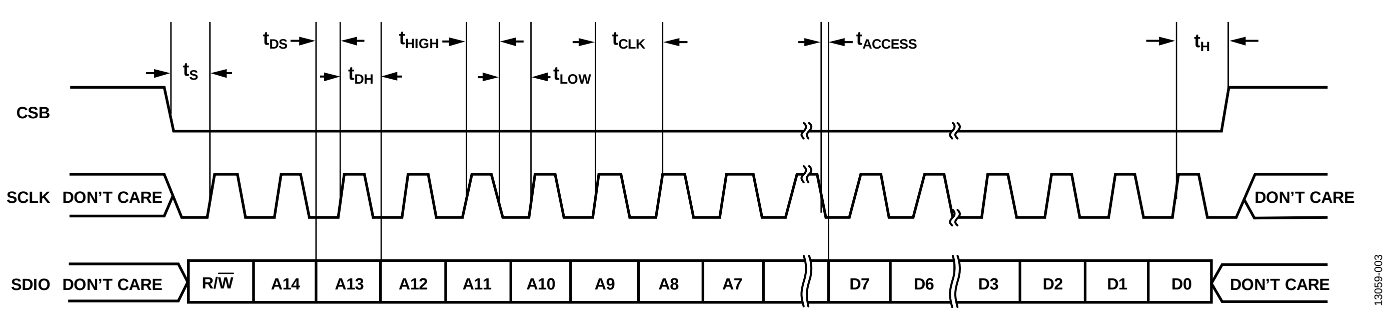
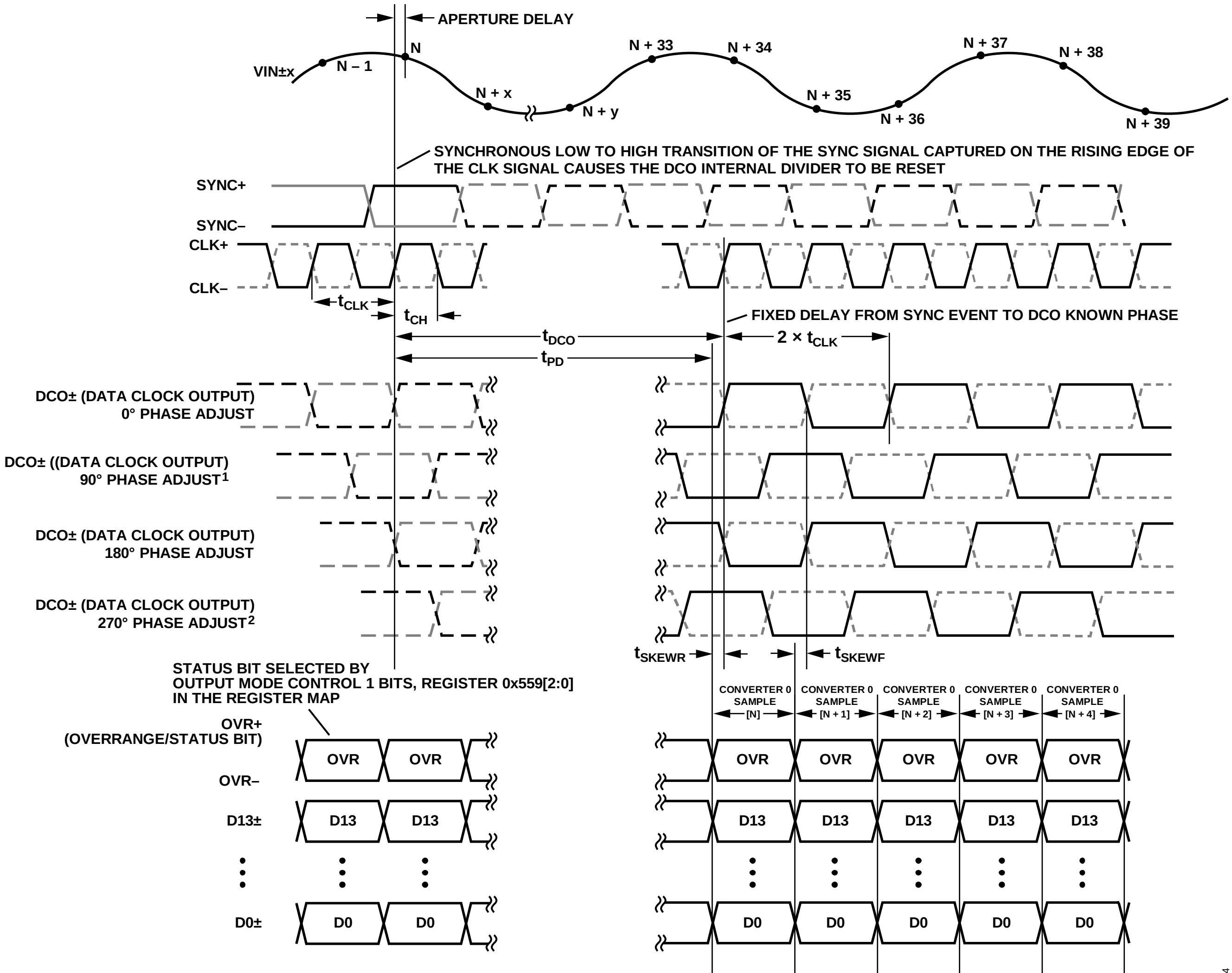


Figure 3. Serial Port Interface Timing Diagram



[1] 90° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
[2] 270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.

Figure 4. Parallel Interleaved Mode—One Virtual Converter (Decimate by 1)

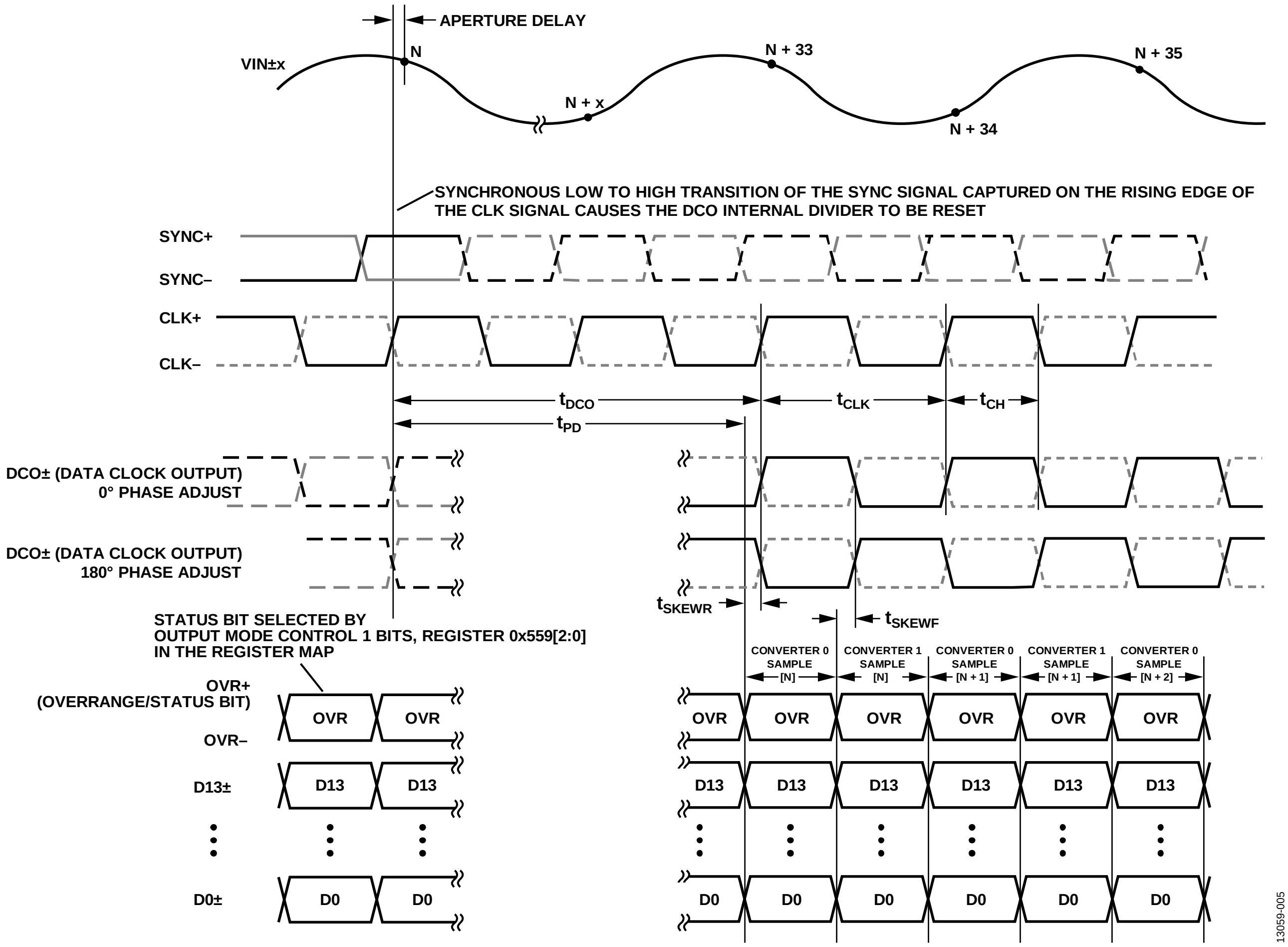


Figure 5. Parallel Interleaved Mode—Two Virtual Converters (Decimate by 1)

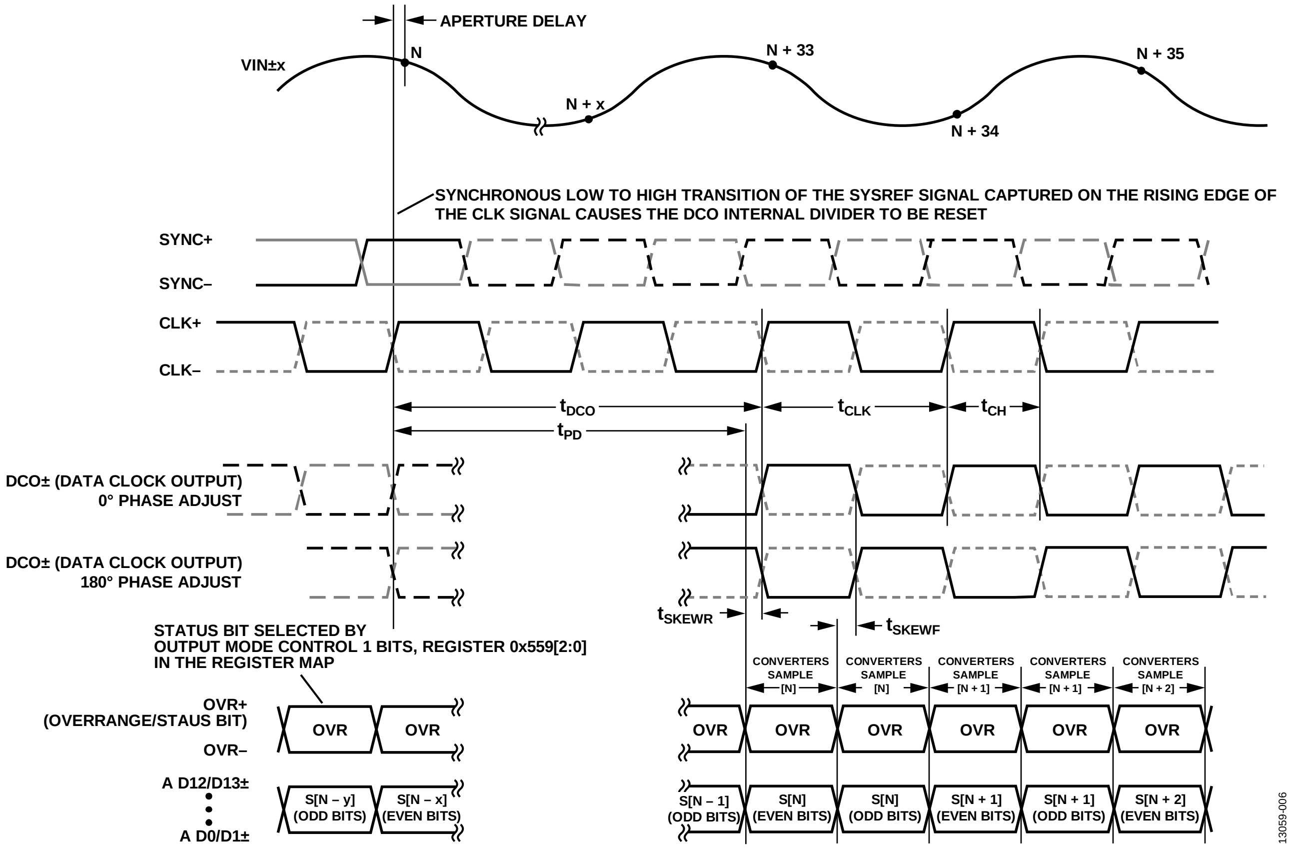


Figure 6. Channel Multiplexed (Even/Odd) Mode—One Virtual Converter (Decimate by 1)

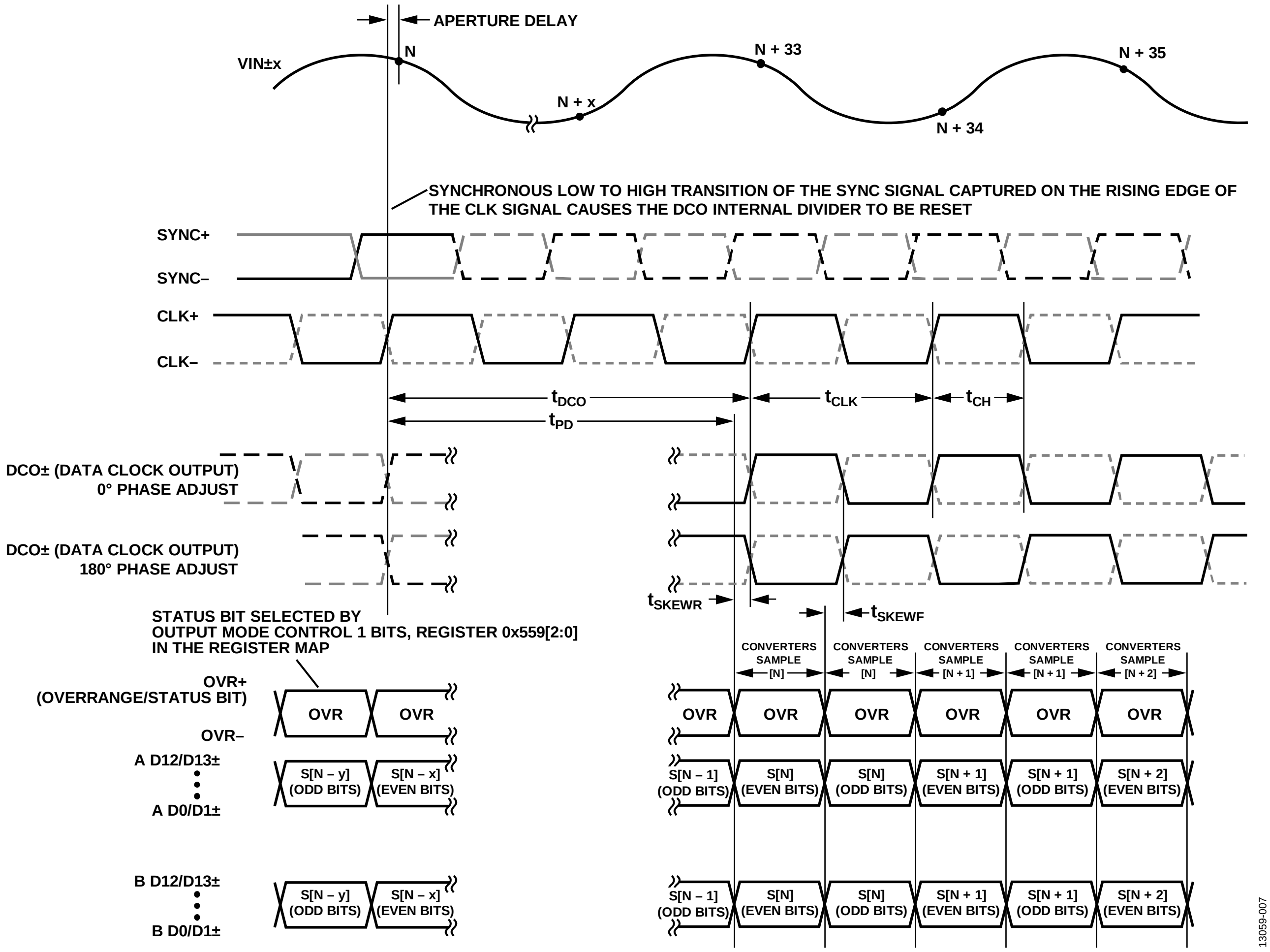
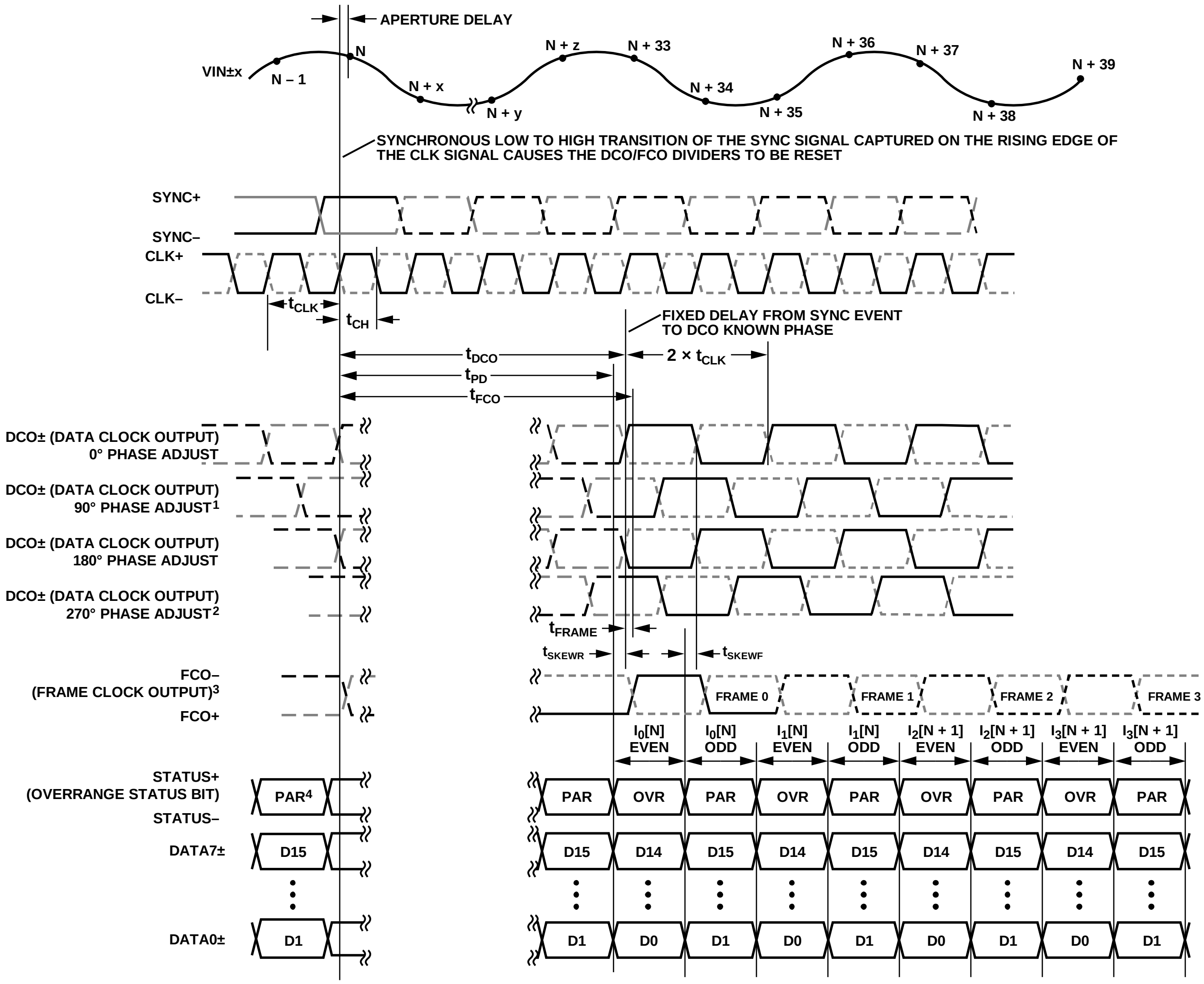


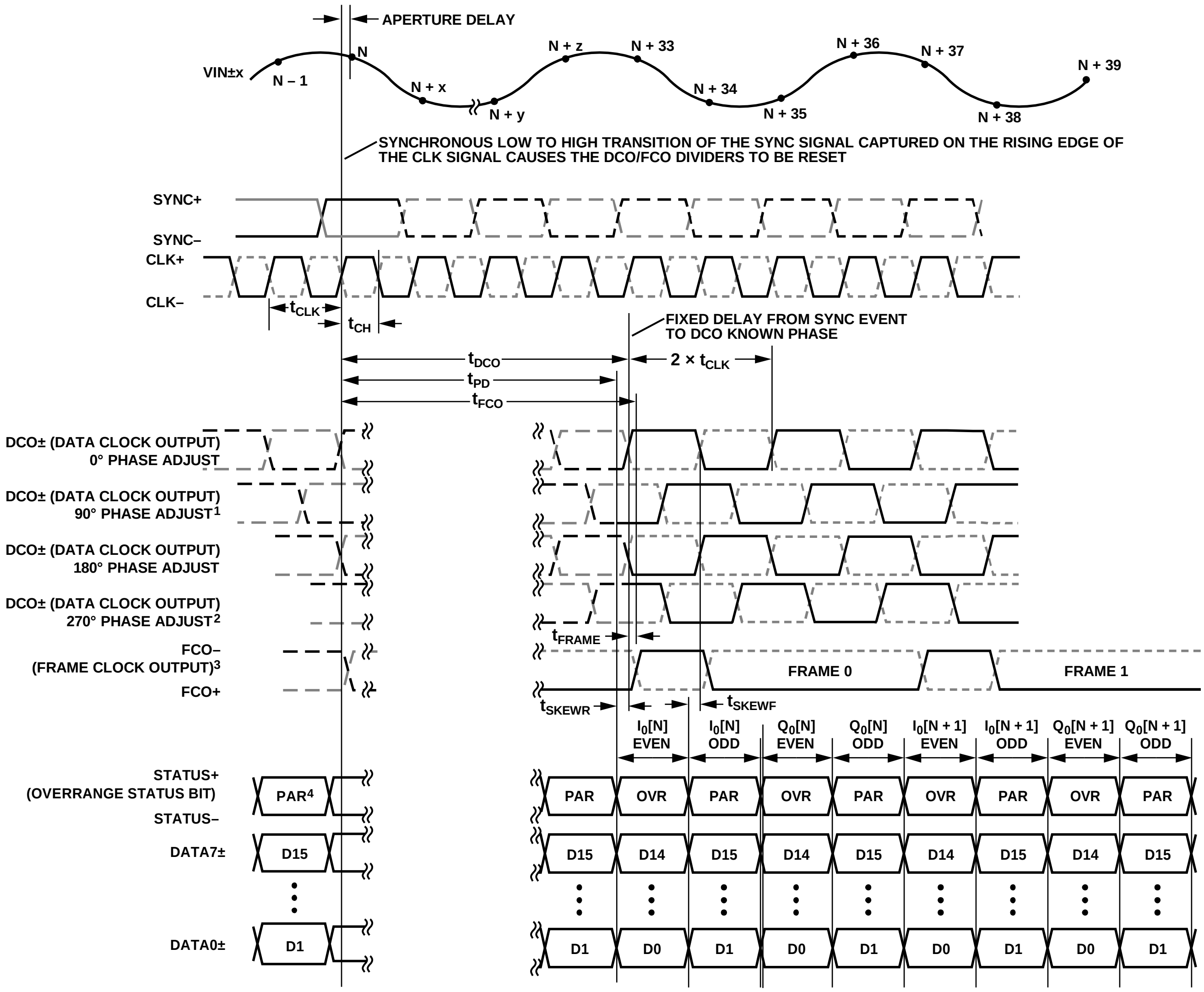
Figure 7. Channel Multiplexed (Even/Odd) Mode—Two Virtual Converters (Decimate by 1)



1 90° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
2 270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
3 FRAME CLOCK OUTPUT SUPPORTS THREE MODES OF OPERATION:
1) ENABLED (ALWAYS ON)
2) DISABLED (ALWAYS OFF)
3) GAPPED PERIODIC (CONDITIONALLY ENABLED BASED ON PSEUDORANDOM BIT)
4 STATUS BIT SELECTED BY THE OUTPUT MODE CONTROL 1 BITS, REGISTER 0x559[2:0] IN THE REGISTER MAP.

13059-100

Figure 8. LVDS Byte Mode—One Virtual Converter, One DDC (I Only, Decimate by 2)



[1]90° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
[2]270° PHASE ADJUST IS GENERATED USING THE FALLING EDGE OF CLK±.
[3]FRAME CLOCK OUTPUT SUPPORTS THREE MODES OF OPERATION:
1) ENABLED (ALWAYS ON)
2) DISABLED (ALWAYS OFF)
3) GAPPED PERIODIC (CONDITIONALLY ENABLED BASED ON PSEUDORANDOM BIT)
[4]STATUS BIT SELECTED BY THE OUTPUT MODE CONTROL 1 BITS, REGISTER 0x559[2:0] IN THE REGISTER MAP.

13059-008

Figure 9. LVDS Byte Mode—Two Virtual Converters, One DDC (I/Q Decimate by 4)

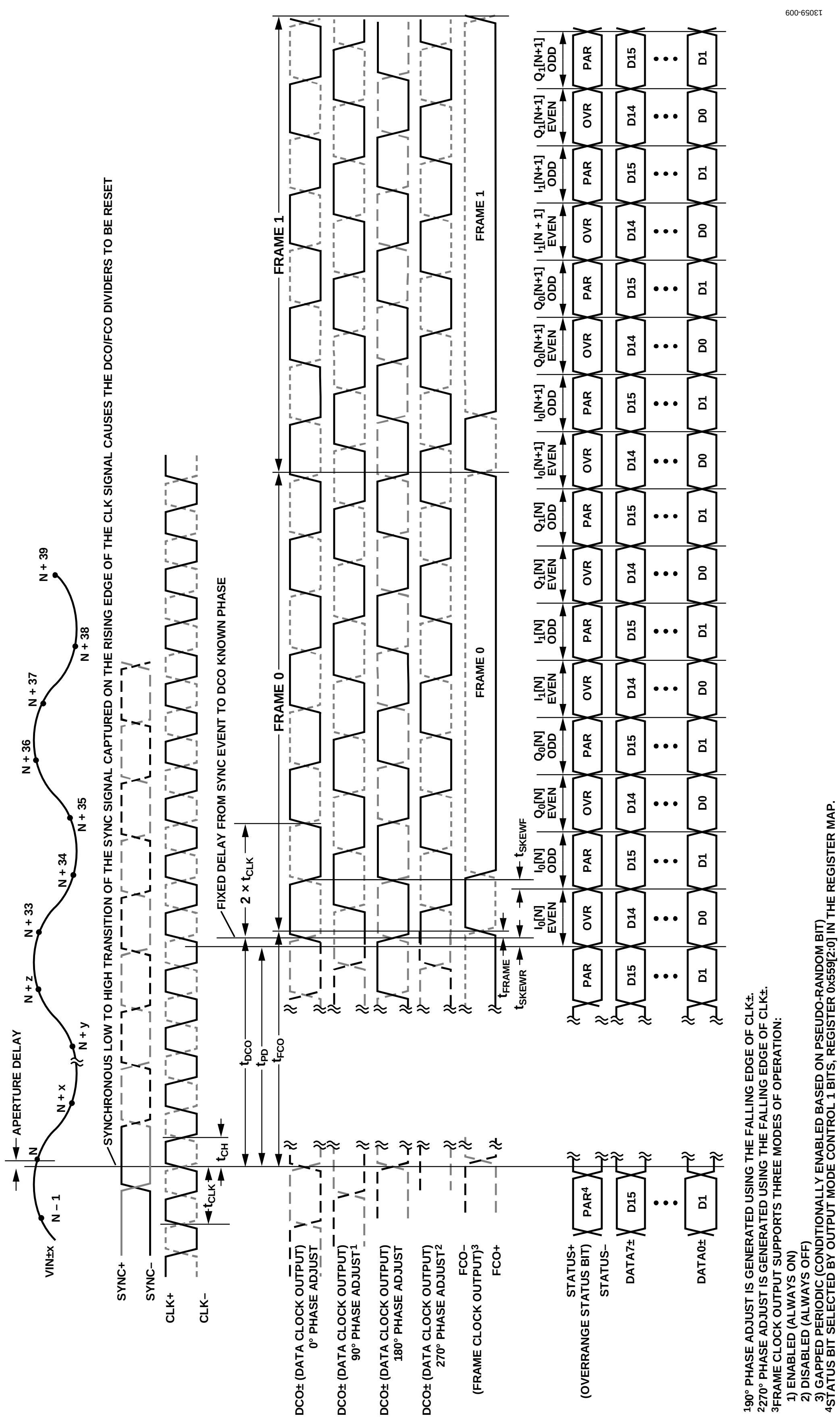


Figure 10. LVDS Byte Mode—Four Virtual Converters, Two DDCs (I/Q Decimate by 8)

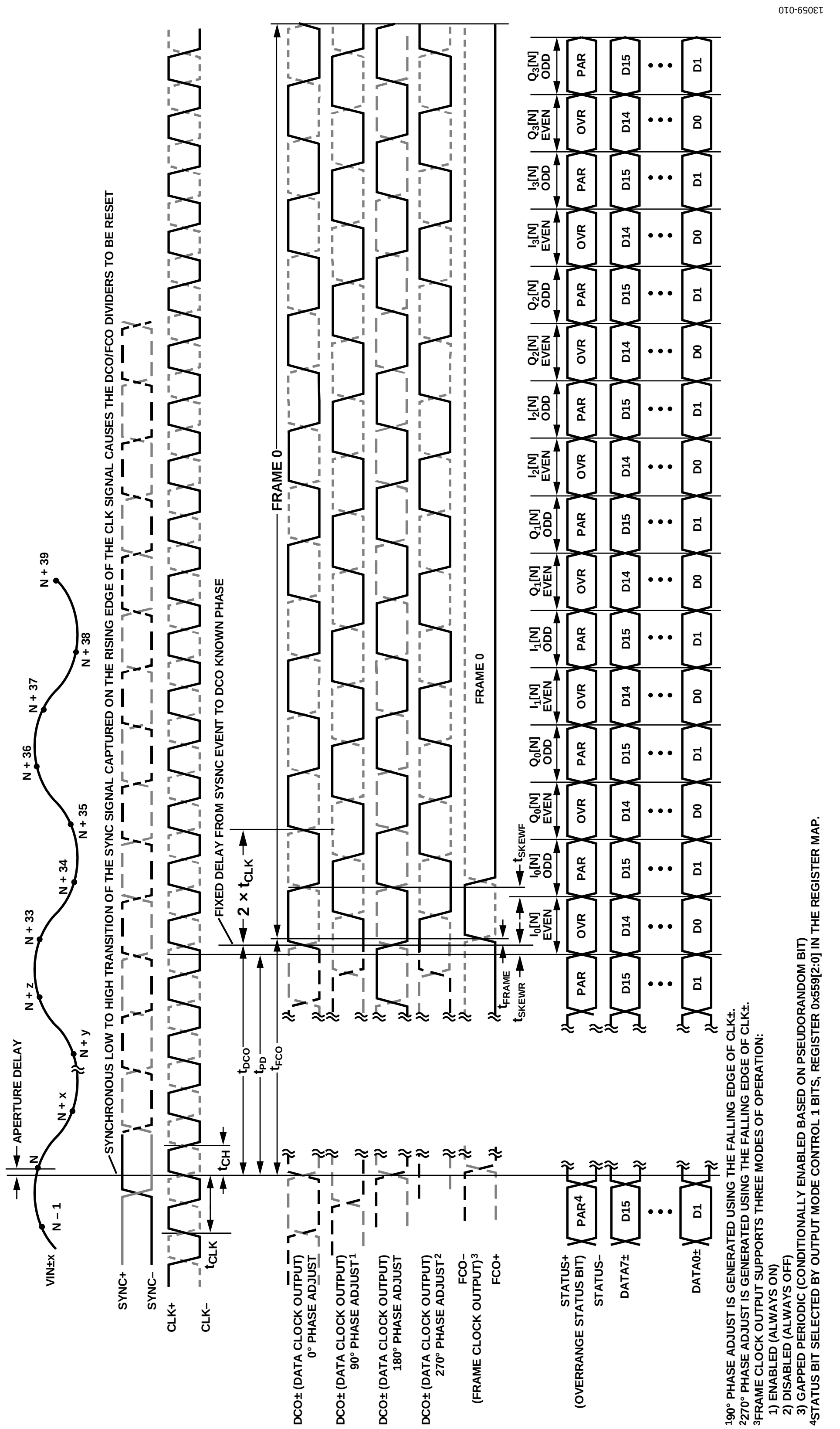


Figure 11. LVDS Byte Mode—Eight Virtual Converters, Four DDCs (I/Q Decimate by 16)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Environmental	
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	+125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, Ψ_{JB}, and Ψ_{JT} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation, effectively reducing θ_{JA} and Ψ_{JB}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	Ψ_{JT}	Ψ_{JB}	Unit
JEDEC 2s2p Board	0.0	27.0[1, 2]	0.7[1, 3]	7.3[1, 3]	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	AGND	AGND	AGND	AVDD2	AVDD1	AGND	CLK+	CLK–	AGND	AVDD1	AVDD2	AGND	AGND	AGND	A
B	AVDD3	AGND	AGND	AVDD2	AVDD1	AGND	AGND	AGND	AGND	AVDD1	AVDD2	AGND	AGND	AVDD3	B
C	AVDD3	AGND	AGND	AVDD2	AVDD1	AGND	SYNC+	SYNC–	AGND	AVDD1	AVDD2	AGND	AGND	AVDD3	C
D	AGND	AGND	AGND	AVDD2	AVDD1	AGND	AVDD1	AGND	AGND	AVDD1	AVDD2	AGND	AGND	AGND	D
E	VIN–B	AGND	AGND	AVDD2	AVDD1	AGND	AGND	AGND	AGND	AVDD1	AVDD2	AGND	AGND	VIN–A	E
F	VIN+B	AGND	AGND	AVDD2	AGND	AGND	AGND	AGND	AGND	AGND	AVDD2	AGND	AGND	VIN+A	F
G	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD2	AGND	AGND	AGND	G
H	AGND	AGND	AGND	CSB	AGND	AGND	AGND	AGND	AGND	V_1P0	AGND	AGND	AGND	AGND	H
J	FD_B	AGND	AGND	SCLK	SPIVDD	AGND	AGND	AGND	AGND	AVDD2	SPIVDD	AGND	PDWN/ STBY	FD_A	J
K	DGND	DGND	AGND	SDIO	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DCO–	DCO+	K
L	DVDD	DVDD	DGND	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	OVR–	OVR+	L
M	D1+	D1–	DVDD	DVDD	DRVDD	DRVDD	DRVDD	DRGND	DRGND	DRGND	DRGND	DRGND	D13–	D13+	M
N	D2–	D3–	D4–	D5–	D6–	D0–	DRVDD	DRGND	D7–	D8–	D9–	D10–	D11–	D12–	N
P	D2+	D3+	D4+	D5+	D6+	D0+	DRVDD	DRGND	D7+	D8+	D9+	D10+	D11+	D12+	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

1.25V ANALOG SUPPLY
2.50V ANALOG SUPPLY
3.3V ANALOG SUPPLY
1.25V DIGITAL SUPPLY
1.25V LVDS DRIVER SUPPLY
1.22V TO 3.4V SPI SUPPLY
ANALOG GROUND
DIGITAL GROUND
LVDS DRIVER GROUND
ADC I/O
LVDS INTERFACE
SPI INTERFACE

13059-011

Figure 12. Pin Configuration—Parallel Interleaved LVDS Mode (Top View)

Table 8. Pin Function Descriptions—Parallel Interleaved LVDS Mode

Pin No.	Mnemonic	Type	Description
Power Supplies			
A5, A10, B5, B10, C5, C10, D5, D7, D10, E5, E10	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
A4, A11, B4, B11, C4, C11, D4, D11, E4, E11, F4, F11, G11, J10	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
B1, B14, C1, C14	AVDD3	Supply	Analog Power Supply (3.3 V Nominal)
L1, L2, M3, M4	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
M5 to M7, N7, P7	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
J5, J11	SPIVDD	Supply	Digital Power Supply for SPI (1.22 V to 3.4 V).
K1, K2, L3, L4	DGND	Ground	Ground Reference for DVDD.
M8 to M12, N8, P8	DRGND	Ground	Ground Reference for DRVDD.
A1 to A3, A6, A9, A12 to A14, B2, B3, B6 to B9, B12, B13, C2, C3, C6, C9, C12, C13, D1 to D3, D6, D8, D9, D12 to D14, E2, E3, E6 to E9, E12, E13, F2, F3, F5 to F10, F12, F13, G1 to G10, G12 to G14, H1 to H3, H5 to H9, H11 to H14, J2, J3, J6 to J9, J12, K3, K5 to K12, L5 to L12	AGND	Ground	Analog Ground.
Analog			
E14, F14	VIN–A, VIN+A	Input	ADC A Analog Input Complement/True.
E1, F1	VIN–B, VIN+B	Input	ADC B Analog Input Complement/True.

Pin No.	Mnemonic	Type	Description
H10	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or as an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
A7, A8	CLK+, CLK−	Input	Clock Input True/Complement.
CMOS Outputs			
J14, J1	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
C7, C8	SYNC+, SYNC−	Input	Active High LVDS Sync Input—True/Complement.
Data Outputs			
N6, P6	D0−, D0+	Output	LVDS Lane 0 Output Data—Complement/True.
M2, M1	D1−, D1+	Output	LVDS Lane 1 Output Data—Complement/True.
N1, P1	D2−, D2+	Output	LVDS Lane 2 Output Data—Complement/True.
N2, P2	D3−, D3+	Output	LVDS Lane 3 Output Data—Complement/True.
N3, P3	D4−, D4+	Output	LVDS Lane 4 Output Data—Complement/True.
N4, P4	D5−, D5+	Output	LVDS Lane 5 Output Data—Complement/True.
N5, P5	D6−, D6+	Output	LVDS Lane 6 Output Data—Complement/True.
N9, P9	D7−, D7+	Output	LVDS Lane 7 Output Data—Complement/True.
N10, P10	D8−, D8+	Output	LVDS Lane 8 Output Data—Complement/True.
N11, P11	D9−, D9+	Output	LVDS Lane 9 Output Data—Complement/True.
N12, P12	D10−, D10+	Output	LVDS Lane 10 Output Data—Complement/True.
N13, P13	D11−, D11+	Output	LVDS Lane 11 Output Data—Complement/True.
N14, P14	D12−, D12+	Output	LVDS Lane 12 Output Data—Complement/True.
M13, M14	D13−, D13+	Output	LVDS Lane 13 Output Data—Complement/True.
L13, L14	OVR−, OVR+	Output	LVDS Overrange Output Data—Complement/True.
K13, K14	DCO−, DCO+	Output	LVDS Digital Clock Output Data—Complement/True.
Device Under Test (DUT) Controls			
K4	SDIO	Input/output	SPI Serial Data Input/Output.
J4	SCLK	Input	SPI Serial Clock.
H4	CSB	Input	SPI Chip Select (Active Low).
J13	PDWN/STBY	Input	Power-Down Input (Active High)/Standby. The operation of this pin depends on the SPI mode and can be configured in power-down or standby mode.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	AGND	AGND	AGND	AVDD2	AVDD1	AGND	CLK+	CLK–	AGND	AVDD1	AVDD2	AGND	AGND	AGND	A
B	AVDD3	AGND	AGND	AVDD2	AVDD1	AGND	AGND	AGND	AGND	AVDD1	AVDD2	AGND	AGND	AVDD3	B
C	AVDD3	AGND	AGND	AVDD2	AVDD1	AGND	SYNC+	SYNC–	AGND	AVDD1	AVDD2	AGND	AGND	AVDD3	C
D	AGND	AGND	AGND	AVDD2	AVDD1	AGND	AVDD1	AGND	AGND	AVDD1	AVDD2	AGND	AGND	AGND	D
E	VIN–B	AGND	AGND	AVDD2	AVDD1	AGND	AGND	AGND	AGND	AVDD1	AVDD2	AGND	AGND	VIN–A	E
F	VIN+B	AGND	AGND	AVDD2	AGND	AGND	AGND	AGND	AGND	AGND	AVDD2	AGND	AGND	VIN+A	F
G	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD2	AGND	AGND	AGND	G
H	AGND	AGND	AGND	CSB	AGND	AGND	AGND	AGND	AGND	V_1P0	AGND	AGND	AGND	AGND	H
J	FD_B	AGND	AGND	SCLK	SPIVDD	AGND	AGND	AGND	AGND	AVDD2	SPIVDD	AGND	PDWN/ STBY	FD_A	J
K	DGND	DGND	AGND	SDIO	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DCO–	DCO+	K
L	DVDD	DVDD	DGND	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	OVR–	OVR+	L
M	B D2/D3+	B D2/D3–	DVDD	DVDD	DRVDD	DRVDD	DRVDD	DRGND	DRGND	DRGND	DRGND	DRGND	A D12/D13–	A D12/D13+	M
N	B D4/D5–	B D6/D7–	B D8/D9–	B D10/D11–	B D12/D13–	B D0/D1–	DRVDD	DRGND	A D0/D1–	A D2/D3–	A D4/D5–	A D6/D7–	A D8/D9–	A D10/D11–	N
P	B D4/D5+	B D6/D7+	B D8/D9+	B D10/D11+	B D12/D13+	B D0/D1+	DRVDD	DRGND	A D0/D1+	A D2/D3+	A D4/D5+	A D6/D7+	A D8/D9+	A D10/D11+	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

1.25V ANALOG SUPPLY
2.50V ANALOG SUPPLY
3.3V ANALOG SUPPLY
1.25V DIGITAL SUPPLY
1.25V LVDS DRIVER SUPPLY
1.22V TO 3.4V SPI SUPPLY
ANALOG GROUND
DIGITAL GROUND
LVDS DRIVER GROUND
ADC I/O
LVDS INTERFACE
SPI INTERFACE

13059-012

Figure 13. Pin Configuration—Channel Multiplexed (Even/Odd) LVDS Mode (Top View)

Table 9. Pin Function Descriptions—Channel Multiplexed (Even/Odd) LVDS Mode[1]

Pin No.	Mnemonic	Type	Description
Power Supplies			
A5, A10, B5, B10, C5, C10, D5, D7, D10, E5, E10	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
A4, A11, B4, B11, C4, C11, D4, D11, E4, E11, F4, F11, G11, J10	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
B1, B14, C1, C14	AVDD3	Supply	Analog Power Supply (3.3 V Nominal)
L1, L2, M3, M4	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
M5 to M7, N7, P7	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
J5, J11	SPIVDD	Supply	Digital Power Supply for SPI (1.22 V to 3.4 V).
K1, K2, L3, L4	DGND	Ground	Ground Reference for DVDD.
M8 to M12, N8, P8	DRGND	Ground	Ground Reference for DRVDD.
A1 to A3, A6, A9, A12 to A14, B2, B3, B6 to B9, B12, B13, C2, C3, C6, C9, C12, C13, D1 to D3, D6, D8, D9, D12 to D14, E2, E3, E6 to E9, E12, E13, F2, F3, F5 to F10, F12, F13, G1 to G10, G12 to G14, H1 to H3, H5 to H9, H11 to H14, J2, J3, J6 to J9, J12, K3, K5 to K12, L5 to L12	AGND	Ground	Analog Ground.
Analog			
E14, F14	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
E1, F1	VIN−B, VIN+B	Input	ADC B Analog Input Complement/True.
H10	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or as an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
A7, A8	CLK+, CLK−	Input	Clock Input True/Complement.

Pin No.	Mnemonic	Type	Description
CMOS Outputs			
J14, J1	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
C7, C8	SYNC+, SYNC−	Input	Active High LVDS Sync Input—True/Complement.
Data Outputs			
N9, P9	A D0/D1−, A D0/D1+	Output	LVDS Channel A Data 0/Data 1 Output Data—Complement/True.
N10, P10	A D2/D3−, A D2/D3+	Output	LVDS Channel A Data 2/Data 3 Output Data—Complement/True.
N11, P11	A D4/D5−, A D4/D5+	Output	LVDS Channel A Data 4/Data 5 Output Data—Complement/True.
N12, P12	A D6/D7−, A D6/D7+	Output	LVDS Channel A Data 6/Data 7 Output Data—Complement/True.
N13, P13	A D8/D9−, A D8/D9+	Output	LVDS Channel A Data 8/Data 9 Output Data—Complement/True.
N14, P14	A D10/D11−, A D10/D11+	Output	LVDS Channel A Data 10/Data 11 Output Data—Complement/True.
M13, M14	A D12/D13−, A D12/D13+	Output	LVDS Channel A Data 12/Data 13 Output Data—Complement/True.
N6, P6	B D0/D1−, B D0/D1+	Output	LVDS Channel B Data 0/Data 1 Output Data—Complement/True.
M2, M1	B D2/D3−, B D2/D3+	Output	LVDS Channel B Data 2/Data 3 Output Data—Complement/True.
N1, P1	B D4/D5−, B D4/D5+	Output	LVDS Channel B Data 4/Data 5 Output Data—Complement/True.
N2, P2	B D6/D7−, B D6/D7+	Output	LVDS Channel B Data 6/Data 7 Output Data—Complement/True.
N3, P3	B D8/D9−, B D8/D9+	Output	LVDS Channel B Data 8/Data 9 Output Data—Complement/True.
N4, P4	B D10/D11−, B D10/D11+	Output	LVDS Channel B Data 10/Data 11 Output Data—Complement/True.
N5, P5	B D12/D13−, B D12/D13+	Output	LVDS Channel B Data 12/Data 13 Output Data—Complement/True.
L13, L14	OVR−, OVR+	Output	LVDS Overrange Output Data—Complement/True.
K13, K14	DCO−, DCO+	Output	LVDS Digital Clock Output Data—Complement/True.
DUT Controls			
K4	SDIO	Input/output	SPI Serial Data Input/Output.
J4	SCLK	Input	SPI Serial Clock.
H4	CSB	Input	SPI Chip Select (Active Low).
J13	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured in power-down or standby mode.

[1] When using channel multiplexed (even/odd) LVDS mode for one converter, the Channel B outputs are disabled and can be left unconnected.

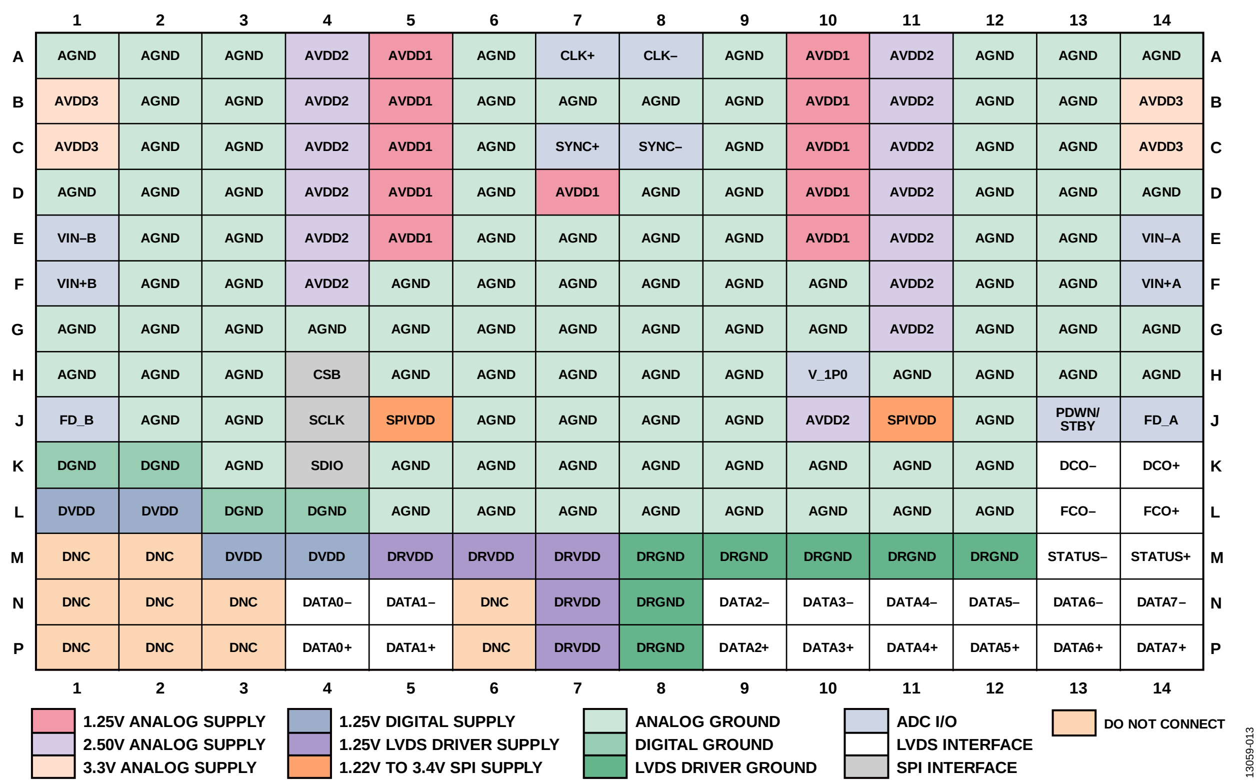


Figure 14. Pin Configuration—LVDS Byte Mode (Top View)

Table 10. Pin Function Descriptions—LVDS Byte Mode

Pin No.	Mnemonic	Type	Description
Power Supplies			
A5, A10, B5, B10, C5, C10, D5, D7, D10, E5, E10	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
A4, A11, B4, B11, C4, C11, D4, D11, E4, E11, F4, F11, G11, J10	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
B1, B14, C1, C14	AVDD3	Supply	Analog Power Supply (3.3 V Nominal)
L1, L2, M3, M4	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
M5 to M7, N7, P7	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
J5, J11	SPIVDD	Supply	Digital Power Supply for SPI (1.22 V to 3.4 V).
K1, K2, L3, L4	DGND	Ground	Ground Reference for DVDD.
M8 to M12, N8, P8	DRGND	Ground	Ground Reference for DRVDD.
A1 to A3, A6, A9, A12 to A14, B2, B3, B6 to B9, B12, B13, C2, C3, C6, C9, C12, C13, D1 to D3, D6, D8, D9, D12 to D14, E2, E3, E6 to E9, E12, E13, F2, F3, F5 to F10, F12, F13, G1 to G10, G12 to G14, H1 to H3, H5 to H9, H11 to H14, J2, J3, J6 to J9, J12, K3, K5 to K12, L5 to L12	AGND	Ground	Analog Ground.
Analog			
E14, F14	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
E1, F1	VIN−B, VIN+B	Input	ADC B Analog Input Complement/True.
H10	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
A7, A8	CLK+, CLK−	Input	Clock Input True/Complement.

Pin No.	Mnemonic	Type	Description
CMOS Outputs			
J14, J1	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.
Digital Inputs			
C7, C8	SYNC+, SYNC−	Input	Active High LVDS Sync Input—True/Complement.
Data Outputs			
N4, P4	DATA0−, DATA0+	Output	LVDS Byte Data 0—Complement/True.
N5, P5	DATA1−, DATA1+	Output	LVDS Byte Data 1—Complement/True.
N9, P9	DATA2−, DATA2+	Output	LVDS Byte Data 2—Complement/True.
N10, P10	DATA3−, DATA3+	Output	LVDS Byte Data 3—Complement/True.
N11, P11	DATA4−, DATA4+	Output	LVDS Byte Data 4—Complement/True.
N12, P12	DATA5−, DATA5+	Output	LVDS Byte Data 5—Complement/True.
N13, P13	DATA6−, DATA6+	Output	LVDS Byte Data 6—Complement/True.
N14, P14	DATA7−, DATA7+	Output	LVDS Byte Data 7—Complement/True.
M13, M14	STATUS−, STATUS+	Output	LVDS Status Output Data—Complement/True.
L13, L14	FCO−, FCO+	Output	LVDS Frame Clock Output Data—Complement/True.
K13, K14	DCO−, DCO+	Output	LVDS Digital Clock Output Data—Complement/True.
DUT Controls			
K4	SDIO	Input/output	SPI Serial Data Input/Output.
J4	SCLK	Input	SPI Serial Clock.
H4	CSB	Input	SPI Chip Select (Active Low).
J13	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured in power-down or standby mode.
No Connects			
M1, M2, N1 to N3, N6, P1 to P3, P6	DNC	DNC	Do Not Connect. Do not connect to these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, A_{IN} = −1.0 dBFS, VDR mode (no violation of VDR mask), clock divider = 2, otherwise default SPI settings, T_A = 25°C, 128k FFT sample, unless otherwise noted.

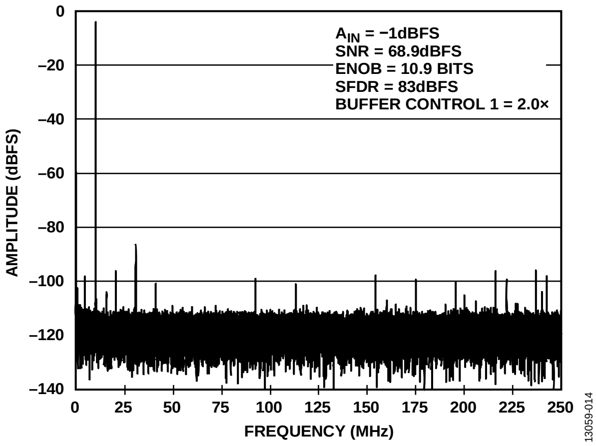


Figure 15. Single Tone FFT with f_{IN} = 10.3 MHz

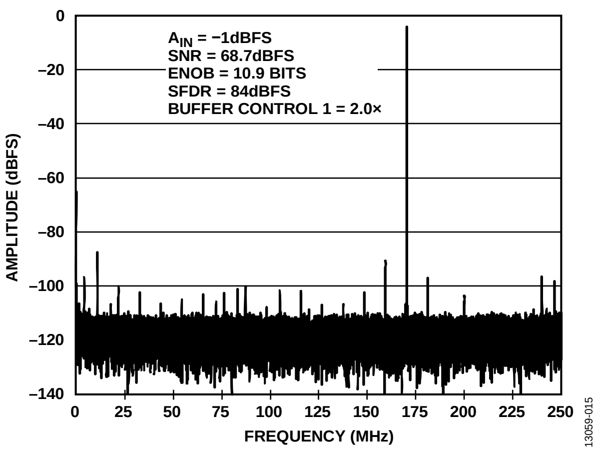


Figure 16. Single-Tone FFT with f_{IN} = 170.3 MHz

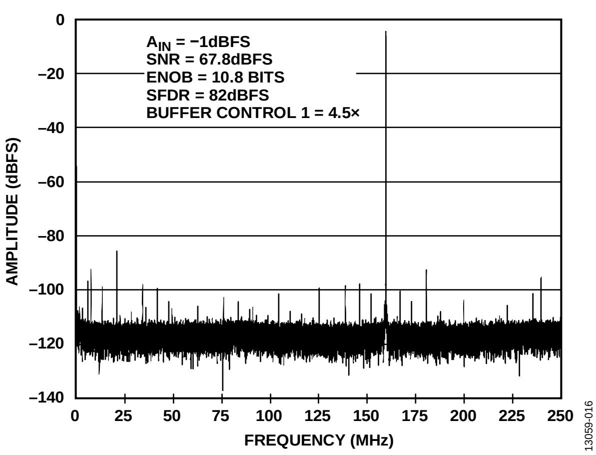


Figure 17. Single-Tone FFT with f_{IN} = 340.3 MHz

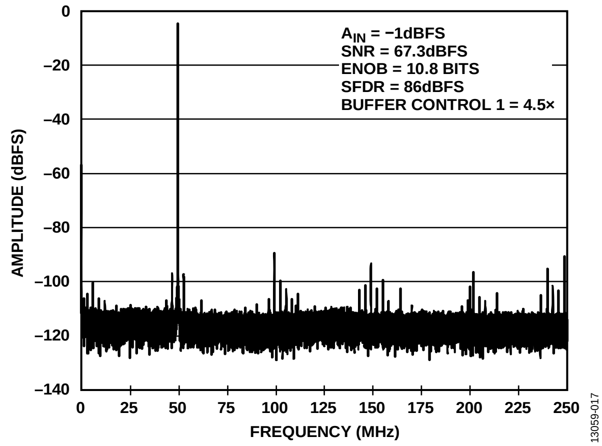


Figure 18. Single-Tone FFT with f_{IN} = 450.3 MHz

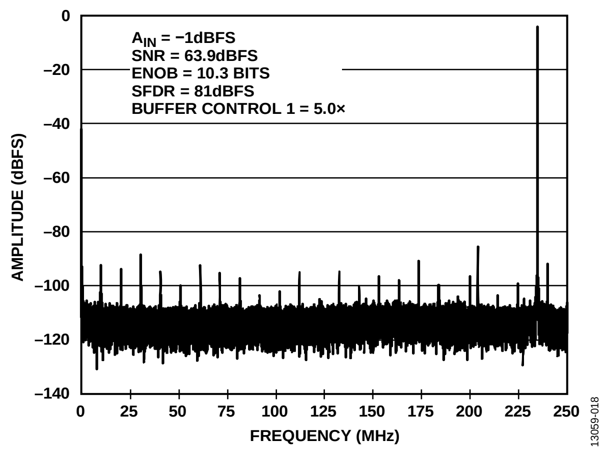


Figure 19. Single-Tone FFT with f_{IN} = 765.3 MHz

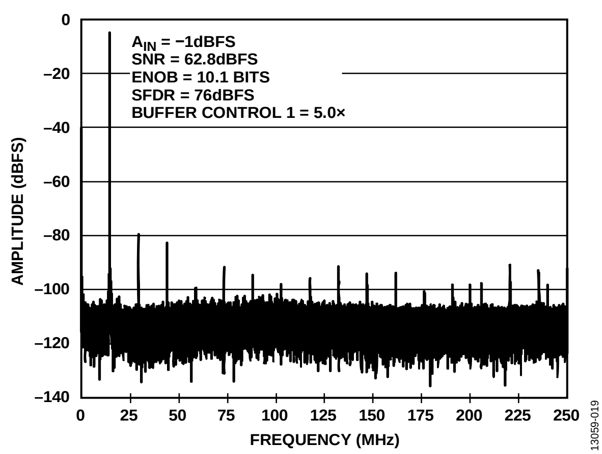


Figure 20. Single-Tone FFT with f_{IN} = 985.3 MHz

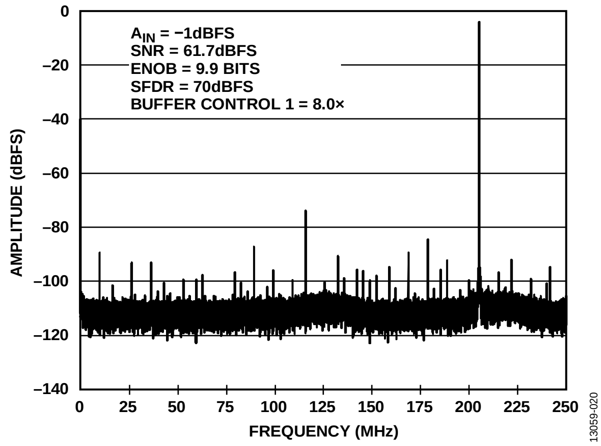


Figure 21. Single-Tone FFT with f_{IN} = 1205.3 MHz

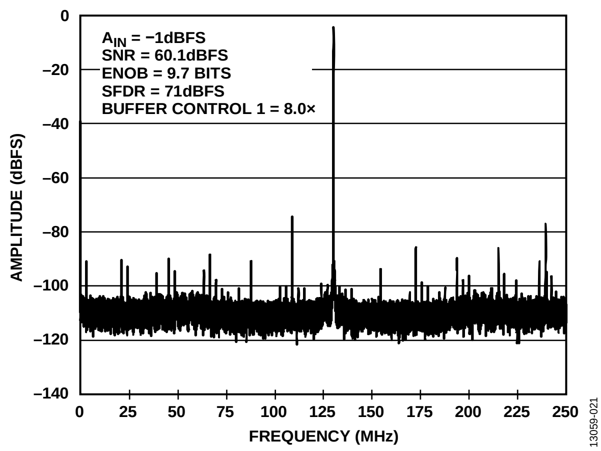


Figure 22. Single-Tone FFT with f_{IN} = 1630.3 MHz

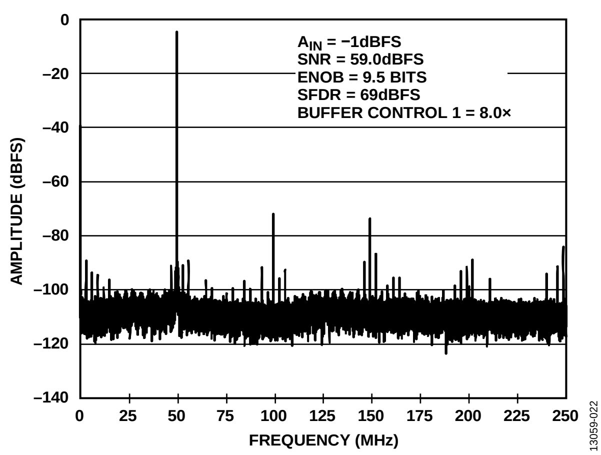


Figure 23. Single-Tone FFT with f_{IN} = 1950.3 MHz

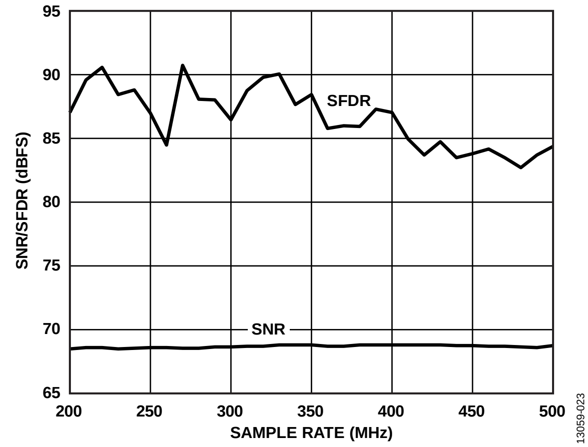


Figure 24. SNR/SFDR vs. Sample Rate (f_S); f_{IN} = 170.3 MHz;

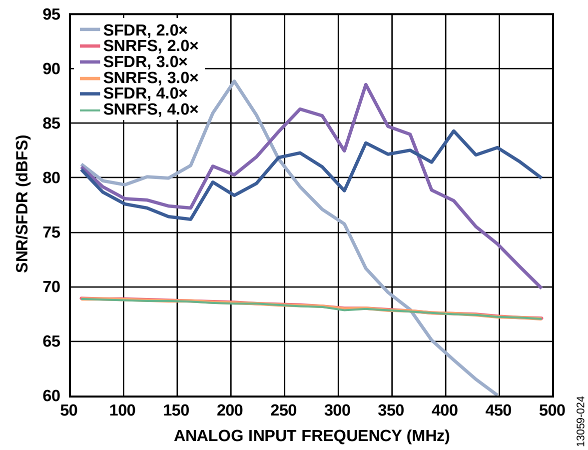


Figure 25. SNR/SFDR vs. Analog Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Control 1 Setting = 2.0×, 3.0×, and 4.0×

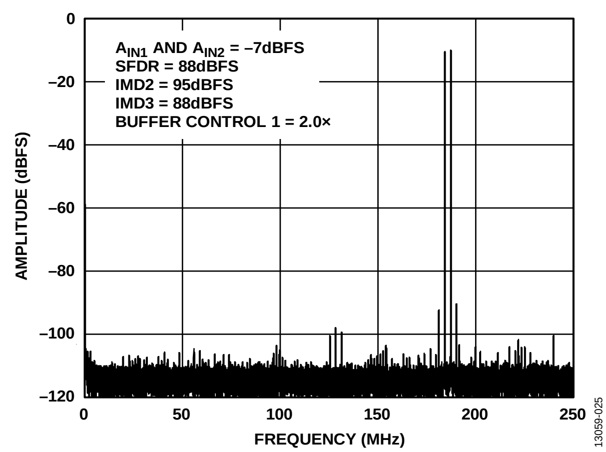


Figure 26. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

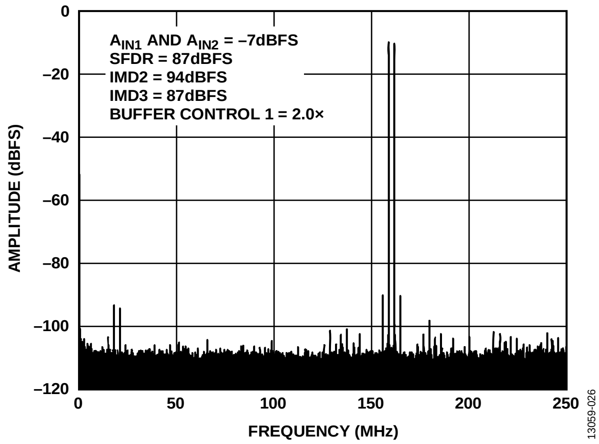


Figure 27. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

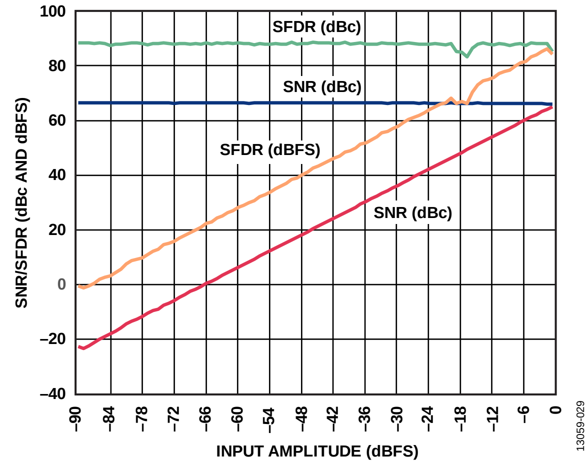


Figure 30. SNR/SFDR vs. Input Amplitude, f_{IN} = 170.3 MHz

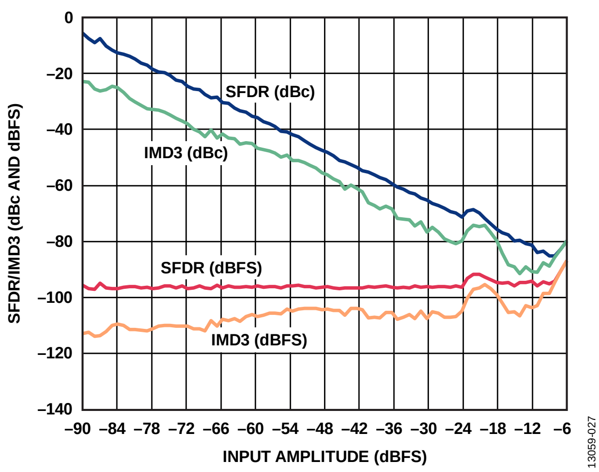


Figure 28. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

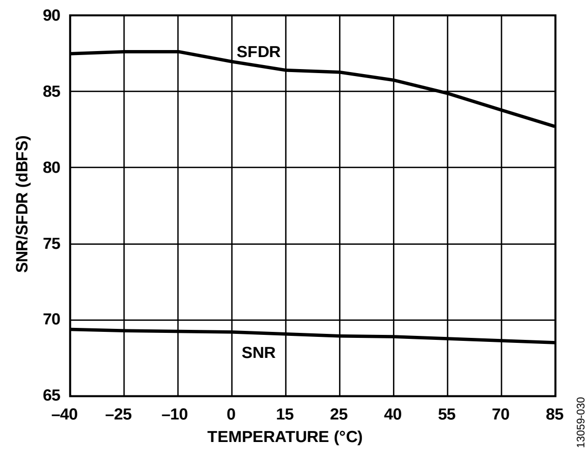


Figure 31. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

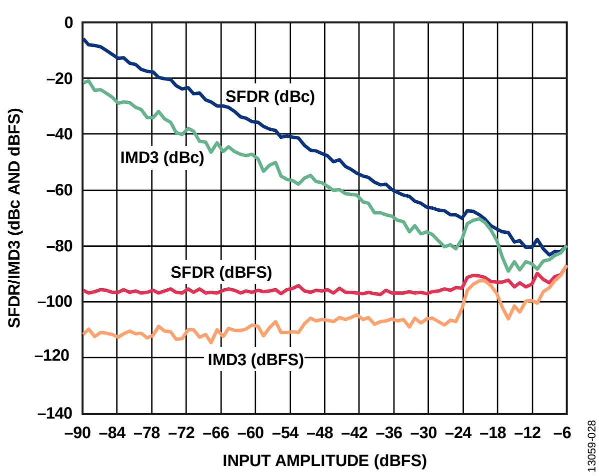


Figure 29. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

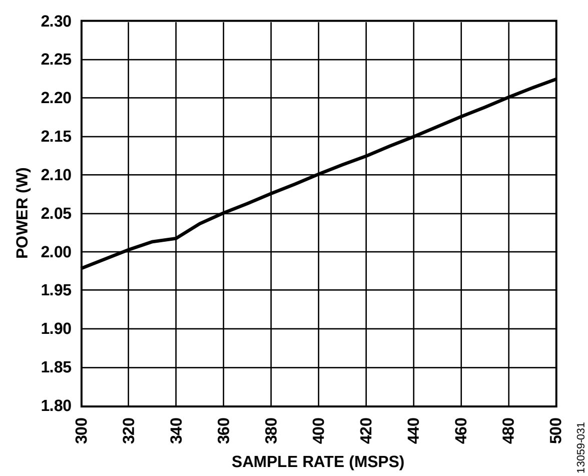


Figure 32. Power Dissipation vs. Sample Rate (f_S), Default SPI

EQUIVALENT CIRCUITS

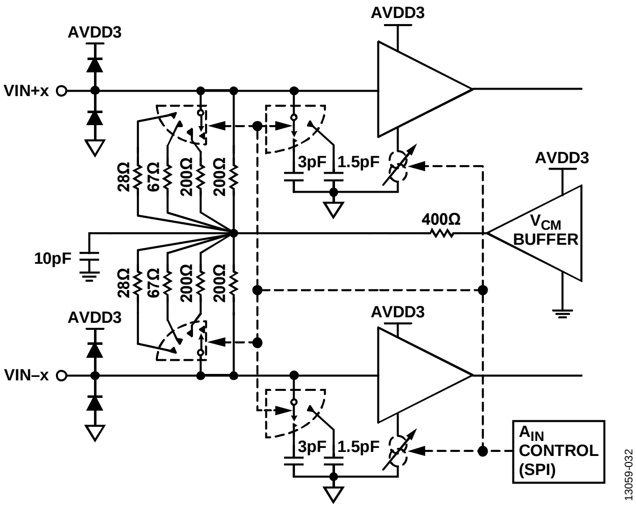


Figure 33. Analog Inputs

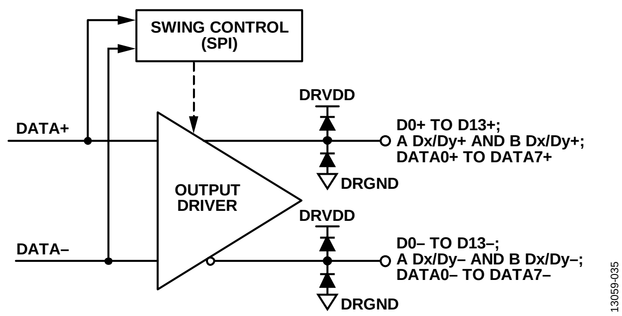


Figure 36. Digital Outputs

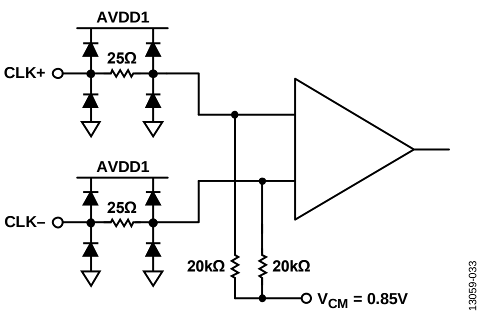


Figure 34. Clock Inputs

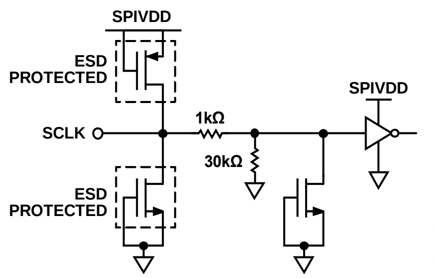


Figure 37. SCLK Inputs

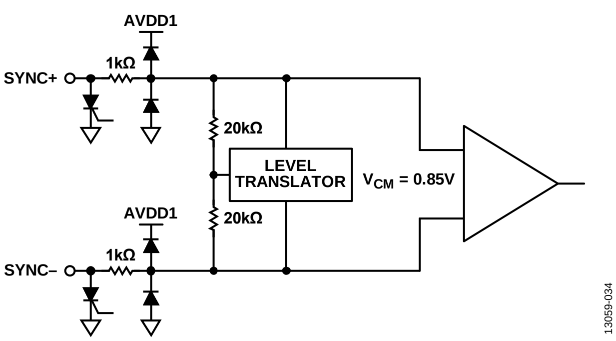


Figure 35. SYNC± Inputs

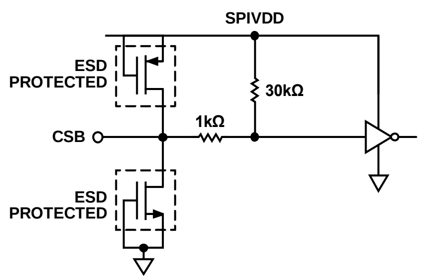


Figure 38. CSB Input

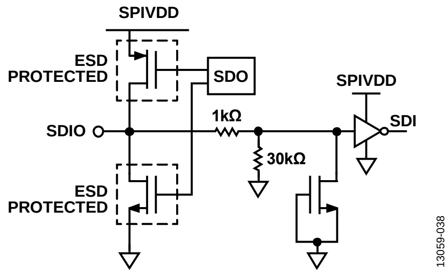


Figure 39. SDIO

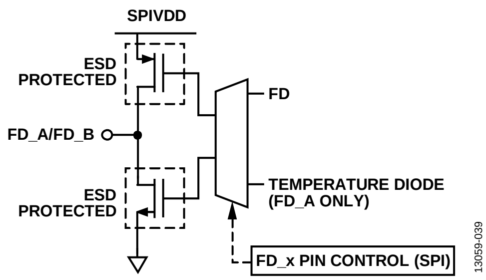


Figure 40. FD_A/FD_B Outputs

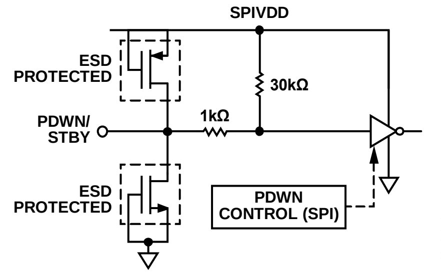


Figure 41. PDWN/STBY Input

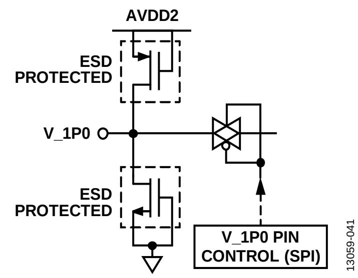


Figure 42. V_1P0 Input/Output

THEORY OF OPERATION

The AD6679 has two analog input channels and 14 LVDS output lane pairs. The AD6679 is designed to sample wide bandwidth analog signals of up to 2 GHz. The AD6679 is optimized for wide input bandwidth, high sampling rates, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD6679 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect bits of the ADC output data stream, which are enabled and programmed via Register 0x245 through Register 0x24C. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly reduce the system gain to avoid an overrange condition at the ADC input.

The LVDS outputs can be configured depending on the decimation ratio. Multiple device synchronization is supported through the SYNC± input pins.

ADC ARCHITECTURE

The architecture consists of an input buffered pipelined ADC. The input buffer provides a termination impedance to the analog input signal. This termination impedance can be changed using the SPI to meet the termination needs of the driver/amplifier. The default termination value is set to 400 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 33. The input buffer is optimized for high linearity, low noise, and low power.

The input buffer provides a linear high input impedance (for ease of drive) and reduces the kickback from the ADC. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6679 is a differential buffer. The internal common-mode voltage of the buffer is 2.05 V. The clock signal alternately switches the input circuit between sample mode and hold mode. When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, can help reduce the peak transient current inserted from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each section of the input to reduce high differential capacitance at the analog inputs and, thus, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This ultimately creates a low-pass filter (LPF) at the input, which limits unwanted broadband noise. For more information, refer to the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) at www.analog.com. In general, the precise values depend on the application.

For best dynamic performance, match the source impedances driving VIN+x and VIN−x such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD6679, the available span is programmable through the SPI port from 1.46 V p-p to 2.06 V p-p differential with 2.06 V p-p differential being the default.

Differential Input Configurations

There are several ways to drive the AD6679, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications in which SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 43 and Figure 44) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD6679.

For low to midrange frequencies, it is recommended to use a double balun or double transformer network (see Figure 43) for optimum performance from the AD6679. For higher frequencies in the second or third Nyquist zone, it is better to remove some of the front-end passive components to ensure wideband operation (see Figure 44).

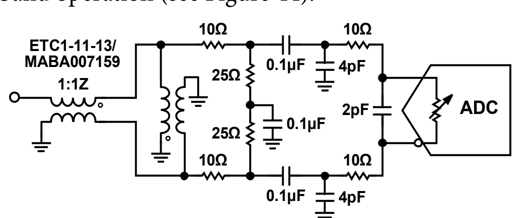


Figure 43. Differential Transformer Coupled Configuration for First and Second Nyquist Frequencies

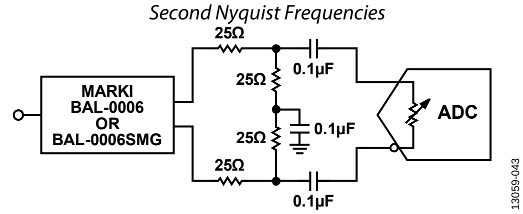


Figure 44. Differential Transformer Coupled Configuration for Second and Third Nyquist Frequencies

Input Common Mode

The analog inputs of the AD6679 are internally biased to the common mode, as shown in Figure 45. The common-mode buffer has a limited range in that the performance suffers greatly if the common-mode voltage drops by more than 100 mV. Therefore, in dc-coupled applications, set the common-mode voltage to 2.05 V ± 100 mV to ensure proper ADC operation.

Analog Input Controls and SFDR Optimization

The AD6679 offers flexible controls for the analog inputs such as input termination, buffer current, and input full-scale adjustment. All of the available controls are shown in Figure 45.

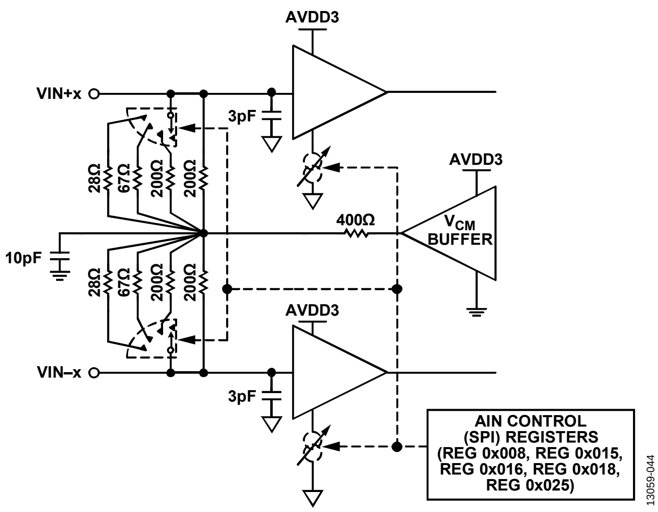


Figure 45. Analog Input Controls

Use Register 0x018, Register 0x019, Register 0x01A, Register 0x11A, Register 0x934, and Register 0x935 to adjust the buffer behavior on each channel to optimize the SFDR over various input frequencies and bandwidths of interest.

Input Buffer Control Registers (Register 0x018, Register 0x019, Register 0x01A, Register 0x11A, Register 0x934, Register 0x935)

The input buffer has many registers that set the bias currents and other settings for operation at different frequencies. These bias currents and settings can be changed to suit the input frequency range of operation. Register 0x018 controls the buffer bias current to reduce the effects of charge kickback from the ADC core. This setting can be scaled from a low setting of 1.0× to a high setting of 8.5×. The default setting in Register 0x018 is 2.0×. These settings are sufficient for operation in the first Nyquist zone. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 46. For a complete list of buffer current settings, see Table 41.

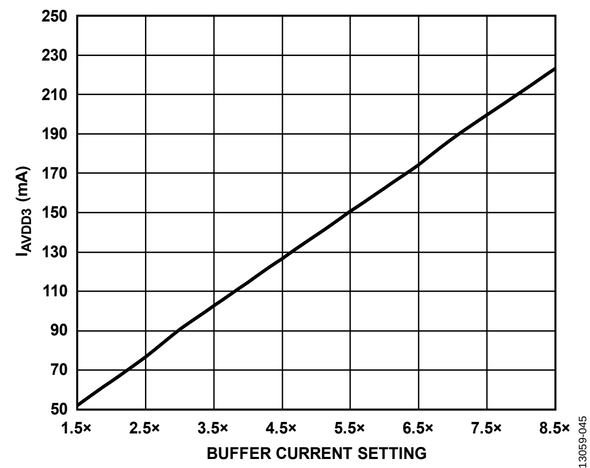


Figure 46. Typical I_{AVDD3} vs. Buffer Current Setting in Register 0x018

Register 0x019, Register 0x01A, Register 0x11A, and Register 0x935 offer secondary bias controls for the input buffer for frequencies >500 MHz. Use Register 0x934 to reduce input capacitance to achieve wider signal bandwidth but doing so may result in slightly lower linearity and noise performance. These register settings do not affect the AVDD3 power as much as Register 0x018 does. For frequencies <500 MHz, it is recommended to use the default settings for these registers. Table 11 shows the recommended values for the buffer current control registers for various speed grades.

Register 0x11A can be used when sampling in higher Nyquist zones (>1000 MHz) but is not necessary. Using Register 0x11A can help the ADC sampling network to optimize the sampling and settling times internal to the ADC for high frequency operation. For frequencies greater than 500 MHz, it is recommended to operate the ADC core at a 1.46 V full-scale setting. This setting offers better SFDR without any significant decrease in SNR.

Figure 47, Figure 48, and Figure 49 show the SFDR vs. input frequency for various buffer settings for the AD6679. The recommended settings shown in Table 11 were used to collect the data while changing the contents of register 0x018 only.

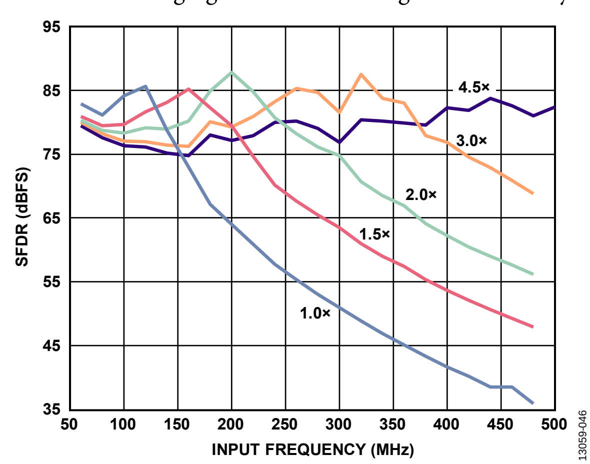


Figure 47. Buffer Current Sweeps (SFDR vs. Input Frequency and I_{BUFF}); 10 MHz < f_{IN} < 500 MHz; Front-End Network Shown in Figure 43

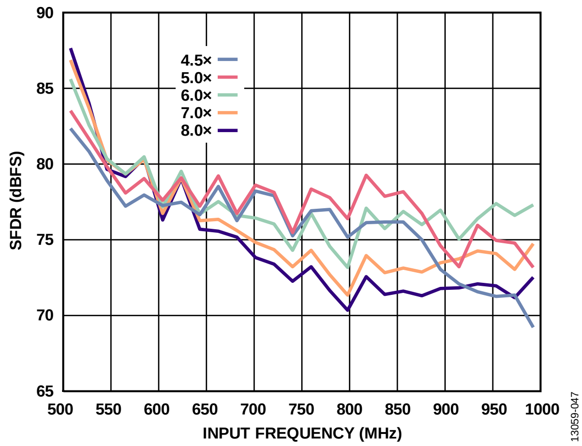


Figure 48. Buffer Current Sweeps (SFDR vs. Input Frequency and I_{BUFF}); 500 MHz < f_{IN} < 1000 MHz; Front-End Network Shown in Figure 44

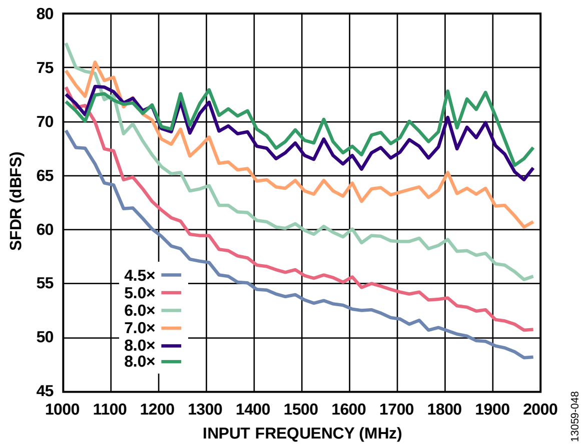


Figure 49. Buffer Current Sweeps (SFDR vs. Input Frequency and I_{BUFF}); 1 GHz < f_{IN} < 2 GHz; Front-End Network Shown in Figure 44

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD6679 is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD6679. This internal 1.0 V reference sets the full-scale input range of the ADC. The full-scale input range can be adjusted via Register 0x025. For more information on adjusting the input swing, see Table 41. Figure 50 shows the block diagram of the internal 1.0 V reference controls.

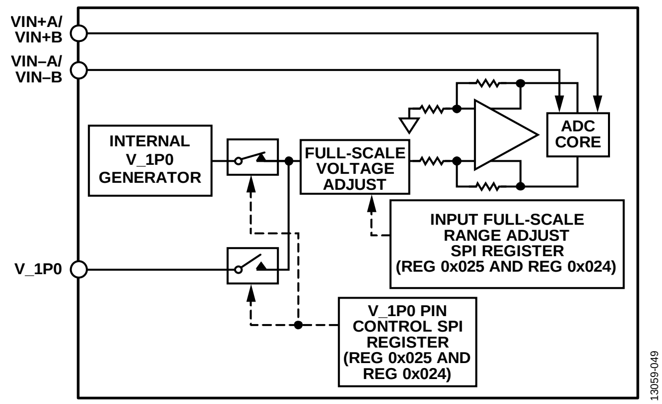


Figure 50. Internal Reference Configuration and Controls

Table 11. SFDR Optimization for Input Frequencies

Frequency	Buffer Control 1 (Register 0x018)	Buffer Control 2 (Register 0x019)	Buffer Control 3 (Register 0x01A)	Buffer Control 4 (Register 0x11A)	Buffer Control 5 (Register 0x935)	Input Full-Scale Range (Register 0x025)	Input Full-Scale Control (Register 0x030)	Input Capacitance (Register 0x934)	Input Termination (Register 0x016)[1]
DC to 250 MHz	0x20 (2.0×)	0x60 (Setting 3)	0x0A (Setting 3)	0x00 (off)	0x04 (on)	0x0C (2.06 V p-p)	0x04	0x1F	0x0C/0x1C/0x6C
250 MHz to 500 MHz	0x70 (4.5×)	0x60 (Setting 3)	0x0A (Setting 3)	0x00 (off)	0x04 (on)	0x0C (2.06 V p-p)	0x04	0x1F	0x0C/0x1C/0x6C
500 MHz to 1 GHz	0x80 (5.0×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x08 (1.46 V p-p)	0x18	0x1F/0x00[2]	0x0C/0x1C/0x6C
1 GHz to 2 GHz	0xF0 (8.5×)	0x40 (Setting 1)	0x08 (Setting 1)	0x00 (off)	0x00 (off)	0x08 (1.46 V p-p)	0x18	0x1F/0x00[2]	0x0C/0x1C/0x6C

[1] The input termination can be changed to accommodate the application with little or no impact to ac performance.
[2] The input capacitance can be set to 1.5 pF to achieve wider input bandwidth but doing so results in slightly lower ac performance.

Register 0x024 enables the user to use either this internal 1.0 V reference, or to provide an external 1.0 V reference. When using an external voltage reference, provide a 1.0 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD6679, refer to the Memory Map Register Table section.

The use of an external reference may be necessary, in some applications, to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 51 shows the typical drift characteristics of the internal 1.0 V reference.

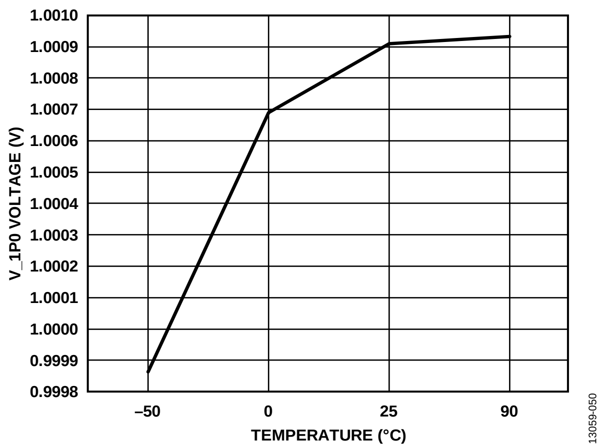


Figure 51. Typical V_1P0 Drift

The external reference must be a stable 1.0 V reference. The ADR130 is a good option for providing the 1.0 V reference. Figure 55 shows how the ADR130 can be used to provide the external 1.0 V reference to the AD6679. The gray areas show unused blocks within the AD6679 while the ADR130 provides the external reference.

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD6679 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 52 shows one preferred method for clocking the AD6679. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

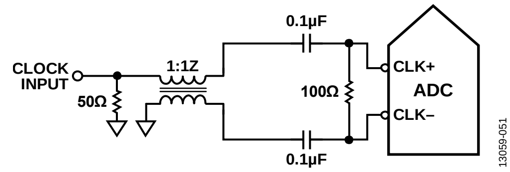


Figure 52. Transformer Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins as shown in Figure 53 and Figure 54.

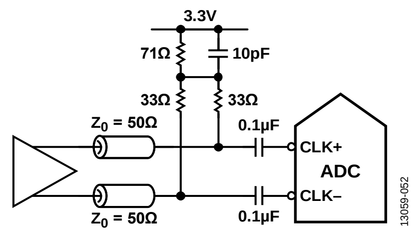


Figure 53. Differential CML Sample Clock

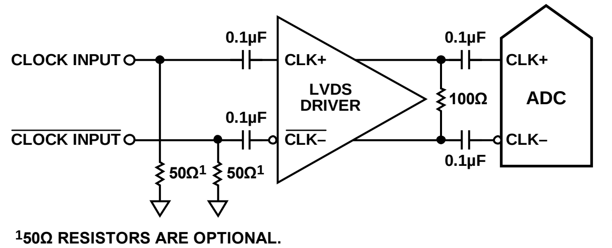


Figure 54. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock can be supplied to the AD6679. For example, the AD6679 can be clocked at 2 GHz with the internal clock divider set to 4. This ensures a 50% duty cycle, high slew rate internal clock for the ADC. See the Memory Map section for more details on using this feature.

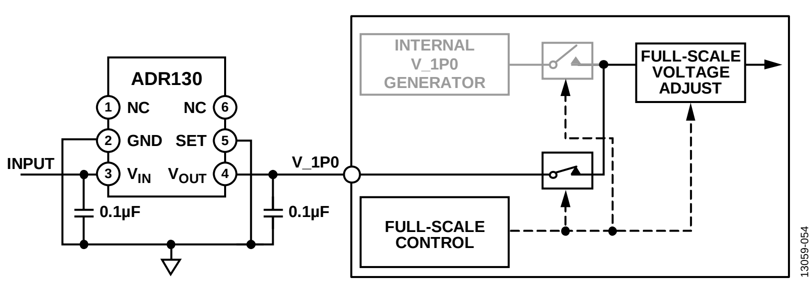


Figure 55. External Reference Using the ADR130

Input Clock Divider

The AD6679 contains an input clock divider with the ability to divide the Nyquist input clock by 1, 2, 4, or 8. The divide ratio can be selected using Register 0x10B. This is shown in Figure 56. The maximum frequency at the output of the divider is 500 MHz.

The maximum frequency at the CLK± inputs is 4 GHz. This is the limit of the divider. In applications where the clock input is a multiple of the sample clock, take care to program the appropriate divider ratio into the clock divider before applying the clock signal. This ensures that the current transients during device startup are controlled.

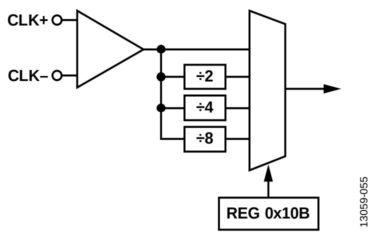


Figure 56. Clock Divider Circuit

The AD6679 clock divider can be synchronized using the external SYNC± input. A valid SYNC± input causes the clock divider to reset to a programmable state. This feature is enabled by setting Bit 7 of Register 0x10D. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling.

After programming the desired clock divider settings, changing the input clock frequency or glitching the input clock a datapath soft reset is recommended by writing 0x02 to Register 0x001. This reset function restarts all the datapath and clock generation circuitry in the device. The reset occurs on the first clock cycle after the register is programmed, and the device requires 5 ms to recover. This reset does not affect the contents of the memory map registers.

Input Clock Divider ½ Period Delay Adjustment

The input clock divider inside the AD6679 provides phase delay in increments of ½ the input clock cycle. Program Register 0x10C to enable this delay independently for each channel.

Clock Fine Delay Adjustment

To adjust the AD6679 sampling edge instant, write to Register 0x117 and Register 0x118. Setting Bit 0 of Register 0x117 enables the fine delay feature, and Register 0x118, Bits[7:0], set the value of the delay. This value can be programmed individually for each channel. The clock delay can be adjusted from −151.7 ps to +150 ps in ~1.7 ps increments. The clock delay adjustment takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjustment in Register 0x117 causes a datapath reset.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) is calculated by

$$SNR = 20 \times \log10(2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 57).

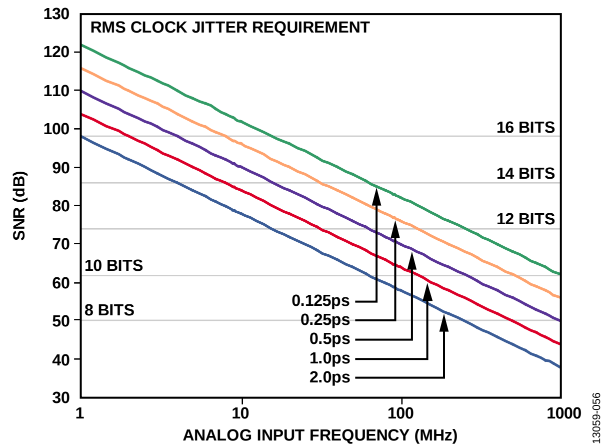


Figure 57. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal when aperture jitter may affect the dynamic range of the AD6679. Separate the power supplies for the clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime it using the original clock at the last step. See the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

Figure 58 shows the estimated SNR of the AD6679 across input frequency for different clock induced jitter values. Estimate the SNR by using the following equation:

$$SNR(\text{dBFS}) = 10\log\left(10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{JITTER}}{10}\right)}\right)$$

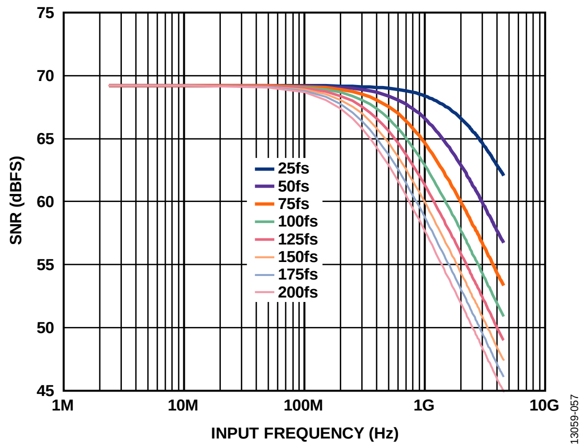


Figure 58. Estimated SNR Degradation for the AD6679 vs. Input Frequency and Jitter

POWER-DOWN/STANDBY MODE

The AD6679 has a PDWN/STBY pin that configures the device in power-down or standby mode. The default operation is the power-down function. The PDWN/STBY pin is a logic high pin. The power-down option can also be set via Register 0x03F and Register 0x040.

TEMPERATURE DIODE

The AD6679 contains a diode-based temperature sensor for measuring the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

The temperature diode voltage can be output to the FD_A pin using the SPI. Use Register 0x028, Bit 0, to enable or disable the diode. Register 0x028 is a local register. Channel A must be selected in the device index register (Register 0x008) to enable the temperature diode readout. Configure the FD_A pin to output the diode voltage by programming Register 0x040, Bits[2:0]. See Table 41 for more information.

The voltage response of the temperature diode (with SPIVDD = 1.8 V) is shown in Figure 59.

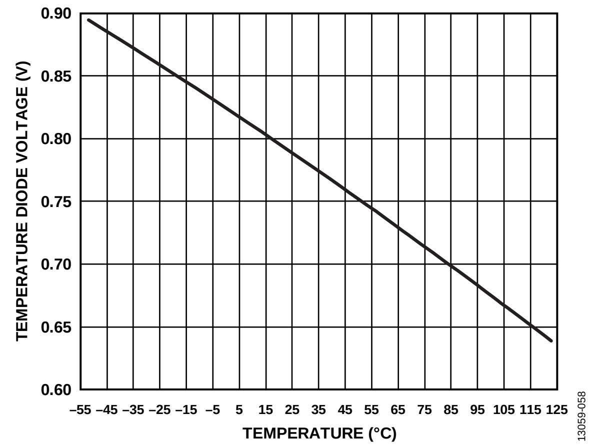


Figure 59. Temperature Diode Voltage vs. Temperature

VIRTUAL CONVERTER MAPPING

The AD6679 contains a configurable signal path that allows different features to be enabled for different applications. These features are controlled through the chip application mode register (0x200). The chip operating mode is controlled by Bits[3:0] and the Chip Q ignore is controlled by Bit 5.

The AD6679 contains the following digital features:

- Two analog-to-digital converter (ADC) cores
- Four digital downconverter (DDC) channels
- Two noise shaped requantizer (NSR) blocks with optional decimate by two blocks
- Two variable dynamic range (VDR) blocks

After the chip application mode has been selected, the output decimation ratio is set using the chip decimation ratio in Register 0x201, Bits[2:0]. The output sample rate is the ADC sample rate divided by the chip decimation ratio.

To support the different application layer modes, the AD6679 treats each sample stream (real or I or Q) as originating from separate virtual converters. Table 12 shows the number of virtual converters required for each chip mode.

The AD6679 supports up to four digital DDC blocks. Each DDC block outputs either two sample streams (I/Q) for the complex data components (real + imaginary) or one sample stream for real (I) data. The AD6679 can be configured to use up to eight virtual converters depending on the DDC configuration. Figure 60 shows the virtual converters and their relationship to DDC outputs when complex outputs are used.

Table 12 shows the virtual converter mapping for each chip operating mode when channel swapping is disabled.

Table 12. Virtual Converter Mapping

No. of Virtual Converters Supported	Chip Operating Mode (Register 0x200[3:0])	Chip Q Ignore (Register 0x200[5])	Virtual Converter Mapping[1]							
			0	1	2	3	4	5	6	7
1	One DDC mode (0x1)	Real (I only) (0x1)	DDC 0 I samples	N/A	N/A	N/A	N/A	N/A	N/A	N/A
2	One DDC mode (0x1)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	N/A	N/A	N/A	N/A	N/A	N/A
2	Two DDC mode (0x2)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	N/A	N/A	N/A	N/A	N/A	N/A
4	Two DDC mode (0x2)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples	N/A	N/A	N/A	N/A
4	Four DDC mode (0x3)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	DDC 2 I samples	DDC 3 I samples	N/A	N/A	N/A	N/A
8	Four DDC mode (0x3)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples	DDC 2 I samples	DDC 2 Q samples	DDC 3 I samples	DDC 3 Q samples
1 to 2	NSR mode (0x7)	Real or complex (0x0)	ADC A samples	ADC B samples	N/A	N/A	N/A	N/A	N/A	N/A
1 to 2	VDR mode (0x8)	Real or complex (0x0)	ADC A samples	ADC B samples	N/A	N/A	N/A	N/A	N/A	N/A

[1] N/A means not applicable.

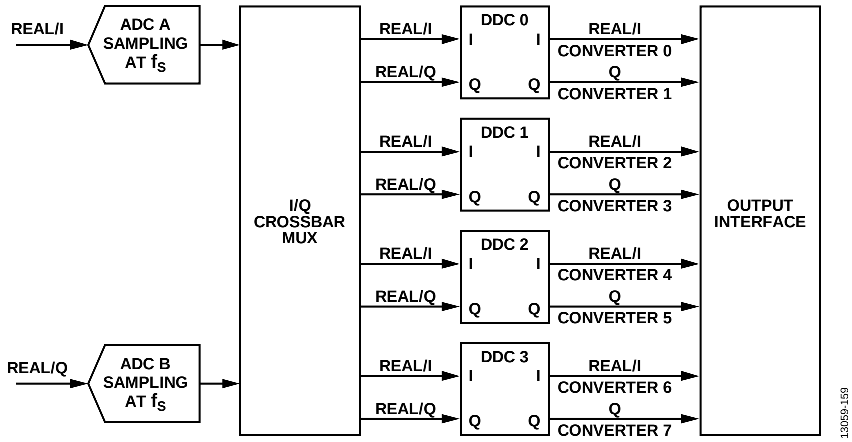


Figure 60. DDCs and Virtual Converter Mapping

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit, available via the STATUS±/OVR± pins, provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD6679 contains fast detect circuitry for individual channels to monitor the threshold and assert the FD_A and FD_B pins.

ADC OVERRANGE (OR)

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be output via the STATUS± pins. The latency of this overrange indicator matches the sample latency.

The AD6679 constantly monitors the analog input level and records any overrange condition in any of the eight virtual converters. For more information on the virtual converters, refer to Figure 63. The overrange status of each virtual converter is registered as a sticky bit (that is, it is set until cleared) in Register 0x563. The contents of Register 0x563 can be cleared using Register 0x562 by toggling the bits corresponding to the virtual converter to set and reset the position.

FAST THRESHOLD DETECTION (FD_A AND FD_B)

The fast detect (FD) bit (enabled in the control bits via Register 0x559) is set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is cleared only when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 61.

The FD_x indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located in Register 0x247 and Register 0x248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28 clock cycles. The approximate upper threshold magnitude is defined by

$$\textit{Upper Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13})$$

The FD_x indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located in Register 0x249 and Register 0x24A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\textit{Lower Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0x0FFF to Register 0x247 and Register 0x248; and to set a lower threshold of −10 dBFS, write 0x0A1D to Register 0x249 and Register 0x24A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located in Register 0x24B and Register 0x24C. See the Memory Map section (Register 0x245 to Register 0x24C in Table 41) for more details.

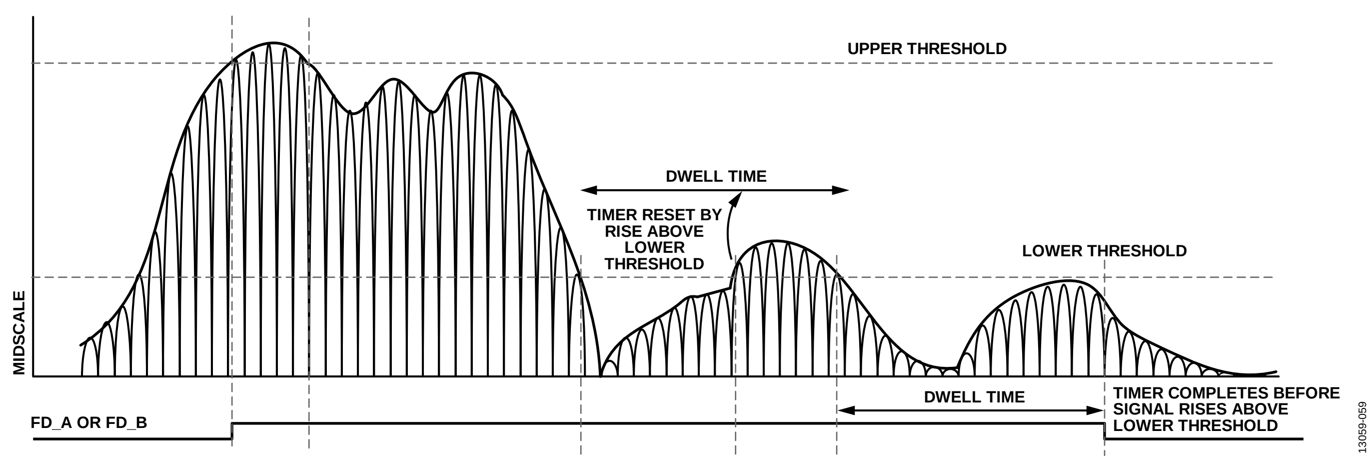


Figure 61. Threshold Settings for FD_A and FD_B Signals

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained by reading back the internal values from the SPI port. A global, 24-bit programmable period controls the duration of the measurement. Figure 62 shows the simplified block diagram of the signal monitor block.

The peak detector captures the largest signal within the observation period. This period observes only the magnitude of the signal. The resolution of the peak detector is a 13-bit value and the observation period is 24 bits and represents converter output samples. The peak magnitude is derived by using the following equation:

$$\textit{Peak Magnitude}\ (\text{dBFS}) = 20 \log(\textit{Peak Detector Value}/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period that is determined by the signal monitor period registers (SMPRs). Only even values of the SMPR are supported. The peak detector function is enabled by setting Bit 1 of Register 0x270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer that decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the magnitude of the first input sample is updated in the internal magnitude storage register, and the comparison and update procedure, as explained previously, continues.

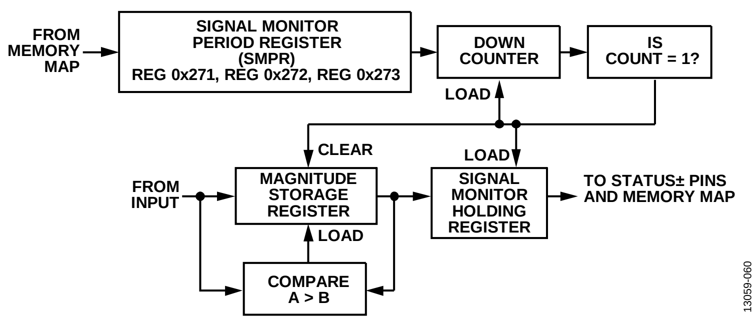


Figure 62. Signal Monitor Block

DIGITAL DOWNCONVERTER (DDC)

The AD6679 includes four digital downconverters (DDCs) that provide filtering and reduce the output data rate. This digital processing section includes an NCO, up to four half-band decimating filter, a finite impulse response (FIR) filter, a gain stage, and a complex to real conversion stage. Each of these processing blocks has control lines that allow it to be independently enabled and disabled to provide the desired processing function. The DDC can be configured to output either real data or complex output data.

DDC I/Q INPUT SELECTION

The AD6679 has two ADC channels and four DDC channels. Each DDC channel has two input ports that can be paired to support both real and complex inputs through the I/Q crossbar mux. For real signals, both DDC input ports must select the same ADC channel (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel A). For complex signals, each DDC input port must select different ADC channels (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel B).

The inputs to each DDC are controlled by the DDC input selection registers (Register 0x311, Register 0x331, Register 0x351, and Register 0x371). See Table 41 for information on how to configure the DDCs.

DDC I/Q OUTPUT SELECTION

Each DDC channel has two output ports that can be paired to support both real and complex outputs. For real output signals, only the DDC Output Port I is used (the DDC Output Port Q is invalid). For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

The I/Q outputs to each DDC channel are controlled by the DDC complex to real enable bit, Bit 3, in the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

The Chip Q ignore bit in the chip mode register (Register 0x200, Bit 5) controls the chip output muxing of all the DDC channels. When all DDC channels use real outputs, set this bit high to ignore all DDC Q output ports. When any of the DDC channels are set to use complex I/Q outputs, the user must clear this bit to use both DDC Output Port I and DDC Output Port Q. For more information, see Figure 71.

DDC GENERAL DESCRIPTION

The four DDC blocks extract a portion of the full digital spectrum captured by the ADC(s). They are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains the following signal processing stages:

- Frequency translation stage (optional)
- Filtering stage
- Gain stage (optional)
- Complex to real conversion stage (optional)

Frequency Translation Stage (Optional)

This stage consists of a 12-bit complex NCO and quadrature mixers that can be used for frequency translation of both real and complex input signals. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage

After shifting down to baseband, this stage decimates the frequency spectrum using a chain of up to four half-band low-pass filters for rate conversion. The decimation process lowers the output data rate, which, in turn, reduces the output interface rate.

Gain Stage (Optional)

Due to losses associated with mixing a real input signal down to baseband, this stage compensates by adding an additional 0 dB or 6 dB of gain.

Complex to Real Conversion Stage (Optional)

When real outputs are necessary, this stage converts the complex outputs back to real outputs by performing an $f_S/4$ mixing operation together with a filter to remove the complex component of the signal.

Figure 63 shows the detailed block diagram of the DDCs implemented in the AD6679.

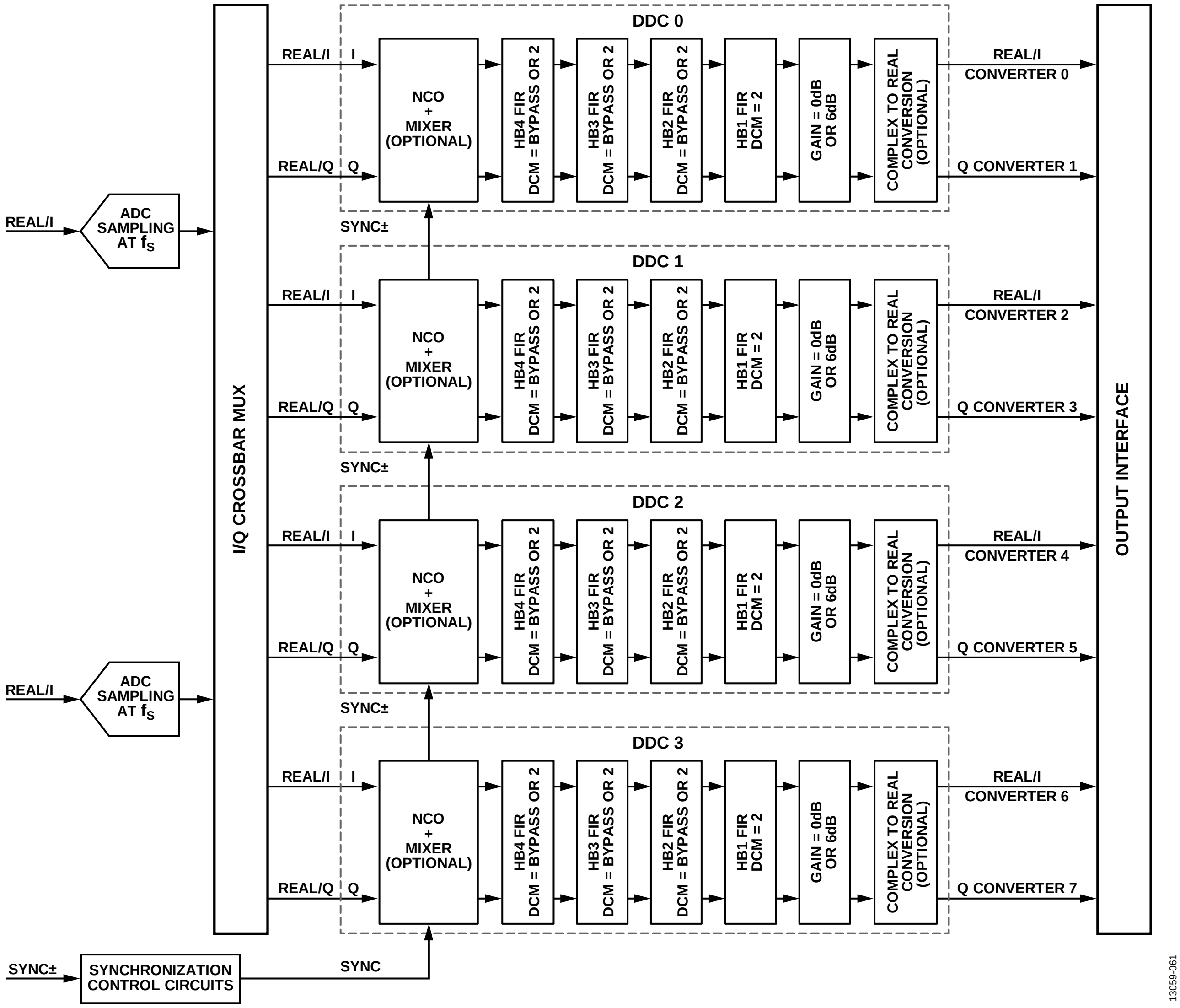


Figure 63. DDC Detailed Block Diagram

Figure 64 shows an example usage of one of the four DDC blocks with a real input signal and four half-band filters (HB4 + HB3 + HB2 + HB1). It shows both complex (decimate by 16) and real (decimate by 8) output options.

When DDCs have different decimation ratios, the chip decimation ratio (Register 0x201) must be set to the lowest decimation ratio of all the DDC blocks. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Whenever the NCO frequency is set or changed, the DDC soft reset must be issued. If the DDC soft reset is not issued, the output may potentially show amplitude variations.

Table 13 through Table 17 show the DDC samples when the chip decimation ratio is set to 1, 2, 4, 8, or 16, respectively. When DDCs have different decimation ratios, the chip decimation ratio must be set to the lowest decimation ratio of all the DDC channels. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate.

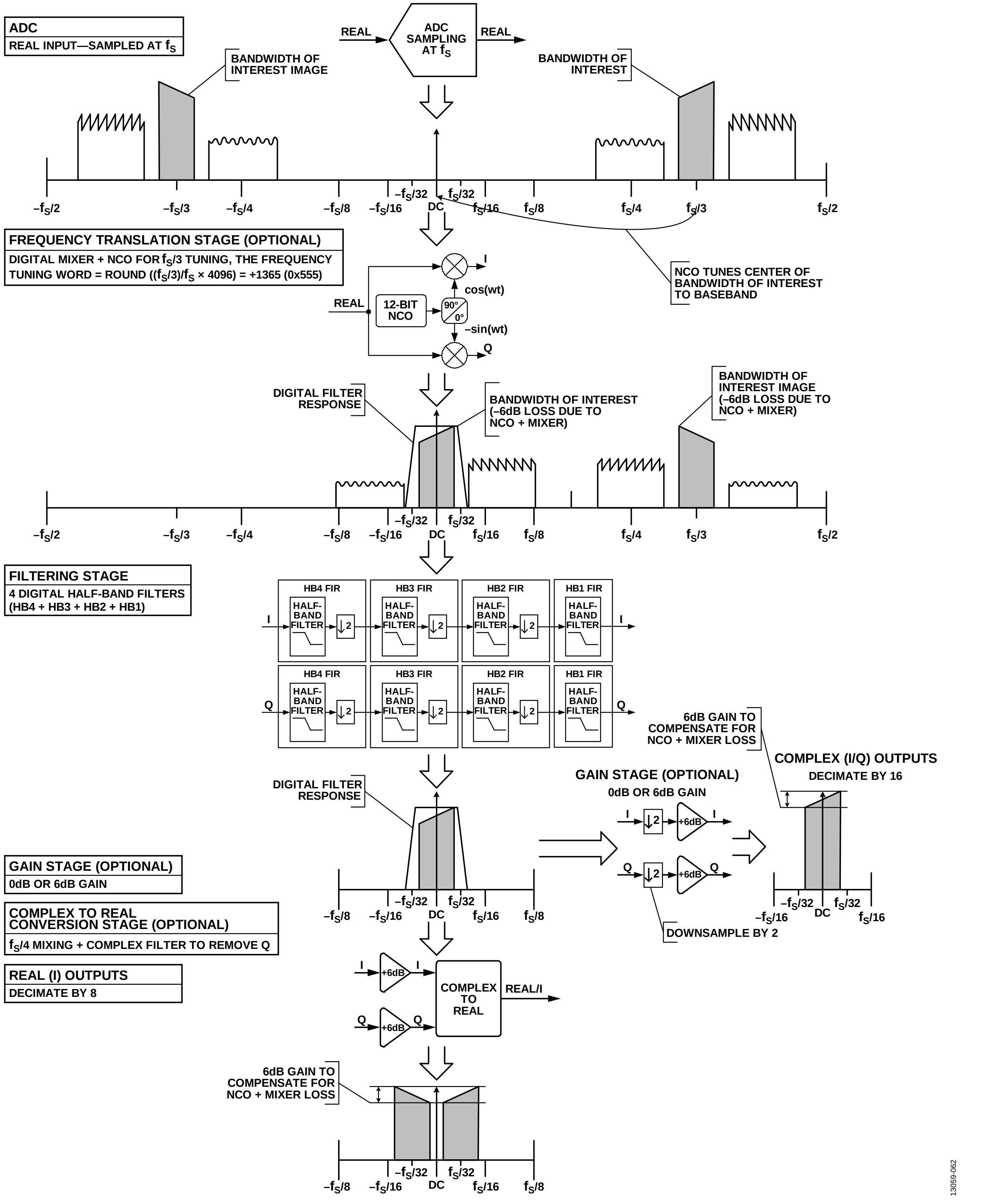


Figure 64. DDC Theory of Operation Example (Real Input, Decimate by 16)

Table 13. DDC Samples When Chip Decimation Ratio = 1

Real (I) Output (Complex to Real Enabled)				Complex (I/Q) Outputs (Complex to Real Disabled)			
HB1 FIR (DCM[1] = 1)	HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N	N	N	N	N	N
N + 3	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 4	N + 2	N	N	N + 2	N	N	N
N + 5	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 6	N + 2	N	N	N + 2	N	N	N
N + 7	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 8	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 9	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 10	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 11	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 12	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 13	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 14	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 15	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 16	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 17	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 18	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 19	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 20	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 21	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 22	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 23	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 24	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 25	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 26	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 27	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 28	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 29	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1
N + 30	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 31	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 14. DDC Samples When Chip Decimation Ratio = 2

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N	N + 2	N	N	N
N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 4	N + 2	N	N + 4	N + 2	N	N
N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 6	N + 2	N	N + 6	N + 2	N	N
N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM[1] = 2)	**HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)**	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB1 FIR (DCM[1] = 2)**	**HB2 FIR + HB1 FIR (DCM[1] = 4)**	**HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)**
N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 15. DDC Samples When Chip Decimation Ratio = 4

Real (I) Output (Complex to Real Enabled)		Complex (I/Q) Outputs (Complex to Real Disabled)		
HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB2 FIR + HB1 FIR (DCM[1] = 4)**	**HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)**
N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N + 2	N	N
N + 3	N + 1	N + 3	N + 1	N + 1
N + 4	N + 2	N + 4	N + 2	N
N + 5	N + 3	N + 5	N + 3	N + 1
N + 6	N + 2	N + 6	N + 2	N
N + 7	N + 3	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 16. DDC Samples When Chip Decimation Ratio = 8

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)	
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	**HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)**	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)**
N	N	N
N + 1	N + 1	N + 1
N + 2	N + 2	N
N + 3	N + 3	N + 1
N + 4	N + 4	N + 2
N + 5	N + 5	N + 3
N + 6	N + 6	N + 2
N + 7	N + 7	N + 3

[1] DCM means decimation.

Table 17. DDC Samples When Chip Decimation Ratio = 16

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)	**HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)**
Not applicable	N
Not applicable	N + 1
Not applicable	N + 2
Not applicable	N + 3

[1] DCM means decimation.

For example, if the chip decimation ratio is set to decimate by 4, DDC 0 is set to use HB2 + HB1 filters (complex outputs, decimate by 4) and DDC 1 is set to use HB4 + HB3 + HB2 + HB1 filters (real outputs, decimate by 8). DDC 1 repeats its output data two times for every one DDC 0 output. The resulting output samples are shown in Table 18.

Table 18. DDC Output Samples When Chip DCM[1] = 4, DDC 0 DCM[1] = 4 (Complex), and DDC 1 DCM[1] = 8 (Real)

	DDC 0		DDC 1	
DDC Input Samples	**Output Port I**	**Output Port Q**	**Output Port I**	**Output Port Q**
N	I0 (N)	Q0 (N)	I1 (N)	Not applicable
N + 1				
N + 2				
N + 3				
N + 4	I0 (N + 1)	Q0 (N + 1)		
N + 5				
N + 6				
N + 7				
N + 8	I0 (N + 2)	Q0 (N + 2)	I1 (N + 1)	Not applicable
N + 9				
N + 10				
N + 11				
N + 12	I0 (N + 3)	Q0 (N + 3)		
N + 13				
N + 14				
N + 15				

[1] DCM means decimation.

FREQUENCY TRANSLATION

GENERAL DESCRIPTION

Frequency translation is accomplished by using a 12-bit complex NCO with a digital quadrature mixer. This stage translates either a real or complex input signal from an IF to a baseband complex digital output (carrier frequency = 0 Hz).

The frequency translation stage of each DDC can be controlled individually and supports four different IF modes using Bits[5:4] of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370). These IF modes are

- Variable IF mode
- 0 Hz IF, or zero IF (ZIF), mode
- $f_S/4$ Hz IF mode
- Test mode

Variable IF Mode

The NCO and the mixers are enabled. The NCO output frequency can be used to digitally tune the IF frequency.

0 Hz IF (ZIF) Mode

The mixers are bypassed, and the NCO is disabled.

$f_S/4$ Hz IF Mode

The mixers and the NCO are enabled in a special downmixing by $f_S/4$ mode to save power.

Test Mode

The input samples are forced to 0.999 to positive full scale. The NCO is enabled. This test mode allows the NCOs to drive the decimation filters directly.

Figure 65 and Figure 66 show examples of the frequency translation stage for both real and complex inputs.

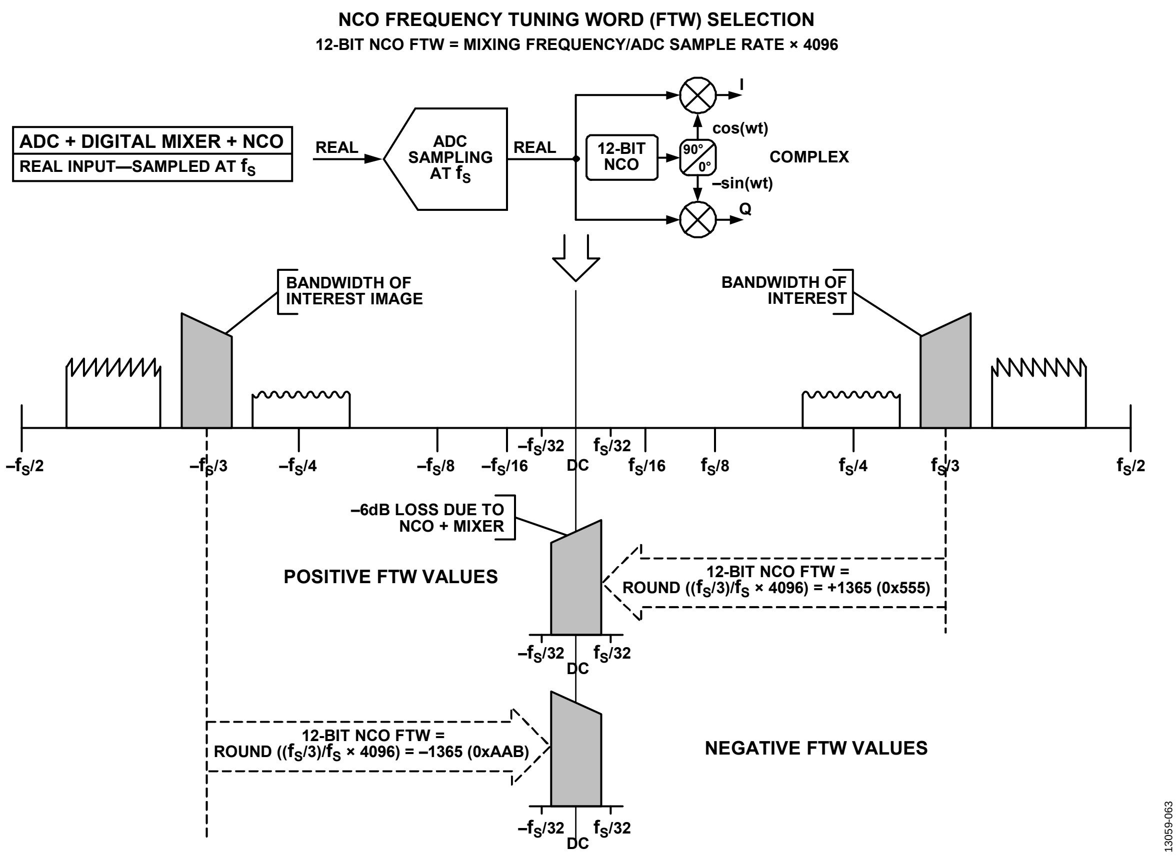


Figure 65. DDC NCO Frequency Tuning Word Selection—Real Inputs

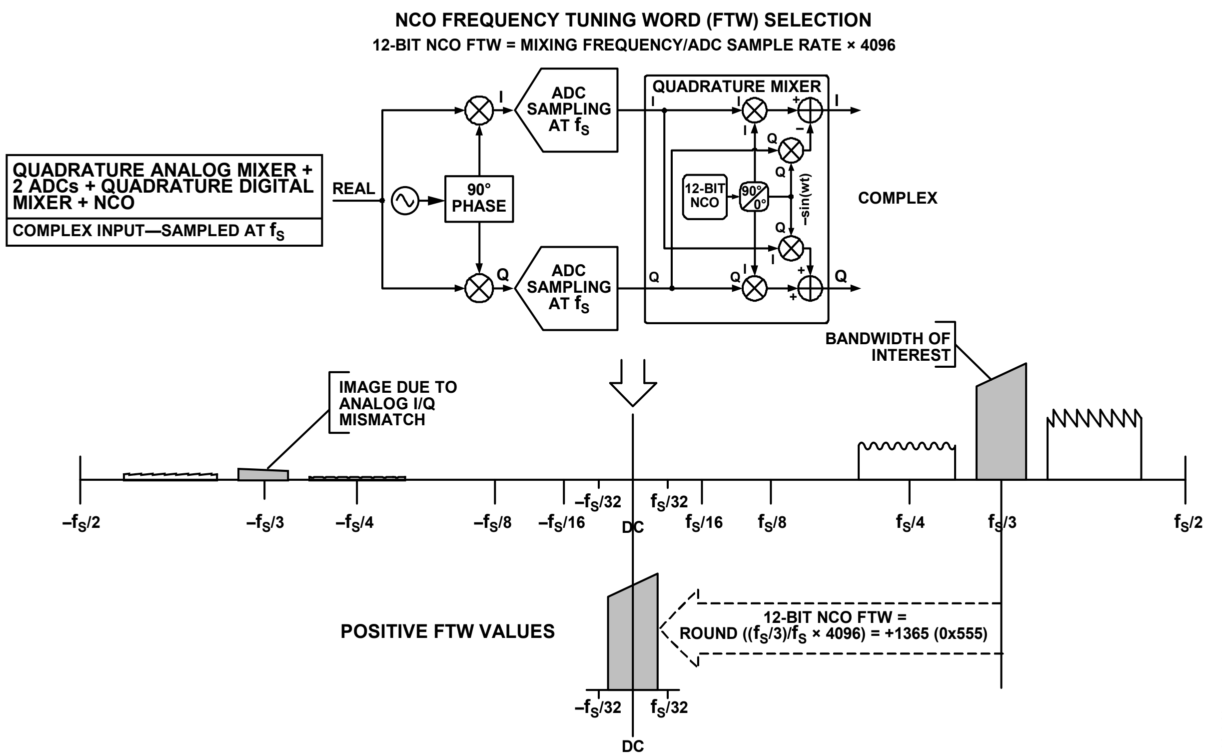


Figure 66. DDC NCO Frequency Tuning Word Selection—Complex Inputs

DDC NCO PLUS MIXER LOSS AND SFDR

When mixing a real input signal down to baseband, 6 dB of loss is introduced in the signal due to filtering of the negative image. The NCO introduces an additional 0.05 dB of loss. The total loss of a real input signal mixed down to baseband is 6.05 dB. For this reason, it is recommended to compensate for this loss by enabling the 6 dB of gain in the gain stage of the DDC to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the maximum value each I/Q sample can reach is 1.414 × full scale after it passes through the complex mixer. To avoid an overrange of the I/Q samples and to keep the data bit-widths aligned with real mixing, 3.06 dB of loss is introduced in the mixer for complex signals. The NCO introduces an additional 0.05 dB of loss. The total loss of a complex input signal mixed down to baseband is −3.11 dB.

The worst case spurious signal from the NCO is greater than 102 dBc SFDR for all output frequencies.

NUMERICALLY CONTROLLED OSCILLATOR

The AD6679 has a 12-bit NCO for each DDC that enables the frequency translation process. The NCO allows the input spectrum to be tuned to dc, where it can be effectively filtered by the subsequent filter blocks to prevent aliasing. The NCO can be set up by providing a frequency tuning word (FTW) and a phase offset word (POW).

Setting Up the NCO FTW and POW

The NCO frequency value is given by the 12-bit, twos complement number entered in the NCO FTW. Frequencies between $-f_S/2$ and $+f_S/2$ ($f_S/2$ excluded) are represented using the following frequency words:

- 0x800 represents a frequency of $-f_S/2$.
- 0x000 represents dc (frequency is 0 Hz).
- 0x7FF represents a frequency of $+f_S/2 - f_S/2^{12}$.

Calculate the NCO frequency tuning word using the following equation:

$$NCO\_FTW = \text{round}\left(2^{12}\frac{\text{mod}(f_C, f_S)}{f_S}\right)$$

where:
NCO_FTW is a 12-bit, twos complement number representing the NCO FTW.
f_C is the desired carrier frequency in Hz.
f_S is the AD6679 sampling frequency (clock rate) in Hz.
mod( ) is a remainder function. For example, mod(110,100) = 10 and for negative numbers, mod(−32,10) = −2.
round( ) is a rounding function. For example, round(3.6) = 4 and for negative numbers, round(−3.4) = −3.

Note that this equation applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals).

For example, if the ADC sampling frequency (f_S) is 500 MSPS and the carrier frequency (f_C) is 140.312 MHz, then

$$NCO\_FTW = \text{round}\left(2^{12}\frac{\text{mod}(140.312,500)}{500}\right) = 1149 \text{ MHz}$$

This, in turn, converts to 0x47D in the 12-bit twos complement representation for NCO_FTW. Calculate the actual carrier frequency, f_{C_ACTUAL}, based on the following equation:

$$f_{C\_ACTUAL} = \frac{NCO\_FTW \times f_S}{2^{12}} = 140.26 \text{ MHz}$$

A 12-bit POW is available for each NCO to create a known phase relationship between multiple AD6679 chips or individual DDC channels inside one AD6679 chip.

The following procedure must be followed to update the FTW and/or POW registers to ensure proper operation of the NCO:

1. Write to the FTW registers for all the DDCs.
2. Write to the POW registers for all the DDCs.
3. Synchronize the NCOs either through the DDC NCO soft reset bit (Register 0x300, Bit 4), accessible through the SPI or through the assertion of the SYNC± pin.

It is important to note that the NCOs must be synchronized either through the SPI or through the SYNC± pin after all writes to the FTW or POW registers are complete. This synchronization is necessary to ensure the proper operation of the NCO.

NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW) that determines the instantaneous phase of the NCO. The initial reset value of each PAW is determined by the POW. The phase increment value of each PAW is determined by the FTW. See the Setting Up the NCO FTW and POW section for more information.

Use the following two methods to synchronize multiple PAWs within the chip:

- Using the SPI. Use the DDC NCO soft reset bit in the DDC synchronization control register (Register 0x300, Bit 4) to reset all the PAWs in the chip. This is accomplished by setting the DDC NCO soft reset bit high and then setting this bit low. Note that this method synchronizes DDC channels within the same AD6679 chip only.
- Using the SYNC± pins. When the SYNC± pins are enabled in the SYNC± control registers (Register 0x120 and Register 0x121) and the DDC synchronization is enabled in the DDC synchronization control register (Register 0x300, Bits[1:0]), any subsequent SYNC± event resets all the PAWs in the chip. Note that this method synchronizes DDC channels within the same AD6679 chip or DDC channels within separate AD6679 chips.

Mixer

The NCO is accompanied by a mixer. Its operation is similar to an analog quadrature mixer. It performs the downconversion of input signals (real or complex) by using the NCO frequency as a local oscillator. For real input signals, this mixer performs a real mixer operation (with two multipliers). For complex input signals, the mixer performs a complex mixer operation (with four multipliers and two adders). The mixer adjusts its operation based on the input signal (real or complex) provided to each individual channel. The selection of real or complex inputs can be controlled individually for each DDC block using Bit 7 of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

FIR FILTERS

OVERVIEW

There are four sets of decimate by 2, low-pass, half-band, FIR filters (labeled HB1 FIR, HB2 FIR, HB3 FIR, and HB4 FIR in Figure 63) following the frequency translation stage. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate, while providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

HB1 FIR is always enabled and cannot be bypassed. The HB2, HB3, and HB4 FIR filters are optional and can be bypassed for higher output sample rates.

Table 20 shows the different bandwidths selectable by including different half-band filters. In all cases, the DDC filtering stage on the AD6679 provides <−0.001 dB of pass-band ripple and >100 dB of stop band alias rejection.

Table 21 shows the amount of stop-band alias rejection for multiple pass-band ripple/cutoff points. The decimation ratio of the filtering stage of each DDC can be controlled individually through Bits[1:0] of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

HALF-BAND FILTERS

The AD6679 offers four half-band filters to enable digital signal processing of the ADC converted data. These half-band filters are bypassable and can be individually selected.

HB4 Filter

The first decimate by 2, half-band, low-pass, FIR filter (HB4) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB4 filter is used only when complex outputs (decimate by 16) or real outputs (decimate by 8) are enabled; otherwise, it is bypassed. Table 19 and Figure 67 show the coefficients and response of the HB4 filter.

Table 19. HB4 Filter Coefficients

HB4 Coefficient Number	Normalized Coefficient	Decimal Coefficient (15-Bit)
C1, C11	0.006042	99
C2, C10	0	0
C3, C9	−0.049316	−808
C4, C8	0	0
C5, C7	0.293273	4805
C6	0.500000	8192

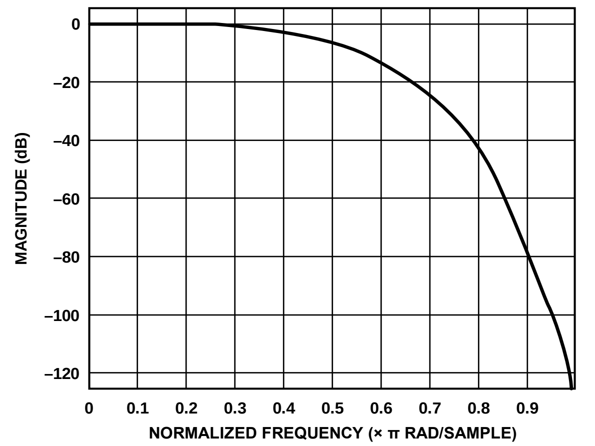


Figure 67. HB4 Filter Response

Table 20. DDC Filter Characteristics

ADC Sample Rate (MSPS)	Half Band Filter Selection	Real Output: Decimation Ratio	Real Output: Output Sample Rate (MSPS)	Complex (I/Q) Output: Decimation Ratio	Complex (I/Q) Output: Output Sample Rate (MSPS)	Alias Protected Bandwidth (MHz)	Ideal SNR Improvement[1] (dB)	Pass-Band Ripple (dB)	Alias Rejection (dB)
500	HB1	1	500	2	250 (I) + 250 (Q)	192.5	1	<−0.001	>100
	HB1 + HB2	2	250	4	125 (I) + 125 (Q)	96.3	4		
	HB1 + HB2 + HB3	4	125	8	62.5 (I) + 62.5 (Q)	48.1	7		
	HB1 + HB2 + HB3 + HB4	8	62.5	16	31.25 (I) + 31.25 (Q)	24.1	10		

[1] Ideal SNR improvement due to oversampling and filtering = 10log(bandwidth/(f_S/2)).

Table 21. DDC Filter Alias Rejection

Alias Rejection (dB)	Pass-Band Ripple/Cutoff Point (dB)	Alias Protected Bandwidth for Real (I) Outputs[1]	Alias Protected Bandwidth for Complex (I/Q) Outputs
>100	<−0.001	<38.5% × f_{OUT}	<77% × f_{OUT}
90	<−0.001	<38.7% × f_{OUT}	<77.4% × f_{OUT}
85	<−0.001	<38.9% × f_{OUT}	<77.8% × f_{OUT}
63.3	<−0.006	<40% × f_{OUT}	<80% × f_{OUT}
25	−0.5	44.4% × f_{OUT}	88.8% × f_{OUT}
19.3	−1.0	45.6% × f_{OUT}	91.2% × f_{OUT}
10.7	−3.0	48% × f_{OUT}	96% × f_{OUT}

[1] *f_{OUT} = ADC input sample rate ÷ DDC decimation.*

HB3 Filter

The second decimate by 2, half-band, low-pass, FIR filter (HB3) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB3 filter is only used when complex outputs (decimate by 8 or 16) or real outputs (decimate by 4 or 8) are enabled; otherwise, it is bypassed. Table 22 and Figure 68 show the coefficients and response of the HB3 filter.

Table 22. HB3 Filter Coefficients

HB3 Coefficient Number	Normalized Coefficient	Decimal Coefficient (18-Bit)
C1, C11	0.006554	859
C2, C10	0	0
C3, C9	−0.050819	−6661
C4, C8	0	0
C5, C7	0.294266	38,570
C6	0.500000	65,536

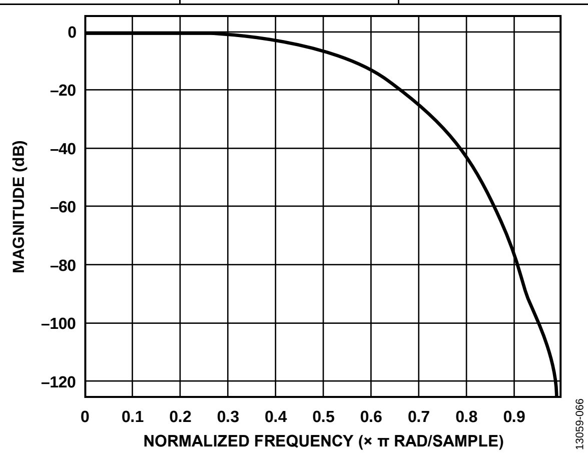


Figure 68. HB3 Filter Response

HB2 Filter

The third decimate by 2, half-band, low-pass, FIR filter (HB2) uses a 19-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption.

The HB2 filter is only used when complex or real outputs (decimate by 4, 8, or 16) are enabled; otherwise, it is bypassed.

Table 23 and Figure 69 show the coefficients and response of the HB2 filter.

Table 23. HB2 Filter Coefficients

HB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (19-Bit)
C1, C19	0.000614	161
C2, C18	0	0
C3, C17	−0.005066	−1328
C4, C16	0	0
C5, C15	0.022179	5814
C6, C14	0	0
C7, C13	−0.073517	−19,272
C8, C12	0	0
C9, C11	0.305786	80,160
C10	0.500000	131,072

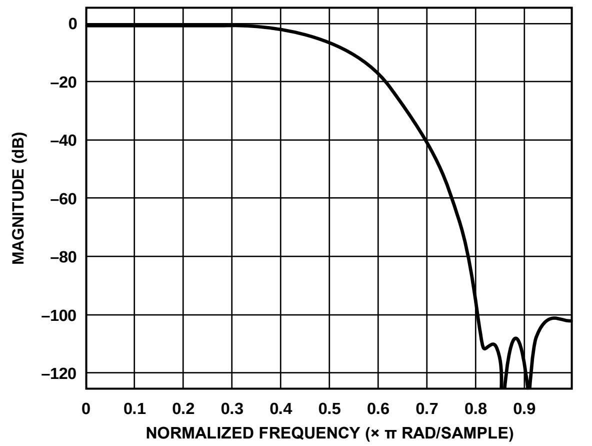


Figure 69. HB2 Filter Response

HB1 Filter

The fourth and final decimate by 2, half-band, low-pass, FIR filter (HB1) uses a 55-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 24 and Figure 70 show the coefficients and response of the HB1 filter.

Table 24. HB1 Filter Coefficients

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
C1, C55	−0.000023	−24
C2, C54	0	0
C3, C53	0.000097	102
C4, C52	0	0
C5, C51	−0.000288	−302
C6, C50	0	0
C7, C49	0.000696	730
C8, C48	0	0
C9, C47	−0.0014725	−1544
C10, C46	0	0
C11, C45	0.002827	2964
C12, C44	0	0
C13, C43	−0.005039	−5284
C14, C42	0	0
C15, C41	0.008491	8903
C16, C40	0	0
C17, C39	−0.013717	−14,383
C18, C38	0	0
C19, C37	0.021591	22,640
C20, C36	0	0
C21, C35	−0.033833	−35,476
C22, C34	0	0
C23, C33	0.054806	57,468
C24, C32	0	0
C25, C31	−0.100557	−105,442
C26, C30	0	0
C27, C29	0.316421	331,792
C28	0.500000	524,288

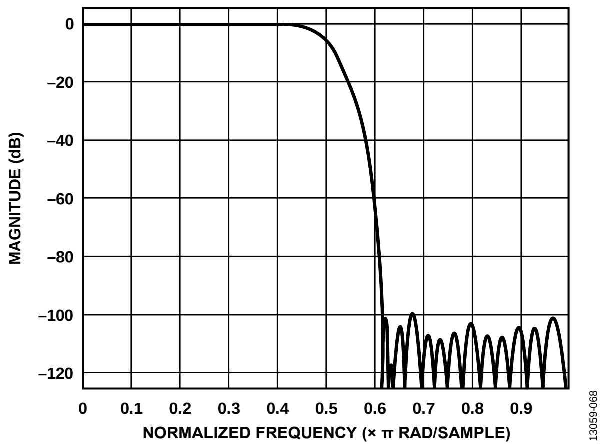


Figure 70. HB1 Filter Response

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended that the user enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits, and no additional gain is necessary. However, the optional 6 dB gain compensates for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage.

DDC COMPLEX TO REAL CONVERSION

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage along with an $f_S/4$ complex mixer to upconvert the signal. After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped.

Figure 71 shows a simplified block diagram of the complex to real conversion.

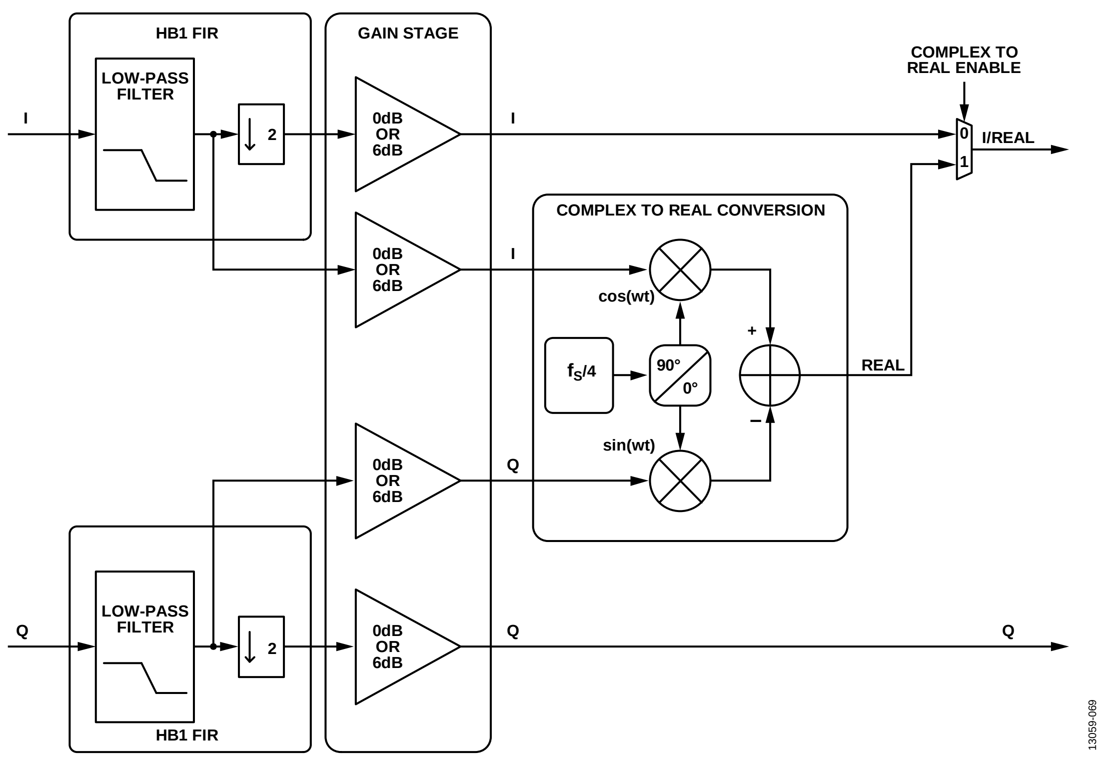


Figure 71. Complex to Real Conversion Block

DDC EXAMPLE CONFIGURATIONS

Table 25 describes the register settings for multiple DDC example configurations.

Table 25. DDC Example Configurations

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
One DDC	2	Complex	Complex	38.5% × f_S	2	Register 0x200 = 0x01 (one DDC; I/Q selected) Register 0x201 = 0x01 (chip decimate by 2) Register 0x310 = 0x83 (complex mixer, 0 dB gain, variable IF, complex outputs, HB1 filter) Register 0x311 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0
One DDC	4	Complex	Complex	19.25% × f_S	2	Register 0x200 = 0x01 (one DDC, I/Q selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310= 0x80 (complex mixer, 0 dB gain, variable IF, complex outputs, HB2 + HB1 filters) Register 0x311 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315= FTW and POW set as required by application for DDC 0
Two DDCs	2	Real	Real	19.25%× f_S	2	Register 0x200 = 0x22 (two DDCs, I only selected) Register 0x201 = 0x01 (chip decimate by 2) Register 0x310, Register 0x330 = 0x48 (real mixer, 6 dB gain, variable IF, real output, HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B, DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	2	Complex	Complex	38.5%× f_S	4	Register 0x200 = 0x22 (two DDCs, I only selected) Register 0x201 = 0x01 (chip decimate by 2) Register 0x310, Register 0x330 = 0x4B (complex mixer, 6 dB gain, variable IF, complex output, HB1 filter) Register 0x311, Register 0x331 = 0x04 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
Two DDCs	4	Complex	Complex	19.25% × f_S	4	Register 0x200 = 0x02 (two DDCs, I/Q selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x80 (complex mixer, 0 dB gain, variable IF, complex outputs, HB2 + HB1 filters) Register 0x311, Register 0x331 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Complex	Real	9.63% × f_S	2	Register 0x200 = 0x22 (two DDCs, I only selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x89 (complex mixer, 0 dB gain, variable IF, real output, HB3 + HB2 + HB1 filters) Register 0x311, Register 0x331 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Real	Real	9.63% × f_S	2	Register 0x200 = 0x22 (two DDCs, I only selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x49 (real mixer, 6 dB gain, variable IF, real output, HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B, DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Real	Complex	19.25% × f_S	4	Register 0x200 = 0x02 (two DDCs, I/Q selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x40 (real mixer, 6 dB gain, variable IF, complex output, HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B, DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
Two DDCs	8	Real	Real	4.81% × f_S	2	Register 0x200 = 0x22 (two DDCs, I only selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330 = 0x4A (real mixer, 6 dB gain, variable IF, real output, HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B, DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Four DDCs	8	Real	Complex	9.63% × f_S	8	Register 0x200 = 0x03 (four DDCs, I/Q selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x41 (real mixer, 6 dB gain, variable IF, complex output, HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A, DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B, DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B, DDC 3 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2 Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3
Four DDCs	8	Real	Real	4.81% × f_S	4	Register 0x200 = 0x23 (four DDCs, I only selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x4A (real mixer, 6 dB gain, variable IF, real output, HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A, DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B, DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B, DDC 3 Q input = ADC Channel B)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
						Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2 Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3
Four DDCs	16	Real	Complex	4.81% × f_S	8	Register 0x200 = 0x03 (four DDCs, I/Q selected) Register 0x201 = 0x04 (chip decimate by 16) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x42 (real mixer, 6 dB gain, variable IF, complex output, HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A, DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B, DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B, DDC 3 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x040, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2 Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3

[1] f_S is the ADC sample rate. Bandwidths listed are <−0.001 dB of pass-band ripple and >100 dB of stop band alias rejection.
[2] The NCOs must be synchronized either through the SPI or through the SYNC± pins after all writes to the FTW or POW registers are complete. This is necessary to ensure the proper operation of the NCO. See the NCO Synchronization section for more information.

NOISE SHAPING REQUANTIZER (NSR)

When operating the AD6679 with the NSR enabled, a decimating half-band filter that is optimized at certain input frequency bands can also be enabled. This filter offers the user the flexibility in signal bandwidth process and image rejection. Careful frequency planning can offer advantages in analog filtering preceding the ADC. The filter can function either in high-pass or low-pass mode. The filter can be optionally enabled on the AD6679 when the NSR is enabled. When operating with NSR enabled, the decimating half-band filter mode (low pass or high pass) is selected by setting Bit 7 in Register 0x41E.

DECIMATING HALF-BAND FILTER

The AD6679 optional decimating half-band filter reduces the input sample rate by a factor of 2 while rejecting aliases that fall into the band of interest. For an input sample clock of 500 MHz, this reduces the output sample rate to 250 MSPS. This filter is designed to provide >40 dB of alias protection for 39.5% of the output sample rate (79% of the Nyquist band). For an ADC sample rate of 500 MSPS, the filter provides a maximum usable bandwidth of 98.75 MHz.

Half-Band Filter Coefficients

The 19-tap, symmetrical, fixed-coefficient half-band filter has low power consumption due to its polyphase implementation. Table 26 lists the coefficients of the half-band filter in low-pass mode. In high-pass mode, Coefficient C9 is multiplied by −1. The normalized coefficients used in the implementation and the decimal equivalent values of the coefficients are listed. Coefficients not listed in Table 26 are 0s.

Table 26. Fixed Coefficients for Half-Band Filter

Coefficient Number	Normalized Coefficient	Decimal Coefficient (12-Bit)
0	0.012207	25
C2, C16	−0.022949	−47
C4, C14	0.045410	93
C6, C12	−0.094726	−194
C8, C10	0.314453	644
C9	0.500000	1024

Half-Band Filter Features

The half-band decimating filter provides approximately 39.5% of the output sample rate in usable bandwidth (19.75% of the input sample clock). The filter provides >40 dB of rejection. The normalized response of the half-band filter in low-pass mode is shown in Figure 72. In low-pass mode, operation is allowed in the first Nyquist zone, which includes frequencies of up to $f_S/2$, where f_S is the decimated sample rate. For example, with an input clock of 500 MHz, the output sample rate is 250 MSPS and $f_S/2$ = 125 MHz.

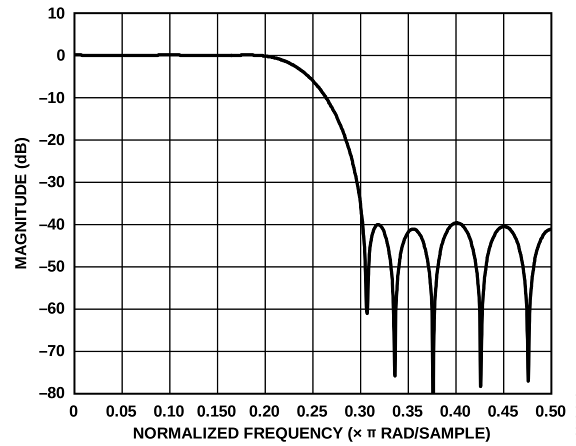


Figure 72. Low-Pass Half-Band Filter Response

The half-band filter can also be utilized in high-pass mode. The usable bandwidth remains at 39.5% of the output sample rate (19.75% of the input sample clock), which is the same as in low-pass mode). Figure 73 shows the normalized response of the half-band filter in high-pass mode. In high-pass mode, operation is allowed in the second and third Nyquist zones, which includes frequencies from $f_S/2$ to $3f_S/2$, where f_S is the decimated sample rate. For example, with an input clock of 500 MHz, the output sample rate is 250 MSPS, $f_S/2$ = 125 MHz, and $3f_S/2$ = 375 MHz.

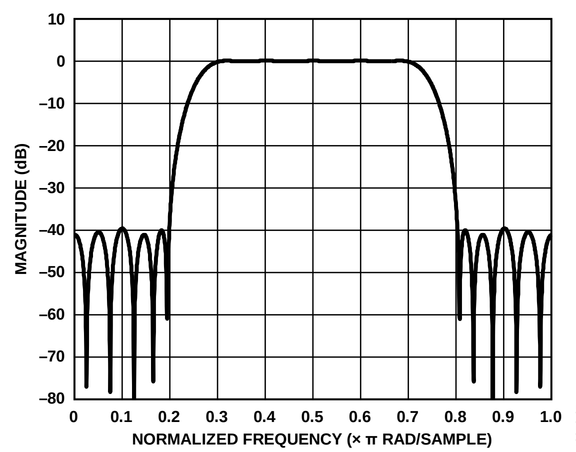


Figure 73. High-Pass Half-Band Filter Response

NSR OVERVIEW

The AD6679 features an NSR to allow higher than 9-bit SNR to be maintained in a subset of the Nyquist band. The harmonic performance of the receiver is unaffected by the NSR feature. When enabled, the NSR contributes an additional 3.0 dB of loss to the input signal, such that a 0 dBFS input is reduced to −3.0 dBFS at the output pins. This loss does not degrade the SNR performance of the AD6679.

The NSR feature can be independently controlled per channel via the SPI.

Two different bandwidth modes are provided; select the mode from the SPI port. In each of the two modes, the center frequency of the band can be tuned such that IFs can be placed anywhere in the Nyquist band. The NSR feature is enabled by default on the AD6679. The bandwidth and mode of the NSR operation are selected by setting the appropriate bits in Register 0x420 and Register 0x422. By selecting the appropriate profile and mode bits in these two registers, the NSR feature can be enabled for the desired mode of operation.

21% BW Mode (>100 MHz at 491.52 MSPS)

The first NSR mode offers excellent noise performance across a bandwidth that is 21% of the ADC output sample rate (42% of the Nyquist band) and can be centered by setting the NSR mode bits in the NSR mode register (Address 0x420) to 000. In this mode, the useful frequency range can be set using the 6-bit tuning word in the NSR tuning register (Address 0x422). There are 59 possible tuning words (TW), from 0 to 58; each step is 0.5% of the ADC sample rate. The following three equations describe the left band edge (f_0), the channel center (f_{CENTER}), and the right band edge (f_1), respectively:

$$f_0 = f_{ADC} \times 0.005 \times TW$$

$$f_{CENTER} = f_0 + 0.105 \times f_{ADC}$$

$$f_1 = f_0 + 0.21 \times f_{ADC}$$

Figure 74 to Figure 76 show the typical spectrum that can be expected from the AD6679 in the 21% BW mode for three different tuning words.

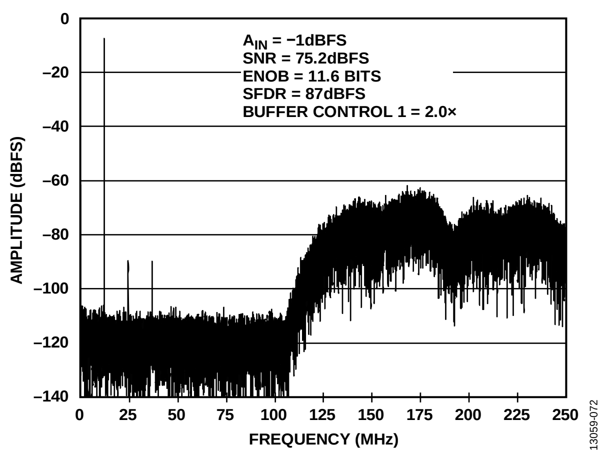


Figure 74. 21% BW Mode, Tuning Word = 0

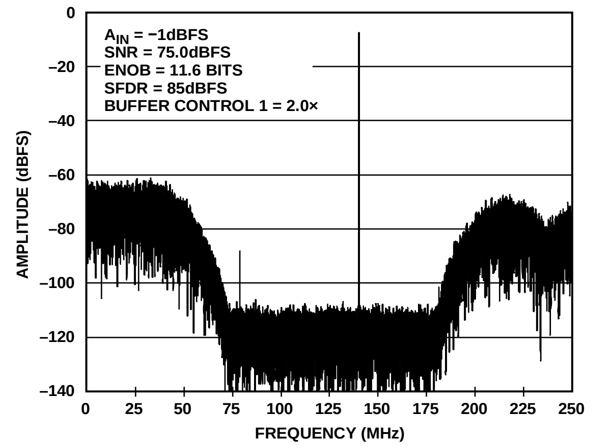


Figure 75. 21% BW Mode, Tuning Word = 26 (f_S/4 Tuning)

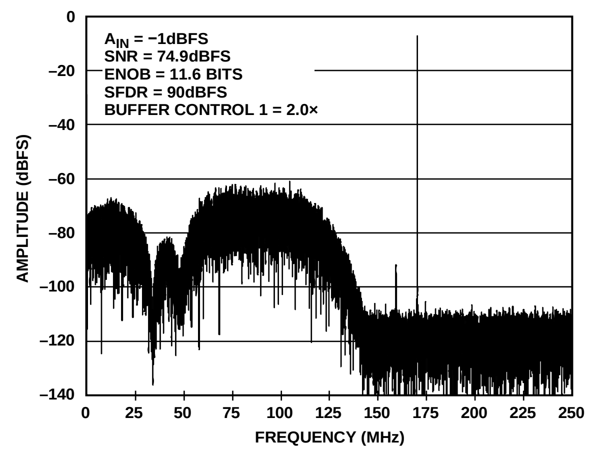


Figure 76. 21% BW Mode, Tuning Word = 58

28% BW Mode (>130 MHz at 491.52 MSPS)

The second NSR mode offers excellent noise performance across a bandwidth that is 28% of the ADC output sample rate (56% of the Nyquist band) and can be centered by setting the NSR mode bits in the NSR mode register (Address 0x420) to 001. In this mode, the useful frequency range can be set using the 6-bit tuning word in the NSR tuning register (Address 0x422). There are 44 possible tuning words (TW, from 0 to 43); each step is 0.5% of the ADC sample rate. The following three equations describe the left band edge (f_0), the channel center (f_{CENTER}), and the right band edge (f_1), respectively:

$$f_0 = f_{ADC} \times 0.005 \times TW$$

$$f_{CENTER} = f_0 + 0.14 \times f_{ADC}$$

$$f_1 = f_0 + 0.28 \times f_{ADC}$$

Figure 77 to Figure 79 show the typical spectrum that can be expected from the AD6679 in the 28% BW mode for three different tuning words.

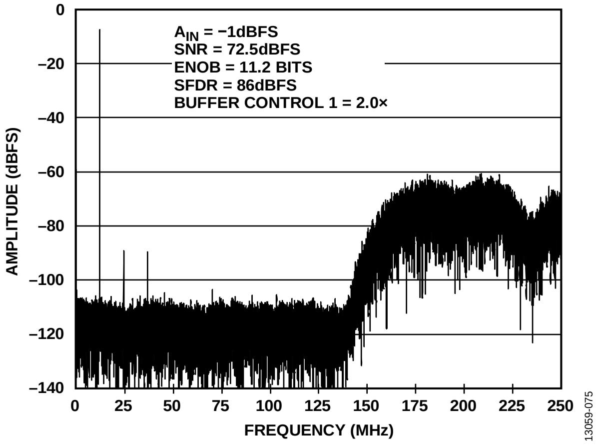


Figure 77. 28% BW Mode, Tuning Word = 0

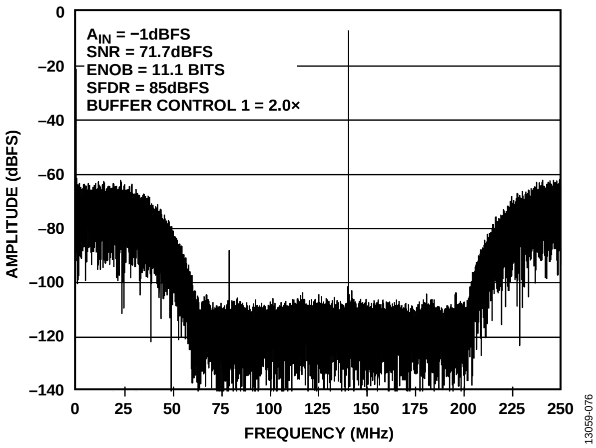


Figure 78. 28% BW Mode, Tuning Word = 19 (f_S/4 Tuning)

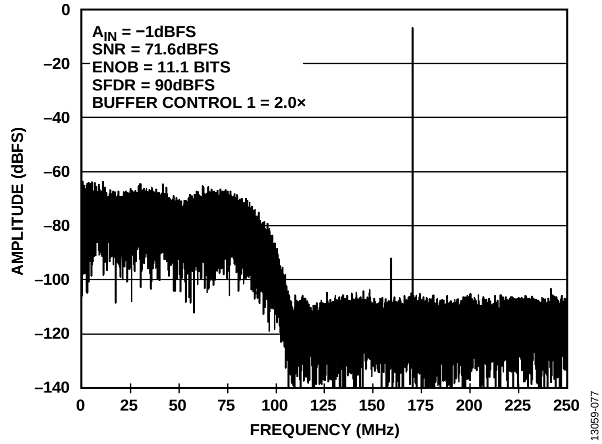


Figure 79. 28% BW Mode, Tuning Word = 43

VARIABLE DYNAMIC RANGE (VDR)

The AD6679 features a variable dynamic range (VDR) digital processing block to allow up to 14-bit dynamic range to be maintained in a subset of the Nyquist band. Across the full Nyquist band, a minimum of a 9-bit dynamic range is available at all times. This operation is suitable for applications such as digital predistortion processing (DPD). The harmonic performance of the receiver is unaffected by this feature. When enabled, VDR does not contribute loss to the input signal but operates by effectively changing the output resolution at the output pins. This feature can be independently controlled per channel via the SPI.

The VDR block operates in either complex or real mode. In complex mode, VDR has selectable bandwidths of 25% and 43% of the output sample rate. In real mode, the bandwidth of operation is limited to 25% of the output sample rate. The bandwidth and mode of the VDR operation are selected by setting the appropriate bits in Register 0x430.

When the VDR block is enabled, input signals that violate a defined mask (signified by gray shaded areas in Figure 80) result in the reduction of the output resolution of the AD6679. The VDR block analyzes the peak value of the aggregate signal level in the disallowed zones to determine the reduction of the output resolution. To indicate that the AD6679 is reducing output, the VDR punish bit or a VDR high/low resolution bit can optionally be on the STATUS±/OVR± pins by programming the appropriate value into Register 0x559. The VDR high/low resolution bit can alternatively be programmed to output on the STATUS± pins and simply indicates if VDR is reducing output resolution (bit value is a 1), or if full resolution is available (bit value is a 0). These VDR high/low resolution and VDR punish bits can be decoded by using Table 27. Note that only one can be output at a given time.

Table 27. VDR Reduced Output Resolution Values

VDR Punish Bit	VDR High/Low Resolution Bit	Output Resolution (Bits)
0	Not applicable	14 or 13
1	Not applicable	≤12
Not applicable	0	14
Not applicable	1	≤13

The frequency zones of the mask are defined by the bandwidth mode selected in Register 0x430. The upper amplitude limit for input signals located in these frequency zones is −30 dBFS. If the input signal level in the disallowed frequency zones goes above an amplitude level of −30 dBFS (into the gray shaded areas), the VDR block triggers a reduction in the output resolution, as shown in Figure 80. The VDR block engages and begins limiting output resolution gradually as the signal amplitudes increase in the mask regions. As the signal amplitude level increases into the mask regions, the output resolution is gradually lowered. For every 6 dB increase in signal level above −30 dBFS, one bit of output resolution is discarded from the output data by the VDR block, as shown in Table 28. These zones can be tuned within the Nyquist band by setting Bits[3:0] in Register 0x434 to determine the VDR center frequency (f_{VDR}). The VDR center frequency in complex mode can be adjusted from 1/16 f_S to 15/16 f_S in 1/16 f_S steps. In real mode, f_{VDR} can be adjusted from 1/8 f_S to 3/8 f_S in 1/16 f_S steps.

Table 28. VDR Reduced Output Resolution Values

Signal Amplitude Violating Defined VDR Mask	Output Resolution (Bits)
Amplitude ≤ −30 dBFS	14
−30 dBFS < amplitude ≤ −24 dBFS	13
−24 dBFS < amplitude ≤ −18 dBFS	12
−18 dBFS < amplitude ≤ −12 dBFS	11
−12 dBFS < amplitude ≤ −6 dBFS	10
−6 dBFS < amplitude ≤ 0 dBFS	9

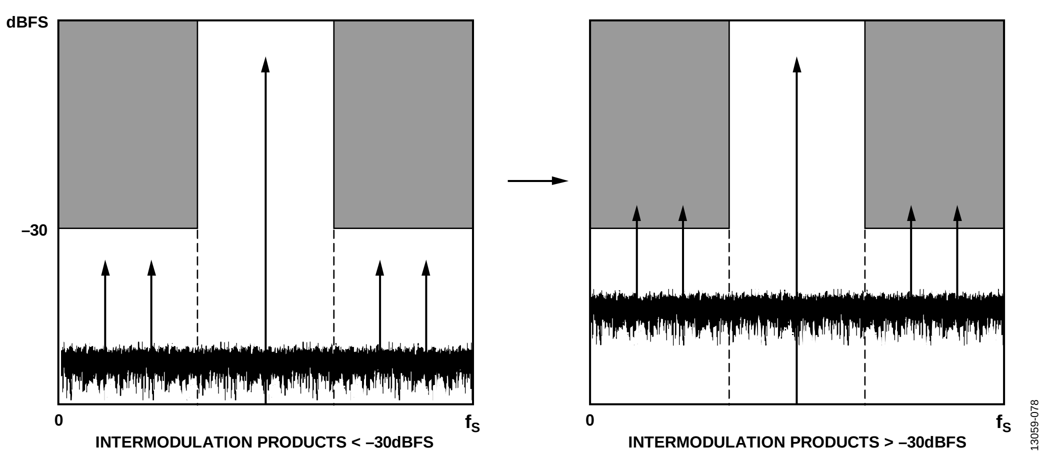


Figure 80. VDR Operation—Reduction in Output Resolution

VDR REAL MODE

The real mode of VDR works over a bandwidth of 25% of the sample rate (50% of the Nyquist band). The output bandwidth of the AD6679 can be 25% only when operating in real mode. Figure 81 shows the frequency zones for the 25% bandwidth real output VDR mode tuned to a center frequency (f_{VDR}) of $f_S/4$ (tuning word = 0x04). The frequency zones where the amplitude may not exceed −30 dBFS are the upper and lower portions of the Nyquist band signified by the red shaded areas.

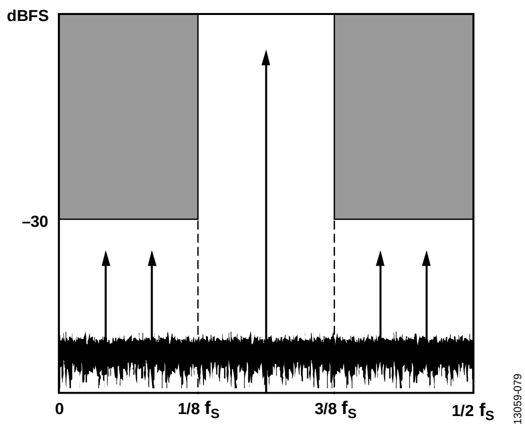


Figure 81. 25% VDR Bandwidth, Real Mode

The center frequency (f_{VDR}) of the VDR function can be tuned within the Nyquist band from 1/8 f_S to 3/8 f_S in 1/16 f_S steps. In real mode, Tuning Word 2 (0x02) through Tuning Word 6 (0x06) are valid. Table 29 shows the relative frequency values, and Table 30 shows the absolute frequency values based on a sample rate of 491.52 MSPS.

Table 29. VDR Tuning Words and Relative Frequency Values, 25% BW, Real Mode

Tuning Word	Lower Band Edge	Center Frequency	Upper Band Edge
2 (0x02)	0	1/8 f_S	1/4 f_S
3 (0x03)	1/16 f_S	3/16 f_S	5/16 f_S
4 (0x04)	1/8 f_S	1/4 f_S	3/8 f_S
5 (0x05)	3/16 f_S	5/16 f_S	7/16 f_S
6 (0x06)	1/4 f_S	3/8 f_S	1/2 f_S

Table 30. VDR Tuning Words and Absolute Frequency Values, 25% BW, Real Mode with f_S = 491.52 MSPS

Tuning Word	Lower Band Edge (MHz)	Center Frequency (MHz)	Upper Band Edge (MHz)
2 (0x02)	0	61.44	122.88
3 (0x03)	30.72	92.16	153.6
4 (0x04)	61.44	122.88	184.32
5 (0x05)	92.16	153.6	215.04
6 (0x06)	122.88	184.32	245.76

VDR COMPLEX MODE

The complex mode of VDR works with selectable bandwidths of 25% of the sample rate (50% of the Nyquist band) and 43% of the sample rate (86% of the Nyquist band). Figure 82 and Figure 83 show the frequency zones for VDR in the complex mode. When operating VDR in complex mode, place in-phase (I) input signal data in Channel A and place quadrature (Q) signal data in Channel B.

Figure 82 shows the frequency zones for the 25% bandwidth VDR mode with a center frequency of $f_S/4$ (tuning word = 0x04). The frequency zones where the amplitude may not exceed −30 dBFS are the upper and lower portions of the Nyquist band extending into the complex domain.

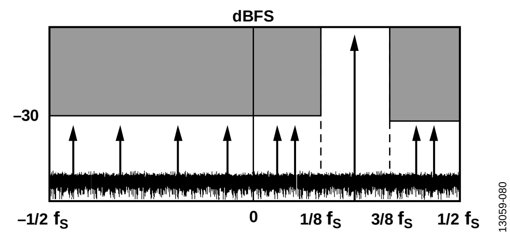


Figure 82. 25% VDR Bandwidth, Complex Mode

The center frequency (f_{VDR}) of the VDR function can be tuned within the Nyquist band from 0 to 15/16f_S in 1/16 f_S steps. In complex mode, Tuning Word 0 (0x00) through Tuning Word 15 (0x0F) are valid. Table 31 and Table 32 show the tuning words and frequency values for the 25% complex mode. Table 31 shows the relative frequency values, and Table 32 shows the absolute frequency values based on a sample rate of 491.52 MSPS.

Table 31. VDR Tuning Words and Relative Frequency Values, 25% BW, Complex Mode

Tuning Word	Lower Band Edge	Center Frequency	Upper Band Edge
0 (0x00)	−1/8 f_S	0	1/8 f_S
1 (0x01)	−1/16 f_S	1/16 f_S	3/16 f_S
2 (0x02)	0	1/8 f_S	1/4 f_S
3 (0x03)	1/16 f_S	3/16 f_S	5/16 f_S
4 (0x04)	1/8 f_S	1/4 f_S	3/8 f_S
5 (0x05)	3/16 f_S	5/16 f_S	7/16 f_S
6 (0x06)	1/4 f_S	3/8 f_S	1/2 f_S
7 (0x07)	5/16 f_S	7/16 f_S	9/16 f_S
8 (0x08)	3/8 f_S	1/2 f_S	5/8 f_S
9 (0x09)	7/16 f_S	9/16 f_S	11/16 f_S
10 (0x0A)	1/2 f_S	5/8 f_S	3/4 f_S
11 (0x0B)	9/16 f_S	11/16 f_S	13/16 f_S
12 (0x0C)	5/8 f_S	3/4 f_S	7/8 f_S
13 (0x0D)	11/16 f_S	13/16 f_S	15/16 f_S
14 (0x0E)	3/4 f_S	7/8 f_S	f_S
15 (0x0F)	13/16 f_S	15/16 f_S	17/16 f_S

Table 32. VDR Tuning Words and Absolute Frequency Values, 25% BW, Complex Mode (f_S = 491.52 MSPS)

Tuning Word	Lower Band Edge (MHz)	Center Frequency (MHz)	Upper Band Edge (MHz)
0 (0x00)	−61.44	0.00	61.44
1 (0x01)	−30.72	30.72	92.16
2 (0x02)	0.00	61.44	122.88
3 (0x03)	30.72	92.16	153.6
4 (0x04)	61.44	122.88	184.32
5 (0x05)	92.16	153.6	215.04
6 (0x06)	122.88	184.32	245.76
7 (0x07)	153.6	215.04	276.48
8 (0x08)	184.32	245.76	307.2
9 (0x09)	215.04	276.48	337.92
10 (0x0A)	245.76	307.2	368.64
11 (0x0B)	276.48	337.92	399.36
12 (0x0C)	307.2	368.64	430.08
13 (0x0D)	337.92	399.36	460.8
14 (0x0E)	368.64	430.08	491.52
15 (0x0F)	399.36	460.8	522.24

Table 33 and Table 34 show the tuning words and frequency values for the 43% complex mode. Table 33 shows the relative frequency values, and Table 34 shows the absolute frequency values based on a sample rate of 491.52 MSPS. Figure 83 shows the frequency zones for the 43% BW VDR mode with a center frequency (f_{VDR}) of f_S/4 (tuning word = 0x04). The frequency zones where the amplitude may not exceed −30 dBFS are the upper and lower portions of the Nyquist band extending into the complex domain.

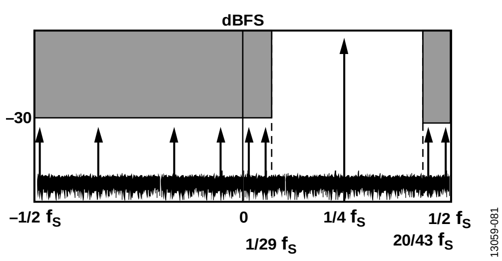


Figure 83. 43% VDR Bandwidth, Complex Mode

Table 33. VDR Tuning Words and Relative Frequency Values, 43% BW, Complex Mode

Tuning Word	Lower Band Edge (MHz)	Center Frequency (MHz)	Upper Band Edge (MHz)
0 (0x00)	−14/65 f_S	0	14/65 f_S
1 (0x01)	−11/72 f_S	1/16 f_S	5/18 f_S
2 (0x02)	−1/11 f_S	1/8 f_S	16/47 f_S
3 (0x03)	−1/36 f_S	3/16 f_S	29/72 f_S
4 (0x04)	1/29 f_S	1/4 f_S	20/43 f_S
5 (0x05)	7/72 f_S	5/16 f_S	19/36 f_S
6 (0x06)	4/25 f_S	3/8 f_S	49/83 f_S
7 (0x07)	2/9 f_S	7/16 f_S	47/72 f_S
8 (0x08)	2/7 f_S	1/2 f_S	5/7 f_S
9 (0x09)	25/72 f_S	9/16 f_S	7/9 f_S
10 (0x0A)	34/83 f_S	5/8 f_S	21/25 f_S
11 (0x0B)	17/36 f_S	11/16 f_S	65/72 f_S
12 (0x0C)	23/43 f_S	3/4 f_S	28/29 f_S
13 (0x0D)	43/72 f_S	13/16 f_S	37/36 f_S
14 (0x0E)	31/47 f_S	7/8 f_S	12/11 f_S
15 (0x0F)	13/18 f_S	15/16 f_S	83/72 f_S

Table 34. VDR Tuning Words and Absolute Frequency Values, 43% BW, Complex Mode (f_S = 491.52 MSPS)

Tuning Word	Lower Band Edge (MHz)	Center Frequency (MHz)	Upper Band Edge (MHz)
0 (0x00)	−105.37	0.00	105.87
1 (0x01)	−75.09	30.72	136.53
2 (0x02)	−44.68	61.44	167.33
3 (0x03)	−13.65	92.16	197.97
4 (0x04)	16.95	122.88	228.61
5 (0x05)	47.79	153.6	259.41
6 (0x06)	78.64	184.32	290.17
7 (0x07)	109.23	215.04	320.85
8 (0x08)	140.43	245.76	351.09
9 (0x09)	170.67	276.48	382.29
10 (0x0A)	201.35	307.2	412.88
11 (0x0B)	232.11	337.92	443.73
12 (0x0C)	262.91	368.64	474.57
13 (0x0D)	293.55	399.36	505.17
14 (0x0E)	324.19	430.08	536.2
15 (0x0F)	354.99	460.8	566.61

DIGITAL OUTPUTS

The AD6679 output drivers are for standard ANSI LVDS, but optionally the drive current can be reduced using Register 0x56A. The reduced drive current for the LVDS outputs potentially reduces the digitally induced noise.

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

The AD6679 has a flexible three-state ability for the digital output pins. The three-state mode is enabled when the device is set for power-down mode.

TIMING

The AD6679 provides latched data with a pipeline delay of 33 input sample clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

Minimize the length of the output data lines and the corresponding loads to reduce transients within the AD6679. These transients can degrade converter dynamic performance.

The minimum conversion rate of the AD6679 is 300 MSPS. At clock rates below 300 MSPS, dynamic performance may degrade.

DATA CLOCK OUTPUT

The AD6679 also provides a data clock output (DCO) intended for capturing the data in an external register. Figure 4 through Figure 11 show the timing diagrams of the AD6679 output modes. The DCO relative to the data output can be adjusted using Register 0x569. There are delay settings with approximately 90° per step ranging from 0° to 270°. Data is output in a DDR format and is aligned to the rising and falling edges of the clock derived from the DCO.

ADC OVERRANGE

The ADC overrange (OR) indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and, therefore, is subject to a latency of 33 ADC clocks. An overrange at the input is indicated by the OR bit, 33 clock cycles after it occurs.

Table 35. LVDS Output Configurations[1]

Parallel Output Mode	No. of Virtual Converters Supported	Maximum Virtual Converter Resolution (Bits)	Output Line Rate[2, 3]	VDR Supported	NSR Decimation Rates Supported	DDC Decimation Rates Supported		Outputs Required
						Real Output	Complex Output	
Parallel Interleaved, One Virtual Converter (Register 0x568 = 0x0)	1	14	$1 \times f_{OUT}$	Yes	1, 2	1, 2, 4, 8	N/A	DCO±, OVR±, and D0± to D13±
Parallel Interleaved, Two Virtual Converters (Register 0x568 = 0x1)	2	14	$2 \times f_{OUT}$	Yes	1, 2	1, 2, 4, 8	2, 4, 8, 16	DCO±, OVR±, and D0± to D13±
Channel Multiplexed, One Virtual Converter (Register 0x568 = 0x2)	1	14	$2 \times f_{OUT}$	Yes	1, 2	1, 2, 4, 8	N/A	DCO±, OVR±, A Dx/Dy±
Channel Multiplexed, Two Virtual Converters (Register 0x568 = 0x3)	2	14	$2 \times f_{OUT}$	Yes	1, 2	1, 2, 4, 8	2, 4, 8, 16	DCO±, OVR±, A Dx/Dy±, and B Dx/Dy±
Byte Mode, One Virtual Converter (Register 0x568 = 0x4)	1	16	$2 \times f_{OUT}$	No	1, 2	1, 2, 4, 8	N/A	DCO±, STATUS±, and DATA0± to DATA7±
Byte Mode, Two Virtual Converters (Register 0x568 = 0x5)	2	16	$4 \times f_{OUT}$	No	2	2, 4, 8	2, 4, 8, 16	DCO±, STATUS±, and DATA0± to DATA7±
Byte Mode, Four Virtual Converters (Register 0x568 = 0x6)	4	16	$8 \times f_{OUT}$	No	N/A	2[4], 4, 8	2[4], 4, 8, 16	DCO±, STATUS±, and DATA0± to DATA7±
Byte Mode, Eight Virtual Converters (Register 0x568 = 0x7)	8	16	$16 \times f_{OUT}$	No	N/A	N/A	4[4], 8, 16	DCO±, STATUS±, and DATA0± to DATA7±

[1] N/A means not applicable.
[2] f_{OUT} = ADC Sample Rate ÷ chip decimation ratio, where f_{OUT} is the output sample rate.
[3] Maximum output line rate is 1000 Mbps.
[4] $f_{OUT} \le 125$ MSPS.

Table 36. Pin Mapping Comparison Between Parallel Interleaved, Channel Multiplexed, and Byte Modes

Pin No.	Parallel Interleaved Output	Channel Multiplexed (Even/Odd) Output	Byte Output
K13, K14	DCO−, DCO+	DCO−, DCO+	DCO−, DCO+
L13, L14	OVR−, OVR+	OVR−, OVR+	FCO−, FCO+
M13, M14	D13−, D13+	A D12/D13−, A D12/D13+	STATUS−, STATUS+
N14, P14	D12−, D12+	A D10/D11−, A D10/D11+	DATA7−, DATA7+
N13, P13	D11−, D11+	A D8/D9−, A D8/D9+	DATA6−, DATA6+
N12, P12	D10−, D10+	A D6/D7−, A D6/D7+	DATA5−, DATA5+
N11, P11	D9−, D9+	A D4/D5−, A D4/D5+	DATA4−, DATA4+
N10, P10	D8−, D8+	A D2/D3−, A D2/D3+	DATA3−, DATA3+
N9, P9	D7−, D7+	A D0/D1−, A D0/D1+	DATA2−, DATA2+
N5, P5	D6−, D6+	B D12/D13−, B D12/D13+	DATA1−, DATA1+
N4, P4	D5−, D5+	B D10/D11−, B D10/D11+	DATA0−, DATA0+
N3, P3	D4−, D4+	B D8/D9−, B D8/D9+	Not applicable
N2, P2	D3−, D3+	B D6/D7−, B D6/D7+	Not applicable
N1, P1	D2−, D2+	B D4/D5−, B D4/D5+	Not applicable
M2, M1	D1−, D1+	B D2/D3−, B D2/D3+	Not applicable
N6, P6	D0−, D0+	B D0/D1−, B D0/D1+	Not applicable

MULTICHIP SYNCHRONIZATION

The AD6679 has a SYNC± input that allows the user flexible options for synchronizing the internal blocks. The SYNC± input is a source synchronous system reference signal that enables multichip synchronization. The input clock divider, DDCs, and signal monitor block can be synchronized using the SYNC± input. For the highest level of timing accuracy, SYNC± must meet the setup and hold requirements relative to the CLK± input.

The flowchart in Figure 84 shows the internal mechanism by which multichip synchronization can be achieved in the AD6679.

The AD6679 supports several features that aid users in meeting the requirements for capturing a SYNC± signal. The SYNC± sample event is defined as either a synchronous low to high transition or a synchronous high to low transition. Additionally, the AD6679 allows the SYNC± signal to be sampled using either the rising edge or falling edge of the CLK± input. The AD6679 also can ignore a programmable number (up to 16) of SYNC± events. The SYNC± control options can be selected using Register 0x120 and Register 0x121.

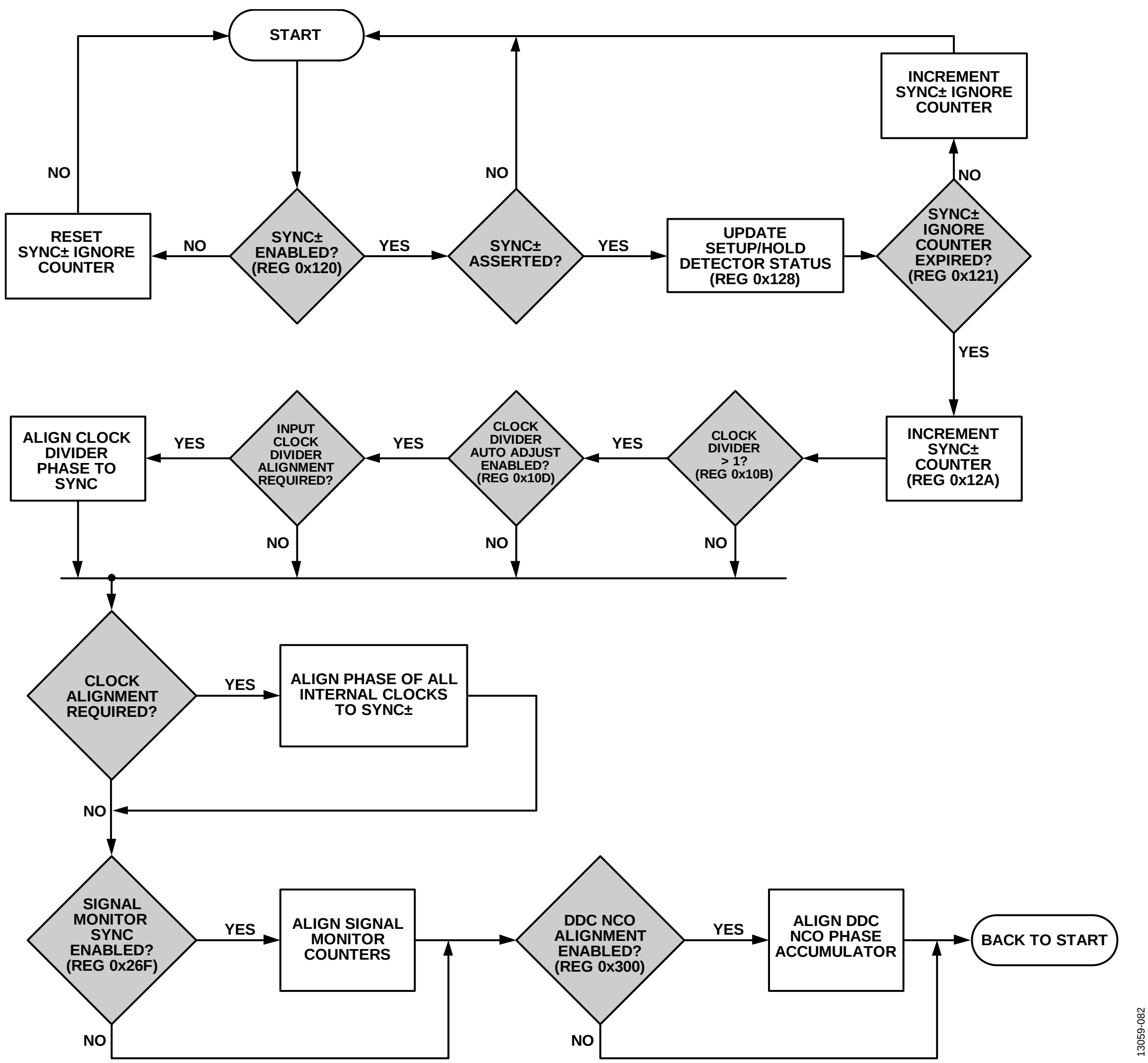


Figure 84. Multichip Synchronization

SYNC± SETUP AND HOLD WINDOW MONITOR

To assist in ensuring a valid SYNC± capture, the AD6679 has a SYNC± setup and hold window monitor. This feature allows the system designer to determine the location of the SYNC± signals relative to the CLK± signals by reading back the amount of setup and hold margin on the interface through the memory map. Figure 85 and Figure 86 show both the setup and hold status values, respectively, for different phases of SYNC±. The setup detector returns the status of the SYNC± signal before the CLK± edge and the hold detector returns the status of the SYNC± signal after the CLK± edge. Register 0x128 stores the status of SYNC± and indicates whether the SYNC± signal was captured by the ADC.

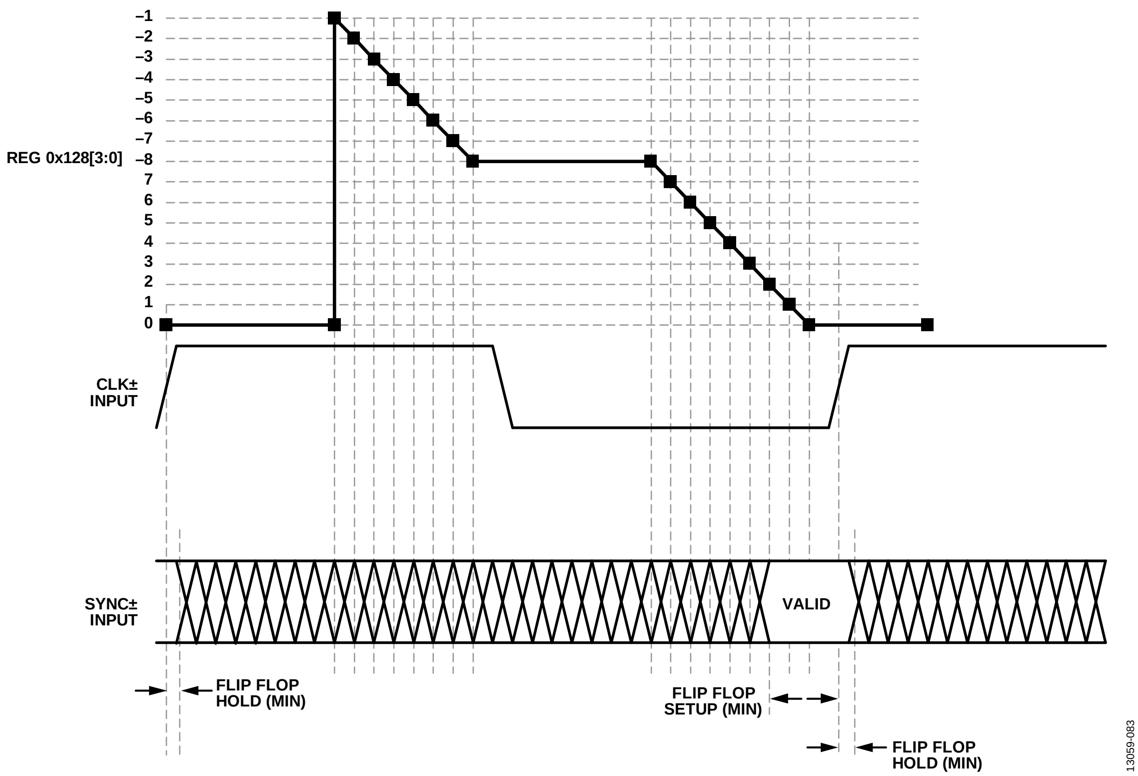


Figure 85. SYNC ± Setup Detector

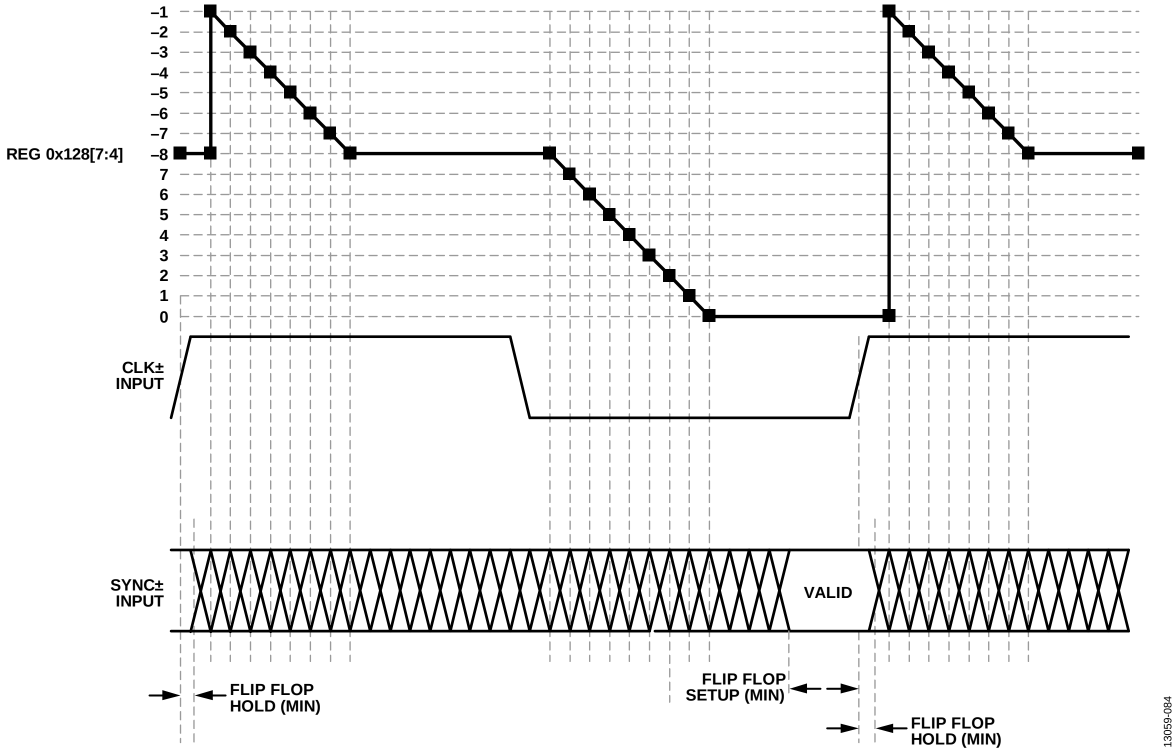


Figure 86. SYNC± Hold Detector

Table 37 shows the description of the contents of Register 0x128 and how to interpret them.

Table 37. SYNC± Setup and Hold Monitor, Register 0x128

Register 0x128, Bits[7:4] Hold Status	Register 0x128, Bits[3:0] Setup Status	Description
0x0	0x0 to 0x7	Possible setup error; the smaller this number, the smaller the setup margin
0x0 to 0x8	0x8	No setup or hold error (best hold margin)
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin)
0x8	0x0	No setup or hold error (best setup margin)
0x9 to 0xF	0x0	Possible hold error; the larger this number, the smaller the hold margin
0x0	0x0	Possible setup or hold error

TEST MODES

ADC TEST MODES

The AD6679 has various test options that aid in the system level implementation. The AD6679 has ADC test modes that are available in Register 0x550. These test modes are described in Table 38. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x550. These tests can be performed with or without an analog signal (if present, the analog signal is ignored); however, they do require an encode clock.

If the application mode has been set to select a DDC mode of operation, the test modes must be enabled for each DDC enabled. The test patterns can be enabled via Bit 2 and Bit 0 of Register 0x327, Register 0x347, Register 0x367, and Register 0x387, depending on which DDC(s) have been selected. The (I) output data uses the test patterns selected for Channel A and the (Q) output data uses the test patterns selected for Channel B. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Table 38. ADC Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	Not applicable	Not applicable	Not applicable
0001	Midscale short	00 0000 0000 0000	Not applicable	Not applicable
0010	Positive Full-scale short	01 1111 1111 1111	Not applicable	Not applicable
0011	Negative Full-scale short	10 0000 0000 0000	Not applicable	Not applicable
0100	Checkerboard	10 1010 1010 1010	Not applicable	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence, long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence, short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697
0111	One-/zero-word toggle	11 1111 1111 1111	Not applicable	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x551 to Register 0x558	Not applicable	For repeat mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2]…
				For single mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000…
1111	Ramp output	$(x) \% 2^{14}$	Not applicable	$(x) \% 2^{14}$, $(x + 1) \% 2^{14}$, $(x + 2) \% 2^{14}$, $(x + 3) \% 2^{14}$

SERIAL PORT INTERFACE (SPI)

The AD6679 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the serial port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the *Serial Control Interface Standard*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 39). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 39. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which synchronizes serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. See Figure 3 and Table 5 for an example of the serial timing and its definitions.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB pin can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This bit allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default configuration on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the *Serial Control Interface Standard*.

HARDWARE INTERFACE

The pins described in Table 39 compose the physical interface between the user programming device and the serial port of the AD6679. The SCLK pin and the CSB pin function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD6679 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 40 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the *Serial Control Interface Standard*. The AD6679 device specific features are described in the Memory Map section.

Table 40. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the clock divider via the SPI
Test Input/Output	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Serializer/Deserializer (SERDES) Output Setup	Allows the user to vary SERDES settings, including swing and emphasis

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into seven sections: the Analog Devices, Inc., SPI registers, the analog input buffer control registers, ADC function registers, the DDC function registers, NSR decimate by 2 and noise shaping requantizer registers, variable dynamic range registers, and the digital outputs and test modes registers.

Table 41 (see the Memory Map Register Table section) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x561, the output format register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see Table 41.

Open and Reserved Locations

All address and bit locations that are not included in Table 41 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is open (for example, Address 0x561). If the entire address location is open (for example, Address 0x013), do not write to this address location.

Default Values

After the AD6679 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 41.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- "X" denotes "don't care".

Channel Specific Registers

Some channel setup functions such as analog input differential termination (Register 0x016) can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 41 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x008. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A or Channel B to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. Registers and bits designated as global in Table 41 affect the entire device and the channel features for which independent settings are not allowed between channels. The settings in Register 0x008 do not affect the global registers and bits.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x000, the AD6679 requires 5 ms to recover. Therefore, when programming the AD6679 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

Datapath Soft Reset

After programming the desired clock divider settings, changing the input clock frequency, or glitching the input clock, a datapath soft reset is recommended by writing 0x02 to Register 0x001. This reset function restarts all the datapath and clock generation circuitry in the device. The reset occurs on the first clock cycle after the register is programmed and the device requires 5 ms to recover. This reset does not affect the contents of the memory map registers.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 41 are not currently supported for this device.

Table 41. Memory Map Registers

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
Analog Devices SPI Registers											
0x000	INTERFACE_CONFIG_A	Soft reset (self clearing): clears memory map registers	LSB first 0 = MSB 1 = LSB	Address ascension	0	0	Address ascension	LSB first 0 = MSB 1 = LSB	Soft reset (self clearing): clears memory map registers	0x00	
0x001	INTERFACE_CONFIG_B	Single instruction	0	0	0	0	0	Datapath soft reset (self clearing): does not clear memory map registers	0	0x00	
0x002	DEVICE_CONFIG (local)	0	0	0	0	0	0	00 = normal operation 10 = standby 11 = power-down		0x00	
0x003	CHIP_TYPE					011 = high speed ADC				0x03	Read only
0x004	CHIP_ID (low byte)									0xD3	Read only
0x005	CHIP_ID (high byte)	0	0	0	0	0	0	0	0	0x00	Read only
0x006	CHIP_GRADE	Chip speed grade 0101 = 500 MSPS				0	1	0	X	X	Read only
0x008	Device index	0	0	0	0	0	0	Channel B	Channel A	0x03	
0x00A	Scratch pad	0	0	0	0	0	0	0	0	0x00	
0x00B	SPI revision	0	0	0	0	0	0	0	1	0x01	
0x00C	Vendor ID (low byte)	0	1	0	1	0	1	1	0	0x56	Read only
0x00D	Vendor ID (high byte)	0	0	0	0	0	1	0	0	0x04	Read only
Analog Input Buffer Control Registers											
0x015	Analog Input (local)	0	0	0	0	0	0	0	Input disable 0 = normal operation 1 = input disabled	0x00	
0x016	Input termination (local)	Analog input differential termination 0000 = 400 Ω (default) 0001 = 200 Ω 0010 = 100 Ω 0110 = 50 Ω				1	1	0	0	0x0C	
0x934	Input capacitance	0	0	0	0x1F = 3 pF to GND (default) 0x00 = 1.5 pF to GND					0x1F	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x018	Buffer Control 1 (local)	0000 = 1.0× buffer current 0001 = 1.5× buffer current 0010 = 2.0× buffer current (default) 0011 = 2.5× buffer current 0100 = 3.0× buffer current 0101 = 3.5× buffer current … 1111 = 8.5× buffer current				0	0	0	0	0x20	
0x019	Buffer Control 2 (local)	0100 = Setting 1 0101 = Setting 2 0110 = Setting 3 (default) 0111 = Setting 4 (see Table 11 for setting per frequency range)				0	0	0	0	0x60	
0x01A	Buffer Control 3 (local)	0	0	0	0	1000 = Setting 1 1001 = Setting 2 1010 = Setting 3 (default) (see Table 11 for setting per frequency range)				0x0A	
0x11A	Buffer Control 4 (local)	0	0	High frequency setting 0 = off (default) 1 = on	0	0	0	0	0	0x00	
0x935	Buffer Control 5 (local)	0	0	0	0	0	Low frequency operation 0 = off 1 = on (default)	0	0	0x04	
0x025	Input full-scale range (local)	0	0	0	0	Full-scale adjust 0000 = 1.94 V p-p 1000 = 1.46 V p-p 1001 = 1.58 V p-p 1010 = 1.70 V p-p 1011 = 1.82 V p-p 1100 = 2.06 V p-p (default)				0x0C	Differ-ential; use in con-junction with Reg. 0x030
0x030	Input full-scale control (local)	0	0	0	Full-scale control See Table 11 for recommended settings for different frequency bands; default values: Full scale range ≥ 1.82 V = 001 Full scale range < 1.82 V = 110			0	0	0x04	Used in con-junction with Reg. 0x025
ADC Function Registers											
0x024	V_1P0 control	0	0	0	0	0	0	0	1.0 V reference select 0 = internal 1 = external	0x00	
0x028	Temperature diode (local)	0	0	0	0	0	0	0	Diode selection 0 = no diode selected 1 = temper-ature diode selected	0x00	
0x03F	PDWN/STBY pin control (local)	0 = PDWN/ STBY enabled 1 = disabled	0	0	0	0	0	0	0	0x00	Used in con-junction with Reg. 0x040

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x040	Chip pin control	PDWN/STBY function 00 = power down 01 = standby 10 = disabled		Fast Detect B (FD_B) 000 = Fast Detect B output 111 = disabled			Fast Detect A (FD_A) 000 = Fast Detect A output 011 = temperature diode 111 = disabled			0x3F	
0x10B	Clock divider	0	0	0	0	0	000 = divide by 1 001 = divide by 2 011 = divide by 4 111 = divide by 8			0x00	
0x10C	Clock divider phase (local)	0	0	0	0	Independently controls Channel A and Channel B clock divider phase offset 0000 = 0 input clock cycles delayed 0001 = ½ input clock cycles delayed 0010 = 1 input clock cycles delayed 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed				0x00	
0x10D	Clock divider and SYNC± control	Clock divider auto-phase adjust 0 = disabled 1 = enabled	0	0	0	Clock divider negative skew window 00 = no negative skew 01 = 1 device clock of negative skew 10 = 2 device clocks of negative skew 11 = 3 device clocks of negative skew		Clock divider positive skew window 00 = no positive skew 01 = 1 device clock of positive skew 10 = 2 device clocks of positive skew 11 = 3 device clocks of positive skew		0x00	Clock divider must be >1
0x117	Clock delay control	0	0	0	0	0	0	0	Clock fine delay adjust enable 0 = disabled 1 = enabled	0x00	Enabling the clock fine delay adjust causes a data-path soft reset
0x118	Clock fine delay	Clock Fine Delay Adjust[7:0] Twos complement coded control to adjust the fine sample clock skew in ~1.7 ps steps ≤−88 = −151.7 ps skew −87 = −150.0 ps skew … 0 = 0 ps skew … ≥ +87 = +150 ps skew								0x00	Used in conjunction with Reg. 0x117
0x11C	Clock status	0	0	0	0	0	0	0	0 = no input clock detected 1 = input clock detected	0x00	Read only
0x120	SYNC± Control 1	0	0	0	SYNC± transition select 0 = low to high 1 = high to low	CLK± edge select 0 = rising 1 = falling	SYNC± mode select 00 = disabled 01 = continuous 10 = N shot		0	0x00	
0x121	SYNC± Control 2	0	0	0	0	SYNC± N-shot ignore counter select 0000 = next SYNC± only 0001 = ignore the first SYNC± transitions 0010 = ignore the first two SYNC± transitions … 1111 = ignore the first 16 SYNC± transitions				0x00	Mode select (Reg. 0x120, Bits[2:1]) must be N-shot

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x128	SYNC± Status 1	SYNC± hold status See Table 37				SYNC± setup status See Table 37					Read only
0x129	SYNC± and clock divider status	0	0	0	0	Clock divider phase when SYNC± is captured 0000 = in phase 0001 = SYNC ± is ½ cycle delayed from clock 0010 = SYNC ± is 1 cycle delayed from clock 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed					Read only
0x12A	SYNC± counter	SYNC± counter, Bits[7:0] increment when a SYNC± signal is captured									Read only
0x200	Chip application mode	0	0	Chip Q ignore 0 = normal (I/Q) 1 = ignore (I only)	0	Chip operating mode 0001 = DDC 0 on 0010 = DDC 0 and DDC 1 on 0011 = DDC 0, DDC 1, DDC 2, and DDC 3 on 0111 = NSR enabled (default) 1000 = VDR enabled				0x07	
0x201	Chip decimation ratio	0	0	0	0	0	Chip decimation ratio select 000 = decimate by 1 001 = decimate by 2 010 = decimate by 4 011 = decimate by 8 100 = decimate by 16			0x00	
0x228	Customer offset	Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	
0x245	Fast detect (FD) control (local)	0	0	0	0	Force FD_A/ FD_B pins 0 = normal function 1 = force to value	Force value of FD_A/ FD_B pins; if force pins is true, this value is output on FD_x pins	0	Enable fast detect output	0x00	
0x247	FD upper threshold LSB (local)	Fast Detect Upper Threshold[7:0]								0x00	
0x248	FD upper threshold MSB (local)	0	0	0	Fast Detect Upper Threshold[12:8]					0x00	
0x249	FD lower threshold LSB (local)	Fast Detect Lower Threshold[7:0]								0x00	
0x24A	FD lower threshold MSB (local)	0	0	0	Fast Detect Lower Threshold[12:8]					0x00	
0x24B	FD dwell time LSB (local)	Fast Detect Dwell Time[7:0]								0x00	
0x24C	FD dwell time MSB (local)	Fast Detect Dwell Time[15:8]								0x00	
0x26F	Signal monitor synchronization control	0	0	0	0	0	0	Synchronization mode 00 = disabled 01 = continuous 11 = one-shot		0x00	See the Signal Monitor section
0x270	Signal monitor control (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x271	Signal Monitor Period Register 0 (local)	Signal Monitor Period[7:1]							0	0x80	In decimated output clock cycles
0x272	Signal Monitor Period Register 1 (local)	Signal Monitor Period[15:8]								0x00	In decimated output clock cycles
0x273	Signal Monitor Period Register 2 (local)	Signal Monitor Period[23:16]								0x00	In decimated output clock cycles
0x274	Signal monitor result control (local)	0	0	0	Result update 1 = update results (self clear)	0	0	0	Result selection 0 = Reserved 1 = peak detector	0x01	
0x275	Signal Monitor Result Register 0 (local)	Signal Monitor Result[7:0] When Register 0x0274, Bit 0 = 1, Result Bits[19:7] = Peak Detector Absolute Value[12:0]; Result Bits[6:0] = 0									Read only, updated based on Reg. 0x274, Bit 4
0x276	Signal Monitor Result Register 1 (local)	Signal Monitor Result[15:8]									Read only, updated based on Reg. 0x274, Bit 4
0x277	Signal Monitor Result Register 1 (local)	0	0	0	0	Signal Monitor Result[19:16]					Read only, updated based on Reg. 0x274, Bit 4
0x278	Signal monitor period counter result (local)	Period Count Result[7:0]									Read only, updated based on Reg 0x274, Bit 4
Digital Downconverter (DDC) Function Registers—See the Digital Downconverter (DDC) Section											
0x300	DDC synchronization control	0	0	0	DDC NCO soft reset 0 = normal operation 1 = reset	0	0	Synchronization mode 00 = disabled 01 = continuous 11 = one shot		0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x310	DDC 0 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_{ADC}/4 Hz IF mode (f_{ADC}/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x311	DDC 0 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x314	DDC 0 frequency LSB	DDC 0 NCO FTW[7:0], twos complement								0x00	
0x315	DDC 0 frequency MSB	X	X	X	X	DDC 0 NCO FTW[11:8], twos complement				0x00	
0x320	DDC 0 phase LSB	DDC 0 NCO POW[7:0], twos complement								0x00	
0x321	DDC 0 phase MSB	X	X	X	X	DDC 0 NCO POW[11:8], twos complement				0x00	
0x327	DDC 0 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
0x330	DDC 1 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_{ADC}/4 Hz IF mode (f_{ADC}/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x331	DDC 1 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x05	
0x334	DDC 1 frequency LSB	DDC 1 NCO FTW[7:0], twos complement								0x00	
0x335	DDC 1 frequency MSB	X	X	X	X	DDC1 NCO FTW[11:8], twos complement				0x00	
0x340	DDC 1 phase LSB	DDC 1 NCO POW[7:0], twos complement								0x00	
0x341	DDC 1 phase MSB	X	X	X	X	DDC1 NCO POW[11:8], twos complement				0x00	
0x347	DDC 1 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x350	DDC 2 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_{ADC}/4 Hz IF mode (f_{ADC}/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x351	DDC 2 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x354	DDC 2 frequency LSB	DDC 2 NCO FTW[7:0], twos complement								0x00	
0x355	DDC 2 frequency MSB	X	X	X	X	DDC 2 NCO FTW[11:8], twos complement				0x00	
0x360	DDC 2 phase LSB	DDC 2 NCO POW[7:0], twos complement								0x00	
0x361	DDC 2 phase MSB	X	X	X	X	DDC 2 NCO POW[11:8], twos complement				0x00	
0x367	DDC 2 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
0x370	DDC 3 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = f_{ADC}/4 Hz IF mode (f_{ADC}/4 downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x371	DDC 3 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x05	
0x374	DDC 3 frequency LSB	DDC 3 NCO FTW[7:0], twos complement								0x00	
0x375	DDC 3 frequency MSB	X	X	X	X	DDC 3 NCO FTW[11:8], twos complement				0x00	
0x380	DDC 3 phase LSB	DDC 3 NCO POW[7:0], twos complement								0x00	
0x381	DDC 3 phase MSB	X	X	X	X	DDC 3 NCO POW[11:8], twos complement				0x00	
0x387	DDC 3 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Ch. B	0	I output test mode enable 0 = disabled 1 = enabled from Ch. A	0x00	
NSR Decimate by 2 and Noise Shaping Requantizer (NSR)											

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x41E	NSR decimate by 2	High-pass filter (HPF)/ low-pass filter mode 0 = enable LPF 1 = enable HPF	X	0	0	X	X	X	NSR decimate by 2 enable 0 = disabled 1 = enabled	0x00	
0x420	NSR mode	X	X	X	X	NSR mode 000 = 21% BW mode 001 = 28% BW mode			X	0x00	
0x422	NSR tuning	X	X	NSR tuning word; see the Noise Shaping Requantizer (NSR) section; equations for the tuning word are dependent on the NSR mode						0x00	
Variable Dynamic Range (VDR)											
0x430	VDR control	X	X	X	0	X	X	VDR BW mode 0 = 25% BW mode 1 = 43% BW mode (only available for dual complex mode)	0 = dual real mode 1 = dual complex mode (Channel A = I, Channel B = Q)	0x01	
0x434	VDR tuning	X	X	X	X	VDR center frequency; see the Variable Dynamic Range (VDR) section for more details on the center frequency, which is dependent on the VDR mode				0x00	
Digital Outputs and Test Modes											
0x550	ADC test modes (local)	User pattern selection 0 = contin-uous repeat 1 = single pattern	0	Reset PN long gen 0 = long PN enable 1 = long PN reset	Reset PN short gen 0 = short PN enable 1 = short PN reset	Test mode selection 0000 = off (normal operation) 0001 = midscale short 0010 = positive full scale 0011 = negative full scale 0100 = alternating checkerboard 0101 = PN sequence, long 0110 = PN sequence, short 0111 = 1/0 word toggle 1000 = user pattern test mode (used with Register 0x550, Bit 7, and User Pattern 1 to User Pattern 4 registers) 1111 = ramp output				0x00	
0x551	User Pattern 1 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550
0x552	User Pattern 1 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550
0x553	User Pattern 2 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550
0x554	User Pattern 2 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x555	User Pattern 3 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550
0x556	User Pattern 3 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550
0x557	User Pattern 4 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550
0x558	User Pattern 4 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550
0x559	Output Mode Control 1	0	0	0	0	0	Status bit selection 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit 011 = fast detect (FD) bit or VDR punish bit 100 = VDR high/low resolution bit 101 = system reference			0x00	
0x561	Output format	0	0	0	0	0	Sample invert 0 = normal 1 = sample invert	Data format select 00 = offset binary 01 = twos complement (default)		0x01	
0x562	Output overrange (OR) clear	Virtual Converter 7 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 6 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 5 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 4 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 3 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 2 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 1 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 0 OR 0 = OR bit enabled 1 = OR bit cleared	0x00	
0x563	Output overrange status	Virtual Converter 7 OR 0 = no OR 1 = OR occurred	Virtual Converter 6 OR 0 = no OR 1 = OR occurred	Virtual Converter 5 OR 0 = no OR 1 = OR occurred	Virtual Converter 4 OR 0 = no OR 1 = OR occurred	Virtual Converter 3 OR 0 = no OR 1 = OR occurred	Virtual Converter 2 OR 0 = no OR 1 = OR occurred	Virtual Converter 1 OR 0 = no OR 1 = OR occurred	Virtual Converter 0 OR 0 = no OR 1 = OR occurred	0x00	Read only
0x564	Output channel select	0	0	0	0	0	0	0	Converter channel swap 0 = normal channel ordering 1 = channel swap enabled	0x00	

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x568	Output mode	0	0	Frame clock mode (only used when in output data mode is in byte mode) 00 = frame clock always off 01 = frame clock always on 10 = reserved 11 = frame clock conditionally on based on PN23 sequence		0	Output data mode 000 = parallel interleaved mode (one virtual converter) 001 = parallel interleaved mode (two virtual converters) 010 = channel multiplexed (even/odd) mode (one virtual converter) 011 = channel multiplexed (even/odd) mode (two virtual converters) 100 = byte mode (one virtual converter) 101 = byte mode (two virtual converters) 110 = byte mode (four virtual converters) 111 = byte mode (eight virtual converters)				
0x569	DCO output delay	0	0	0	0	0	0	DCO clock delay 00 = 0° 01 = 90° (available when DCO rate is less than sample clock rate) 10 = 180° 11 = 270° (available when DCO rate is less than sample clock rate)		0x01	
0x56A	Output adjust	0	1	0	0	LVDS output drive current adjust 000 = 2 mA 001 = 2.25 mA 010 = 2.5 mA 011 = 2.75 mA 100 = 3.0 mA 101 = 3.25 mA 110 = 3.5 mA (default) 111 = 3.75 mA			0	0x4C	
0x56B	Output slew rate adjust	0	0	0	0	0	0	Output slew rate control 00 = 80 ps 01 = 150 ps 10 = 200 ps 11 = 250 ps		0x00	

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD6679 must be powered by the following six supplies: AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V. For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the ADP2164 and ADP2370 switching regulators be used to convert the 3.3 V, 5.0 V, or 12 V input rails to an intermediate rail (1.8 V and 3.8 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators (ADP1741, ADM7172, and ADP125). Figure 87 shows the recommended method. For more detailed information on the recommended power solution, see the AD6679 evaluation board wiki, *Evaluating the AD6679 IF Diversity Receiver*.

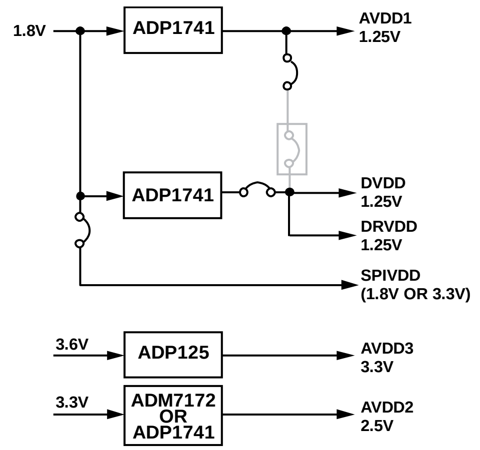
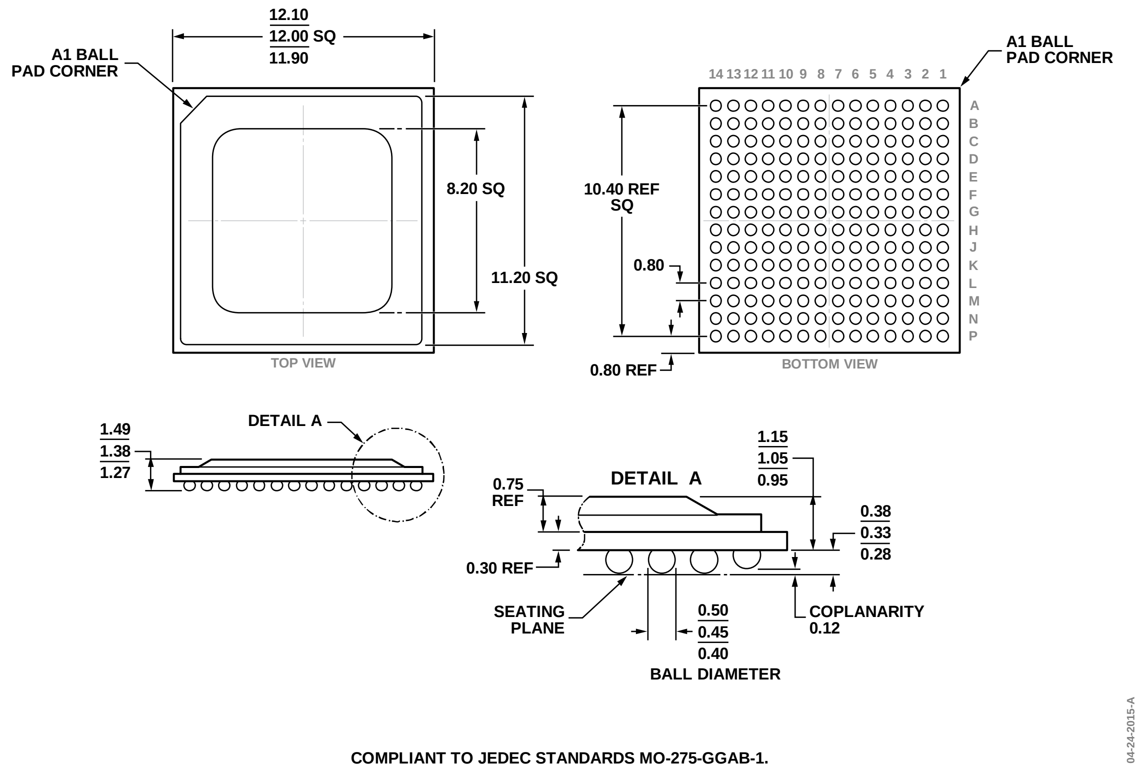


Figure 87. High Efficiency, Low Noise Power Solution for the AD6679

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 87 provides the lowest noise, highest efficiency power delivery system for the AD6679. If only one 1.25 V supply is available, it must be routed to AVDD1 first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for SPIVDD, DVDD, and DRVDD, in that order. The user can use several different decoupling capacitors to cover both high and low frequencies. These capacitors must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-GGAB-1.

Figure 88. 196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-196-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD6679BBPZ-500	−40°C to +85°C	196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-196-3
AD6679BBPZRL7-500	−40°C to +85°C	196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-196-3
AD6679-500EBZ		Evaluation Board for AD6679-500	

[1] Z = RoHS Compliant Part.

D13059-0-4/16(B)

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