2-/4-/8-Channel, 1 MSPS, Ultralow Power, 12-Bit SAR ADC

Data Sheet

AD7091R-2/AD7091R-4/AD7091R-8

FEATURES

- Ultralow system power
  - Flexible power/throughput rate management
  - Normal mode
    - 1.4 mW at 1 MSPS
  - Power-down mode
    - 550 nA typical at V_{DD} = 5.25 V
    - 435 nA typical at V_{DD} = 3 V
  - Programmable ALERT interrupt pin (4-/8-channel models)
- High performance
  - 1 MSPS throughput with no latency/pipeline delay
  - SNR: 70 dB typical at 10 kHz input frequency
  - THD: −80 dB typical at 10 kHz input frequency
  - INL: ±0.7 LSB typical, ±1.0 LSB maximum
- Small system footprint
  - On-chip accurate 2.5 V reference, 5 ppm/°C typical drift
  - MUX_{OUT}/ADC_{IN} to allow single buffer amplifier
  - Daisy-chain mode
  - 16-lead, 20-lead, and 24-lead 4 mm × 4 mm LFCSP packages
  - 16-lead, 20-lead, and 24-lead TSSOP packages
- Easy to use
  - SPI/QSPI™/MICROWIRE™/DSP compatible digital interface
  - Integrated programmable channel sequencer
  - BUSY indication available (4-/8-channel models)
- Built in features for control and monitoring applications
  - GPOx pins available (4-/8-channel models)
- Wide operating range
  - Temperature range: −40°C to +125°C
  - Specified for V_{DD} of 2.7 V to 5.25 V

APPLICATIONS

- Battery-powered systems
- Personal digital assistants
- Medical instruments
- Mobile communications
- Instrumentation and control systems
- Data acquisition systems
- Optical sensors
- Diagnostic/monitoring functions

FUNCTIONAL BLOCK DIAGRAM

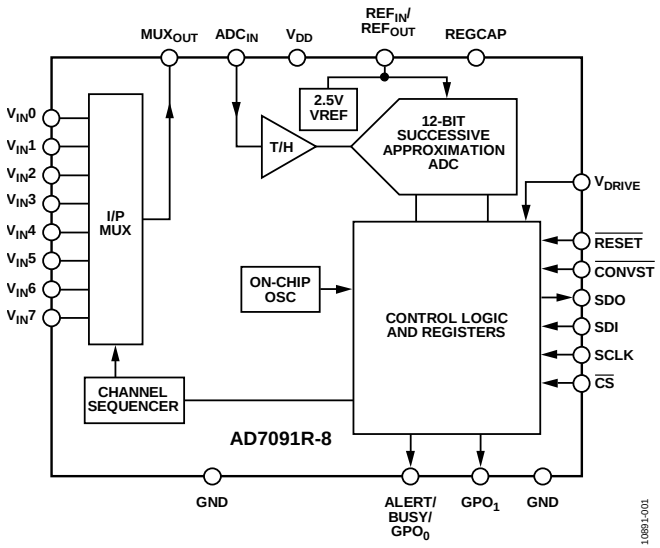

Figure 1.

GENERAL DESCRIPTION

The AD7091R-2/AD7091R-4/AD7091R-8 family is a multichannel 12-bit, ultralow power, successive approximation analog-to-digital converter (ADC) that is available in two, four, or eight analog input channel options. The AD7091R-2/AD7091R-4/AD7091R-8 operate from a single 2.7 V to 5.25 V power supply and are capable of achieving a sampling rate of 1 MSPS.

The AD7091R-2/AD7091R-4/AD7091R-8 family offers up to eight single-ended analog input channels with a channel sequencer that allows a preprogrammed selection of channels to be converted sequentially. The AD7091R-2/AD7091R-4/ AD7091R-8 also feature an on-chip conversion clock, an on-chip accurate 2.5 V reference, and a high speed serial interface.

The AD7091R-2/AD7091R-4/AD7091R-8 have a serial port interface (SPI) that allows data to be read after the conversion while achieving a 1 MSPS throughput rate. The conversion process and data acquisition are controlled using the $\overline{\text{CONVST}}$ pin.

The AD7091R-2/AD7091R-4/AD7091R-8 use advanced design techniques to achieve ultralow power dissipation at high throughput rates. They also feature flexible power management options. An on-chip configuration register allows the user to set up different operating conditions. These include power management, alert functionality, busy indication, channel sequencing, and general-purpose output pins. The MUX_{OUT} and ADC_{IN} pins allow signal conditioning of the multiplexer output prior to acquisition by the ADC.

Rev. C
Document Feedback

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7/14—Rev. 0 to Rev. A

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SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, V_{DRIVE} = 1.8 V to 5.25 V, V_{REF} = 2.5 V internal reference, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 50 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 10 kHz sine wave				
Signal-to-Noise Ratio (SNR)		66.5	70		dB
Signal-to-Noise-and-Distortion (SINAD) Ratio		65.5	69		dB
Total Harmonic Distortion (THD)			−80		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1 kHz sine wave		−81		dB
Channel-to-Channel Isolation			−95		dB
Aperture Delay			5		ns
Aperture Jitter			40		ps
Full Power Bandwidth	At −3 dB		1.5		MHz
	At −0.1 dB		1.2		MHz
DC ACCURACY					
Resolution		12			Bits
Integral Nonlinearity (INL)	V_{DD} ≥ 3.0 V	−1	±0.7	+1	LSB
	V_{DD} ≥ 2.7 V	−1.25	±0.8	+1.25	LSB
Differential Nonlinearity (DNL)	Guaranteed no missing codes to 12 bits	−0.9	±0.3	+0.9	LSB
Offset Error	T_A = 25°C	−1.5	0.2	+1.5	mV
Offset Error Matching	T_A = 25°C	−1.5	0.2	+1.5	mV
Offset Error Drift			2		ppm/°C
Gain Error	T_A = 25°C	−0.1	0.0	+0.1	% FS
Gain Error Matching	T_A = 25°C	−0.1	0.0	+0.1	% FS
Gain Error Drift			2		ppm/°C
ANALOG INPUT					
Input Voltage Range[1]	At ADC_{IN}	0		V_{REF}	V
DC Leakage Current		−1		+1	µA
Input Capacitance[2]	During acquisition phase		10		pF
	Outside acquisition phase		1.5		pF
Multiplexer On Resistance	V_{DD} = 5.0 V		50		Ω
	V_{DD} = 2.5 V		100		Ω
VOLTAGE REFERENCE INPUT/OUTPUT					
REF_{OUT}[3]	Internal reference output, T_A = 25°C	2.49	2.5	2.51	V
REF_{IN}[3]	External reference input	1.0		V_{DD}	V
Drift			5		ppm/°C
Power-On Time	C_{REF} = 2.2 µF		50		ms
LOGIC INPUTS					
Input High Voltage (V_{IH})		0.7 × V_{DRIVE}			V
Input Low Voltage (V_{IL})				0.3 × V_{DRIVE}	V
Input Current (I_{IN})	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}	−1		+1	µA
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	I_{SOURCE} = 200 µA	V_{DRIVE} − 0.2			V
Output Low Voltage (V_{OL})	I_{SINK} = 200 µA			0.4	V
Floating State Leakage Current		−1		+1	µA
Output Coding		Straight (natural) binary			

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CONVERSION RATE					
Conversion Time				600	ns
Transient Response	Full-scale step input			400	ns
Throughput Rate				1	MSPS
POWER REQUIREMENTS					
V_{DD}		2.7		5.25	V
V_{DRIVE}	Specified performance	2.7		5.25	V
V_{DRIVE} Range[4]	Functional	1.8		5.25	V
I_{DD}	V_{IN} = 0 V				
Normal Mode—Static[5]	V_{DD} = 5.25 V		22	50	µA
	V_{DD} = 3 V		21.6	46	µA
Normal Mode—Operational	V_{DD} = 5.25 V, f_{SAMPLE} = 1 MSPS		500	570	µA
	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS		450	530	µA
Power-Down Mode	V_{DD} = 5.25 V		0.550	17	µA
	V_{DD} = 5.25 V, T_A = −40°C to +85°C		0.550	6	µA
	V_{DD} = 3 V		0.435	15	µA
I_{DRIVE}	V_{IN} = 0 V				
Normal Mode—Static[6]	V_{DRIVE} = 5.25 V		2	4	µA
	V_{DRIVE} = 3 V		1	3.5	µA
Normal Mode—Operational	V_{DRIVE} = 5.25 V, f_{SAMPLE} = 1 MSPS		30	70	µA
	V_{DRIVE} = 3 V, f_{SAMPLE} = 1 MSPS		10	15	µA
Power-Down Mode	V_{DRIVE} = 5.25 V			1	µA
	V_{DRIVE} = 3 V			1	µA
Total Power Dissipation[7]	V_{IN} = 0 V				
Normal Mode—Static	V_{DD} = V_{DRIVE} = 5.25 V		0.130	0.290	mW
	V_{DD} = V_{DRIVE} = 3 V		0.070	0.149	mW
Normal Mode—Operational	V_{DD} = V_{DRIVE} = 5.25 V, f_{SAMPLE} = 1 MSPS		2.8	3.4	mW
	V_{DD} = V_{DRIVE} = 3 V, f_{SAMPLE} = 1 MSPS		1.4	1.7	mW
	V_{DD} = V_{DRIVE} = 3 V, f_{SAMPLE} = 100 SPS		0.080		mW
Power-Down Mode	V_{DD} = 5.25 V		3	95	µW
	V_{DD} = 5.25 V, T_A = −40°C to +85°C		3	33	µW
	V_{DD} = V_{DRIVE} = 3 V		1.4	50	µW

[1] Multiplexer input voltage should not exceed V_{DD}.
[2] Sample tested during initial release to ensure compliance.
[3] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configurations and Function Descriptions section.
[4] Device is functional and meets dynamic performance/dc accuracy specifications with V_{DRIVE} down to 1.8 V, but the device is not capable of achieving a throughput of 1 MSPS.
[5] SCLK operates in burst mode, and $\overline{CS}$ idles high. With a free running SCLK and $\overline{CS}$ pulled low, the I_{DD} static current is increased by 30 µA typical at V_{DD} = 5.25 V.
[6] SCLK operates in burst mode, and $\overline{CS}$ idles high. With a free running SCLK and $\overline{CS}$ pulled low, the I_{DRIVE} static current is increased by 32 µA typical at V_{DRIVE} = 5.25 V.
[7] Total power dissipation includes contributions from V_{DD}, V_{DRIVE}, and REF_{IN} (see Note 2).

TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, V_{DRIVE} = 1.8 V to 5.25 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: $\overline{CONVST}$ Falling Edge to Data Available	$t_{CONVERT}$			600	ns
Acquisition Time	t_{ACQ}	400			ns
Time Between Conversions (Normal Mode)	t_{CYC}	1000			ns
$\overline{CONVST}$ Pulse Width	t_{CNVPW}	10		500	ns
SCLK Period (Normal Mode)	t_{SCLK}				
V_{DRIVE} Above 2.7 V		16			ns
V_{DRIVE} Above 1.8 V		22			ns
SCLK Period (Chain Mode)	t_{SCLK}				
V_{DRIVE} Above 2.7 V		20			ns
V_{DRIVE} Above 1.8 V		25			ns
SCLK Low Time	t_{SCLKL}	6			ns
SCLK High Time	t_{SCLKH}	6			ns
SCLK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCLK Falling Edge to Data Valid Delay	t_{DSDO}				
V_{DRIVE} Above 4.5 V				12	ns
V_{DRIVE} Above 3.3 V				13	ns
V_{DRIVE} Above 2.7 V				14	ns
V_{DRIVE} Above 1.8 V				20	ns
End of Conversion to $\overline{CS}$ Falling Edge	t_{EOCCSL}	5			ns
$\overline{CS}$ Low to SDO Enabled	t_{EN}			5	ns
$\overline{CS}$ High or Last SCLK Falling Edge to SDO High Impedance	t_{DIS}			5	ns
SDI Data Setup Time Prior to SCLK Rising Edge	$t_{SSDISCLK}$	5			ns
SDI Data Hold Time After SCLK Rising Edge	$t_{HSDISCLK}$	2			ns
Last SCLK Falling Edge to Next $\overline{CONVST}$ Falling Edge	t_{QUIET}	50			ns
$\overline{RESET}$ Pulse Width	$t_{RESETPW}$	10			ns
$\overline{RESET}$ Pulse Delay Upon Power Up	t_{RESET_DELAY}	50			ns
Time Between Conversions (Power On Software Reset)	t_{CYC_RESET}	2			µs

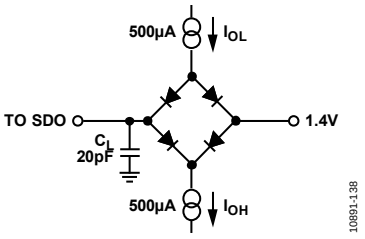


Figure 2. Load Circuit for Digital Interface Timing

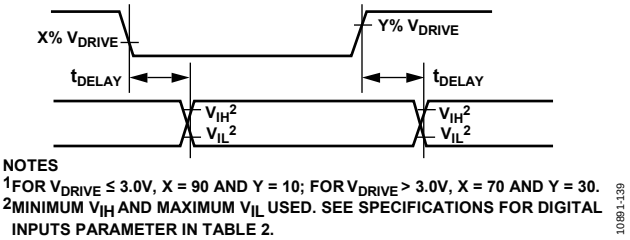


Figure 3. Voltage Levels for Timing

Timing Diagram

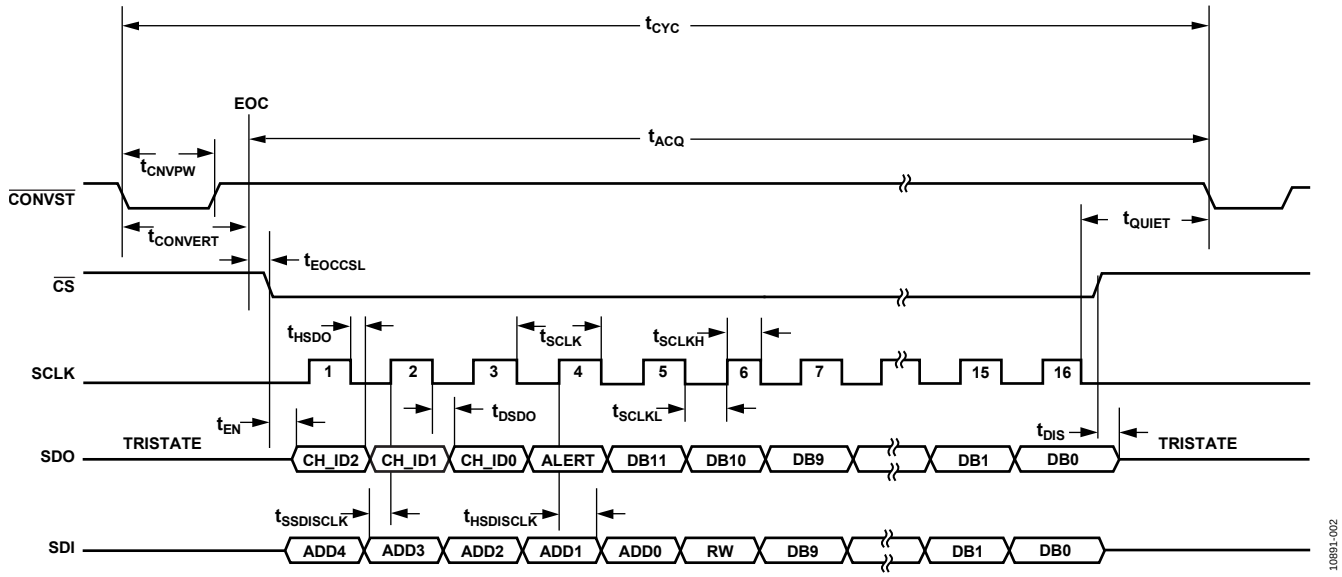


Figure 4. Serial Port Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{DRIVE} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{REF} + 0.3 V
Digital Input[1] Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output[2] Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Input Current to Any Pin Except Supplies[3]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD	
Human Body Model (HBM)	1.5 kV
Field Induced Charged Device Model (FICDM)	500 V

[1] The digital input pins include the following: $\overline{\text{RESET}}$, $\overline{\text{CONVST}}$, SDI, SCLK, and $\overline{\text{CS}}$.

[2] The digital output pins include the following: SDO, GPO_1, and ALERT/BUSY/GPO_0.

[3] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead LFCSP	47.3	27.78	°C/W
24-Lead TSSOP	73.54	14.94	°C/W
20-Lead LFCSP	49.05	29.18	°C/W
20-Lead TSSOP	84.29	18.43	°C/W
16-Lead LFCSP	50.58	29.64	°C/W
16-Lead TSSOP	106.03	28.31	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

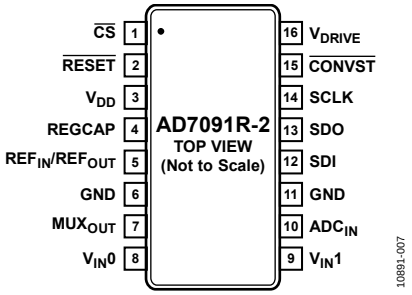


Figure 5. 2-Channel, 16-Lead TSSOP Pin Configuration

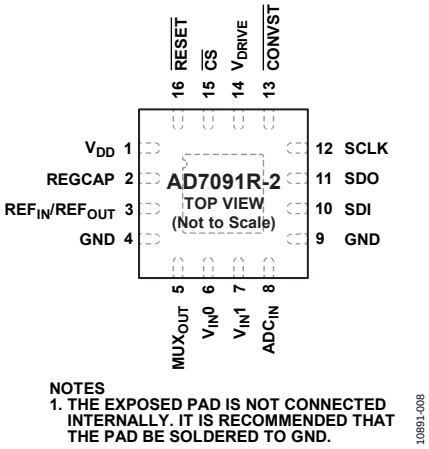


Figure 6. 2-Channel, 16-Lead LFCSP Pin Configuration

Table 5. 2-Channel, 16-Lead LFCSP and 16-Lead TSSOP Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	$\overline{CS}$	Chip Select Input. When $\overline{CS}$ is held low, the serial bus enables, and $\overline{CS}$ frames the output data on the SPI.
2	16	$\overline{RESET}$	Reset. Logic input.
3	1	V_{DD}	Power Supply Input. The V_{DD} range is from 2.7 V to 5.25 V. Decouple this supply pin to GND.
4	2	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple this output pin separately to GND using a 1.0 µF capacitor.
5	3	REF_{IN}/REF_{OUT}	Voltage Reference Output, 2.5 V. Decouple this pin to GND. Typical recommended decoupling capacitor value is 2.2 µF. The user can either access the internal 2.5 V reference or overdrive the internal reference with the voltage applied to this pin. The reference voltage range for an externally applied reference is 1.0 V to V_{DD}.
6, 11	4, 9	GND	Chip Ground Pins. These pins are the ground reference point for all circuitry on the AD7091R-2.
7	5	MUX_{OUT}	Multiplexer Output. The output of the multiplexer appears at this pin. If no external filtering or buffering is required, tie this pin directly to the ADC_{IN} pin; otherwise, tie the output of the conditioning network to the ADC_{IN} pin.
8	6	$V_{IN}0$	Analog Input 0. Single-ended analog input. The analog input range is 0 V to V_{REF}.
9	7	$V_{IN}1$	Analog Input 1. Single-ended analog input. The analog input range is 0 V to V_{REF}.
10	8	ADC_{IN}	ADC Input. This pin allows access to the on-chip track-and-hold. If no external filtering or buffering is required, tie this pin directly to the MUX_{OUT} pin; otherwise tie the input of the conditioning network to the MUX_{OUT} pin.
12	10	SDI	Serial Data Input Bus. This input provides the data written to the on-chip control registers. Data clocks into the registers on the falling edge of the SCLK input. Provide data MSBs first.
13	11	SDO	Serial Data Output Bus. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 13 SCLKs are required to access the data. The data is provided MSB first.
14	12	SCLK	Serial Clock. This pin acts as the serial clock input.
15	13	$\overline{CONVST}$	Convert Start Input Signal. Edge triggered logic input. The falling edge of $\overline{CONVST}$ places the track-and-hold mode into hold mode and initiates a conversion.
16	14	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Connect decoupling capacitors between V_{DRIVE} and GND. Typical recommended values are 10 µF and 0.1 µF. The voltage range on this pin is 1.8 V to 5.25 V and may be different to the voltage range at V_{DD}.
Not applicable	17	EPAD	Exposed Pad. The exposed pad is not connected internally. It is recommended that the pad be soldered to GND.

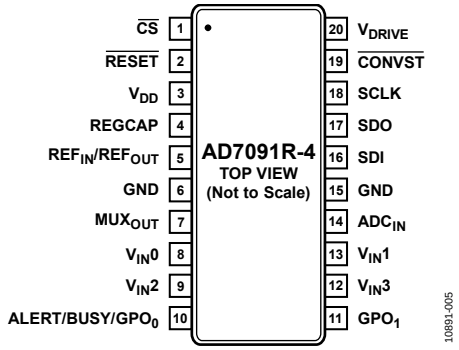


Figure 7. 4-Channel, 20-Lead TSSOP Pin Configuration

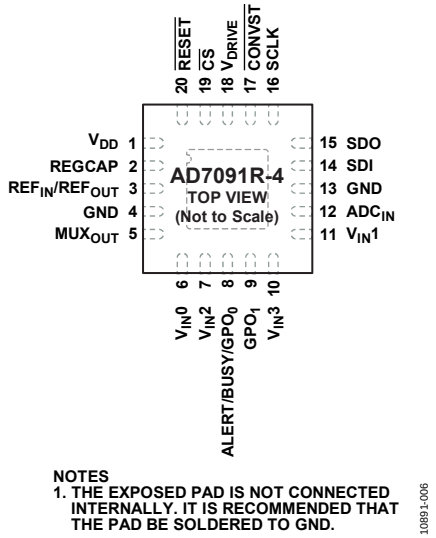


Figure 8. 4-Channel, 20-Lead LFCSP Pin Configuration

Table 6. 4-Channel, 20-Lead LFCSP and 20-Lead TSSOP Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	$\overline{CS}$	Chip Select Input. When $\overline{CS}$ is held low, the serial bus enables, and $\overline{CS}$ frames the output data on the SPI.
2	20	$\overline{RESET}$	Reset. Logic input.
3	1	V_{DD}	Power Supply Input. The V_{DD} range is from 2.7 V to 5.25 V. Decouple this supply pin to GND.
4	2	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple this output pin separately to GND using a 1.0 µF capacitor.
5	3	REF_{IN}/REF_{OUT}	Voltage Reference Output, 2.5 V. Decouple this pin to GND. Typical recommended decoupling capacitor value is 2.2 µF. The user can either access the internal 2.5 V reference or overdrive the internal reference with the voltage applied to this pin. The reference voltage range for an externally applied reference is 1.0 V to V_{DD}.
6, 15	4, 13	GND	Chip Ground Pins. These pins are the ground reference point for all circuitry on the AD7091R-4.
7	5	MUX_{OUT}	Multiplexer Output. The output of the multiplexer appears at this pin. If no external filtering or buffering is required, tie this pin directly to the ADC_{IN} pin; otherwise, tie the output of the conditioning network to the ADC_{IN} pin.
8	6	$V_{IN}0$	Analog Input 0. Single-ended analog input. The analog input range is 0 V to V_{REF}.
9	7	$V_{IN}2$	Analog Input 2. Single-ended analog input. The analog input range is 0 V to V_{REF}.
10	8	ALERT/BUSY/GPO_0	Alert Output Pin (ALERT). This is a multifunction pin determined by the configuration register. When functioning as ALERT, this pin is a logic output indicating that a conversion result has fallen outside the limit of the register settings. When the ALERT/BUSY/GPO_0 pin is configured as a BUSY output, use this pin to indicate when a conversion is taking place. The pin can also function as a general-purpose digital output.
11	9	GPO_1	General-Purpose Digital Output.
12	10	$V_{IN}3$	Analog Input 3. Single-ended analog input. The analog input range is 0 V to V_{REF}.
13	11	$V_{IN}1$	Analog Input 1. Single-ended analog input. The analog input range is 0 V to V_{REF}.
14	12	ADC_{IN}	ADC Input. This pin allows access to the on-chip track-and-hold. If no external filtering or buffering is required, tie this pin directly to the MUX_{OUT} pin; otherwise, tie the input of the conditioning network to the MUX_{OUT} pin.
16	14	SDI	Serial Data Input Bus. This input provides data written to the on-chip control registers. Data clocks into the registers on the falling edge of the SCLK input. Provide data MSB first.
17	15	SDO	Serial Data Output Bus. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 13 SCLKs are required to access the data. The data is provided MSB first.

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
18	16	SCLK	Serial Clock. This pin acts as the serial clock input.
19	17	$\overline{\text{CONVST}}$	Convert Start Input Signal. Edge triggered logic input. The falling edge of $\overline{\text{CONVST}}$ places the track-and-hold mode into hold mode and initiates a conversion.
20	18	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Connect decoupling capacitors between V_{DRIVE} and GND. Typical recommended values are 10 µF and 0.1 µF. The voltage range on this pin is 1.8 V to 5.25 V and may be different to the voltage range at V_{DD}.
Not applicable	21	EPAD	Exposed Pad. The exposed pad is not connected internally. It is recommended that the pad be soldered to GND.

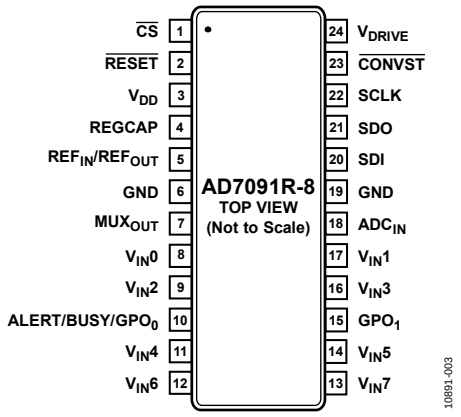


Figure 9. 8-Channel, 24-Lead TSSOP Pin Configuration

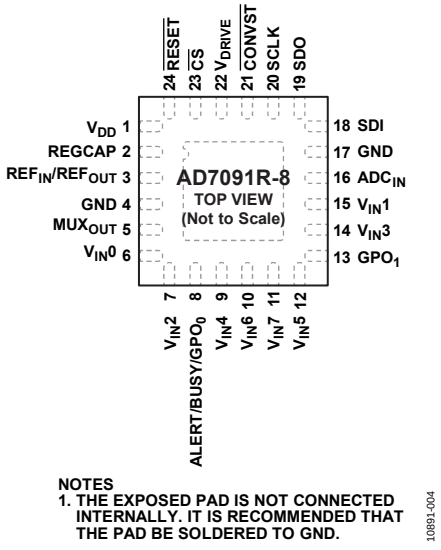


Figure 10. 8-Channel, 24-Lead LFCSP Pin Configuration

Table 7. 8-Channel, 24-Lead LFCSP and 24-Lead TSSOP Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	23	$\overline{CS}$	Chip Select Input. When $\overline{CS}$ is held low, the serial bus enables, and $\overline{CS}$ frames the output data on the SPI.
2	24	$\overline{RESET}$	Reset. Logic input.
3	1	V_{DD}	Power Supply Input. The V_{DD} range is from 2.7 V to 5.25 V. Decouple this supply pin to GND.
4	2	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple this output pin separately to GND using a 1.0 µF capacitor.
5	3	REF_{IN}/REF_{OUT}	Voltage Reference Output, 2.5 V. Decouple this pin to GND. Typical recommended decoupling capacitor value is 2.2 µF. The user can either access the internal 2.5 V reference or overdrive the internal reference with the voltage applied to this pin. The reference voltage range for an externally applied reference is 1.0 V to V_{DD}.
6, 19	4, 17	GND	Chip Ground Pins. These pins are the ground reference point for all circuitry on the AD7091R-8.
7	5	MUX_{OUT}	Multiplexer Output. The output of the multiplexer appears at this pin. If no external filtering or buffering is required, tie this pin directly to the ADC_{IN} pin; otherwise, tie the output of the conditioning network to the ADC_{IN} pin.
8	6	$V_{IN}0$	Analog Input 0. Single-ended analog input. The analog input range is 0 V to V_{REF}.
9	7	$V_{IN}2$	Analog Input 2. Single-ended analog input. The analog input range is 0 V to V_{REF}.
10	8	$ALERT/BUSY/GPO_0$	Alert Output Pin (ALERT). This is a multifunction pin determined by the configuration register. When functioning as ALERT, this pin is a logic output indicating that a conversion result has fallen outside the limit of the register settings. When the $ALERT/BUSY/GPO_0$ pin is configured as a BUSY output, use this pin to indicate when a conversion is taking place. The pin can also function as a general-purpose digital output.
11	9	$V_{IN}4$	Analog Input 4. Single-ended analog input. The analog input range is 0 V to V_{REF}.
12	10	$V_{IN}6$	Analog Input 6. Single-ended analog input. The analog input range is 0 V to V_{REF}.
13	11	$V_{IN}7$	Analog Input 7. Single-ended analog input. The analog input range is 0 V to V_{REF}.
14	12	$V_{IN}5$	Analog Input 5. Single-ended analog input. The analog input range is 0 V to V_{REF}.
15	13	GPO_1	General-Purpose Digital Output.
16	14	$V_{IN}3$	Analog Input 3. Single-ended analog input. The analog input range is 0 V to V_{REF}.
17	15	$V_{IN}1$	Analog Input 1. Single-ended analog input. The analog input range is 0 V to V_{REF}.
18	16	ADC_{IN}	ADC Input. This pin allows access to the on-chip track-and-hold. If no external filtering or buffering is required, tie this pin directly to the MUX_{OUT} pin; otherwise, tie the input of the conditioning network to the MUX_{OUT} pin.

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
20	18	SDI	Serial Data Input Bus. Data to be written to the on-chip control registers is provided on this input. Data is clocked into the registers on the falling edge of the SCLK input. Provide data MSB first.
21	19	SDO	Serial Data Output Bus. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 13 SCLKs are required to access the data. The data is provided MSB first.
22	20	SCLK	Serial Clock. This pin acts as the serial clock input.
23	21	$\overline{\text{CONVST}}$	Convert Start Input Signal. Edge triggered logic input. The falling edge of $\overline{\text{CONVST}}$ places the track-and-hold mode into hold mode and initiates a conversion.
24	22	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Connect decoupling capacitors between V_{DRIVE} and GND. Typical recommended values are 10 µF and 0.1 µF. The voltage range on this pin is 1.8 V to 5.25 V and may be different to the voltage range at V_{DD}.
Not applicable	25	EPAD	Exposed Pad. The exposed pad is not connected internally. It is recommended that the pad be soldered to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

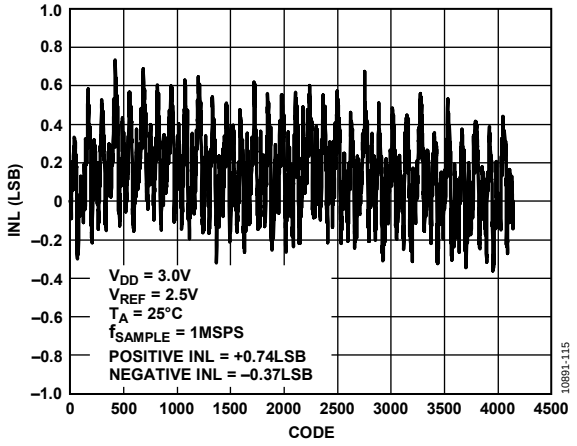


Figure 11. Integral Nonlinearity vs. Code

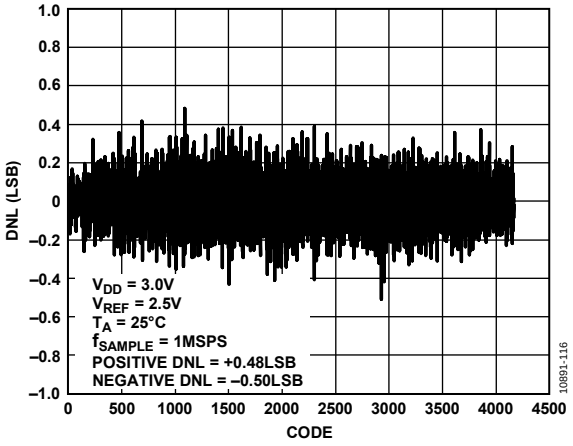


Figure 14. Differential Nonlinearity vs. Code

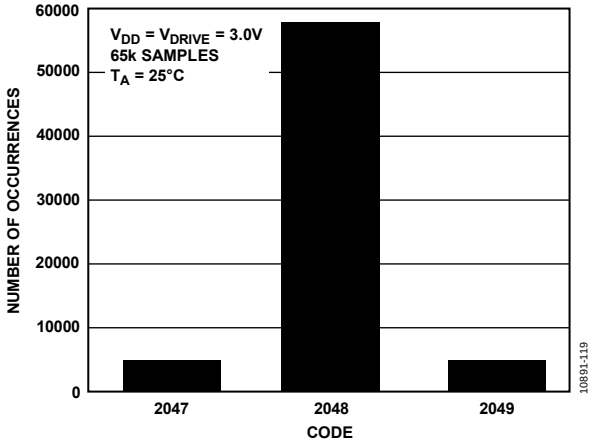


Figure 12. Histogram of a DC Input at Code Center

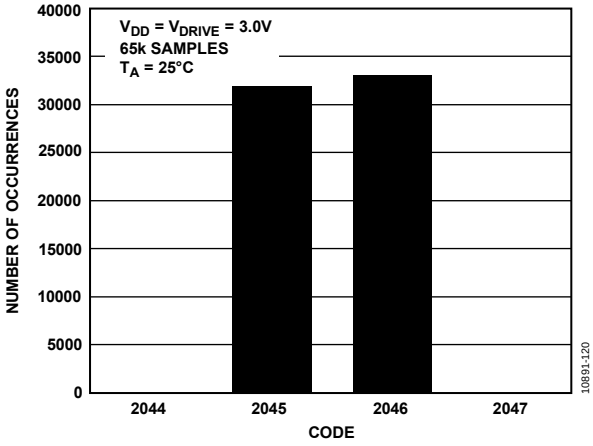


Figure 15. Histogram of a DC Input at Code Transition

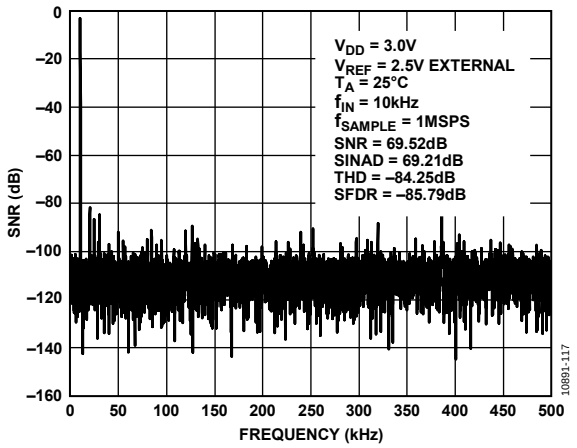


Figure 13. 10 kHz Fast Fourier Transform (FFT), V_{DD} = 3.0 V, V_{REF} = 2.5 V External

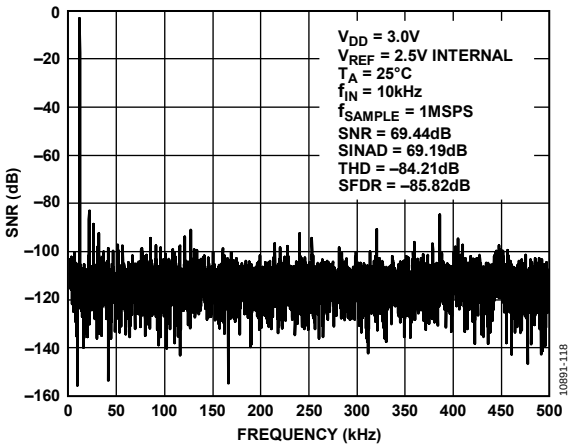


Figure 16. 10 kHz FFT, V_{DD} = 3.0 V, V_{REF} = 2.5 V Internal

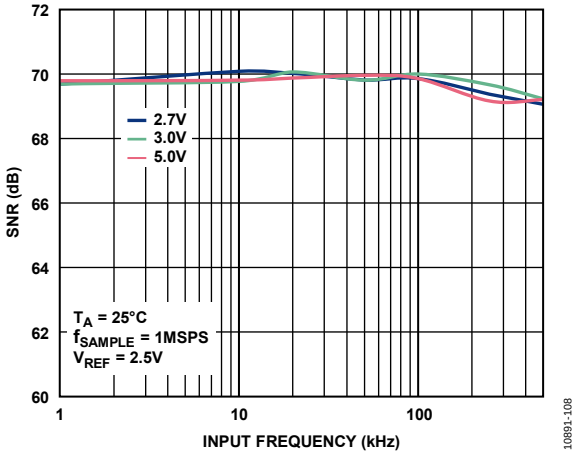


Figure 17. SNR vs. Analog Input Frequency for Various Supply Voltages

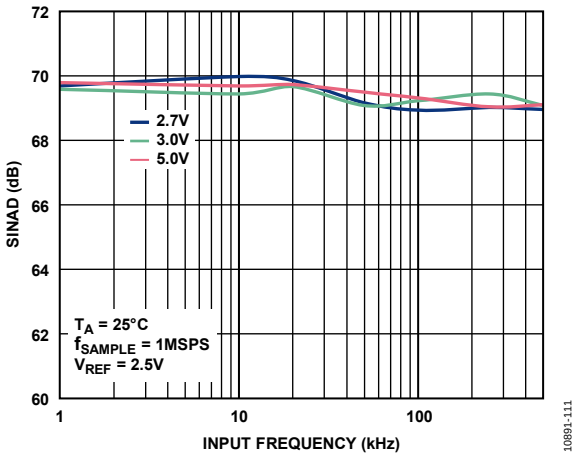


Figure 18. SINAD vs. Analog Input Frequency for Various Supply Voltages

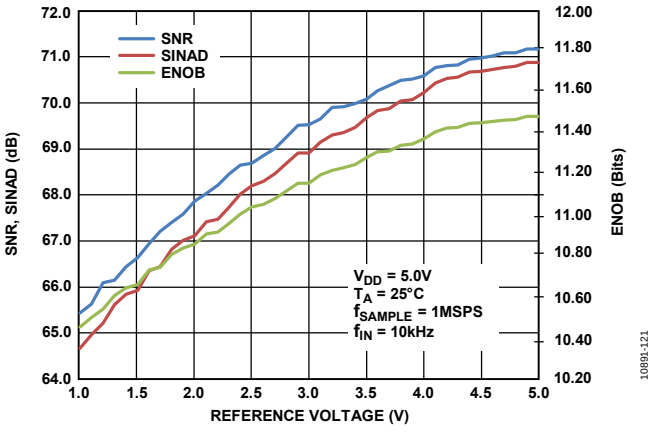


Figure 19. SNR, SINAD, and ENOB vs. Reference Voltage

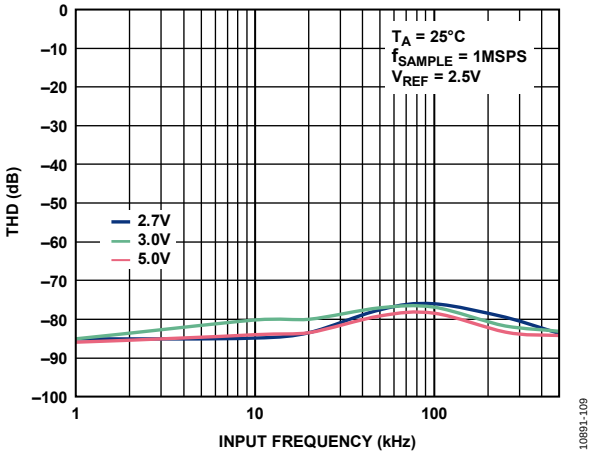


Figure 20. THD vs. Analog Input Frequency for Various Supply Voltages

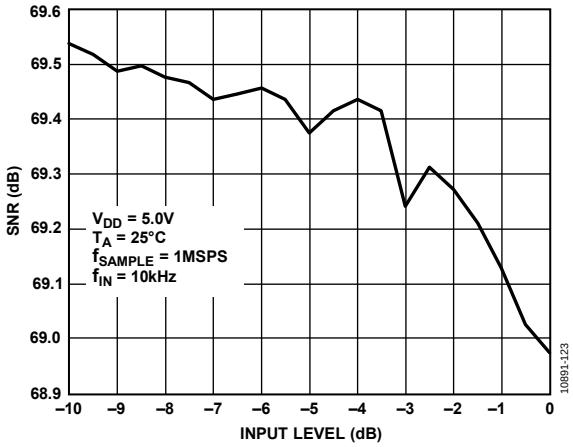


Figure 21. SNR vs. Input Level

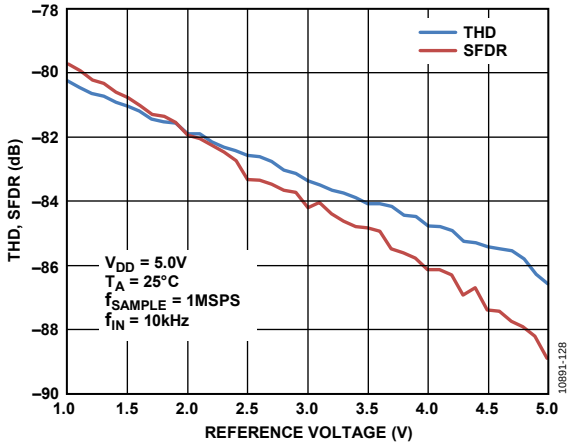


Figure 22. THD and SFDR vs. Reference Voltage

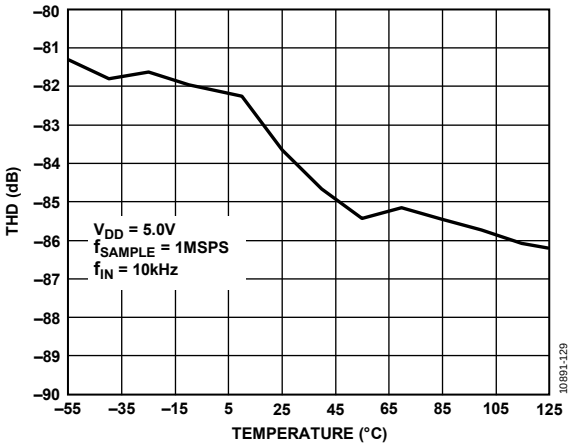


Figure 23. THD vs. Temperature

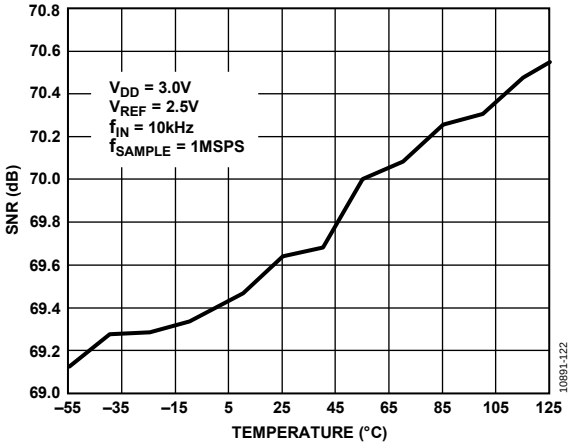


Figure 24. SNR vs. Temperature

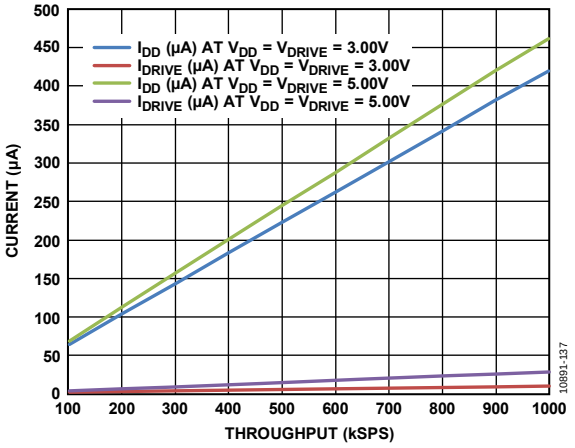


Figure 25. Operating Current vs. Throughput

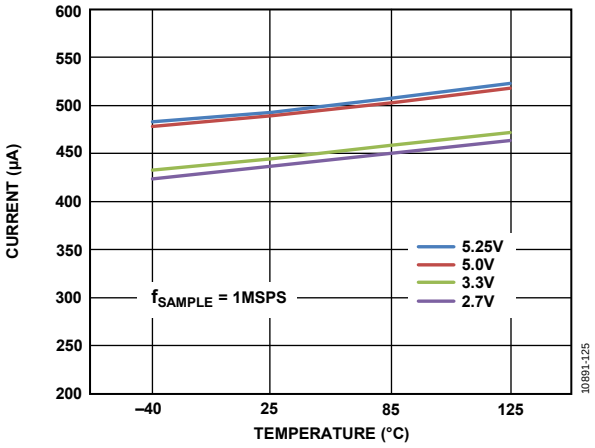


Figure 26. Operational I_{DD} Supply Current vs. Temperature for Various V_{DD} Supply Voltages

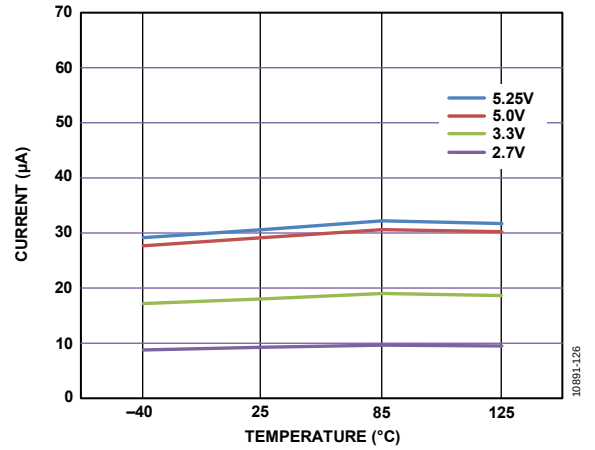


Figure 27. Operational I_{DRIVE} Supply Current vs. Temperature for Various V_{DRIVE} Supply Voltages

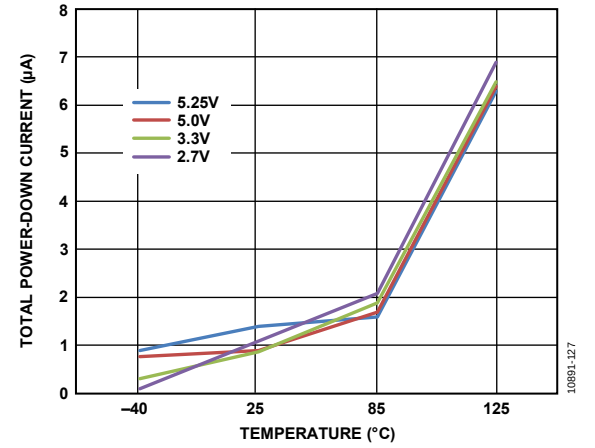


Figure 28. Total Power-Down Current vs. Temperature for Various Supplies

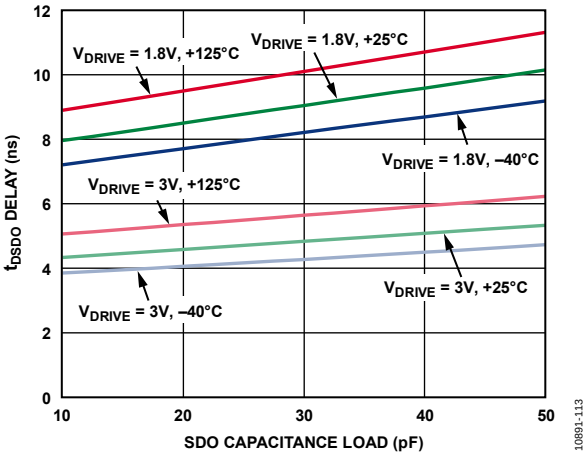


Figure 29. t_{DSDO} Delay vs. SDO Capacitance Load and Supply

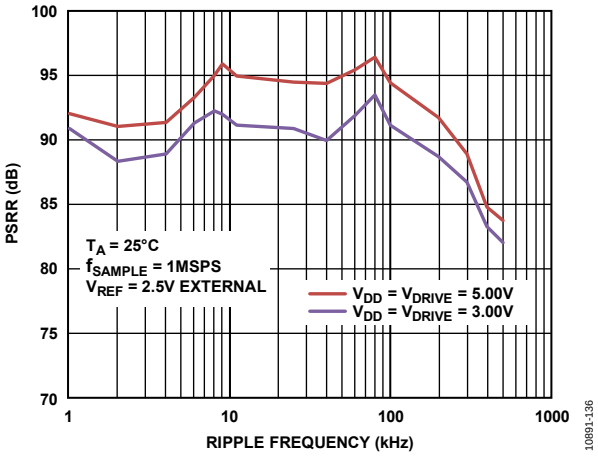


Figure 32. PSRR vs. Ripple Frequency

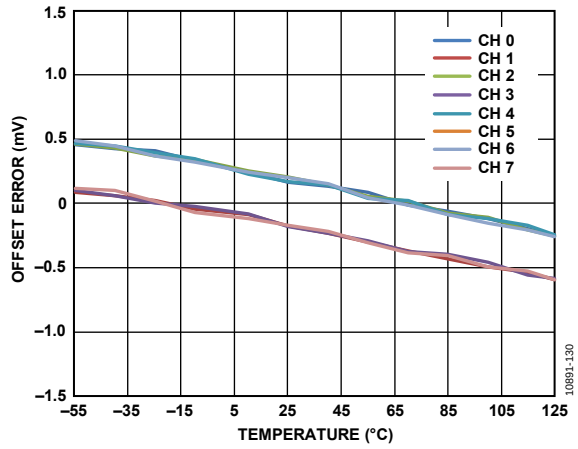


Figure 30. Offset Error vs. Temperature

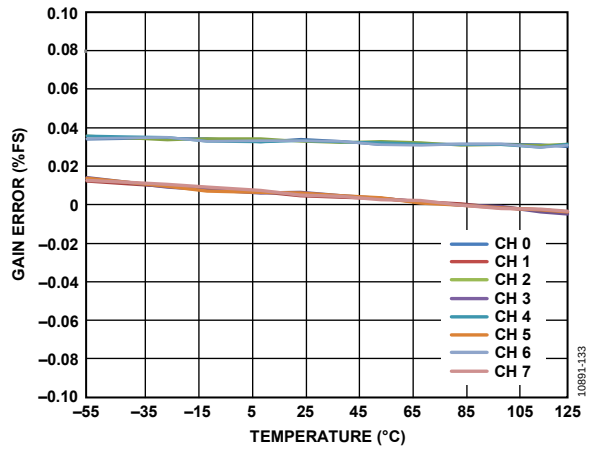


Figure 33. Gain Error vs. Temperature

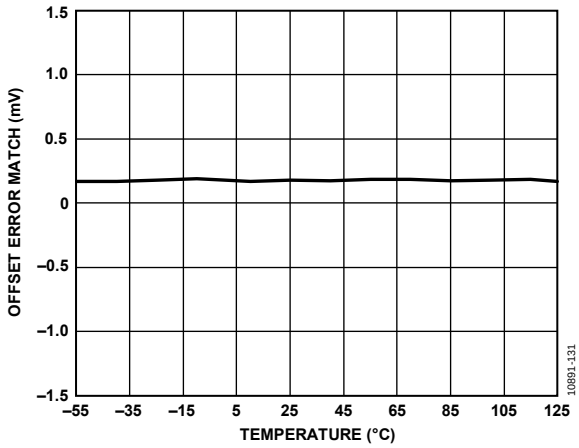


Figure 31. Offset Error Match vs. Temperature

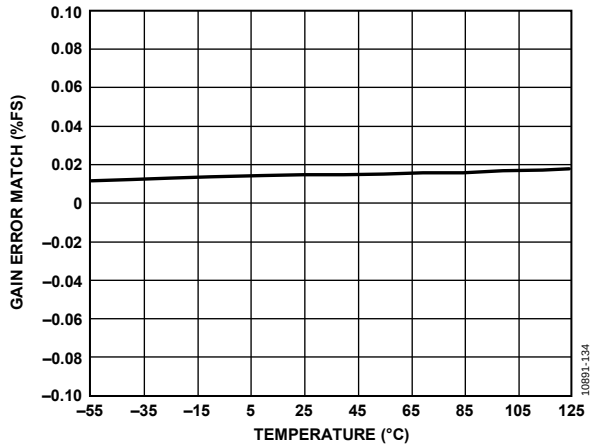


Figure 34. Gain Error Match vs. Temperature

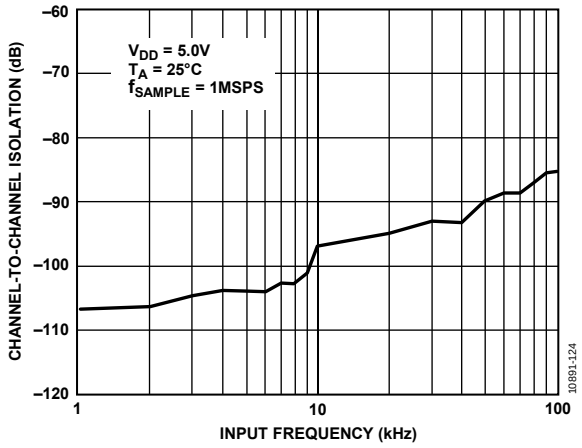


Figure 35. Channel-to-Channel Isolation vs. Input Frequency

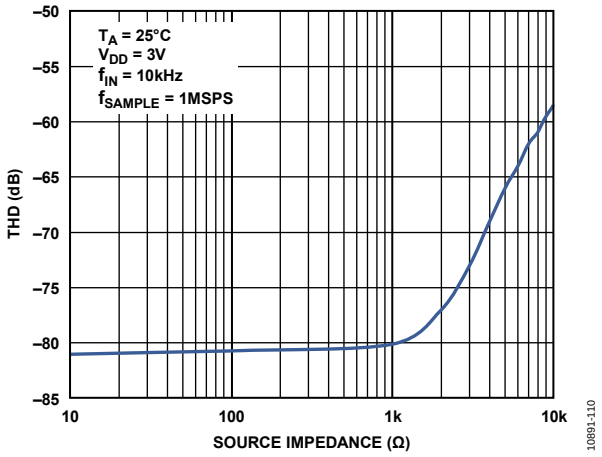


Figure 38. THD vs. Source Impedance

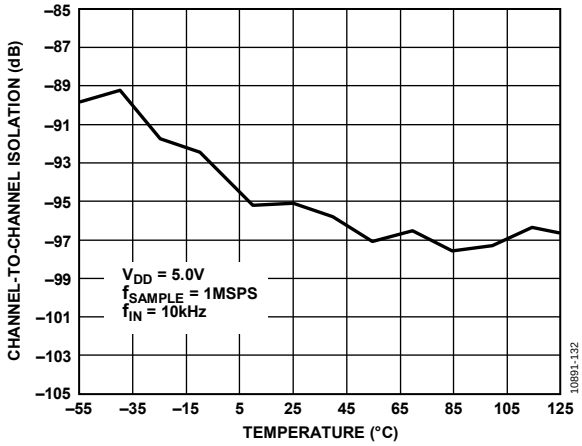


Figure 36. Channel-to-Channel Isolation vs. Temperature

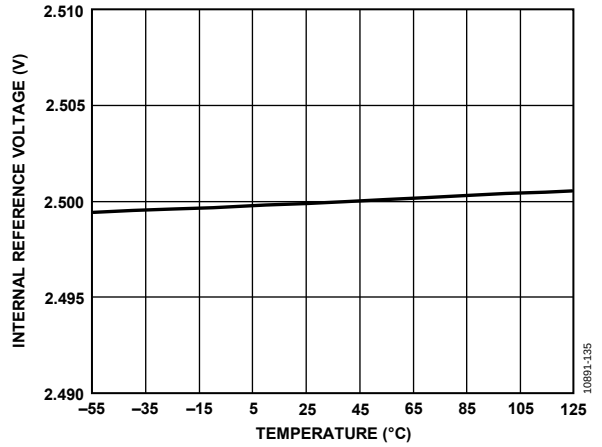


Figure 39. Internal Reference Voltage vs. Temperature

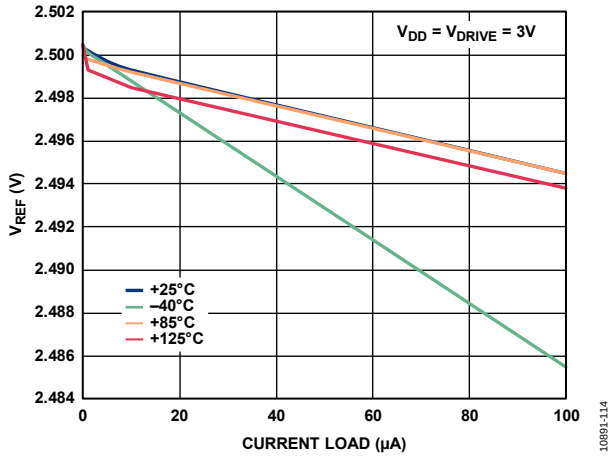


Figure 37. Reference Voltage Output (V_{REF}) vs. Current Load for Various Temperatures

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7091R-2/AD7091R-4/AD7091R-8, the endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The offset error is the deviation of the first code transition (00 … 000 to 00 … 001) from the ideal (such as GND + 0.5 LSB).

Offset Error Match
Offset error match is the difference in offset error between any two input channels.

Gain Error
For the AD7091R-2/AD7091R-4/AD7091R-8, the gain error is the deviation of the last code transition (111 … 110 to 111 … 111) from the ideal (such as V_{REF} − 1.5 LSB) after the offset error has been adjusted out.

Gain Error Match
Gain error match is the difference in gain error between any two input channels.

Transient Response Time
The track-and-hold amplifier returns to track mode after the end of conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See the Serial Port Interface section for more details.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the measured ratio of signal-to-noise-and-distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$SINAD = (6.02N + 1.76)\ \text{dB}$$

Thus, for a 12-bit converter, the SINAD ratio is 74 dB.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between the selected channel and all of the other channels. It is measured by applying a full-scale, 10 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel that has a dc signal applied to it. Figure 35 shows the worst case across all channels for the AD7091R-2/AD7091R-4/AD7091R-8.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7091R-2/AD7091R-4/AD7091R-8, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonic.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7091R-2/AD7091R-4/AD7091R-8 are 12-bit, fast (1 MSPS), ultralow power, single-supply ADCs. The devices operate from a 2.7 V to 5.25 V supply. The AD7091R-2/AD7091R-4/AD7091R-8 are capable of throughput rates of 1 MSPS.

The AD7091R-2/AD7091R-4/AD7091R-8 provide an on-chip, track-and-hold ADC and a serial interface housed in a 16-lead, 20-lead, or 24-lead TSSOP or LFCSP package, which offers considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the device. The clock for the successive approximation ADC is generated internally. The reference voltage for the AD7091R-2/AD7091R-4/AD7091R-8 is provided externally, or it is generated internally by an accurate on-chip reference source. The analog input range for the AD7091R-2/AD7091R-4/AD7091R-8 is 0 V to V_{REF}.

The AD7091R-2/AD7091R-4/AD7091R-8 also feature a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7091R-2/AD7091R-4/AD7091R-8 are successive approximation ADCs based on a charge redistribution digital-to-analog converter (DAC). Figure 40 and Figure 41 show simplified schematics of the ADC. Figure 40 shows the ADC during its acquisition phase. When SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

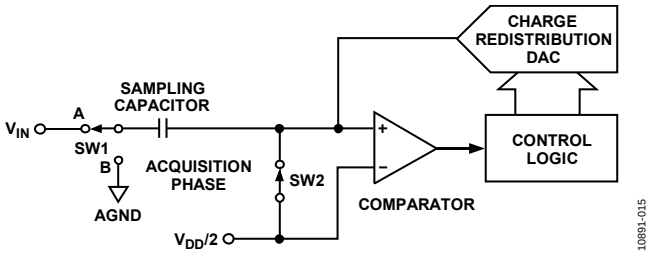


Figure 40. ADC Acquisition Phase

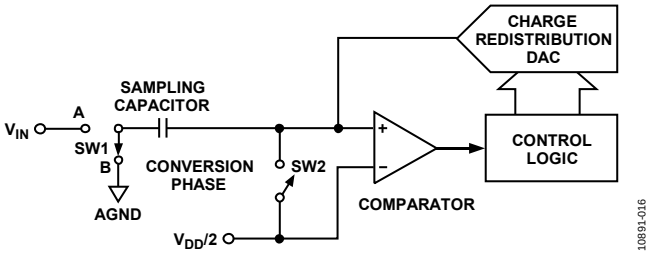


Figure 41. ADC Conversion Phase

When the ADC starts a conversion, SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced (see Figure 41). Using the control logic, the charge redistribution DAC adds and subtracts fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the SAR decisions are made, the comparator inputs are rebalanced. From these SAR decisions, the control logic generates the ADC output code.

ADC TRANSFER FUNCTION

The output coding of the AD7091R-2/AD7091R-4/AD7091R-8 is straight binary. The designed code transitions occur midway between successive integer LSB values, such as ½ LSB, 1½ LSB, and so on. The LSB size for the AD7091R-2/AD7091R-4/AD7091R-8 is V_{REF}/4096. The ideal transfer characteristic for the AD7091R-2/AD7091R-4/AD7091R-8 is shown in Figure 42.

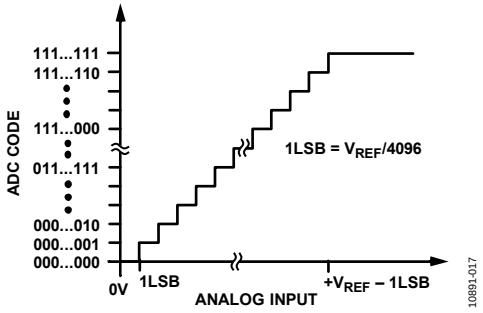


Figure 42. AD7091R-2/AD7091R-4/AD7091R-8 Transfer Characteristic

REFERENCE

The AD7091R-2/AD7091R-4/AD7091R-8 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The logic state of the P_DOWN LSB bit in the configuration register determines whether the internal reference is used. The internal reference is selected for the ADCs when the P_DOWN LSB bit is set to 1.

When the P_DOWN LSB bit is set to 0, supply an external reference in the range of 1.0 V to V_{DD} through the REF_{IN}/REF_{OUT} pin. At power-up, the internal reference disables by default.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When operating the AD7091R-2/AD7091R-4/AD7091R-8 in internal reference mode, the 2.5 V internal reference is available at the REF_{IN}/REF_{OUT} pin, which is typically decoupled to GND using a 2.2 µF capacitor. It is recommended to buffer the internal reference before applying it elsewhere in the system.

The reference buffer requires 50 ms to power up and charge the 2.2 µF decoupling capacitor during the power-up time.

POWER SUPPLY

The AD7091R-2/AD7091R-4/AD7091R-8 use two power supply pins: a core supply (V_{DD}) and a digital input/output interface supply (V_{DRIVE}). V_{DRIVE} allows direct interface with any logic between 1.8 V and 5.25 V. To reduce the number of supplies needed, V_{DRIVE} and V_{DD} can be tied together depending upon the logic levels of the system. Additionally, the AD7091R-2/AD7091R-4/AD7091R-8 are insensitive to power supply variation over a wide frequency range, as shown in Figure 32. AD7091R-2/AD7091R-4/AD7091R-8 operation is independent of power supply sequencing between V_{DRIVE} and V_{DD}.

The AD7091R-2/AD7091R-4/AD7091R-8 power down automatically at the end of each conversion phase; therefore, the power scales linearly with the sampling rate. The automatic power-down feature makes the AD7091R-2/AD7091R-4/AD7091R-8 devices ideal for low sampling rates (of even a few hertz) and battery-powered applications.

Table 8. Recommended Power Management Devices[1]

Product	Description
ADP7102	20 V, 300 mA, low noise, CMOS LDO
ADM7160	Ultralow noise, 200 mA linear regulator
ADP162	Ultralow quiescent current, CMOS linear regulator

[1] For the latest recommended power management devices, see the AD7091R-2/AD7091R-4/AD7091R-8 product pages.

DEVICE RESET

Upon power up, a reset pulse of at least 10 ns in width must be provided on the $\overline{\text{RESET}}$ pin to ensure proper initialization of the device. Failure to apply the reset pulse may result in a device malfunction. See Figure 43 for reset pulse timing relative to power supply establishment. If the system has a limited number of digital pins and one cannot be allocated to the reset pin of the ADC, a software reset may be issued in place of the hardware reset signal (see the Power-On Device Initialization section).

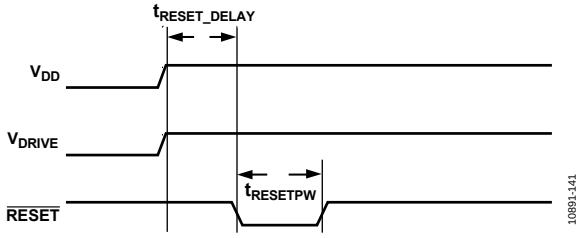


Figure 43. $\overline{\text{RESET}}$ Pin Power Up Timing

TYPICAL CONNECTION DIAGRAM

Figure 45 shows a typical connection diagram for the AD7091R-2/AD7091R-4/AD7091R-8.

Connect a positive power supply in the 2.7 V to 5.25 V range to the V_{DD} pin. Typical values for these decoupling capacitors are 0.1 µF and 10 µF. Place these capacitors near the device pins. Take care to decouple the REF_{IN}/REF_{OUT} pin to achieve specified performance. The typical value for the REF_{IN}/REF_{OUT} capacitor is 2.2 µF, which provides an analog input range of 0 V to V_{REF}.

The typical value for the regulator bypass (REGCAP) decoupling capacitor is 1.0 µF. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface; therefore, connect this pin to the supply voltage of the microprocessor. Set V_{DRIVE} in the 1.8 V to 5.25 V range. Typical values for the V_{DRIVE} decoupling capacitors are 0.1 µF and 10 µF. The conversion result is output in a 16-bit word with the MSBs first.

When an externally applied reference is required, disable the internal reference using the configuration register. Choose the externally applied reference voltage in the 1.0 V to 5.25 V V_{DD} range and connect it to the REF_{IN}/REF_{OUT} pin.

For applications where power consumption is a concern, use the power-down mode of the ADC to improve power performance. See the Modes of Operation section for additional details.

ANALOG INPUT

Figure 44 shows an equivalent circuit of the analog input structure of the AD7091R-2/AD7091R-4/AD7091R-8. The two diodes, D1 and D2, provide ESD protection for the analog input. Take care to ensure that the analog input signal never exceeds the supply rails by more than 300 mV because this causes these diodes to become forward-biased and start conducting current into the substrate. These diodes can conduct a maximum of 10 mA without causing irreversible damage to the device.

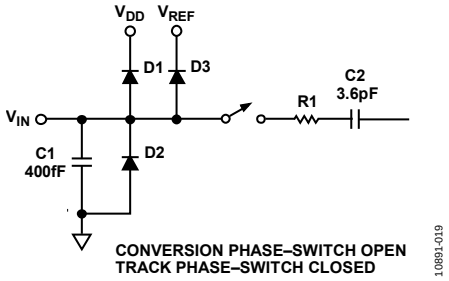


Figure 44. Equivalent Analog Input Circuit

The C1 capacitor in Figure 44 is typically about 400 fF and can primarily be attributed to pin capacitance. The R1 resistor is a lumped component composed of the on resistance of a switch. This resistor is typically about 500 Ω. The C2 capacitor is the ADC sampling capacitor and typically has a capacitance of 3.6 pF.

In applications where harmonic distortion and signal-to-noise ratio are critical, drive the analog inputs from low impedance sources. Large source impedances significantly affect the ac performance of the ADC that can necessitate using input buffer amplifiers, as shown in Figure 45. The choice of the op amp is a function of the particular application.

When no amplifiers are used to drive the analog input, limit the source impedance to low values. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades.

Use an external filter on the analog input signal paths to the AD7091R-2/AD7091R-4/AD7091R-8 $V_{IN}x$ pins to achieve the specified performance. This filter can be a one-pole low-pass RC filter, or similar.

Connect the MUX_{OUT} pin directly to the ADC_{IN} pin. Insert a buffer amplifier in the path, if desired. When sequencing channels, do not place a filter between MUX_{OUT} and the input to any buffering because doing so leads to crosstalk. If buffering is not employed, do not place a filter between MUX_{OUT} and ADC_{IN} when sequencing channels because doing so leads to crosstalk.

DRIVER AMPLIFIER CHOICE

Although the AD7091R-2/AD7091R-4/AD7091R-8 are easy to drive, a driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7091R-2/AD7091R-4/AD7091R-8. The noise from the driver is filtered by the one-pole, low-pass filter of the AD7091R-2/AD7091R-4/AD7091R-8 analog input circuit, made by R1 and C2, or by the external filter, if one is used. Because the typical noise of the AD7091R-2/AD7091R-4/AD7091R-8 is 280 μV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log\left(\frac{280}{\sqrt{280^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}}\right)$$

  where:
  f_{-3dB} is the input bandwidth, in megahertz, of the AD7091R-2/AD7091R-4/AD7091R-8 (1.5 MHz), or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, gain = 1 in buffer configuration; see Figure 45).
  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.
- For ac applications, the driver must have a THD performance that is commensurate with the AD7091R-2/AD7091R-4/AD7091R-8.
- If the buffer is placed between MUX_{OUT} and ADC_{IN}, the driver amplifier and the AD7091R-2/AD7091R-4/AD7091R-8 analog input circuit must settle for a full-scale step onto the capacitor array at a 12-bit level (0.0244%, 244 ppm). In an amplifier data sheet, settling at 0.1% to 0.01% is more commonly specified and may differ significantly from the settling time at a 12-bit level. Be sure to verify the amplifier settling time prior to driver selection.

Table 9. Recommended Driver Amplifiers[1]

Product	Description
ADA4805-1	Low noise, ultralow power, wide bandwidth amplifier
AD8031	Low voltage, low power, single channel amplifier
AD8032	Low voltage, low power, dual channel amplifier
AD8615	Low frequency, low voltage amplifier

[1] For the latest recommended ADC driver products, see the AD7091R-2/AD7091R-4/AD7091R-8 product pages.

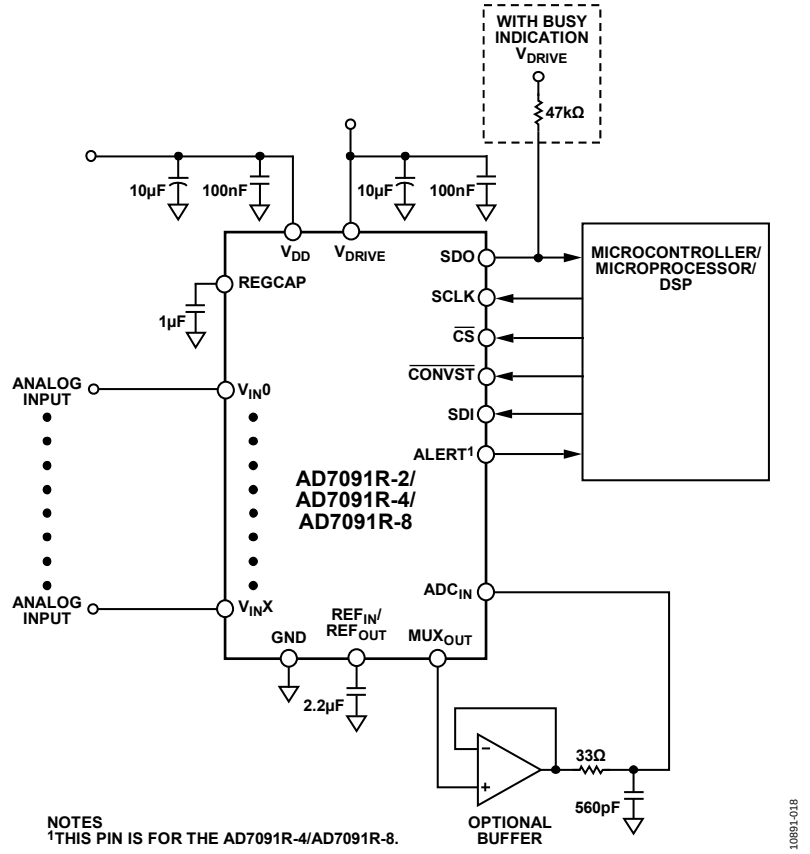


Figure 45. Typical Connection Diagram with Optional Buffer

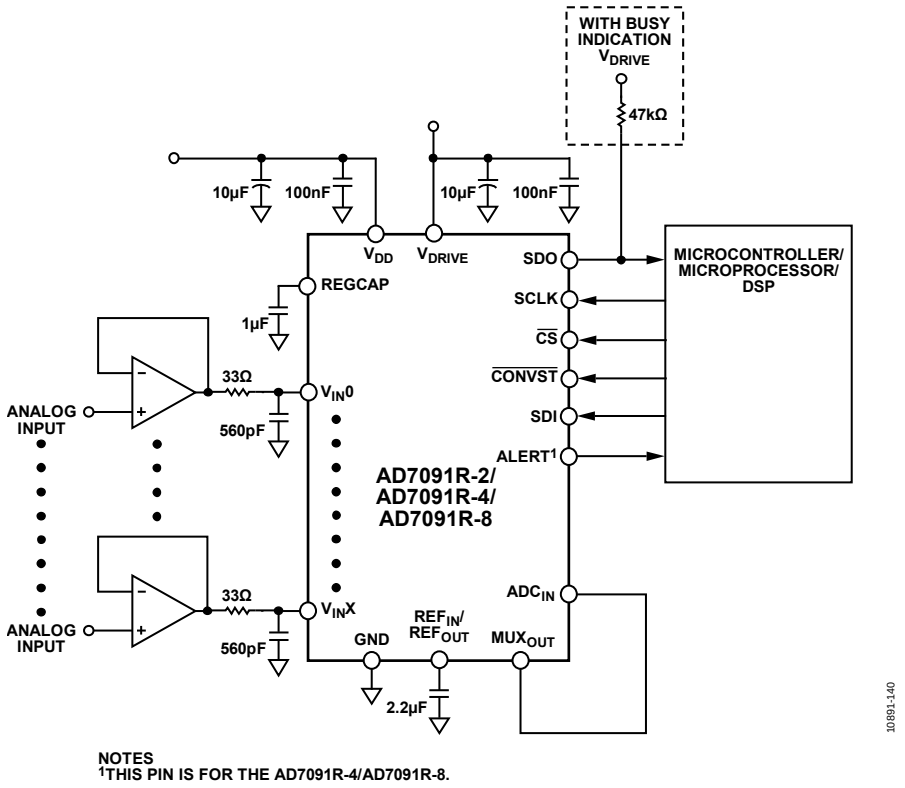


Figure 46. Typical Connection Diagram Without Optional Buffer

REGISTERS

The AD7091R-2/AD7091R-4/AD7091R-8 have user programmable registers. Table 10 contains the complete list of registers.

The registers are either read/write (R/W) or read only (R). Data is written to or read back from the read/write registers. Read only registers is only read. Any write to a read only register or unimplemented register address is considered no operation (NOP). A NOP command is an SPI command that is ignored by the AD7091R-2/AD7091R-4/AD7091R-8. After a write to a read only register, the output on the subsequent SPI frame is all zeros if there was no conversion before the next SPI frame. Similarly, any read of an unimplemented register outputs zeros.

ADDRESSING REGISTERS

A serial transfer on the AD7091R-2/AD7091R-4/AD7091R-8 consists of 16 SCLK cycles. The six MSBs on the SDI line during the 16 SCLK transfer are decoded to determine which register is addressed. The six MSBs consist of the register address (ADDx), Bits[4:0], and the read/write bit. The register address bits determine which of the on-chip registers are selected. The read/write bit determines if the data on the SDI line following the read/write bit loads into the addressed register. If the read/write bit is 1, the bits load into the register addressed by the register select bits. Data loads into the register on the rising edge of $\overline{CS}$. If the read/write bit is 0, the command is seen as a read request. The requested register data is available on the subsequent message on the SDO line.

Table 10. Register Description

			Access		
Address	**Register Name**	**Default**	**AD7091R-8**	**AD7091R-4**	**AD7091R-2**
0x00	Conversion result	0x0000	R	R	R
0x01	Channel	0x0000	R/W	R/W	R/W
0x02	Configuration	0x00C0	R/W	R/W	R/W
0x03	Alert indication	0x0000	R	R	R
0x04	Channel 0 low limit	0x0000	R/W	R/W	R/W
0x05	Channel 0 high limit	0x01FF	R/W	R/W	R/W
0x06	Channel 0 hysteresis	0x01FF	R/W	R/W	R/W
0x07	Channel 1 low limit	0x0000	R/W	R/W	R/W
0x08	Channel 1 high limit	0x01FF	R/W	R/W	R/W
0x09	Channel 1 hysteresis	0x01FF	R/W	R/W	R/W
0x0A	Channel 2 low limit	0x0000	R/W	R/W	NOP
0x0B	Channel 2 high limit	0x01FF	R/W	R/W	NOP
0x0C	Channel 2 hysteresis	0x01FF	R/W	R/W	NOP
0x0D	Channel 3 low limit	0x0000	R/W	R/W	NOP
0x0E	Channel 3 high limit	0x01FF	R/W	R/W	NOP
0x0F	Channel 3 hysteresis	0x01FF	R/W	R/W	NOP
0x10	Channel 4 low limit	0x0000	R/W	NOP	NOP
0x11	Channel 4 high limit	0x01FF	R/W	NOP	NOP
0x12	Channel 4 hysteresis	0x01FF	R/W	NOP	NOP
0x13	Channel 5 low limit	0x0000	R/W	NOP	NOP
0x14	Channel 5 high limit	0x01FF	R/W	NOP	NOP
0x15	Channel 5 hysteresis	0x01FF	R/W	NOP	NOP
0x16	Channel 6 low limit	0x0000	R/W	NOP	NOP
0x17	Channel 6 high limit	0x01FF	R/W	NOP	NOP
0x18	Channel 6 hysteresis	0x01FF	R/W	NOP	NOP
0x19	Channel 7 low limit	0x0000	R/W	NOP	NOP
0x1A	Channel 7 high limit	0x01FF	R/W	NOP	NOP
0x1B	Channel 7 hysteresis	0x01FF	R/W	NOP	NOP
0x1C	Reserved	0x0000	NOP	NOP	NOP
…	…	…	…	…	…
0x1F	Reserved	0x0000	NOP	NOP	NOP

CONVERSION RESULT REGISTER

The conversion result register is a 16-bit, read only register that stores the results from the most recent ADC conversion in straight binary format. The channel ID of the converted channel and the alert status are also included in the register.

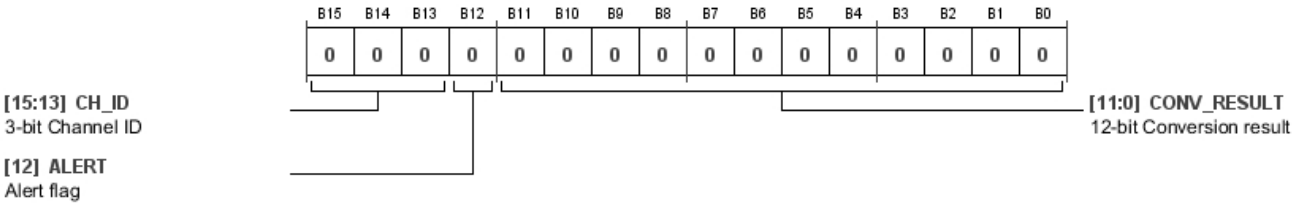


Figure 47. Conversion Result Register

Table 11. Conversion Result Register Map

MSB															LSB
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
CH_ID			ALERT	CONV_RESULT											

Table 12. Bit Descriptions for the Conversion Result Register

Bit(s)	Name	Description				Reset	Access
[15:13]	CH_ID	3-bit channel ID of channel converted				0x0	R
		B15[1, 2]	**B14**[2]	**B13**	**Analog Input Channel**		
		0	0	0	$V_{IN}0$		
		0	0	1	$V_{IN}1$		
		0	1	0	$V_{IN}2$		
		0	1	1	$V_{IN}3$		
		1	0	0	$V_{IN}4$		
		1	0	1	$V_{IN}5$		
		1	1	0	$V_{IN}6$		
		1	1	1	$V_{IN}7$		
12	ALERT	ALERT flag 0: No ALERT occurred 1: ALERT occurred				0	R
[11:0]	CONV_RESULT	12-bit conversion result				0x000	R

[1] Always zero on the AD7091R-4.
[2] Always zero on the AD7091R-2.

CHANNEL REGISTER

The channel register on the AD7091R-2/AD7091R-4/AD7091R-8 is an 8-bit, read/write register. Each of the eight analog input channels has one corresponding bit in the channel register. To select a channel for inclusion in the channel conversion sequence, set the corresponding channel bit to 1 in the channel register. There is a latency of one conversion before the channel conversion sequence is updated. If the channel register is programmed with a new value, the conversion sequence is reset to the lowest numbered channel in the new value.

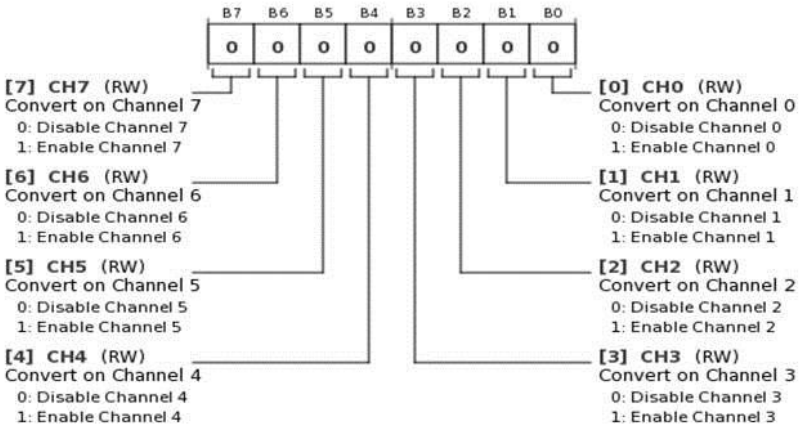


Figure 48. Channel Registers

Table 13. Channel Register Map

MSB															LSB
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Table 14. Bit Descriptions for the Channel Register

Bit(s)	Name	Description	Reset	Access
[15:8]	Reserved	Reserved	0x00	R
7	CH7	Convert on Channel 7 0: Disable Channel 7 1: Enable Channel 7	0x0	R/W
6	CH6	Convert on Channel 6 0: Disable Channel 6 1: Enable Channel 6	0x0	R/W
5	CH5	Convert on Channel 5 0: Disable Channel 5 1: Enable Channel 5	0x0	R/W
4	CH4	Convert on Channel 4 0: Disable Channel 4 1: Enable Channel 4	0x0	R/W
3	CH3	Convert on Channel 3 0: Disable Channel 3 1: Enable Channel 3	0x0	R/W
2	CH2	Convert on Channel 2 0: Disable Channel 2 1: Enable Channel 2	0x0	R/W
1	CH1	Convert on Channel 1 0: Disable Channel 1 1: Enable Channel 1	0x0	R/W
0	CH0	Convert on Channel 0 0: Disable Channel 0 1: Enable Channel 0	0x0	R/W

CONFIGURATION REGISTER

The configuration register is a 16-bit, read/write register that is used to set the operating modes of the AD7091R-2/AD7091R-4/AD7091R-8.

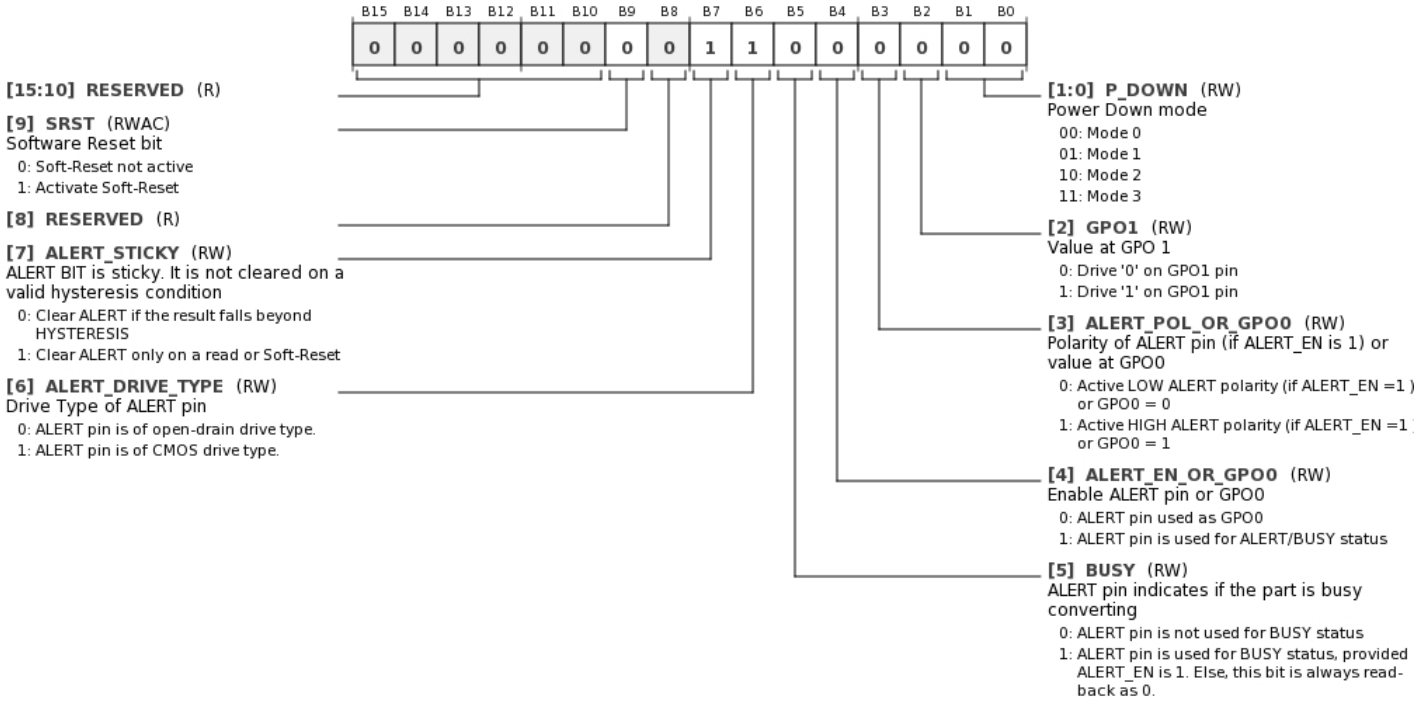


Figure 49. Configuration Register

Table 15. Configuration Register Map

MSB **LSB**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Reserved						SRST	Reserved	ALERT_ STICKY	ALERT_ DRIVE_TYPE	BUSY	ALERT_EN_ OR_GPO0	ALERT_POL_ OR_GPO0	GPO1	P_DOWN	

Table 16. Bit Descriptions for the Configuration Register

Bit(s)	Name	Description	Reset	Access
[15:10]	Reserved	Reserved	0x00	R
9	SRST	Software reset bit. Setting this bit resets the internal digital control logic and the result and alert registers, but it does not reset the other memory map registers. This bit automatically clears in the next clock cycle. Note that it loads random access memory (RAM) from fuses. 0: Soft reset not active. 1: Activate soft reset.	0x0	RWAC
8	Reserved	Reserved	0x0	R
7	ALERT_STICKY	ALERT bit is sticky. It is not cleared on a valid hysteresis condition. 0: Clear ALERT[1] if the result falls beyond hysteresis. 1: Clear ALERT[1] only on a read or soft reset.	0x1	R/W
6	ALERT_DRIVE_TYPE	Drive type of ALERT[1] pin. 0: ALERT[1] pin is of open-drain drive type. 1: ALERT[1] pin is of CMOS drive type.	0x1	R/W
5	BUSY	ALERT[1] pin indicates if the part is busy converting. 0: ALERT[1] pin is not used for BUSY status. 1: ALERT[1] pin is used for BUSY status, provided ALERT_EN_OR_GPO0) is 1. Else, this bit is always read back as 0.	0x0	R/W

Bit(s)	Name	Description				Reset	Access
4	ALERT_EN_OR_GPO0	Enable ALERT pin or GPO_0[1]. 0: ALERT[1] pin used as GPO_0[1]. 1: ALERT[1] pin is used for ALERT[1]/BUSY[1] status.				0x0	R/W
3	ALERT_POL_OR_GPO0	Polarity of ALERT[1] pin (if ALERT_EN_OR_GPO0 is 1) or value at GPO_0[1]. 0: Active low ALERT[1] polarity (if ALERT_EN_OR_GPO0 = 1) or GPO_0[1] = 0. 1: Active high ALERT[1] polarity (if ALERT_EN_OR_GPO0 = 1) or GPO_0[1] = 1.				0x0	R/W
2	GPO1	Value at GPO_1[1]. 0: Drive 0 on GPO_1[1] pin. 1: Drive 1 on GPO_1[1] pin.				0x0	R/W
[1:0]	P_DOWN	Power-down mode.				0x0	R/W
		Setting	**Mode**	**Sleep Mode/Bias Generator**	**Internal Reference**		
		00	Mode 0	Off	Off		
		01	Mode 1	Off	On		
		10	Mode 2	On	Off		
		11	Mode 3	On	On		

[1] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configurations and Function Descriptions section.

ALERT INDICATION REGISTER

The 16-bit, alert indication register is a read only register that provides information on an alert event. If a conversion result activates the ALERT function of the ALERT/BUSY/GPO_0 pin, as described in the Channel x Low Limit Register section and the Channel x High Limit Register section, the alert register can be read to determine the source of the alert. The register contains two status bits per channel, one corresponding to the high limit, and the other to the low limit. The bit with a status equal to 1 shows where the violation occurred, that is, on which channel, and whether the violation occurred on the upper or lower limit.

If a second alert event occurs on another channel between receiving the first alert and interrogating the alert register, the corresponding bit for that alert event is also set.

The contents of the alert indication register are reset by reading it. The alert indication register is reset on the second SCLK cycle of the SPI frame where the ALERT data is read out. If a conversion happens in the meantime, the conversion result is sent instead of the alert indication register contents. The alert indication register is not reset in this case.

The alert bits for any unimplemented channels on the 2-channel and 4-channel devices always return zeros.

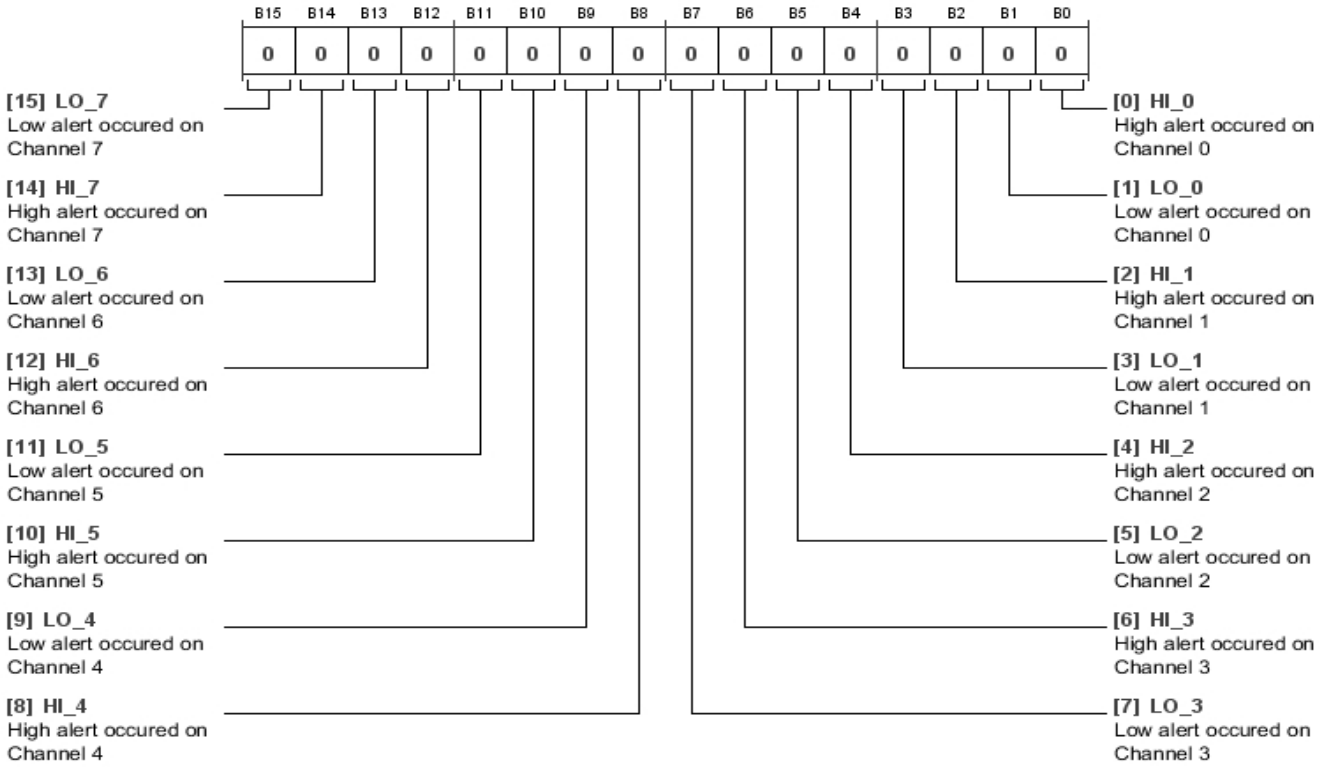


Figure 50. Alert Indication Register (Figure Shows Default Register Value of 0, Indicating No Alert Has Occurred)

Table 17. Alert Indication Register Map

MSB															LSB
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
LO_7	HI_7	LO_6	HI_6	LO_5	HI_5	LO_4	HI_4	LO_3	HI_3	LO_2	HI_2	LO_1	HI_1	LO_0	HI_0

Table 18. Bit Descriptions for the Alert Indication Register

Bit(s)	Bit Name	Description	Reset	Access
15	LO_7	Channel 7 low alert status 0: No alert on Channel 7 1: Low alert occurred on Channel 7	0x0	R
14	HI_7	Channel 7 high alert status 0: No alert on Channel 7 1: High alert occurred on Channel 7	0x0	R

Bit(s)	Bit Name	Description	Reset	Access
13	LO_6	Channel 6 low alert status 0: No alert on Channel 6 1: Low alert occurred on Channel 6	0x0	R
12	HI_6	Channel 6 high alert status 0: No alert on Channel 6 1: High alert occurred on Channel 6	0x0	R
11	LO_5	Channel 5 low alert status 0: No alert on Channel 5 1: Low alert occurred on Channel 5	0x0	R
10	HI_5	Channel 5 high alert status 0: No alert on Channel 5 1: High alert occurred on Channel 5	0x0	R
9	LO_4	Channel 4 low alert status 0: No alert on Channel 4 1: Low alert occurred on Channel 4	0x0	R
8	HI_4	Channel 4 high alert status 0: No alert on Channel 4 1: High alert occurred on Channel 4	0x0	R
7	LO_3	Channel 3 low alert status 0: No alert on Channel 3 1: Low alert occurred on Channel 3	0x0	R
6	HI_3	Channel 3 high alert status 0: No alert on Channel 3 1: High alert occurred on Channel 3	0x0	R
5	LO_2	Channel 2 low alert status 0: No alert on Channel 2 1: Low alert occurred on Channel 2	0x0	R
4	HI_2	Channel 2 high alert status 0: No alert on Channel 2 1: High alert occurred on Channel 2	0x0	R
3	LO_1	Channel 1 low alert status 0: No alert on Channel 1 1: Low alert occurred on Channel 1	0x0	R
2	HI_1	Channel 1 high alert status 0: No alert on Channel 1 1: High alert occurred on Channel 1	0x0	R
1	LO_0	Channel 0 low alert status 0: No alert on Channel 0 1: Low alert occurred on Channel 0	0x0	R
0	HI_0	Channel 0 high alert status 0: No alert on Channel 0 1: High alert occurred on Channel 0	0x0	R

CHANNEL x LOW LIMIT REGISTER

Each analog input channel of the AD7091R-2/AD7091R-4/AD7091R-8 has its own low limit register. The low limit registers are 16-bit read/write registers. See Table 10 for the register addresses. The low limit registers store the lower limit of the conversion value that activates the ALERT output.

Of the 16 bits, B15 to B9 are not used. Only the nine LSBs, B8 to B0, are used. These 9 bits, which are programmed by the user, are used as the MSBs of the internal 12-bit register. The 3 LSBs in the internal 12-bit registers are set to 000.

CHANNEL x HIGH LIMIT REGISTER

Each analog input channel of the AD7091R-2/AD7091R-4/AD7091R-8 has its own high limit register. The high limit registers are 16-bit read/write registers. See Table 10 for the register addresses. The high limit registers store the upper limit of the conversion value that activates the ALERT output.

Of the 16 bits, B15 to B9 are not used. Only the nine LSBs, B8 to B0, are used. These 9 bits, which are programmed by the user, are used as the MSBs of the internal 12-bit register. The 3 LSBs in the internal 12-bit registers are set to 111.

CHANNEL x HYSTERESIS REGISTER

Each analog input channel of the AD7091R-2/AD7091R-4/AD7091R-8 has its own hysteresis register, which are 16-bit read/write registers. See Table 10 for the register addresses. The hysteresis register stores the hysteresis value (N) when using the limit registers. The hysteresis value determines the reset point for the ALERT/BUSY/GPO_0 pin if a violation of the limits has occurred.

Of the 16 bits, B15 to B9 are not used. Only the nine LSBs, B8 to B0, are used. These 9 bits, which are programmed by the user, are used as the MSBs of the internal 12-bit register. The 3 LSBs in the internal 12-bit registers are set to 000.

Table 19. Channel x Low Limit Register Map

MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Reserved							CHx LOW LIMIT								

Table 20. Bit Descriptions for the Channel x Low Limit Register

Bit(s)	Bit Name	Description	Reset	Access
[15:9]	Reserved	Reserved	0x00	R
[8:0]	CHx LOW LIMIT	Low limit value for Channel x	0x000	R/W

Table 21. Channel x High Limit Register Map

MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Reserved							CHx HIGH LIMIT								

Table 22. Bit Descriptions for the Channel x High Limit Register

Bits	Bit Name	Description	Reset	Access
[15:9]	Reserved	Reserved	0x00	R
[8:0]	CHx HIGH LIMIT	High limit value for Channel x	0x1FF	R/W

Table 23. Channel x Hysteresis Register Map

MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Reserved							CHx HYSTERESIS								

Table 24. Bit Descriptions for the Channel x Hysteresis Register

Bit(s)	Bit Name	Description	Reset	Access
[15:9]	Reserved	Reserved	0x00	R
[8:0]	CHx HYSTERESIS	Hysteresis value for Channel x	0x1FF	R/W

SERIAL PORT INTERFACE

The SPI is a 4-wire interface (three inputs and one output) for serial data communication. It has a chip select ($\overline{CS}$) line, a serial clock (SCLK), a serial data input (SDI), and a serial data output (SDO). Data transfers on SDI and SDO take place with respect to SCLK. $\overline{CS}$ is used to frame the data and is active low. When $\overline{CS}$ is high, SDO is kept in high impedance. The falling edge of $\overline{CS}$ takes the SDO line out of the high impedance state. A rising edge on $\overline{CS}$ returns the SDO to a high impedance state.

The SPI implemented on the AD7091R-2/AD7091R-4/AD7091R-8 can support both of the following: CPHA and CPOL = 0, and CPHA and CPOL = 1. This support ensures that the device can interface to microcontrollers and DSPs that keep either SCLK high or SCLK low when $\overline{CS}$ is not asserted. The device ignores SCLK toggling when $\overline{CS}$ is not asserted.

READING CONVERSION RESULT

The $\overline{CONVST}$ signal is used to initiate the conversion process. A high-to-low transition on the $\overline{CONVST}$ signal puts the track-and-hold into hold mode and samples the analog input at this point. A conversion is initiated and requires 600 ns to complete. Before the end of the conversion, take the $\overline{CONVST}$ signal high again. When the conversion process is finished, the track-and-hold mode goes back into track mode. Then, take the $\overline{CS}$ pin low, and the conversion result clocks out on the SDO pin. The data is shifted out of the device as a 16-bit word under the control of the serial clock (SCLK) input. The data is shifted out on the falling edge of SCLK, and the data bits are valid on both the rising edge and the falling edge. The MSB is shifted out on the falling edge of $\overline{CS}$. The final bit in the data transfer is valid on the 16th rising edge and the 16th falling edge, having clocked out on the previous (15th) falling edge. After the 16th falling edge, take $\overline{CS}$ high again to return the SDO to a high impedance state. If another conversion is required, take the $\overline{CONVST}$ pin low again (after at least 1 µs), and repeat the read cycle. The timing diagram for this operation is shown in Figure 52.

WRITING DATA TO THE REGISTERS

All the read/write registers in the device can be written over the SPI. A register write command is performed by a single 16-bit SPI access. The format for a write command is shown in Table 25. Bits[B15:B11] contain the register address. See Table 10 for the complete list of register addresses. Setting Bit B10 to 1 selects a write command. The subsequent 10 bits (Bits[B9:B0]) contain the data to be written to the selected register.

READING DATA FROM THE REGISTERS

All the registers in the device can be read over the SPI. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or NOP. The format for a read command is shown in Table 26. Bits[B15:B11] contain the register address. See Table 10 for the complete list of register addresses. Setting Bit B10 to 0 selects a read command. The device ignores the subsequent bits (Bits[B9:B0]).

Any conversion event is treated as a special case and overrides a previous read command. The AD7091R-2/AD7091R-4/AD7091R-8 always drive out the conversion result register on SDO after a conversion even though a register read was initiated in the previous SPI frame.

Table 25. Write Command Message Configuration

MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register Address[4:0]					1	Data[9:0]									

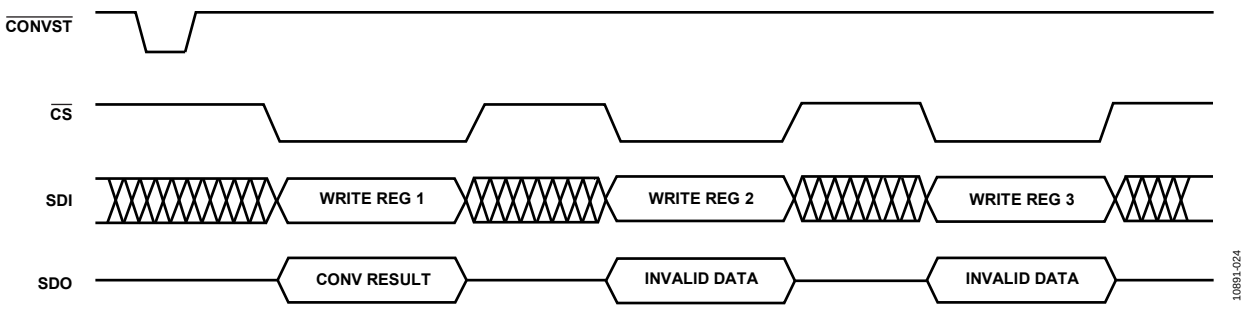


Figure 51. Serial Interface Register Write

Table 26. Read Command Message Configuration

MSB															LSB
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Register Address[4:0]					0	Don't Care									

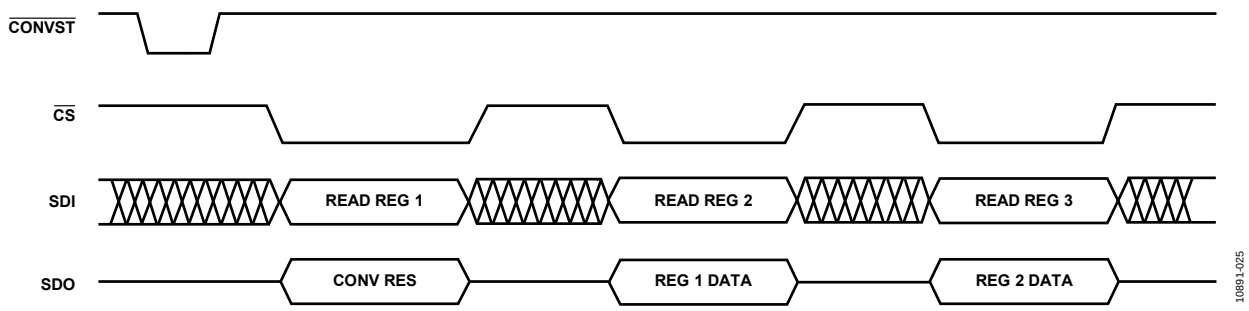


Figure 52. Serial Interface Register Read

POWER-ON DEVICE INITIALIZATION

In lieu of applying a pulse to the $\overline{\text{RESET}}$ pin from the digital host at initial power up, it is possible to replicate the behavior of the hardware reset function through the application of an alternative stimulus to the $\overline{\text{CONVST}}$ pin. Once the internal regulator voltage has been established by V_{DD} reaching a voltage of 2.1 V, a series of $\overline{\text{CONVST}}$ pulses must be sent to the ADC. Following the subsequent procedure will reset the device, allowing for proper and expected operation.

To issue a software initialization,

1. Establish the V_{DD} and V_{DRIVE} supplies for the AD7091R-2/ AD7091R-4/ AD7091R-8. The power-on time will depend upon the supply pin decoupling load and drive strength of the supply resource.
2. Provide 66 pulses on the $\overline{\text{CONVST}}$ pin that are spaced a minimum of 2 µs apart. The pulse width on the $\overline{\text{CONVST}}$ pin must adhere to the t_{CNVPW} timing specification.
3. At the end of the 66th pulse, the ADC is initialized and in a ready state. The device can now be configured by the user.
4. At this point, all internal registers will be in an unknown state. Write the desired device configuration as described in the Writing Data to the Registers section. To place all write enabled internal registers in a known state, writing to all device registers is required.
5. Reset the read-only registers by activating the software reset bit of the Configuration Register when performing the write actions described in Step 4. See details in the Configuration Register section.

If using the on-chip internal reference, to meet specified performance, the user should wait until the reference capacitor is fully charged. The reference buffer requires 50 ms to power up and charge the 2.2 µF decoupling capacitor during the power-up time.

In digital pin limited applications, the $\overline{\text{RESET}}$ pin of the AD7091R-2/AD7091R-4/AD7091R-8 should be tied to the V_{DRIVE} supply either directly or via a pull-up resistor.

Figure 53 shows the timing diagram for this operation.

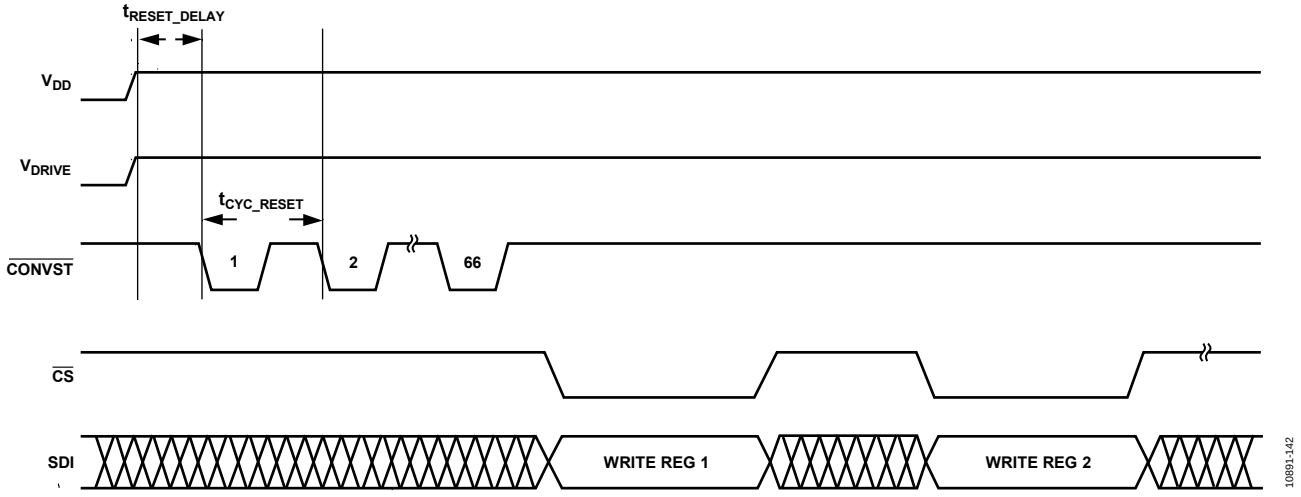


Figure 53. Power On Software Reset Timing

MODES OF OPERATION

NORMAL MODE

The user controls whether the device remains in normal mode or enters power-down mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

To achieve the fastest throughput rate performance, use normal mode. Power-up times are not an issue for the AD7091R-2/AD7091R-4/AD7091R-8 because they remain fully powered at all times. Figure 54 shows the general diagram of the AD7091R-2/AD7091R-4/AD7091R-8 in normal mode. The conversion initiates on the falling edge of $\overline{\text{CONVST}}$, as described in the Serial Port Interface section. To ensure that the device remains fully powered up at all times, return $\overline{\text{CONVST}}$ high before $t_{CONVERT}$ and keep it high until the conversion has finished. The end of conversion (EOC) point shown in Figure 54 indicates the end of EOC and the moment when the logic level of $\overline{\text{CONVST}}$ is tested.

To read back data stored in the conversion result register, wait until the conversion is completed. Then, take $\overline{\text{CS}}$ low, and the conversion data clocks out on the SDO pin. The output shift register is 16 bits wide. Data is shifted out of the device as a 16-bit word under the control of the serial clock (SCLK) input. The full timing diagram for this operation is shown in Figure 4. When the conversion read is completed, pull $\overline{\text{CONVST}}$ low again to start another conversion.

POWER-DOWN MODE

When slower throughput rates and lower power consumption are required, use power-down mode by either powering down the ADC between each conversion or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration between these burst conversions. When the AD7091R-2/AD7091R-4/AD7091R-8 are in power-down mode, all analog circuitry power down; however, the serial interface is active.

To enter power-down mode, write to the power-down configuration bits in the configuration register, as seen in Table 15. To enter full power-down mode, set the sleep mode/bias generator bit to 1, and set the internal reference bit to 0, which ensures that all analog circuitry and the internal reference power down. When the internal reference is enabled, it consumes power anytime Bit 0 of the configuration register is set to 1.

The serial interface of the AD7091R-2/AD7091R-4/AD7091R-8 is functional in power-down; therefore, the user can read back the results of the conversion after the device enters power-down mode.

To exit this mode of operation and to power up the AD7091R-2/AD7091R-4/AD7091R-8 again, write to the power-down configuration bits in the configuration register (see Table 15). On the rising edge of $\overline{\text{CONVST}}$, the device begins to power up. The power-up time of the AD7091R-2/AD7091R-4/AD7091R-8 is typically 1 µs. After power-up is complete, the ADC is fully powered up, and the input signal is properly acquired. To start the next conversion, operate the interface as described in the Normal Mode section. When using the internal reference, and the device is in full power-down mode, the user must wait to perform conversions until the internal reference has had time to power up and settle. The reference buffer requires 50 ms to power up and charge the 2.2 µF decoupling capacitor during the power-up time.

By using the power-down mode on the AD7091R-2/AD7091R-4/AD7091R-8 when this device is not converting, the average power consumption of the ADC decreases at lower throughput rates. Use power-down mode with lower throughput rates. When there is not a significant time interval between bursts of conversions, use normal mode (see the Normal Mode section).

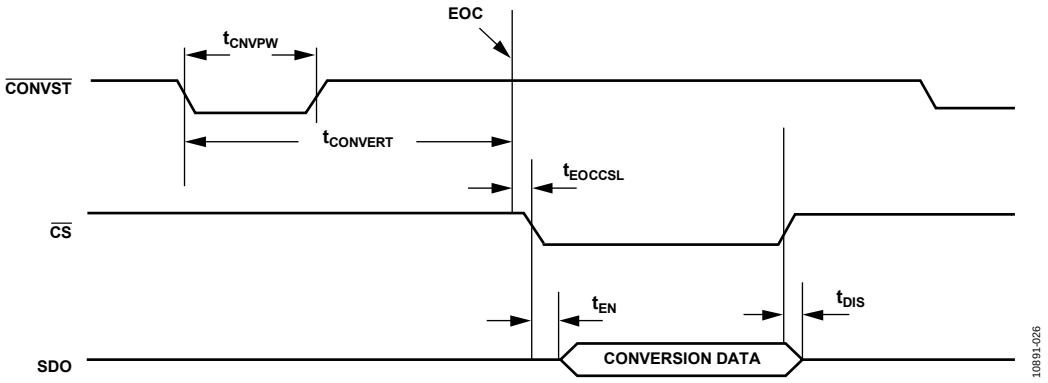


Figure 54. Serial Interface Read Timing in Normal Mode

ALERT (AD7091R-4 AND AD7091R-8 ONLY)

The alert functionality is used as an out-of-range indicator. An alert event is triggered when the value in the conversion result register exceeds the CHx HIGH LIMIT value in the channel high limit register or falls below the CHx LOW LIMIT value in the channel low limit register for a selected channel.

Detailed alert information is accessible in the alert register. The register contains two status bits per channel, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all channels creates a common alert value. This value can be accessed by the alert bit in the conversion result register and configured to drive out on the ALERT function of the ALERT/BUSY/GPO_0 pin. The ALERT/BUSY/GPO_0 pin is configured as ALERT by configuring the following bits in the configuration register:

- Set the ALERT_EN_OR_GPO0 bit, Bit 4, to 1.
- Set the BUSY bit, Bit 5, to 0.
- Set the ALERT_POL_OR_GPO0 bit, Bit 3, to 0 for the ALERT function of the ALERT/BUSY/GPO_0 pin to be active low, and set it to 1 for the ALERT function of the ALERT/BUSY/GPO_0 pin to be active high.

The alert register, alert bit, and the ALERT function of the ALERT/BUSY/GPO_0 pin are cleared by reading the alert register contents. Additionally, if the conversion result goes beyond the hysteresis value for a selected channel, the alert bit corresponding to that channel is reset automatically. The automatic clearing of the alert status can be disabled by setting the ALERT_STICKY bit in the configuration register to 1. If the ALERT_STICKY bit is set when an alert occurs, it can only be reset by a read of the alert register. Issuing a software reset also clears the alert status.

The ALERT/BUSY/GPO_0 pin has an open-drain configuration that allows the alert outputs of several AD7091R-4/AD7091R-8 devices to be wired together when the ALERT function of the ALERT/BUSY/GPO_0 pin is active low. The ALERT_DRIVE_TYPE bit (Bit 6) of the configuration register controls the ALERT/BUSY/GPO_0 pin configuration.

Use the ALERT_POL_OR_GPO0 bit (Bit 3) of the configuration register to set the active polarity of the alert output. The power-up default is active low.

When using the ALERT function of the ALERT/BUSY/GPO_0 pin and the open-drain configuration, an external pull-up resistor is required. Connect the external pull-up resistor to V_{DRIVE}. The resistor value is application dependent; however, it must be large enough to avoid excessive sink currents when the ALERT function of the ALERT/BUSY/GPO_0 pin is triggered.

BUSY (AD7091R-4 AND AD7091R-8 ONLY)

When configuring the ALERT/BUSY/GPO_0 pin as a BUSY output, use the pin to indicate when a conversion is taking place. To configure the ALERT/BUSY/GPO_0 pin as BUSY, use the following bits in the configuration register:

- Set the ALERT_EN_OR_GPO0 bit, Bit 4, to 1.
- Set the BUSY bit, Bit 5, to 1.
- Set the ALERT_POL_OR_GPO0 bit, Bit 3, to 0 for the BUSY pin to be active low, and set it to 1 for the BUSY pin to be active high.

When using the BUSY function of the ALERT/BUSY/GPO_0 pin, an external pull-up resistor is required because the output is an open-drain configuration. Connect the external pull-up resistor to V_{DRIVE}. The resistor value is application dependent; however, it must be large enough to avoid excessive sink currents when the BUSY function of the ALERT/BUSY/GPO_0 pin is triggered.

CHANNEL SEQUENCER

The AD7091R-2/AD7091R-4/AD7091R-8 include a channel sequencer that is useful for scanning channels in a repeated fashion. Channels included in the sequence are configured in the channel register. If all the bits in the channel register are 0, Channel 0 is selected by default, and all conversions happen on this channel. If the channel register is nonzero, the conversion sequence starts from the lowest numbered channel enabled in the channel register. The sequence cycles through all the enabled channels in ascending order. After all the channels in the sequence are converted, the sequence starts again.

There is a latency of one conversion before the channel conversion sequence is updated. If the channel register is programmed with a new value, the conversion sequence is reset to the lowest numbered channel in the new value.

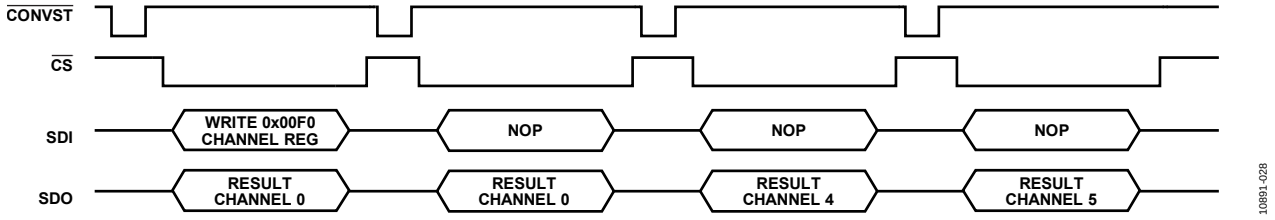


Figure 55. Channel Sequencer

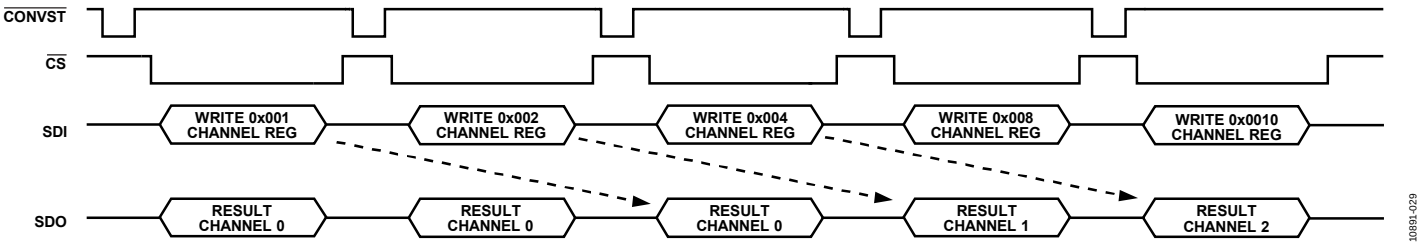


Figure 56. Channel Sequencer Multiple Channel Write

DAISY CHAIN

Daisy-chain mode is intended for applications where multiple AD7091R-2/AD7091R-4/AD7091R-8 devices are used. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity.

All ADC slaves are addressed by the same $\overline{CS}$, $\overline{CONVST}$, and SCLK signals. The SDI of the first AD7091R-2/AD7091R-4/AD7091R-8 slave in the chain is driven directly by the master output, slave input (MOSI) pin of the SPI master. The SDO of the first slave is connected to the SDI of the second slave. All the subsequent slaves are connected in this fashion, and the SDO of the last slave drives the master input, slave output (MISO) pin of the master. A connection diagram example using two AD7091R-2/AD7091R-4/AD7091R-8 devices is shown in Figure 57.

Each AD7091R-2/AD7091R-4/AD7091R-8 slave in the chain requires a 16-bit SPI command. If there are N slaves, each SPI frame must have N × 16 bits of data. In the AD7091R-2/AD7091R-4/AD7091R-8, when the bit counter crosses 16 bits, all of the received bits are sent out over the SDO. The output from the first slave is the input of the second slave. Effectively, each slave ignores all the incoming 16-bit SPI commands except the last one. The SPI command received just before the $\overline{CS}$ rising edge is the only valid SPI command for a given device in the daisy chain. The output on the next SPI frame is determined by the valid SPI command or any conversion event.

The methods for reading a conversion result to configuring the slave registers are outlined in Figure 58 to Figure 62 for a two-slave example. Additional slave devices can be added to the chain by following the same principles defined for the two-device configuration.

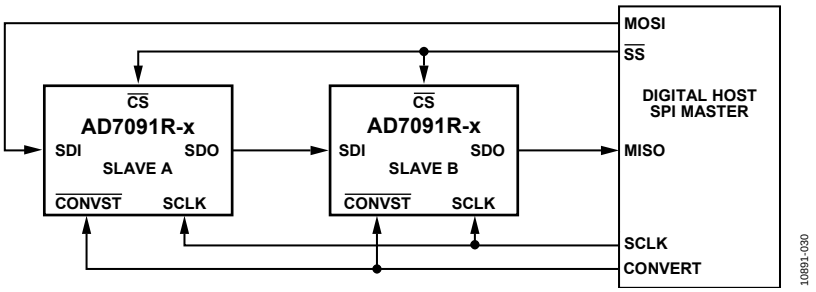


Figure 57. Daisy-Chain Configuration

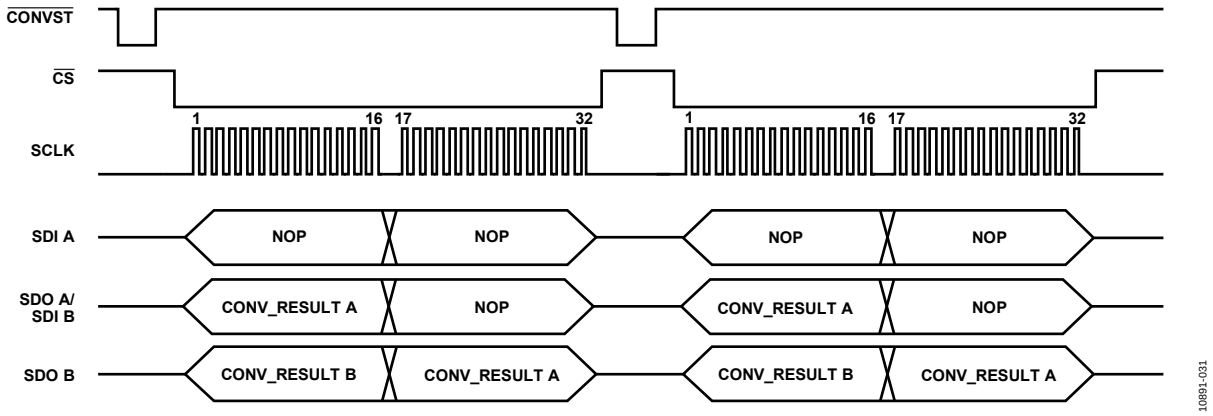


Figure 58. Conversion in a Two-Slave Daisy-Chain Mode Configuration

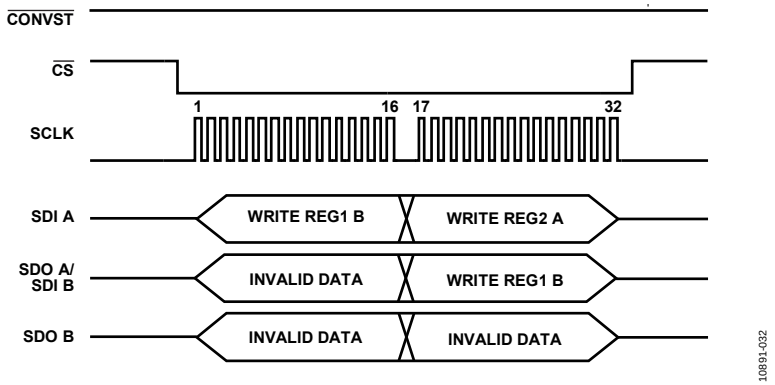


Figure 59. Single Register Write in a Two-Slave Daisy-Chain Mode Configuration

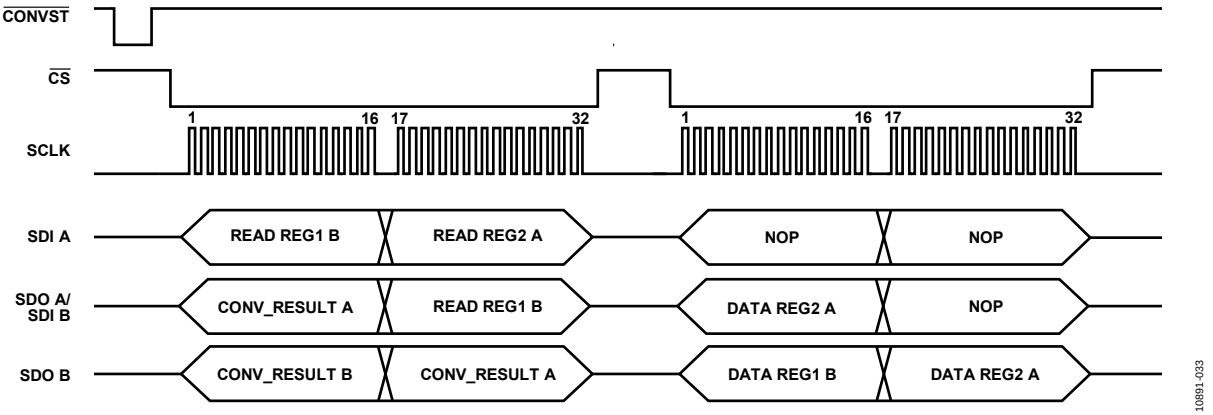


Figure 60. Single Register Read in a Two-Slave Daisy-Chain Mode Configuration

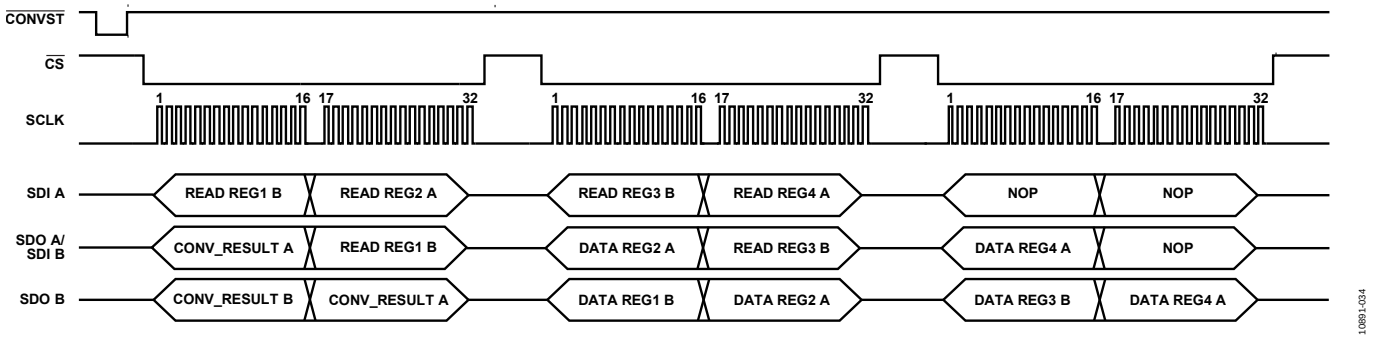


Figure 61. Multiple Register Read in a Two-Slave Daisy-Chain Mode Configuration

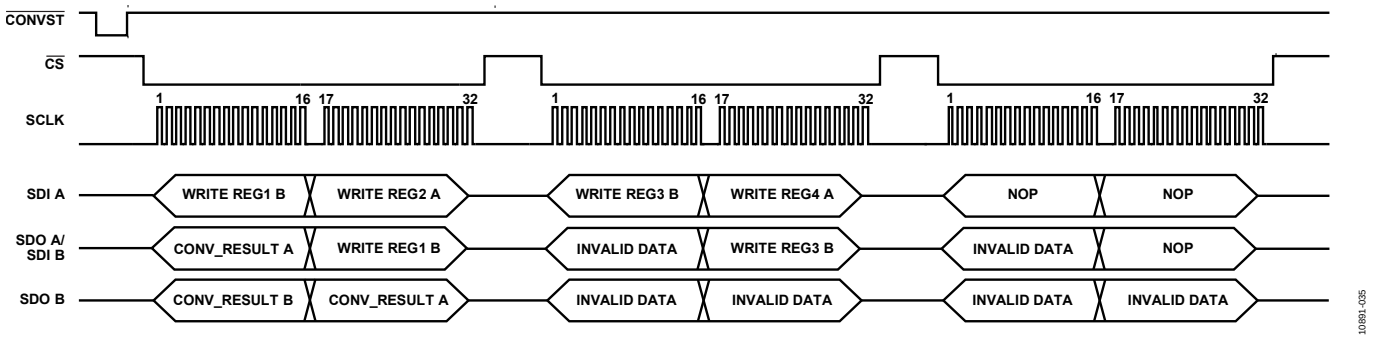
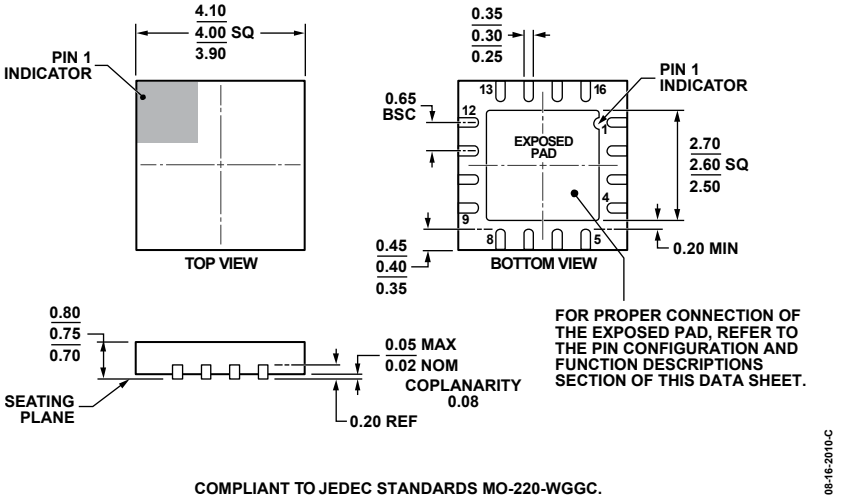


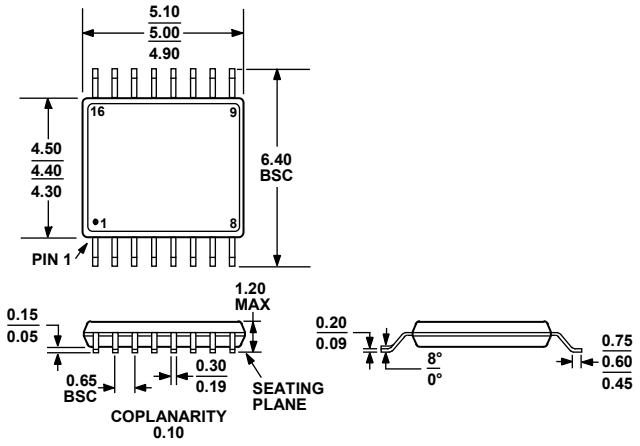
Figure 62. Multiple Register Write in a Two-Slave Daisy-Chain Mode Configuration

OUTLINE DIMENSIONS



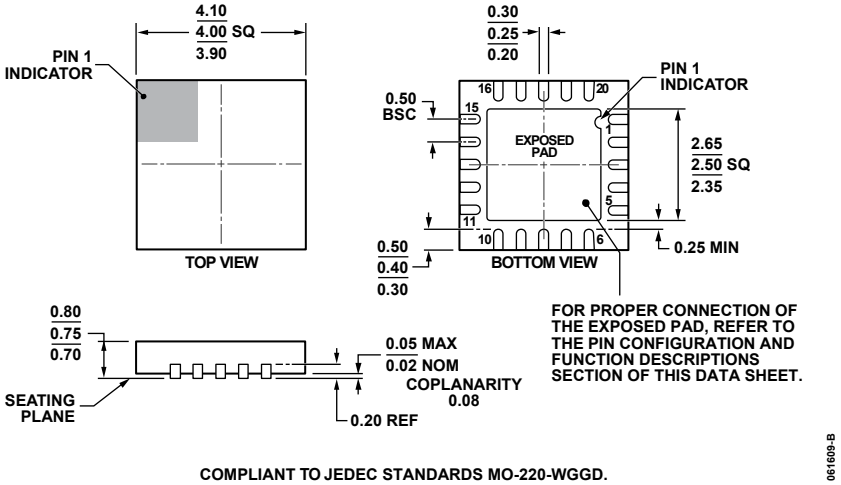
COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 63. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-17)
Dimensions shown in millimeters



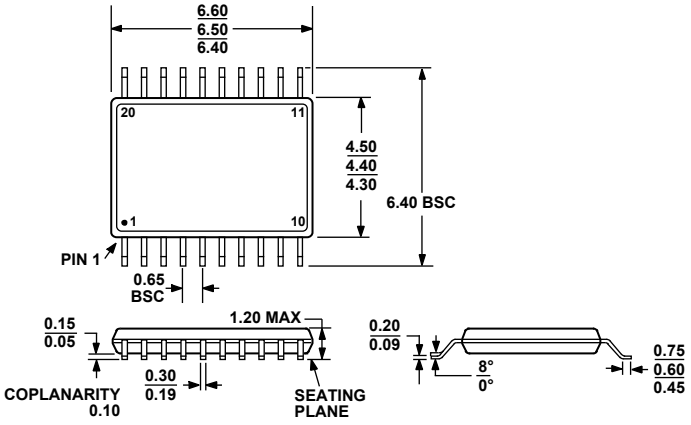
COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 64. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



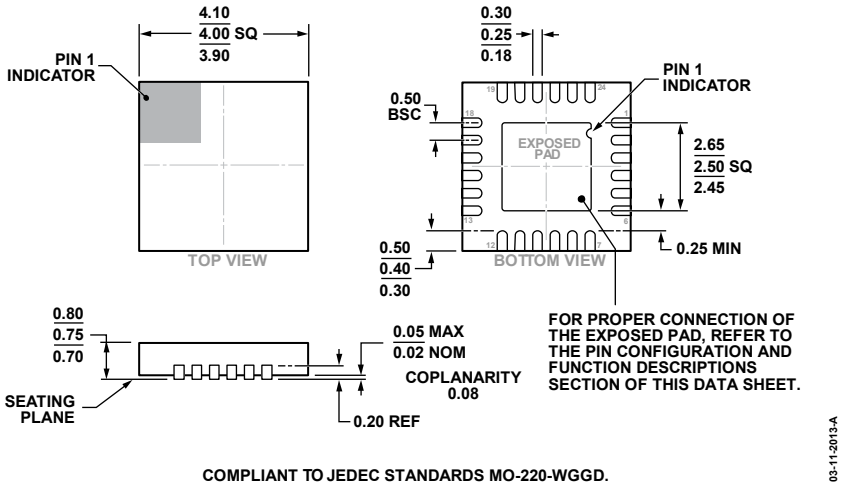
COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 65. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-10)
Dimensions shown in millimeters



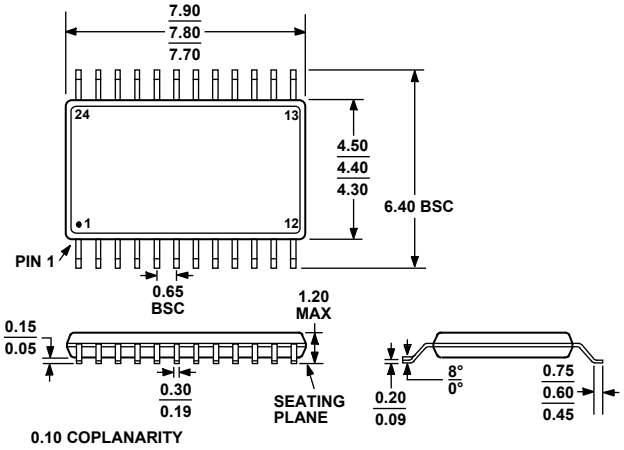
COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 66. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 67. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-7)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 68. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Channels	Temperature Range	Package Description	Package Option
AD7091R-2BCPZ	2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17
AD7091R-2BCPZ-RL7	2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17
AD7091R-2BRUZ	2	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD7091R-2BRUZ-RL7	2	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
EVAL-AD7091R-2SDZ			Evaluation Board	
AD7091R-4BCPZ	4	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD7091R-4BCPZ-RL7	4	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD7091R-4BRUZ	4	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD7091R-4BRUZ-RL7	4	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
EVAL-AD7091R-4SDZ			Evaluation Board	
AD7091R-8BCPZ	8	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-7
AD7091R-8BCPZ-RL7	8	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-7
AD7091R-8BRUZ	8	−40°C to +125°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7091R-8BRUZ-RL7	8	−40°C to +125°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
EVAL-AD7091R-8SDZ			Evaluation Board	
EVAL-SDP-CB1Z			Evaluation Controller Board	

[1] Z = RoHS Compliant Part.

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