12-Bit ADC in 6-Lead SOT-23

AD7476-EP

FEATURES

Specified for V_{DD} of 2.35 V to 5.25 V
Low power
3.6 mW at 600 kSPS with 3 V supplies
15 mW at 600 kSPS with 5 V supplies
Wide input bandwidth
70 dB SNR at 100 kHz input frequency
High speed serial interface
SPI/QSPI™/MICROWIRE™/DSP compatible
Standby mode: 1 µA maximum
6-lead SOT-23 package

ENHANCED PRODUCT FEATURES

Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available upon request

APPLICATIONS

Battery-powered systems
Personal digital assistants
Medical instruments
Mobile communications
Instrumentation and control systems
Data acquisition systems

GENERAL DESCRIPTION

The AD7476[1] is a 12-bit, high speed, low power, successive approximation ADC. The part operates from a single 2.35 V to 5.25 V power supply and features throughput rates up to 600 kSPS. The part contains a low noise, wide bandwidth, track-and-hold amplifier that can handle input frequencies in excess of 6 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the device to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is initiated at this point. There are no pipeline delays associated with this part.

The AD7476 uses advanced design techniques to achieve very low power dissipation at high throughput rates.

[1] Protected by U.S. Patent No. 6,681,332.

FUNCTIONAL BLOCK DIAGRAM

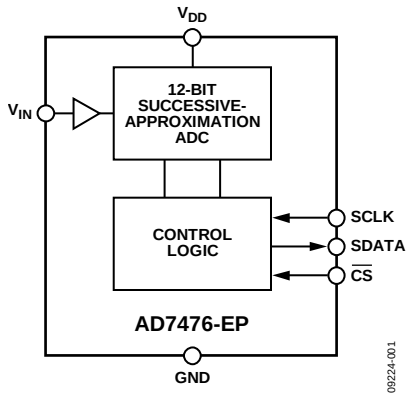

Figure 1.

The reference for the part is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC. Thus, the analog input range for the part is 0 V to V_{DD}. The conversion rate is determined by the SCLK pin.

Additional application and technical information can be found in the AD7476 data sheet.

PRODUCT HIGHLIGHTS

1. First 12-Bit ADC in a SOT-23 Package.
2. High Throughput with Low Power Consumption.
3. Flexible Power/Serial Clock Speed Management. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced while not converting. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Current consumption is 1 µA maximum when in shutdown mode.
4. Reference Derived from the Power Supply.
5. No Pipeline Delay. The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

Rev. 0

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REVISION HISTORY

8/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 12 MHz, f_{SAMPLE} = 600 kSPS, unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	S Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 100 kHz sine wave
Signal-to-(Noise + Distortion) (SINAD)	69	dB min	
	70	dB min	T_A = 25°C
Signal-to-Noise Ratio (SNR)	70	dB min	
Total Harmonic Distortion (THD)	−78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)	−80	dB typ	
Intermodulation Distortion (IMD)			
Second-Order Terms	−78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Third-Order Terms	−78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	6.5	MHz typ	At 3 dB
DC ACCURACY			V_{DD} = (2.35 V to 3.6 V)[1]
Resolution	12	Bits	
Integral Nonlinearity	±1.5	LSB max	
	±0.6	LSB typ	
Differential Nonlinearity	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits
	±0.75	LSB typ	
Offset Error	±2	LSB max	
		LSB typ	
Gain Error	±2	LSB max	
		LSB typ	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUT			
Input High Voltage, V_{INH}	2.4	V min	
	1.8	V min	V_{DD} = 2.35 V
Input Low Voltage, V_{INL}	0.4	V max	V_{DD} = 3 V
	0.8	V max	V_{DD} = 5 V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[2]	10	pF max	
LOGIC OUTPUT			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[2]	10	pF max	
Output Coding	Straight (natural) binary		
CONVERSION RATE			
Conversion Time	1.33	µs max	16 SCLK cycles
Track-and-Hold Acquisition Time	500	ns max	Full-scale step input
	400	ns max	Sine wave input ≤ 100 kHz
Throughput Rate	600	kSPS max	

Parameter	S Version	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	2.35/5.25	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2	mA typ	V_{DD} = 4.75 V to 5.25 V, SCLK on or off
	1	mA typ	V_{DD} = 2.35 V to 3.6 V, SCLK on or off
Normal Mode (Operational)	3	mA max	V_{DD} = 4.75 V to 5.25 V, $f_{SAMPLE} = f_{SAMPLE}MAX$[3]
	1.4	mA max	V_{DD} = 2.35 V to 3.6 V, $f_{SAMPLE} = f_{SAMPLE}MAX$[4]
Full Power-Down Mode	1	µA max	SCLK off
	80	µA max	SCLK on
Power Dissipation			
Normal Mode (Operational)	15	mW max	V_{DD} = 5 V, $f_{SAMPLE} = f_{SAMPLE}MAX$[4]
	4.2	mW max	V_{DD} = 3 V, $f_{SAMPLE} = f_{SAMPLE}MAX$[4]
Full Power-Down	5	µW max	V_{DD} = 5 V, SCLK off
	3	µW max	V_{DD} = 3 V, SCLK off

[1] S version specifications apply as typical figures when V_{DD} = 5.25 V.
[2] Guaranteed by characterization.
[3] $f_{SAMPLE}MAX$ = 600 kSPS.

TIMING SPECIFICATIONS

V_{DD} = 2.35 V to 5.25 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

	Limit at T_{MIN}, T_{MAX}[1]			
Parameter[2]	**3 V**	**5 V**	**Unit**	**Description**
f_{SCLK}[3]	10	10	kHz min	
	12	12	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}		
t_{QUIET}	50	50	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_1	10	10	ns min	Minimum $\overline{CS}$ pulse width
t_2	10	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[4]	20	20	ns max	Delay from $\overline{CS}$ until SDATA three-state disabled
t_4[4]	40	20	ns max	Data access time after SCLK falling edge, A version
	70	20	ns max	Data access time after SCLK falling edge, B version
t_5	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	10	10	ns min	SCLK to data valid hold time
t_8[5]	10	10	ns min	SCLK falling edge to SDATA high impedance
	25	25	ns max	SCLK falling edge to SDATA high impedance
$t_{POWER-UP}$	1	1	µs typ	Power-up time from full power-down

[1] 3 V specifications apply from V_{DD} = 2.35 V to 3.6 V; 5 V specifications apply from V_{DD} = 4.75 V to 5.25 V.
[2] Guaranteed by characterization. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[3] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[4] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[5] t_8 is derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, is the true bus relinquish time of the part and is independent of the bus loading.

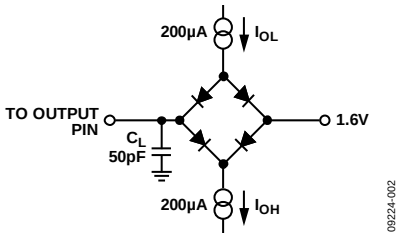


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Enhanced Plastic (EP Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOT-23 Package	
θ_{JA} Thermal Impedance	230°C/W
θ_{JC} Thermal Impedance	92°C/W
Lead Temperature, Soldering Reflow	
(10 sec to 30 sec)	235 (0/+5)°C
Pb-free Temperature Soldering Reflow	255 (0/+5)°C
ESD	3.5 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

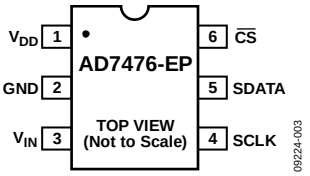


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7476-EP is from 2.35 V to 5.25 V.
2	GND	Analog Ground. Ground reference point for all circuitry on the part. All analog input signals should be referred to this GND voltage.
3	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to V_{DD}.
4	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7476-EP conversion process.
5	SDATA	Data Out. Logic output. The conversion result is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7476-EP consists of four leading zeros followed by the 12 bits of conversion data; this is provided MSB first.
6	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7476-EP and framing the serial data transfer.

TYPICAL PERFORMANCE CHARACTERISTICS

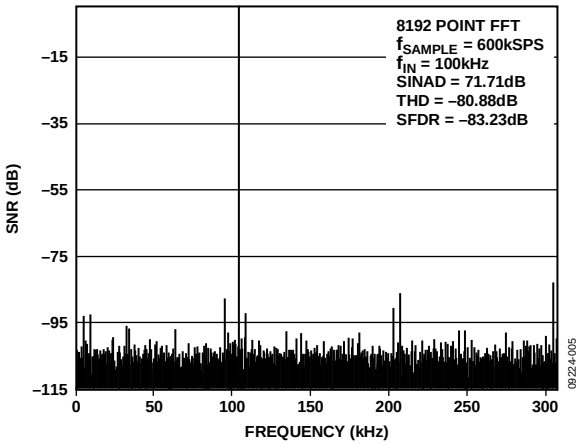


Figure 4. AD7476-EP Dynamic Performance at 600 kSPS

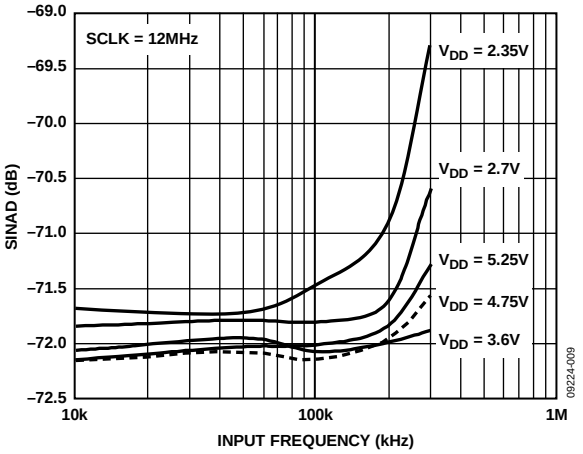
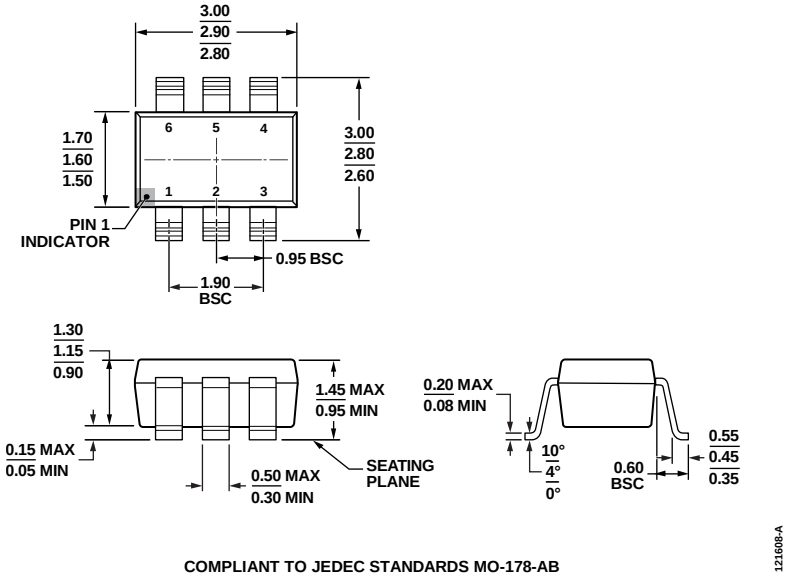


Figure 5. AD7476-EP SINAD vs. Input Frequency at 605 kSPS

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 6. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error (LSB)[2]	Package Description	Package Option	Branding
AD7476SRTZ-EP-RL7	−55°C to +125°C	±1.5 maximum	6-Lead SOT-23	RJ-6	C73#

[1] Z = RoHS Compliant Part, # denotes RoHS compliant part maybe top or bottom marked.
[2] Linearity error refers to integral linearity error.

NOTES

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