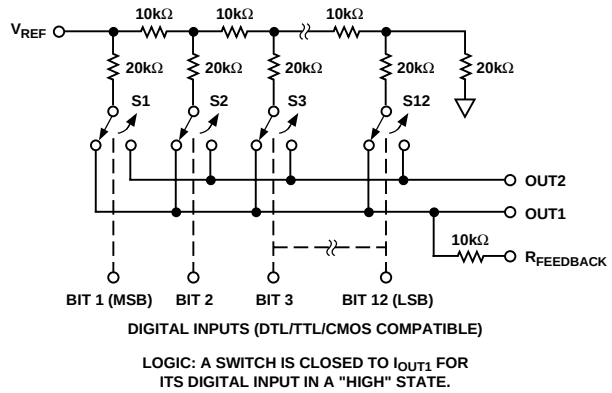
CMOS 12-Bit Monolithic Multiplying DAC

AD7541A

FEATURES
Improved Version of AD7541
Full Four-Quadrant Multiplication
12-Bit Linearity (Endpoint)
All Parts Guaranteed Monotonic
TTL/CMOS Compatible
Low Cost
Protection Schottky Diodes Not Required
Low Logic Input Leakage

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices AD7541A is a low cost, high performance 12-bit monolithic multiplying digital-to-analog converter. It is fabricated using advanced, low noise, thin film on CMOS technology and is available in a standard 18-lead DIP and in 20-terminal surface mount packages.

The AD7541A is functionally and pin compatible with the industry standard AD7541 device and offers improved specifications and performance. The improved design ensures that the device is latch-up free so no output protection Schottky diodes are required.

This new device uses laser wafer trimming to provide full 12-bit endpoint linearity with several new high performance grades.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy T_{MIN} to T_{MAX}	Gain Error T_A = +25°C	Package Options[3]
AD7541AJN	0°C to +70°C	±1 LSB	±6 LSB	N-18
AD7541AKN	0°C to +70°C	±1/2 LSB	±1 LSB	N-18
AD7541AJP	0°C to +70°C	±1 LSB	±6	P-20A
AD7541AKP	0°C to +70°C	±1/2 LSB	±1	P-20A
AD7541AKR	0°C to +70°C	±1/2 LSB	±1	R-18
AD7541AAQ	–25°C to +85°C	±1 LSB	±6 LSB	Q-18
AD7541ABQ	–25°C to +85°C	±1/2 LSB	±1 LSB	Q-18
AD7541ASQ	–55°C to +125°C	±1 LSB	±6 LSB	Q-18
AD7541ATQ	–55°C to +125°C	±1/2 LSB	±1 LSB	Q-18
AD7541ASE	–55°C to +125°C	±1 LSB	±6 LSB	E-20A
AD7541ATE	–55°C to +125°C	±1/2 LSB	±1 LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-18) or cerdip (Q-18) hermetic packages.
[2]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline IC.

PRODUCT HIGHLIGHTS

Compatibility: The AD7541A can be used as a direct replacement for any AD7541-type device. As with the Analog Devices AD7541, the digital inputs are TTL/CMOS compatible and have been designed to have a ±1 μA maximum input current requirement so as not to load the driving circuitry.

Improvements: The AD7541A offers the following improved specifications over the AD7541:

1. Gain Error for all grades has been reduced with premium grade versions having a maximum gain error of ±3 LSB.
2. Gain Error temperature coefficient has been reduced to 2 ppm/°C typical and 5 ppm/°C maximum.
3. Digital-to-analog charge injection energy for this new device is typically 20% less than the standard AD7541 part.
4. Latch-up proof.
5. Improvements in laser wafer trimming provides 1/2 LSB max differential nonlinearity for top grade devices over the operating temperature range (vs. 1 LSB on older 7541 types).
6. All grades are guaranteed monotonic to 12 bits over the operating temperature range.

REV. B

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AD7541A–SPECIFICATIONS (V_{DD} = +15 V, V_{REF} = +10 V; OUT 1 = OUT 2 = GND = 0 V unless otherwise noted)

Parameter	Version	T_A = +25°C	T_A = T_{MIN}, T_{MAX}[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J, A, S	±1	±1	LSB max	±1 LSB = ±0.024% of Full Scale
	K, B, T	±1/2	±1/2	LSB max	±1/2 LSB = ±0.012% of Full Scale
Differential Nonlinearity	J, A, S	±1	±1	LSB max	All Grades Guaranteed Monotonic
	K, B, T	±1/2	±1/2	LSB max	to 12 Bits, T_{MIN} to T_{MAX}.
Gain Error	J, A, S	±6	±8	LSB max	Measured Using Internal R_{FB} and Includes
	K, B, T	±3	±5	LSB max	Effect of Leakage Current and Gain TC.
					Gain Error Can Be Trimmed to Zero.
Gain Temperature Coefficient[2]					
ΔGain/ΔTemperature	All	5	5	ppm/°C max	Typical Value Is 2 ppm/°C.
Output Leakage Current					
OUT1 (Pin 1)	J, K	±5	±10	nA max	All Digital Inputs = 0 V.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
OUT2 (Pin 2)	J, K	±5	±10	nA max	All Digital Inputs = V_{DD}.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
REFERENCE INPUT					
Input Resistance (Pin 17 to GND)	All	7–18	7–18	kΩ min/max	Typical Input Resistance = 11 kΩ. Typical Input Resistance Temperature Coefficient = –300 ppm/°C.
DIGITAL INPUTS					
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	V min	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	μA max	Logic Inputs Are MOS Gates. I_{IN} typ (25°C) = 1 nA.
C_{IN} (Input Capacitance)[2]	All	8	8	pF max	V_{IN} = 0 V
POWER SUPPLY REJECTION					
$\Delta Gain/\Delta V_{DD}$	All	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min/V max	Accuracy Is Not Guaranteed Over This Range.
I_{DD}	All	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}.
		100	500	μA max	All Digital Inputs 0 V or V_{DD}.

AC PERFORMANCE CHARACTERISTICS

These Characteristics are included for Design Guidance only and are not subject to test. V_{DD} = +15 V, V_{IN} = +10 V except where noted, OUT1 = OUT2 = GND = 0 V, Output Amp is AD544 except where noted.

Parameter	Version[1]	T_A = +25°C	T_A = T_{MIN}, T_{MAX}[1]	Units	Test Conditions/Comments
PROPAGATION DELAY (From Digital Input Change to 90% of Final Analog Output)	All	100	—	ns typ	OUT 1 Load = 100 Ω, C_{EXT} = 13 pF. Digital Inputs = 0 V to V_{DD} or V_{DD} to 0 V.
DIGITAL TO ANALOG GLITCH IMPULSE	All	1000	—	nV-sec typ	V_{REF} = 0 V. All digital inputs 0 V to V_{DD} or V_{DD} to 0 V. Measured using Model 50K as output amplifier.
MULTIPLYING FEEDTHROUGH ERROR[3] (V_{REF} to OUT1)	All	1.0	—	mV p-p typ	V_{REF} = ±10 V, 10 kHz sine wave.
OUTPUT CURRENT SETTLING TIME	All	0.6	—	μs typ	To 0.01% of full-scale range. OUT 1 Load = 100 Ω, C_{EXT} = 13 pF. Digital Inputs = 0 V to V_{DD} or V_{DD} to 0 V.
OUTPUT CAPACITANCE					
C_{OUT1} (Pin 1)	All	200	200	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	70	70	pF max	= V_{IH}
C_{OUT1} (Pin 1)	All	70	70	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	200	200	pF max	= V_{IL}

NOTES
[1]Temperature range as follows: J, K versions, 0°C to +70°C; A, B versions, –25°C to +85°C; S, T versions, –55°C to +125°C.
[2]Guaranteed by design but not production tested.
[3]To minimize feedthrough in the ceramic package (Suffix D) the user must ground the metal lid.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to GND	+17 V
V_{REF} to GND	±25 V
V_{RFB} to GND	±25 V
Digital Input Voltage to GND	–0.3 V, V_{DD} + 0.3 V
OUT 1, OUT 2 to GND	–0.3 V, V_{DD} + 0.3 V
Power Dissipation (Any Package)	
To +75°C	450 mW
Derates above +75°C	6 mW/°C
Operating Temperature Range	
Commercial (J, K Versions)	0°C to +70°C
Industrial (A, B Versions)	–25°C to +85°C
Extended (S, T Versions)	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7541A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full-scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* l LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range insures monotonicity.

GAIN ERROR

Gain error is a measure of the output error between an ideal DAC and the actual device output. For the AD7541A, ideal maximum output is

$$-\left(\frac{4095}{4096}\right)(V_{REF}).$$

Gain error is adjustable to zero using external trims as shown in Figures 4, 5 and 6.

OUTPUT LEAKAGE CURRENT

Current which appears at OUTI with the DAC loaded to all 0s or at OUT2 with the DAC loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC loaded to all 0s.

OUTPUT CURRENT SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to full scale.

PROPAGATION DELAY

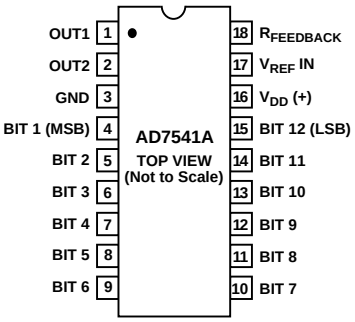
This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL-TO-ANALOG CHARGE INJECTION (QDA)

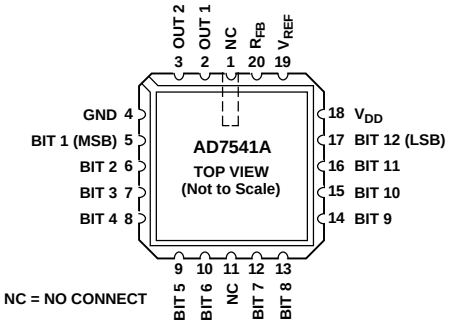
This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV secs and is measured with V_{REF} = GND and a Model 50K as the output op amp, C1 (phase compensation) = 0 pF.

PIN CONFIGURATIONS

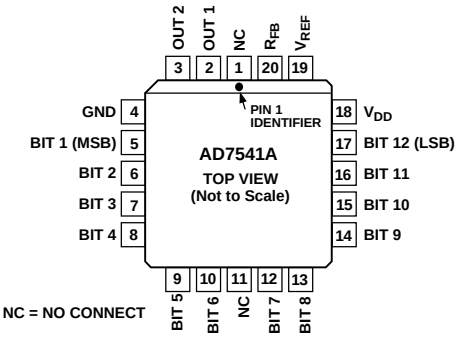
DIP/SOIC



LCCC



PLCC



GENERAL CIRCUIT INFORMATION

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

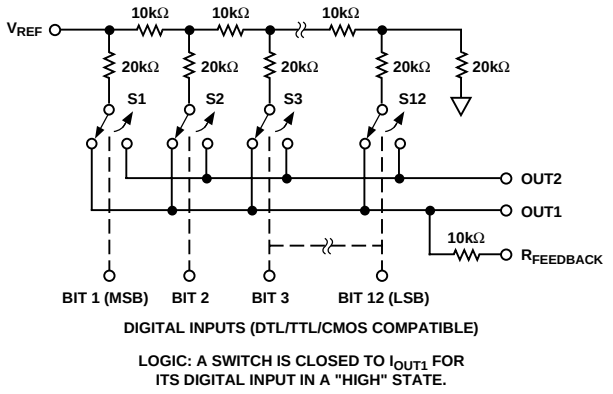


Figure 1. Functional Diagram (Inputs HIGH)

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 2 and 3. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the $I/_{4096}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The ON capacitance of the output N-channel switch is 200 pF, as shown on the OUT2 terminal. The OFF switch capacitance is 70 pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 3 is similar to Figure 2; however, the ON switches are now on terminal OUT1, hence the 200 pF at that terminal.

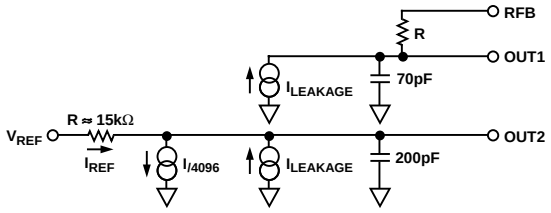


Figure 2. DAC Equivalent Circuit All Digital Inputs LOW

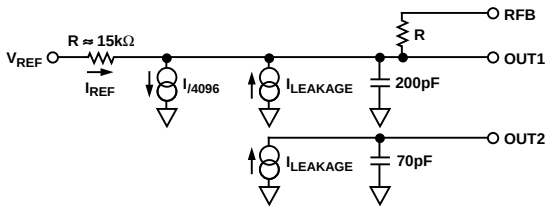


Figure 3. DAC Equivalent Circuit All Digital Inputs HIGH

APPLICATIONS

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at Pin 17, the circuit is a unipolar D/A converter. With an ac reference voltage or current, the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full-scale trim capability [i.e., load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 pF to 25 pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq$ 10% of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 11 kΩ). The AD544L is a high speed implanted FET input op amp with low factory-trimmed V_{OS}.

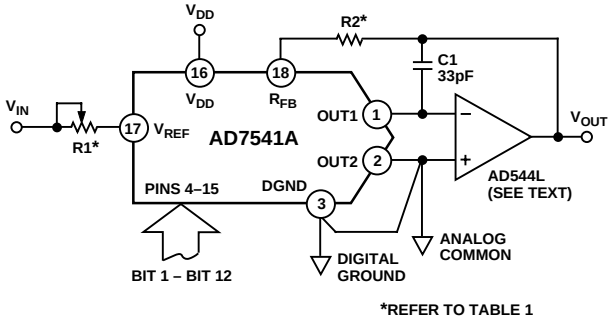


Figure 4. Unipolar Binary Operation

Table I. Recommended Trim Resistor Values vs. Grades

Trim Resistor	JN/AQ/SD	KN/BQ/TD
R1	100 Ω	100 Ω
R2	47 Ω	33 Ω

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Binary Number in DAC MSB		LSB	Analog Output, V_{OUT}
1 1 1 1	1 1 1 1	1 1 1 1	$-V_{IN}\left(\frac{4095}{4096}\right)$
1 0 0 0	0 0 0 0	0 0 0 0	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0 0 0 0	0 0 0 0	0 0 0 1	$-V_{IN}\left(\frac{1}{4096}\right)$
0 0 0 0	0 0 0 0	0 0 0 0	0 Volts

BIPOLAR OPERATION
(4-QUADRANT MULTIPLICATION)

Figure 5 and Table III illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference the circuit provides full 4-quadrant multiplication.

With the DAC loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0 V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0 V). Full-scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and full-scale error. Mismatch of R5 to R4 or 2R3 causes full-scale error. C1 phase compensation (10 pF to 50 pF) may be required for stability, depending on amplifier used.

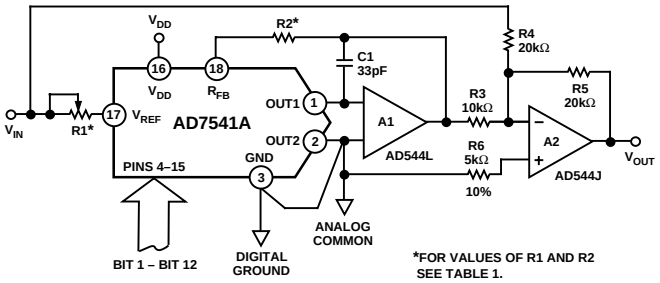


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

Binary Number in DAC MSB LSB	Analog Output, V_{OUT}
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0 Volts
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{2048}{2048}\right)$

Figure 6 and Table IV show an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage of giving 12-bit resolution in each quadrant, compared with 11-bit resolution per quadrant for the circuit of Figure 5. The AD7592 is a fully protected CMOS changeover switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error.

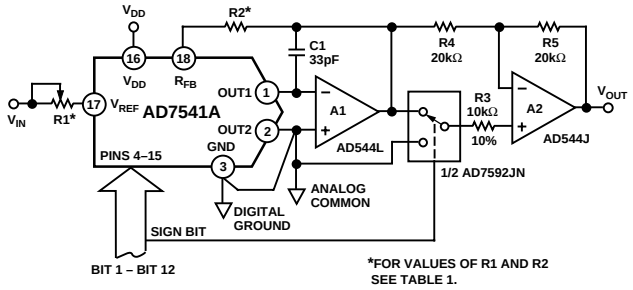


Figure 6. 12-Bit Plus Sign Magnitude Operation

Table IV. 12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 6

Sign Bit	Binary Number in DAC MSB LSB	Analog Output, V_{OUT}
0	1 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN}\times\left(\frac{4095}{4096}\right)$
0	0 0 0 0 0 0 0 0 0 0 0 0	0 Volts
1	0 0 0 0 0 0 0 0 0 0 0 0	0 Volts
1	1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN}\times\left(\frac{4095}{4096}\right)$

Note: Sign bit of "0" connects R3 to GND.

APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code-dependent output resistance which in turn can cause a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50 μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

Digital Glitches: One cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and OUT2 terminals. This should be minimized by screening the analog pins of the AD7541A (Pins 1, 2, 17, 18) from the digital pins by a ground track run between Pins 2 and 3 and between Pins 16 and 17 of the AD7541A. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and GND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital-to-analog sections of the AD7541A, particularly in circuits with high currents and fast rise and fall times.

Temperature Coefficients: The gain temperature coefficient of the AD7541A has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSBs, respectively, over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full-scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs," Publication Number E630c-5-3/86.

SINGLE SUPPLY OPERATION

Figure 7 shows the AD7541A connected in a voltage switching mode. OUT1 is connected to the reference voltage and OUT2 is connected to GND. The D/A converter output voltage is available at the V_{REF} pin (Pin 17) and has a constant output impedance equal to R_{LDR}. The feedback resistor R_{FB} is not used in this circuit.

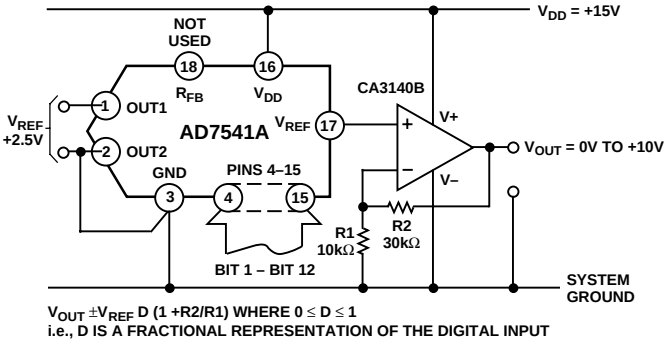


Figure 7. Single Supply Operation Using Voltage Switching Mode

The reference voltage must always be positive. If OUT1 goes more than 0.3 V less than GND, an internal diode will be turned on and a heavy current may flow causing device damage (the AD7541A is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices). Suitable references include the AD580 and AD584.

The loading on the reference voltage source is code-dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions. To maintain linearity, the voltage at OUT1 should remain within 2.5 V of GND, for a V_{DD} of 15 V. If V_{DD} is reduced from 15 V or the reference voltage at OUT1 increased to more than 2.5 V, the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded.

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters, the reader is referred to the following texts:

CMOS DAC Application Guide, Publication Number G872b-8-1/89 available from Analog Devices.

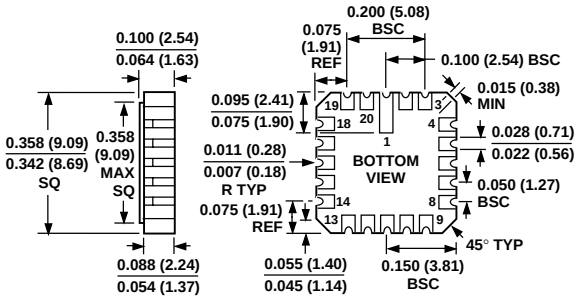
Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs Application Note, Publication Number E630c-5-3/86 available from Analog Devices.

Analog-Digital Conversion Handbook—available from Analog Devices.

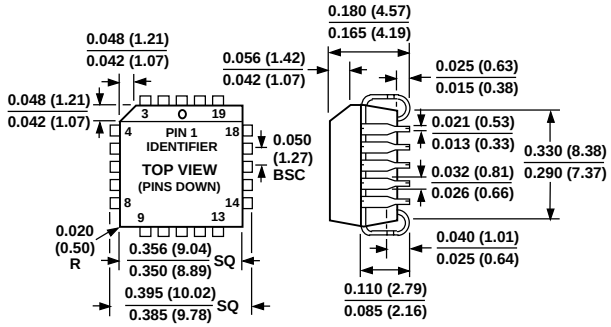
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

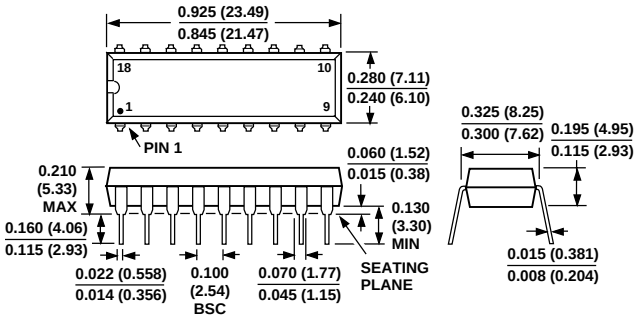
20-Terminal Ceramic Leadless Chip Carrier (E-20A)



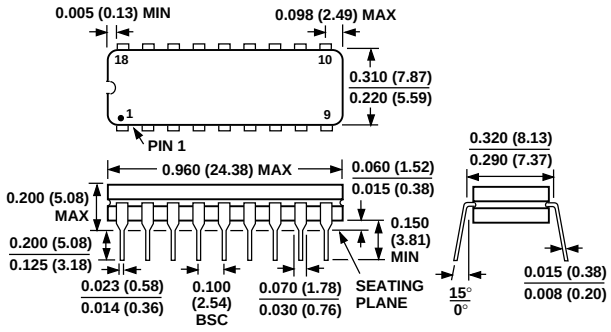
20-Lead Plastic Leadless Chip Carrier (P-20A)



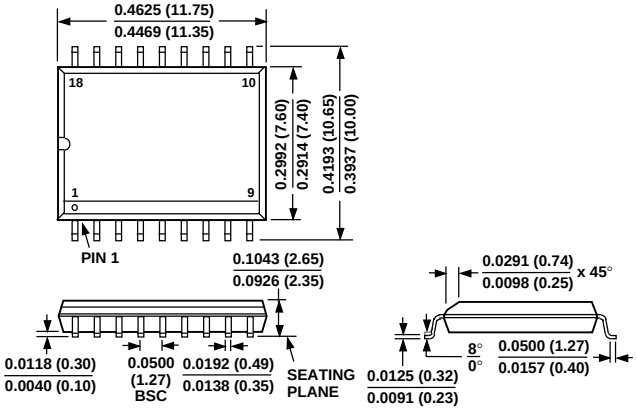
18-Lead Plastic DIP (N-18)



18-Lead Cerdip (Q-18)



18-Lead SOIC (R-18)



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