

**FEATURES**

Two Doubled Buffered 12-Bit DACs  
 4-Quadrant Multiplication  
 Low Gain Error (3LSBs max)  
 DAC Ladder Resistance Matching: 1%  
 Space Saving Skinny DIP and Surface Mount Packages  
 Latch-Up Proof  
 Extended Temperature Range Operation

**APPLICATIONS**

Programmable Filters  
 Automatic Test Equipment  
 Microcomputer Based Process Control  
 Audio Systems  
 Programmable Power Supplies  
 Synchro Applications

**GENERAL DESCRIPTION**

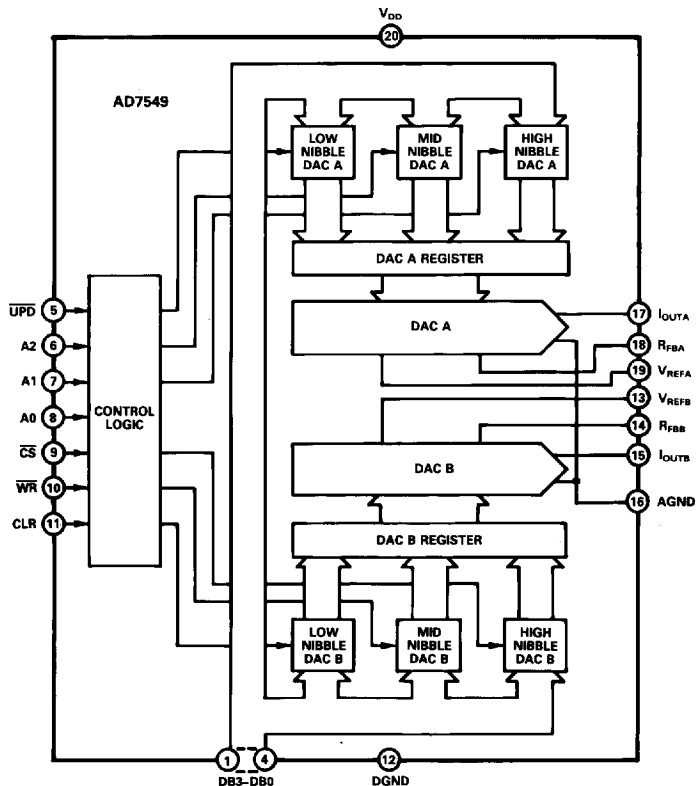
The AD7549 is a monolithic dual, 12-bit, current output D/A converter. It is packaged in both 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages. Both DACs provide four quadrant multiplication capabilities with a separate reference input and feedback resistor for each DAC. The monolithic construction ensures excellent thermal tracking and gain error tracking between the two DACs.

The DACs in the AD7549 are each loaded in three 4-bit nibbles. The control logic is designed for easy processor interfacing. Input and DAC register loading is accomplished using address lines A0, A1, A2 and  $\overline{CS}$ ,  $\overline{WR}$  lines. A logic high level on the CLR input clears all registers. Both DACs may be simultaneously updated using the  $\overline{UPD}$  input.

The AD7549 is manufactured using the Linear Compatible CMOS (LC<sup>2</sup>MOS) process. It is speed compatible with most microprocessors and accepts TTL, 74HC or 5V CMOS logic level inputs.

**REV. A**

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**FUNCTIONAL BLOCK DIAGRAM**

**PRODUCT HIGHLIGHTS**

1. Small package size: the loading structure adopted for the AD7549 enables two 12-Bit DACs to be packaged in either a small 20-pin 0.3" DIP or in 20-terminal surface mount packages.
2. DAC to DAC matching: since both DACs are fabricated on the same chip, precise matching and tracking is inherent. This opens up applications which otherwise would not be considered, i.e., Programmable Filters, Audio Systems, etc.

# AD7549—SPECIFICATIONS<sup>1</sup> ( $V_{DD} = +15V \pm 5\%$ , $V_{REFA} = V_{REFB} = 10V$ ; $I_{OUTA} = I_{OUTB} = AGND = 0V$ . All specifications $T_{min}$ to $T_{max}$ unless otherwise specified.)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
<b>ACCURACY</b>						
Resolution	12	12	12	12	Bits	All grades guaranteed monotonic over temperature.
Relative Accuracy	$\pm 1$	$\pm 1/2$	$\pm 1$	$\pm 1/2$	LSB max	
Differential Nonlinearity	$\pm 1$	$\pm 1$	$\pm 1$	$\pm 1$	LSB max	
Full Scale Error	$\pm 6$	$\pm 3$	$\pm 6$	$\pm 3$	LSB max	
Gain Temperature Coefficient <sup>2</sup> ; $\Delta$ Gain/ $\Delta$ Temperature	$\pm 5$	$\pm 5$	$\pm 5$	$\pm 5$	ppm/ $^{\circ}$ C max	Typical value is 1ppm/ $^{\circ}$ C
<b>Output Leakage Current</b>						
$I_{OUTA}$ (Pin 17) +25 $^{\circ}$ C	20	20	20	20	nA max	DAC A Register loaded with all 0's
$T_{min}$ to $T_{max}$	150	150	250	250	nA max	
$I_{OUTB}$ (Pin 15) +25 $^{\circ}$ C	20	20	20	20	nA max	DAC B Register loaded with all 0's
$T_{min}$ to $T_{max}$	150	150	250	250	nA max	
<b>REFERENCE INPUT</b>						
Input Resistance (Pin 19, Pin 13)	7 18	7 18	7 18	7 18	k $\Omega$ min k $\Omega$ max	Typical Input Resistance = 11k $\Omega$
$V_{REFA}/V_{REFB}$ Input Resistance Match	$\pm 3$	$\pm 2$	$\pm 3$	$\pm 2$	% max	Typically $\pm 1\%$
<b>DIGITAL INPUTS</b>						
$V_{IH}$ (Input High Voltage)	2.4	2.4	2.4	2.4	V min	$V_{IN} = V_{DD}$
$V_{IL}$ (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
$I_{IN}$ (Input Current) +25 $^{\circ}$ C	$\pm 1$	$\pm 1$	$\pm 1$	$\pm 1$	$\mu$ A max	
$T_{min}$ to $T_{max}$	$\pm 10$	$\pm 10$	$\pm 10$	$\pm 10$	$\mu$ A max	
$C_{IN}$ (Input Capacitance) <sup>3</sup>	7	7	7	7	pF max	
<b>POWER SUPPLY</b>						
$I_{DD}$	5	5	5	5	mA max	

## AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

( $V_{DD} = +15V$ ;  $V_{REFA} = V_{REFB} = +10V$ ,  $I_{OUTA} = I_{OUTB} = AGND = 0V$ , Output Amplifiers are AD644 except where stated.)

Parameter	$T_A = +25^{\circ}$ C	$T_A = T_{MIN}, T_{MAX}$	Units	Test Conditions/Comments
Output Current Settling Time	1.5	—	$\mu$ s max	To 0.01% of full scale range. $I_{OUT}$ load = 100 $\Omega$ ; $C_{EXT} = 13$ pF. DAC output measured from falling edge of WR. Typical value of Settling Time is 0.8 $\mu$ s.
Digital-to-Analog Glitch Impulse	10	—	nV-sec typ	Measured with $V_{REFA} = V_{REFB} = 0V$ , $I_{OUTA}, I_{OUTB}$ load = 100 $\Omega$ , $C_{EXT} = 13$ pF. DAC registers alternately loaded with all 0's and all 1's.
<b>AC Feedthrough<sup>4</sup></b>				
$V_{REFA}$ to $I_{OUTA}$	-70	-65	dB max	$V_{REFA}, V_{REFB} = 20V$ p-p 10kHz sine wave. DAC registers loaded with all 0s.
$V_{REFB}$ to $I_{OUTB}$	-70	-65	dB max	
<b>Power Supply Rejection</b>				
$\Delta$ Gain/ $\Delta V_{DD}$	$\pm 0.01$	$\pm 0.02$	% per % max	$\Delta V_{DD} = \pm 5\%$
<b>Output Capacitance</b>				
$C_{OUTA}$	80	80	pF max	DAC A, DAC B loaded with all 0's.
$C_{OUTB}$	80	80	pF max	
$C_{OUTA}$	160	160	pF max	DAC A, DAC B loaded with all 1's.
$C_{OUTB}$	160	160	pF max	
<b>Channel-to-Channel Isolation</b>				
$V_{REFA}$ to $I_{OUTB}$	-62	—	dB typ	$V_{REFA} = 20V$ p-p 100kHz sine wave, $V_{REFB} = 0V$ $V_{REFB} = 20V$ p-p 100kHz sine wave, $V_{REFA} = 0V$
$V_{REFB}$ to $I_{OUTA}$	-62	—	dB typ	
Digital Crosstalk	10	—	nV-sec typ	Measured for a Code Transition of all 0's to all 1's
Output Noise Voltage Density (10Hz-100kHz)	15	—	nV/ $\sqrt{Hz}$ typ	Measured between $R_{FBA}$ and $I_{OUTA}$ or $R_{FBB}$ and $I_{OUTB}$
Harmonic Distortion	-90	—	dB typ	$V_{IN} = 6V$ rms 1kHz

### NOTES

<sup>1</sup>Temperature range as follows: J, K, Versions: -40 $^{\circ}$ C to +85 $^{\circ}$ C

A, B, Versions: -40 $^{\circ}$ C to +85 $^{\circ}$ C

S, T, Versions: -55 $^{\circ}$ C to +125 $^{\circ}$ C

<sup>2</sup>At  $V_{DD} = 5V$ , the device is fully functional with degraded performance.

<sup>3</sup>Guaranteed by Product Assurance testing.

<sup>4</sup>Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

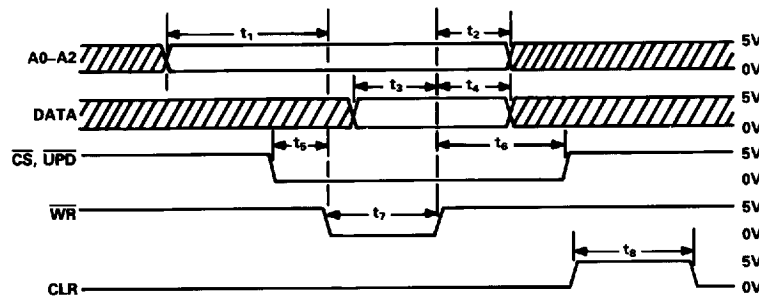
Specifications subject to change without notice.

**TIMING CHARACTERISTICS<sup>1</sup>**

( $V_{DD} = +15V$ ,  $V_{REFA} = V_{RFB} = +10V$ ,  $I_{OUTA} = I_{OUTB} = AGND = 0V$ , unless otherwise stated)

Parameter	Limit at $T_A = 25^\circ C$	Limit at $T_A = -40^\circ C$ to $+85^\circ C$	Limit at $T_A = -55^\circ C$ to $+125^\circ C$	Units	Test Conditions/Comments
$t_1$	50	80	110	ns min	Address Valid to Write Setup Time
$t_2$	0	0	0	ns min	Address Valid to Write Hold Time
$t_3$	180	200	240	ns min	Data Setup Time
$t_4$	0	0	0	ns min	Data Hold Time
$t_5$	20	20	20	ns min	Chip Select or Update to Write Setup Time
$t_6$	0	0	0	ns min	Chip Select or Update to Write Hold Time
$t_7$	170	200	250	ns min	Write Pulse Width
$t_8$	170	200	250	ns min	Clear Pulse Width

Specifications subject to change without notice.



**NOTES**

1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V.  $t_1 = t_4 = 20ns$ .

2. TIMING MEASUREMENT REFERENCE LEVEL IS  $\frac{V_{HI} + V_{LI}}{2}$

**ABSOLUTE MAXIMUM RATINGS\***

( $T_A = +25^\circ C$  unless otherwise noted)

- $V_{DD}$  (Pin 20) to DGND . . . . . -0.3V, +17V
- $V_{REFA}$ ,  $V_{RFB}$  (Pins 19, 13) to AGND . . . . .  $\pm 25V$
- $V_{RFBA}$ ,  $V_{RFB}$  (Pins 18, 14) to AGND . . . . .  $\pm 25V$
- Digital Input Voltage (Pins 1-11)  
to DGND . . . . . -0.3V,  $V_{DD} + 0.3V$
- $V_{PIN15}$ ,  $V_{PIN17}$ , to DGND . . . . . -0.3V,  $V_{DD} + 0.3V$
- AGND to DGND . . . . . -0.3V,  $V_{DD} + 0.3V$
- Power Dissipation (Any Package)  
To  $+75^\circ C$  . . . . . 450mW  
Derates above  $+75^\circ C$  . . . . . 6mW/ $^\circ C$

**Operating Temperature Range**

- Commercial (J, K Versions) . . . . . -40°C to +85°C
- Industrial (A, B Versions) . . . . . -40°C to +85°C
- Extended (S, T Versions) . . . . . -55°C to +125°C
- Storage Temperature . . . . . -65°C to +150°C
- Lead Temperature (Soldering, 10secs) . . . . . +300°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAUTION**

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Relative Accuracy	Full Scale Error	Package Option <sup>2</sup>
AD7549JN	-40°C to +85°C	± 1LSB	± 6LSB	N-20
AD7549KN	-40°C to +85°C	± 1/2LSB	± 3LSB	N-20
AD7549JP	-40°C to +85°C	± 1LSB	± 6LSB	P-20A
AD7549KP	-40°C to +85°C	± 1/2LSB	± 3LSB	P-20A
AD7549AQ	-40°C to +85°C	± 1LSB	± 6LSB	Q-20
AD7549BQ	-40°C to +85°C	± 1/2LSB	± 3LSB	Q-20
AD7549SQ	-55°C to +125°C	± 1LSB	± 6LSB	Q-20
AD7549TQ	-55°C to +125°C	± 1/2LSB	± 3LSB	Q-20
AD7549SE	-55°C to +125°C	± 1LSB	± 6LSB	E-20A
AD7549TE	-55°C to +125°C	± 1/2LSB	± 3LSB	E-20A

NOTES

<sup>1</sup>To order MIL-STD-883, Class B process parts, add /883B to part number. Contact your local sales office for military data sheet.

<sup>2</sup>E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of 1LSB max over the operating temperature range ensures monotonicity.

FULL-SCALE ERROR

Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero.

OUTPUT CAPACITANCE

This is the capacitance from I<sub>OUTA</sub> or I<sub>OUTB</sub> to AGND.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse.

This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V<sub>REFA</sub> and V<sub>REFB</sub> equal to AGND.

OUTPUT LEAKAGE CURRENT

Output Leakage Current is current which appears at I<sub>OUTA</sub> or I<sub>OUTB</sub> with the DAC registers loaded to all zeros.

MULTIPLYING FEEDTHROUGH ERROR

This is the error due to capacitive feedthrough from V<sub>REFA</sub> to I<sub>OUTA</sub> or V<sub>REFB</sub> to I<sub>OUTB</sub> with the DAC registers loaded to all zeros.

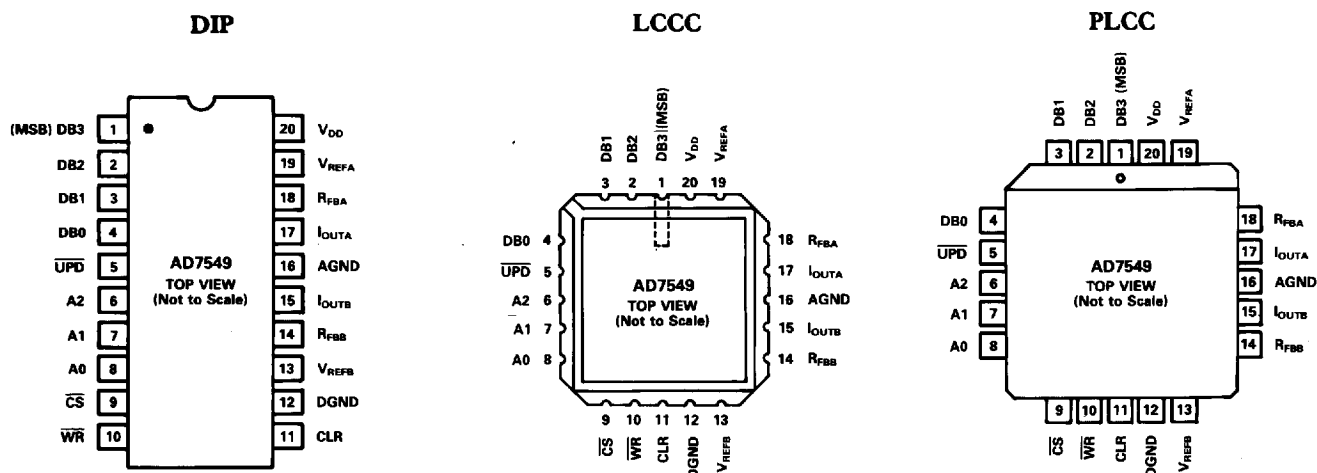
CHANNEL-TO-CHANNEL ISOLATION

Channel-to-Channel Isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

DIGITAL CROSSTALK

The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as Digital Crosstalk and is specified in nV-secs.

PIN CONFIGURATIONS



PIN	FUNCTION	DESCRIPTION
1	DB3	Data Bit 3, Data Bit 7 or Data Bit 11 (MSB)
2	DB2	Data Bit 2, Data Bit 6 or Data Bit 10.
3	DB1	Data Bit 1, Data Bit 5 or Data Bit 9.
4	DB0	Data Bit 0, Data Bit 4 or Data Bit 8.
5	$\overline{\text{UPD}}$	Updates DAC Registers from 4-bit input registers. DAC A and DAC B both updated simultaneously.
6	A2	Address line 2.
7	A1	Address line 1.
8	A0	Address line 0.
9	$\overline{\text{CS}}$	Chip Select Input. Active low.
10	$\overline{\text{WR}}$	Write Input. Active low.
11	CLR	Clear Input. Active High. Clears all registers.
12	DGND	Digital Ground.
13	V <sub>REFB</sub>	Voltage reference input to DAC B.
14	R <sub>FBB</sub>	Feedback resistor of DAC B.
15	I <sub>OUTB</sub>	Current output terminal of DAC B.
16	AGND	Analog ground.
17	I <sub>OUTA</sub>	Current output terminal of DAC A.
18	R <sub>FBA</sub>	Feedback resistor of DAC A.
19	V <sub>REFA</sub>	Voltage reference input to DAC A.
20	V <sub>DD</sub>	+ 15V supply input.

CLR	UPD	$\overline{\text{CS}}$	WR	A2	A1	A0	FUNCTION
0	X	X	1	X	X	X	No data transfer.
0	1	1	X	X	X	X	No data transfer.
1	X	X	X	X	X	X	All registers cleared.
0	1	0	$\overline{\text{L}}$	0	0	0	DAC A LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	$\overline{\text{L}}$	0	0	1	DAC A MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	$\overline{\text{L}}$	0	1	0	DAC A HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	$\overline{\text{L}}$	0	1	1	DAC A Register loaded from Input Registers.
0	1	0	$\overline{\text{L}}$	1	0	0	DAC B LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	$\overline{\text{L}}$	1	0	1	DAC B MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	$\overline{\text{L}}$	1	1	0	DAC B HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	$\overline{\text{L}}$	1	1	1	DAC B Register loaded from Input Registers.
0	0	1	$\overline{\text{L}}$	X	X	X	DAC A, DAC B Registers updated simultaneously from Input Registers.

NOTE: X = Don't Care

Table 1. AD7549 Truth Table

# AD7549

## UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 2 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (i.e. AD644) or separate packages (AD544). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high speed op-amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all 0's and amplifier offset adjusted so that  $V_{OUTA}$  or  $V_{OUTB}$  is at a minimum (i.e.  $\leq 120\mu V$ ). Full scale trimming is accomplished by loading the DAC register with all 1's and adjusting R1 (R3) so that  $V_{OUTA}$  ( $V_{OUTB}$ ) =  $-V_{IN}$  (4095/4096). In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

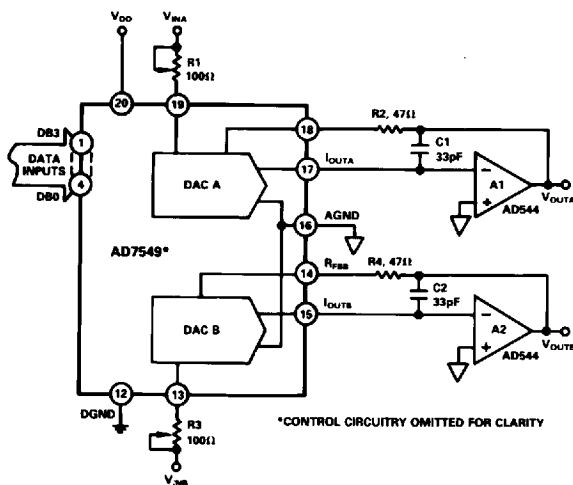


Figure 2. AD7549 Unipolar Binary Operation

## BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that  $V_{OUTA}$  ( $V_{OUTB}$ ) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, R10) varied for  $V_{OUTA}$  ( $V_{OUTB}$ ) = 0V. Full scale trimming can be accomplished by adjusting the amplitude of  $V_{IN}$  or by varying the value of R5 (R8).

Resistors R5, R6, R7 (R8, R9, R10) must be ratio matched to 0.01%. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 3 is given in Table III.

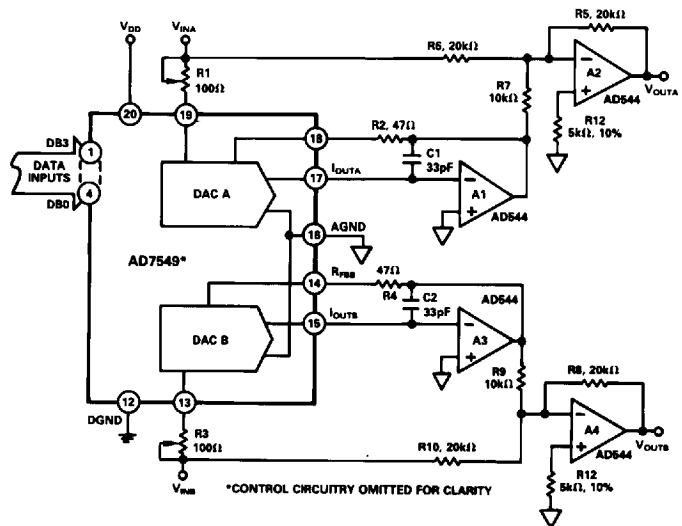


Figure 3. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register		Analog Output, $V_{OUTA}$ or $V_{OUTB}$
MSB	LSB	
1111	1111 1111	$-V_{IN} \left( \frac{4095}{4096} \right)$
1000	0000 0000	$-V_{IN} \left( \frac{2048}{4096} \right) = -1/2 V_{IN}$
0000	0000 0001	$-V_{IN} \left( \frac{1}{4096} \right)$
0000	0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 2

Binary Number in DAC Register		Analog Output, $V_{OUTA}$ or $V_{OUTB}$
MSB	LSB	
1111	1111 1111	$+V_{IN} \left( \frac{2047}{2048} \right)$
1000	0000 0001	$+V_{IN} \left( \frac{1}{2048} \right)$
1000	0000 0000	0V
0111	1111 1111	$-V_{IN} \left( \frac{1}{2048} \right)$
0000	0000 0000	$-V_{IN} \left( \frac{2048}{2048} \right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 3

## APPLICATION HINTS

**Output Offset:** CMOS D/A converters in circuits such as Figures 2 and 3 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, depends on  $V_{OS}$  where  $V_{OS}$  is the amplifier input offset voltage. To maintain monotonic operation, it is recommended that  $V_{OS}$  be no greater than  $(25 \times 10^{-6})(V_{REF})$  over the temperature range of operation. Suitable op amps are AD644L, AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset ( $50\mu V$ ) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

**Temperature Coefficients:** The gain temperature coefficient of the AD7549 has a maximum value of  $5\text{ppm}/^\circ\text{C}$  and typical value of  $1\text{ppm}/^\circ\text{C}$ . This corresponds to worst case gain shifts of 2LSBs and 0.4LSBs respectively over a  $100^\circ\text{C}$  temperature range. When trim resistors R1(R3) and R2(R4) are used to adjust full scale range, the temperature coefficient of R1(R3) and R2(R4) should also be taken into account.

**High Frequency Considerations:** AD7549 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

**Feedthrough:** The dynamic performance of the AD7549 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 2 is shown in Figure 4 which minimizes feedthrough from  $V_{REFA}$ ,  $V_{REFB}$  to the output in multiplying applications.

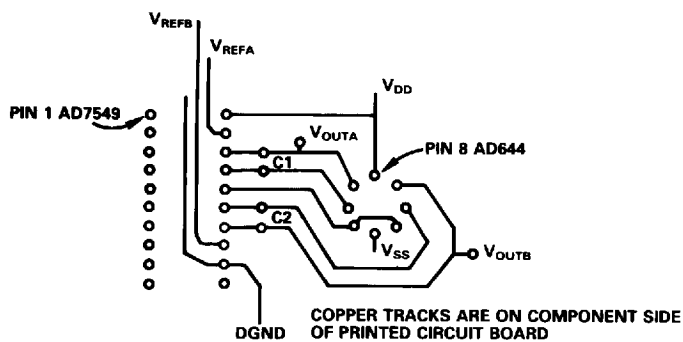


Figure 4. Suggested Layout for AD7549 with AD644 (Dual Op Amp)

## AD7549 – 8085A INTERFACE

A typical interface circuit for the AD7549 and the 8085A microprocessor is given in Figure 5. Only the bottom 4 bits of the microprocessor data bus are used. The address decoder provides both the  $\overline{CS}$  and  $\overline{UPD}$  signals for the DAC. Address lines A0, A1, A2 select one of six DAC Input Registers for accepting data. In applications where simultaneous loading of the DACs is required then the  $\overline{UPD}$  pin must be used to strobe both DAC registers. Otherwise,  $\overline{UPD}$  may be tied high and address lines A0-A2, in conjunction with  $\overline{CS}$  and  $\overline{WR}$  signals, will select each DAC register separately (see Pin Function Description).

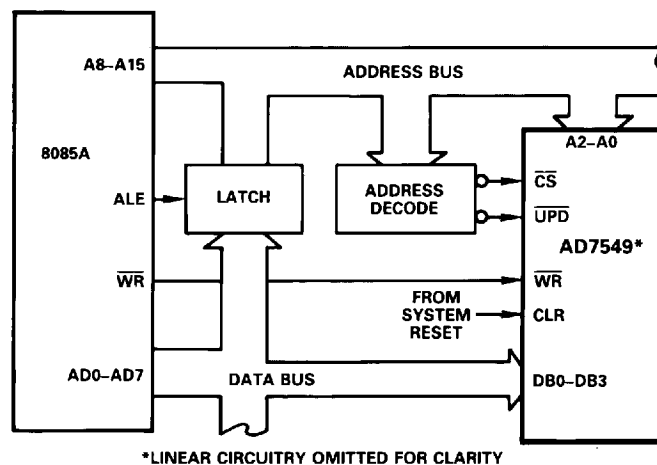


Figure 5. AD7549-8085A Interface

## AD7549 – Z80 INTERFACE

Figure 6 shows the AD7549 connected to the Z80 microprocessor. The interface structure is similar to that for the 8085A.

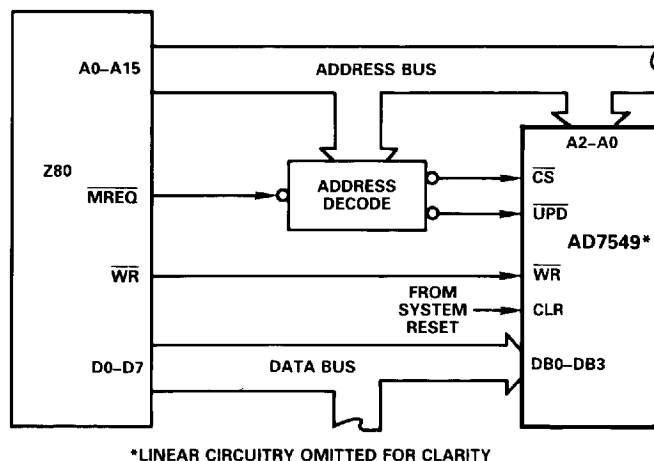
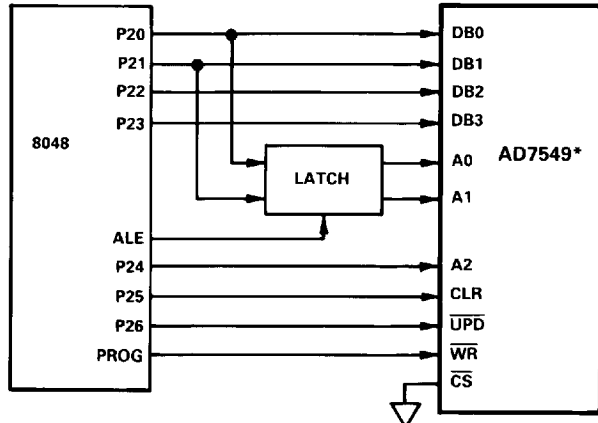


Figure 6. AD7549-Z80 Interface

# AD7549

## AD7549 - 8048 INTERFACE

The AD7549 can be interfaced to the 8048 single component microcomputer using the circuit of Figure 7. A minimum number of I/O lines are needed. The system is easily expanded by using extra port lines to provide Chip Selects for more AD7549's. The advantage of this interface lies in its simplicity. In either single or multiple DAC applications both the software and chip select decoding are simplified over what would be required if the devices were memory mapped in a conventional manner.



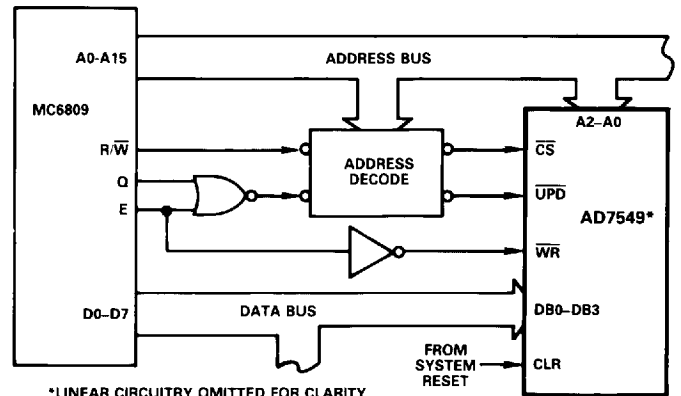
\*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 7. AD7549-8048 Interface

The combination of 8048 system and AD7549 is particularly suitable for dedicated control applications. By adding reference and output circuitry a complete control system can be configured with a minimum number of components.

## AD7549 - MC6809 INTERFACE

Figure 8 is the interface circuit for the popular MC6809 8-bit microprocessor. CS and UPD signals are decoded from the address for the simultaneous update facility while the WR pulse is provided by inverting the microprocessor clock, E.



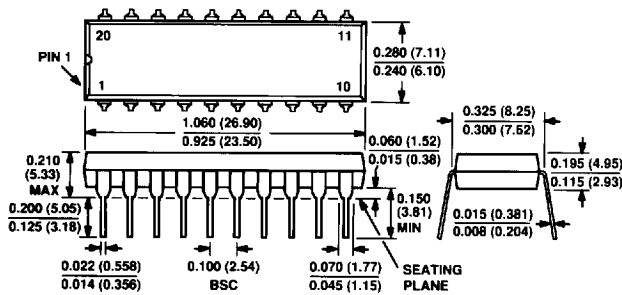
\*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 8. AD7549-MC6809 Interface

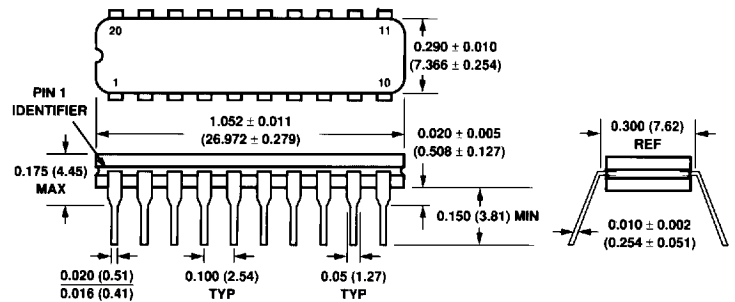
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

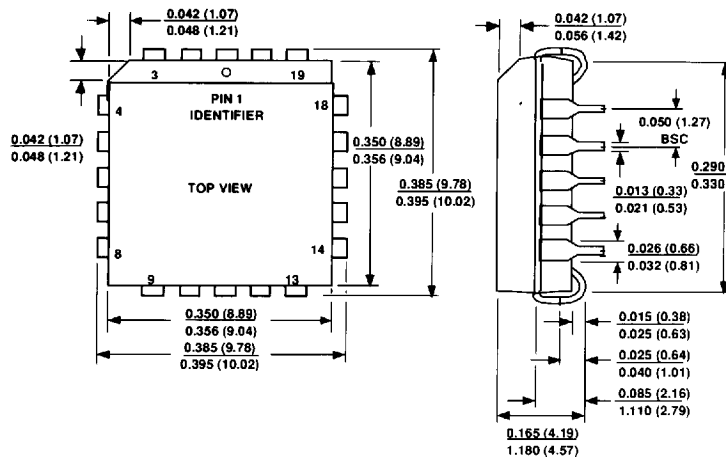
### 20-Pin Plastic DIP (N-20)



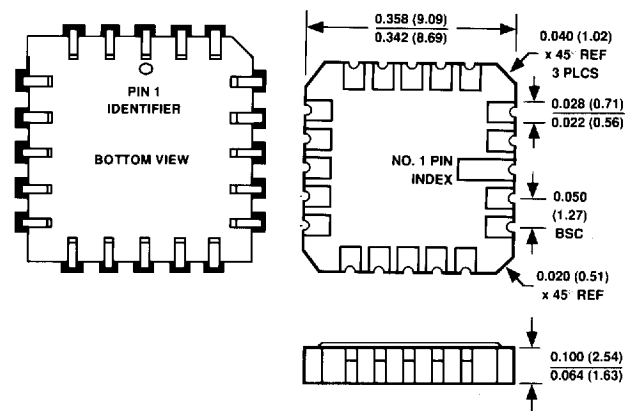
### 20-Pin Cerdip (Q-20)



### 20-Terminal Plastic Leaded Chip Carrier (P-20A)



### E-20 LCCC E Package





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