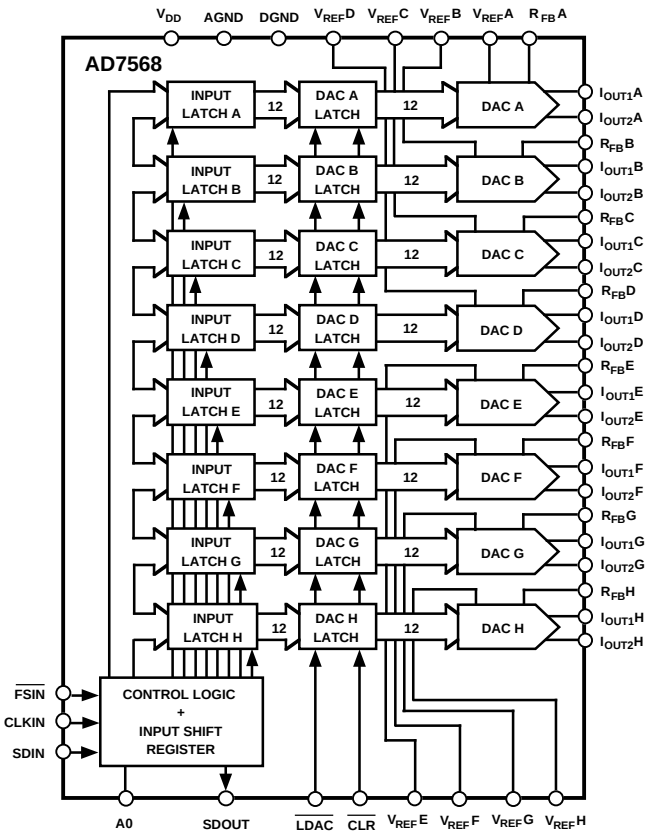
LC²MOS Octal 12-Bit DAC

AD7568

FEATURES
Eight 12-Bit DACs in One Package
4-Quadrant Multiplication
Separate References
Single +5 V Supply
Low Power: 1 mW
Versatile Serial Interface
Simultaneous Update Capability
Reset Function
44-Pin PQFP and PLCC

APPLICATIONS
Process Control
Automatic Test Equipment
General Purpose Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7568 contains eight 12-bit DACs in one monolithic device. The DACs are standard current output with separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} terminals.

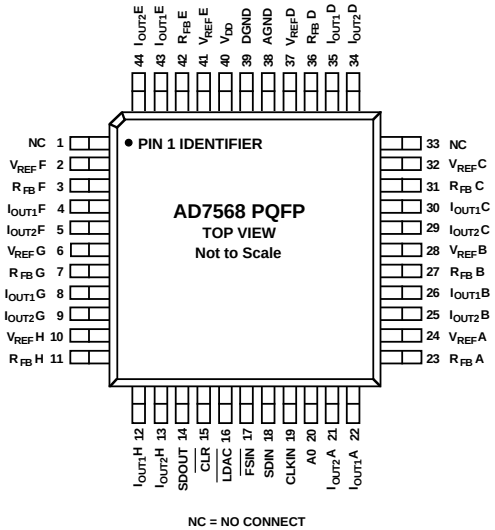
The AD7568 is a serial input device. Data is loaded using $\overline{FSIN}$, CLKIN and SDIN. One address pin, A0, sets up a device address, and this feature may be used to simplify device loading in a multi-DAC environment.

All DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input and they can be cleared by asserting the asynchronous $\overline{CLR}$ input.

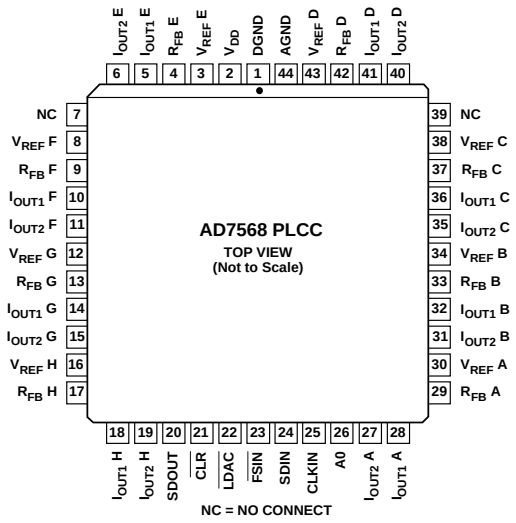
The AD7568 is housed in a space-saving 44-pin plastic quad flatpack and 44-lead PLCC.

PIN CONFIGURATIONS

Plastic Quad Flatpack



Plastic Leaded Chip Carrier



REV. C

AD7568–SPECIFICATIONS[1] (V_{DD} = +4.75 V to +5.25 V; I_{OUT1} = I_{OUT2} = 0 V; V_{REF} = +5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	AD7568B[2]	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 1.22 mV when V_{REF} = 5 V
Relative Accuracy	±0.5	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			
I_{OUT1}			
@ +25°C	10	nA max	See Terminology Section
T_{MIN} to T_{MAX}	200	nA max	
REFERENCE INPUT			
Input Resistance	5	kΩ min	Typical Input Resistance = 7 kΩ
	9	kΩ max	
Ladder Resistance Mismatch	2	% max	Typically 0.6%
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	µA max	
C_{IN}, Input Capacitance	10	pF max	
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	
Power Supply Sensitivity			
$\Delta Gain/\Delta V_{DD}$	–75	dB typ	
I_{DD}	300	µA max	V_{INH} = 4.0 V min, V_{INL} = 0.4 V max
	3.5	mA max	V_{INH} = 2.4 V min, V_{INL} = 0.8 V max

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance and are not subject to test. DAC output op amp is AD843.)

Parameter	AD7568B[2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	500	ns typ	To 0.01% of Full-Scale Range. DAC Latch Alternately Loaded with All 0s and All 1s.
Digital to Analog Glitch Impulse	40	nV–s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s.
Multiplying Feedthrough Error	–66	dB max	V_{REF} = 20 V pk-pk, 10 kHz Sine Wave. DAC Latch Loaded with All 0s.
Output Capacitance	60	pF max	All 1s Loaded to DAC.
	30	pF max	All 0s Loaded to DAC.
Channel-to-Channel Isolation	–76	dB typ	Feedthrough from Any One Reference to the Others with 20 V pk-pk, 10 kHz Sine Wave Applied.
Digital Crosstalk	40	nV–s typ	Effect of all 0s to all 1s Code Transition on Nonselected DACs.
Digital Feedthrough	40	nV–s typ	Feedthrough to Any DAC Output with $\overline{FSIN}$ High and Square Wave Applied to SDIN and SCLK.
Total Harmonic Distortion	–83	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave.
Output Noise Spectral Density			
@ 1 kHz	20	nV/$\sqrt{Hz}$	All 1s Loaded to the DAC. V_{REF} = 0 V. Output Op Amp is AD OP07.

NOTES
[1]Temperature range as follows: B Version: –40°C to +85°C.
[2]All specifications also apply for V_{REF} = +10 V, except relative accuracy which degrades to ±1 LSB.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{DD} = +5 V ± 5%; I_{OUT1} = I_{OUT2} = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_A = +25°C	Limit at T_A = –40°C to +85°C	Units	Description
t_1	100	100	ns min	CLKIN Cycle Time
t_2	40	40	ns min	CLKIN High Time
t_3	40	40	ns min	CLKIN Low Time
t_4	30	30	ns min	$\overline{\text{FSIN}}$ Setup Time
t_5	30	30	ns min	Data Setup Time
t_6	5	5	ns min	Data Hold Time
t_7	90	90	ns min	$\overline{\text{FSIN}}$ Hold Time
t_8[2]	70	70	ns max	SDOUT Valid After CLKIN Falling Edge
t_9	40	40	ns min	$\overline{\text{LDAC}}$, $\overline{\text{CLR}}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_8 is measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V.

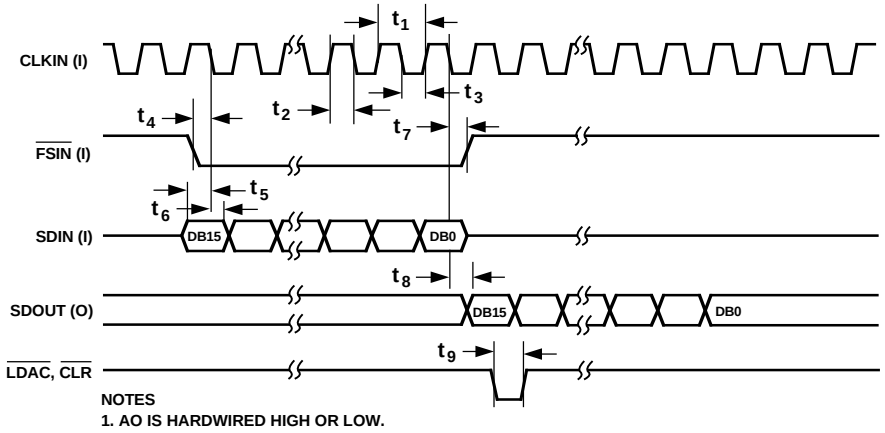


Figure 1. Timing Diagram

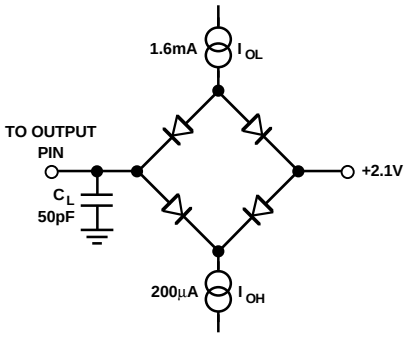


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Parameter	Rating
V_{DD} to DGND	−0.3 V to +6 V
I_{OUT1} to DGND	−0.3 V to V_{DD} +0.3 V
I_{OUT2} to DGND	−0.3 V to V_{DD} +0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} +0.3 V
V_{RFB}, V_{REF} to DGND	±15 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial Plastic (B Versions)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Power Dissipation (Any Package) to 75°C	250 mW
Derates above 75°C by	10 mW/°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[1] Transient currents of up to 100 mA will not cause SCR latch-up.

PIN DESCRIPTION

Mnemonic	Description
V_{DD}	Positive Power Supply. This is 5 V ± 5%.
DGND	Digital Ground.
AGND	Analog Ground
V_{REFA} to V_{REFH}	DAC Reference Inputs.
R_{FBA} to R_{FBH}	DAC Feedback Resistor Pins.
I_{OUTA} to I_{OUTH}	DAC Current Output Terminals.
AGND	This pin connects to the back gates of the current steering switches. It should be connected to the signal ground of the system.
CLKIN	Clock Input. Data is clocked into the input shift register on the falling edges of CLKIN. Add a pull-down resistor on the clock line to avoid timing issues.
$\overline{\text{FSIN}}$	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{\text{FSIN}}$ goes low, it enables the input shift register, and data is transferred on the falling edges of CLKIN. If the address bit is valid, the 12-bit DAC data is transferred to the appropriate input latch on the sixteenth falling edge after $\overline{\text{FSIN}}$ goes low.
SDIN	Serial Data Input. The device accepts a 16-bit word. The first bit (DB15) is the DAC MSB, with the remaining bits following. Next comes the device address bit, A0. If this does not correspond to the logic level on Pin A0, the data is ignored. Finally comes the three DAC select bits. These determine which DAC in the device is selected for loading.
SDOUT	This shift register output allows multiple devices to be connected in a daisy-chain configuration.
A0	Device Address Pin. This input gives the device an address. If DB3 of the serial input stream does not correspond to this, the data that follows is ignored and not loaded to any input latch. However, it will appear at SDOUT irrespective of this.
$\overline{\text{LDAC}}$	Asynchronous $\overline{\text{LDAC}}$ Input. When this input is taken low, all DAC latches are simultaneously updated with the contents of the input latches.
$\overline{\text{CLR}}$	Asynchronous $\overline{\text{CLR}}$ Input. When this input is taken low, all DAC latch outputs go to zero.

TERMINOLOGY

Relative Accuracy
Relative Accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage or full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Gain Error
Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

Output Leakage Current
Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s. This is a combination of the switch leakage current and the ladder termination resistor current. The I_{OUT2} leakage current is typically equal to that in I_{OUT1}.

Output Capacitance
This is the capacitance from the I_{OUT1} pin to AGND.

Output Voltage Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For the AD7568, it is specified with the AD843 as the output op amp.

Digital to Analog Glitch Impulse
This is the amount of charge injected into the analog output when the inputs change state. It is normally specified as the area of the glitch in either pA-secs or nV-secs, depending upon whether the glitch is measured as a current or voltage signal. It is measured with the reference input connected to AGND and the digital inputs toggled between all 1s and all 0s.

AC Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT} terminal, when all 0s are loaded in the DAC.

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of any other DAC in the device and is expressed in dBs.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the Digital Crosstalk and is specified in nV-secs.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the I_{OUT} pin and subsequently on the op amp output. This noise is digital feedthrough.

Table I. AD7568 Loading Sequence

DB15															DB0
DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	A0	DS2	DS1	DS0

Table II. DAC Selection

DS2	DS1	DS0	Function
0	0	0	DAC A Selected
0	0	1	DAC B Selected
0	1	0	DAC C Selected
0	1	1	DAC D Selected
1	0	0	DAC E Sclected
1	0	1	DAC F Selected
1	1	0	DAC G Sclected
1	1	1	DAC H Selected

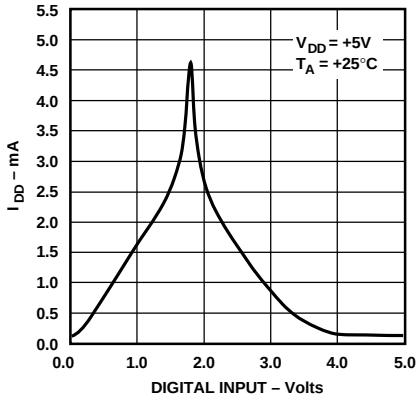


Figure 3. Supply Current vs. Logic Input Voltage

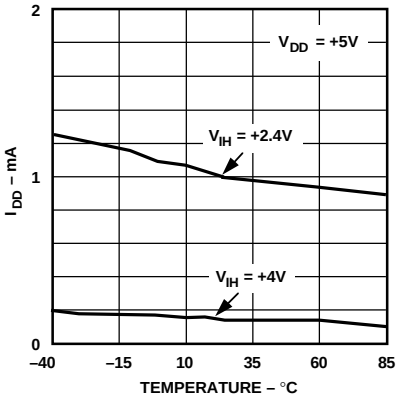


Figure 4. Supply Current vs. Temperature

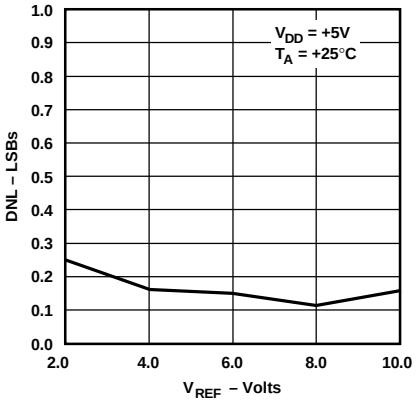


Figure 5. Differential Nonlinearity Error vs. V_{REF}

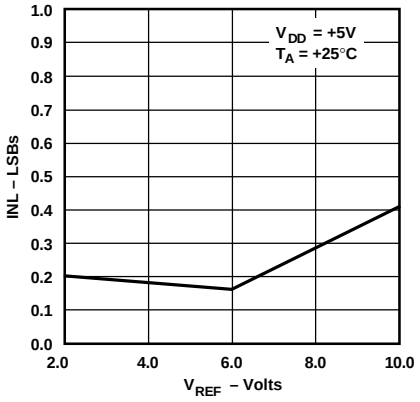


Figure 6. Integral Nonlinearity Error vs. V_{REF}

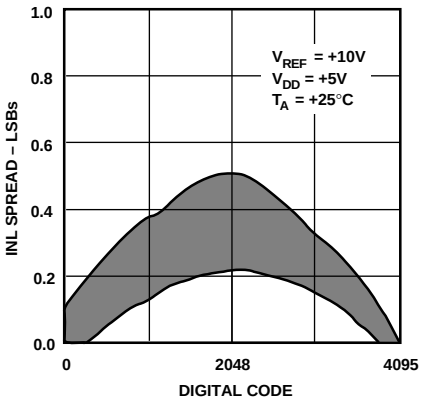


Figure 7. Typical DAC to DAC Linearity Matching

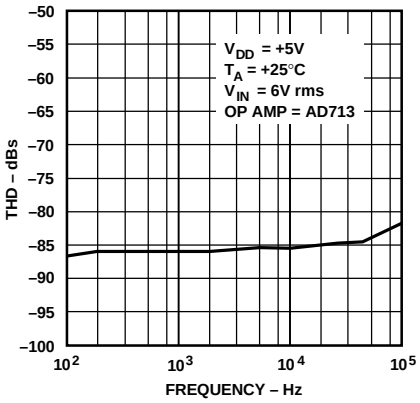


Figure 8. Total Harmonic Distortion vs. Frequency

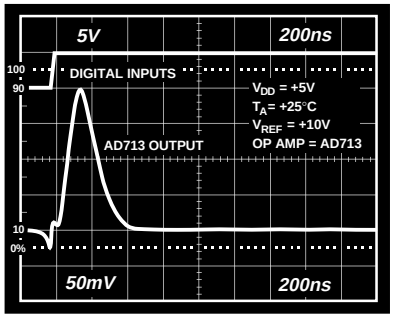


Figure 9. Digital-to-Analog Glitch Impulse

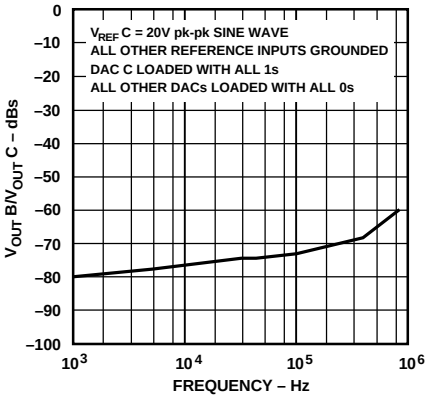


Figure 10. Channel-to-Channel Isolation (1 DAC to 1 DAC)

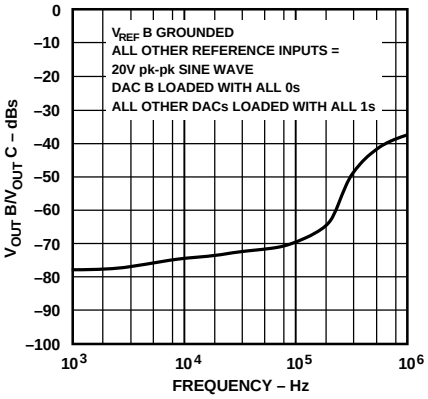


Figure 11. Channel-to-Channel Isolation (1 DAC to All Other DACs)

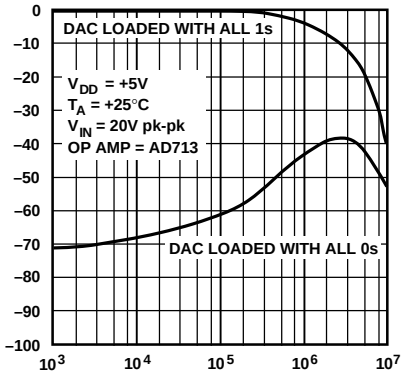


Figure 12. Multiplying Frequency Response vs. Digital Code

GENERAL DESCRIPTION

D/A Section

The AD7568 contains eight 12-bit current-output D/A converters. A simplified circuit diagram for one of the D/A converters is shown in Figure 13.

A segmented scheme is used whereby the 2 MSBs of the 12-bit data word are decoded to drive the three switches A, B and C. The remaining 10 bits of the data word drive the switches S0 to S9 in a standard R–2R ladder configuration.

Each of the switches A to C steers 1/4 of the total reference current with the remaining current passing through the R–2R section.

Each DAC in the device has separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} pins. This makes the device extremely versatile and allows DACs in the same device to be configured differently.

When an output amplifier is connected in the standard configuration of Figure 15, the output voltage is given by:

$$V_{OUT} = -D \cdot V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC. Thus, in the AD7568, D can be set from 0 to 4095/4096.

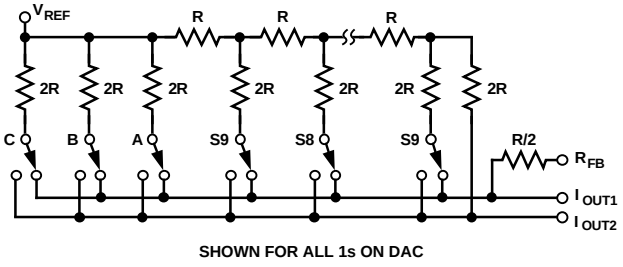


Figure 13. Simplified D/A Circuit Diagram

Interface Section

The AD7568 is a serial input device. Three lines control the serial interface, $\overline{FSIN}$, CLKIN and SDIN. The timing diagram is shown in Figure 1.

When the $\overline{FSIN}$ input goes low, data appearing on the SDIN line is clocked into the input shift register on each falling edge of CLKIN. When sixteen bits have been received, the register loading is automatically disabled until the next falling edge of $\overline{FSIN}$ detected. Also, the received data is clocked out on the next rising edge of CLKIN and appears on the SDOUT pin. This feature allows several devices to be connected together in a daisy chain fashion.

When the sixteen bits have been received in the input shift register, DB3 (A0) is checked to see if it corresponds to the state of pin A0. If it does, then the word is accepted. Otherwise, it is disregarded. This allows the user to address one of two AD7568s in a very simple fashion. DB0 to DB2 of the 16-bit word determine which of the eight DAC input latches is to be loaded. When the $\overline{LDAC}$ line goes low, all eight DAC latches in the device are simultaneously loaded with the contents of their respective input latches, and the outputs change accordingly.

Bringing the $\overline{CLR}$ line low resets the DAC latches to all 0s. The input latches are not affected, so that the user can revert to the previous analog output if desired.

Figure 14. Input Logic

UNIPOLAR BINARY OPERATION
(2-Quadrant Multiplication)

Figure 15 shows the standard unipolar binary connection diagram for one of the DACs in the AD7568. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. Resistors R1 and R2 allow the user to adjust the DAC gain error. Offset can be removed by adjusting the output amplifier offset voltage.

A1 should be chosen to suit the application. For example, the AD OP07 or OP177 are ideal for very low bandwidth applications while the AD843 and AD845 offer very fast settling time in wide bandwidth applications. Appropriate multiple versions of these amplifiers can be used with the AD7568 to reduce board space requirements.

The code table for Figure 15 is shown in Table III.

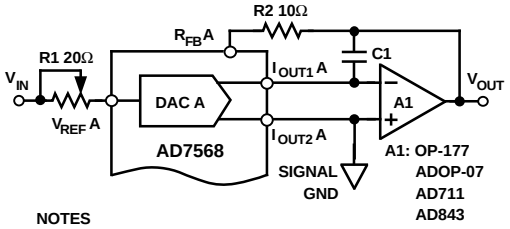


Figure 15. Unipolar Binary Operation

Table III. Unipolar Binary Code Table

Digital Input MSB.....LSB	Analog Output (V_{OUT} As Shown in Figure 15)
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0001	$-V_{REF}$ (2049/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0111 1111 1111	$-V_{REF}$ (2047/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	$-V_{REF}$ (0/4096) = 0

NOTE
Nominal LSB size for the circuit of Figure 15 is given by: V_{REF} (1/4096).

BIPOLAR OPERATION
(4-Quadrant Multiplication)

Figure 16 shows the standard connection diagram for bipolar operation of any one of the DACs in the AD7568. The coding is offset binary as shown in Table IV. When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. To maintain the gain error specifications, resistors R3, R4 and R5 should be ratio matched to 0.01%.

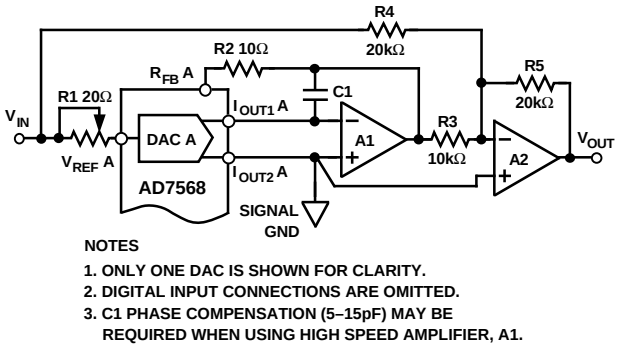


Figure 16. Bipolar Operation (4-Quadrant Multiplication)

Table IV. Bipolar (Offset Binary) Code Table

Digital Input MSB . . . . . LSB	Analog Output (V_{OUT} As Shown in Figure 16)
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	$+V_{REF}$ (0/2048) = 0
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0001	$-V_{REF}$ (2047/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

NOTE
Nominal LSB size for the circuit of Figure 16 is given by: V_{REF} (1/2048).

SINGLE SUPPLY CIRCUITS

The AD7568 operates from a single +5 V supply, and this makes it ideal for single supply systems. When operating in such a system, it is not possible to use the standard circuits of Figures 15 and 16 since these invert the analog input, V_{IN}. There are two alternatives. One of these continues to operate the DAC as a current-mode device, while the other uses the voltage switching mode.

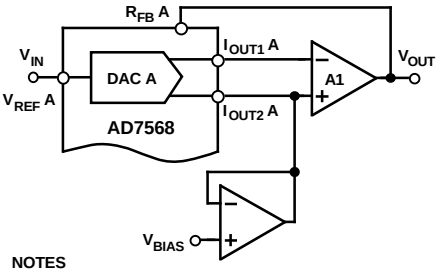


Figure 17. Single Supply Current-Mode Operation

Current Mode Circuit

In the current mode circuit of Figure 17, I_{OUT2}, and hence I_{OUT1}, is biased positive by an amount V_{BIAS}. For the circuit to operate correctly, the DAC ladder termination resistor must be connected internally to I_{OUT2}. This is the case with the AD7568. The output voltage is given by:

$$V_{OUT} = \left\{ D \frac{R_{FB}}{R_{DAC}} \left(V_{BIAS} - V_{IN} \right) \right\} + V_{BIAS}$$

As D varies from 0 to 4095/4096, the output voltage varies from $V_{OUT} = V_{BIAS}$ to $V_{OUT} = 2\ V_{BIAS} - V_{IN}$. V_{BIAS} should be a low impedance source capable of sinking and sourcing all possible variations in current at the I_{OUT2} terminal without any problems.

Voltage Mode Circuit

Figure 18 shows DAC A of the AD7568 operating in the voltage-switching mode. The reference voltage, V_{IN} is applied to the I_{OUT1} pin, I_{OUT2} is connected to AGND and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage making single supply operation possible. The output from the DAC is a voltage at a constant impedance (the DAC ladder resistance). Thus, an op amp is necessary to buffer the output voltage. The reference voltage input no longer sees a constant input impedance, but one which varies with code. So, the voltage input should be driven from a low impedance source.

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC no longer have the same source-drain voltage. As a result, their on-resistance differs and this degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 volts or an internal diode will turn on, causing possible damage to the device. This means that the full-range multiplying capability of the DAC is lost.

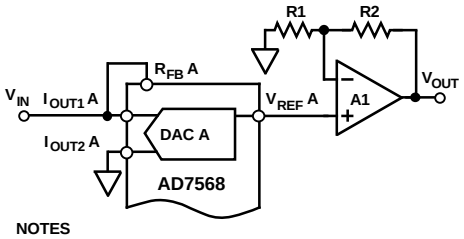


Figure 18. Single Supply Voltage Switching Mode Operation

APPLICATIONS

Programmable State Variable Filter

The AD7568 with its multiplying capability and fast settling time is ideal for many types of signal conditioning applications. The circuit of Figure 19 shows its use in a state variable filter design. This type of filter has three outputs: low pass, high pass and bandpass. The particular version shown in Figure 19 uses one half of an AD7568 to control the critical parameters f_0, Q and A_0. Instead of several fixed resistors, the circuit uses the DAC equivalent resistances as circuit elements. Thus, R1 in Figure 19 is controlled by the 12-bit digital word loaded to DAC A of the AD7568. This is also the case with R2, R3 and R4. The fixed resistor R5 is the feedback resistor, $R_{FB}B$.

DAC Equivalent Resistance, $R_{EQ} = (R_{LADDER} \times 4096)/N$

where:

R_{LADDER} is the DAC ladder resistance.

N is the DAC Digital Code in Decimal ($0 < N < 4096$).

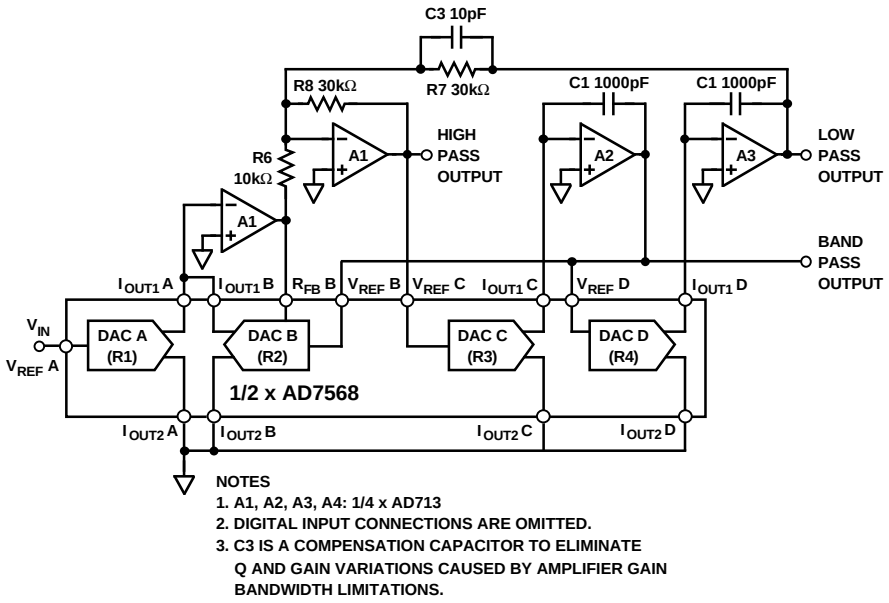


Figure 19. Programmable 2nd Order State Variable Filter

In the circuit of Figure 19:

C1 = C2, R7 = R8, R3 = R4 (i.e., the same code is loaded to each DAC).

Resonant frequency, $f_0 = 1/(2\pi R3C1)$.

Quality Factor, Q = (R6/R8)•(R2/R5).

Bandpass Gain, A0 = –R2/R1.

Using the values shown in Figure 19, the Q range is 0.3 to 5, and the f_0 range is 0 to 12 kHz.

APPLICATION HINTS

Output Offset

CMOS D/A converters in circuits such as Figures 15, 16 and 17 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. For the AD7568 to maintain specified accuracy with V_{REF} at 10 V, it is recommended that V_{OS} be no greater than 500 μV, or (50×10^{-6})•(V_{REF}), over the temperature range of operation. Suitable amplifiers include the AD OP07, AD OP27, OP177, AD711, AD845 or multiple versions of these.

Temperature Coefficients

The gain temperature coefficient of the AD7568 has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This corresponds to gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full-scale in Figures 15 and 16, their temperature coefficients should be taken into account. For further information see "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs," Application Note, Publication Number E630c–5–3/86, available from Analog Devices.

High Frequency Considerations

The output capacitances of the AD7568 DACs work in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor. This is shown as C1 in Figures 15, 16 and 17.

MICROPROCESSOR INTERFACING

AD7568–80C51 Interface

A serial interface between the AD7568 and the 80C51 microcontroller is shown in Figure 20. TXD of the 80C51 drives SCLK of the AD7568 while RXD drives the serial data line of the part. The $\overline{FSIN}$ signal is derived from the port line P3.3.

The 80C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the data word transmitted to the AD7568 corresponds to the loading sequence shown in Table I. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 80C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7568, P3.3 is left low after the first eight bits are transferred, and a second byte of data is then transferred serially to the AD7568. When the second serial transfer is complete, the P3.3 line is taken high. Note that the 80C51 outputs the serial data byte in a format which has the LSB first. The AD7568 expects the MSB first. The 80C51 transmit routine should take this into account.

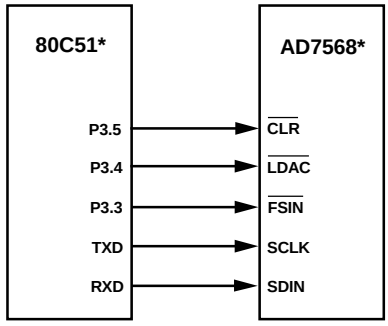


Figure 20. AD7568 to 80C51 Interface

$\overline{LDAC}$ and $\overline{CLR}$ on the AD7568 are also controlled by 80C51 port outputs. The user can bring $\overline{LDAC}$ low after every two bytes have been transmitted to update the DAC which has been programmed. Alternatively, it is possible to wait until all the input registers have been loaded (sixteen byte transmits) and then update the DAC outputs.

AD7568–68HC11 Interface

Figure 21 shows a serial interface between the AD7568 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7568, while the MOSI output drives the serial data line of the AD7568. The $\overline{FSIN}$ signal is derived from a port line (PC7 shown).

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC7 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes (MSB first), with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7568, PC7 is left low after the first eight bits are transferred, and a second byte of data is then transferred serially to the AD7568. When the second serial transfer is complete, the PC7 line is taken high.

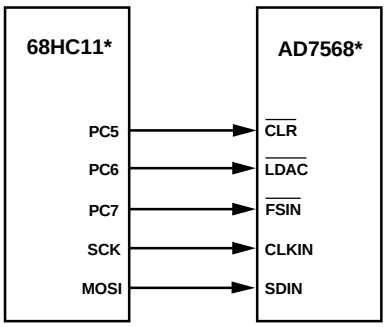


Figure 21. AD7568 to 68HC11 Interface

In Figure 21, $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ are controlled by the PC6 and PC5 port outputs. As with the 80C51, each DAC of the AD7568 can be updated after each two-byte transfer, or else all DACs can be simultaneously updated.

AD7568–ADSP-2101 Interface

Figure 22 shows a serial interface between the AD7568 and the ADSP-2101 digital signal processor. The ADSP-2101 may be set up to operate in the SPORT Transmit Normal Internal Framing Mode. The following ADSP-2101 conditions are recommended: Internal SCLK; Active High Framing Signal; 16-bit word length. Transmission is initiated by writing a word to the TX register after the SPORT has been enabled. The data is then clocked out on every rising edge of SCLK after TFS goes low. TFS stays low until the next data transfer.

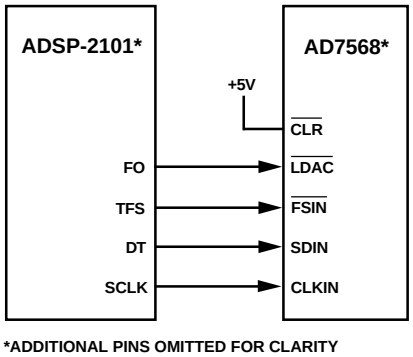


Figure 22. AD7568 to ADSP-2101 Interface

AD7568–TMS320C25 Interface

Figure 23 shows an interface circuit for the TMS320C25 digital signal processor. The data on the DX pin is clocked out of the processor's Transmit Shift Register by the CLKX signal. Sixteen-bit transmit format should be chosen by setting the FO bit in the ST1 register to 0. The transmit operation begins when data is written into the data transmit register of the TMS320C25. This data will be transmitted when the FSX line goes low while CLKX is high or going high. The data, starting with the MSB, is then shifted out to the DX pin on the rising edge of CLKX. When all bits have been transmitted, the user can update the DAC outputs by bringing the XF output flag low.

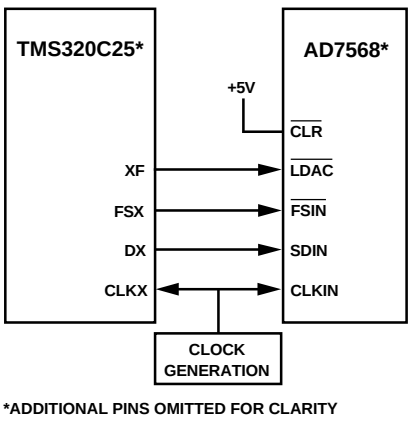


Figure 23. AD7568 to TMS320C25 Interface

Multiple DAC Systems

If there are only two AD7568s in a system, there is a simple way of programming each. This is shown in Figure 24. If the user wishes to program one of the DACs in the first AD7568, then DB3 of the serial bit stream should be set to 0, to correspond to the state of the A0 pin on that device. If the user wishes to program a DAC in the second AD7568, then DB3 should be set to 1, to correspond to A0 on that device.

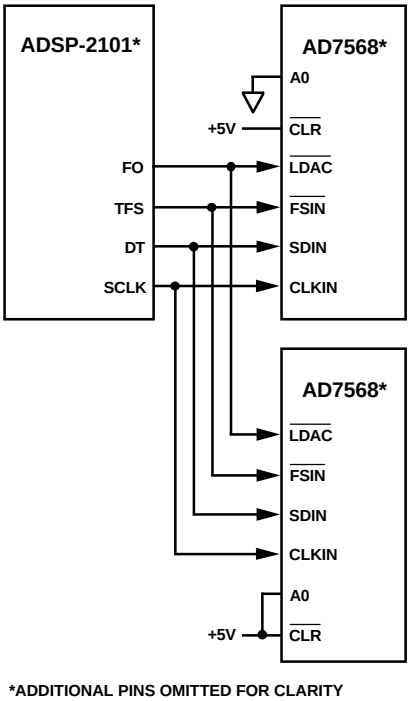


Figure 24. Interfacing ADSP-2101 to Two AD7568s

For systems which contain larger numbers of AD7568s and where the user also wishes to read back the DAC contents for diagnostic purposes, the SDOUT pin may be used to daisy chain several devices together and provide the necessary serial readback. An example with the 68HC11 is shown in Figure 25. The routine below shows how four AD7568s would be programmed in such a system. Data is transmitted at the MOSI pin of the 68HC11. It flows through the input shift registers of the AD7568s and finally appears at the SDOUT pin of DAC N. So, the readback routine can be invoked any time after the first four words have been transmitted (the four input shift registers in the chain will now be filled up and further activity on the CLKIN pin will result in data being read back to the microcomputer through the MISO pin). System connectivity can be verified in this manner. For a four-device system (32 DACs) a two-line to four-line decoder is necessary.

Note that to program the 32 DACs, 35 transmit operations are needed. In the routine, three words must be retransmitted. The first word for DACs #3, #2 and #1 must be transmitted twice in order to synchronize their arrival at the SDIN pin with A0 going low.

Table V. Routine for Loading 4 AD7568s Connected As in Figure 25

Bring PC7 ($\overline{\text{FSIN}}$) low to allow writing to the AD7568s.
  Enable AD7568 #4 (Bring A0 low). Disable the others.
    Transmit 1st 16-bit word: Data for DAC H, #4
    . . . .
    . . . .
    Transmit 9th 16-bit word: Data for DAC H, #3
    Transmit 9th 16-bit word again: Data for DAC H, #3
    Transmit 10th 16-bit word: Data for DAC G, #3
    Transmit 11th 16-bit word: Data for DAC F, #3
  Enable AD7568 #3, Disable the others.
    Transmit 12th 16-bit word: Data for DAC E, #3
    . . . .
    . . . .
    Transmit 17th 16-bit word: Data for DAC H, #2
    Transmit 17th 16-bit word again: Data for DAC H, #2
    Transmit 18th 16-bit word: Data for DAC G, #2
  Enable AD7568 #2, Disable the others.
    Transmit 19th 16-bit word: Data for DAC F, #2
    . . . .
    . . . .
    Transmit 25th word: Data for DAC H, #1
  Enable AD7568 #1, Disable the others.
    Transmit 25th word again: Data for DAC H, #1
    Transmit 26th word: Data for DAC G, #1
    . . . .
    . . . .
    Transmit 32nd word: Data for DAC A, #1
Bring PC7 ($\overline{\text{FSIN}}$) high to disable writing to the AD7568s.

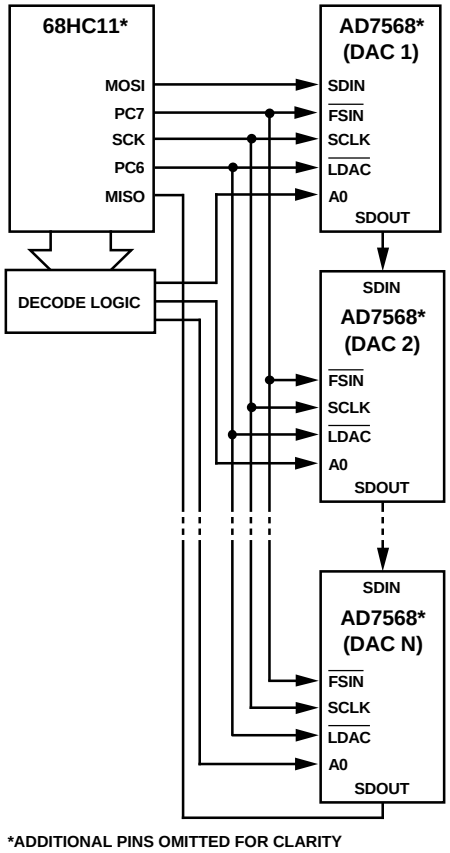
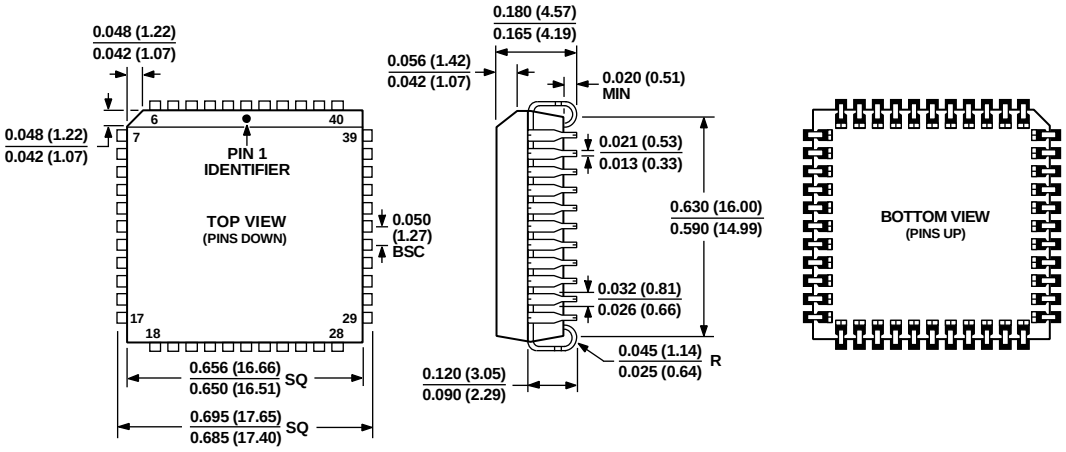


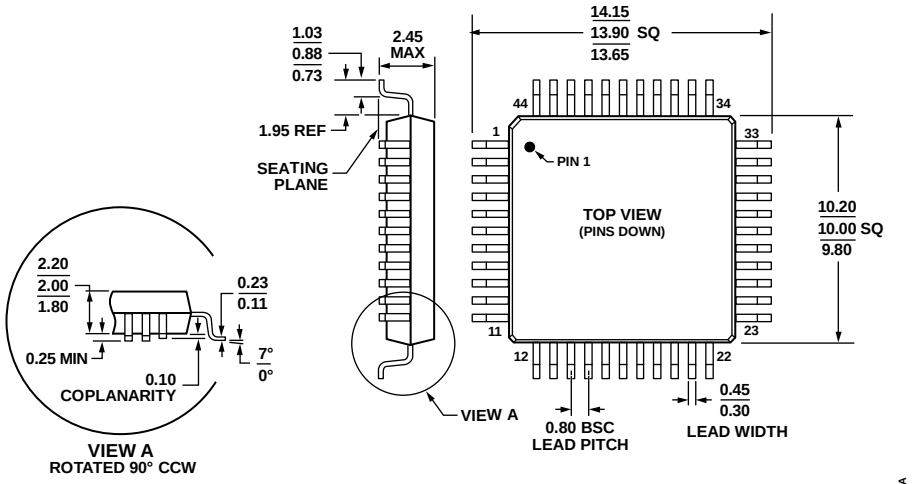
Figure 25. Multi-DAC System

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-047-AC
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 44-Lead Plastic Leaded Chip Carrier [PLCC]
(P-44)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-112-AA-1

Figure 27. 44-Lead Metric Quad Flat Package [MQFP]
(S-44-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error (LSBs)	Package Description	Package Option
AD7568BP	−40°C to +85°C	±0.5	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44
AD7568BP-REEL	−40°C to +85°C	±0.5	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44
AD7568BPZ	−40°C to +85°C	±0.5	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44
AD7568BPZ-REEL	−40°C to +85°C	±0.5	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44
AD7568BSZ	−40°C to +85°C	±0.5	44-Lead Metric Quad Flat Package [MQFP]	S-44-2
AD7568BSZ-REEL	−40°C to +85°C	±0.5	44-Lead Metric Quad Flat Package [MQFP]	S-44-2

[1] Z = RoHS Compliant Part

REVISION HISTORY

2/12—Rev. B to Rev. C

D10541-0-2/12(C)

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