

FEATURES

Throughput:

- 1 MSPS (Warp mode)
- 800 kSPS (Normal mode)
- 666 kSPS (Impulse mode)

16-bit resolution

Analog input voltage range: 0 V to 2.5 V

No pipeline delay

Parallel and serial 5 V/3 V interface

SPI®/QSPI™/MICROWIRE™/DSP compatible

Single 5 V supply operation

Power dissipation

- 92 mW typ @ 666 kSPS, 138 μW @ 1 kSPS without REF
- 128 mW typ @ 1 MSPS with REF

48-lead LQFP and 48-lead LFCSP packages

Pin-to-pin compatible with PuSAR ADCs

APPLICATIONS

Data acquisition

Instrumentation

Digital signal processing

Spectrum analysis

Medical instruments

Battery-powered systems

Process control

GENERAL DESCRIPTION

The **AD7653** is a 16-bit, 1 MSPS, charge redistribution SAR analog-to-digital converter that operates from a single 5 V power supply. The part contains a high speed 16-bit sampling ADC, internal conversion clock, internal reference, error correction circuits, and both serial and parallel system interface ports. It features a very high sampling rate mode (Warp), a fast mode (Normal) for asynchronous conversion rate applications, and a reduced power mode (Impulse) for low power applications where power is scaled with the throughput. The **AD7653** is fabricated using Analog Devices' high performance, 0.6 micron CMOS process, with correspondingly low cost. It is available in a 48-lead LQFP and a tiny 48-lead LFCSP with operation specified from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

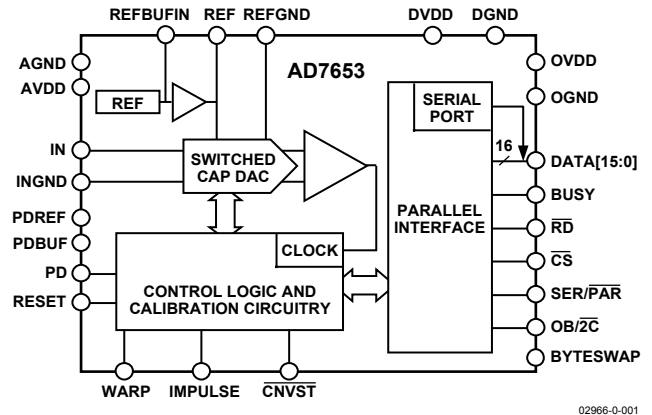


Figure 1.

Table 1. PuSAR™ Selection

Type/kSPS	100–250	500–570	800–1000
Pseudo-Differential	AD7651 AD7660/AD7661	AD7650/AD7652 AD7664/AD7666	AD7653 AD7667
True Bipolar	AD7663	AD7666	AD7671
True Differential	AD7675	AD7676	AD7677
18-Bit	AD7678	AD7679	AD7674
Multichannel/ Simultaneous		AD7654 AD7655	

PRODUCT HIGHLIGHTS

1. Fast Throughput.
The **AD7653** is a 1 MSPS, charge redistribution, 16-bit SAR ADC with internal error correction circuitry.
2. Internal Reference.
The **AD7653** has an internal reference with a typical temperature drift of 7 ppm/°C.
3. Single-Supply Operation.
The **AD7653** operates from a single 5 V supply. In Impulse mode, its power dissipation decreases with the throughput.
4. Serial or Parallel Interface.
Versatile parallel or 2-wire serial interface arrangement is compatible with both 3 V and 5 V logic.

Rev. C

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REVISION HISTORY

12/2017—Rev. B to Rev. C

Changes to Figure 4	8
Updated Outline Dimensions	26
Changes to Ordering Guide	26

9/2016—Rev. A to Rev. B.

Changes to Figure 4 and Table 6	8
Changes to Microprocessor Interface Section, SPI Interface (ADSP-2191M) Section, and Figure 37	24
Deleted Evaluating the AD7653's Performance Section	25
Updated Outline Dimensions	26
Changes to Ordering Guide	26

9/2003—Rev. 0 to Rev. A.

Change to Product Highlights	1
Changes to Specifications	3
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8/2003—Revision 0: Initial Version

SPECIFICATIONS

Table 2. -40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN} - V_{INGND}$	0		V_{REF}	V
Operating Input Voltage	V_{IN}	-0.1		+3	V
	V_{INGND}	-0.1		+0.5	V
Analog Input CMRR	$f_{IN} = 10$ kHz		65		dB
Input Current	1 MSPS Throughput		12		μ A
Input Impedance ¹					
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			1	μ s
Throughput Rate	In Warp Mode	1		1000	kSPS
Time between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			1.25	μ s
Throughput Rate	In Normal Mode	0		800	kSPS
Complete Cycle	In Impulse Mode			1.5	μ s
Throughput Rate	In Impulse Mode	0		666	kSPS
DC ACCURACY					
Integral Linearity Error		-6		+6	LSB ²
No Missing Codes		15			Bits
Differential Linearity Error		-2		+3	LSB
Transition Noise			0.7		LSB
Unipolar Zero Error, T_{MIN} to T_{MAX} ³				± 25	LSB
Unipolar Zero Error Temperature Drift			± 0.2		ppm/ $^{\circ}$ C
Full-Scale Error, T_{MIN} to T_{MAX} ³	REF = 2.5 V			± 0.12	% of FSR
Full-Scale Error Temperature Drift			± 0.4		ppm/ $^{\circ}$ C
Power Supply Sensitivity	AVDD = 5 V \pm 5%, with REF		± 2		LSB
AC ACCURACY					
Signal-to-Noise	$f_{IN} = 100$ kHz		86		dB ⁴
Spurious Free Dynamic Range	$f_{IN} = 100$ kHz		98		dB
Total Harmonic Distortion	$f_{IN} = 45$ kHz		-98		dB
	$f_{IN} = 100$ kHz		-96		dB
Signal-to-(Noise + Distortion)	$f_{IN} = 100$ kHz		86		dB
	-60 dB Input, $f_{IN} = 100$ kHz		30		dB
-3 dB Input Bandwidth			12		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			250	ns
REFERENCE					
Internal Reference Voltage	V_{REF} @ 25 $^{\circ}$ C	2.48	2.50	2.52	V
Internal Reference Temperature Drift	-40 $^{\circ}$ C to +85 $^{\circ}$ C		± 7		ppm/ $^{\circ}$ C
Line Regulation	AVDD = 5 V \pm 5%		± 24		ppm/V
Turn-On Settling Time	$C_{REF} = 10$ μ F		5		ms
Temperature Pin					
Voltage Output @ 25 $^{\circ}$ C			300		mV
Temperature Sensitivity			1		mV/ $^{\circ}$ C
Output Resistance			4.3		k Ω
External Reference Voltage Range		2.3	2.5	AVDD - 1.85	V
External Reference Current Drain	1 MSPS Throughput		300		μ A

Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS					
Logic Levels					
V_{IL}		-0.3		+0.8	V
V_{IH}		2.0		DVDD + 0.3	V
I_{IL}		-1		+1	μ A
I_{IH}		-1		+1	μ A
DIGITAL OUTPUTS					
Data Format ⁵					
Pipeline Delay ⁶					
V_{OL}	$I_{SINK} = 1.6 \text{ mA}$			0.4	V
V_{OH}	$I_{SOURCE} = -500 \mu\text{A}$	OVDD - 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25 ⁷	V
Operating Current ⁸					
AVDD ⁹	1 MSPS Throughput With Reference and Buffer		18.7		mA
AVDD ¹⁰	Reference and Buffer Alone		3		mA
DVDD ¹¹			6.7		mA
OVDD ¹¹			200		μ A
Power Dissipation without REF					
	666 kSPS Throughput ¹¹		92	115	mW
	1 kSPS Throughput ¹¹		138		μ W
Power Dissipation with REF					
	1 MSPS Throughput ⁸		128	145	mW
TEMPERATURE RANGE¹²					
Specified Performance					
	T_{MIN} to T_{MAX}	-40		+85	$^{\circ}$ C

¹ See Analog Input section.

² LSB means least significant bit. With the 0 V to 2.5 V input range, 1 LSB is 38.15 μ V.

³ See Definitions of Specifications section. These specifications do not include the error contribution from the external reference.

⁴ All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.

⁵ Parallel or serial 16-bit.

⁶ Conversion results are available immediately after completed conversion.

⁷ The max should be the minimum of 5.25 V and DVDD + 0.3 V.

⁸ In Warp mode.

⁹ With REF, PDREF and PDBUF are LOW; without REF, PDREF and PDBUF are HIGH.

¹⁰ With PDREF, PDBUF LOW and PD HIGH.

¹¹ Impulse Mode. Tested in Parallel Reading mode.

¹² Consult factory for extended temperature range.

TIMING SPECIFICATIONS

Table 3. -40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figure 26 and Figure 27					
Convert Pulse Width	t ₁	10			ns
Time between Conversions (Warp Mode/Normal Mode/Impulse Mode) ¹	t ₂	1/1.25/1.5			μs
$\overline{\text{CNVST}}$ LOW to BUSY HIGH Delay	t ₃			35	ns
BUSY HIGH All Modes Except Master Serial Read after Convert (Warp Mode/Normal Mode/Impulse Mode)	t ₄			0.75/1/1.25	μs
Aperture Delay	t ₅		2		ns
End of Conversion to BUSY LOW Delay	t ₆	10			ns
Conversion Time (Warp Mode/Normal Mode/Impulse Mode)	t ₇			0.75/1/1.25	μs
Acquisition Time	t ₈	250			ns
RESET Pulse Width	t ₉	10			ns
Refer to Figure 28, Figure 29, and Figure 30 (Parallel Interface Modes)					
$\overline{\text{CNVST}}$ LOW to DATA Valid Delay (Warp Mode/Normal Mode/Impulse Mode)	t ₁₀			0.75/1/1.25	μs
DATA Valid to BUSY LOW Delay	t ₁₁	12			ns
Bus Access Request to DATA Valid	t ₁₂			45	ns
Bus Relinquish Time	t ₁₃	5		15	ns
Refer to Figure 32 and Figure 33 (Master Serial Interface Modes) ²					
$\overline{\text{CS}}$ LOW to SYNC Valid Delay	t ₁₄			10	ns
$\overline{\text{CS}}$ LOW to Internal SCLK Valid Delay ²	t ₁₅			10	ns
$\overline{\text{CS}}$ LOW to SDOUT Delay	t ₁₆			10	ns
$\overline{\text{CNVST}}$ LOW to SYNC Delay (Warp Mode/Normal Mode/Impulse Mode)	t ₁₇		25/275/525		ns
SYNC Asserted to SCLK First Edge Delay	t ₁₈	3			ns
Internal SCLK Period ³	t ₁₉	25		40	ns
Internal SCLK HIGH ³	t ₂₀	12			ns
Internal SCLK LOW ³	t ₂₁	7			ns
SDOUT Valid Setup Time ³	t ₂₂	4			ns
SDOUT Valid Hold Time ³	t ₂₃	2			ns
SCLK Last Edge to SYNC Delay ³	t ₂₄	3			ns
$\overline{\text{CS}}$ HIGH to SYNC HI-Z	t ₂₅			10	ns
$\overline{\text{CS}}$ HIGH to Internal SCLK HI-Z	t ₂₆			10	ns
$\overline{\text{CS}}$ HIGH to SDOUT HI-Z	t ₂₇			10	ns
BUSY HIGH in Master Serial Read after Convert ³ (Warp Mode/Normal Mode/Impulse Mode)	t ₂₈		See Table 4		
$\overline{\text{CNVST}}$ LOW to SYNC Asserted Delay (Warp Mode/Normal Mode/Impulse Mode)	t ₂₉		0.75/1/1.25		μs
SYNC Deasserted to BUSY LOW Delay	t ₃₀		25		ns
Refer to Figure 34 and Figure 35 (Slave Serial Interface Modes) ²					
External SCLK Setup Time	t ₃₁	5			ns
External SCLK Active Edge to SDOUT Delay	t ₃₂	3		18	ns
SDIN Setup Time	t ₃₃	5			ns
SDIN Hold Time	t ₃₄	5			ns
External SCLK Period	t ₃₅	25			ns
External SCLK HIGH	t ₃₆	10			ns
External SCLK LOW	t ₃₇	10			ns

¹ In Warp mode only, the maximum time between conversions is 1 ms; otherwise, there is no required maximum time.² In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.³ In Serial Master Read during Convert Mode. See Table 4 for Serial Master Read after Convert mode.

Table 4. Serial Clock Timings in Master Read after Convert

DIVSCLK[1] DIVSCLK[0]	Symbol	0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t ₁₈	3	17	17	17	ns
Internal SCLK Period Minimum	t ₁₉	25	50	100	200	ns
Internal SCLK Period Maximum	t ₁₉	40	70	140	280	ns
Internal SCLK HIGH Minimum	t ₂₀	12	22	50	100	ns
Internal SCLK LOW Minimum	t ₂₁	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t ₂₂	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t ₂₃	2	4	30	80	ns
SCLK Last Edge to SYNC Delay Minimum	t ₂₄	3	55	130	290	ns
BUSY HIGH Width Maximum (Warp)	t ₂₈	1.5	2	3	5.25	μs
BUSY HIGH Width Maximum (Normal)	t ₂₈	1.75	2.25	3.25	5.55	μs
BUSY HIGH Width Maximum (Impulse)	t ₂₈	2	2.5	3.5	5.75	μs

ABSOLUTE MAXIMUM RATINGS

Table 5. AD7653 Absolute Maximum Ratings

Parameter	Rating
IN ¹ , TEMP ¹ , REF, REFBUF ¹ , INGND, REF ¹ GND to AGND	AVDD + 0.3 V to AGND – 0.3 V
Ground Voltage Differences AGND, DGND, OGND	±0.3 V
Supply Voltages AVDD, DVDD, OVDD AVDD to DVDD, AVDD to OVDD DVDD to OVDD	–0.3 V to +7 V ±7 V –0.3 V to +7 V
Digital Inputs	–0.3 V to DVDD + 0.3 V
PDREF, PDBUF ²	±20 mA
Internal Power Dissipation ³	700 mW
Internal Power Dissipation ⁴	2.5 W
Junction Temperature	150°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

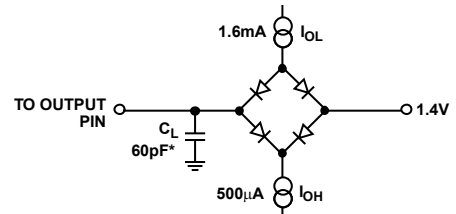
¹ See Analog Input section.

² See Voltage Reference Input section.

³ Specification is for the device in free air:
48-Lead LQFP; $\theta_{JA} = 91^\circ\text{C}/\text{W}$, $\theta_{JC} = 30^\circ\text{C}/\text{W}$

⁴ Specification is for the device in free air:
48-Lead LFCSP; $\theta_{JA} = 26^\circ\text{C}/\text{W}$.

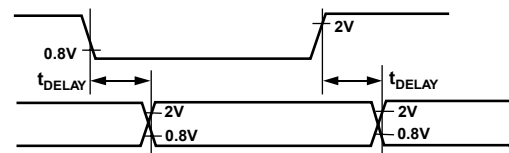
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.



*IN SERIAL INTERFACE MODES, THE SYNC, SCLK, AND SDO_{UT} TIMINGS ARE DEFINED WITH A MAXIMUM LOAD C_L OF 10pF; OTHERWISE, THE LOAD IS 60pF MAXIMUM.

02966-0-006

Figure 2. Load Circuit for Digital Interface Timing, SDO_{UT}, SYNC, SCLK Outputs $C_L = 10$ pF



02966-0-007

Figure 3. Voltage Reference Levels for Timing

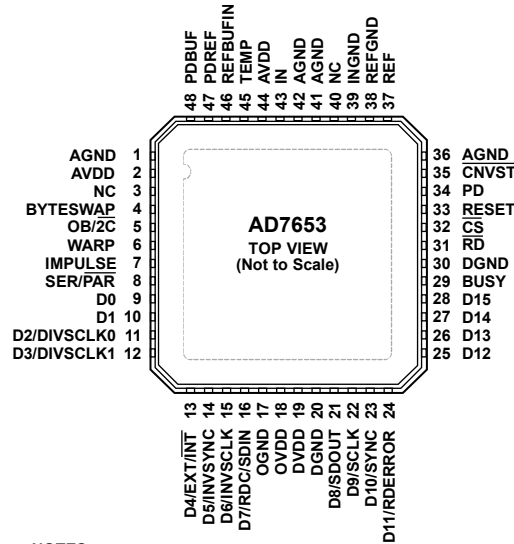
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE LFCSP PACKAGE HAS AN EXPOSED PAD. THIS EPAD CAN BE CONNECTED AGND. THIS CONNECTION IS NOT REQUIRED TO MEET ELECTRICAL PERFORMANCE SPECIFICATIONS.

02966-0-002

Figure 4. 48-Lead LQFP (ST-48) and 48-Lead LFCSP (CP-48-1)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
0	EPAD		Exposed Pad. The LFCSP package has an exposed pad. This EPAD can be connected to AGND. This connection is not required to meet electrical performance specifications.
1, 36, 41, 42	AGND	P	Analog Power Ground Pin.
2, 44	AVDD	P	Input Analog Power Pin. Nominally 5 V.
3, 40	NC		No Connect.
4	BYTESWAP	DI	Parallel Mode Selection (8-/16-bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	OB/ $\overline{2C}$	DI	Straight Binary/Binary Twos Complement. When OB/ $\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted, resulting in a twos complement output from its internal shift register.
6	WARP	DI	Mode Selection. When this pin is HIGH and the IMPULSE pin is LOW, this input selects the fastest mode, the maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When LOW, full accuracy is maintained independent of the minimum conversion rate.
7	IMPULSE	DI	Mode Selection. When IMPULSE is HIGH and WARP is LOW, this input selects a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	SER/ \overline{PAR}	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface mode is selected and some bits of the DATA bus are used as a serial port.
9, 10	D[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, these outputs are in high impedance.
11, 12	D[2:3] or DIVSCLK[0:1]	DI/O	When SER/ \overline{PAR} is LOW, these outputs are used as Bit 2 and Bit 3 of the parallel port data output bus. When SER/ \overline{PAR} is HIGH, EXT/INT is LOW, and RDC/SDIN is LOW (serial master read after convert), these inputs, part of the serial port, are used to slow down, if desired, the internal serial clock that clocks the data output. In other serial modes, these pins are not used.

Pin No.	Mnemonic	Type ¹	Description
13	D4 or EXT/ $\overline{\text{INT}}$	DI/O	When SER/ $\overline{\text{PAR}}$ is LOW, this output is used as Bit 4 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal data clock or an external data clock. With EXT/ $\overline{\text{INT}}$ tied LOW, the internal clock is selected on the SCLK output. With EXT/ $\overline{\text{INT}}$ set to logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D5 or INVS $\overline{\text{SYNC}}$	DI/O	When SER/ $\overline{\text{PAR}}$ is LOW, this output is used as Bit 5 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal. It is active in both master and slave modes. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	D6 or INV $\overline{\text{SCLK}}$	DI/O	When SER/ $\overline{\text{PAR}}$ is LOW, this output is used as Bit 6 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave modes.
16	D7 or RDC/ $\overline{\text{SDIN}}$	DI/O	When SER/ $\overline{\text{PAR}}$ is LOW, this output is used as Bit 7 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/ $\overline{\text{INT}}$. When EXT/ $\overline{\text{INT}}$ is HIGH, RDC/ $\overline{\text{SDIN}}$ could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDO $\overline{\text{UT}}$ line. The digital data level on SDIN is output on DATA with a delay of 16 SCLK periods after the initiation of the read sequence. When EXT/ $\overline{\text{INT}}$ is LOW, RDC/ $\overline{\text{SDIN}}$ is used to select the read mode. When RDC/ $\overline{\text{SDIN}}$ is HIGH, the data is output on SDO $\overline{\text{UT}}$ during conversion. When RDC/ $\overline{\text{SDIN}}$ is LOW, the data can be output on SDO $\overline{\text{UT}}$ only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 5 V.
20	DGND	P	Digital Power Ground.
21	D8 or SDO $\overline{\text{UT}}$	DO	When SER/ $\overline{\text{PAR}}$ is LOW, this output is used as Bit 8 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ is HIGH, this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7653 provides the conversion result, MSB first, from its internal shift register. The DATA format is determined by the logic level of OB/ $\overline{\text{ZC}}$. In serial mode when EXT/ $\overline{\text{INT}}$ is LOW, SDO $\overline{\text{UT}}$ is valid on both edges of SCLK. In serial mode when EXT/ $\overline{\text{INT}}$ is HIGH, if INV $\overline{\text{SCLK}}$ is LOW, SDO $\overline{\text{UT}}$ is updated on the SCLK rising edge and valid on the next falling edge; if INV $\overline{\text{SCLK}}$ is HIGH, SDO $\overline{\text{UT}}$ is updated on the SCLK falling edge and valid on the next rising edge.
22	D9 or SCLK	DI/O	When SER/ $\overline{\text{PAR}}$ is LOW, this output is used as Bit 9 of the parallel port data or SCLK output bus. When SER/ $\overline{\text{PAR}}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, depending upon the logic state of the EXT/ $\overline{\text{INT}}$ pin. The active edge where the data SDO $\overline{\text{UT}}$ is updated depends upon the logic state of the INV $\overline{\text{SCLK}}$ pin.
23	D10 or SYNC	DO	When SER/ $\overline{\text{PAR}}$ is LOW, this output is used as Bit 10 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/ $\overline{\text{INT}}$ = logic LOW). When a read sequence is initiated and INVS $\overline{\text{SYNC}}$ is LOW, SYNC is driven HIGH and remains HIGH while the SDO $\overline{\text{UT}}$ output is valid. When a read sequence is initiated and INVS $\overline{\text{SYNC}}$ is HIGH, SYNC is driven LOW and remains LOW while the SDO $\overline{\text{UT}}$ output is valid.
24	D11 or RD $\overline{\text{ERROR}}$	DO	When SER/ $\overline{\text{PAR}}$ is LOW, this output is used as Bit 11 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ and EXT/ $\overline{\text{INT}}$ are HIGH, this output, part of the serial port, is used as an incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RD $\overline{\text{ERROR}}$ is pulsed HIGH.
25–28	D[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data Output Bus. These pins are always outputs regardless of the state of SER/ $\overline{\text{PAR}}$.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
30	DGND	P	Must Be Tied to Digital Ground.
31	$\overline{\text{RD}}$	DI	Read Data. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled.

Pin No.	Mnemonic	Type ¹	Description
32	$\overline{\text{CS}}$	DI	Chip Select. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{\text{CS}}$ is also used to gate the external clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, this pin resets the AD7653 and the current conversion, if any, is aborted. If not used, this pin could be tied to DGND.
34	PD	DI	Power-Down Input. When set to logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{\text{CNVST}}$	DI	Start Conversion. A falling edge on $\overline{\text{CNVST}}$ puts the internal sample/hold into the hold state and initiates a conversion. In Impulse mode (IMPULSE HIGH, WARP LOW), if $\overline{\text{CNVST}}$ is held LOW when the acquisition phase (t_a) is complete, the internal sample/hold is put into the hold state and a conversion is immediately started.
37	REF	AI/O	Reference Input Voltage. On-chip reference output voltage.
38	REFGND	AI	Reference Input Analog Ground.
39	INGND	AI	Analog Input Ground.
43	IN	AI	Primary Analog Input with a Range of 0 V to 2.5 V.
45	TEMP	AO	Temperature Sensor Voltage Output.
46	REFBUFIN	AI/O	Reference Input Voltage. The reference output and the reference buffer input.
47	PDREF	DI	This pin allows the choice of internal or external voltage references. When LOW, the on-chip reference is turned on. When HIGH, the internal reference is switched off and an external reference must be used.
48	PDBUF	DI	This pin allows the choice of buffering an internal or external reference with the internal buffer. When LOW, the buffer is selected. When HIGH, the buffer is switched off.

¹ AI = Analog Input; AI/O = Bidirectional Analog; AO = Analog Output; DI = Digital Input; DI/O = Bidirectional Digital; DO = Digital Output; P = Power.

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity Error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Full-Scale Error

The last transition (from 011...10 to 011...11 in twos complement coding) should occur for an analog voltage 1½ LSB below the nominal full scale (2.49994278 V for the 0 V to 2.5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

Unipolar Zero Error

The first transition should occur at a level ½ LSB above analog ground (19.073 µV for the 0 V to 2.5 V range). Unipolar zero error is the deviation of the actual transition from that point.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to $S/(N+D)$ by the following formula:

$$ENOB = (S/[N+D]dB - 1.76)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal, and is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio ($S/[N+D]$)

$S/(N+D)$ is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for $S/(N+D)$ is expressed in decibels.

Aperture Delay

Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the CNVST input to when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the AD7653 to achieve its rated accuracy after a full-scale step function is applied to its input.

Overvoltage Recovery

Overvoltage recovery is the time required for the ADC to recover to full accuracy after an analog input signal 150% of the full-scale value is reduced to 50% of the full-scale value.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is the change of internal reference voltage output voltage V over the operating temperature range and normalized by the output voltage at 25°C, expressed in ppm/°C. The equation follows:

$$TCV(ppm/°C) = \frac{V(T_2) - V(T_1)}{V(25°C) \times (T_2 - T_1)} \times 10^6$$

where:

$V(25°C) = V$ at +25°C.

$V(T_2) = V$ at Temperature 2 (+85°C).

$V(T_1) = V$ at Temperature 1 (-40°C).

TYPICAL PERFORMANCE CHARACTERISTICS

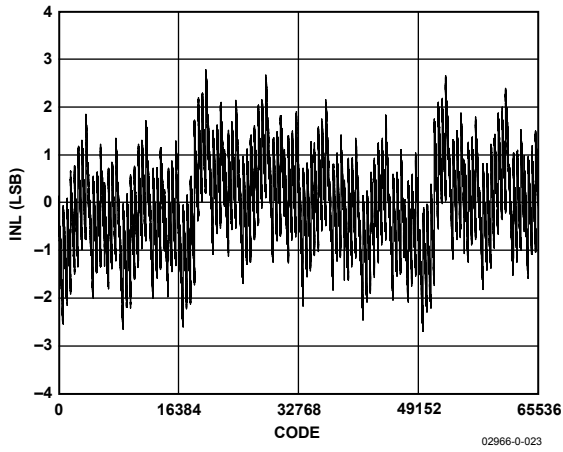


Figure 5. Integral Nonlinearity vs. Code

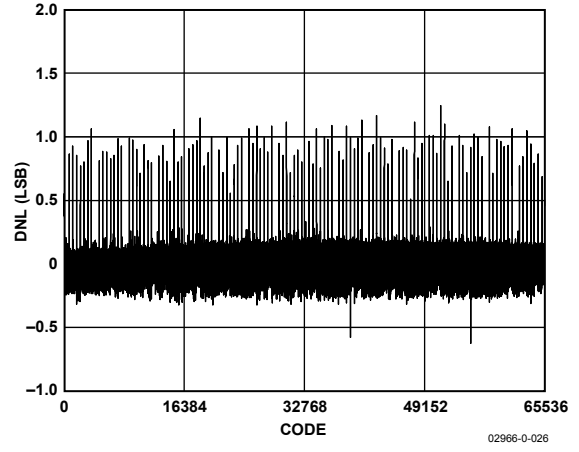


Figure 8. Differential Nonlinearity vs. Code

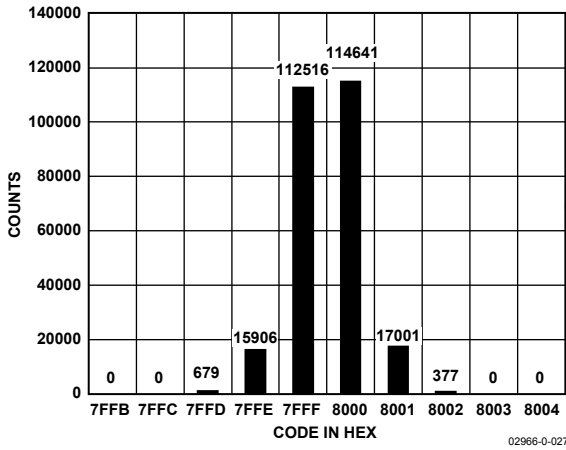


Figure 6. Histogram of 261,120 Conversions of a DC Input at the Code Transition

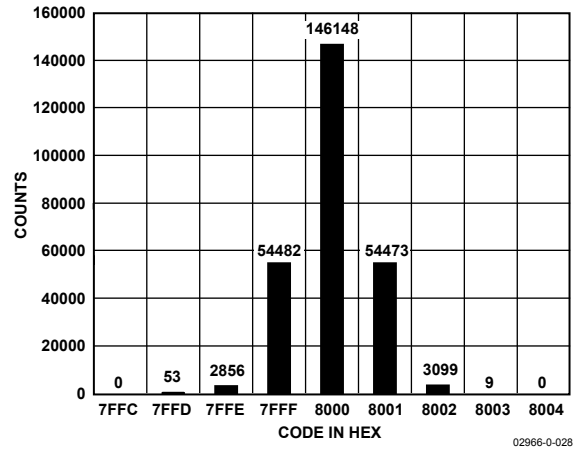


Figure 9. Histogram of 261,120 Conversions of a DC Input at the Code Center

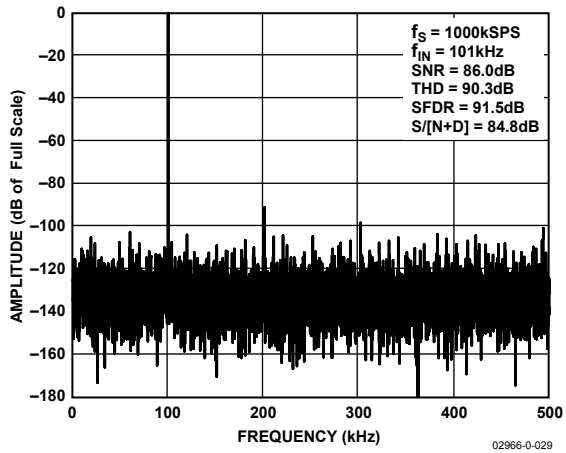


Figure 7. FFT Plot

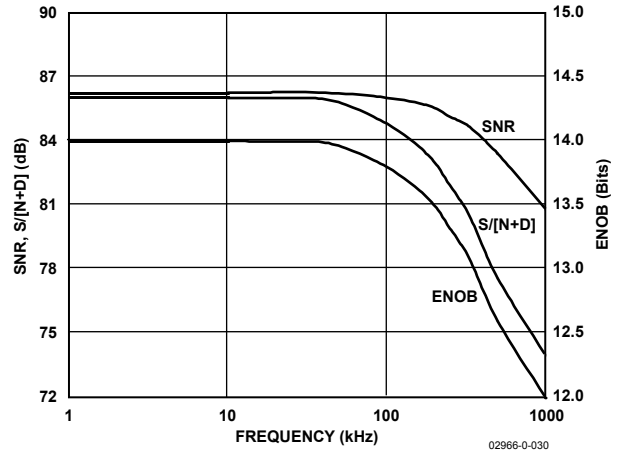


Figure 10. SNR, S/(N+D), and ENOB vs. Frequency

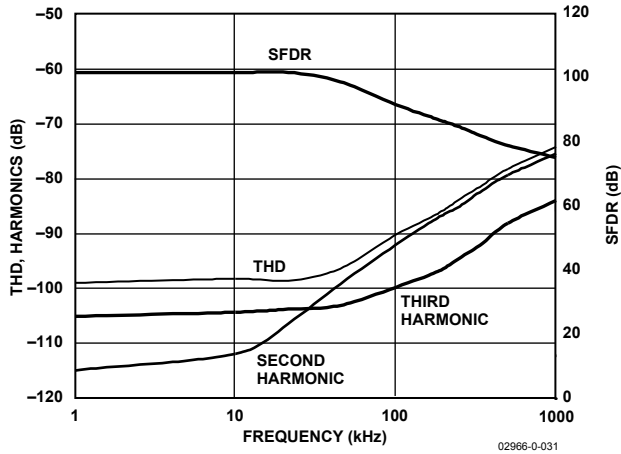


Figure 11. THD, Harmonics, and SFDR vs. Frequency

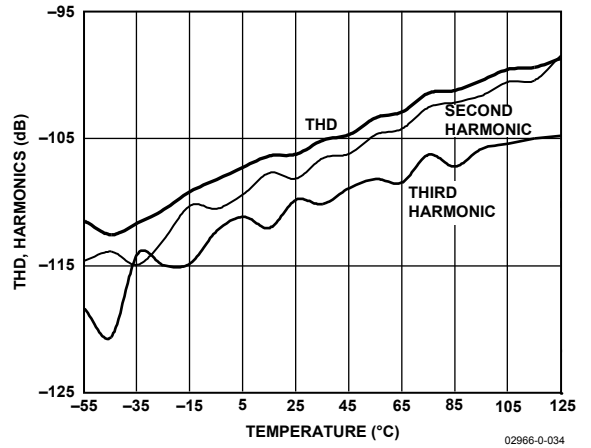


Figure 14. THD and Harmonics vs. Temperature

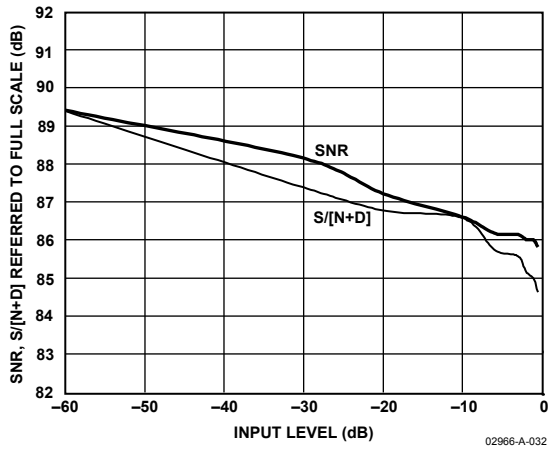


Figure 12. SNR and S/(N+D) vs. Input Level (Referred to Full Scale)

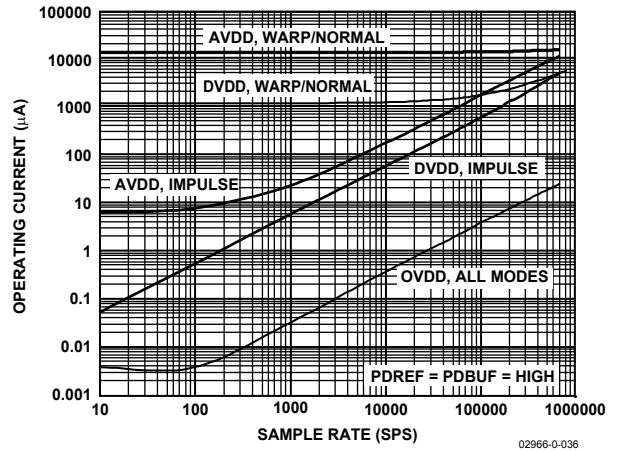


Figure 15. Operating Current vs. Sample Rate

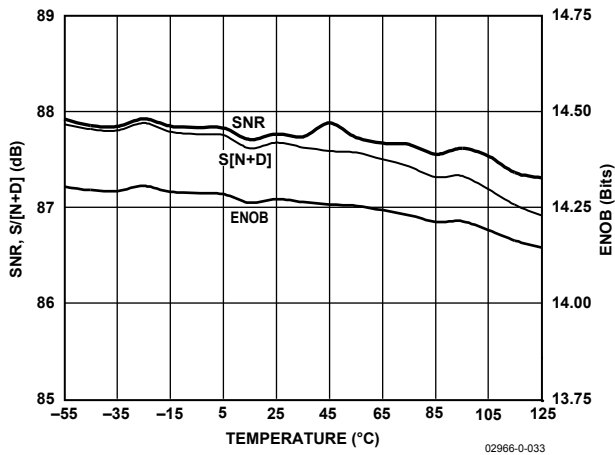


Figure 13. SNR, S/(N+D), and ENOB vs. Temperature

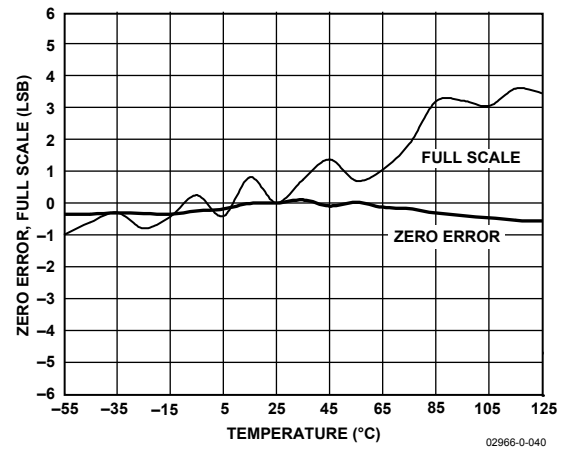


Figure 16. Zero Error, Full Scale with Reference vs. Temperature

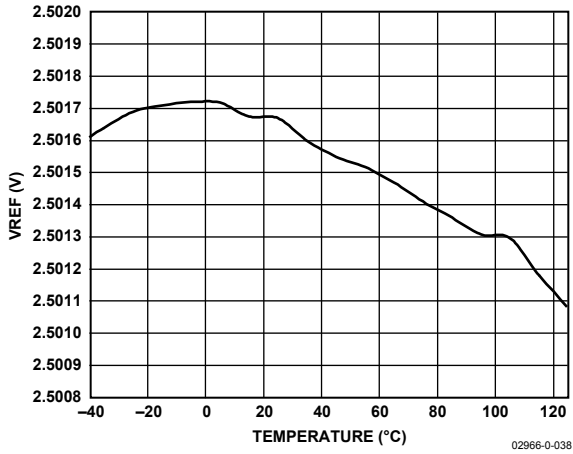


Figure 17. Typical Reference Output Voltage vs. Temperature

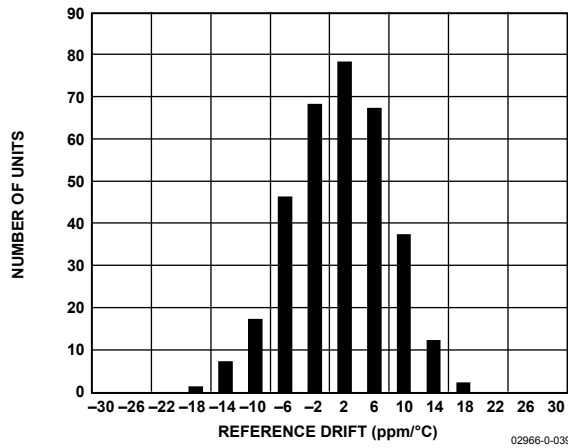


Figure 18. Reference Voltage Temperature Coefficient Distribution (335 Units)

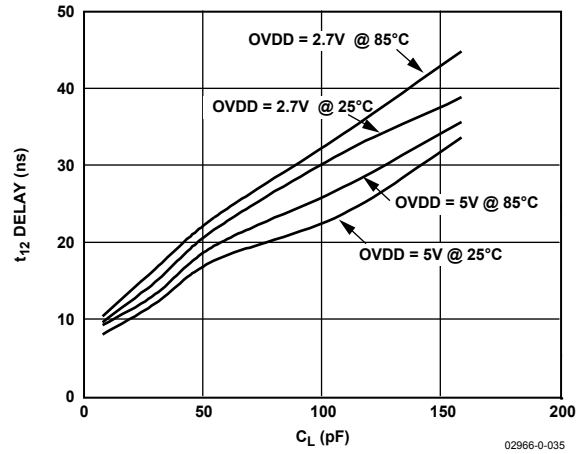
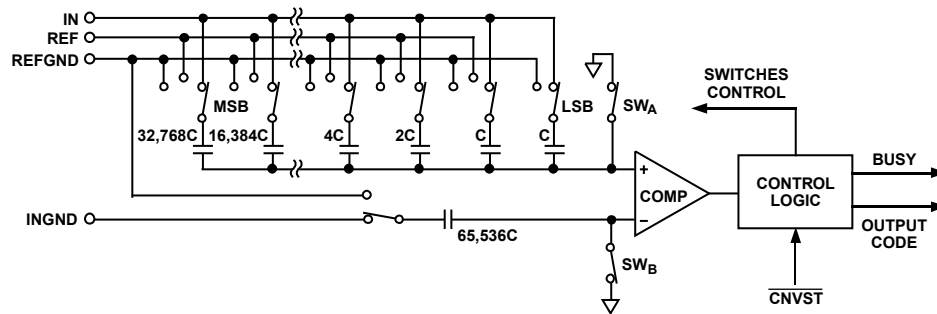


Figure 19. Typical Delay vs. Load Capacitance C_L

CIRCUIT INFORMATION



02966-0-005

Figure 20. ADC Simplified Schematic

The [AD7653](#) is a very fast, low power, single supply, precise 16-bit analog-to-digital converter (ADC). The [AD7653](#) features different modes to optimize performance according to the application. In Warp mode, the part can convert 1 million samples per second.

The [AD7653](#) provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The [AD7653](#) can be operated from a single 5 V supply and can be interfaced to either 5 V or 3 V digital logic. It is housed in either a 48-lead LQFP or a 48-lead LFCSP that saves space and allows flexible configurations as either a serial or a parallel interface. The [AD7653](#) is a pin-to-pin compatible upgrade of the [AD7651/AD7652](#).

CONVERTER OPERATION

The [AD7653](#) is a successive approximation ADC based on a charge redistribution DAC. Figure 20 shows a simplified schematic of the ADC. The capacitive DAC consists of an array of 16 binary weighted capacitors and an additional LSB capacitor. The comparator's negative input is connected to a dummy capacitor of the same value as the capacitive DAC array.

During the acquisition phase, the common terminal of the array tied to the comparator's positive input is connected to AGND via SWA. All independent switches are connected to the analog input IN. Thus, the capacitor array is used as a sampling capacitor and acquires the analog signal on IN. Similarly, the dummy capacitor acquires the analog signal on INGND.

When $\overline{\text{CNVST}}$ goes LOW, a conversion phase is initiated. When the conversion phase begins, SWA and SWB are opened. The capacitor array and dummy capacitor are then disconnected

from the inputs and connected to REF and REFND. Therefore, the differential voltage between IN and INGND captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REF and REFND, the comparator input varies by binary weighted voltage steps ($V_{\text{REF}}/2$, $V_{\text{REF}}/4$, ... $V_{\text{REF}}/65536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition.

After this process is completed, the control logic generates the ADC output code and brings the BUSY output LOW.

Modes of Operation

The [AD7653](#) features three modes of operations: Warp, Normal, and Impulse. Each mode is best suited for specific applications.

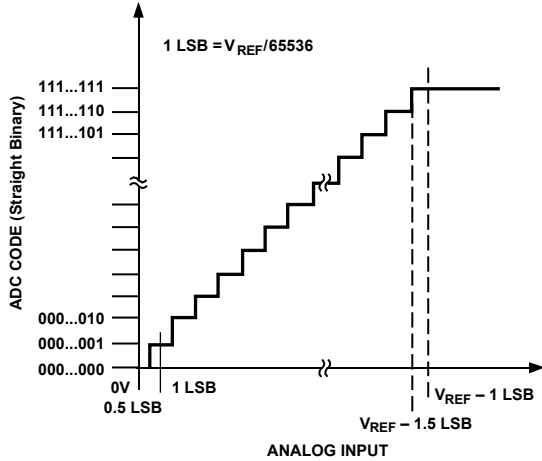
Warp mode allows the fastest conversion rate up to 1 MSPS. However in this mode and this mode only, the full specified accuracy is guaranteed only when the time between conversions does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms (e.g., after power-up), the first conversion result should be ignored. This mode makes the [AD7653](#) ideal for applications where both high accuracy and fast sample rate are required.

Normal mode is the fastest mode (800 kSPS) without any limitations on the time between conversions. This mode makes the [AD7653](#) ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

Impulse mode, the lowest power dissipation mode, allows power saving between conversions. When operating at 1 kSPS, for example, it typically consumes only 138 μW . This feature makes the [AD7653](#) ideal for battery-powered applications.

Transfer Functions

Using the $\overline{OB}/2\overline{C}$ digital input, the AD7653 offers two output codings: straight binary and twos complement. The LSB size is $V_{REF}/65536$, which is about $38.15 \mu\text{V}$. The AD7653's ideal transfer characteristic is shown in Figure 21 and Table 7.



02966-0-003

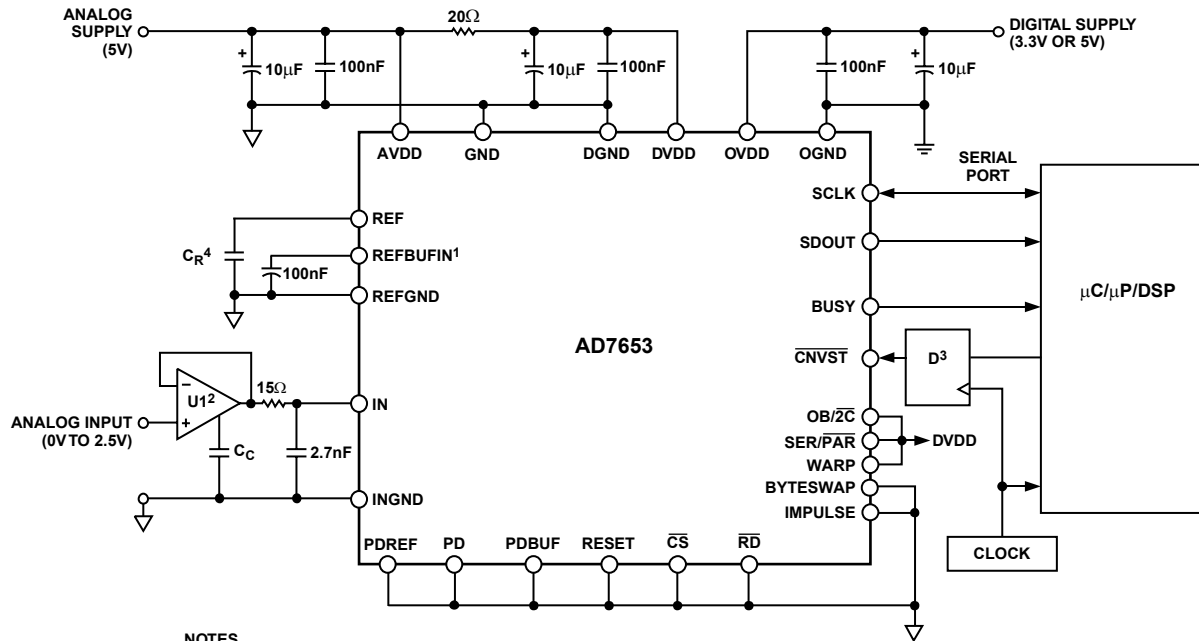
Figure 21. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input	Digital Output Code (Hex)	
		Straight Binary	Twos Complement
FSR - 1 LSB	2.499962 V	FFFF ¹	7FFF ¹
FSR - 2 LSB	2.499923 V	FFFE	7FFE
Midscale + 1 LSB	1.250038 V	8001	0001
Midscale	1.25 V	8000	0000
Midscale - 1 LSB	1.249962 V	7FFF	FFFF
-FSR + 1 LSB	38 μV	0001	8001
-FSR	0 V	0000 ²	8000 ²

¹This is also the code for overrange analog input ($V_{IN} - V_{INGND}$ above $V_{REF} - V_{REFGND}$).

²This is also the code for underrange analog input (V_{IN} below V_{INGND}).



NOTES

- ¹THE CONFIGURATION SHOWN IS USING THE INTERNAL REFERENCE AND INTERNAL BUFFER.
- ²THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
- ³OPTIONAL LOW JITTER.
- ⁴A 10 μF CERAMIC CAPACITOR (X5R, 1206 SIZE) IS RECOMMENDED (e.g., PANASONIC ECJ3YB0J106M). SEE VOLTAGE REFERENCE INPUT SECTION.

02966-A-004

Figure 22. Typical Connection Diagram

TYPICAL CONNECTION DIAGRAM

Figure 22 shows a typical connection diagram for the [AD7653](#).

Analog Input

Figure 23 shows an equivalent circuit of the input structure of the [AD7653](#).

The two diodes, D1 and D2, provide ESD protection for the analog inputs IN and INGND. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 100 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from AVDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

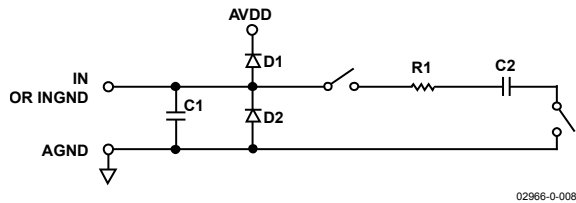


Figure 23. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the differential signal between IN and INGND. Unlike other converters, INGND is sampled at the same time as IN. By using this differential input, small signals common to both inputs are rejected. For instance, by using INGND to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated.

During the acquisition phase, the impedance of the analog input IN can be modeled as a parallel combination of capacitor C1 and the network formed by the series connection of R1 and C2. C1 is primarily the pin capacitance. R1 is typically 168 Ω and is a lumped component made up of some serial resistors and the on resistance of the switches. C2 is typically 60 pF and is mainly the ADC sampling capacitor.

During the conversion phase, when the switches are opened, the input impedance is limited to C1. R1 and C2 make a 1-pole low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the [AD7653](#) can be driven directly. Large source impedances will significantly affect the ac performance, especially total harmonic distortion.

Driver Amplifier Choice

Although the [AD7653](#) is easy to drive, the driver amplifier needs to meet the following requirements:

- The driver amplifier and the [AD7653](#) analog input circuit must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection. The tiny op amp [AD8021](#), which combines ultralow noise and high gain-bandwidth, meets this settling time requirement even when used with gains up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the [AD7653](#). The noise coming from the driver is filtered by the [AD7653](#) analog input circuit 1-pole low-pass filter made by R1 and C2 or by the external filter, if one is used.
- The driver needs to have a THD performance suitable to that of the [AD7653](#).

The [AD8021](#) meets these requirements and is appropriate for almost all applications. The [AD8021](#) needs a 10 pF external compensation capacitor that should have good linearity as an NPO ceramic or mica type.

The [AD8022](#) could also be used if a dual version is needed and gain of 1 is present. The [AD829](#) is an alternative in applications where high frequency (above 100 kHz) performance is not required. In gain of 1 applications, it requires an 82 pF compensation capacitor. The [AD8610](#) is an option when low bias current is needed in low frequency applications.

Voltage Reference Input

The AD7653 allows the choice of either a very low temperature drift internal voltage reference or an external 2.5 V reference.

Unlike many ADCs with internal references, the internal reference of the AD7653 provides excellent performance and can be used in almost all applications.

To use the internal reference along with the internal buffer, PDREF and PDBUF should both be LOW. This will produce a 1.207 V voltage on REFBUFIN which, amplified by the buffer, will result in a 2.5 V reference on the REF pin.

The output impedance of REFBUFIN is 11 k Ω (minimum) when the reference is enabled. It is useful to decouple REFBUFIN with a 100 nF ceramic capacitor. Thus, the 100 nF capacitor provides an RC filter for noise reduction.

To use an external reference along with the internal buffer, PDREF should be HIGH and PDBUF should be LOW. This powers down the internal reference and allows the 2.5 V reference to be applied to REFBUFIN.

To use an external reference directly on the REF pin, PDREF and PDBUF should both be HIGH.

PDREF and PDBUF, respectively, power down the internal reference and the internal reference. Note that the PDREF and PDBUF input current should never exceed 20 mA. This could eventually occur when input voltage is above AVDD (for instance at power-up). In this case, a 100 Ω series resistor is recommended.

The internal reference is temperature compensated to 2.5 V \pm 20 mV. The reference is trimmed to provide a typical drift of 7 ppm/ $^{\circ}$ C. This typical drift characteristic is shown in Figure 17. For improved drift performance, an external reference such as the AD780 can be used.

The AD7653 voltage reference input REF has a dynamic input impedance; it should, therefore, be driven by a low impedance source with efficient decoupling between the REF and REFGND inputs. This decoupling depends on the choice of the voltage reference, but usually consists of a low ESR capacitor connected to REF and REFGND with minimum parasitic inductance. A 10 μ F (X5R, 1206 size) ceramic chip capacitor (or 47 μ F tantalum capacitor) is appropriate when using either the internal reference or one of these recommended reference voltages:

- The low noise, low temperature drift ADR421 and AD780
- The low power ADR291
- The low cost AD1582

For applications that use multiple AD7653s, it is more effective to use the internal buffer to buffer the reference voltage.

Care should be taken with the voltage reference's temperature coefficient, which directly affects the full-scale accuracy, if this parameter matters. For instance, a ± 15 ppm/ $^{\circ}$ C temperature coefficient of the reference changes full scale by ± 1 LSB/ $^{\circ}$ C.

Note that V_{REF} can be increased to AVDD – 1.85 V. Since the input range is defined in terms of V_{REF}, this would essentially increase the range to 0 V to 3 V with an AVDD above 4.85 V. The AD780 can be selected with a 3 V reference voltage.

The TEMP pin, which measures the temperature of the AD7653, can be used as shown in Figure 24. The output of the TEMP pin is applied to one of the inputs of the analog switch (e.g., ADG779), and the ADC itself is used to measure its own temperature. This configuration is very useful for improving the calibration accuracy over the temperature range.

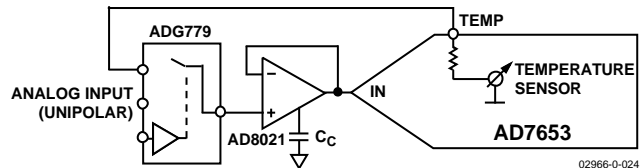


Figure 24. Temperature Sensor Connection Diagram

Power Supply

The AD7653 uses three power supply pins: an analog 5 V supply AVDD, a digital 5 V core supply DVDD, and a digital input/output interface supply OVDD. OVDD allows direct interface with any logic between 2.7 V and DVDD + 0.3 V. To reduce the supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply, as shown in Figure 22. The AD7653 is independent of power supply sequencing once OVDD does not exceed DVDD by more than 0.3 V, and is thus free of supply voltage induced latch-up.

POWER DISSIPATION VS. THROUGHPUT

Operating currents are very low during the acquisition phase, allowing significant power savings when the conversion rate is reduced (see Figure 25). This power savings depends on the mode used. In Impulse mode, the AD7653 automatically reduces power consumption at the end of each conversion phase. This makes the part ideal for very low power battery applications. The digital interface and the reference remain active even during the acquisition phase. To reduce operating digital supply currents even further, digital inputs need to be driven close to the power supply rails (i.e., DVDD or DGND), and OVDD should not exceed DVDD by more than 0.3 V.

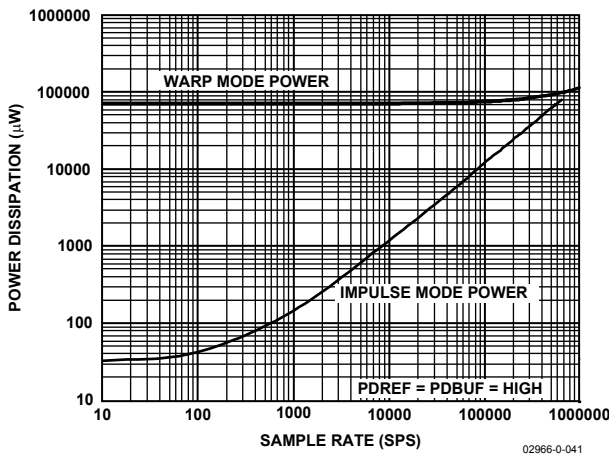


Figure 25. Power Dissipation vs. Sampling Rate

CONVERSION CONTROL

Figure 26 shows the detailed timing diagrams of the conversion process. The AD7653 is controlled by the $\overline{\text{CNVST}}$ signal, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. $\overline{\text{CNVST}}$ operates independently of CS and RD.

In Impulse mode, conversions can be automatically initiated. If $\overline{\text{CNVST}}$ is held LOW when BUSY is LOW, the AD7653 controls the acquisition phase and automatically initiates a new conversion. By keeping $\overline{\text{CNVST}}$ LOW, the AD7653 keeps the conversion process running by itself. It should be noted that the analog input must be settled when BUSY goes low. Also, at power-up, $\overline{\text{CNVST}}$ should be brought LOW once to initiate the conversion process. In this mode, the AD7653 can run slightly faster than the guaranteed 666 kSPS limits in Impulse mode. This feature does not exist in Warp and Normal modes.

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot and undershoot or ringing.

The $\overline{\text{CNVST}}$ trace should be shielded with ground and a low value serial resistor (i.e., 50 Ω) termination should be added close to the output of the component that drives this line.

For applications where SNR is critical, the $\overline{\text{CNVST}}$ signal should have very low jitter. This may be achieved by using a dedicated oscillator for $\overline{\text{CNVST}}$ generation, or to clock $\overline{\text{CNVST}}$ with a high frequency, low jitter clock, as shown in Figure 22.

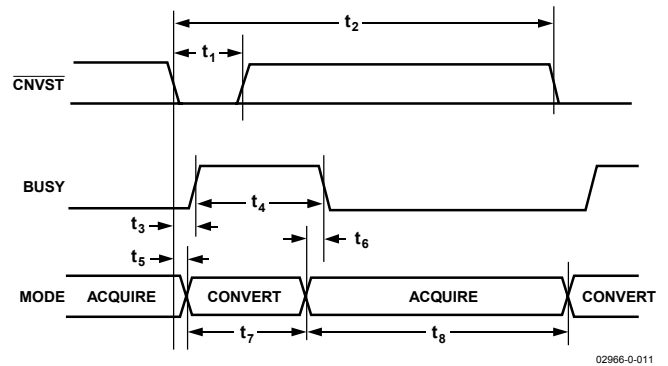


Figure 26. Basic Conversion Timing

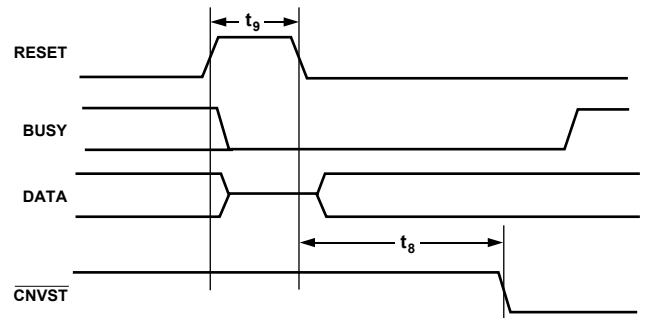


Figure 27. RESET Timing

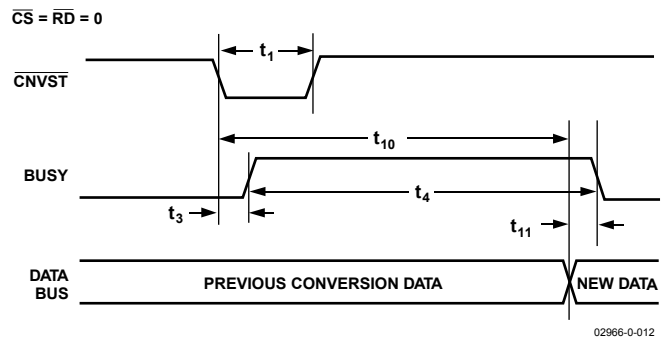


Figure 28. Master Parallel Data Timing for Reading (Continuous Read)

DIGITAL INTERFACE

The AD7653 has a versatile digital interface; it can be interfaced with the host system by using either a serial or a parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7653 digital interface also accommodates both 3 V and 5 V logic by simply connecting the OVDD supply pin of the AD7653 to the host system interface digital supply. Finally, by using the OB/2C input pin, both twos complement and straight binary coding can be used.

The two signals, CS and RD, control the interface. CS and RD have a similar effect because they are OR'd together internally. When at least one of these signals is HIGH, the interface outputs are in high impedance. Usually CS allows the selection of each AD7653 in multicircuit applications and is held LOW in a single AD7653 design. RD is generally used to enable the conversion result on the data bus.

PARALLEL INTERFACE

The AD7653 is configured to use the parallel interface when SER/PAR is held LOW. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 29 and Figure 30, respectively. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 31, the LSB byte is output on D[7:0] and the MSB is output on D[15:8] when BYTESWAP is LOW. When BYTESWAP is HIGH, the LSB and MSB bytes are swapped and the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16-bit data can be read in two bytes on either D[15:8] or D[7:0].

SERIAL INTERFACE

The AD7653 is configured to use the serial interface when SER/PAR is held HIGH. The AD7653 outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on the SCLK pin. The output data is valid on both the rising and falling edges of the data clock.

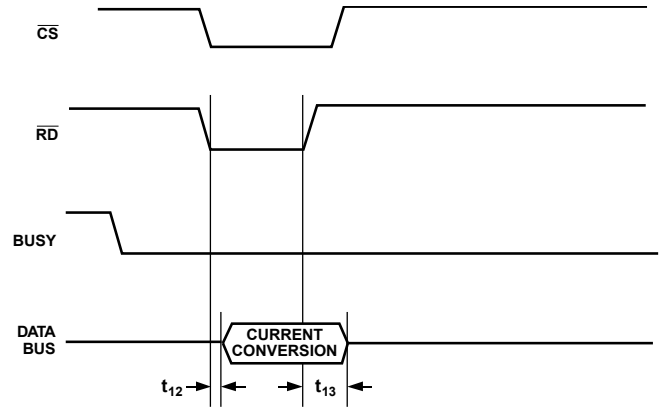


Figure 29. Slave Parallel Data Timing for Reading (Read after Convert Mode)

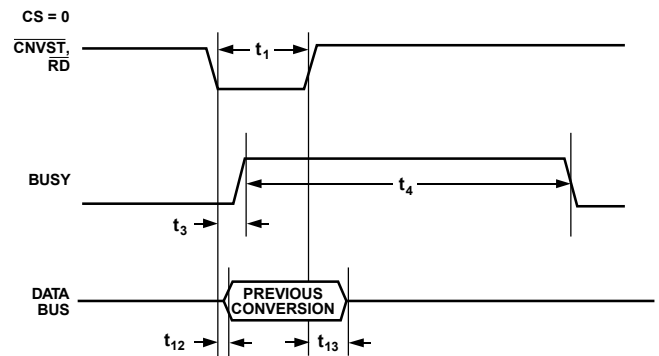


Figure 30. Slave Parallel Data Timing for Reading (Read during Convert Mode)

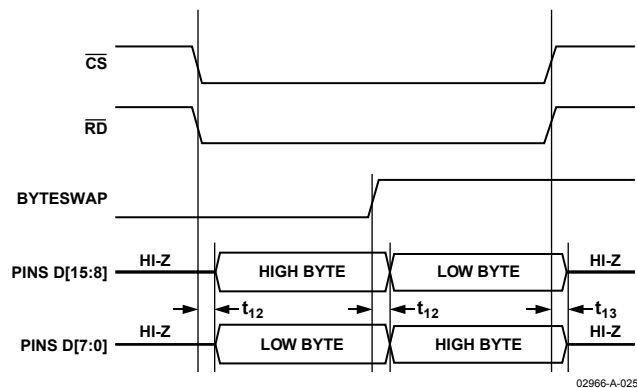


Figure 31. 8-Bit Parallel Interface

MASTER SERIAL INTERFACE

Internal Clock

The AD7653 is configured to generate and provide the serial data clock SCLK when the EXT/INT pin is held LOW. The AD7653 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted, if desired. Depending on the RDC/SDIN input, the data can be read after each conversion or during the following conversion. Figure 32 and Figure 33 show the detailed timing diagrams of these two modes.

Usually, because the AD7653 is used with a fast throughput, the Master Read During Conversion mode is the most recommended serial mode. In this mode, the serial clock and data toggle at appropriate instants, minimizing potential feedthrough between digital activity and critical conversion decisions.

In Read After Conversion mode, it should be noted that unlike in other modes, the BUSY signal returns LOW after the 16 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width.

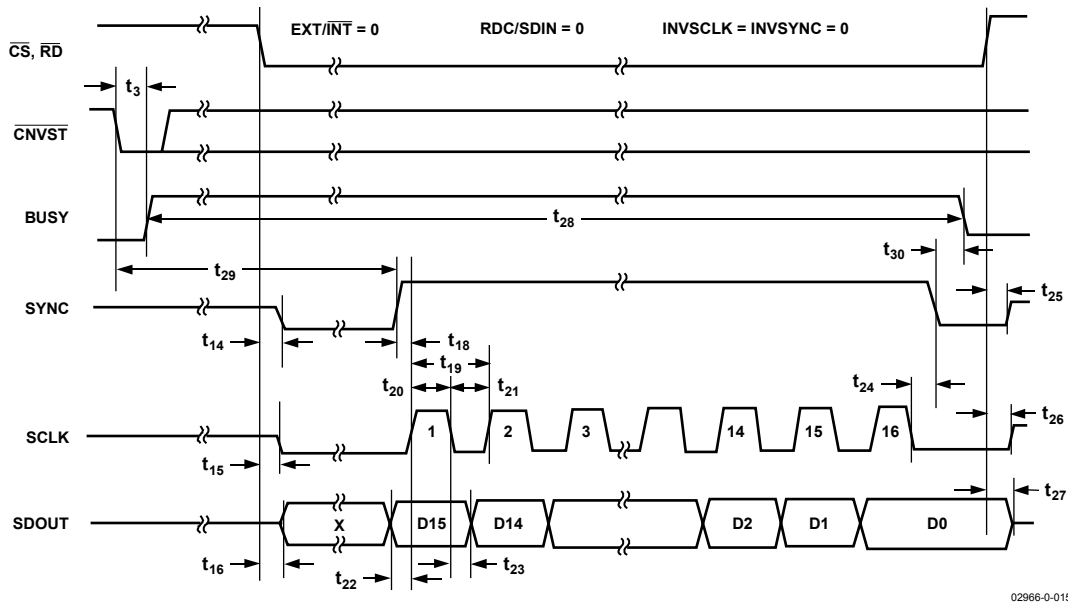


Figure 32. Master Serial Data Timing for Reading (Read after Convert)

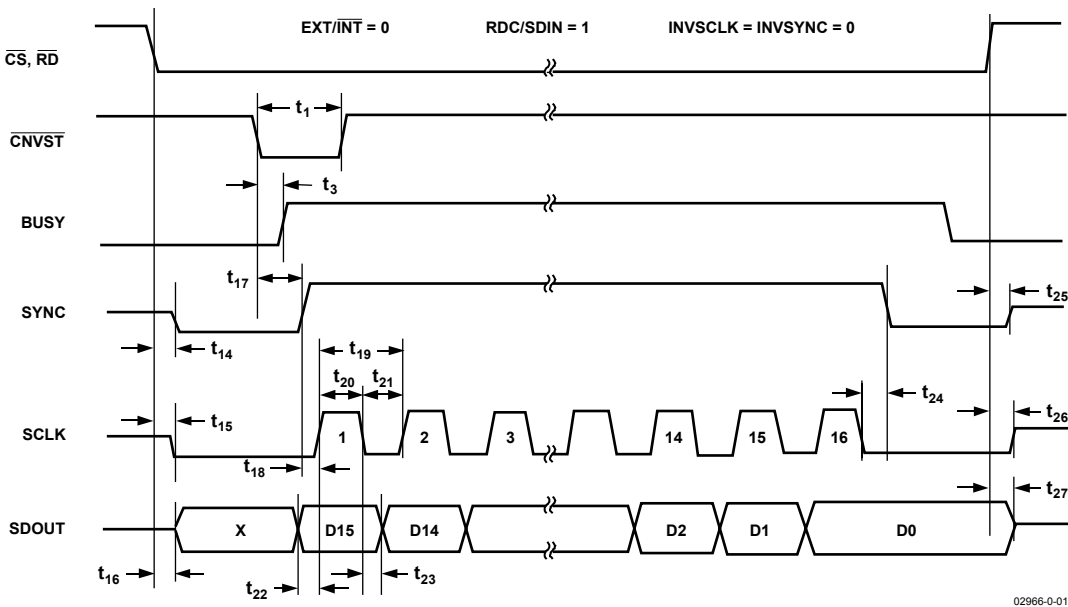


Figure 33. Master Serial Data Timing for Reading (Read Previous Conversion during Convert)

SLAVE SERIAL INTERFACE

External Clock

The AD7653 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/INT pin is held HIGH. In this mode, several methods can be used to read the data. The external serial clock is gated by CS. When CS and RD are both LOW, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or a discontinuous clock. A discontinuous clock can be either normally HIGH or normally LOW when inactive. Figure 34 and Figure 35 show the detailed timing diagrams of these methods.

While the AD7653 is performing a bit decision, it is important that voltage transients be avoided on digital input/output pins, or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7653 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is LOW, or, more importantly, that it does not transition during the latter half of BUSY HIGH.

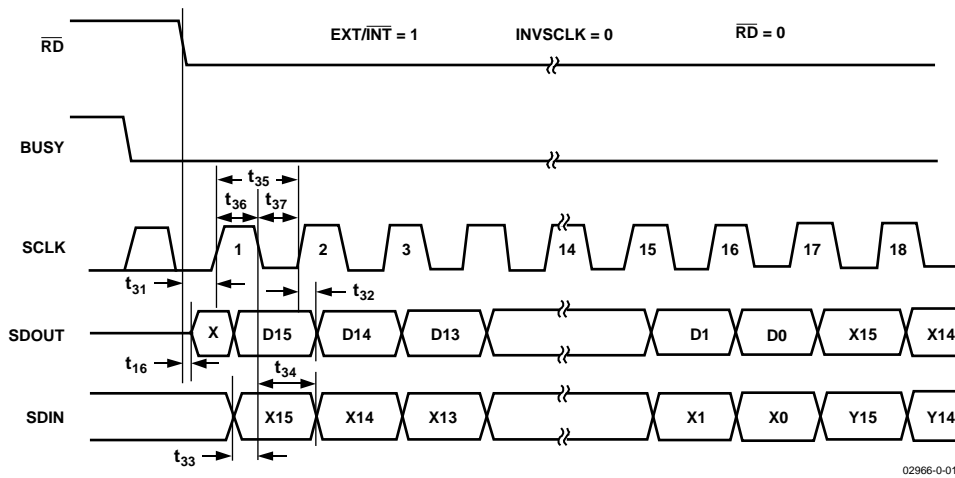


Figure 34. Slave Serial Data Timing for Reading (Read after Convert)

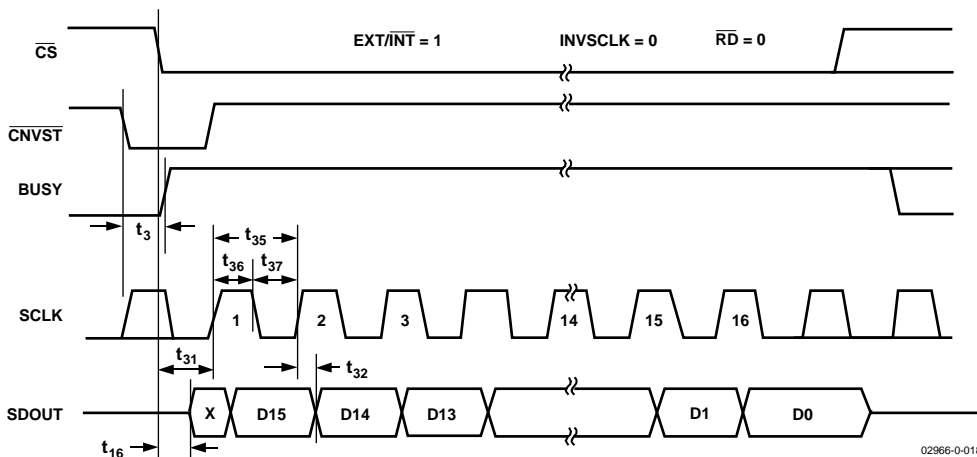


Figure 35. Slave Serial Data Timing for Reading (Read Previous Conversion during Convert)

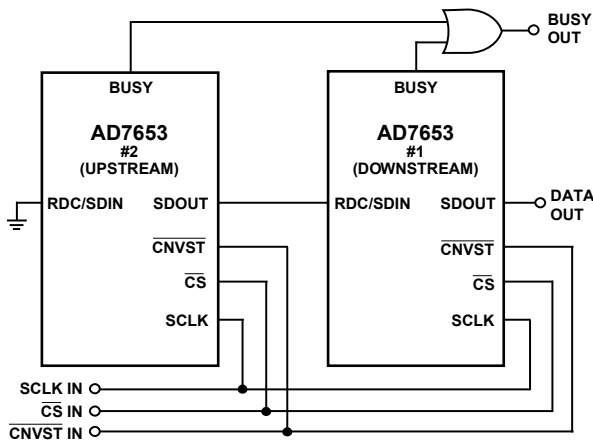
External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 34 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by **BUSY** returning **LOW**, the conversion's result can be read while both **CS** and **RD** are **LOW**. Data is shifted out MSB first with 16 clock pulses and is valid on the rising and falling edges of the clock.

Among the advantages of this method is the fact that conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is the ability to read the data at any speed up to 40 MHz, which accommodates both the slow digital host interface and the fastest serial reading.

Finally, in this mode only, the **AD7653** provides a daisy-chain feature using the **RDC/SDIN** pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired, as, for instance, in isolated multiconverter applications.

The concatenation of two devices is shown in Figure 36. Simultaneous sampling is possible by using a common **CNVST** signal. It should be noted that the **RDC/SDIN** input is latched on the edge of **SCLK** opposite the one used to shift out the data on **SDOUT**. Thus, the MSB of the upstream converter follows the LSB of the downstream converter on the next **SCLK** cycle.



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Figure 36. Two **AD7653**s in a Daisy-Chain Configuration

External Clock Data Read During Conversion

Figure 35 shows the detailed timing diagrams of this method. During a conversion, while both **CS** and **RD** are both **LOW**, the result of the previous conversion can be read. The data is shifted out MSB first with 16 clock pulses, and is valid on both the rising and falling edges of the clock. The 16 bits must be read before the current conversion is complete; otherwise, **RDERROR** is pulsed **HIGH** and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode, and the **RDC/SDIN** input should always be tied either **HIGH** or **LOW**.

To reduce performance degradation due to digital activity, a fast discontinuous clock (at least 18 MHz when Impulse mode is used, 25 MHz when Normal mode is used, or 40 MHz when Warp mode is used) is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read data after conversion and continue to read the last bits after a new conversion has been initiated. This allows the use of a slower clock speed like 14 MHz in Impulse mode, 18 MHz in Normal mode, and 25 MHz in Warp mode.

MICROPROCESSOR INTERFACING

The AD7653 is ideally suited for traditional dc measurement applications supporting a microprocessor, and for ac signal processing applications interfacing to a digital signal processor. The AD7653 is designed to interface either with a parallel 8-bit or 16-bit wide interface, or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7653 to prevent digital noise from coupling into the ADC. The following section discusses the use of an AD7653 with an SPI equipped DSP, the ADSP-2191M.

SPI Interface (ADSP-2191M)

Figure 37 shows an interface diagram between the AD7653 and the SPI equipped ADSP-2191M. To accommodate the slower speed of the DSP, the AD7653 acts as a slave device and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command can be initiated in response to an internal timer interrupt. The reading process can be initiated in response to the end-of-conversion signal (BUSY going LOW) using an interrupt line of the DSP. The serial inter-

face (SPI) on the ADSP-2191M is configured for master mode—(MSTR) = 1, Clock Polarity bit (CPOL) = 0, Clock Phase bit (CPHA) = 1, and SPI Interrupt Enable (TIMOD) = 00—by writing to the SPI control register (SPICLTX). To meet all timing requirements, the SPI clock should be limited to 17 Mbps, which allows it to read an ADC result in less than 1 μs. When a higher sampling rate is desired, use of one of the parallel interface modes is recommended.

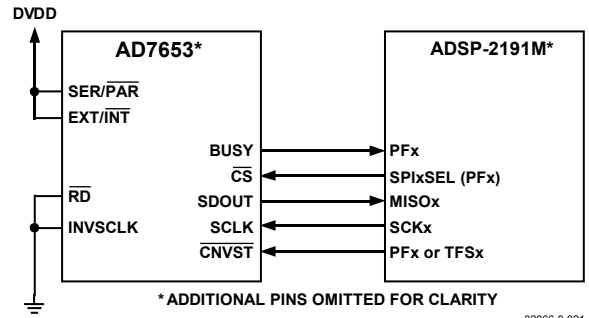
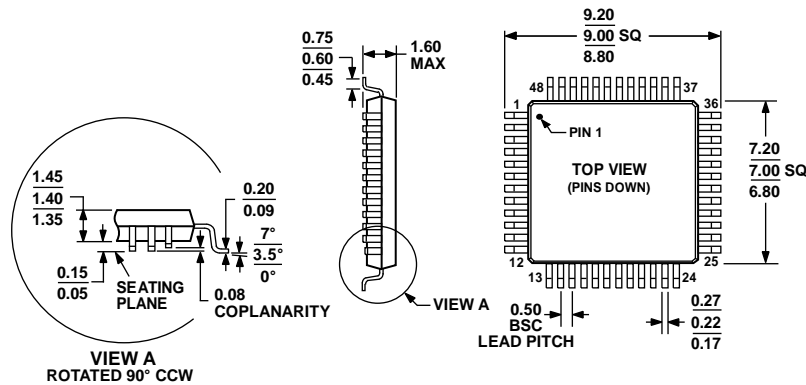


Figure 37. Interfacing the AD7653 to an SPI Interface

OUTLINE DIMENSIONS

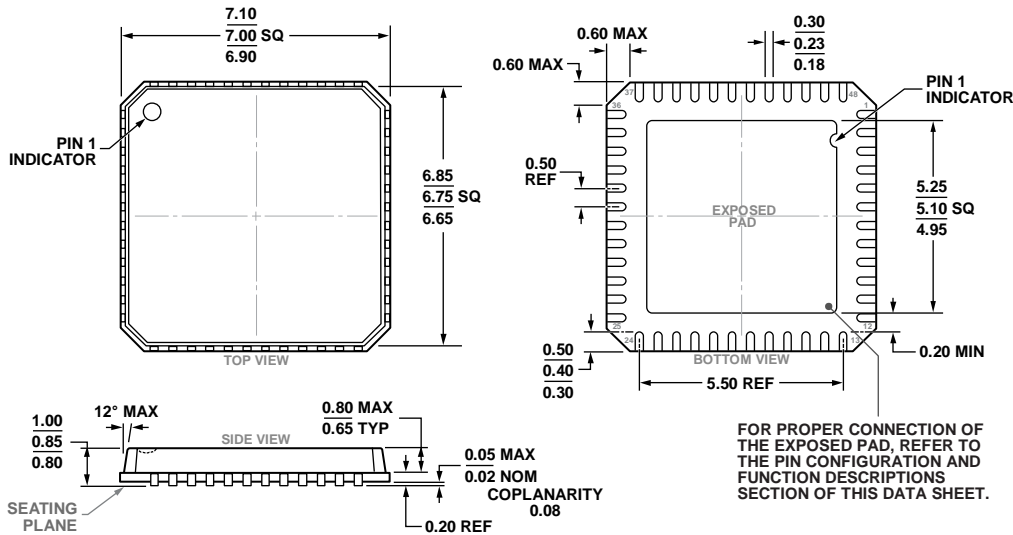


COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 39. 48-Lead Quad Flat Package [LQFP] (ST-48)

Dimensions shown in millimeters

051706-A



COMPLIANT TO JEDEC STANDARDS MO-220-VKDD-2

Figure 40. 48-Lead Lead Frame Chip Scale Package [LFCSP] 7 mm x 7 mm Body and 0.85 mm Package Height (CP-48-1)

Dimensions shown in millimeters

11-13-2017-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD7653ASTZ	-40°C to +85°C	48-Lead Quad Flat Package [LQFP]	ST-48
AD7653ASTZRL	-40°C to +85°C	48-Lead Quad Flat Package [LQFP]	ST-48
AD7653ACPZ	-40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-1
AD7653ACPZRL	-40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-1

¹Z = RoHS Compliant Part.

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