Triple, 1.5 GHz Op Amp

Data Sheet **AD8003**

FEATURES

High speed
- **1650 MHz (G = +1)**
- **730 MHz (G = +2, V_O = 2 V p-p)**
- **4300 V/µs (G = +2, 4 V step)**
- **Settling time 12 ns to 0.1%, 2 V step**

Excellent for QXGA resolution video
- **Gain flatness 0.1 dB to 190 MHz**
- **0.05% differential gain error, R_L = 150 Ω**
- **0.01° differential phase error, R_L = 150 Ω**

Low voltage offset: 0.7 mV (typical)
Low input bias current: 7 µA (typical)
Low noise: 1.8 nV/√Hz
Low distortion over wide bandwidth: SFDR −73 dBc @ 20 MHz
High output drive: 100 mA output load drive
Supply operation: +5 V to ±5 V voltage supply
Supply current: 9.5 mA/amplifier

APPLICATIONS

High resolution video graphics
Professional video
Consumer video
High speed instrumentation
Muxing

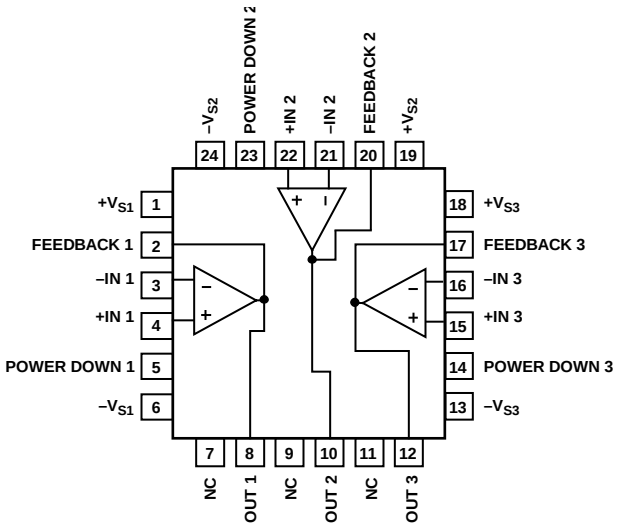
GENERAL DESCRIPTION

The AD8003 is a triple ultrahigh speed current feedback amplifier. Using ADI's proprietary eXtra Fast Complementary Bipolar (XFCB) process, the AD8003 achieves a bandwidth of 1.5 GHz and a slew rate of 4300 V/µs. Additionally, the amplifier provides excellent dc precision with an input bias current of 50 µA maximum and a dc input voltage of 0.7 mV.

The AD8003 has excellent video specifications with a frequency response that remains flat out to 190 MHz and 0.1% settling within 12 ns to ensure that even the most demanding video systems maintain excellent fidelity. For applications that use NTSC video, as well as high speed video, the amplifier provides a differential gain of 0.05% and a differential gain of 0.01°.

The AD8003 has very low spurious-free dynamic range (SFDR) (−73 dBc @ 20 MHz) and noise (1.8 nV/√Hz). With a supply range between 5 V and 11 V and ability to source 100 mA of output current, the AD8003 is ideal for a variety of applications.

CONNECTION DIAGRAM



NOTES
1. NC = NO CONNECT.
2. EXPOSED PAD (LFCSP ONLY): THE EXPOSED PAD CAN BE CONNECTED TO GND OR POWER PLANES, OR IT CAN BE LEFT FLOATING.

Figure 1. 24-Lead, 4 mm × 4 mm LFCSP_WQ (CP-24)

The AD8003 operates on only 9.5 mA of supply current per amplifier. The independent power-down function of the AD8003 reduces the quiescent current even further to 1.6 mA.

The AD8003 amplifier is available in a compact 4 mm × 4 mm, 24-lead LFCSP_WQ. The AD8003 is rated to work over the industrial temperature range of −40°C to +85°C.

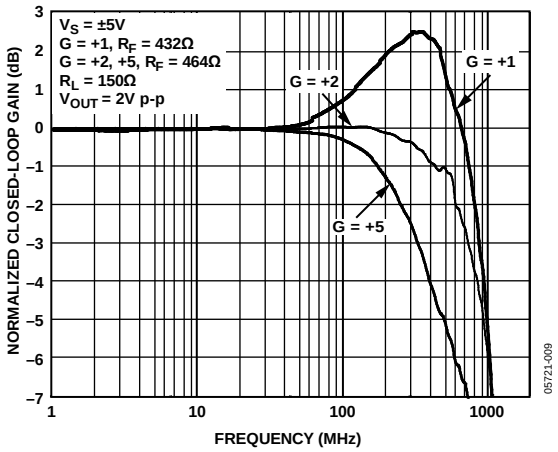


Figure 2. Large Signal Frequency Response for Various Gains

Rev. C **Document Feedback**

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9/08—Rev. A to Rev. B

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2/06—Rev. 0 to Rev. A

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10/05—Revision 0: Initial Version

SPECIFICATIONS WITH ±5 V SUPPLY

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, Gain = +2, R_F = 464 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p, R_F = 432 Ω		1650		MHz
	G = +2, V_O = 2 V p-p		730		MHz
	G = +10, V_O = 0.2 V p-p		290		MHz
	G = +5, V_O = 2 V p-p		330		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p		190		MHz
Slew Rate	G = +2, V_O = 2 V step, R_L = 150 Ω		3800		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		12		ns
Overload Recovery Input/Output			30/40		ns
NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic @ 5 MHz	G = +1, V_O = 2 V p-p		76/97		dBc
Second/Third Harmonic @ 20 MHz	G = +1, V_O = 2 V p-p		79/73		dBc
Input Voltage Noise	f = 1 MHz		1.8		nV/√Hz
Input Current Noise (I^-/I^+)	f = 1 MHz		36/3		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.05		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.01		Degree
DC PERFORMANCE					
Input Offset Voltage		−9.3	+0.7	+9.3	mV
	$T_{MIN} - T_{MAX}$		1.08		mV
Input Offset Voltage Drift			7.4		µV/°C
Input Bias Current	$+I_B/-I_B$	−19/−40	−7/−7	+4/+50	µA
	$T_{MIN} - T_{MAX}$ ($+I_B/-I_B$)		−3.8/+29.5		µA
Input Offset Current			±14.2		µA
Transimpedance	V_O = ±2.5 V	400	600	1100	kΩ
INPUT CHARACTERISTICS					
Noninverting Input Impedance			1.6/3		MΩ/pF
Input Common-Mode Voltage Range			±3.6		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	−51	−48	−46	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	±3.85	±3.9	±3.92	V
Linear Output Current	V_O = 2 V p-p, second harmonic < −50 dBc		100		mA
Capacitive Load Drive	40% over shoot		27		pF
POWER DOWN PINS					
Power-Down Input Voltage	Power down		<V_S − 2.5		V
	Enable		>V_S − 2.5		V
Turn-Off Time	50% of power-down voltage to 10% of V_{OUT} final, V_{IN} = 0.5 V p-p		40		ns
Turn-On Time	50% of power-down voltage to 90% of V_{OUT} final, V_{IN} = 0.5 V p-p		130		ns
Input Current					
Enabled			0.1		µA
Power-Down		−365	−235	−85	µA
POWER SUPPLY					
Operating Range		4.5		10	V
Quiescent Current per Amplifier	Enabled	8.1	9.5	10.2	mA
Quiescent Current per Amplifier	Power down	1.2	1.4	1.6	mA
Power Supply Rejection Ratio (+PSRR/−PSRR)		−59/−57	−57/−53	−55/−50	dB

SPECIFICATIONS WITH +5 V SUPPLY

T_A = 25°C, V_S = 5 V, R_L = 150 Ω, Gain = +2, R_F = 464 Ω, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p, R_F = 432 Ω		1050		MHz
	G = +2, V_O = 2 V p-p		590		MHz
	G = +10, V_O = 0.2 V p-p		290		MHz
	G = +5, V_O = 2 V p-p		310		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p		83		MHz
Slew Rate	G = +2, V_O = 2 V step, R_L = 150 Ω		2860		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		12		ns
Overload Recovery Input/Output			40/60		ns
NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic @ 5 MHz	G = +1, V_O = 2 V p-p		75/78		dBc
Second/Third Harmonic @ 20 MHz	G = +1, V_O = 2 V p-p		66/61		dBc
Input Voltage Noise	f = 1 MHz		1.8		nV/√Hz
Input Current Noise (I^-/I^+)	f = 1 MHz		36/3		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.04		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.01		Degree
DC PERFORMANCE					
Input Offset Voltage		−6.5	+2.7	+11	mV
	$T_{MIN} - T_{MAX}$		2.06		mV
Input Offset Voltage Drift			14.2		µV/°C
Input Bias Current ($+I_B/-I_B$)		−21/−50	−7.7/−2.3	+5/+48	µA
	$T_{MIN} - T_{MAX}$ ($+I_B/-I_B$)		−4/−27.8		µA
Input Offset Current			±5.4		µA
Transimpedance		300	530	1500	kΩ
INPUT CHARACTERISTICS					
Noninverting Input Impedance			1.6/3		MΩ/pF
Input Common-Mode Voltage Range			1.3 to 3.7		V
Common-Mode Rejection Ratio		−50	−48	−45	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	±1.52	±1.57	±1.62	V
Linear Output Current	V_O = 2 V p-p, second harmonic < −50 dBc		70		mA
Capacitive Load Drive	45% over shoot		27		pF
POWER DOWN PINS					
Power-Down Input Voltage	Power down		$<V_S - 2.5$		V
	Enable		$>V_S - 2.5$		V
Turn-Off Time	50% of power-down voltage to 10% of V_{OUT} final, V_{IN} = 0.5 V p-p		125		ns
Turn-On Time	50% of power-down voltage to 90% of V_{OUT} final, V_{IN} = 0.5 V p-p		80		ns
Input Current					
Enabled			0.1		µA
Power-Down		−160	−43	+80	µA
POWER SUPPLY					
Operating Range		4.5		10	V
Quiescent Current per Amplifier	Enabled	6.3	7.9	9.4	mA
Quiescent Current per Amplifier	Power down	0.8	0.9	1.1	mA
Power Supply Rejection Ratio (+PSRR/−PSRR)		−59/−56	−57/−53	−55/−50	dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_S - 0.7$ V to $+V_S + 0.7$ V
Differential Input Voltage	$\pm V_S$
Exposed Paddle Voltage	$-V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
24-Lead LFCSP_WQ	70	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the AD8003 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8003. Exceeding a junction temperature of 175°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the AD8003 drive at the output. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S).

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes reduce θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the exposed paddle, 4 mm × 4 mm LFCSP_WQ (70°C/W) package on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

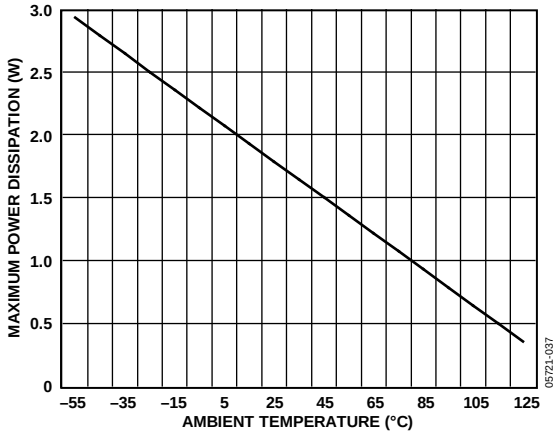


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

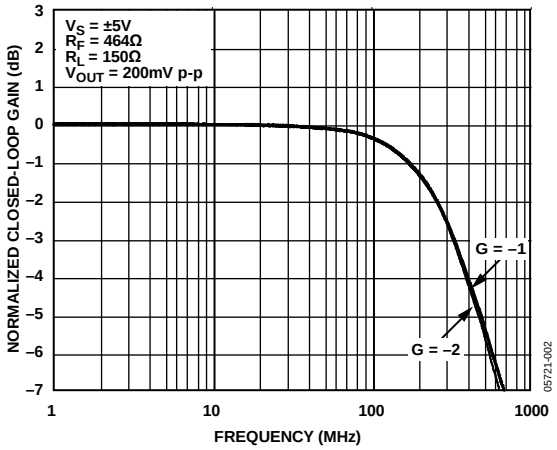


Figure 4. Small Signal Frequency Response for Various Gains

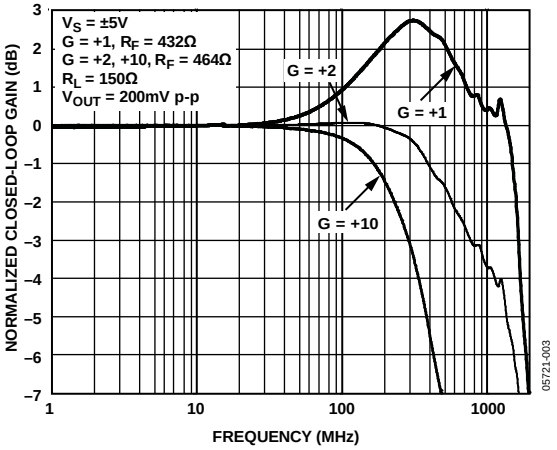


Figure 7. Small Signal Frequency Response for Various Gains

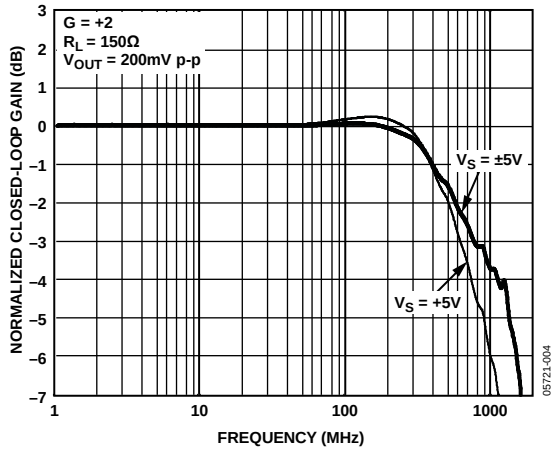


Figure 5. Small Signal Frequency Response for Various Supplies

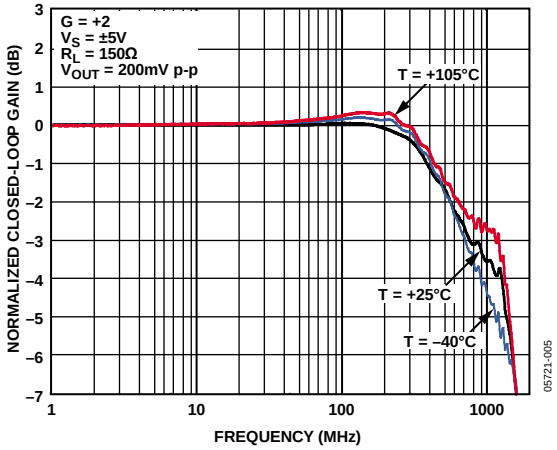


Figure 8. Small Signal Frequency Response for Various Temperatures

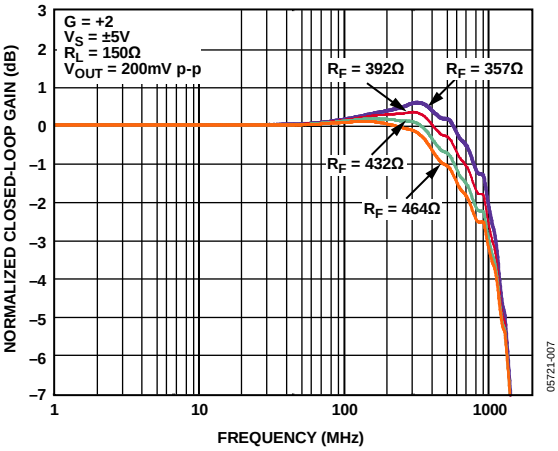


Figure 6. Small Signal Feedback Resistor (R_F) Optimization

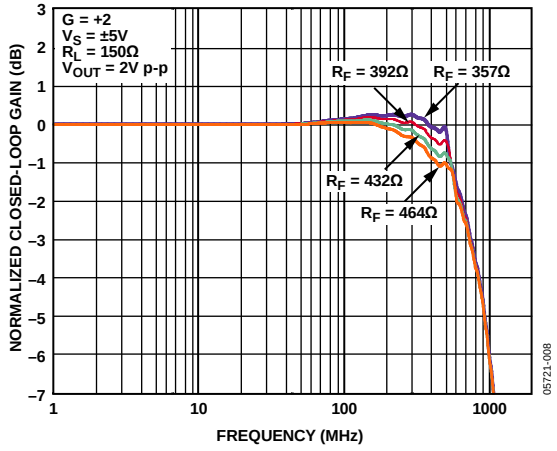


Figure 9. Large Signal Feedback Resistor (R_F) Optimization

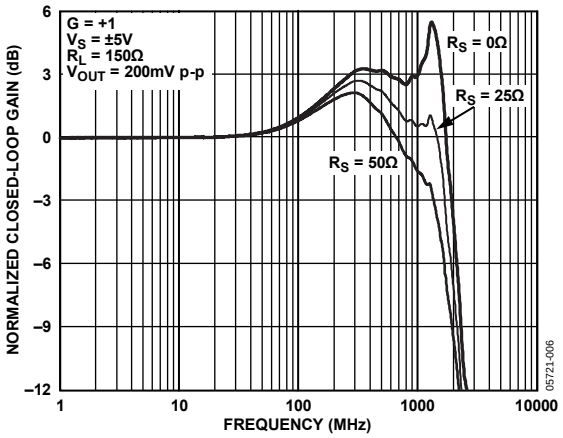


Figure 10. G = +1 Series Resistor (R_S) Optimization

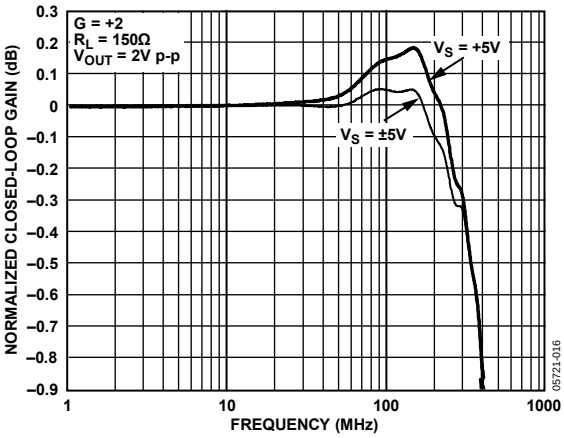


Figure 13. 0.1 dB Flatness Response

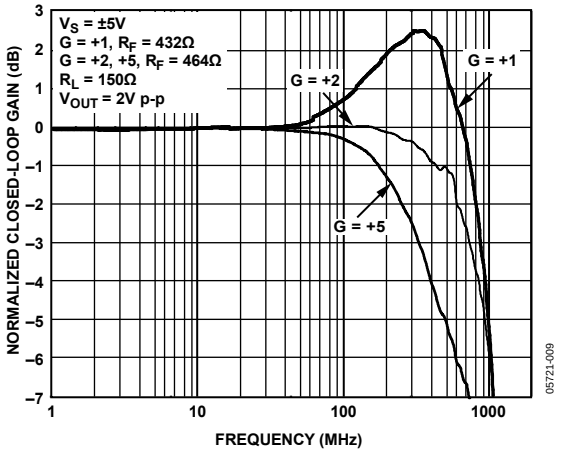


Figure 11. Large Signal Frequency Response for Various Gains

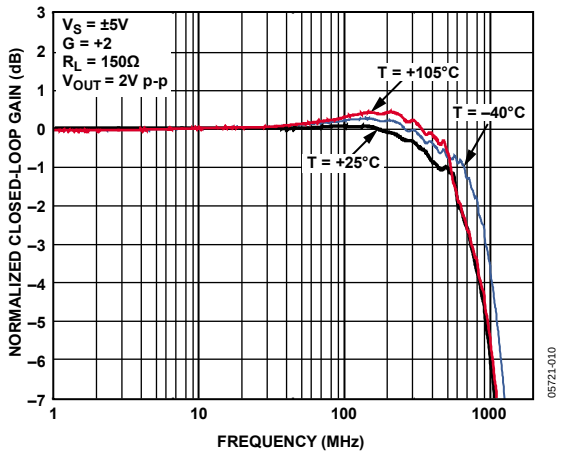


Figure 14. Large Signal Frequency Response for Various Temperatures

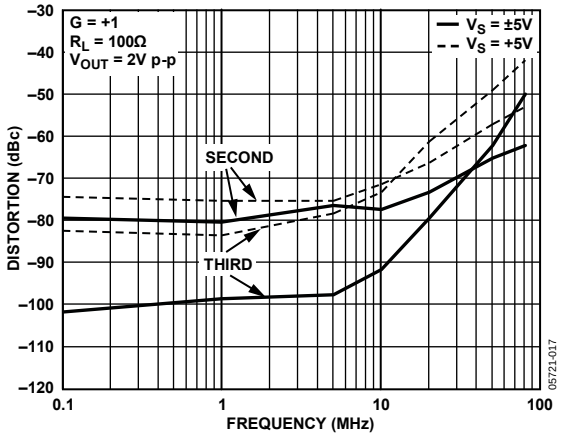


Figure 12. Harmonic Distortion vs. Frequency for Various Supplies

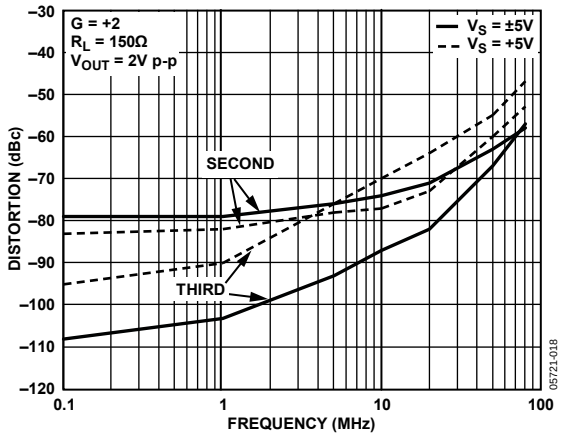


Figure 15. Harmonic Distortion vs. Frequency for Various Supplies

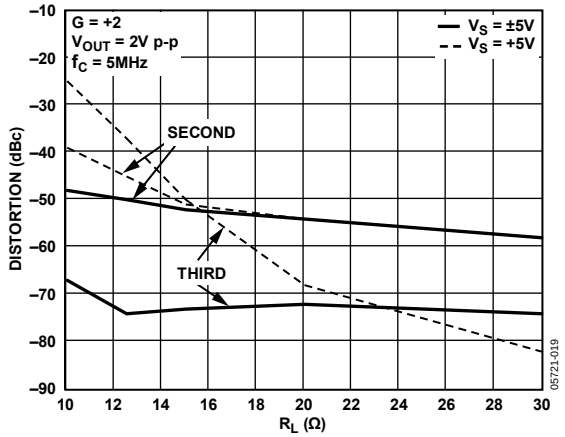


Figure 16. Harmonic Distortion vs. R_L

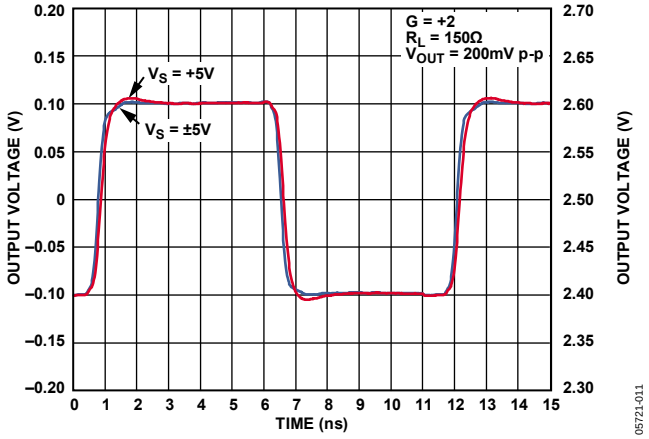


Figure 19. Small Signal Pulse Response for Various Supplies

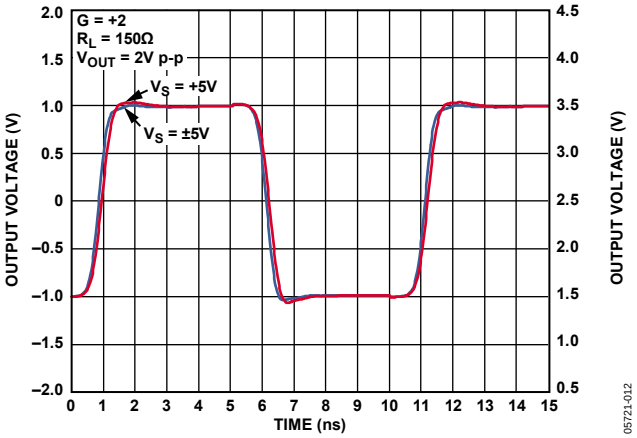


Figure 17. Large Signal Pulse Response for Various Supplies

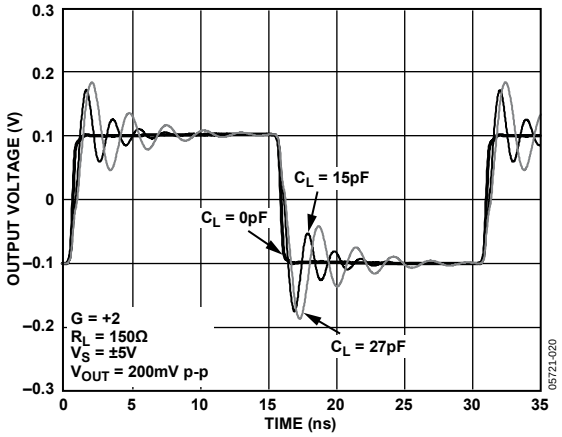


Figure 20. Small Signal Pulse Response for Various Capacitive Loads

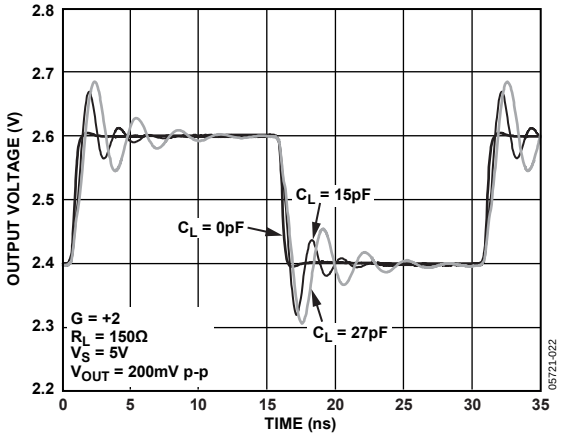


Figure 18. Small Signal Pulse Response for Various Capacitive Loads

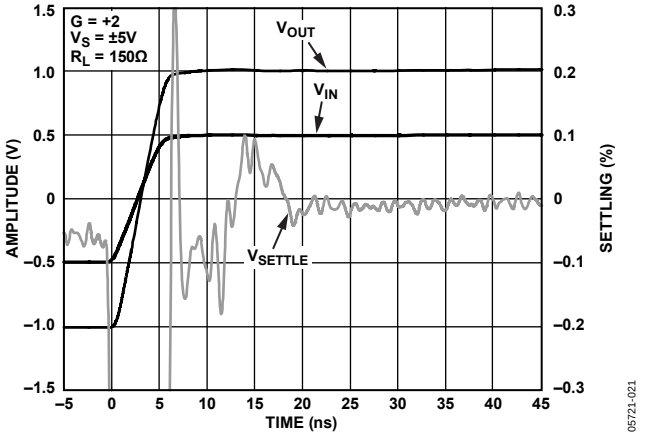


Figure 21. Short-Term 0.1% Settling Time

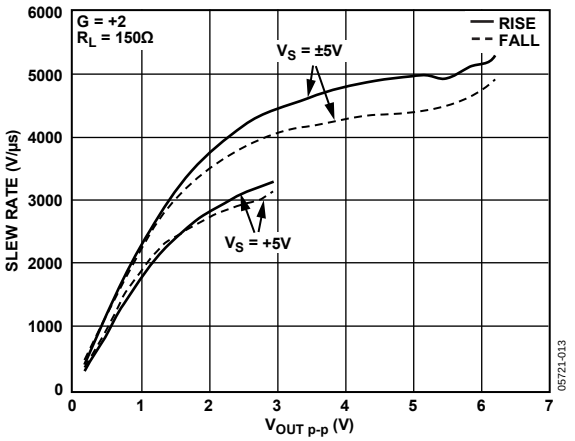


Figure 22. Slew Rate vs. Output Voltage

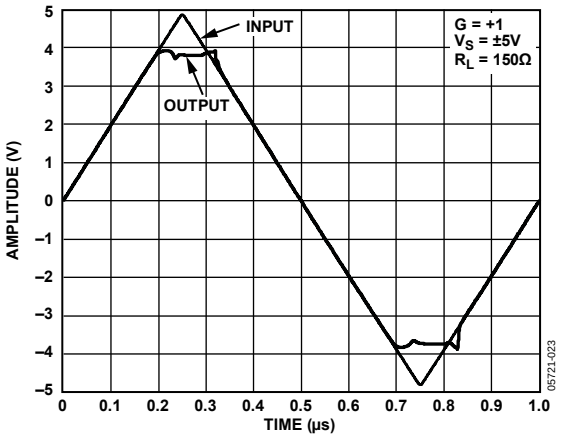


Figure 25. Input Overdrive Recovery

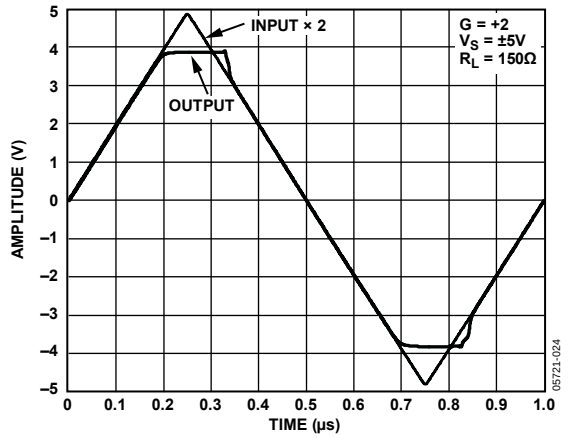


Figure 23. Output Overdrive Recovery

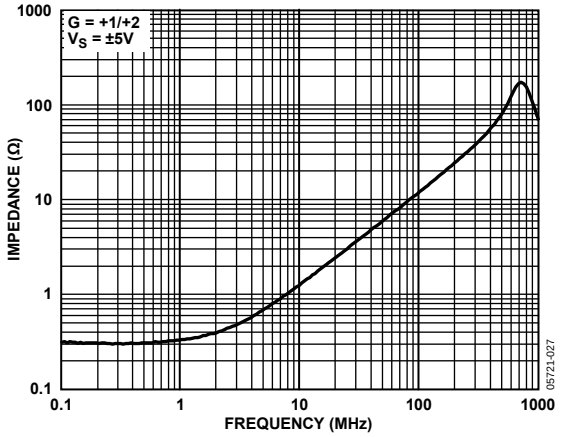


Figure 26. Output Impedance vs. Frequency

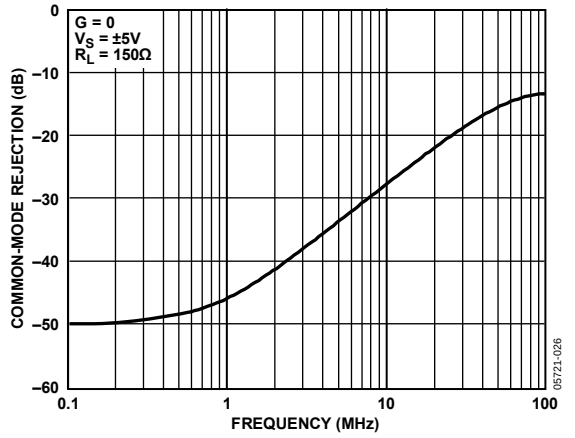


Figure 24. Common-Mode Rejection vs. Frequency

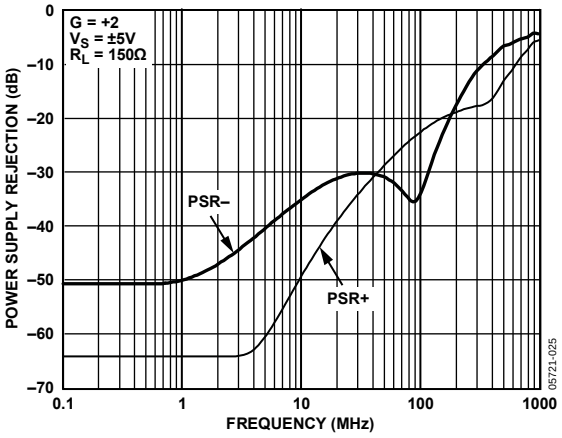


Figure 27. Power Supply Rejection vs. Frequency

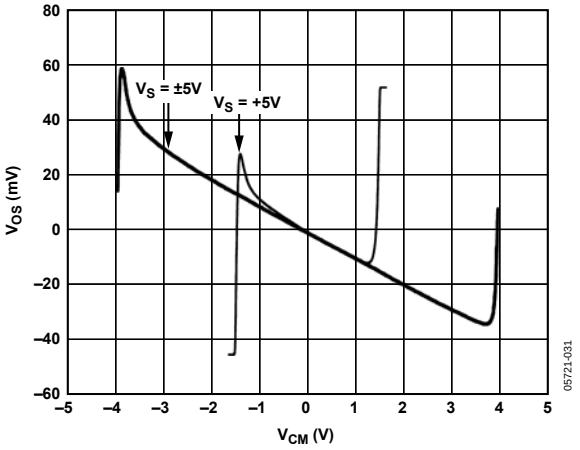


Figure 28. Offset Voltage vs. Input Common-Mode Range

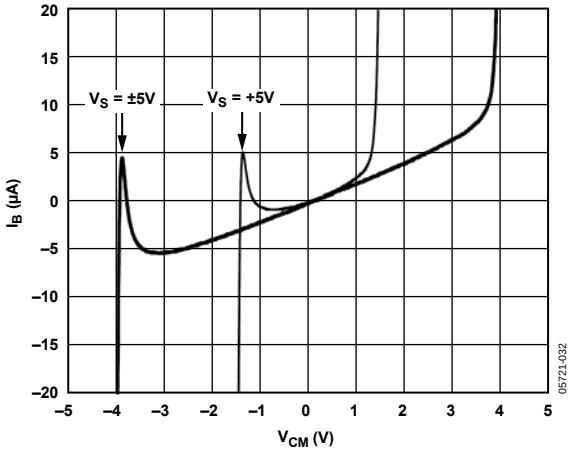


Figure 31. Noninverting Input Bias Current vs. Common-Mode Range

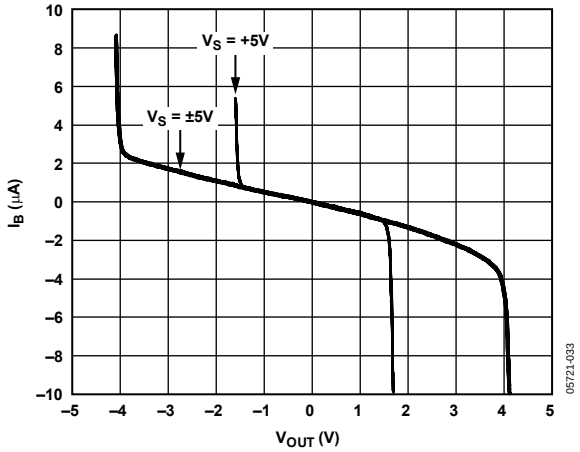


Figure 29. Inverting Input Bias Current Linearity

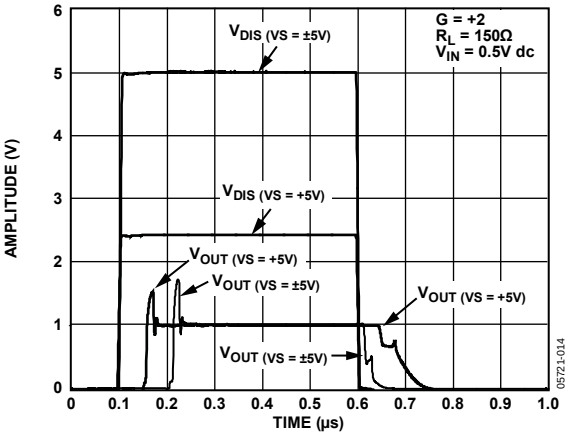


Figure 32. Disable Switching Time for Various Supplies

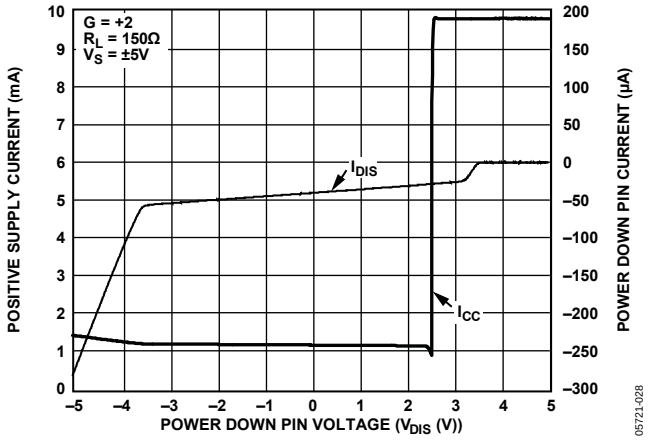


Figure 30. POWER DOWN Pin Current and Supply Current vs. POWER DOWN Pin Voltage

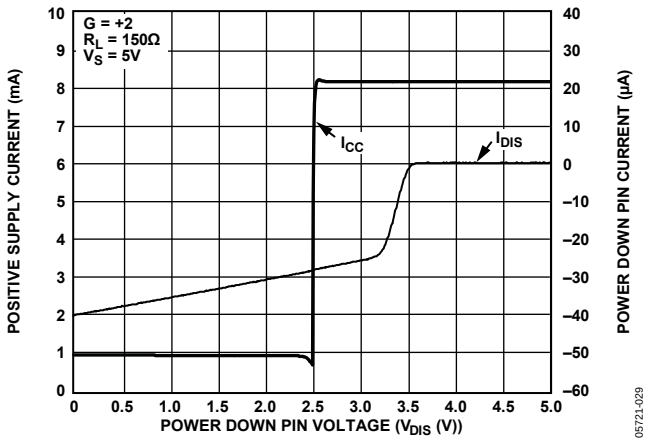


Figure 33. POWER DOWN Pin Current and Supply Current vs. POWER DOWN Pin Voltage

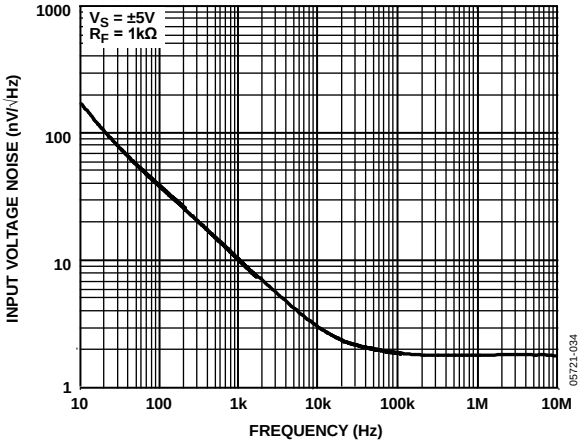


Figure 34. Input Voltage Noise vs. Frequency

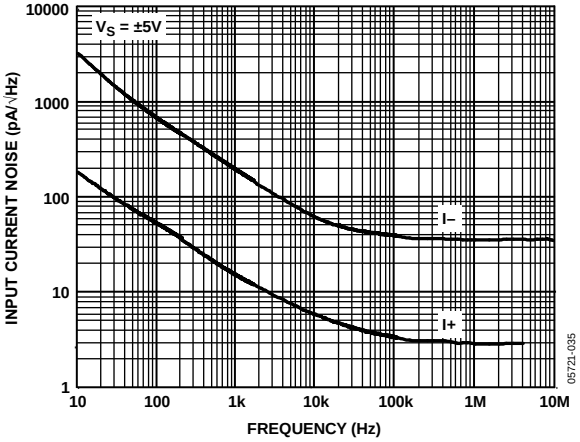


Figure 36. Input Current Noise vs. Frequency

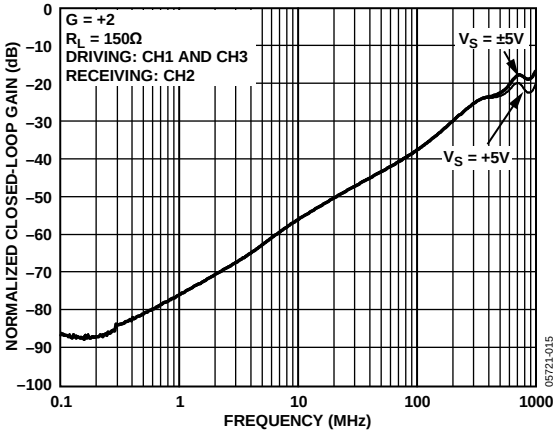


Figure 35. Worst-Case Crosstalk

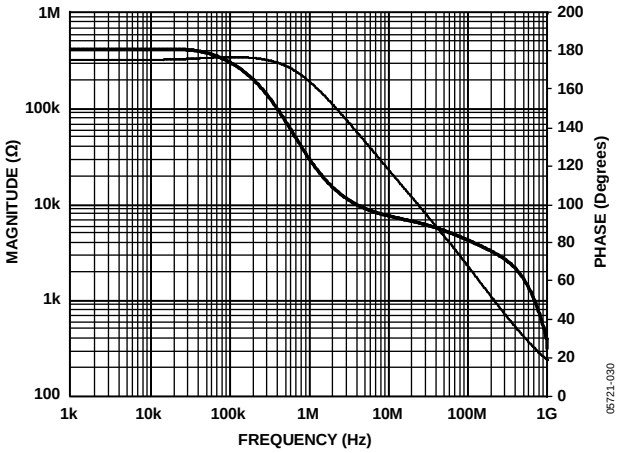


Figure 37. Transimpedance

APPLICATIONS INFORMATION

GAIN CONFIGURATIONS

Unlike conventional voltage feedback amplifiers, the feedback resistor has a direct impact on the closed-loop bandwidth and stability of the current feedback op amp circuit. Reducing the resistance below the recommended value can make the amplifier response peak and can even become unstable. Increasing the size of the feedback resistor reduces the closed-loop bandwidth.

Table 5 provides a convenient reference for quickly determining the feedback and gain set resistor values, and the small and large signal bandwidths for common gain configurations. The feedback resistors in Table 5 have been optimized for 0.1 dB flatness frequency response.

Table 5. Recommended Values and Frequency Response[1]

Gain	R_F (Ω)	R_G (Ω)	R_S (Ω)	−3 dB SS BW (MHz)	Large Signal −3 dB BW	Large Signal 0.1 dB BW
−1	300	300	0	734	668	--
+1	432	N/A	24.9	1650	822	--
+2	464	464	0	761	730	190
+5	300	75	0	567	558	165
+10	300	33.2	0	446	422	170

[1]Conditions: V_S = ±5 V, T_A = 25°C, R_L = 150 Ω.

Figure 38 and Figure 39 show the typical noninverting and inverting configurations and recommended bypass capacitor values.

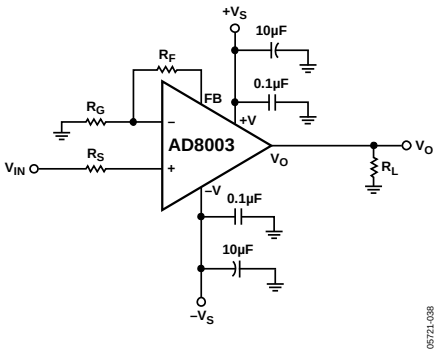


Figure 38. Noninverting Gain

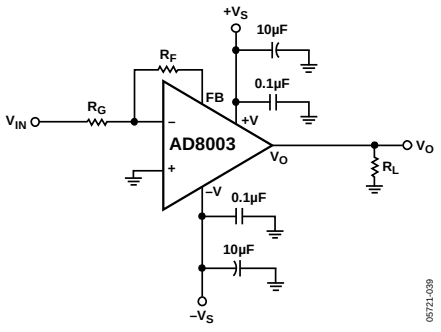


Figure 39. Inverting Gain

RGB VIDEO DRIVER

Figure 40 shows a typical RGB driver application using bipolar supplies. The gain of the amplifier is set at +2, where $R_F = R_G$ = 464 Ω. The amplifier inputs are terminated with shunt 75 Ω resistors, and the outputs have series 75 Ω resistors for proper video matching. In Figure 40, the POWER DOWN pins are not shown connected to any signal source for simplicity. If the power-down function is not used, it is recommended that the POWER DOWN pins be tied to the positive supply and not be left floating (not connected).

In applications that require a fixed gain of +2, as previously mentioned, the designer may consider the ADA4862-3. The ADA4862-3 is another high performance triple current feedback amplifier. The ADA4862-3 has integrated feedback and gain set resistors that reduce board area and simplify designs.

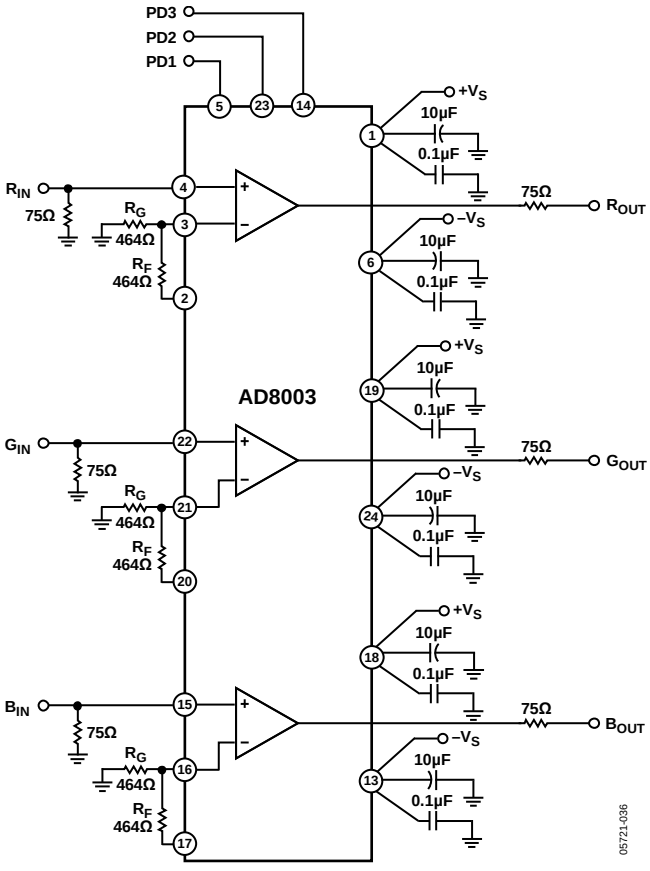


Figure 40. RGB Video Driver

PRINTED CIRCUIT BOARD LAYOUT

Printed circuit board (PCB) layout is usually one of the last steps in the design process and often proves to be one of the most critical. A high performance design can be rendered mediocre due to poor or sloppy layout. Because the AD8003 can operate into the RF frequency spectrum, high frequency board layout considerations must be taken into account. The PCB layout, signal routing, power supply bypassing, and grounding must all be addressed to ensure optimal performance.

LOW DISTORTION PINOUT

The AD8003 LFCSP features ADI's low distortion pinout. The pinout lowers the second harmonic distortion and simplifies the circuit layout. The close proximity of the noninverting input and the negative supply pin creates a source of second harmonic distortion. Physical separation of the noninverting input pin and the negative power supply pin reduces this distortion.

By providing an additional output pin, the feedback resistor can be connected directly between the feedback pin and the inverting input. This greatly simplifies the routing of the feedback resistor and allows a more compact circuit layout, which reduces its size and helps to minimize parasitics and increase stability.

SIGNAL ROUTING

To minimize parasitic inductances, ground planes should be used under high frequency signal traces. However, the ground plane should be removed from under the input and output pins to minimize the formation of parasitic capacitors, which degrades phase margin. Signals that are susceptible to noise pickup should be run on the internal layers of the PCB, which can provide maximum shielding.

EXPOSED PADDLE

The AD8003 features an exposed paddle, which lowers the thermal resistance by approximately 40% compared to a standard SOIC plastic package. The paddle can be soldered directly to the ground plane of the board. Thermal vias or heat pipes can also be incorporated into the design of the mounting pad for the exposed paddle. These additional vias improve the thermal transfer from the package to the PCB. Using a heavier weight copper also reduces the overall thermal resistance path to ground.

POWER SUPPLY BYPASSING

Power supply bypassing is a critical aspect of the PCB design process. For best performance, the AD8003 power supply pins need to be properly bypassed.

Each amplifier has its own supply pins brought out for the utmost flexibility. Supply pins can be commoned together or routed to a dedicated power plane. Commoned supply connections can also reduce the need for bypass capacitors on each supply line. The exact number and values of the bypass capacitors are dictated by the design specifications of the actual circuit.

A parallel combination of different value capacitors from each of the power supply pins to ground tends to work the best. Paralleling different values and sizes of capacitors helps to ensure that the power supply pins see a low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier. Starting directly at the power supply pins, the smallest value and physical-sized component should be placed on the same side of the board as the amplifier, and as close as possible to the amplifier, and connected to the ground plane. This process should be repeated for the next largest capacitor value. It is recommended that a 0.1 µF ceramic 0508 case be used for the AD8003. The 0508 offers low series inductance and excellent high frequency performance. The 0.1 µF case provides low impedance at high frequencies. A 10 µF electrolytic capacitor should be placed in parallel with the 0.1 µF. The 10 µF capacitor provides low ac impedance at low frequencies. Smaller values of electrolytic capacitors can be used depending on the circuit requirements. Additional smaller value capacitors help provide a low impedance path for unwanted noise out to higher frequencies but are not always necessary.

Placement of the capacitor returns (grounds), where the capacitors enter into the ground plane, is also important. Returning the capacitor grounds close to the amplifier load is critical for distortion performance. Keeping the capacitors distance short, but equal from the load, is optimal for performance.

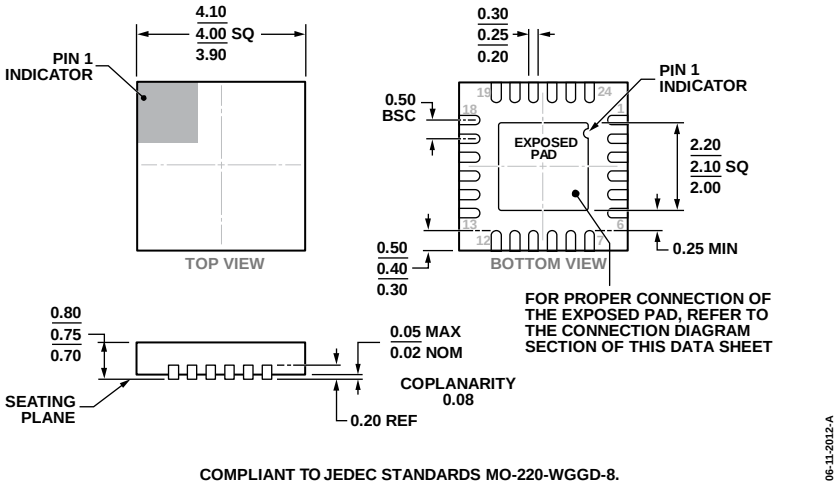
In some cases, bypassing between the two supplies can help improve PSRR and maintain distortion performance in crowded or difficult layouts. Designers should note this as another option for improving performance.

Minimizing the trace length and widening the trace from the capacitors to the amplifier reduces the trace inductance. A series inductance with the parallel capacitance can form a tank circuit, which can introduce high frequency ringing at the output. This additional inductance can also contribute to increased distortion due to high frequency compression at the output. The use of vias should be minimized in the direct path to the amplifier power supply pins because vias can introduce parasitic inductance, which can lead to instability. When required, use multiple large diameter vias because this lowers the equivalent parasitic inductance.

GROUNDING

The use of ground and power planes is encouraged as a method of proving low impedance returns for power supply and signal currents. Ground and power planes can also help to reduce stray trace inductance and provide a low thermal path for the amplifier. Ground and power planes should not be used under any of the pins of the AD8003. The mounting pads and the ground or power planes can form a parasitic capacitance at the amplifiers input. Stray capacitance on the inverting input and the feedback resistor form a pole, which degrades the phase margin, leading to instability. Excessive stray capacitance on the output also forms a pole, which degrades phase margin.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 41. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8003ACPZ-R2	–40°C to +85°C	24-Lead LFCSP_WQ	CP-24-10	250
AD8003ACPZ-REEL7	–40°C to +85°C	24-Lead LFCSP_WQ	CP-24-10	1,500
AD8003ACHIPS		Die		
AD8003ACPZ-EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

D05721-0-3/14(C)

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