200 mA Output Current High-Speed Amplifier

AD8010

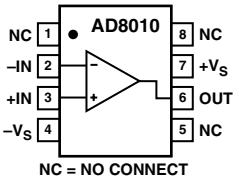
FEATURES
200 mA of Output Current
9 Ω Load
SFDR –54 dBc @ 1 MHz
Differential Gain Error 0.04%, f = 4.43 MHz
Differential Phase Error 0.06°, f = 4.43 MHz
Maintains Video Specifications Driving Eight Parallel 75 Ω Loads
- **0.02% Differential Gain**
- **0.03° Differential Phase**
- **0.1 dB Gain Flatness to 60 MHz**

THD –72 dBc @ 1 MHz, R_L = 18.75 Ω
IP3 42 dBm @ 5 MHz, R_L = 18.75 Ω
1 dB Gain Compression 21 dBm @ 5 MHz, R_L = 100 Ω
230 MHz –3 dB Bandwidth, G = +1, R_L = 18.75 Ω
800 V/μs Slew Rate, R_L = 18.75 Ω
25 ns Settling Time to 0.1%
Available in 8-Lead DIP, 16-Lead Wide Body SOIC and Thermally Enhanced 8-Lead SOIC

APPLICATIONS
Video Distribution Amplifier
VDSL, xDSL Line Driver
Communications
ATE
Instrumentation

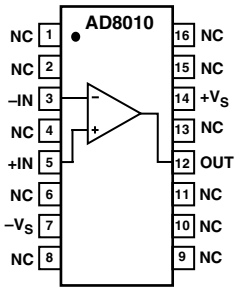
CONNECTION DIAGRAMS

8-Lead DIP and SOIC



NC = NO CONNECT

16-Lead Wide Body SOIC



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD8010 is a low power, high current amplifier capable of delivering a minimum load drive of 175 mA. Signal performance such as 0.02% and 0.03° differential gain and phase error is maintained while driving eight 75 Ω back terminated video lines. The current feedback amplifier features gain flatness to 60 MHz and –3 dB (G = +1) signal bandwidth of 230 MHz and only requires a typical of 15.5 mA supply current from ±5 V supplies. These features make the AD8010 an ideal component for Video Distribution Amplifiers or as the drive amplifier within high data rate Digital Subscriber Line (VDSL and xDSL) systems.

The AD8010 is an ideal component choice for any application that needs a driver that will maintain signal quality when driving low impedance loads.

The AD8010 is offered in three package options: an 8-lead DIP, 16-lead wide body SOIC and a low thermal resistance 8-lead SOIC, and operates over the industrial temperature range of –40°C to +85°C.

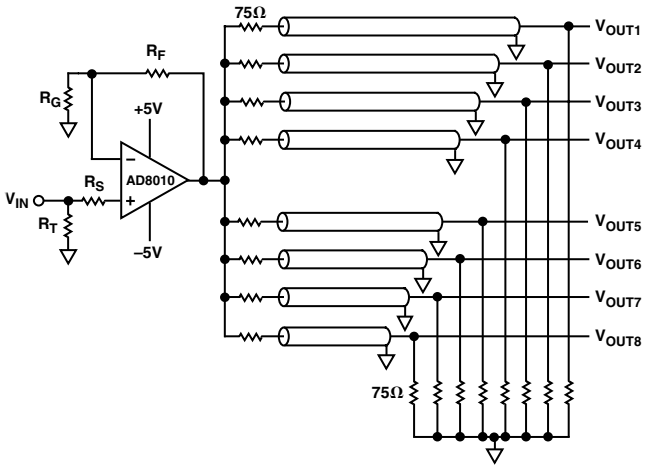


Figure 1. Video Distribution Amplifier

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD8010—SPECIFICATIONS (@ 25°C, V_S = ±5 V, G = +2, R_L = 18.75 Ω, R_{S+} = 150 Ω, R_F = R_G = 604 Ω (R-16), R_F = R_G = 562 Ω (N-8), R_F = R_G = 499 Ω (R-8). T_{MIN} = –40°C, T_{MAX} = +85°C unless otherwise noted)

Model	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_{OUT} = 0.2 V p-p	180	230		MHz
	G = +2, V_{OUT} = 0.2 V p-p	130	190		MHz
0.1 dB Bandwidth	V_{OUT} = 0.2 V p-p	30	60		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p		90		MHz
Peaking	V_{OUT} = 0.2 V p-p, < 5 MHz		0.02		dB
Slew	V_{OUT} = 2 V p-p		800		V/µs
Rise and Fall Time	V_{OUT} = 2 V p-p		2.0		ns
Settling Time	0.1%, V_{OUT} = 2 V p-p		25		ns
NOISE/HARMONIC PERFORMANCE					
Distortion	V_{OUT} = 2 V p-p				
2nd Harmonic	1 MHz		–73		dBc
	5 MHz		–58		dBc
	10 MHz		–53		dBc
	10 MHz, R_L = 39 Ω		–67		dBc
	20 MHz		–44		dBc
3rd Harmonic	1 MHz		–77		dBc
	5 MHz		–63		dBc
	10 MHz		–57		dBc
	10 MHz, R_L = 39 Ω		–63		dBc
	20 MHz		–50		dBc
IMD	5 MHz Δf = 10 kHz		–73		dBc
IP3	5 MHz		42		dBm
1 dB Gain Compression	5 MHz		21		dBm
Input Noise Voltage	f = 10 kHz		2		$nV\sqrt{Hz}$
Input Noise Current	f = 10 kHz, +In		3		$pA\sqrt{Hz}$
	f = 20 kHz, –In		20		$pA\sqrt{Hz}$
Differential Gain	f = 4.43 MHz, R_L = 150 Ω		0.02		%
	f = 4.43 MHz, R_L = 18.75 Ω		0.02		%
Differential Phase	f = 4.43 MHz, R_L = 150 Ω		0.02		Degrees
	f = 4.43 MHz, R_L =18.75 Ω		0.03		Degrees
DC PERFORMANCE					
Input Offset Voltage			5	12	mV
	T_{MIN}–T_{MAX}			15	mV
Offset Drift			10		µV/°C
Input Bias Current (–)			10	135	µA
	T_{MIN}–T_{MAX}			200	µA
Input Bias Current (+)			6	12	µA
	T_{MIN}–T_{MAX}			20	µA
INPUT CHARACTERISTICS					
Input Resistance	+Input		125		kΩ
	–Input		12.5		Ω
Input Capacitance			2.75		pF
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	50	54		dB
Input Common-Mode Voltage Range			±2.5		V
Open Loop Transresistance	V_{OUT} = ±2.5 V	300	500		kΩ
	T_{MIN}–T_{MAX}	250			kΩ
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
R_L = 18.75 Ω		±2.1	±2.5		V
R_L = 150 Ω		±2.7	±3.0		V
Output Current	R_L = 9 Ω	175	200		mA
Short-Circuit Current			240		mA
Capacitive Load Drive			40		pF
POWER SUPPLY					
Operating Range		±4.5		±6.0	V
Quiescent Current			15.5	17	mA
	T_{MIN} to T_{MAX}			20	mA
Power Supply Rejection Ratio	$+V_S$ = +4 V to +6 V, $–V_S$ = +5 V	60	66		dB
	$+V_S$ = +5 V, $–V_S$ = –4 V to –6 V	50	56		dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
Plastic Package (N) . . . . . Observe Power Derating Curves
Small Outline Package (R) . Observe Power Derating Curves
Wide Body SOIC (R-16) . . . Observe Power Derating Curves
Input Voltage (Common-Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±1.2 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range N, R . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead Plastic Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 122°C/W
16-Lead SOIC Package: θ_{JA} = 73°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8010 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8010 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

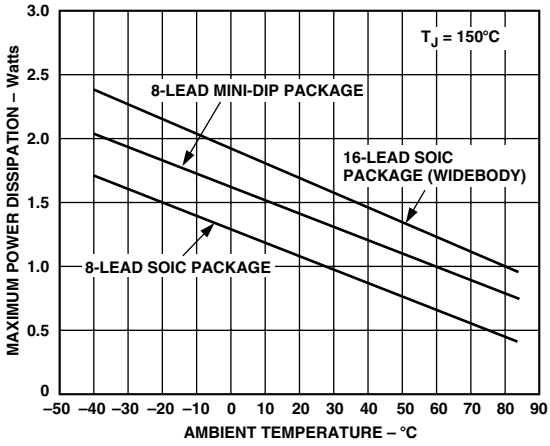


Figure 2. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD8010AN	–40°C to +85°C	8-Lead Plastic DIP	N-8
AD8010AR	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD8010AR-16	–40°C to +85°C	16-Lead Wide Body SOIC	R-16
AD8010AR-REEL		REEL SOIC	13" REEL
AD8010AR-REEL7		REEL SOIC	7" REEL
AD8010AR-16-REEL		REEL SOIC	13" REEL
AD8010AR-16-REEL7		REEL SOIC	7" REEL

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8010 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD8010–Typical Performance Characteristics

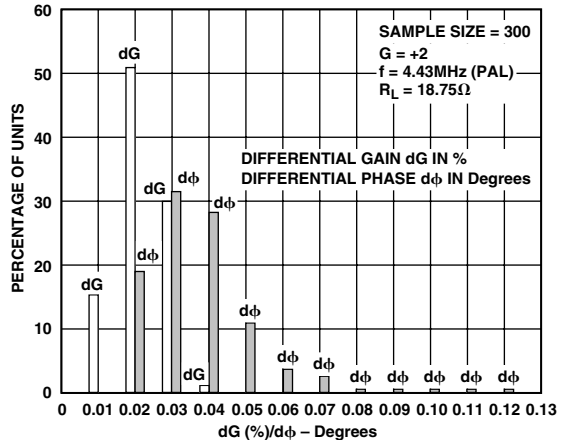


Figure 3. Distribution of Differential Gain (dG) and Differential Phase (dϕ); R_L = 18.75 Ω

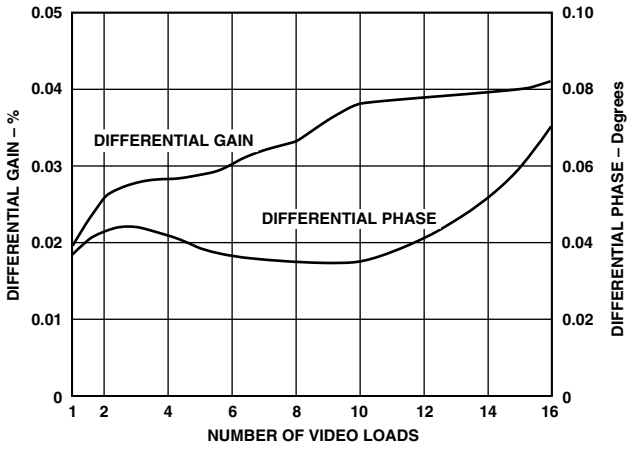


Figure 6. Differential Gain and Phase vs. Number of Video Loads Over Temperature (–40°C to +85°C); f = 4.43 MHz

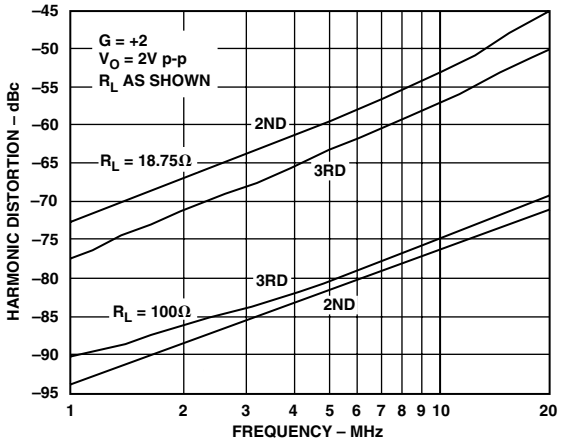


Figure 4. Harmonic Distortion vs. Frequency; G = +2

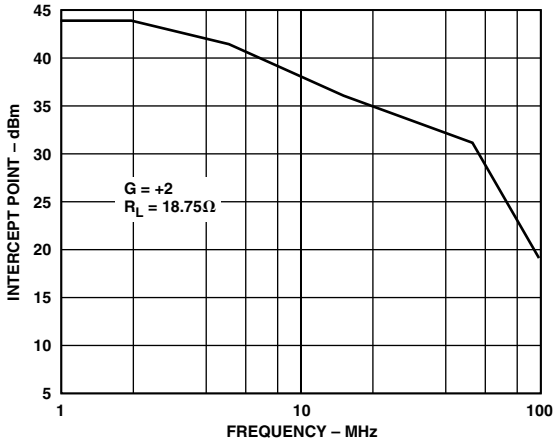


Figure 7. Two-Tone, 3rd Order IMD Intercept vs. Frequency; G = +2, R_L = 18.75 Ω

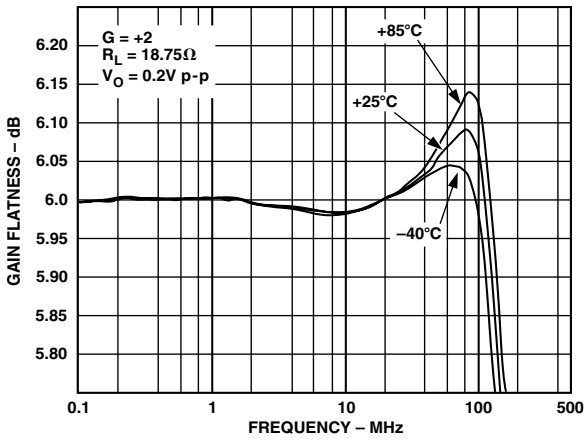


Figure 5. Gain Flatness vs. Frequency Over Temperature (–40°C to +85°C)

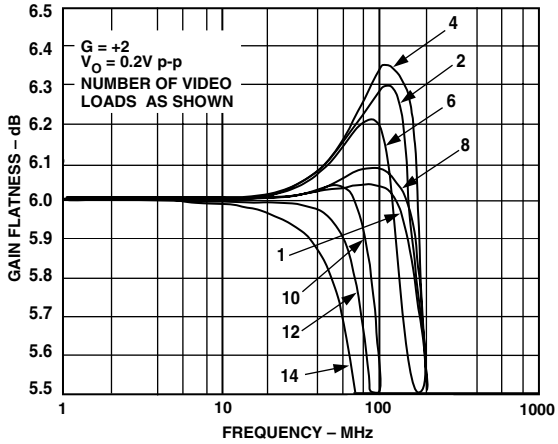


Figure 8. Gain Flatness vs. Frequency vs. Number of Video Loads

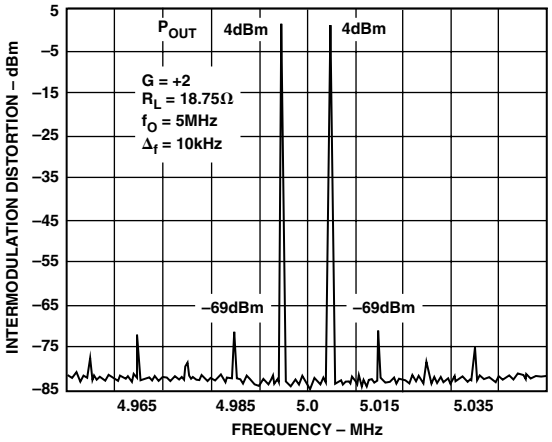


Figure 9. Intermodulation Distortion

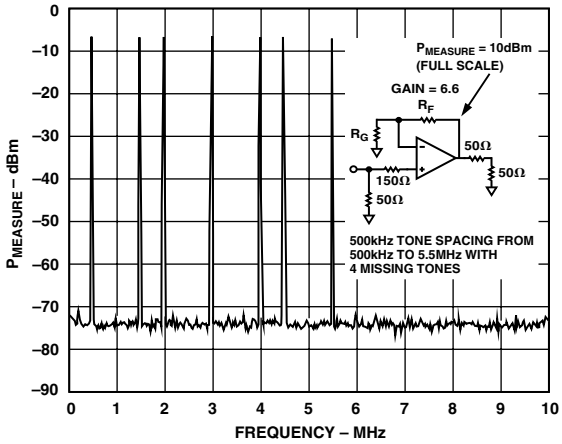


Figure 12. Multitone Distortion; R_L = 100 Ω

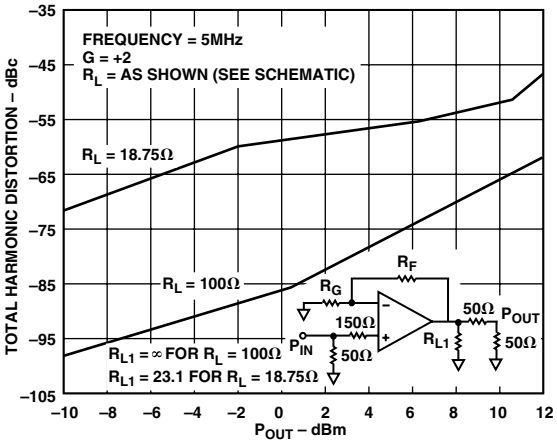


Figure 10. Total Harmonic Distortion vs. P_{OUT}; G = +2

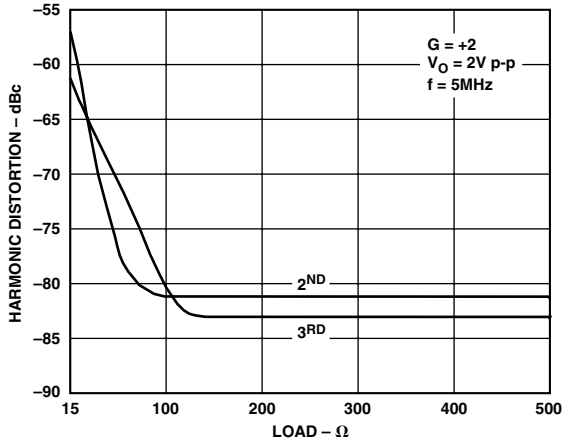


Figure 13. Harmonic Distortion vs. Load

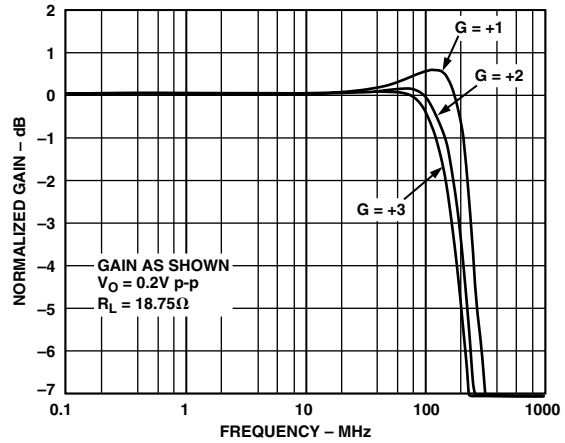


Figure 11. Small Signal Closed-Loop Frequency Response; R_L = 18.75 Ω

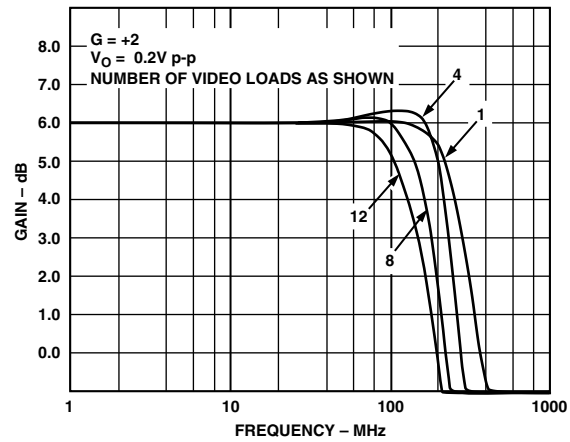


Figure 14. Closed-Loop Frequency Response vs. Number of Video Loads

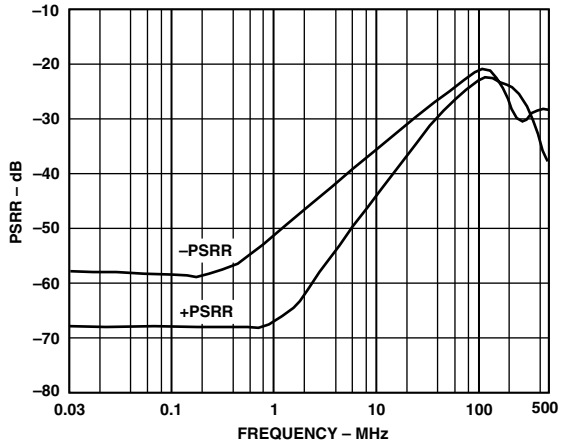


Figure 15. PSRR vs. Frequency

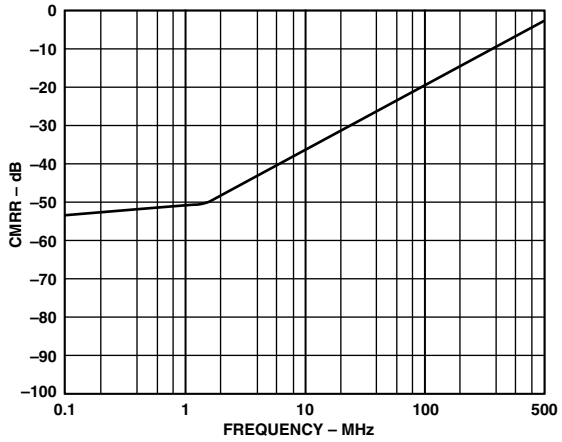


Figure 18. CMRR vs. Frequency

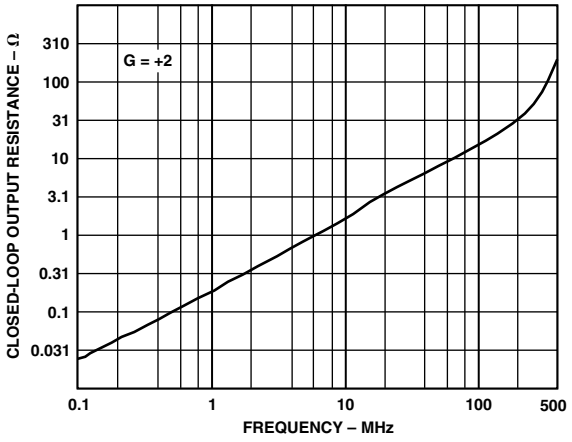


Figure 16. Closed-Loop Output Resistance vs. Frequency

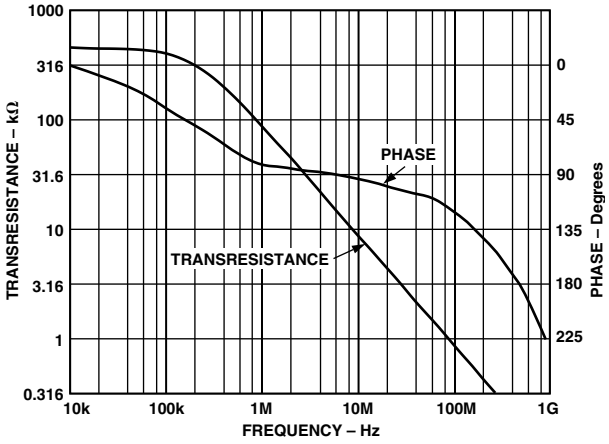


Figure 19. Transresistance and Phase vs. Frequency; R_L = 18.75 Ω

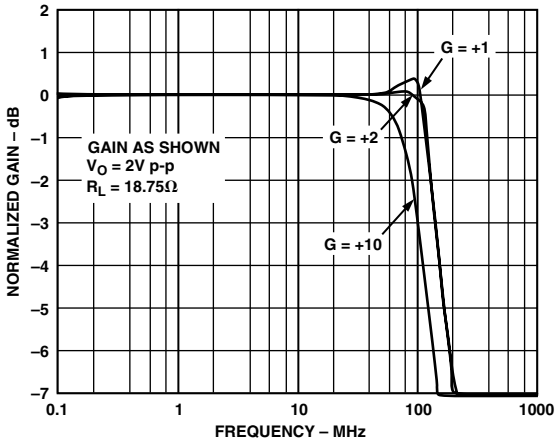


Figure 17. Large Signal Frequency Response; V_O = 2 V p-p

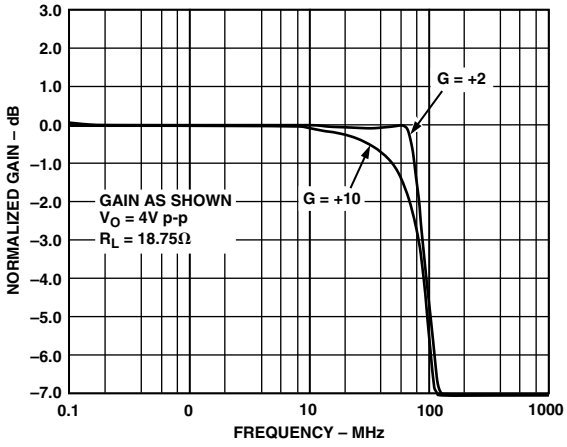


Figure 20. Large Signal Frequency Response; V_O = 4 V p-p

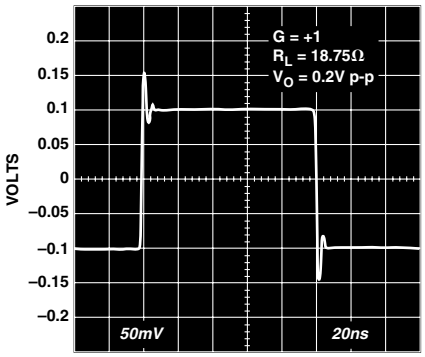


Figure 21. Small-Signal Pulse Response; G = +1

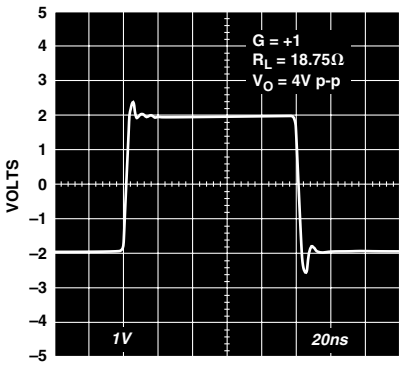


Figure 24. Large-Signal Pulse Response; G = +1

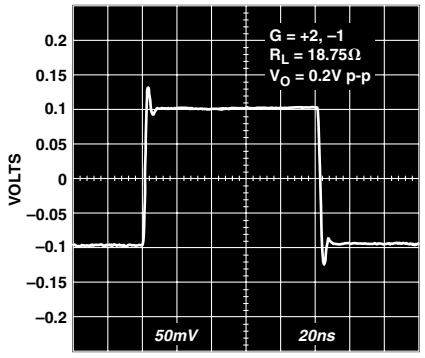


Figure 22. Small-Signal Pulse Response; G = +2, –1

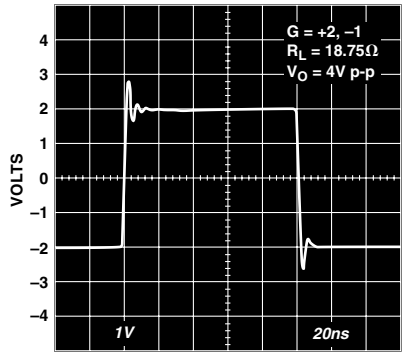


Figure 25. Large-Signal Pulse Response; G = +2, –1

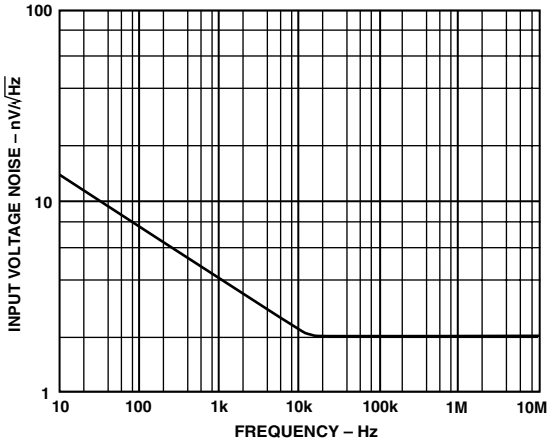


Figure 23. Input Voltage Noise vs. Frequency

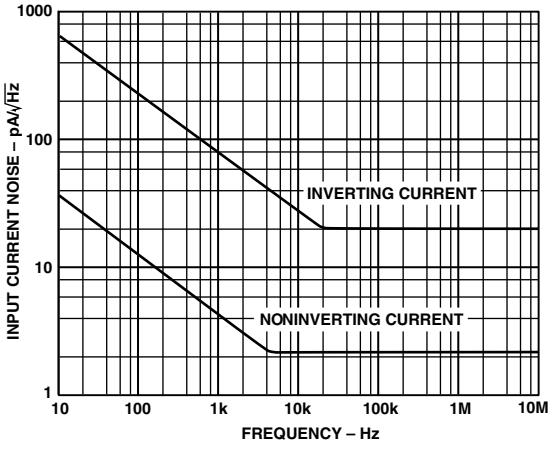


Figure 26. Input Current Noise vs. Frequency

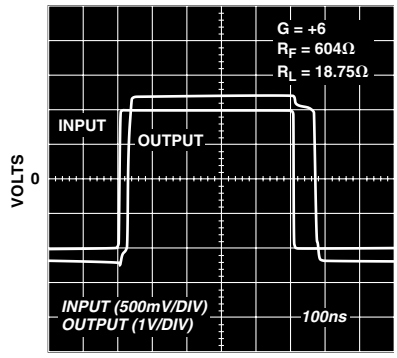


Figure 27. Overdrive Recovery; G = +6

OVERDRIVE RECOVERY

Overdrive of an amplifier occurs when the output and/or input range are exceeded. The amplifier must recover from this overdrive condition. As shown in Figure 27, the AD8010 recovers within 35 ns from negative overdrive and within 75 ns from positive overdrive.

THEORY OF OPERATION

The AD8010 is a current feedback amplifier optimized for high current output while maintaining excellent performance with respect to flatness, distortion and differential gain/phase. As a video distribution amplifier, the AD8010 will drive up to 12 parallel video loads (12.5 Ω) from a single output with 0.04% differential gain and 0.04° differential phase errors. This means that, unlike designs with one driver per output, any output is a true reflection of the signal on all other outputs.

The high output current capability of the AD8010 also make it useful in xDSL applications. The AD8010 can drive a 12.5 Ω single-ended or 25 Ω differential load with low harmonic distortion. This makes it useful in designs that utilize a step-up transformer to drive a twisted-pair transmission line.

To achieve these levels of performance special precautions with respect to supply bypassing are recommended (Figure 29). This configuration minimizes the contribution from high frequency supply rejection to differential gain and phase errors as well as reducing distortion due to harmonic energy in the power supplies.

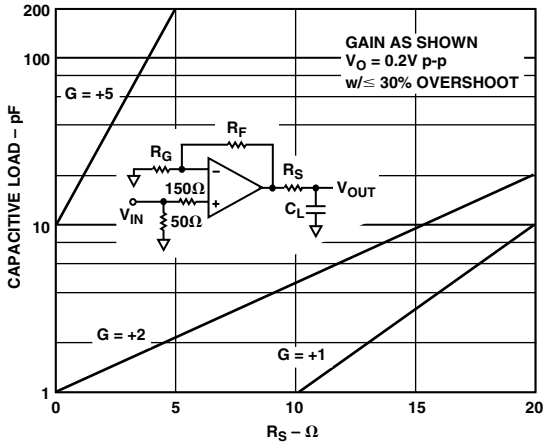


Figure 28. Capacitive Load Drive vs. Series Resistor for Various Gains

Driving Capacitance Loads

The AD8010 was designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, best frequency response is obtained by the addition of a small series resistance as shown in Figure 28. The inset figure shows the optimum value for R_{SERIES} vs. capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

LAYOUT CONSIDERATIONS

The specified high speed performance of the AD8010 requires careful attention to board layout and component selection. Proper R_F design techniques and low-pass parasitic component selection are necessary.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide low impedance path. The ground plane should be removed from the area near the input pins to reduce the parasitic capacitance.

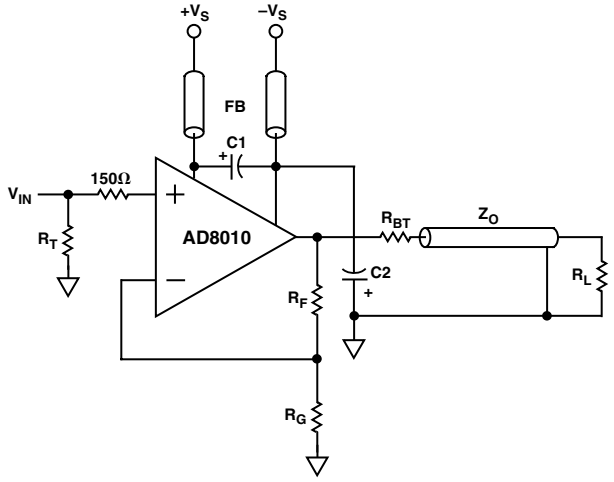


Figure 29. Standard Noninverting Closed-Loop Configuration with Recommended Bypassing Technique

The standard noninverting closed-loop configuration with the recommended power supply bypassing technique is shown in Figure 29. Ferrite beads (Amidon Associates, Torrance CA, Part Number 43101) are used to suppress high frequency power supply energy on the DUT supply lines at the DUT. C1 and C2 each represent the parallel combination of a 47 µF (16 V) tantalum electrolytic capacitor, a 10 µF (10 V) tantalum electrolytic capacitor and a 0.1 µF ceramic chip capacitor. Connect C1 from the $+V_S$ pin to the $–V_S$ pin. Connect C2 from the $–V_S$ pin to signal ground.

The feedback resistor should be located close to the inverting input pin in order to keep the parasitic capacitance at this node to a minimum. Parasitic capacitances of less than 1 pF at the inverting input can significantly affect high speed performance.

Stripline design techniques should be used for long traces (greater than about 3 cm). These should be designed with a characteristic impedance (Z_O) of 50 Ω or 75 Ω and be properly terminated at each end.

APPLICATIONS

Video Distribution Amplifier

The AD8010 is optimized for the specific function of providing excellent video performance when driving multiple video loads in parallel. Significant power is saved and heat sinking is greatly simplified because of the ability of the AD8010 to obtain this performance when running on a ±5 V supply. However, due to the high currents that flow when driving many parallel video loads, special layout and bypassing techniques are required to assure optimal performance.

When designing a video distribution amplifier with the AD8010, it is very important to keep in mind where the high (ac) currents will flow. These paths include the power supply pins of the chip along with the bypass capacitors and the return path for these capacitors, the output circuits and the return path of the output current from the loads.

In general, any loops that are formed by any of the above paths should be made as small as possible. Large loops are both generators and receivers of magnetic fields and can cause undesired coupling of signals that lowers the performance of the amplifier. Effects that have not been seen before in other op amp circuits might arise because of the high currents. Most op amp circuits output, at most, tens of milliamps and do not require extremely tight video specifications, while a video distribution amplifier can output hundreds of milliamps and require extremely low differential gain and phase errors.

The bypassing scheme that is used for the AD8010 requires special attention. It was found that the conventional technique of bypassing each power pin individually to ground can have an adverse effect on the differential phase error of the circuit. The cause of this is attributed to the fact that there is an internal compensation capacitor in the AD8010 that is referenced to the negative supply.

The recommended technique is to connect parallel bypass capacitors from the positive supply to the negative supply and then to bypass the negative supply to ground. For high frequency bypassing, 0.1 μF ceramic capacitors are recommended. These should be placed within a few millimeters of the power pins and should preferably be chip type capacitors.

The high currents that can potentially flow through the power supply pins require large bypassing capacitors. These should be low inductance tantalum types and at least 47 μF. The ground side of the capacitor that bypasses the negative supply should be brought to a single point ground that is the common for the returns of the outputs.

Figure 30 shows a circuit for making an N-channel video distribution amplifier. As a practical matter, the AD8010 can readily drive eight standard 150 Ω video loads. When driving up to 12 video loads, there is minimal degradation in video performance.

Another important consideration when driving multiple cables is the high frequency isolation between the outputs of the cables. Due to its low output impedance, the AD8010 achieves better than 46 dB of output-to-output isolation at 5 MHz driving back terminated 75 Ω cables.

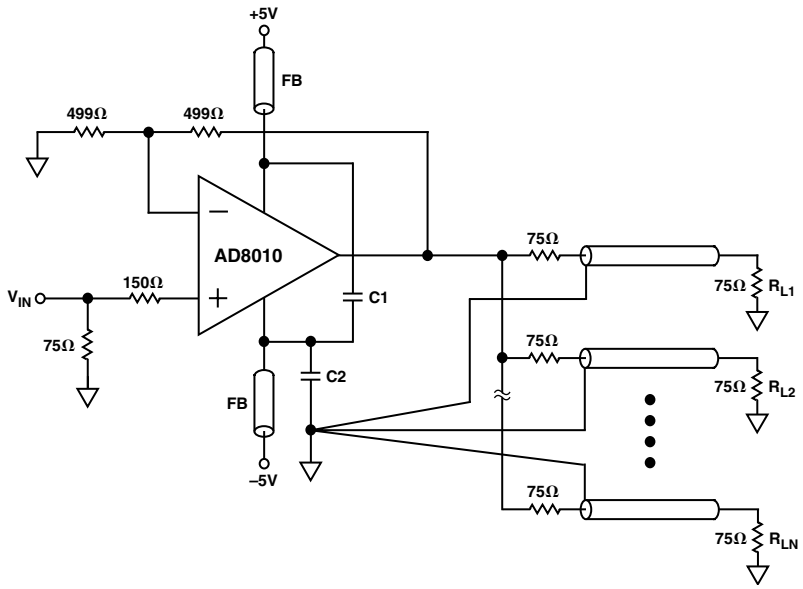


Figure 30. An N-Channel Video Distribution Amplifier Using An AD8010.
NOTE: Please see Figure 29 for Recommended Bypassing Technique.

Differential Line Driver

Twisted pair transmission lines are more often being used for high frequency analog and digital signals. Over long distances, however, the attenuation characteristics of these lines can degrade the performance of the transmission system. To compensate for this, larger signals are transmitted, which after the attenuation, will still have useful signal strength.

The high output current of two AD8010s can be used along with a transformer to create a high power differential line driver. The differential configuration effectively doubles the output swing, while the step-up transformer further increases the output voltage.

In the circuit in Figure 31 the A device is configured as a gain-of-two follower, while the B device is a gain-of-two inverter. These will produce a differential output signal whose maximum value is twice the peak-to-peak value of the maximum output of one device. For this circuit a 12 V peak-to-peak output can be obtained.

The op amps drive a 1:2 step-up transformer that drives a 100 Ω transmission line. Since the impedance reflected back to the primary varies as the square of the turns ratio, it will appear as 25 Ω at the primary. This source terminating resistor is split as a 12.4 Ω resistor at the output of each device.

The circuit shown is capable of delivering 12 V p-p to the line and operates with a –3 dB bandwidth of 40 MHz. The peak current output of either op amp is 100 mA.

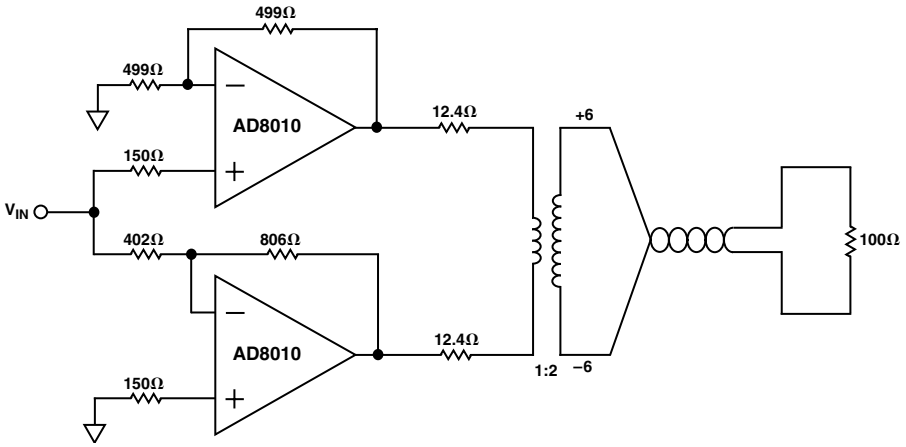


Figure 31. High Output Differential Line Driver Using Two AD8010s.
NOTE: Please see Figure 29 for Recommended Bypassing Technique.

Closed-Loop Gain and Bandwidth

The AD8010 is a current feedback amplifier optimized for use in high performance video and data acquisition applications. Since it uses a current feedback architecture, its closed-loop –3 dB bandwidth is dependent on the magnitude of the feedback resistor. The desired closed-loop bandwidth and gain are obtained by varying the feedback resistor (R_F) to set the bandwidth, and varying the gain resistor (R_G) to set the desired gain. The characteristic curves and specifications for this data sheet reflect the performance of the AD8010 using the values of R_F noted at the top of the specifications table. If a greater –3 dB bandwidth and/or slew rate is required (at the expense of video performance), Table I provides the recommended resistor values. Figure 32 shows the test circuit and conditions used to produce Table I.

Effect of Feedback Resistor Tolerance on Gain Flatness

Because of the relationship between the 3 dB bandwidth and the feedback resistor, the fine scale gain flatness will, to some extent, vary with feedback resistor tolerance. It is therefore recommended that resistors with a 1% tolerance be used if it is desired to maintain flatness over a wide range of production lots. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Metal-film resistors were used for the bulk of the characterization for this data sheet. It is possible that values other than those indicated will be optimal for other resistor types.

Quality of Coaxial Cable

Optimum flatness when driving a coax cable is possible only when the driven cable is terminated at each end with a resistor matching its characteristic impedance. If the coax was ideal, then the resulting flatness would not be affected by the length of the cable. While outstanding results can be achieved using inexpensive cables, it should be noted that some variation in flatness due to varying cable lengths may be experienced.

Table I. –3 dB Bandwidth and Slew Rate vs. Closed-Loop Gain and Resistor Values

Package: N-8

Closed-Loop Gain	R_F (Ω)	R_G (Ω)	–3 dB BW (MHz)	Slew Rate (V/μs)
+1	453	∞	285	900
+2	374	374	255	900
+5	348	86.6	200	800
+10	562	61.9	120	550

Package: R-16

Closed-Loop Gain	R_F (Ω)	R_G (Ω)	–3 dB BW (MHz)	Slew Rate (V/μs)
+1	412	∞	245	900
+2	392	392	220	900
+5	392	97.6	160	800
+10	604	66.5	95	550

Package: SO-8

Closed-Loop Gain	R_F (Ω)	R_G (Ω)	–3 dB BW (MHz)	Slew Rate (V/μs)
+1	392	∞	345	950
+2	374	374	305	1000
+5	348	86.6	220	1000
+10	499	54.9	135	650

1. V_O = 0.2 V p-p for –3 dB Bandwidth.
2. V_O = 2 V p-p for Slew Rate.
3. Bypassing per Figure 29.

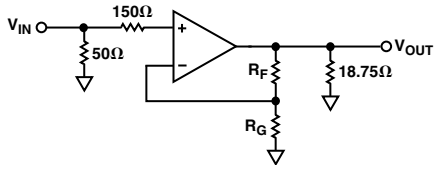
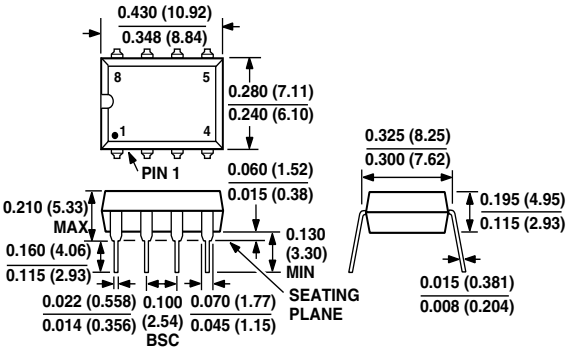


Figure 32. Test Circuit for Table I

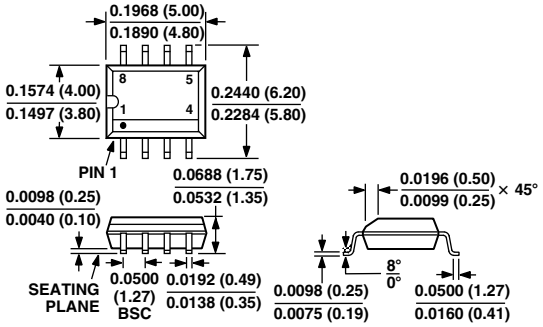
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

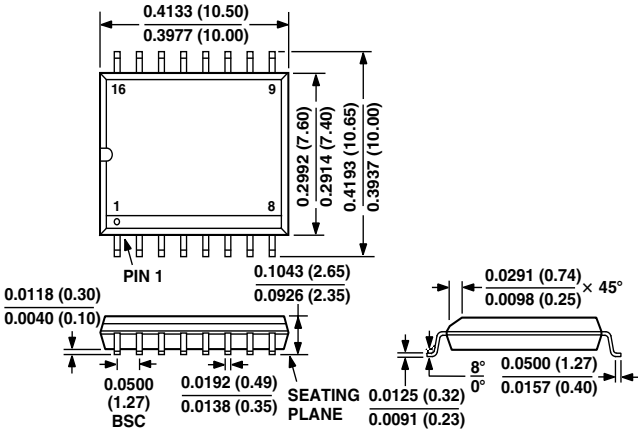
8-Lead Plastic Mini-DIP
(N-8)



8-Lead SOIC
(SO-8)



16-Lead Wide Body SOIC
(R-16)



C01047a–0–12/00 (rev. B)

PRINTED IN U.S.A.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for High Speed Operational Amplifiers ***category:***

Click to view products by Analog Devices ***manufacturer:***

Other Similar products are found below :

NJU7047RB1-TE2 LTC6226IS8#PBF LTC6226HS8#PBF LT1058ACN LT1206CR LT1058ISW THS4222DGNR OPA2677IDDAR THS6042ID THS4221DBVR THS4081CD ADA4858-3ACPZ-R7 LT6202IS5#TRMPBF LT1206CR#PBF LTC6253CMS8#PBF LT1813CDD#PBF ADA4851-4YRUZ-RL LT1037IN8#PBF LTC6401CUD-20#PBF LT1192CN8#PBF LTC6401IUD-26#PBF LT1037ACN8#PBF LTC6253CTS8#TRMPBF LT1399HVCS#PBF LT1993CUD-2#PBF LT6203CDD#PBF LT1722CS8#PBF LT1208CN8#PBF LT1222CN8#PBF LT6203IDD#PBF LT6411IUD#PBF LTC6400CUD-26#PBF LTC6400CUD-8#PBF LT6211IDD#PBF OP27EN8#PBF LT1810IMS8#PBF OP37EN8#PBF LTC6253IMS8#PBF LT1360CS8 OPA2132PAG4 OPA2691I-14D OPA4353UA/2K5 OPA690IDRG4 LMH6723MFX/NOPB 5962-9151901MPA ADP5302ACPZ-3-R7 AD8007AKSZ-REEL7 AD8008ARMZ AD8009JRTZ-REEL7 AD8010ANZ