Low Distortion Differential ADC Driver

AD8138-EP

FEATURES

Adjustable output common-mode voltage
Low harmonic distortion
- **−94 dBc SFDR @ 5 MHz**
- **−85 dBc SFDR @ 20 MHz**
- **−3 dB bandwidth of 320 MHz, G = +1**

Fast settling to 0.01% of 16 ns
Fast overdrive recovery of 4 ns
Low input voltage noise of 5 nV/√Hz
Low power 90 mW on 5 V

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC)
Extended temperature range −55°C to +105°C
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

ADC drivers
Single-ended-to-differential converters
IF and baseband gain blocks
Differential buffers
Line drivers

GENERAL DESCRIPTION

The AD8138-EP is a major advancement over op amps for differential signal processing. The AD8138-EP can be used as a single-ended-to-differential amplifier or as a differential-to-differential amplifier. The AD8138-EP is as easy to use as an op amp and greatly simplifies differential signal amplification and driving. Manufactured on Analog Devices, Inc., proprietary XFCB bipolar process, the AD8138-EP has a −3 dB bandwidth of 320 MHz and delivers a differential signal with the lowest harmonic distortion available in a differential amplifier. The AD8138-EP has a unique internal feedback feature that provides balanced output gain and phase matching, suppressing even order harmonics. The internal feedback circuit also minimizes any gain error that would be associated with the mismatches in the external gain setting resistors.

PIN CONFIGURATION

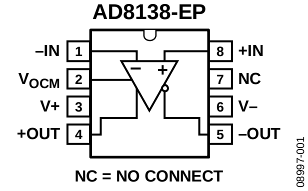

Figure 1.

TYPICAL APPLICATION CIRCUIT

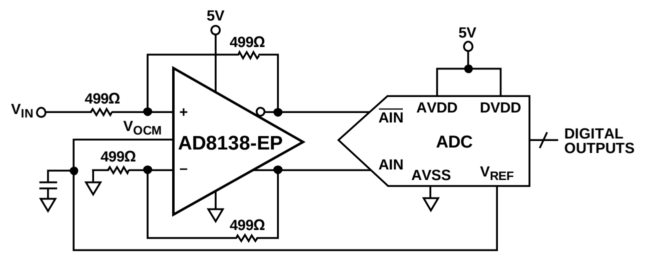

Figure 2.

The AD8138-EP's differential output helps balance the input to the differential ADCs, maximizing the performance of the ADC.

The AD8138-EP eliminates the need for a transformer with high performance ADCs, preserving the low frequency and dc information. The common-mode level of the differential output is adjustable by a voltage on the V_{OCM} pin, easily level-shifting the input signals for driving single-supply ADCs. Fast overload recovery preserves sampling accuracy.

The AD8138-EP distortion performance makes it an ideal ADC driver for communication systems, with distortion performance good enough to drive state-of-the-art 10-bit to 16-bit converters at high frequencies. The AD8138-EP's high bandwidth and IP3 also make it appropriate for use as a gain block in IF and baseband signal chains. The AD8138-EP offset and dynamic performance make it well suited for a wide variety of signal processing and data acquisition applications. The AD8138-EP is available in the MSOP package for operation over −55°C to +105°C temperatures.

Full details about this enhanced product are available in the AD8138 data sheet, which should be consulted in conjunction with this data sheet.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

4/10—Revision 0: Initial Version

SPECIFICATIONS

±D_{IN} TO ±OUT SPECIFICATIONS

At 25°C, V_S = ±5 V, V_{OCM} = 0 V, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.5 V p-p, C_F = 0 pF	290	320		MHz
	T_{MIN} to T_{MAX}[1]	256			MHz
	V_{OUT} = 0.5 V p-p, C_F = 1 pF		225		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, C_F = 0 pF		30		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, C_F = 0 pF		265		MHz
Slew Rate	V_{OUT} = 2 V p-p, C_F = 0 pF		1150		V/μs
Settling Time	0.01%, V_{OUT} = 2 V p-p, C_F = 1 pF		16		ns
Overdrive Recovery Time	V_{IN} = 5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−94		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−87		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		−62		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−114		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−85		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		−57		dBc
IMD	20 MHz		−77		dBc
IP3	20 MHz		37		dBm
Voltage Noise (RTI)	f = 100 kHz to 40 MHz		5		nV/√Hz
Input Current Noise	f = 100 kHz to 40 MHz		2		pA/√Hz
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm} = V_{OUT, dm}/2$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	−2.5	±1	+2.5	mV
	T_{MIN} to T_{MAX}[1]	−4.8		+4.8	mV
Input Bias Current			3.5	7	μA
	T_{MIN} to T_{MAX} variation		−0.01		μA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			−4.7 to +3.4		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V,		−77	−70	dB
	T_{MIN} to T_{MAX}[1]			−69	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing[2]	Maximum ΔV_{OUT}; single-ended output		7.75		V p-p
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V		−66		dB

[1] Specified to ±6 sigma over the −55°C to +105°C operating temperature range.
[2] Output swing capabilities vary over operating temperature. See Figure 4 for more information.

V_{OCM} TO ±OUT SPECIFICATIONS

At 25°C, V_S = ±5 V, V_{OCM} = 0 V, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth			250		MHz
Slew Rate			330		V/μs
INPUT VOLTAGE NOISE (RTI)	f = 0.1 MHz to 100 MHz		17		nV/√Hz
DC PERFORMANCE					
Input Voltage Range			±3.8		V
Input Resistance			200		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	−3.5	±1	+3.5	mV
	T_{MIN} to T_{MAX}[1]	−10.2		+10.2	mV
Input Bias Current			0.5		μA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−75		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V, T_{MIN} to T_{MAX}[1]	0.9955	1	1.0045	V/V
POWER SUPPLY					
Operating Range		±1.4		±5.5	V
Quiescent Current		18	20	23	mA
	T_{MIN} to T_{MAX}[1]	13.2			mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V, T_{MIN} to T_{MAX}[1]		−90	−70	dB
OPERATING TEMPERATURE RANGE		−55		+105	°C

[1] Specified to ±6 sigma over the −55°C to +105°C operating temperature range.

±D_{IN} TO ±OUT SPECIFICATIONS

At 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. All specifications refer to single-ended input and differential output, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.5 V p-p, C_F = 0 pF	280	310		MHz
	T_{MIN} to T_{MAX}[1]	242			MHz
	V_{OUT} = 0.5 V p-p, C_F = 1 pF		225		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, C_F = 0 pF		29		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, C_F = 0 pF		265		MHz
Slew Rate	V_{OUT} = 2 V p-p, C_F = 0 pF		950		V/μs
Settling Time	0.01%, V_{OUT} = 2 V p-p, C_F = 1 pF		16		ns
Overdrive Recovery Time	V_{IN} = 2.5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−90		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−79		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		−60		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−100		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−82		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		−53		dBc
IMD	20 MHz		−74		dBc
IP3	20 MHz		35		dBm
Voltage Noise (RTI)	f = 100 kHz to 40 MHz		5		nV/√Hz
Input Current Noise	f = 100 kHz to 40 MHz		2		pA/√Hz
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm} = V_{OUT, dm}/2$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	−2.5	±1	+2.5	mV
	T_{MIN} to T_{MAX}[1]	−5.1		+5.1	mV
Input Bias Current			3.5	7	μA
	T_{MIN} to T_{MAX} variation		−0.01		μA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			−0.3 to +3.2		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = 1 V		−77	−70	dB
	T_{MIN} to T_{MAX}[1]			−69.5	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing[2]	Maximum ΔV_{OUT}; single-ended output		2.9		V p-p
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V		−65		dB

[1] Specified to ±6 sigma over the −55°C to +105°C operating temperature range.
[2] Output swing capabilities vary over operating temperature. See Figure 5 for more information.

V_{OCM} TO ±OUT SPECIFICATIONS

At 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. All specifications refer to single-ended input and differential output, unless otherwise noted.

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth			220		MHz
Slew Rate			250		V/μs
INPUT VOLTAGE NOISE (RTI)	f = 0.1 MHz to 100 MHz		17		nV/√Hz
DC PERFORMANCE					
Input Voltage Range			1.0 to 3.8		V
Input Resistance			100		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	−5	±1	+5	mV
	T_{MIN} to T_{MAX}[1]	−9.7		+9.7	mV
Input Bias Current			0.5		μA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 V ± 1 V		−70		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 V ± 1 V, T_{MIN} to T_{MAX}[1]	0.9968	1	1.0032	V/V
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current		15	20	21	mA
	T_{MIN} to T_{MAX}[1]	10.6			mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ± 1 V		−90	−70	dB
	T_{MIN} to T_{MAX}[1]			−57	dB
OPERATING TEMPERATURE RANGE		−55		+105	°C

[1] Specified to ±6 sigma over the −55°C to +105°C operating temperature range.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	±5.5 V
V_{OCM}	$\pm V_S$
Output Voltage Swing	See Figure 4 and Figure 5
Internal Power Dissipation	550 mW
Operating Temperature Range	−55°C to +105°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 6.

Package Type	θ_{JA}	Unit
8-Lead MSOP/4-Layer	145	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8138-EP package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8138-EP. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The load current consists of the differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a negligible differential load on the output. RMS voltages and currents should be considered when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation vs. the ambient temperature for the 8-lead MSOP (θ_{JA} = 145°C/W) package on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

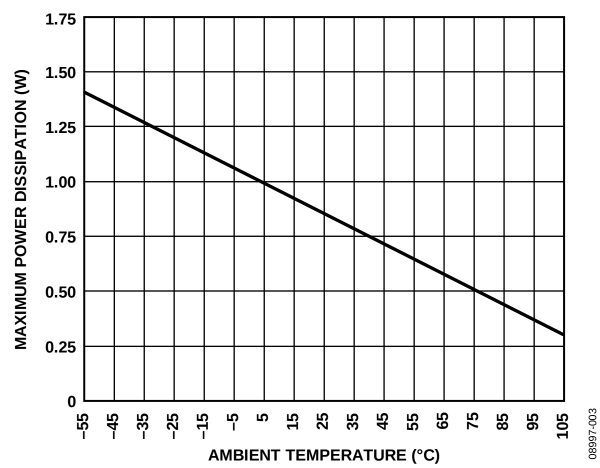
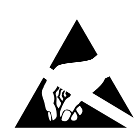


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM OUTPUT VOLTAGE SWING

The maximum output voltage swing must be considered in order for the AD8138-EP to remain current density compliant over the extended temperature range. The maximum output swing is dependent on the load resistance and operating temperatures. Figure 4 shows the maximum output swing over operating temperatures for various loads at ±5 V operation.

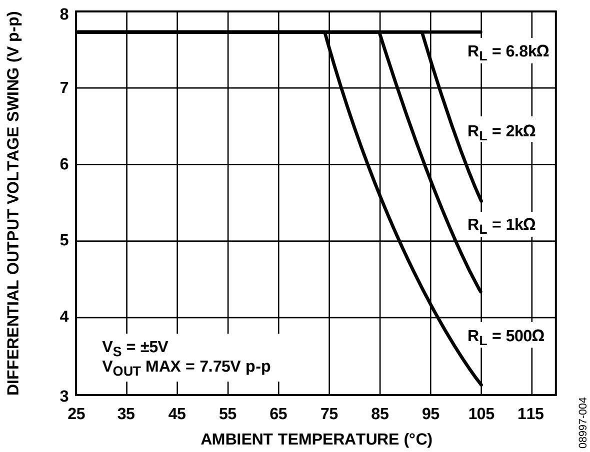


Figure 4. Differential Output Voltage Swing vs. Ambient Temperature, V_S = ±5 V

The following equation can be used to determine the maximum output voltage swing for V_S = ±5 V:

$$Output = (38.21 \times ln(R_L) - 169.26) \times e^{(-0.0293 \times T_A)}$$

where:
Output is the maximum output voltage swing that cannot exceed 7.75 V p-p.
R_L is the load resistance (Ω).
T_A is the ambient temperature (°C).

Figure 5 shows the maximum output swing over operating temperatures for various loads at V_S = 5 V operation.

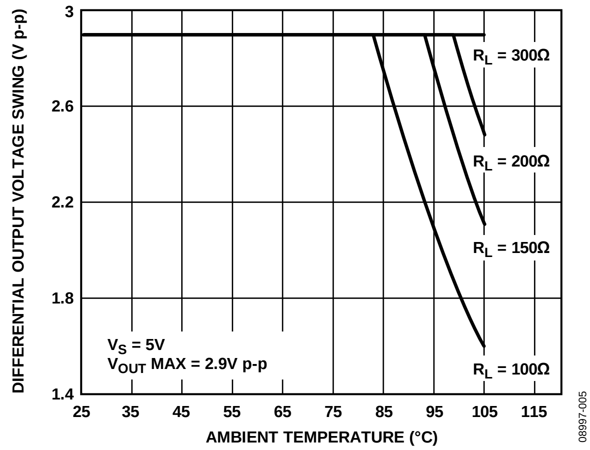


Figure 5. Differential Output Voltage Swing vs. Ambient Temperature, V_S = 5 V

The following equation can be used to determine the maximum output voltage swing for V_S = 5 V:

$$Output = (24.36 \times ln(R_L) - 82.34) \times e^{(-0.028 \times T_A)}$$

where:
Output is the maximum output voltage swing that cannot exceed 2.9 V p-p.
R_L is the load resistance (Ω).
T_A is the ambient temperature (°C).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

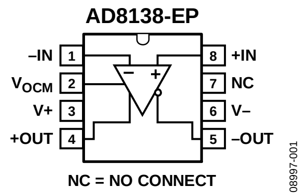


Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input Summing Node.
2	V_{OCM}	Voltage applied to this pin sets the common-mode output voltage with a ratio of 1:1. For example, 1 V dc on V_{OCM} sets the dc bias level on +OUT and −OUT to 1 V.
3	V+	Positive Supply Voltage.
4	+OUT	Positive Output. Note that the voltage at $-D_{IN}$ is inverted at +OUT.
5	−OUT	Negative Output. Note that the voltage at $+D_{IN}$ is inverted at −OUT.
6	V−	Negative Supply Voltage.
7	NC	No Connect.
8	+IN	Positive Input Summing Node.

OUTLINE DIMENSIONS

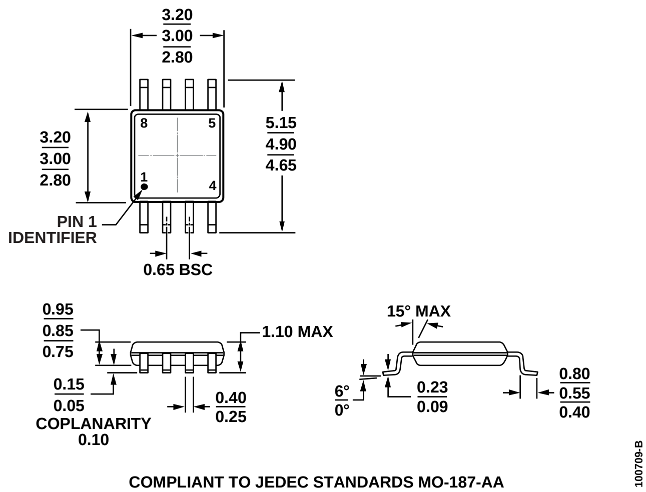


Figure 7. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8138SRMZ-EP-R7	−55°C to +105°C	8-Lead MSOP, 7" Tape and Reel	RM-8	H27

[1] Z = RoHS Compliant Part.

NOTES

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